$$\mathbf{I} = (\text{NumIter}_{in}, \text{NumIter}_{out})$$

$$\mathbf{S}_t(\mathbf{I}) = Tsw_{in} * \text{NumIter}_{in} * \text{NumIter}_{out} + Tsw_{out} * \text{NumIter}_{out}$$

$$\mathbf{H}_t(\mathbf{I}) = Thw_{in} * \text{NumIter}_{in} * \text{NumIter}_{out} + Thw_{out} * \text{NumIter}_{out}$$

Constant Coefficients

Tsw_{out}, Tsw_{in} : CPU execution time for instructions in the outer and inner loop

Thw_{out}, Thw_{in} : FPGA accelerator execution time for operations in the outer and inner loop

Dt : Time to perform SW_{check} or HW_{check}

Run time variables

NumIter_{in}, NumIter_{out} : Number of iterations for each loop level, computed from register/stack variables