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NOTES:						REV	DATE	PAGES		DESCRIPTION	
Project Drawing Numbers:						A B	24/08/2010 28/09/2010	All 3	Rev A F	Release Release, LVDS Pair Swap	
Raw PCB	100-0310902-B1						28/09/2010		nev b r	nelease, LVDS Fall Swap	
Gerber Files PCB Design Files	110-0310902-B1 120-0310902-B1					\vdash	<u> </u>		+		
Assembly Drawing	130-0310902-B1								1		
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Schematic Design Files	180-0310902-B1								1		
Functional Specification PCB Layout Guidelines	210-0310902-B1 220-0310902-B1								$\pm -$		
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			Push Use	er GPIO					1	Title, Notes, Block Diagram, Revision Histor	у
			Buttons LED	Os Header 2					2	CPLD Package Top	\Box
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					-				4	EEPROMs, GPIO Header	7
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3.3V

I²C x2

EEPROM

EEPROM

X1

1.2-3.3V

1.2-3.3V

X36

B2

1.2-3.3V

Motor

Header 1

MAX'V

EP5M570ZF256N

1.2-3.3V

Motor

Header 2

Sense

Buttons

Speaker

GPIO

Header 1

27 28 29 Altera Corporation, Plot 6, Bayan Lepas Technoplex,11900 Penang MAX V CPLD Development Kit Board Rev 0.1 150-0310902-B1 (6XX-43366R)

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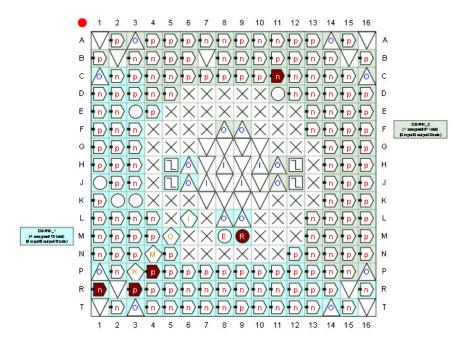
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CPLD Package Top View

Top View - Wire Bond MAX V - 5M570ZF256C5





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