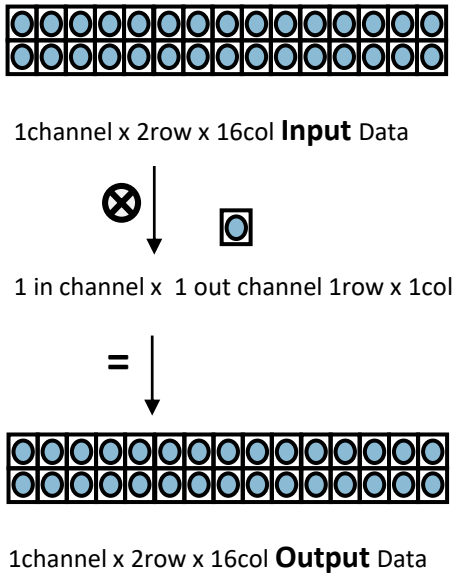

(a) A simplest example.
Two lines of output are calculated by instruction 3 and 7.

DDR

0x0000	Input
…	
0x1000	Weight
…	
0x2000	Output
…	

On-Chip Cache

0x4000	Input
…	
0x5000	Weight
…	
0x6000	Output
…	

(b) Addr Map of DDR and Cache

	Type	Address1	Address2	Address3	Workload	Virtual	SaveID
1	LOAD_W	0x1000	0x5000	-	0x1	2'b00	1
2	LOAD_D	0x0000	0x4000	-	0x20	2'b00	1
3	CALC_F	0x4000	0x6000	0x5000	0x10	2'b00	1
4	SAVE	0x2000	0x6000	-	0x10	2'b01	1
5	LOAD_W	0x1000	0x5000	-	0x1	2'b10	1
6	LOAD_D	0x0010	0x4010	-	0x10	2'b10	1
7	CALC_F	0x4010	0x6010	0x5000	0x10	2'b00	1
8	SAVE	0x2000	0x6000	-	0x20	2'b00	1

(c) Input Instruction Sequence

	Type	Address1	Address2	Address3	Workload
1	LOAD_W	0x1000	0x5000	-	0x1
2	LOAD_D	0x0000	0x4000	-	0x20
3	CALC_F	0x4000	0x6000	0x5000	0x10
4	SAVE	0x2000	0x6000	-	0x20
5	LOAD_W	0x1000	0x5000	-	0x1
6	LOAD_D	0x0010	0x4010	-	0x10
7	CALC_F	0x4010	0x6010	0x5000	0x10
8	SAVE	0x2010	0x6010	-	0x10

(d) Executed Sequence When No Interrupt.
Virtual Instr are deleted.

	Type	Address1	Address2	Address3	Workload
1	LOAD_W	0x1000	0x5000	-	0x1
2	LOAD_D	0x0000	0x4000	-	0x20
3	CALC_F	0x4000	0x6000	0x5000	0x10
4	SAVE	0x2000	0x6000	-	0x10
	HIGH-PRIORITY CNN				
5	LOAD_W	0x1000	0x5000	-	0x1
6	LOAD_D	0x0010	0x4010	-	0x10
7	CALC_F	0x4010	0x6010	0x5000	0x10
8	SAVE	0x2010	0x6010	-	0x10

(e) Executed Sequence When Interrupt Occurs.
Virtual Instr (**Blue**) are executed.
Normal SAVE (**Red**) are modified.