10uF 50V 1206 Samsung: CL31B106KBHNNNE

10uF Tantalum 35V caseB KYOCERA AVX : TCJB106M035R0200

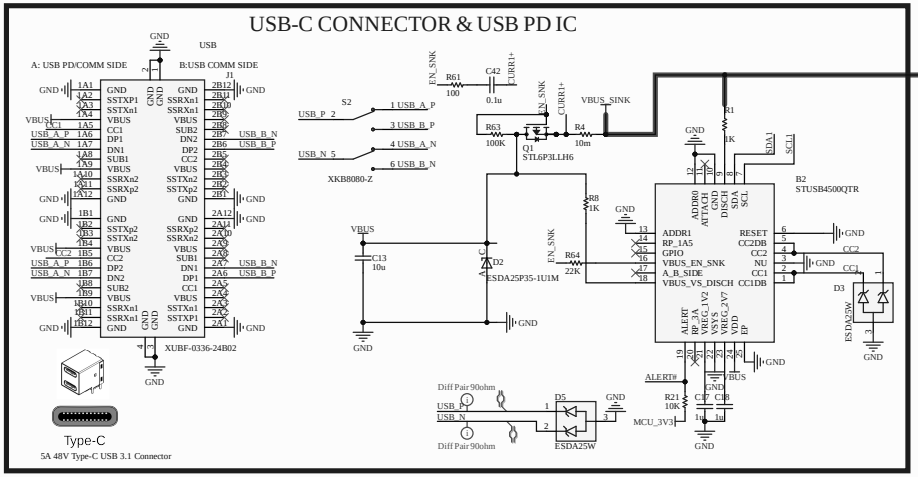
1u 50V 0603 Murata:GRT188R61H105ME 13D

0.1u 50V 0603 Murata: GCJ188R71H104K A12D

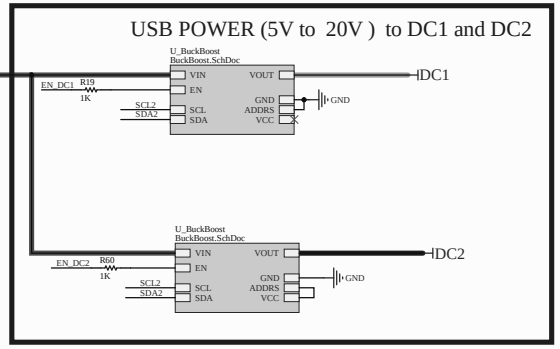
8p 50V 0603 FH: 0603CG8R0C500NT

When the LDO bypass jumper is enabled, the DC1 rail can bypass the 1.8 V or 2.5 V LDO regulators and be driven directly from the main converter. This allows DC1 to output any voltage between 0.8 V and 22 V through the standard output terminals.This feature is referred to as Hacky Mode and is intended for advanced users who need an additional high-voltage output channel.However, when this mode is enabled, the remaining LDO rail (for example, 2.5 V if 1.8 V is bypassed, or vice-versa) is still connected to the DC1 line. Drawing high current from that LDO while DC1 is running at a higher voltage may cause the LDO to enter thermal shutdown or current limit.Therefore, in this mode, the unused LDO rail must not be heavily loaded.This mode should only be used by users who fully understand the implications and internal power routing.

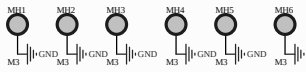
USB-C CONNECTOR & USB PD IC



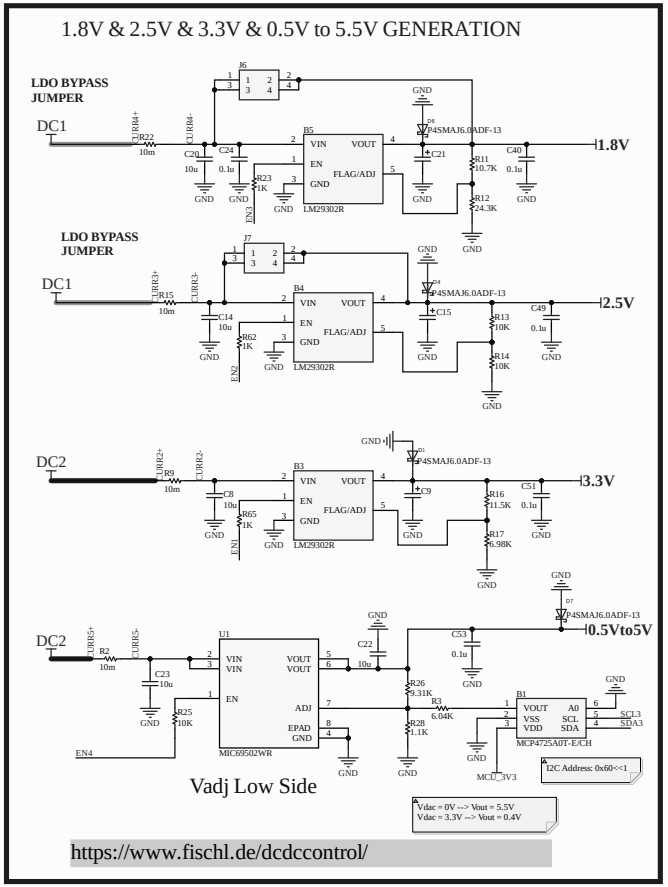
USB POWER (5V to 20V) to DC1 and DC2



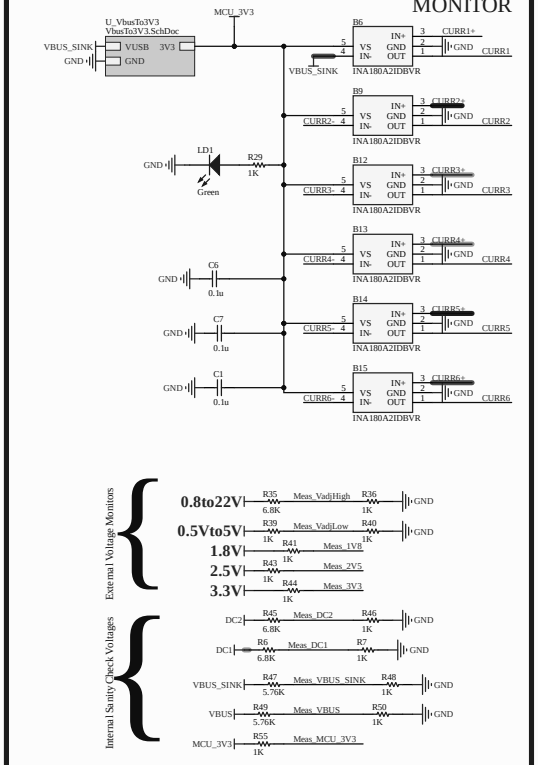
MOUNTING HOLEs



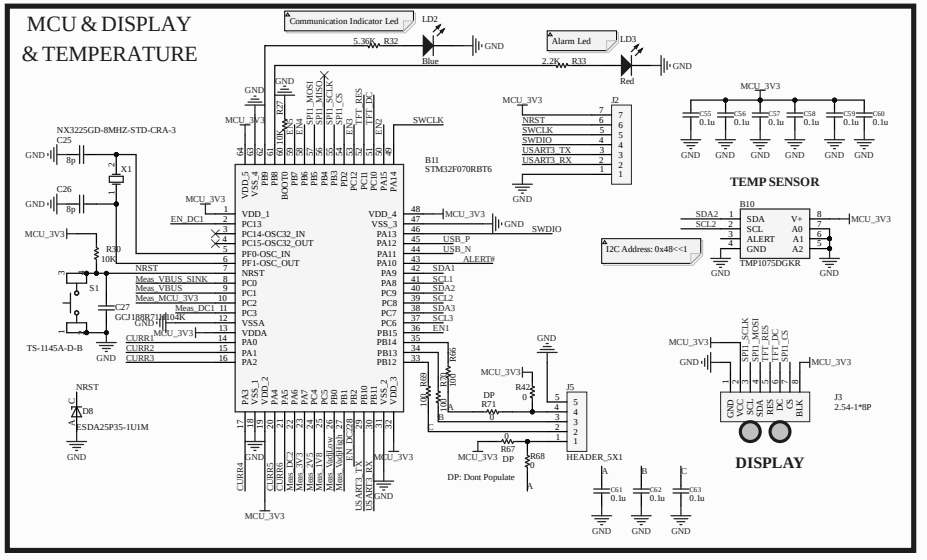
1.8V & 2.5V & 3.3V & 0.5V to 5.5V GENERATION



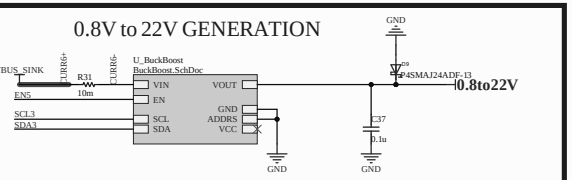
INTERNAL 3.3V GEN & CURRENT and VOLTAGE MONITOR



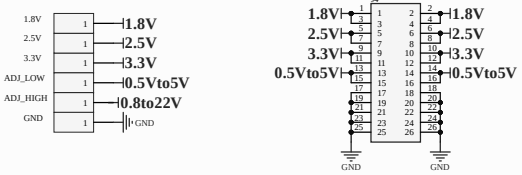
MCU & DISPLAY & TEMPERATURE



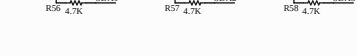
0.8V to 22V GENERATION



BANANA & HEADER



I2C PULLUPs



STEP-UP / STEP-DOWN CONVERSION

0.01u 50V 0402 TDK: CGA2B3X7R1H103K 050BB

0.1u 50V 0402 Murata: GRM155R71H104M E14D

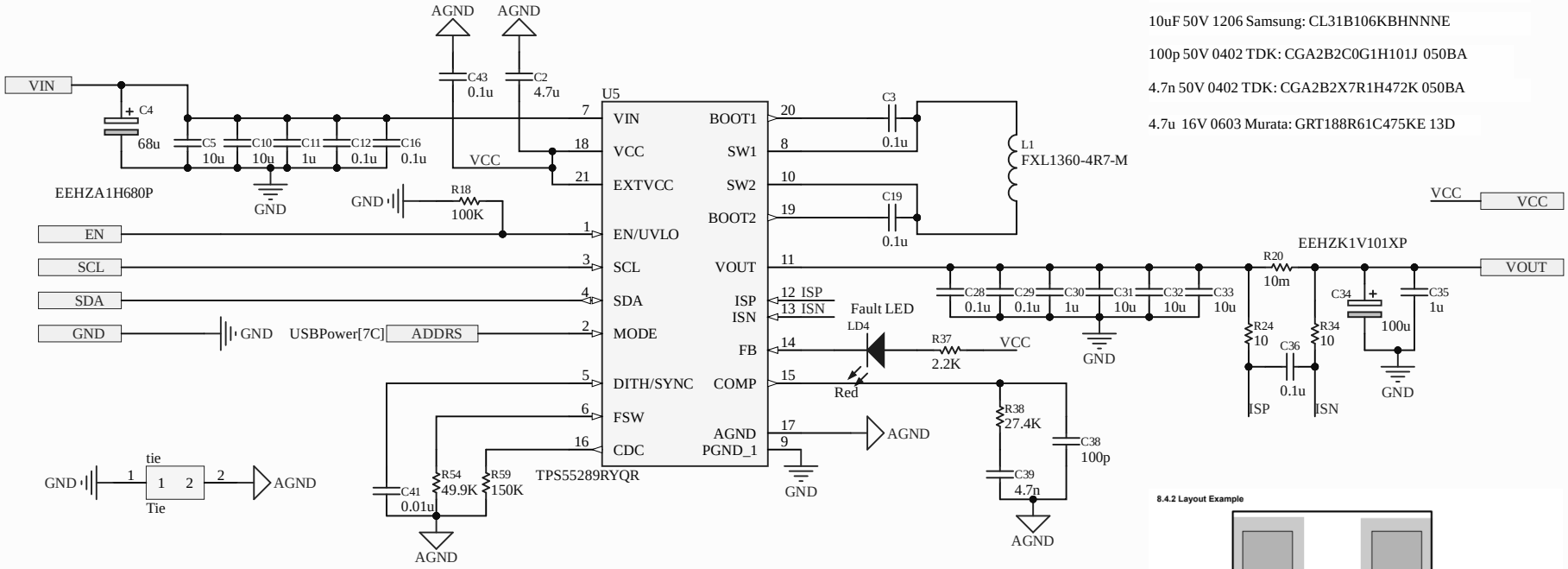
1u 50V 0603 Murata:GRT188R61H105ME 13D

10uF 50V 1206 Samsung: CL31B106KBHNNNE

100p 50V 0402 TDK: CGA2B2C0G1H101J 050BA

4.7n 50V 0402 TDK: CGA2B2X7R1H472K 050BA

4.7u 16V 0603 Murata: GRT188R61C475KE 13D



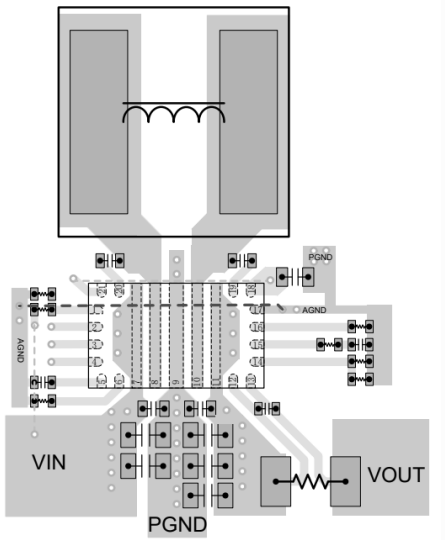
8.4 Layout

8.4.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If layout is not carefully done, the regulator can suffer from instability and noise problems.

1. Place the 0.1-µF small package (0402) ceramic capacitors close to the VIN/VOUT pins to minimize high frequency current loops, which improves the radiation of high-frequency noise (EMI) and efficiency.
2. Use multiple GND vias near PGND pin to connect the PGND to the internal ground plane, which also improves thermal performance.
3. Minimize the SW1 and SW2 loop areas as these are high dv/dt nodes. Use a ground plane under the switching regulator to minimize interplane coupling.
4. Use Kelvin connections to RSENSE for the current sense signals ISP and ISN and run lines in parallel from the RSENSE terminals to the IC pins. Place the filter capacitor for the current sense signal as close to the IC pins as possible.
5. Place the BOOT1 bootstrap capacitor close to the IC and connect directly to the BOOT1 to SW1 pins. Place the BOOT2 bootstrap capacitor close to the IC and connect directly to the BOOT2 and SW2 pins.
6. Place the VCC capacitor close to the IC with wide and short trace. The GND terminal of the VCC capacitor is directly connected with PGND plane through three to four vias.
7. Isolate the power ground from the analog ground. The PGND plane and AGND plane are connected at the terminal of the VCC capacitor. Thus the noise caused by the MOSFET driver and parasitic inductance does not interface with the AGND and internal control circuit.
8. Place the compensation components as close to the COMP pin as possible. Keep the compensation components, feedback components, and other sensitive analog circuitry far away from the power components, switching nodes SW1 and SW2, and high-current trace to prevent noise coupling into the analog signals.
9. To improve thermal performance, it is recommended to use thermal vias beneath the TPS552892 connecting the VIN pin to a large VIN area, and the VOUT pin to a large VOUT area separately.

8.4.2 Layout Example



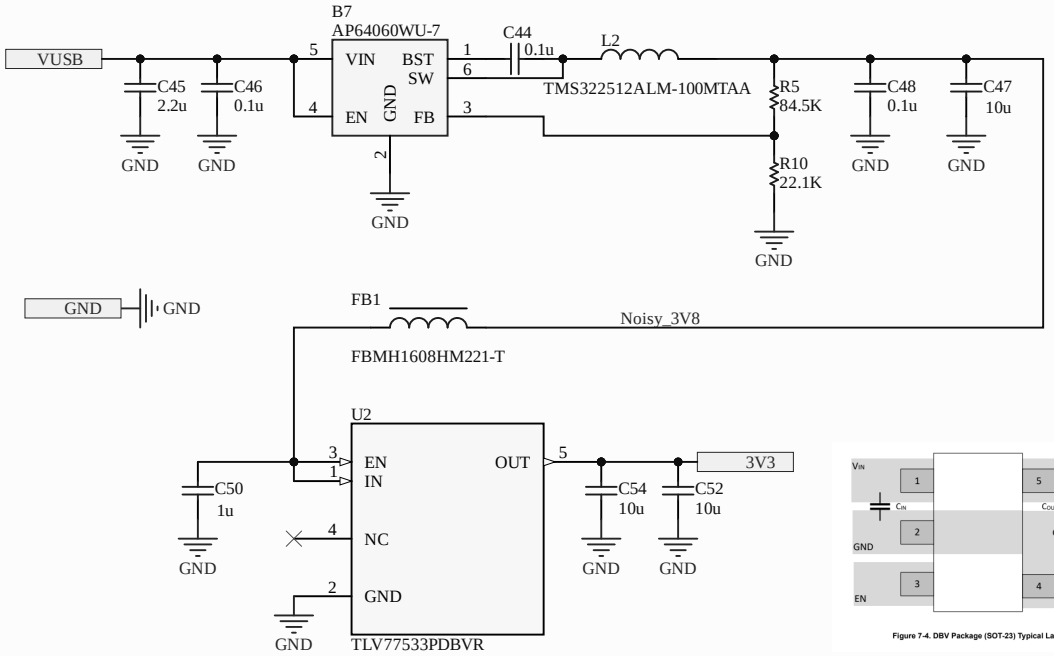
0.1u 50V 0603 Murata: GCJ188R71H104K A12D

1u 50V 0603 Murata:GRT188R61H105ME 13D

2.2u 50V 1206 Murata: GCM31CR71H225K A55L

10uF 50V 1206 Samsung: CL31B106KBHNNNE

VUSB (5V to 20V) to 3.3V



Layout

PCB Layout

1. The AP64060/AP64062 works at 600mA load current so heat dissipation is a major concern in the layout of the PCB. 2oz copper for both the top and bottom layers is recommended.
2. Place the input capacitors as closely across VIN and GND as possible.
3. Place the inductor as close to SW as possible.
4. Place the output capacitors as close to GND as possible.
5. Place the feedback components as close to FB as possible.
6. If using four or more layers, use at least the 2nd and 3rd layers as GND to maximize thermal performance.
7. Add as many vias as possible around both the GND pin and under the GND plane for heat dissipation to all the GND layers.
8. Add as many vias as possible around both the VIN pin and under the VIN plane for heat dissipation to all the VIN layers.
9. See Figure 26 for more details.

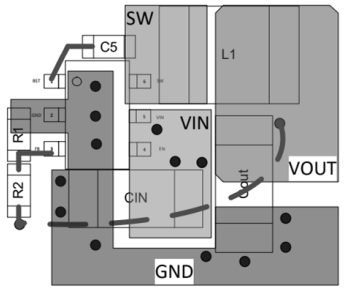


Figure 26. Recommended PCB Layout

Figure 7-4. DBV Package (SOT-23) Typical Layout