

Department of Electrical and Computer Engineering

Course Number	ELE504-02L
Course Title	Electric Circuits II
Semester/Year	Fall/2023

Instructor	Dr. Kassam, TA: Ian Perczak
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Assignment #	1
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Assignment Title	Operational Amplifier Circuits (review)
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Submission Date	Sept 10, 2023
Due Date	Sept 11, 2023

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*By signing above you attest that you have contributed to this written lab report and confirm that all work you have contributed to this lab report is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a "0" on the work, an "F" in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at: www.ryerson.ca/senate/current/pol60.pdf.



ELE504 Laboratory #1

Electrical Engineering

Prepared by Dr. M. S. Kassam. © Toronto Metropolitan University, 2022.

Select Operational Amplifier Circuits (Review)

1.0 PREAMBLE:

The most important single linear Integrated Circuit (IC) is the Operational Amplifier (**Op-Amp**). Op-Amps are among the most widely used building blocks for design of wide variety of linear and non-linear signal processing functions. One of the key reasons for this is that Op-Amps are nearly *ideal voltage amplifiers*, which makes the analysis and design of many Op-Amp based circuits to be simple and straightforward. *The purpose of this lab exercise is to do reviews of some select ideal Op-Amp based circuit configurations (beyond ELE302 course) that should help to better understand building-block concepts for some advanced linear/non-linear circuits to be covered later in this course*

2.0 OBJECTIVE(S):

To analyze, simulate and investigate the characteristics of Op-Amp circuit configurations such as a basic comparator, buffers, and switched “polarity inversion” converter.

3.0 Pre-Lab ASSIGNMENT – Analysis & Simulations

Note: For the parameter variables in the circuits shown in **BLUE**, you must use the values provided to you by your Lab TA. Zero mark will be awarded for use of incorrect parameter value.

Assigned Parameters:

$$V_i = 5V \text{ peak@ } 200\text{Hz}$$

3.01

Pre-Lab ANALYSIS

- (a) For the Op-Amp circuit of **Figure 1**, assume V_i to be a sinusoidal signal [= $V_p \cos(2\pi f_0 t)$], and the Op-Amp output saturation voltage limit is at $(\pm)14V$ when $(\pm)15V$ d.c. power supplies are used for the 741 Op-amp. If the d.c. threshold voltage is V_{TH} , what will be the value of the output voltage, V_o when V_i is below V_{TH} ?, and when it is above V_{TH} ? Why? Neatly sketch and label the $V_i(t)$ waveform and the resultant $V_o(t)$ waveform over at least 2 period cycles.

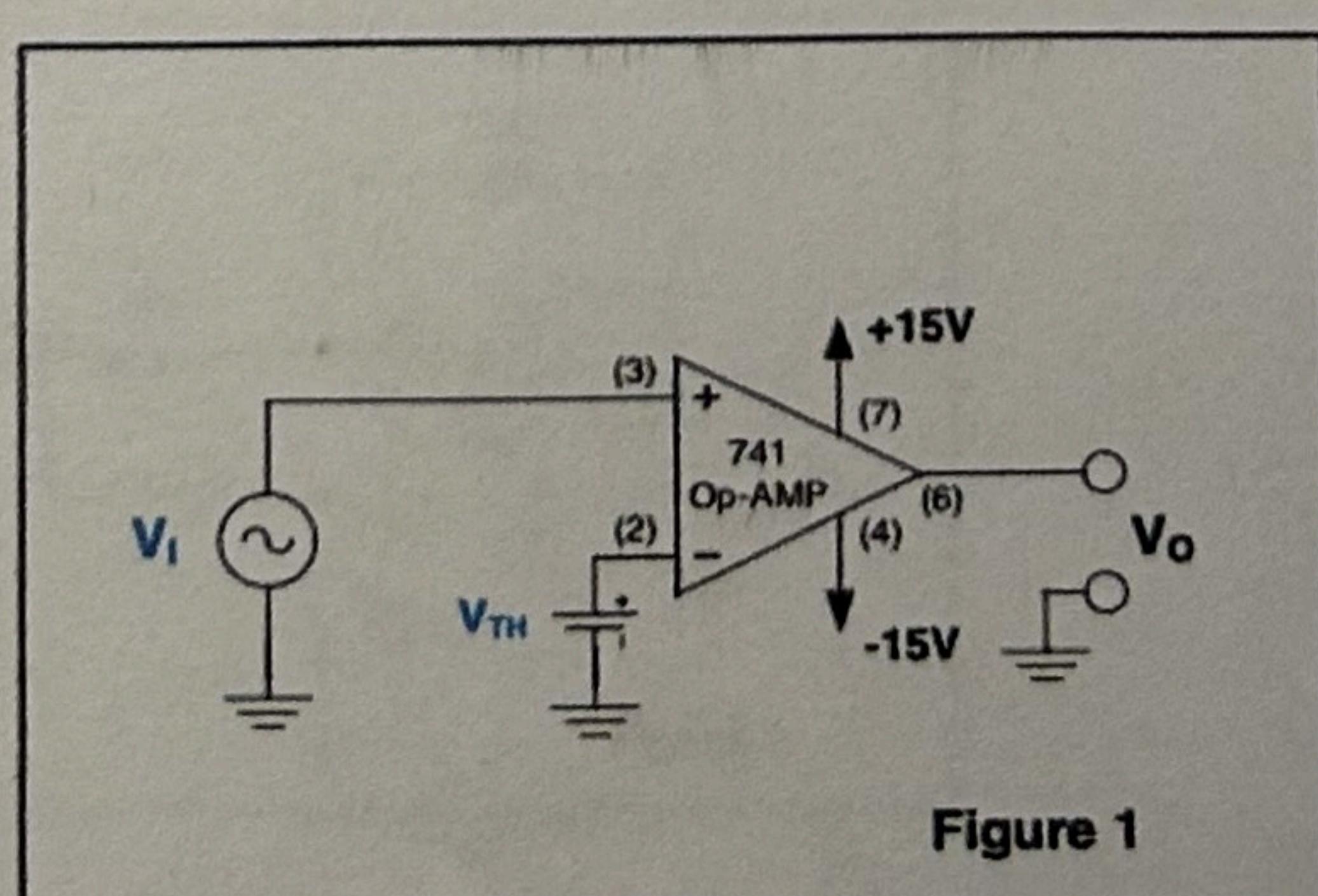
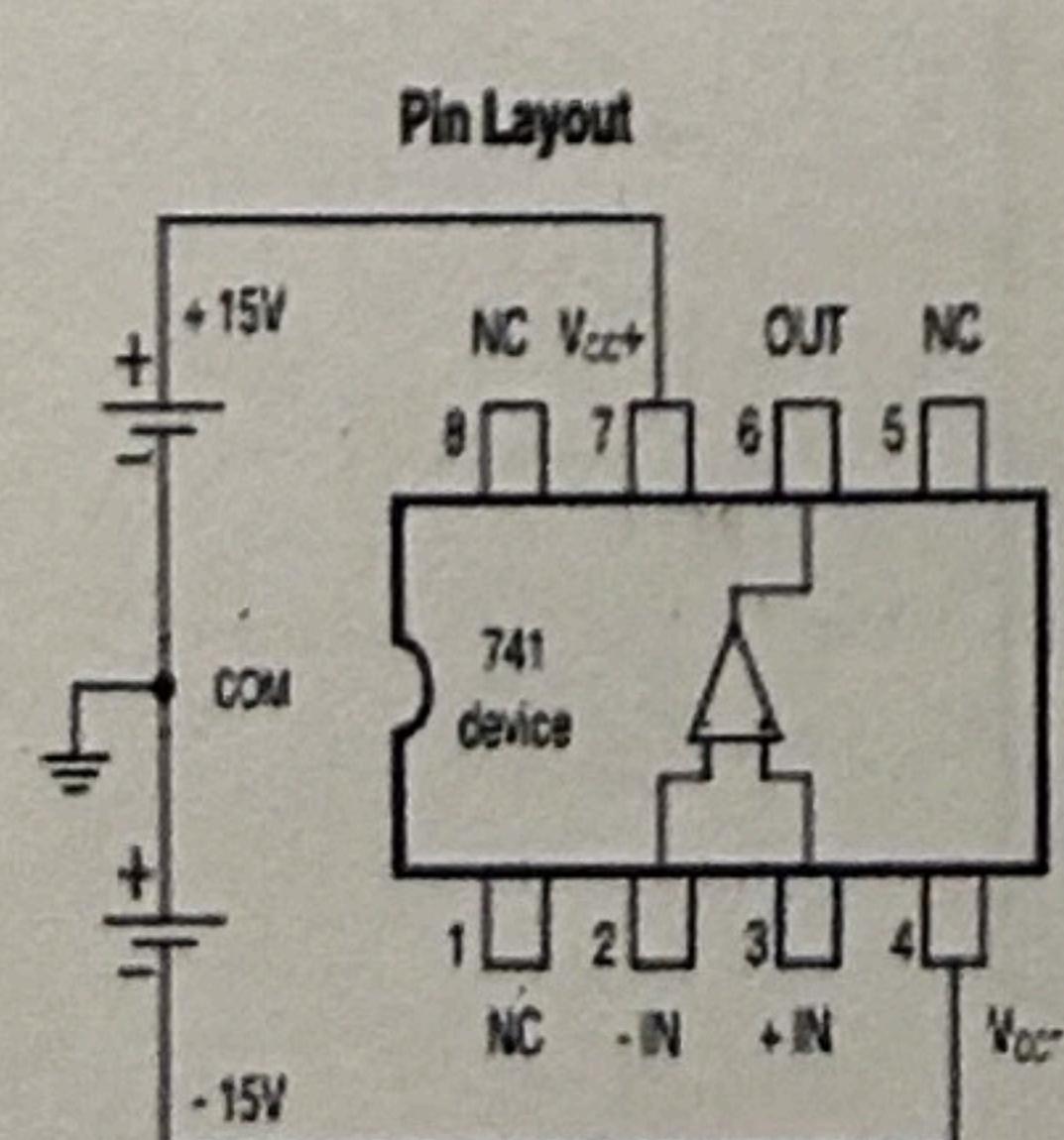
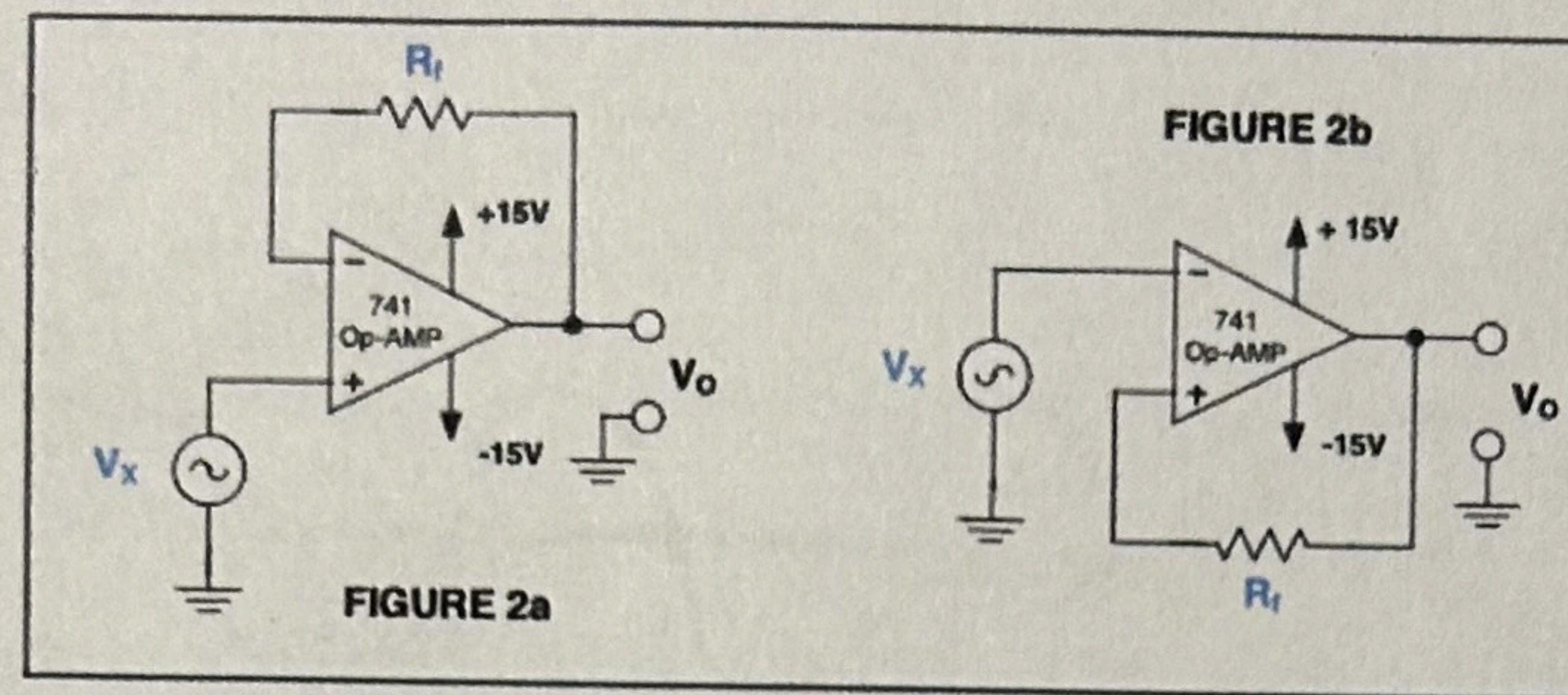


Figure 1

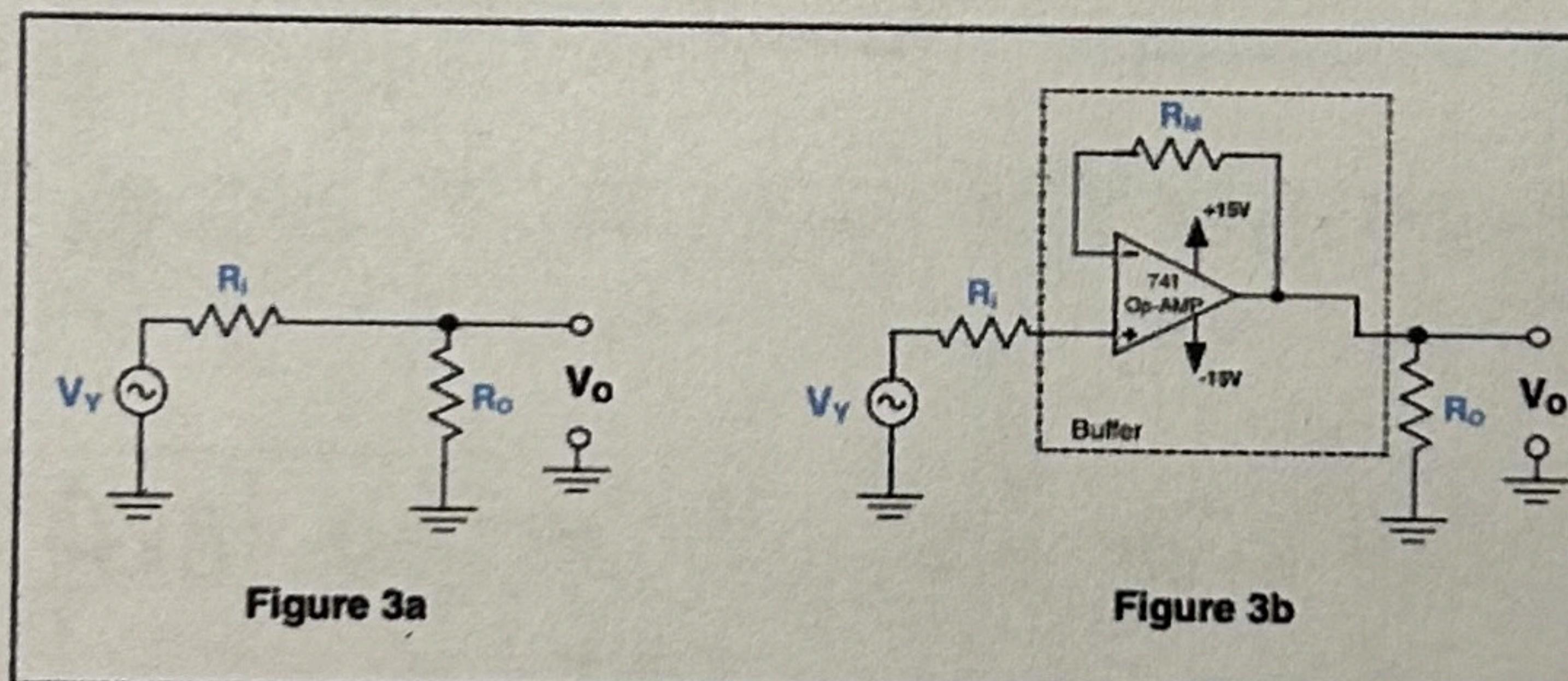
$$\begin{aligned} R_f &= 100k\Omega \\ R_V &= 10k\Omega \\ R_x &= 1k\Omega \\ R_o &= 2k\Omega \\ R_M &= 100k\Omega \end{aligned}$$



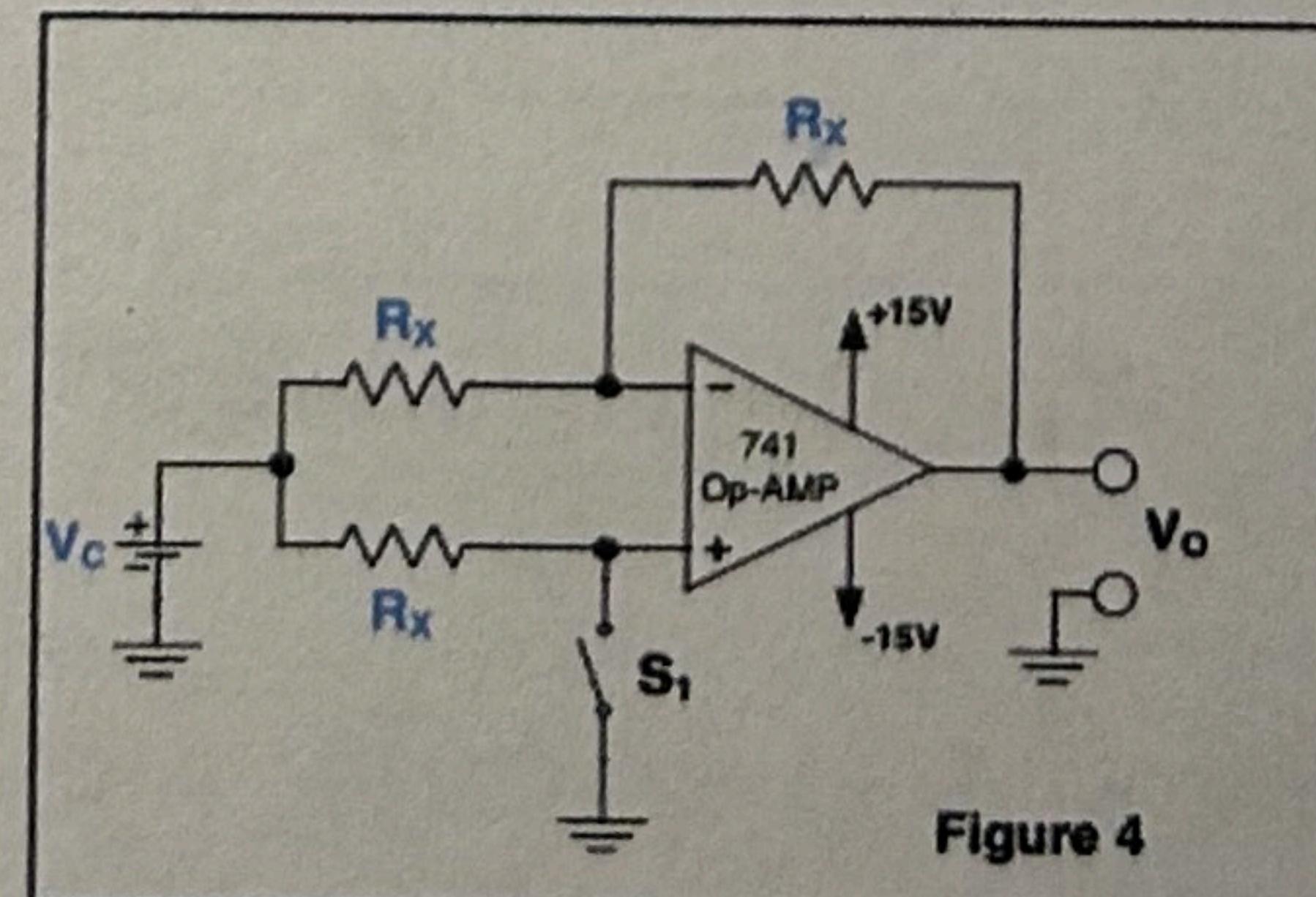
- (b) For the non-inverting “Buffer” circuit of **Figure 2a**, assume input signal, V_x to be a sinusoidal signal [= $V_{x\text{peak}} \cos(2\pi f_0 t)$], and the Op-Amp output saturation voltage limit is at (+/-)14V. Determine the expression of the output voltage, $V_o(t)$ with the provided R_f value? If the designer mistakenly reverses the polarity of the input terminals of this “Buffer” circuit as in **Figure 2b**, explain the effect this change will have on the performance of the Op-Amp circuit? For each circuit, neatly sketch and label the $V_i(t)$ waveform and the resultant $V_o(t)$ waveform over at least 2 period cycles.



- (c) For *each* of the circuit shown in **Figure 3a** and **Figure 3b**, derive the voltage gain, V_o/V_y with the values R_i , R_o , and R_M as provided; and answer the following questions:
(i) Should the voltage gains (V_o/V_y) be the same for both circuits? Why?
(ii) what advantage is there, if any, of using a “Buffer” in **Figure 3b**? and (iii) does the actual value of R_M matter to the voltage gain of **Figure 3b** circuit? Why?



- (d) For the Op-Amp circuit of Figure 4 with the V_c and R_x values as provided, determine the value of V_o , when Switch (S_1) is CLOSED; and when Switch (S_1) is OPEN? What function does this circuit perform?



Prelab #1

①

a) *Assume op-amp is ideal, $\therefore A \gg 1$

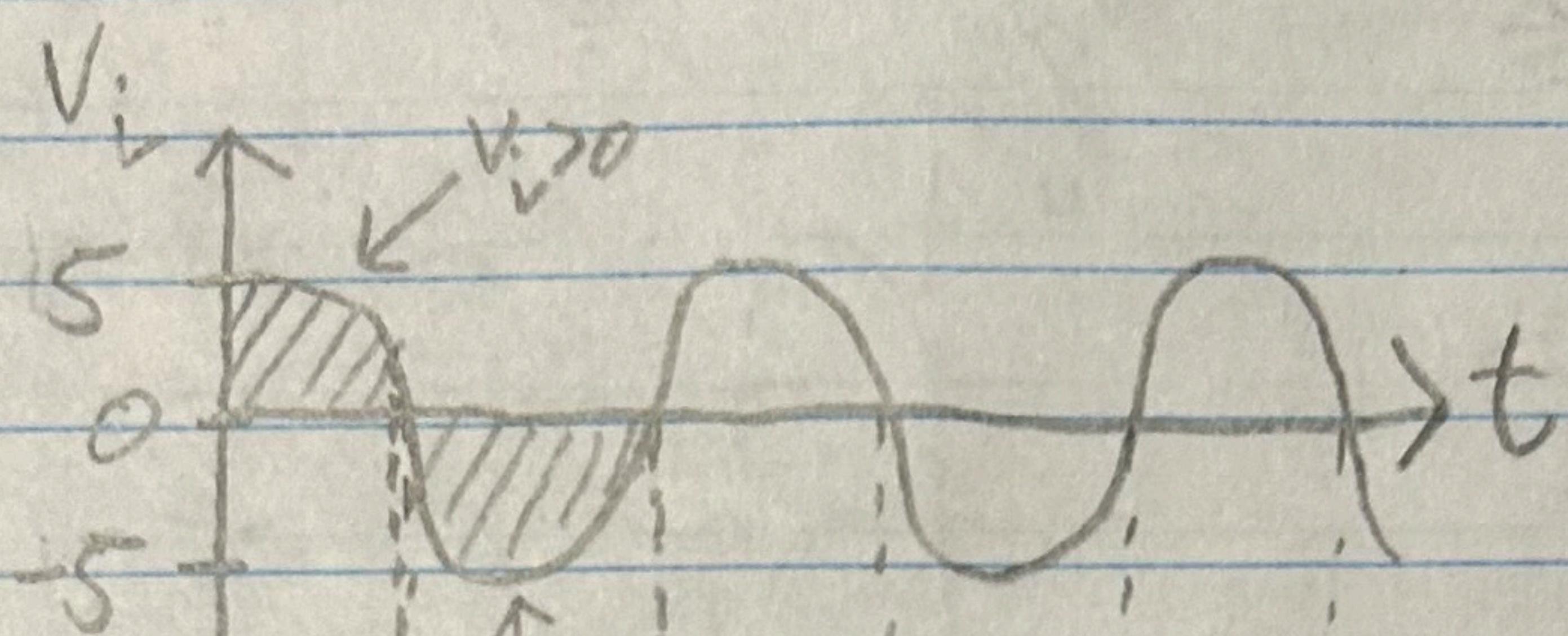
$$V_o = A \cdot \Delta V$$

$$= \infty \cdot [(V^+) - (V^-)]$$

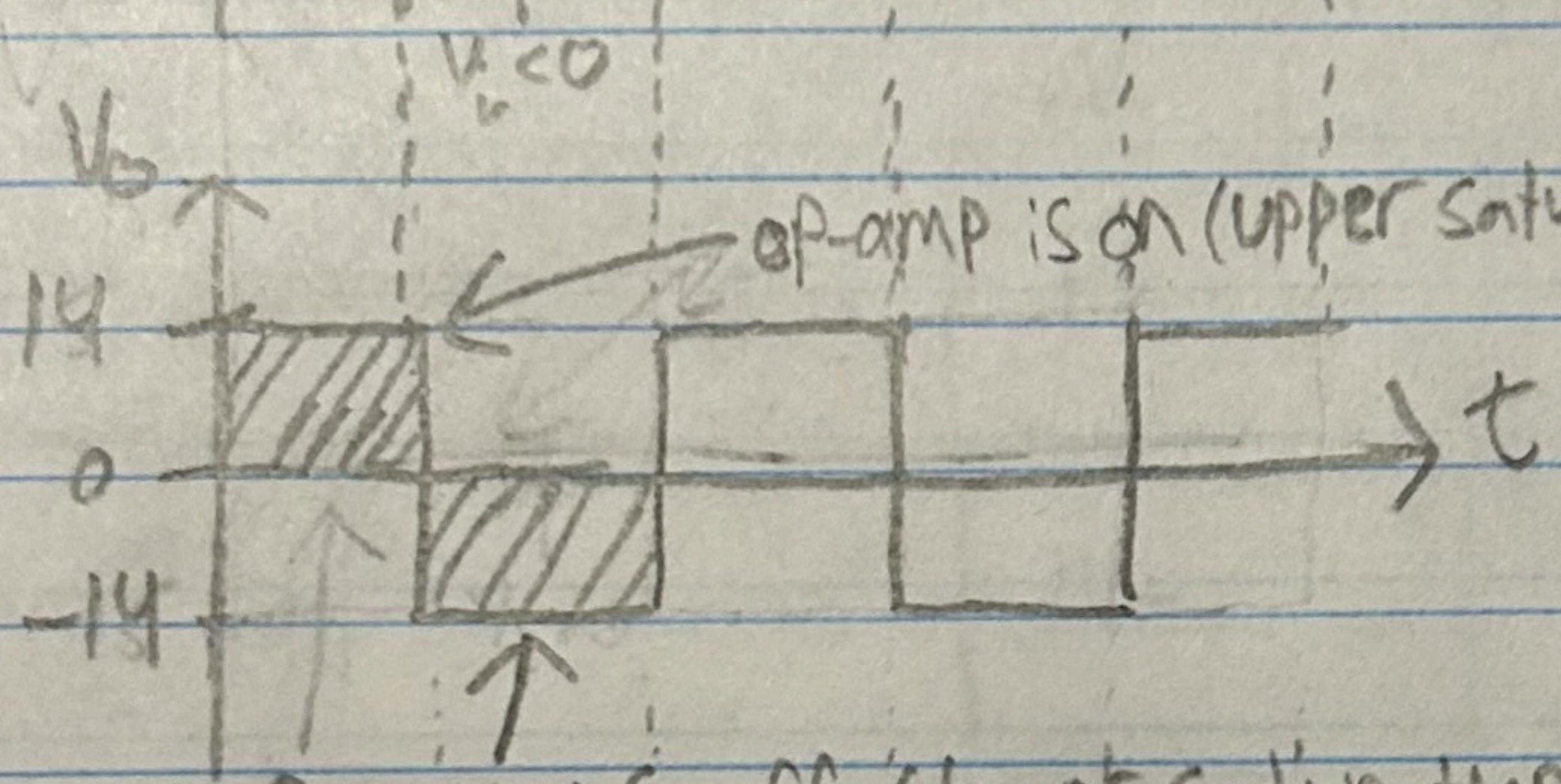
Since it's in open-loop mode (no feedback)
op-amp can have only 2 states:

$$\Delta V > 0 \rightarrow V_o = L^+$$

$$\Delta V < 0 \rightarrow V_o = L^-$$



\therefore when



op-amp is on (upper saturation limit)

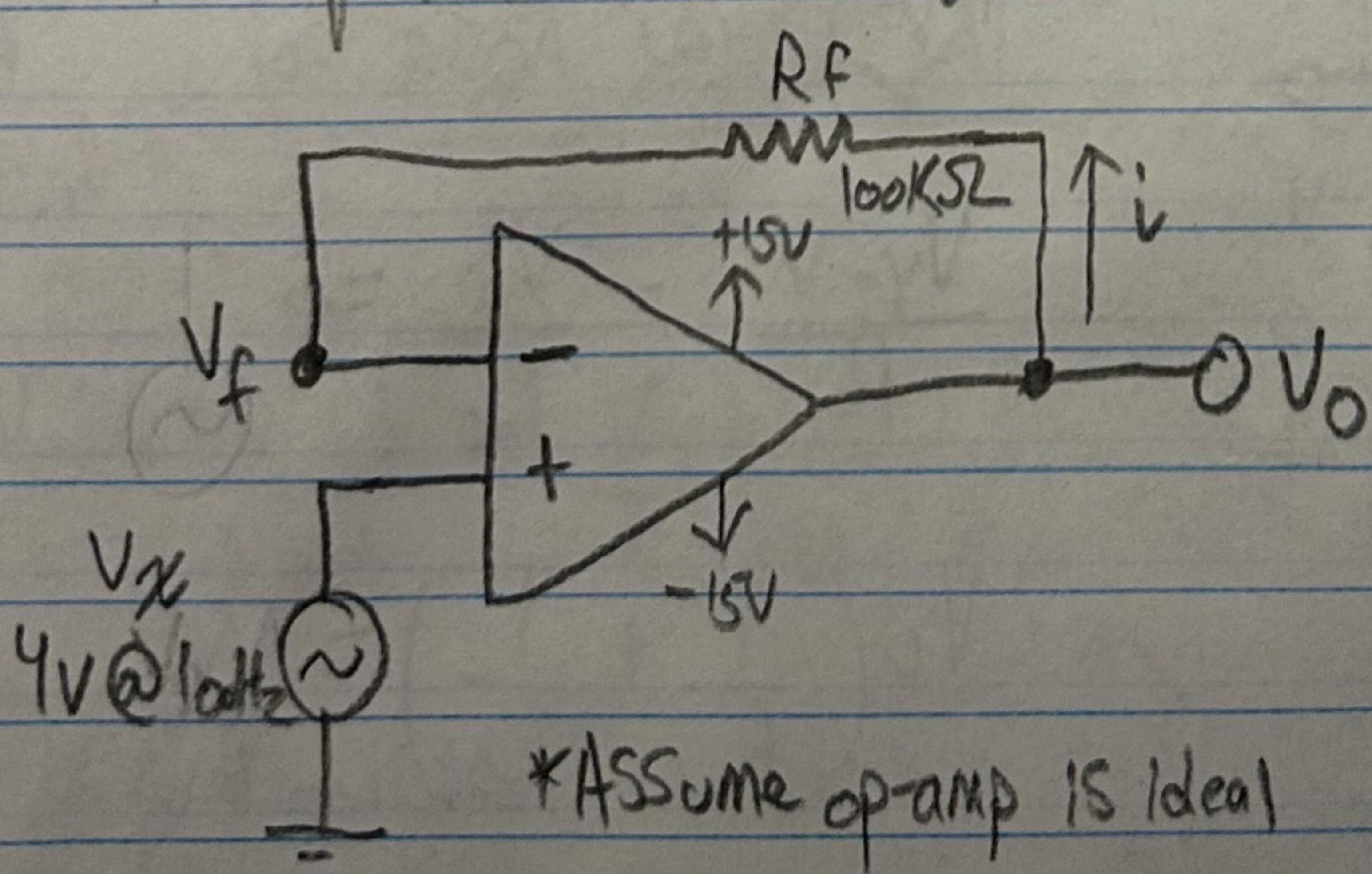
$$V_i < V_{TH} \rightarrow \text{op-amp is off}$$

$$V_i > V_{TH} \rightarrow \text{op-amp is on}$$

op-amp is off (lower saturation limit)

*the point where V_i and V_o intersect is V_{TH}

b)



$$V_o = A_o \cdot V_e$$

$$V_e = \Delta V = [(V^+) - (V^-)] = V_x - V_f$$

$$V_o = A_o (V_x - V_f)$$

$$V = \frac{V_o - V_e}{R_F}$$

$$\Rightarrow V_f = V_x$$

*Assume op-amp is ideal

Since NF exists, op-amp is assumed to be ideal and not saturated, then
 V_f tracks V_x and the gain, $A_o \approx 1$

$$V_o = A_o \left(V_x - \left(\frac{V_o - V_f}{R_F} \cdot R_F \right) \right) \quad *V_f = L \cdot R_F$$

$$V_o = 1 (V_x - (V_o - V_x))$$

$$2V_o = 2V_x \rightarrow \boxed{V_o = V_x}$$

(2)

Assuming the polarities are switched, then V_o will continue to saturate until it saturates at L^+

Figure 2a:

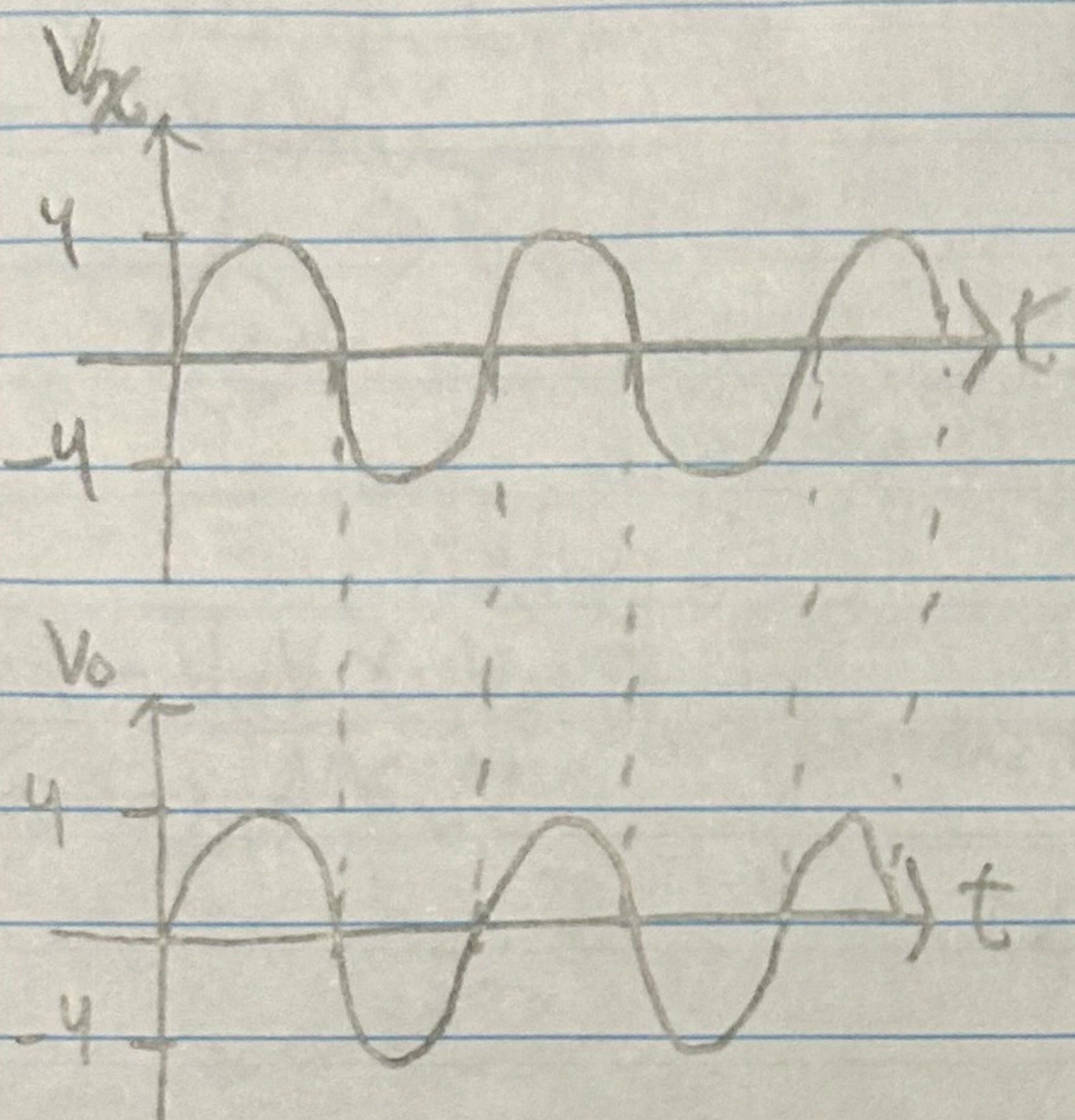
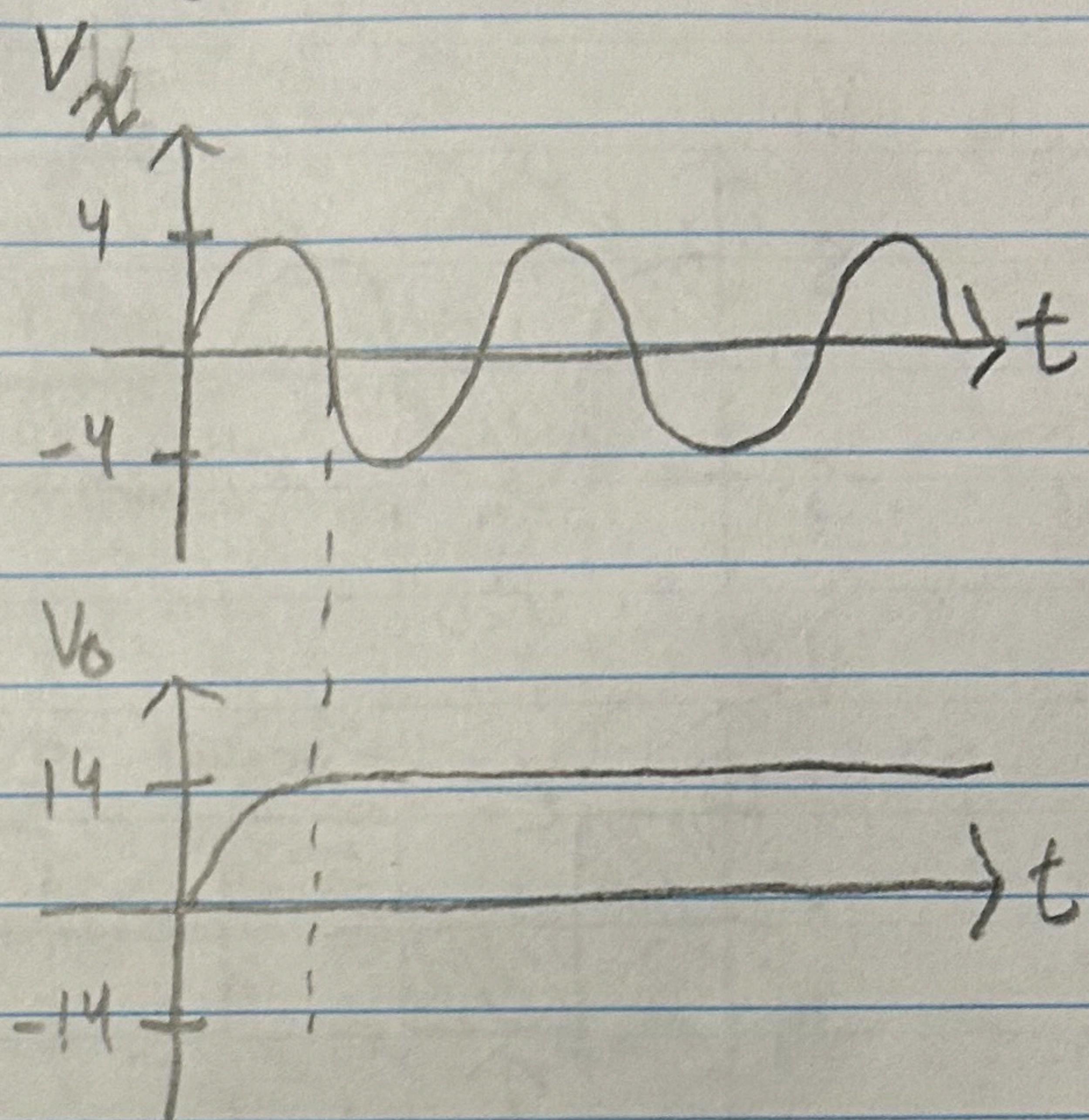
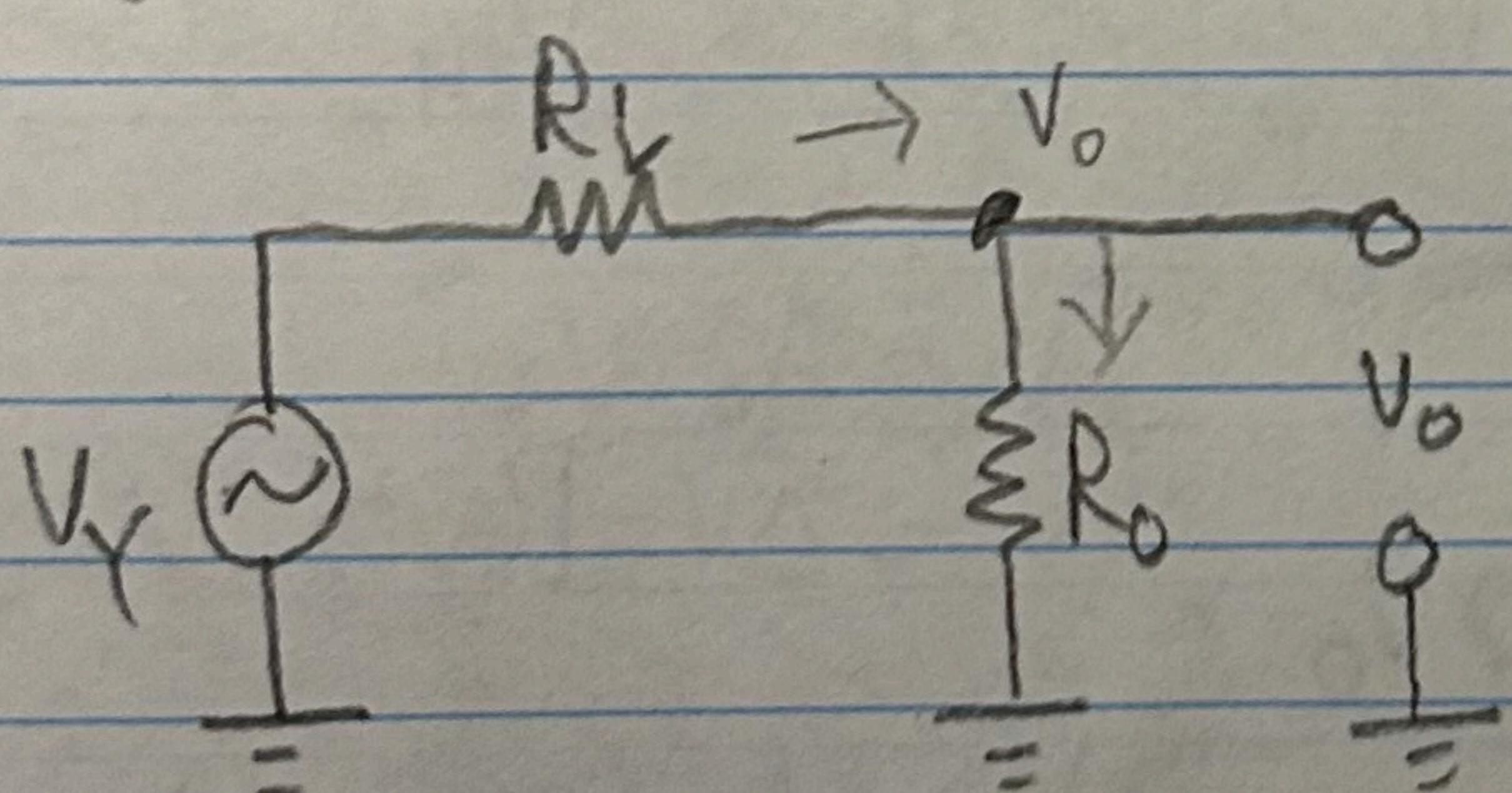


Figure 2b:



c) Figure 3a:

KCL @ node V_o

$$\frac{V_y - V_o}{R_L} - \frac{V_o}{R_o} = 0$$

$$\frac{R_o}{R_o + R_L}$$

$$V_y = 8V \text{ @ } 500\text{Hz}$$

$$R_L = 10k\Omega$$

$$R_o = 2k\Omega$$

$$V_o \left(\frac{1}{R_L} + \frac{1}{R_o} \right) = \frac{V_y}{R_L}$$

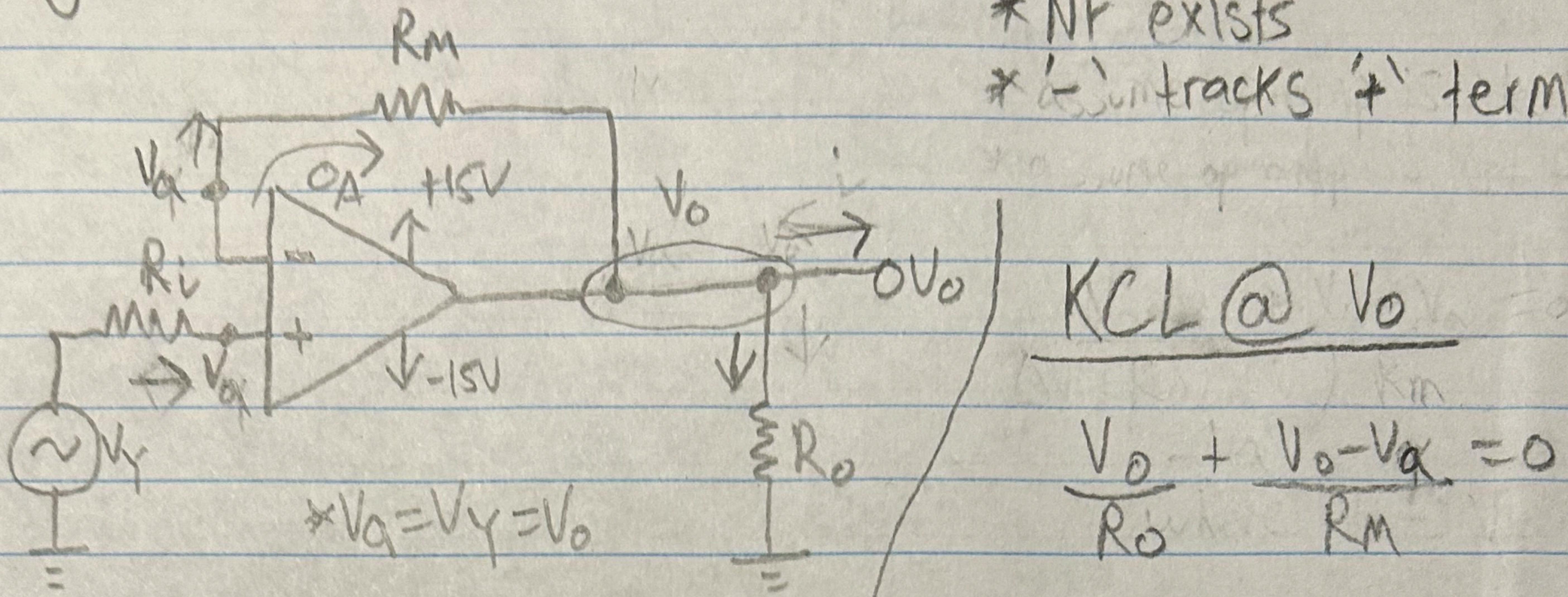
$$V_o = \frac{V_y}{R_L} \left(\frac{1}{\frac{1}{R_L} + \frac{1}{R_o}} \right)$$

\therefore the gain, A_o , for figure 3a is $A_o = \frac{V_o}{V_y} = \frac{R_o}{R_o + R_L}$

$$A_o = \frac{2k\Omega}{2k\Omega + 10k\Omega} = 0.167 \frac{V}{V}$$

(3)

Figure 3b:

 \star NF exists \star 'i' tracks '+' terminalsKCL @ V_O

$$\frac{V_O}{R_O} + \frac{V_O - V_Q}{R_M} = 0$$

$$\textcircled{1} \quad V_O = \left(\frac{V_Q - 1}{R_M} \right) - \frac{1}{R_O}$$

KCL @ V_Q

$$\frac{V_Q - V_Y}{R_V} = \frac{V_O - V_A}{R_M} = 0$$

 \star Substitute equation 2 into 1

$$V_O = \left(\frac{\frac{V_Y + 1}{R_V} + \frac{V_O + 1}{R_M}}{R_M} \right) - 1 - \frac{1}{R_O}$$

$$\textcircled{2} \quad V_A = \frac{V_Y + 1}{R_V} + \frac{V_O + 1}{R_M}$$

$$\frac{V_O - V_O + 1}{R_M} = \frac{V_Y + 1}{R_V \cdot R_M} - \frac{1}{R_M} - \frac{1}{R_O}$$

$$V_O \left(1 - \frac{1+1}{R_M^2} \right) = \frac{V_Y + 1}{R_V \cdot R_M} - \frac{1}{R_M} - \frac{1}{R_O}$$

$$V_O = \left(\frac{V_Y + 1}{R_V \cdot R_M} - \frac{1}{R_M} - \frac{1}{R_O} \right) \left(\frac{R_M^2}{R_M^2 - 2} \right) \xrightarrow{R_M^2 \approx 1}$$

$$A_O = \frac{V_O}{V_Y} = \left(\frac{V_Y + 1}{R_V \cdot R_M} - \frac{1}{R_M} - \frac{1}{R_O} \right) \frac{1}{V_Y}$$

$$\therefore \text{since } V_O \approx V_Y \rightarrow A_O = \frac{V_O}{V_Y} \approx 1$$

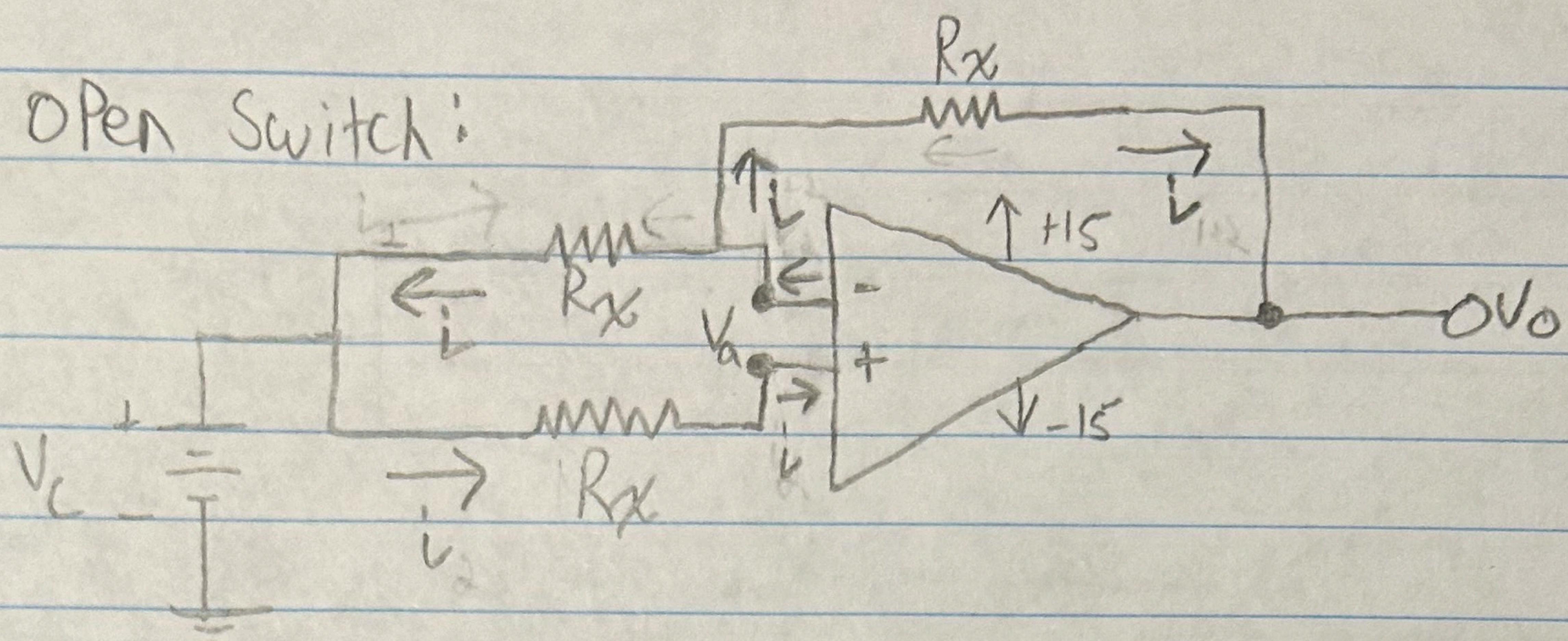
i) the gain would be different since figure 3b includes a buffer and NF

ii) the gain of figure 3b, $A_O \approx 1$, meaning the waveforms would be very similar, ^{allows} circuit _{isolation}

iii) The value of R_M doesn't effect the gain since the NF has $i=0A$

(U)

d) Open Switch:



$$V_c = 4V$$

$$R_g = 1K\Omega$$

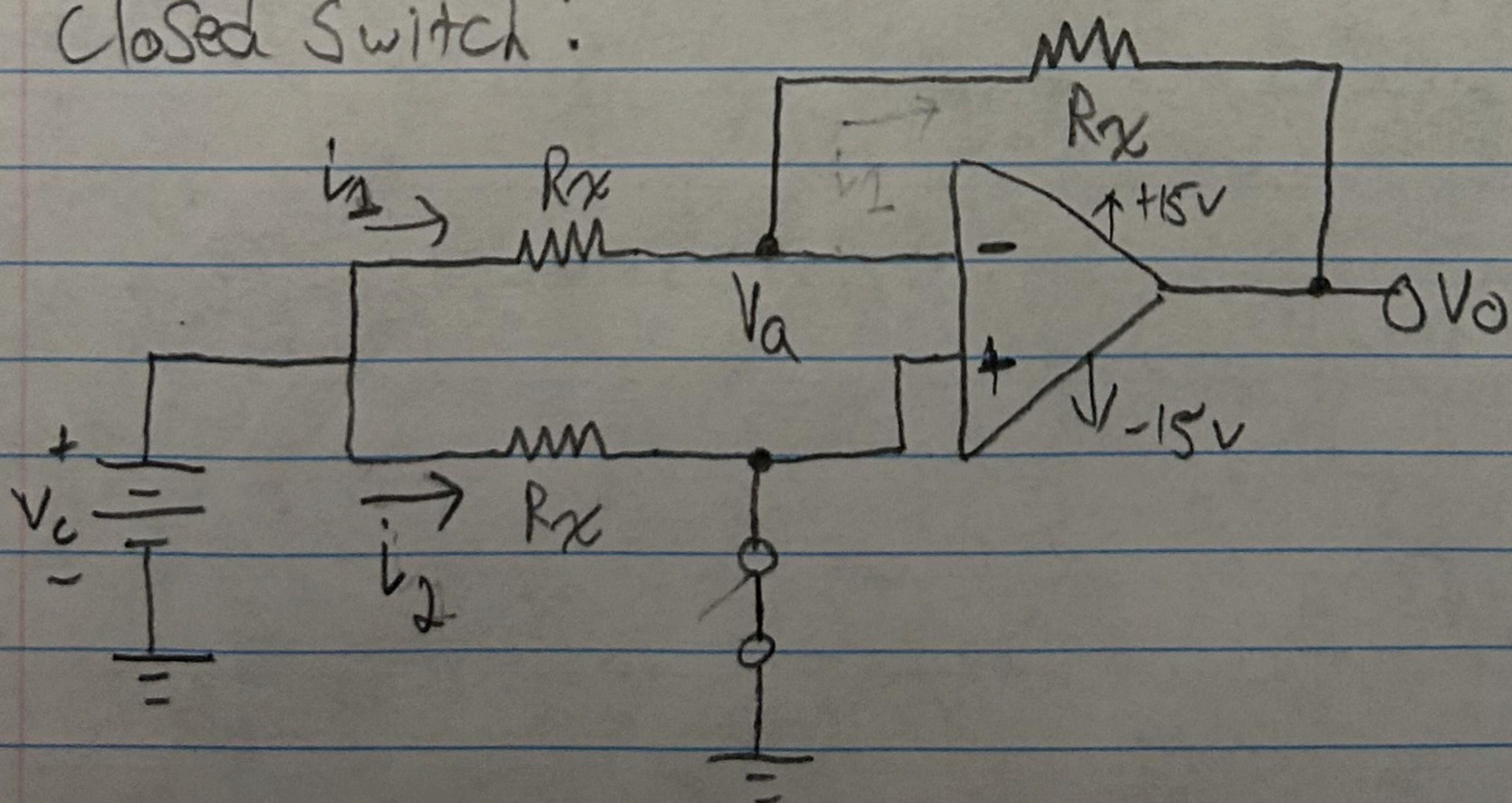
$$V_a = \frac{R_g}{2R_g} (V_c) = \frac{V_c}{2} = \frac{4}{2} = 2V$$

$$i = \frac{V_a - V_c}{R_g} = \frac{2 - 4}{10k} = -0.0002A$$

*Since all resistor values
are equal $i_1 = i_2$

$$\begin{aligned} V_o &= (i_1 + i_2) R_x \\ &\approx 2i R_x \\ &\approx 2(-0.0002)(10k) \\ \boxed{V_o &= -4V} \end{aligned}$$

Closed Switch:



*Now since the switch is closed, it is a short circuit,
 $i_1 = 0$ and all current flows through i_2

$$V_a = 2V, i = \frac{V_c - V_a}{R_g} = -0.0002A = \frac{V_a - V_b}{R_x} \Rightarrow \boxed{V_o = 4V}$$

3.02

Pre-Lab SIMULATIONS

Note the below instructions for the SIMULATIONS =>

- Refer to ELE504 D2L for information and instruction on securing the licensed version of **Multisim 14.2 Education**. You are required to use this Department issued licensed version of MultiSIM for all your required lab work simulations. No mark will be given for any simulation lab work submitted that: (a) is not supported by the required Pre-Lab Analysis in sec.3.01; and (b) did not use this particular licensed version of MultiSIM. **No exceptions.**
- The 741 Op-Amp to be used from the MultiSim Simulator Library is:- **LM741CN** model version.
- For each of the following circuits simulations, screen capture both your MultiSIM “simulated” circuit (*to include the entire screen with timestamp shown*) and all relevant Oscilloscope plots and/or device settings (*per the examples of screen-shots shown in the last page*). Include these screen captures in your *Pre-Lab submission*, and compare the plots with your *Pre-Lab analysis* results. Also, include your MultiSIM circuit file (.ms14).

EQUIPMENT: Power Supplies (PS), Function Generator (FG), Oscilloscope (OSC) & Digital Multi-Meter (DMM)

- (a) Implement the circuit of **Figure 1** in MultiSIM, and simulate the circuit operation using the parameter values provided to you for **Pre-Lab 3.01(a)** analysis. Set up the Function Generator (FG) for the input sinusoidal signal, V_I for each case, one at a time. Connect the V_I signal to the circuit and to the Oscilloscope (OSC) channel. Connect the output signal to the second channel of the Oscilloscope (OSC); and then observe the input V_I and V_o output signals on the Oscilloscope’s screen showing at least 2 period cycles. Record and compare the specified values as shown in the below Table, and include these in your *Pre-Lab submission*.

	V_o (Pre-lab Analysis)	V_o (Simulation)
$V_I < V_{TH}$	-14.0	-14.027
$V_I > V_{TH}$	14.0	14.027

- (b) Implement the circuit of **Figure 2a** first, and simulate the circuit operation using the parameter values provided to you for **Pre-Lab 3.01(b)**. Set up the Function Generator (FG) for the input sinusoidal signal, V_x at the specified frequency for each circuit, one at a time. Connect the V_x signal to the circuit and the Oscilloscope (OSC) channel.



Connect the output signal to the second channel of the Oscilloscope (OSC); and then observe the input V_x and V_o output signals on the Oscilloscope's screen showing at least 2 period cycles.

Now switch the input terminals of the circuit of Figure 2a as shown in **Figure 2b**. Using the same V_x input signal, observe the resultant output signal, V_o , and include the screenshots and comparisons in your *Pre-Lab submission*.

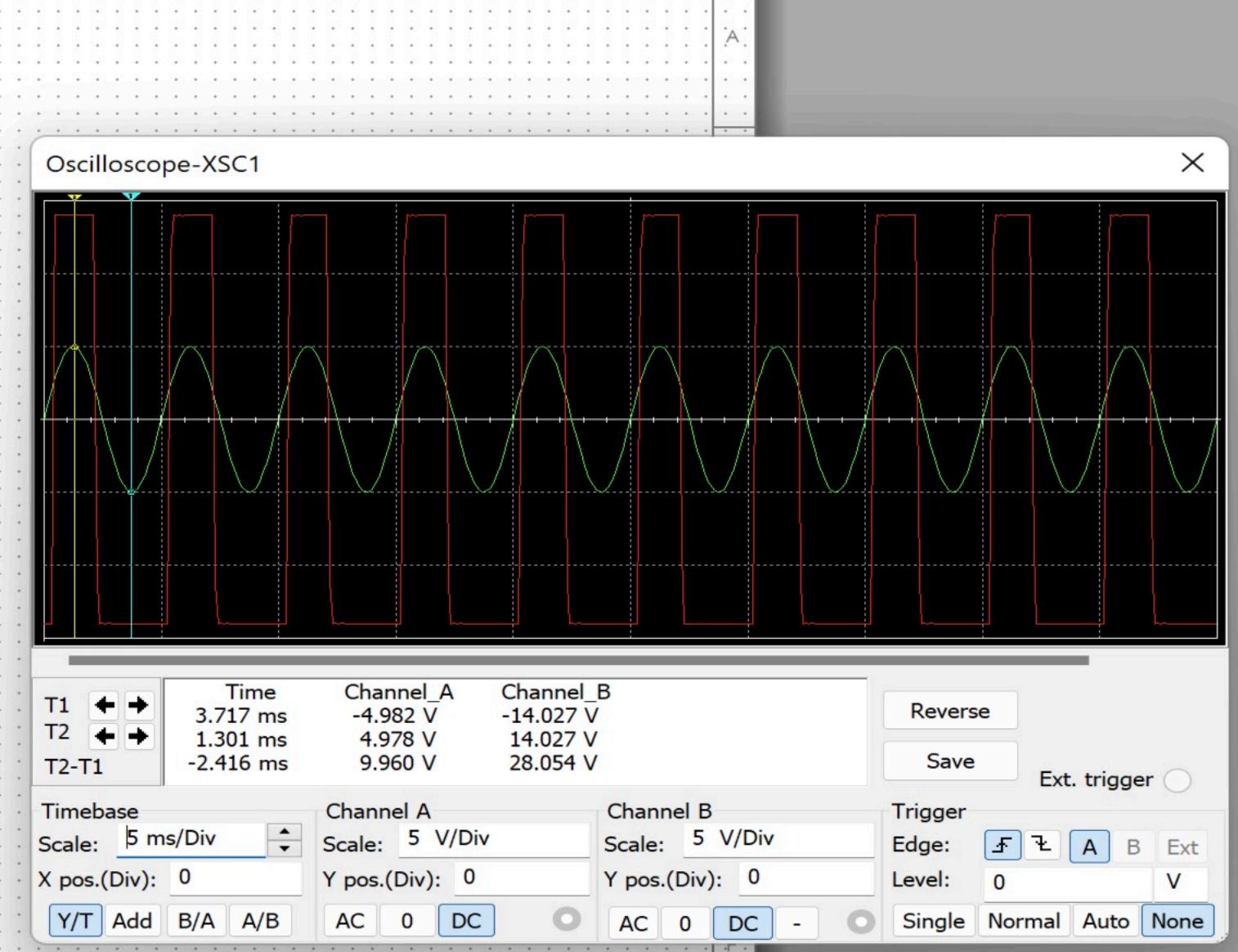
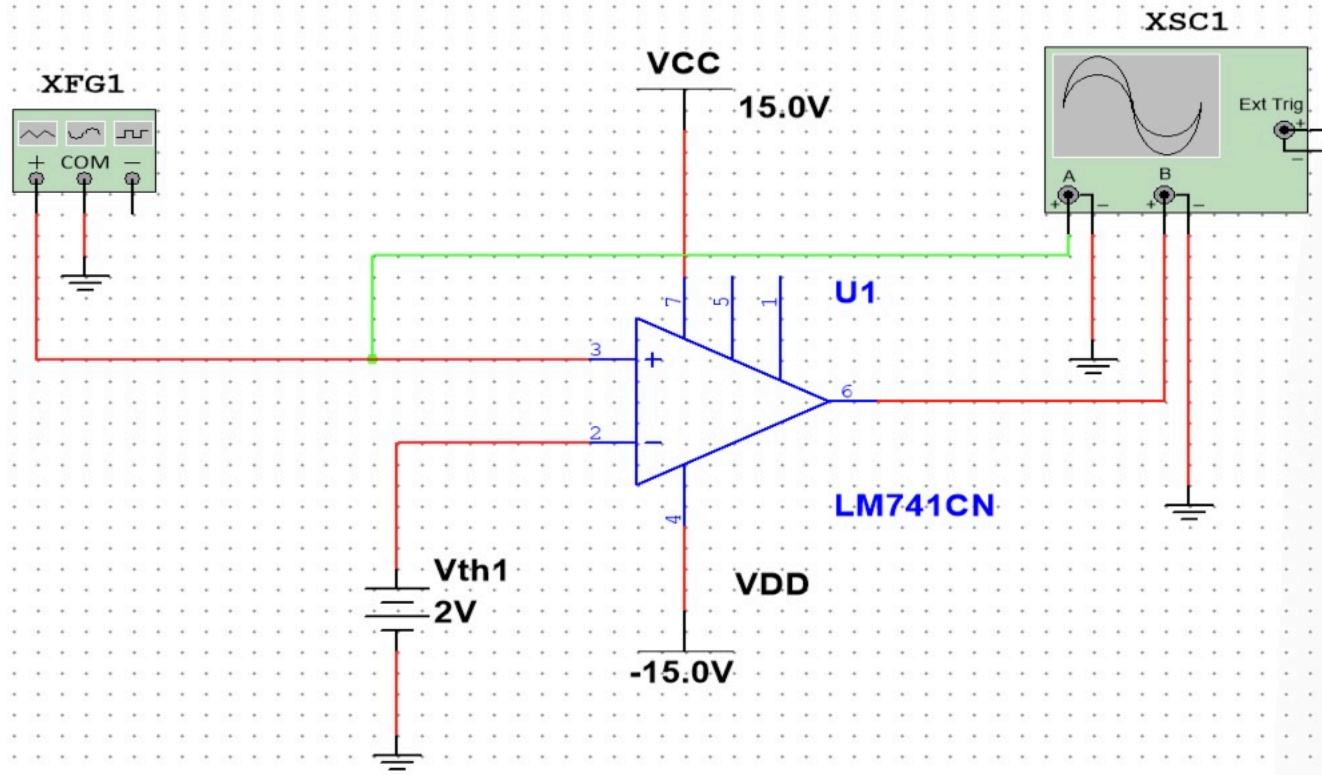
- (c) (1) Implement the circuit of **Figure 3a** and simulate its operation using the same parameter values of the resistors and input signal, V_y provided to you for **Pre-Lab 3.01(c)**. Observe and capture the input V_y and V_o output signals on the Oscilloscope screen showing at least 2 period cycles. Use FG for V_y input signal, and observe both V_y and V_o signals on the Oscilloscope (OSC) screen.
- (2) Next, implement the circuit of **Figure 3b**, simulate using the same input signal, V_y and record the respective waveforms. Use FG for V_y input signal, and observe both V_y and V_o signals on the Oscilloscope (OSC) screen.

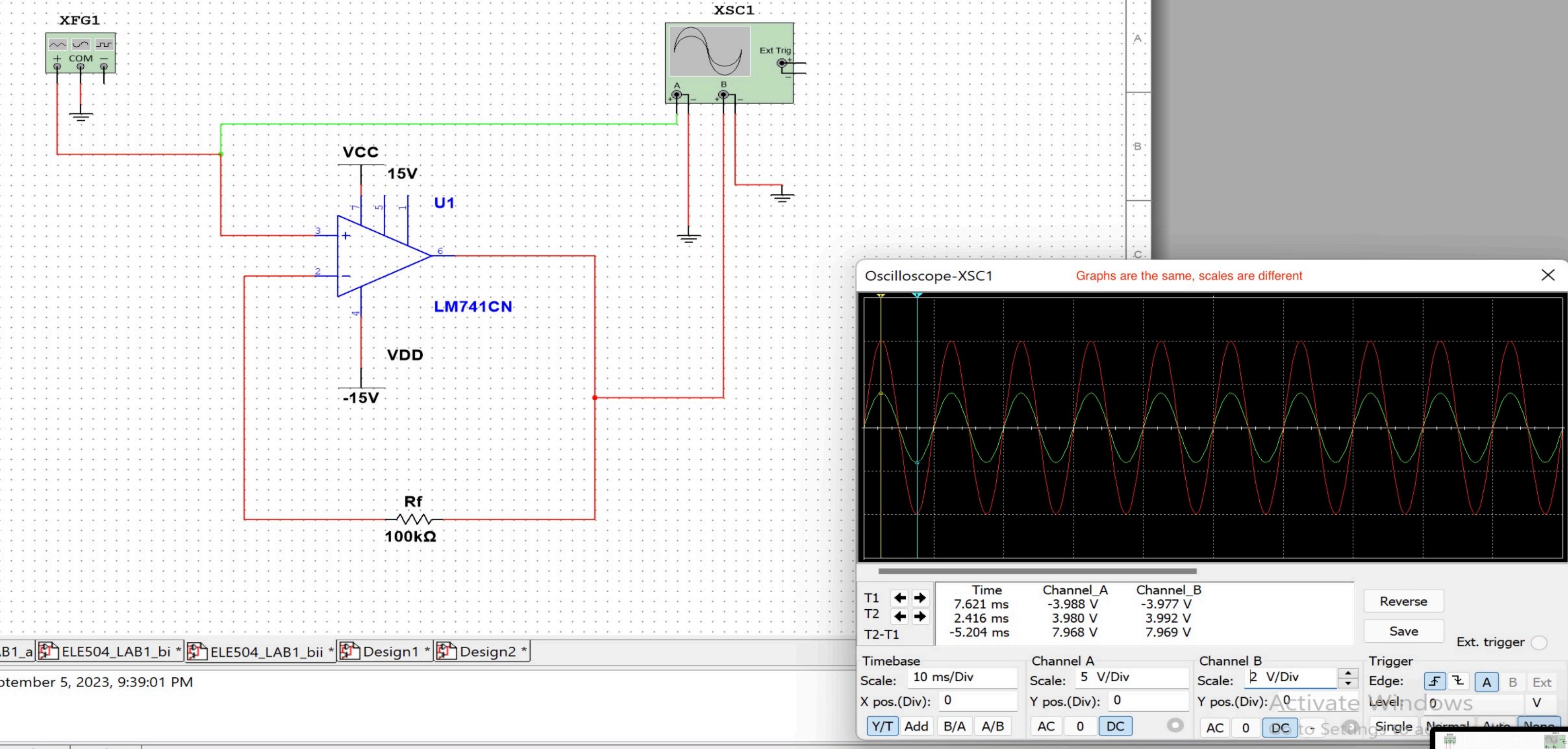
Record and compare the specified values as shown in the below Table, and include the screenshots and the below results in your *Pre-Lab submission*.

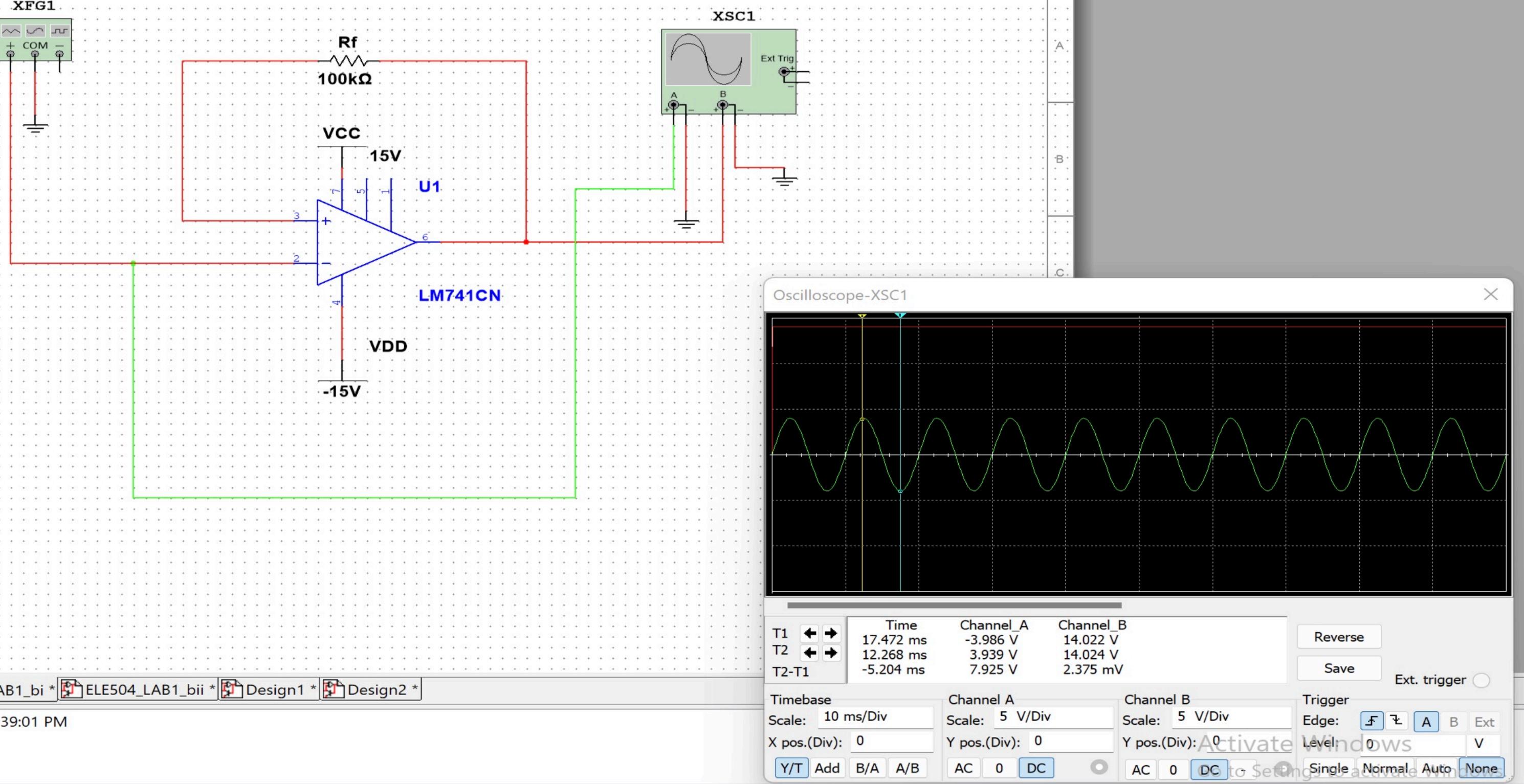
	V_{Yp-p}	V_{Op-p}	Gain (V_{Op-p}/V_{Yp-p}) Pre-Lab Analysis	Gain (V_{Op-p}/V_{Yp-p}) Simulation
Fig. 3a no Buffer	7.971	1.328	0.167	0.167
Fig. 3b with Buffer	7.942	7.953	1.00	1.00

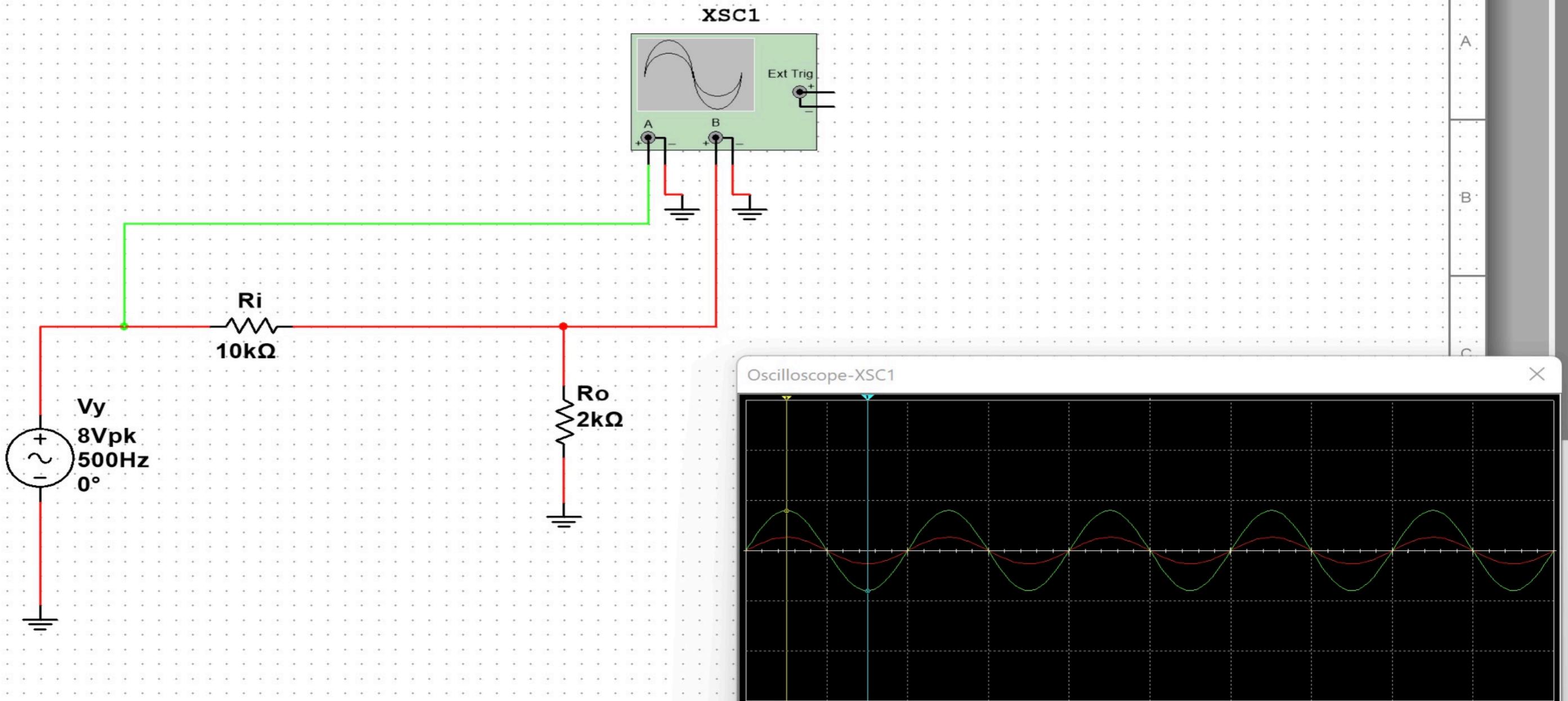
- (d) Implement the circuit of **Figure 4**, and simulate the circuit operation using the parameter values (R_x and V_c) provided to you for **Pre-Lab 3.01(d)**. Measure the output voltage, V_o (using a DMM d.c.Voltmeter) when the switch S_1 is CLOSED, and when S_1 is OPEN. and record your results in the Table below.

Switch S_1	V_c	V_o Pre-Lab Analysis	V_o Simulation
Close	4	-4.00	-3.998
Open	4	4.00	4.002







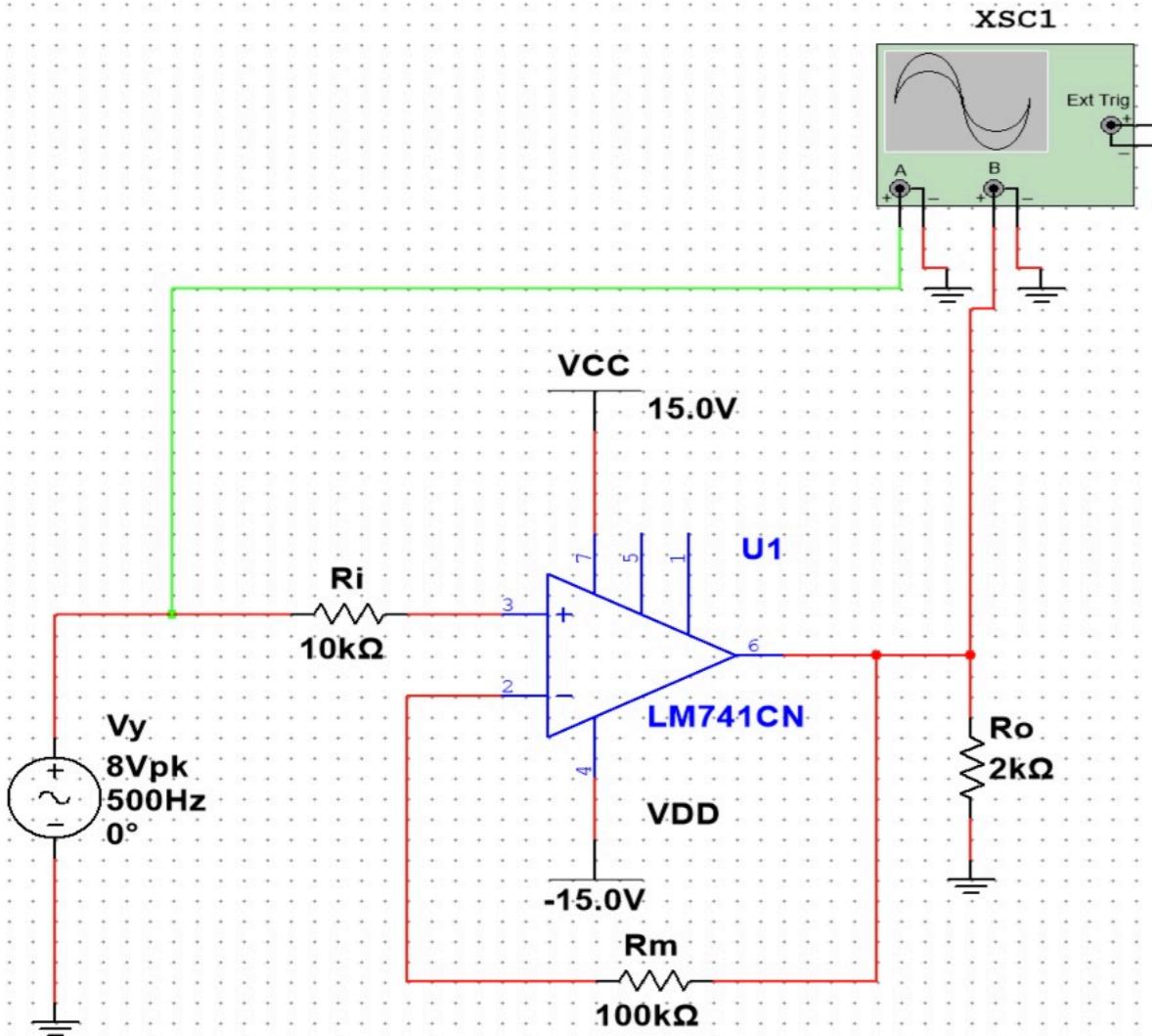


LAB1_bi * ELE504_LAB1_bii * Design1 * Design2 *

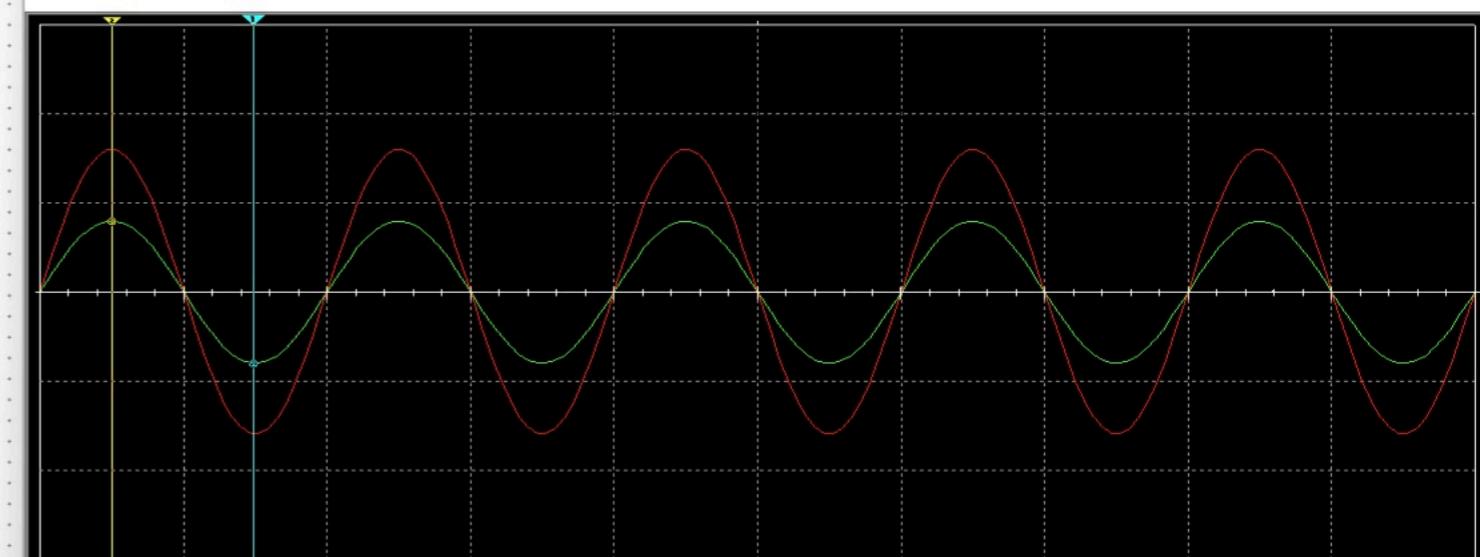
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T1	Time	Channel_A	Channel_B	Reverse
1.506 ms	-7.975 V	-1.329 V		
501.859 us	7.971 V	1.328 V		
-1.004 ms	15.946 V	2.658 V		
				Save
				Ext. trigger
				Trigger
				Edge: F A B Ext
				Level: 0 V

Activate Windows
Go to Settings to activate Windows.



Oscilloscope-XSC1



04_LAB1_a ELE504_LAB1_bi * ELE504_LAB1_bii * ELE504_LAB1_ci ELE504_LAB1_cii * ELE504_LAB1_d

September 5, 2023, 9:39:01 PM

	Time	Channel_A	Channel_B
T1	1.487 ms	-7.958 V	-7.948 V
T2	501.859 us	7.962 V	7.972 V
T2-T1	-985.130 us	15.920 V	15.920 V

Reverse

Save

Ext. trigger

Activate Windows

Go to Settings to activate Windows.

Trigger

