Department of Electrical
& Computer Engineering
Faculty of Engineering & Architectural Science

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Instructor:	Dr. Mike Kassam

Assignment/Lab Number:	Lab 1
Assignment/Lab Title:	Operational Amplifier Circuits (review)

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Student LAST Name	Student FIRST Name	Student Number	Section	Signature*
Abbas	Syed Maisam	501103255	02	Maisam
Raza	Hasnain	501101632	02	Hasnain

*By signing above you attest that you have contributed to this written lab report and confirm that all work you have contributed to this lab report is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a "0" on the work, an "F" in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at: http://www.ryerson.ca/senate/current/pol60.pdf

Lab 1 Report: Operational Amplifier Circuits (review)

By: Syed Maisam Abbas & Hasnain Raza

Table of Contents

1. Introduction

This is the lab report for Lab 1: Operational Amplifier Circuits (review) by Syed Maisam Abbas and Hasnain Raza. The experiment was conducted on Monday, September 11, 2023. The pre-labs were individually done and submitted before the start of the lab. The results of the prelab analysis, online simulations, and in-lab measurements are recorded and observed in greater detail in this lab report.

2. Objectives

The objective of this lab is to analyze, simulate, and investigate the characteristics of different types of Op-Amp circuit configurations provided in the lab manual (figures 1-4) using the individually assigned values provided by TA. These circuit configurations include a basic comparator, buffers, and a switched "polarity inversion" converter.

Values assigned to Syed Maisam Abbas:

V_I = 5V peak @ 200Hz	V_{TH} = 2V d.c.		
V_X = 4V peak @ 100Hz	R_f = 100KΩ		
V_Y = 8V peak @ 500Hz	R_i = 10KΩ	R_O = 2KΩ	R_M = 100KΩ
V_C = 4V d.c.	R_X = 1KΩ		

Values assigned to Hasnain Raza: (values used for the duration of the in-lab experiment)

V_I = 3V peak @ 200Hz	V_{TH} = 1V d.c.		
V_X = 6V peak @ 300Hz	R_f = 220KΩ		
V_Y = 8V peak @ 500Hz	R_i = 47KΩ	R_O = 10KΩ	R_M = 220KΩ
V_C = 5V d.c.	R_X = 10KΩ		

3. Results and Calculations

Circuit Figure 1: Basic Comparator

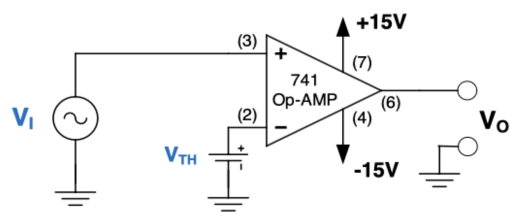
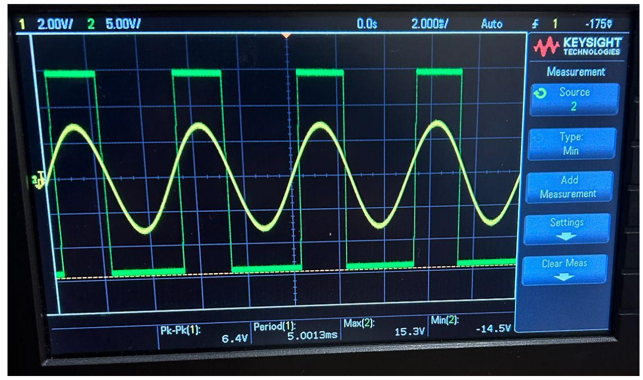
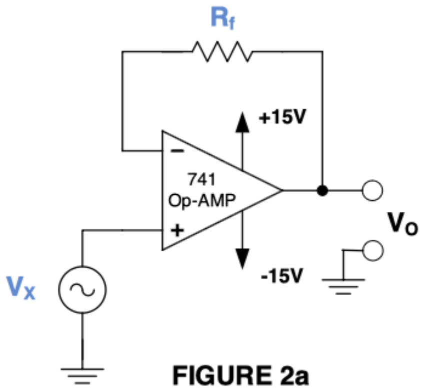


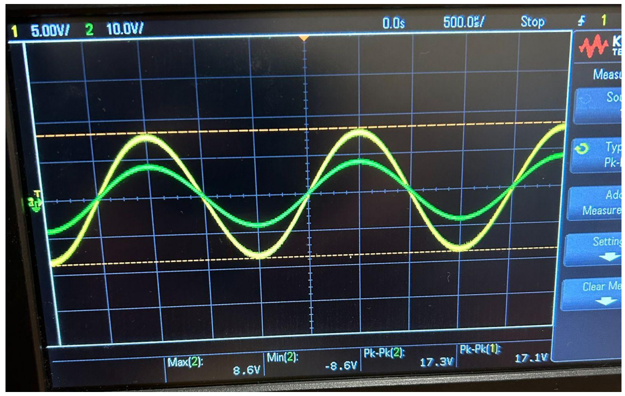
Figure 1



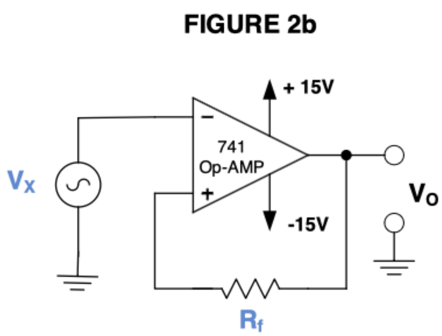
	V_O (Pre-Lab Analysis)	V_O (Pre-Lab Simulations)	V_O (In-Lab Measurement)
$V_I < V_{TH}$	-14 V	-14.027 V	-14.5 V
$V_I > V_{TH}$	14 V	14.027 V	15.1 V

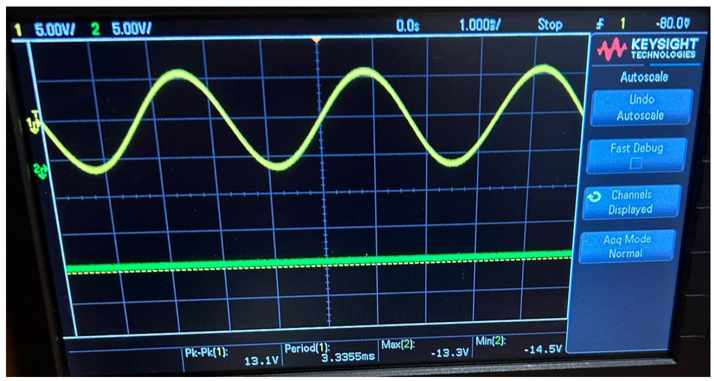
Circuit Figure 2a: Non-Inverting Buffer





Circuit Figure 2b: Non-Inverting Buffer (mistakely switched input polarities)





Note: Refer to the appendix for the theoretical graphical representation of figures 2a and 2b

Circuit Figure 3a: Simple Circuit Configuration (no buffer)

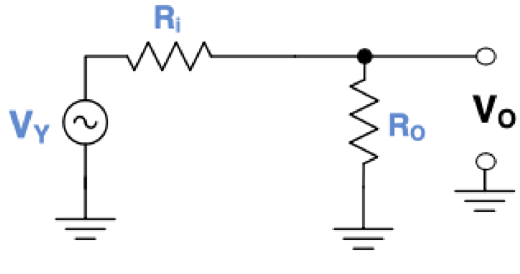
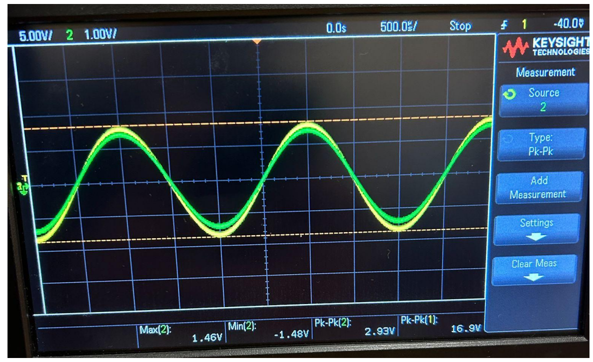


Figure 3a



Circuit Figure 3b: Simple Circuit Configuration (with buffer)

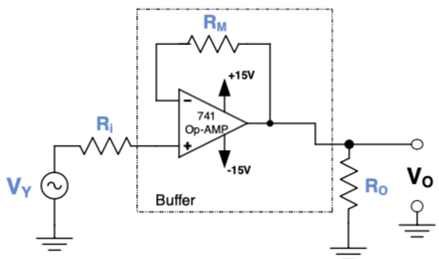
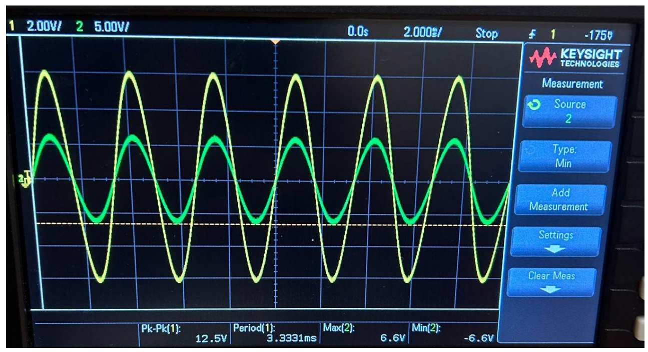


Figure 3b



	Vip-p Measured	**VOp-p** Measured	**Gain (Vop-p/Vip-p)** Derived from the measurement	**Gain (Vop-p/Vip-p)** From the Pre-Lab Analysis	**Gain (Vop-p/Vip-p)** From the Pre-Lab Simulation
Fig.3a no Buffer	16.9 V	2.93 V	0.173 V/V	0.175 V/V	0.175 V/V
Fig.3b with Buffer	17.1 V	17.3 V	1.012 V/V	1.00 V/V	0.99 V/V

Circuit Figure 4: Switched "Polarity Inversion" Converter

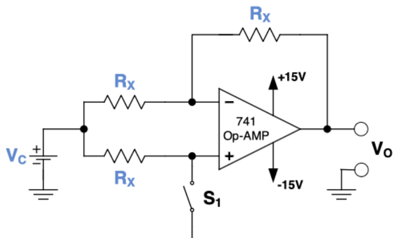
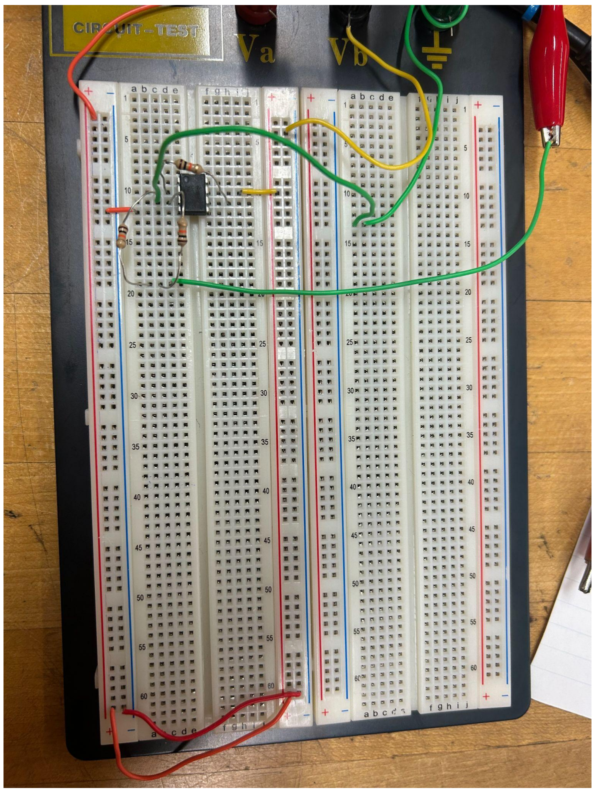
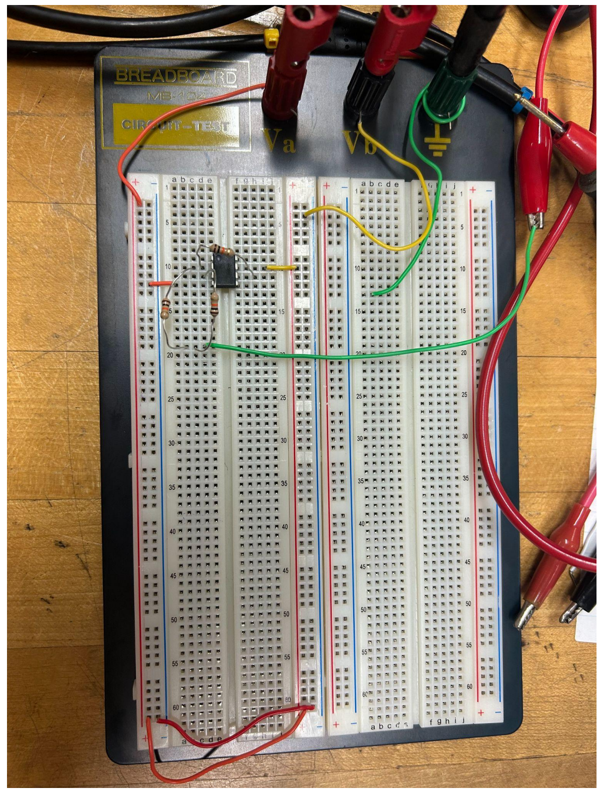


Figure 4





(closed switch)

(open switch)

	Vc	Vo (Pre-Lab Analysis)	Vo (Pre-Lab Simulations)	Vo Measured
Switch CLOSED	-5 V	-5 V	-4.998	-5.039 V
Switch OPEN	5 V	5 V	5.002	5.035 V

The percentage error can be calculated using the following equation:

$$e\% \;=\; \frac{[(calculated\ value \;-\; measured\ value)]}{measured\ value} \times 100\%$$

Circuit Configuration	Calculated Values (pre-lab analysis)	Measured Values (In-lab experiment)	Percentage Error (e%)
Figure 1	-14.0 V	-14.5 V	-3.45 %
	14.0 V	15.1 V	-7.28 %
Figure 3a	0.175 V/V	0.173 V/V	1.16 %
Figure 3b	1.00 V/V	1.012 V/V	-1.19 %
Figure 4	-5.00 V	-5.039 V	-0.774 %
	5.00 V	5.035 V	-0.695 %

Table 1: Calculation of percentage errors

The percentage errors calculated in table 1 above include the output voltages for figure 1 (Vi < Vth & Vi > Vth), the gains for figure 3a and 3b, and the output voltages for figure 4 (closed switch & open switch), respectively. No in-lab or simulation measurements were required for circuit configuration 2 in this lab experiment. By analyzing the table above, it is clear that the percentage errors are reasonably low since each circuit configuration has a percentage error of ±10%. However, the reason(s) for these discrepancies may be due to the measurement uncertainties or input dealy time in an ideal experimental setup.

4. Conclusion and Remarks

In summary, the experiment was successful with minimal discrepancies. In the first segment, our focus was on an open-loop circuit without feedback. Preliminary observations indicated that it functioned as a comparator circuit, with output voltages of 14 V and -14 V. The graphs generated from our theoretical assumptions closely mirrored the actual results, with slight variations likely due to equipment and setup nuances.

For the second segment, the initial circuit displayed no current in its negative terminal because of the absence of a voltage differential. As a result, Vx and Vo were inferred to be identical. In the lab, the graphs were nearly the same with a insignificant deviation. However, the theoretical predictions differed from both the simulated and actual findings. This minor deviation was likely caused by static and fluctuations due to loose connections on the breadboard. Through graphical representation, we gained insight into the role of positive feedback in determining Vo.

In the third segment, both our prelab simulation and in lab test revealed a gain of approximately 0.175 for figure 3a. The introduction of a buffer aimed to demonstrate its function – balancing input and output resistances. The resultant voltage gain was identical, in agreement with our pre-lab assumptions and simulations which was a gain of 1. This is due to the non existent current flow in the circuit causing the output voltage to equal the input voltage.

In the fourth segment, when the switch was in closed, both terminals – positive and negative – would be grounded to 0 V. An analysis of the node linked to the negative terminal and the feedback resistor showed that Vo is merely the inverse of the source voltage, Vc. With the switch in an open state, both terminal voltages stand at 5V. Since the voltage variance is null (equalling 0), any Rx linked to these terminals has no current flow, making its behavior akin to a buffer, with VC and Vo being identical. This was in line with our in-lab observations, which displayed no anomalies.

To wrap up, this experiment offered a comprehensive study of various op-amp setups and configurations. It provided invaluable hands-on experience with op-amps, enhancing our grasp on their interactions with diverse components.

5. Appendix— Handwritten Work, Pre-Lab of Syed Maisam Abbas and Hasnain Raza

5.1 Syed Maisam Abbas' Pre-Lab: Full Pre-Lab Submitted to D2L

Prelab #1

1

a) *Assume op-amp is ideal, ∴ $A >> 1$

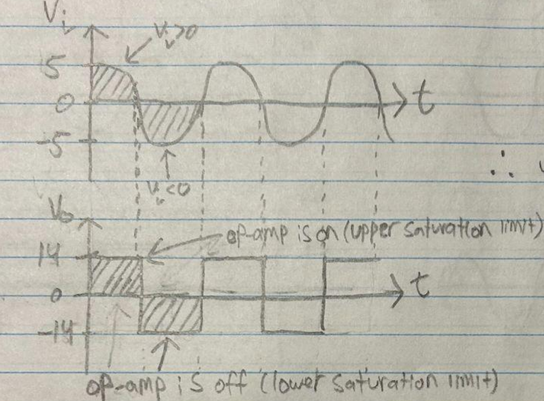
$V_0 = A \cdot \Delta V$

$* = \infty \cdot [(v^+) - (v^-)]$

Since it's in open-loop mode (no feedback) op-amp can have only 2 states:

$\Delta V > 0 \rightarrow V_0 = L^+$

$\Delta V < 0 \rightarrow V_0 = L^-$



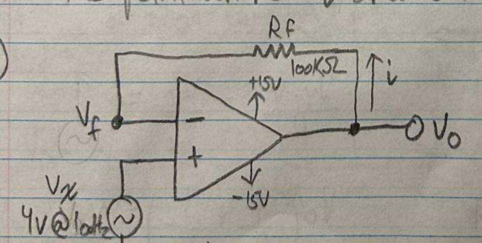
∴ when

$V_i < V_{TH} \rightarrow$ op-amp is off

$V_i > V_{TH} \rightarrow$ op-amp is on

*the point where V_i and V_o intersect is V_{TH}

b)



*Assume op-amp is ideal

$V_0 = A_0 \cdot V_e$

$V_e = \Delta V = [(v^+) - (v^-)] = V_x - V_f$

$V_0 = A_0 (V_x - V_f)$

$i = \frac{V_0 - V_f}{R_f}$ $\quad *V_f = V_x$

Since NF exists, op-amp is assumed to be ideal and not saturated, then V_f tracks V_x and the gain, $A_0 \approx 1$

$V_0 = A_0\left(V_x - \left(\frac{V_0 - V_f}{R_f} \cdot R_f\right)\right)$ $\quad *V_f = i \cdot R_f$

$V_0 = 1(V_x - (V_0 - V_x))$

$2V_0 = 2V_x \rightarrow \boxed{V_0 = V_x}$

2

Assuming the polarities are switched, then V_o will continue to saturate until it saturates at L^+

Figure 2a:

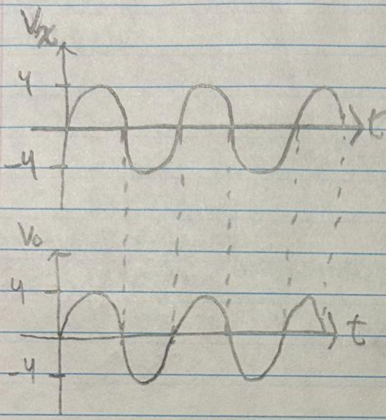
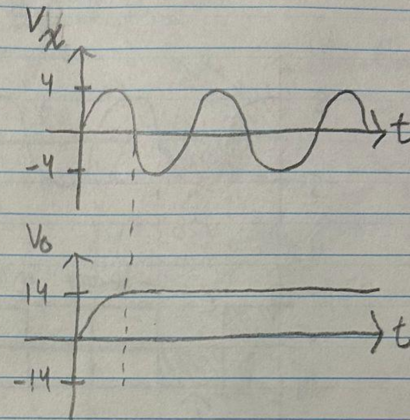
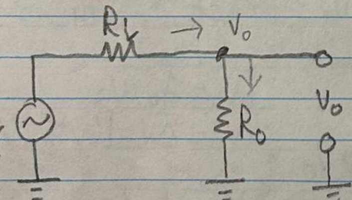


Figure 2b:



c) Figure 3a:



$V_y = 8V$ @ 500Hz
$R_i = 10K\Omega$
$R_o = 2K\Omega$

KCL @ node V_o

$$\frac{R_o}{R_o + R_i}$$

$$\frac{V_y - V_o}{R_i} - \frac{V_o}{R_o} = 0$$

$$V_o\left(\frac{1}{R_i} + \frac{1}{R_o}\right) = \frac{V_y}{R_i}$$

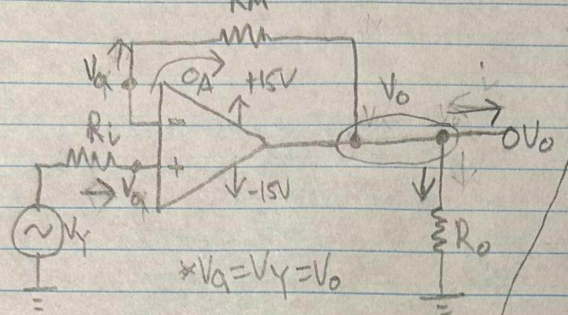
$$V_o = \frac{V_y}{R_i}\left(\frac{1}{\frac{1}{R_i} + \frac{1}{R_o}}\right)$$

$\therefore$ the gain, A_o, for figure 3a is $\frac{V_o}{V_y} = \boxed{A_o = \frac{R_o}{R_o + R_i}}$

$$A_o = \frac{2K\Omega}{2K\Omega + 10K\Omega} = 0.167\ \frac{V}{V}$$

③

Figure 3b:



$*V_a = V_Y = V_o$

* NF exists
* '-' tracks '+' terminals

$V_Y = 8v$ @ 500Hz
$R_i = 10K\Omega$
$R_M = 100K\Omega$
$R_o = 2K\Omega$

KCL @ Vo

$$\frac{V_o}{R_o} + \frac{V_o - V_a}{R_M} = 0$$

① $$V_o = \left(\frac{V_a - 1}{R_M}\right) - \frac{1}{R_o}$$

KCL @ Va

$$\frac{V_a - V_Y}{R_i} = \frac{V_o - V_a}{R_M} = 0$$

② $$V_a = \frac{V_Y + 1}{R_i} + \frac{V_o + 1}{R_M}$$

*Substitute equation 2 into 1

$$V_o = \frac{\left(\frac{V_Y + 1}{R_i} + \frac{V_o + 1}{R_M}\right) - 1}{R_M} - \frac{1}{R_o}$$

$$V_o - \frac{V_o + 1}{R_M^2} = \frac{V_Y + 1}{R_i \cdot R_M} - \frac{1}{R_M} - \frac{1}{R_o}$$

$$V_o\left(1 - \frac{1+1}{R_M^2}\right) = \frac{V_Y + 1}{R_i \cdot R_M} - \frac{1}{R_M} - \frac{1}{R_o}$$

$$V_o = \left(\frac{V_Y + 1}{R_i \cdot R_M} - \frac{1}{R_M} - \frac{1}{R_o}\right)\underbrace{\left(\frac{R_M^2}{R_M^2 - 2}\right)}_{\approx 1}$$

$$A_o = \frac{V_o}{V_Y} = \left(\frac{V_Y + 1}{R_i \cdot R_M} - \frac{1}{R_M} - \frac{1}{R_o}\right)\frac{1}{V_Y}$$

$\therefore$ since $V_o \approx V_Y \rightarrow \boxed{A_o = \frac{V_o}{V_Y} \approx 1}$

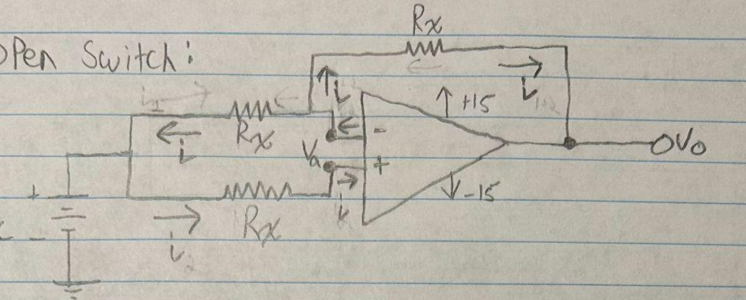
i) the gain would be different since figure 3b includes a buffer and NF

ii) the gain of figure 3b, $A_o \approx 1$, meaning the waveforms would be very similar, allows circuit isolation

iii) The value of RM doesn't effect the gain since the NF has $i = 0A$

4

d) Open Switch:



$V_c = 4V$

$R_x = 1K\Omega$

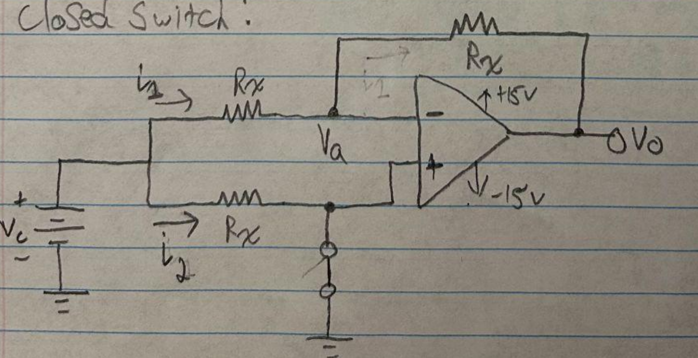
$$V_a = \frac{R_x}{2R_x}(V_c) = \frac{V_c}{2} = \frac{4}{2} = 2V$$

$$i = \frac{V_a - V_c}{R_x} = \frac{2-4}{10k} = -0.0002A$$

*Since all resistor values are equal $i_1 = i_2$

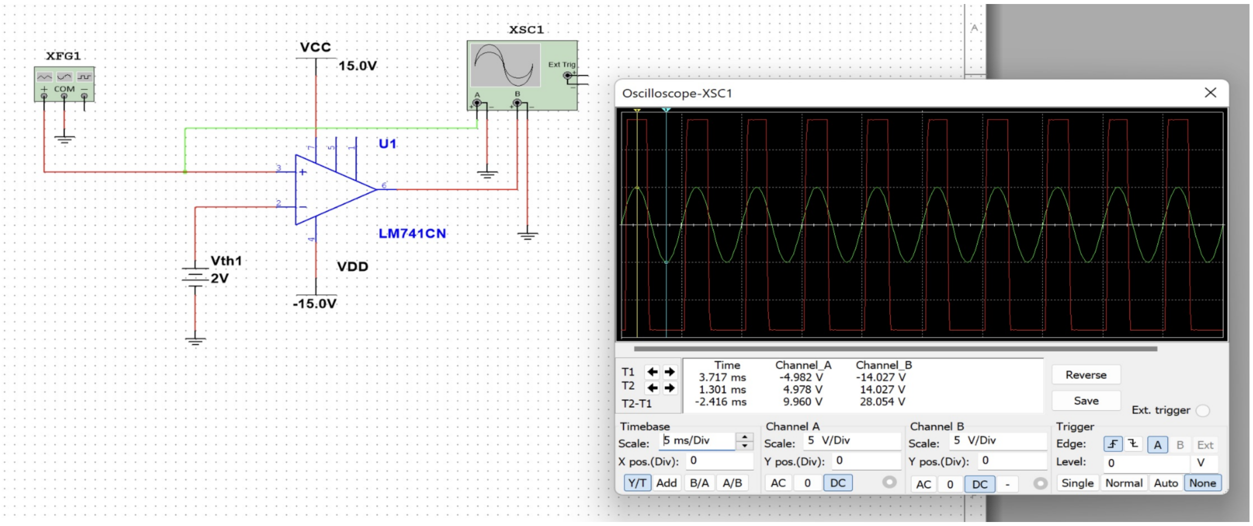
$$V_o = (i_1 + i_2)R_x$$
$$= 2iR_x$$
$$= 2(-0.0002)(10k)$$
$$\boxed{V_o = -4V}$$

Closed Switch:



*Now since the switch is closed, it is a short circuit, $i_1 = 0$ and all current flows through i_2

$$V_a = 2V, \quad i = \frac{V_c - V_a}{2R_x} = -0.0002A = \frac{V_a - V_o}{R_x} \Rightarrow \boxed{V_o = 4V}$$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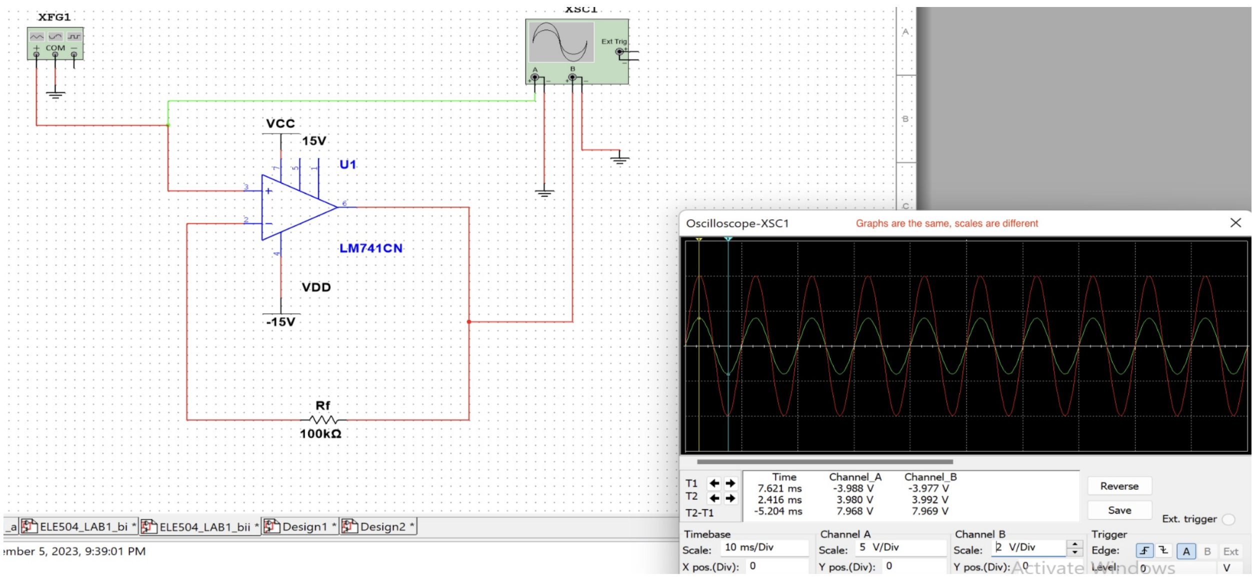
VCC
15.0V
XSC1
U1
LM741CN
Vth1
2V
VDD
-15.0V
Oscilloscope-XSC1
Time Channel_A Channel_B
T1 3.717 ms -4.982 V -14.027 V
T2 1.301 ms 4.978 V 14.027 V
T2-T1 -2.416 ms 9.960 V 28.054 V
Reverse
Save
Ext. trigger
Timebase Scale: 5 ms/Div X pos.(Div): 0
Channel A Scale: 5 V/Div Y pos.(Div): 0
Channel B Scale: 5 V/Div Y pos.(Div): 0
Trigger Edge: Level: 0 V
Y/T Add B/A A/B AC 0 DC AC 0 DC -
Single Normal Auto None


XFG1
XSC1
VCC
15V
U1
LM741CN
VDD
-15V
Rf
100kΩ
Oscilloscope-XSC1
Graphs are the same, scales are different
Time Channel_A Channel_B
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T2 2.416 ms 3.980 V 3.992 V
T2-T1 -5.204 ms 7.968 V 7.969 V
Reverse
Save
Ext. trigger
Timebase Scale: 10 ms/Div X pos.(Div): 0
Channel A Scale: 5 V/Div Y pos.(Div): 0
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Trigger Edge: Level: 0 V
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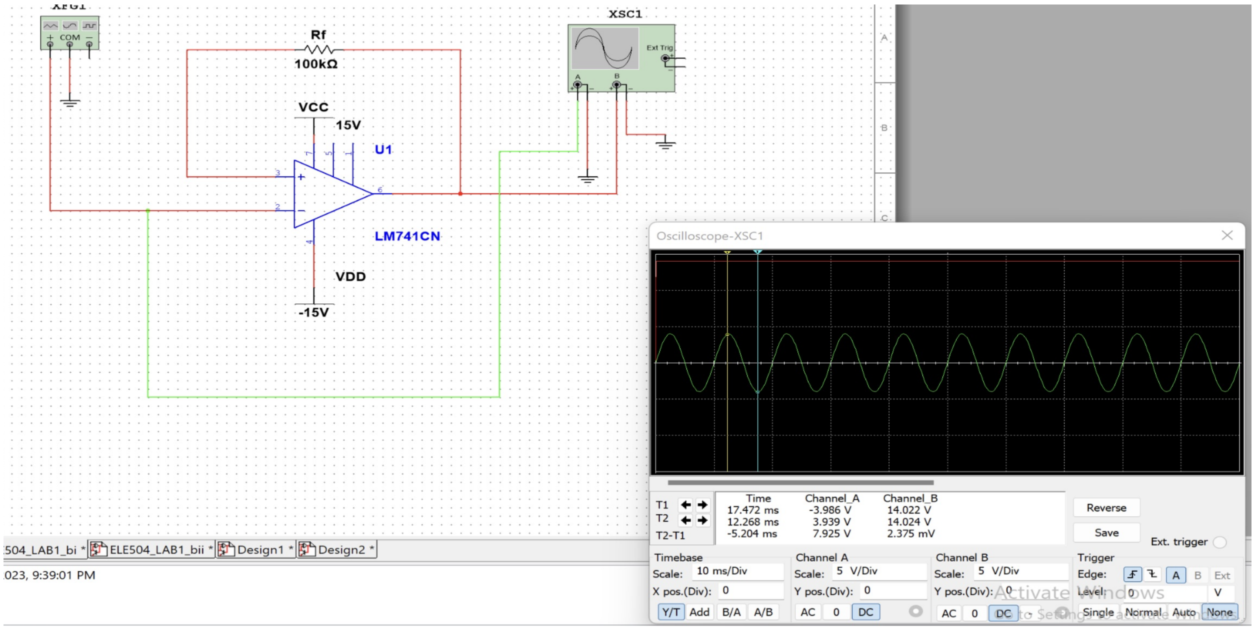
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Rf
100kΩ
VCC
15V
U1
LM741CN
VDD
-15V
Oscilloscope-XSC1
Time
Channel_A
Channel_B
T1
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-3.986 V
14.022 V
T2
12.268 ms
3.939 V
14.024 V
T2-T1
-5.204 ms
7.925 V
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Save
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Channel A
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Y pos.(Div): 0
AC 0 DC
Channel B
Scale: 5 V/Div
Y pos.(Div): 0
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Edge:
Level: 0 V
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ELE504_LAB1_bii
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Design2
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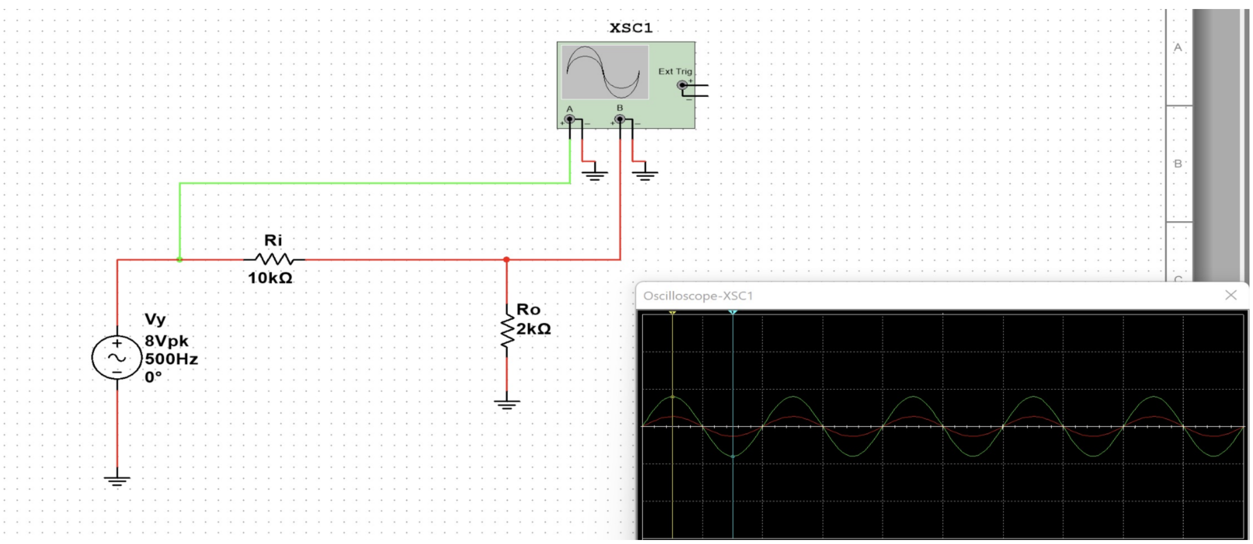
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Ext Trig
Ri
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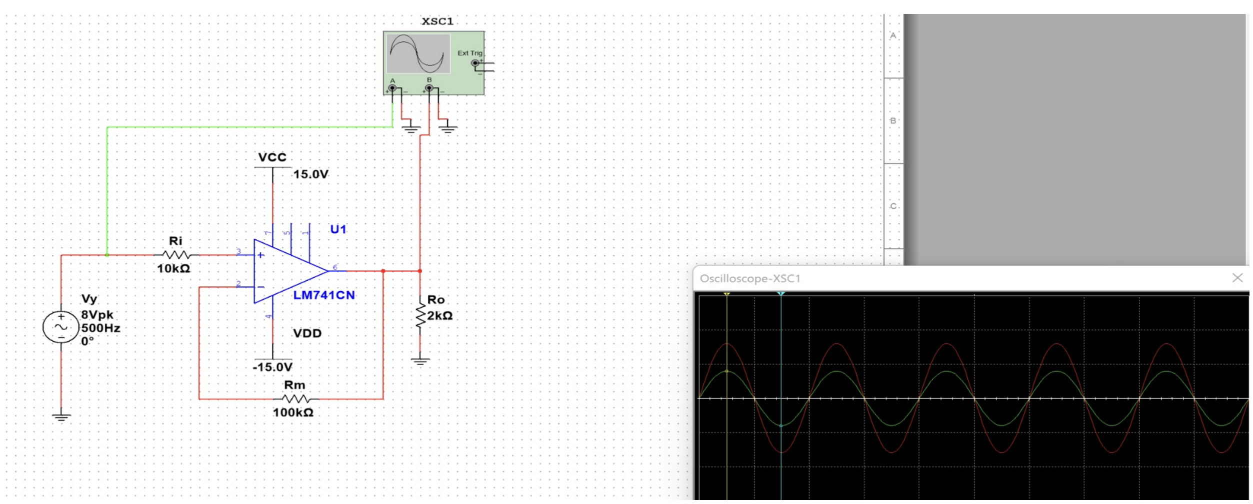
Ro
2kΩ
Vy
8Vpk
500Hz
0°
Oscilloscope-XSC1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500Hz
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Ro
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VDD
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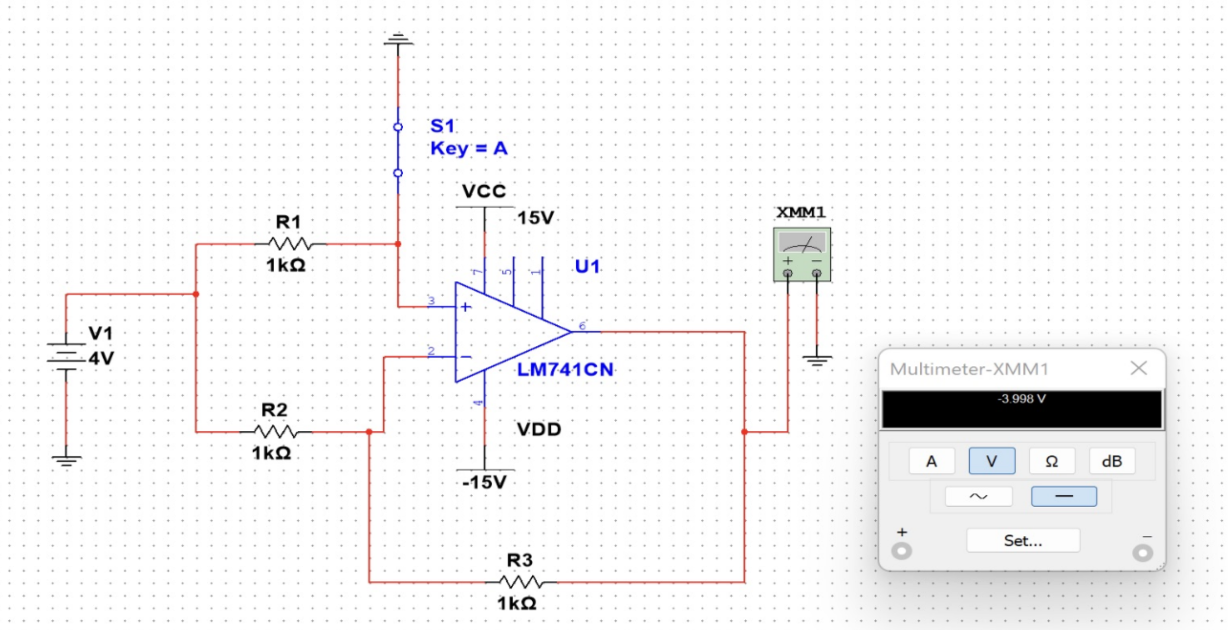
Rm
100kΩ
Oscilloscope-XSC1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R1
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U1
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V1
4V
LM741CN
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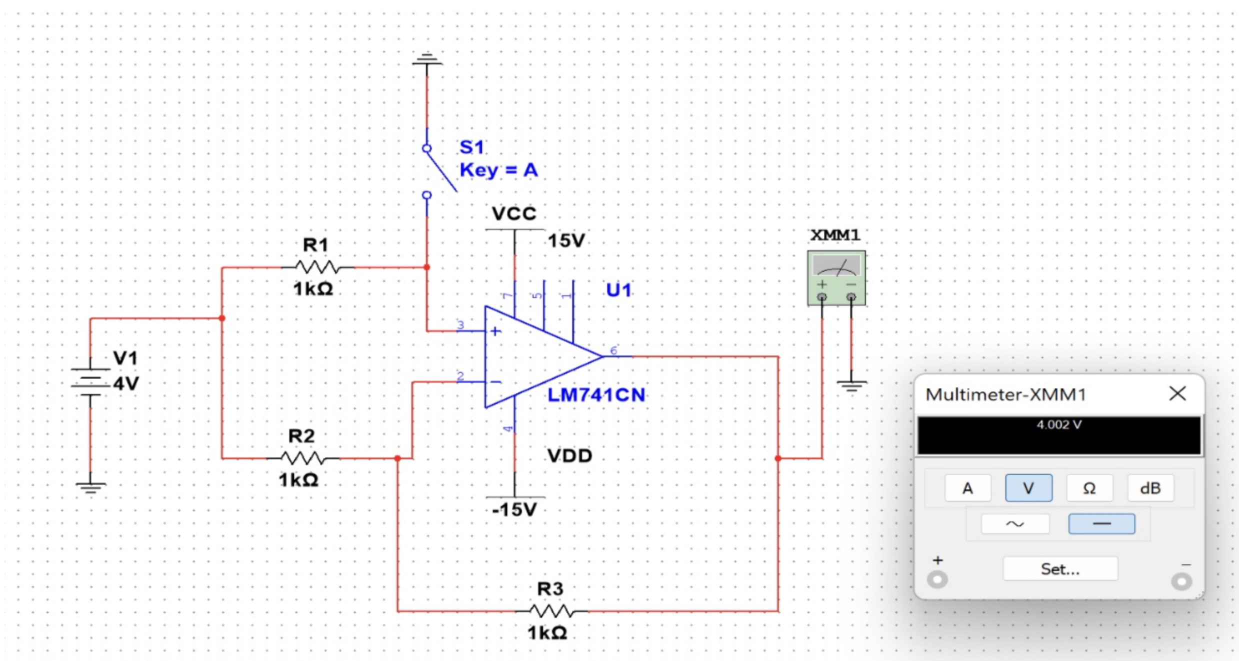
R2
1kΩ
VDD
A
V
Ω
dB
-15V
Set...
R3
1kΩ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VCC
15V
R1
1kΩ
U1
XMM1
V1
4V
LM741CN
Multimeter-XMM1
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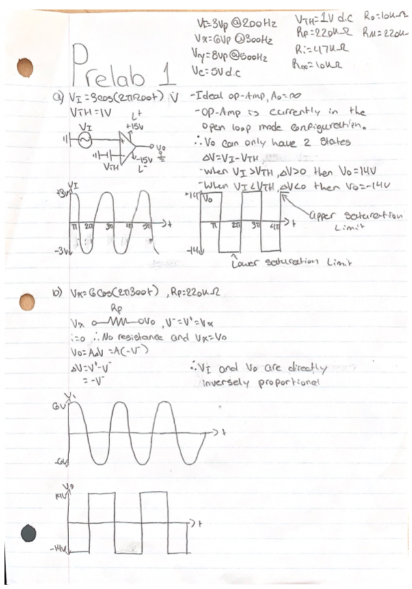
R2
1kΩ
VDD
A
V
Ω
dB
-15V
Set...
R3
1kΩ

5.2 Hasnain Raza’s Pre-Lab: Full Pre-Lab Submitted to D2L



Prelab 1

$V_I = 3V_p$ @ 200Hz
$V_x = 6V_p$ @ 300Hz
$V_y = 8V_p$ @ 500Hz
$V_c = 5V$ d.c
$V_{TH} = 1V$ d.c
$R_p = 220k\Omega$
$R_i = 47k\Omega$
$R_x = 10k\Omega$
$R_o = 10k\Omega$
$R_u = 220k$

a) $V_I = 3\cos(2\pi 200t)$ V
$V_{TH} = 1V$

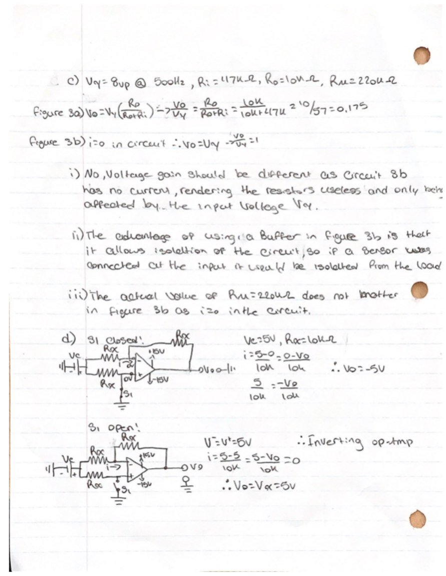
- Ideal op-Amp, $A_o = \infty$
- op-Amp is currently in the open loop mode configuration.

∴ V_o can only have 2 states
$\Delta V = V_I - V_{TH}$
- when $V_I > V_{TH}$, $\Delta V > 0$ then $V_o = 14V$
- When $V_I < V_{TH}$, $\Delta V < 0$ then $V_o = -14V$

b) $V_x = 6\cos(2\pi 300t)$, $R_p = 220k\Omega$

$V^- = V^+ = V_x$
$i = 0$ ∴ No resistance and $V_x = V_o$
$V_o = A\Delta V = A(-V^-)$
$\Delta V = V^+ - V^-$
$= -V^-$

∴ V_I and V_o are directly inversely proportional



c) $V_y = 8V_p$ @ 500Hz, $R_i = 47k\Omega$, $R_o = 10k\Omega$, $R_u = 220k\Omega$

figure 3a) $V_o = V_y\left(\frac{R_o}{R_o+R_i}\right) \rightarrow \frac{V_o}{V_y} = \frac{R_o}{R_o+R_i} = \frac{10k}{10k+47k} = 10/57 = 0.175$

figure 3b) $i = 0$ in circuit ∴ $V_o = V_y \rightarrow \frac{V_o}{V_y} = 1$

i) No, Voltage gain should be different as Circuit 3b has no current, rendering the resistors useless and only being affected by the input voltage V_y.

ii) The advantage of using a Buffer in figure 3b is that it allows isolation of the circuit, so if a sensor was connected at the input it would be isolated from the load

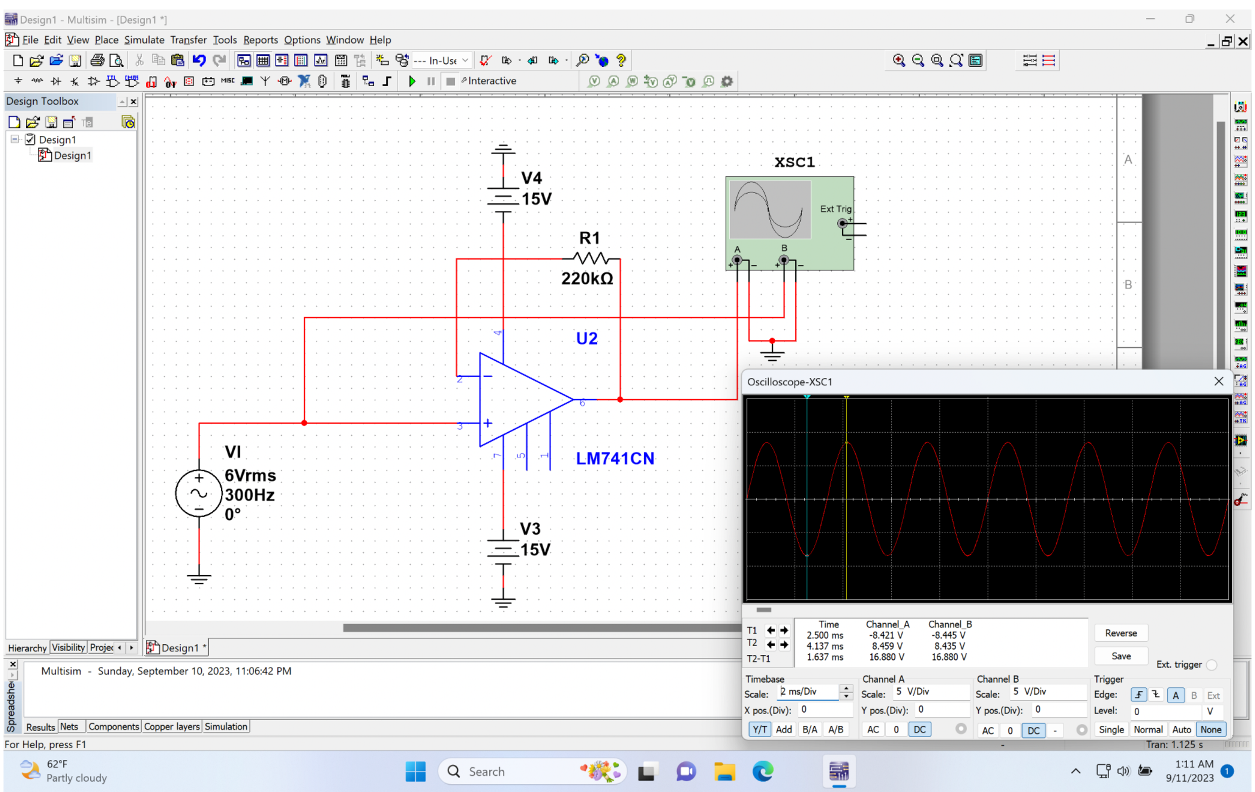
iii) The actual value of $R_u = 220k\Omega$ does not matter in figure 3b as $i = 0$ in the circuit.

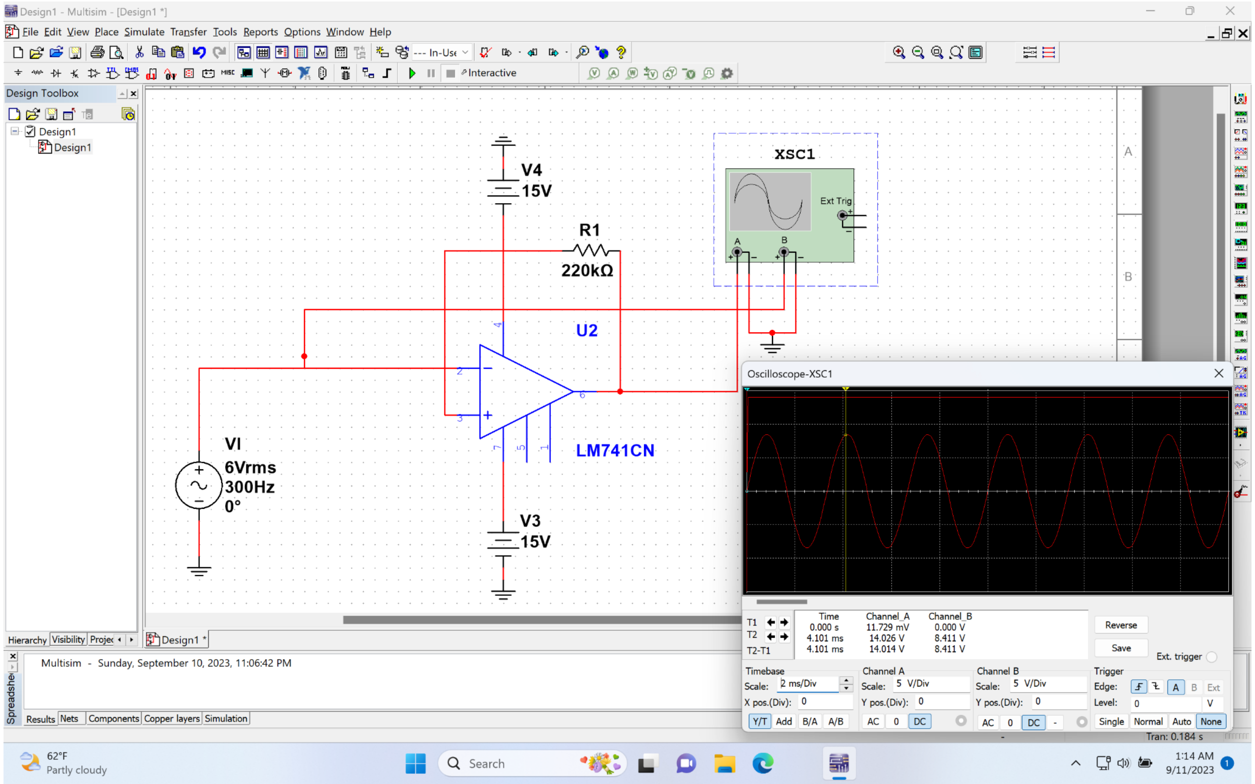
d) S_1 closed:

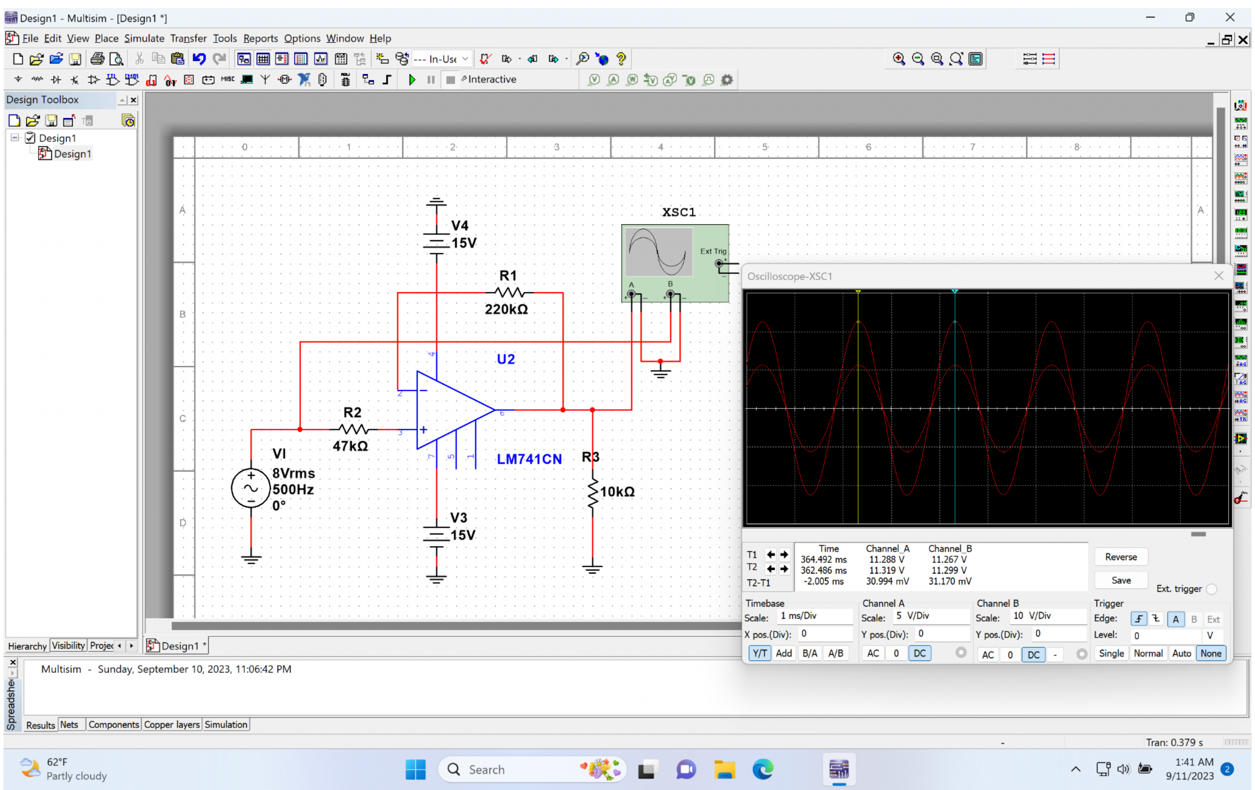
$V_c = 5V$, $R_x = 10k\Omega$
$i = \frac{5-0}{10k} = \frac{0-V_o}{10k}$
$\frac{5}{10k} = \frac{-V_o}{10k}$
∴ $V_o = -5V$

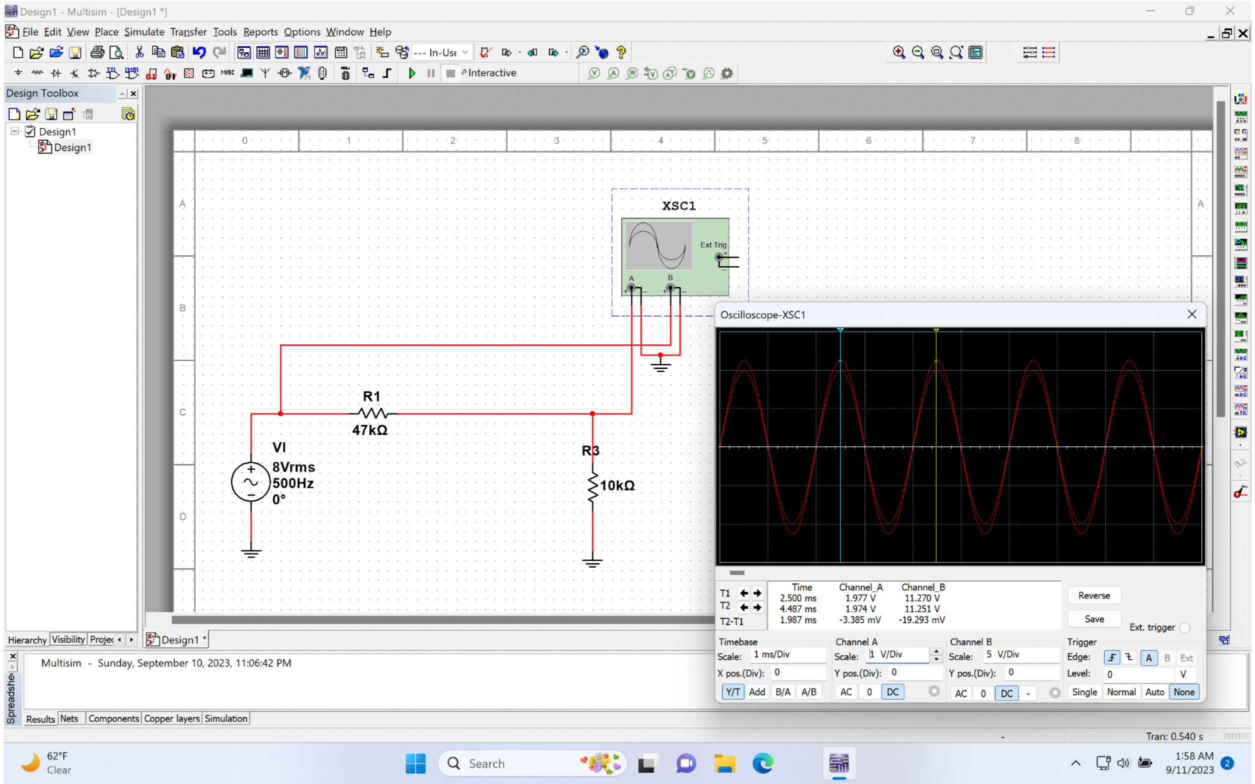
S_1 open:

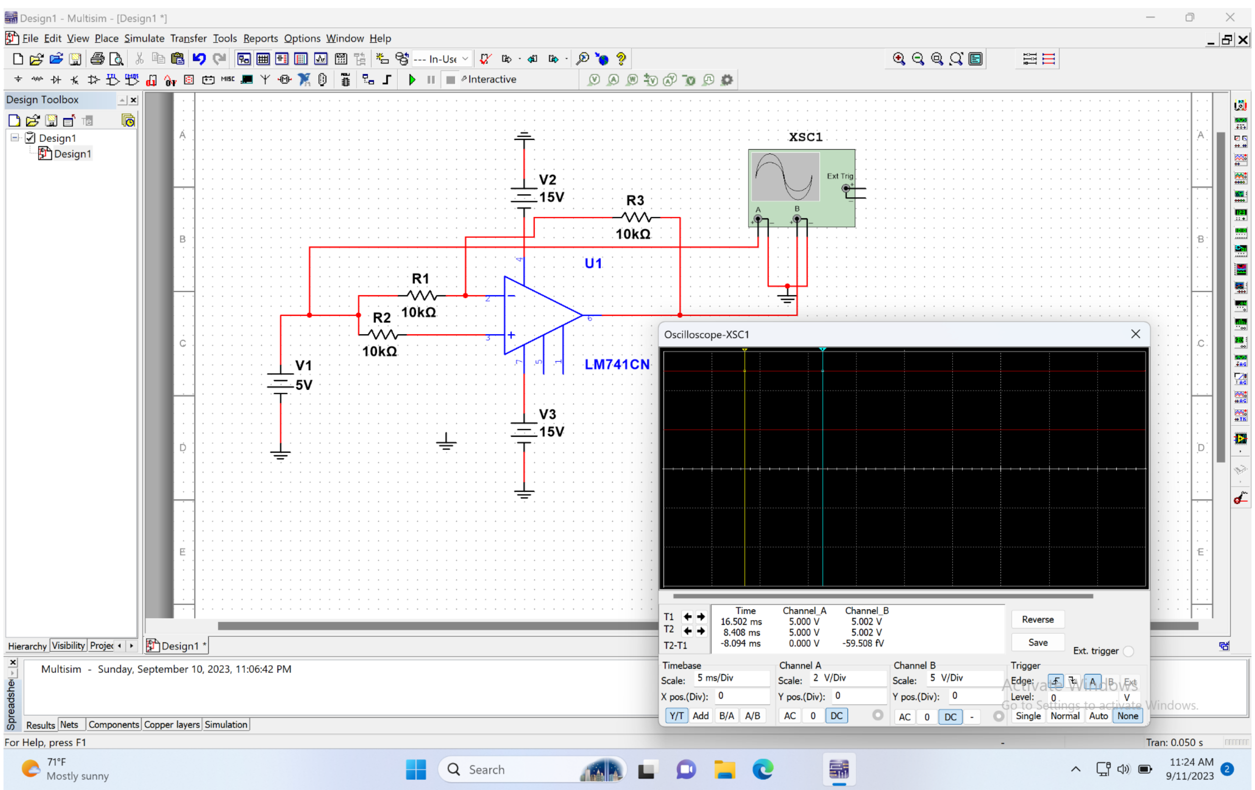
$V^- = V^+ = 5V$
$i = \frac{5-5}{10k} = \frac{5-V_o}{10k} = 0$
∴ $V_o = V_x = 5V$
∴ Inverting op-Amp

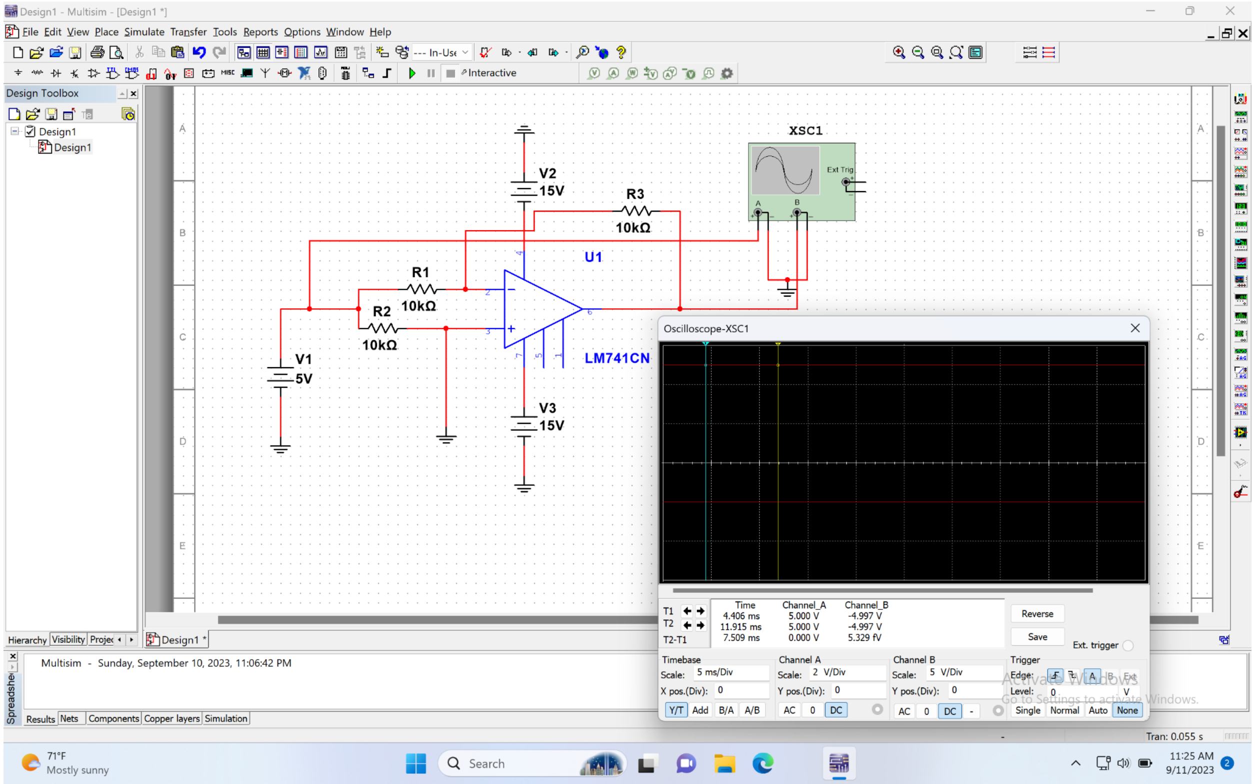


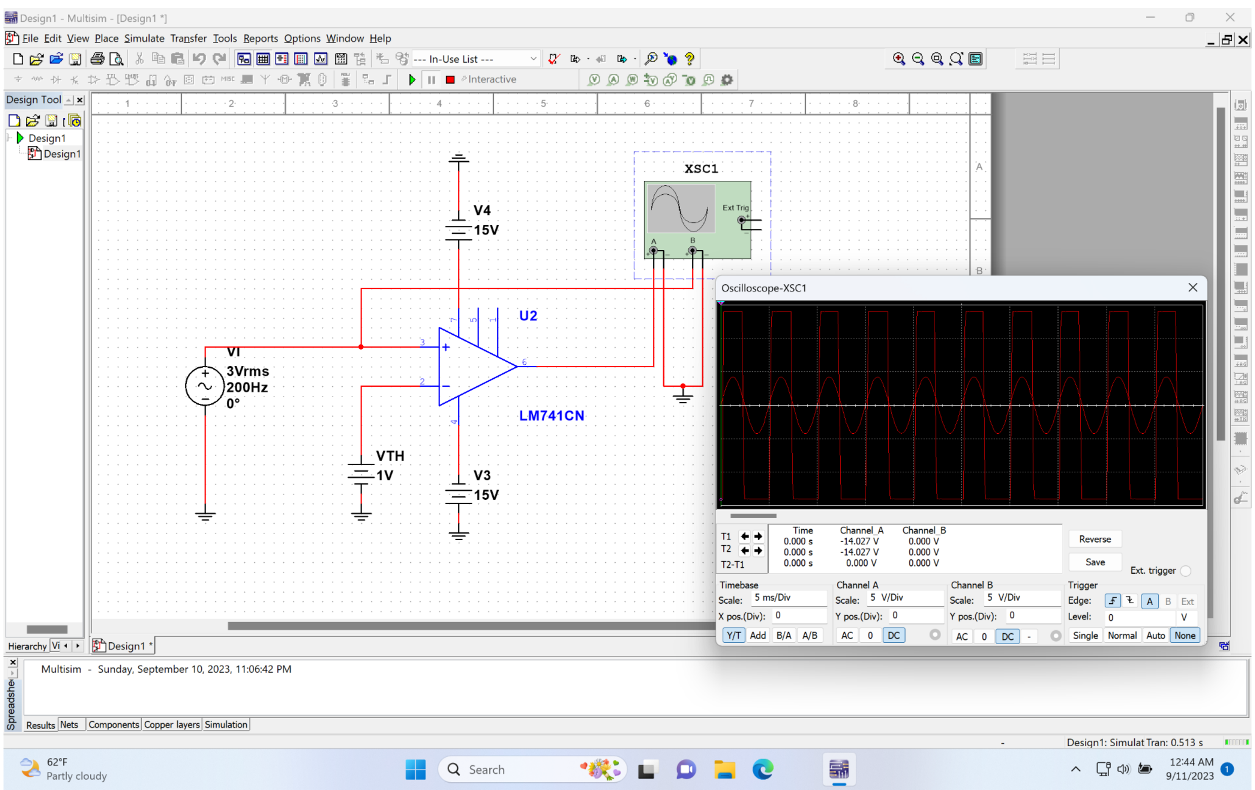

Design1 - Multisim - [Design1 *]
V4
15V
R1
220kΩ
U2
XSC1
VI
6Vrms
300Hz
0°
LM741CN
V3
15V
Oscilloscope-XSC1
Multisim - Sunday, September 10, 2023, 11:06:42 PM


Design1 - Multisim - [Design1 *]
V4
15V
R1
220kΩ
U2
XSC1
R2
47kΩ
VI
8Vrms
500Hz
0°
LM741CN
R3
10kΩ
V3
15V
Oscilloscope-XSC1
Multisim - Sunday, September 10, 2023, 11:06:42 PM


Design1 - Multisim - [Design1 *]
XSC1
R1
47kΩ
VI
8Vrms
500Hz
0°
R3
10kΩ
Oscilloscope-XSC1
Time Channel_A Channel_B
T1 2.500 ms 1.977 V 11.270 V
T2 4.487 ms 1.974 V 11.251 V
T2-T1 1.987 ms -3.385 mV -19.293 mV
Timebase Scale: 1 ms/Div
Channel A Scale: 1 V/Div
Channel B Scale: 5 V/Div
Multisim - Sunday, September 10, 2023, 11:06:42 PM
Tran: 0.540 s
1:58 AM
9/11/2023


Design1 - Multisim - [Design1 *]
XSC1
V2
15V
R3
10kΩ
U1
R1
10kΩ
R2
10kΩ
V1
5V
LM741CN
V3
15V
Oscilloscope-XSC1
Time Channel_A Channel_B
T1 16.502 ms 5.000 V 5.002 V
T2 8.408 ms 5.000 V 5.002 V
T2-T1 -8.094 ms 0.000 V -59.508 fV
Timebase Scale: 5 ms/Div
Channel A Scale: 2 V/Div
Channel B Scale: 5 V/Div
Multisim - Sunday, September 10, 2023, 11:06:42 PM
For Help, press F1
Tran: 0.050 s
11:24 AM
9/11/2023


Design1 - Multisim - [Design1 *]
File Edit View Place Simulate Transfer Tools Reports Options Window Help
Design Toolbox
XSC1
V2
15V
R3
10kΩ
U1
R1
10kΩ
R2
10kΩ
V1
5V
LM741CN
V3
15V
Oscilloscope-XSC1
Time
Channel_A
Channel_B
T1 4.406 ms 5.000 V -4.997 V
T2 11.915 ms 5.000 V -4.997 V
T2-T1 7.509 ms 0.000 V 5.329 fV
Reverse
Save
Ext. trigger
Timebase
Scale: 5 ms/Div
X pos.(Div): 0
Channel A
Scale: 2 V/Div
Y pos.(Div): 0
Channel B
Scale: 5 V/Div
Y pos.(Div): 0
Trigger
Edge:
Level: 0 V
Single Normal Auto None
Multisim - Sunday, September 10, 2023, 11:06:42 PM
Tran: 0.055 s
71°F
Mostly sunny
11:25 AM
9/11/2023


Design1 - Multisim - [Design1 *]
File Edit View Place Simulate Transfer Tools Reports Options Window Help
XSC1
V4
15V
U2
VI
3Vrms
200Hz
0°
LM741CN
VTH
1V
V3
15V
Oscilloscope-XSC1
Time
Channel_A
Channel_B
T1 0.000 s -14.027 V 0.000 V
T2 0.000 s -14.027 V 0.000 V
T2-T1 0.000 s 0.000 V 0.000 V
Reverse
Save
Ext. trigger
Timebase
Scale: 5 ms/Div
X pos.(Div): 0
Channel A
Scale: 5 V/Div
Y pos.(Div): 0
Channel B
Scale: 5 V/Div
Y pos.(Div): 0
Trigger
Level: 0 V
Single Normal Auto None
Multisim - Sunday, September 10, 2023, 11:06:42 PM
Design1: Simulat Tran: 0.513 s
62°F
Partly cloudy
12:44 AM
9/11/2023

Note: Full Pre-Lab Files (including simulations) submitted to D2L on Sunday, September 10, 2023, before the start of the lab (on monday