ASSIGNMENT 1

1. How are the registers collectively placed and referred as in multiple Bus organisation?
2. Which format is used to store data in the Computer System?
3. In which language is the source program written?
4. Which type of register is used by ALU to store the immediate result of an operation?
5. Which bus structure is usually used to connect I/O devices?
6. The control memory has 4096 words of 24 bits each.
   (a) How many bits are there in the control address register?
   (b) How many bits are there in each of the four inputs going into the multiplexer?
   (c) What are the number of inputs in each multiplexer and how many multiplexer are needed?
7. When an instruction is read from the memory, it is called _____. Explain various micro-operation.
8. What will be the contents of register 'ashl' after performing arithmetic shift left to a register containing data $(11001100)_2$.
9. With the help of a neat sketch, explain the working of a 4-bit universal shift register.
10. Design a hardware circuit to implement logical shift, arithmetic shift and circular shift operations. State your design specifications
11. Contents of flag register after execution of following program by 8085 microprocessor shall be:-

    Program

SUB A

MVI B, (01)H

DCR B

HLT

ASSIGNMENT 2

12. Explain with an example, how effective address is calculated in different types of addressing modes.
13. State the condition in which overflow occurs in case of addition & subtraction of two signed 2's complement number. How is it detected?
14. Give the flow chart for add and subtract operation of two signed 2's complement data. Explain the logic of each operation.
15. Explain with neat flow chart the addition and subtraction of floating point numbers.
16. How an interrupt is recognized? Explain the interrupt cycle.
17. The 8-bit registers A, B, C & D are loaded with the value (F2) H, (FF) H, (B9) H and (EA)H respectively. Determine the register content after the execution of the following sequence of micro-operations sequentially.
    (i) A ← A + B, C ← C + Shl(D)
    (ii) C ← C ^ D, B ← B + 1.
    (iii) A ← A – C.
    (iv) A ← Shr(B) ⊕ Cir(D)
18. With neat flow chart, explain the procedure for division of floating point numbers carried out in a computer.
19. What is difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register?

ASSIGNMENT 3

20. How many different addresses are required by the memory that contain 16K words?
21. How many 128 x 8 RAM chips are needed to provide a memory capacity of
22. Explain Booth's multiplications algorithm through an example. Give an example of multiplicant and multiplier for which this algorithm takes the maximum time.
    2048 bytes?

23. Consider a cache (M1) and memory (M2) hierarchy with the following characteristics:
    M1 : 16 K words, 50 ns access time
    M2 : 1 M words, 400 ns access time
    Assume 8 words cache blocks and a set size of 256 words with set associative mapping.
    (i)Show the mapping between M2 and M1
    (ii)Calculate the Effective Memory Access time with a cache hit ratio of h = .95.
24. Multiply (-7)10 with (3)10 by using Booth's multiplication. Give the flow table of the multiplication.
25. Explain in detail the different mappings used for cache memory. Compare them.
26. What is cycle stealing DMA operation?
27. A RAM chip 4096 x 8 bits has two enable lines. How many pains are needed for the integrated circuit package of Draw a block diagram and label all input and outputs pins of the RAM. What is the main feature of random access memory
28. Give the comparison between & examples of hardwired control unit and micro programmed control unit.
29. Give the flow table for register contents used in implementing booth's algorithm for the multiplier = - 6 and multiplicant = + 5.
30. The access time of a cache memory is 120 ns and that of main memory 900 ns. It is estimated that 80% of the memory requests are for read and remaining 20% for write. The hit ratio for read access only is 0.9. A write-through procedure is used.
    (i) What is the average access time of the system considering only memory real cycles?
    (ii) What is the hit ratio taking in to consideration the write cycle?
    (iii) What is the average access time of the system for both read and write requests.