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Group - C7

MPMC
Microcontroller and Microprocessors
Assignment - 2

Ques 1. What are the differences between 8085 and 8086 ?

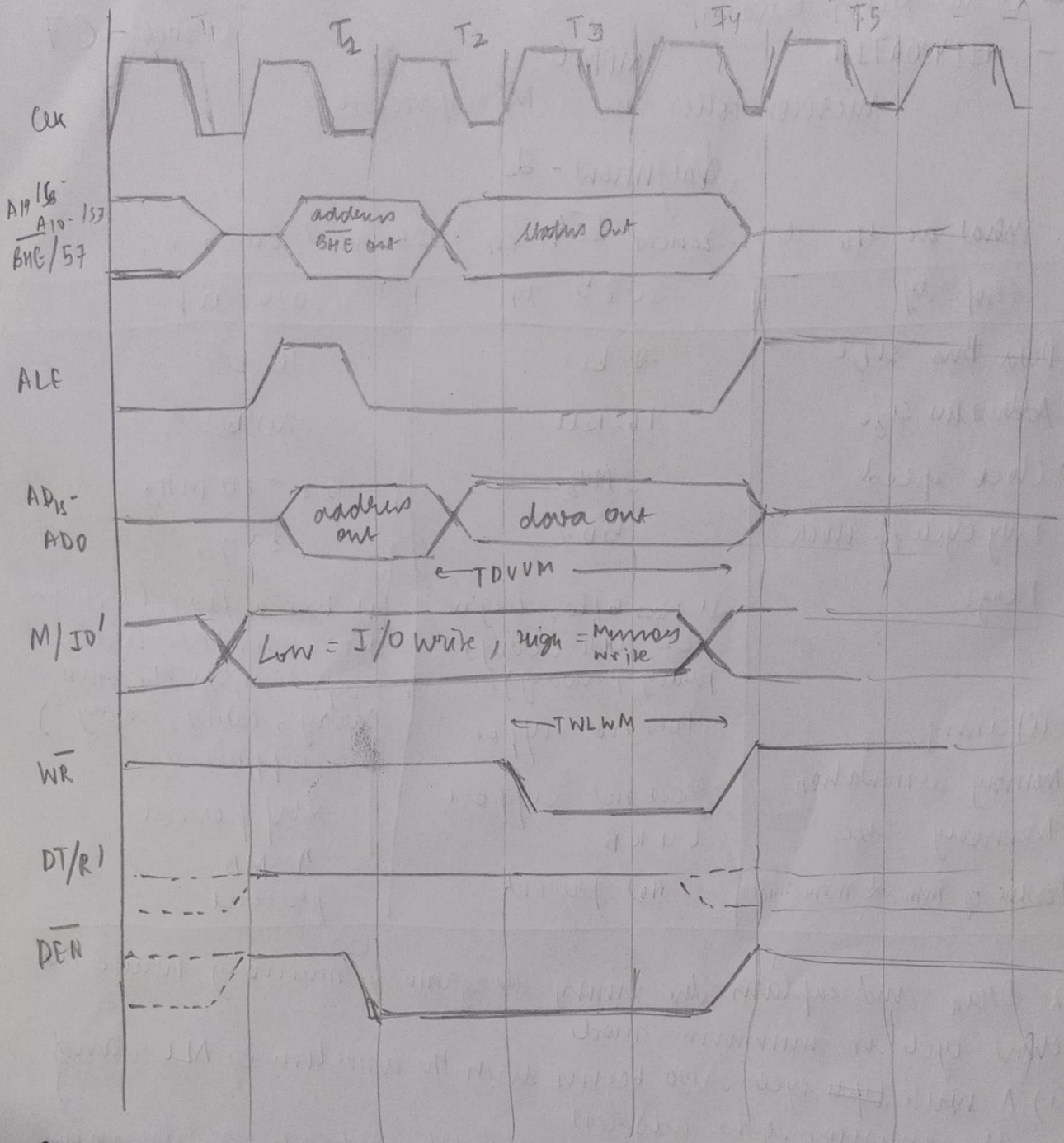
Ans

Property	8085 μp	8086 μp
Data Bus size	8-bit	16-bit
Address Bus size	16-bit	20 bit
Clock speed	3 MHz	5.8 - 10 MHz
Duty cycle for clock	50%	33%.
Flags	It has 5 flags (sign, zero, aux-carry, parity, carry)	It has a flags (overflow, direction, Interrupt, trap, sign, zero, Aux. carry, Parity, carry)
Pipelining	Does not support	supported
Memory Segmentation	Does not support	supported
Memory size	64 KB	1 MB
Presence of min & max mode	Not present	present

Ques 2. Draw and explain the timing diagram of memory write machine cycle in minimum mode.

Ans i) A write cycle also begins with the assertion of ALE and the emission of the address.
ii) The M̄/IO signal is again asserted to indicate a memory or I/O operation.
iii) In T2; after sending the address in T1, the processor sends the data to be written to the addressed location.
iv) The data remains on the bus until middle of T4 state.
v) The WR becomes active at the beginning of T2.
vi) The BHE and A0 signals are used to select the proper byte or bytes of memory or I/O word to be read or write.

IO/M	RD'	WR'	Transfer type
0	0	1	I/O read
0	1	0	I/O write
1	0	1	memory read
1	1	0	memory write



Ans 3. List advantages of memory segmentation in 8086

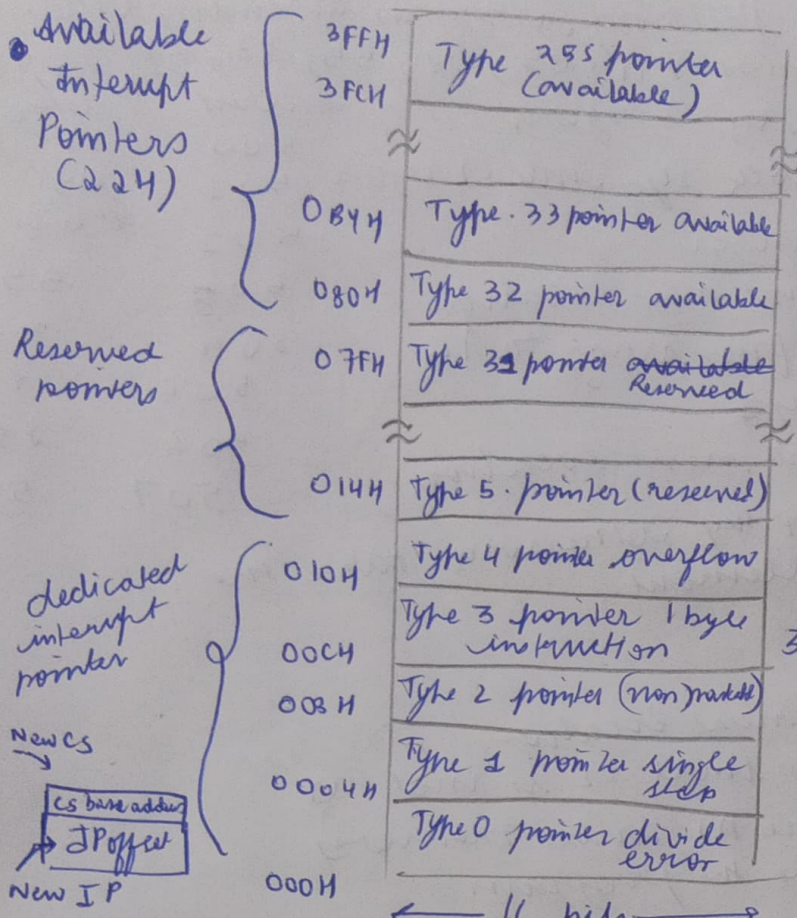
a) It allows the memory addressing capacity to be 1MB even though the address associated with individual instruction is only 16-bit

b) It allows instruction code, data, stack, and portion of program to be more than 64kB long by using more than one code, data, stack segment and extra segment.

c) It facilitates use of seperate memory area for program, data and stack.

d) It permits a program or its data to be put in different areas of memory, each time the program is executed.

Ans 4. Draw and explain the interrupt vector table of 8086. Also explain the interrupt response sequence of 8086.



1) The interrupt vector table is the link between an interrupt type code and the procedures that has been designed to service interrupts associated with that code. 8086 supports total 256 bytes.

2) For each type it has to require 4 bytes i.e. double pointer word. This double word pointers contains the address of the procedure that is to service interrupts of that type.

3) The higher addressed word of the pointer contains the base address of the segment containing the procedures. This base address as New ip.

4) The lower addressed word contains the procedures do offset from the beginning of the segment this offset is normally called near

5) Means new CS : New IP provides new physical address from where user ISR routine will start

6) 4 for each type, four byte. (4 for New is and 2 required; thereafter interrupt pointer table occupies up to the first 1k bytes of base memory.

7) The total interrupt vector table is divided into three groups.
   (a) Dedicated Interrupt (Int 0 — INT4)
   (b) Reserved Interrupt (Int 5 - Int 31)
   (c) Available Interrupt (Int 32 - - Int 255)

Interrupt Response Sequence

1. The value of flag register is pushed into the stack. It means that the first value of SP is determined first value of SP is differentiated address of stack segment
2. The value of starting memory address of cs (code segment) is pushed into the stack.
3. The value of I/P (instruction Pointer) is pushed into the stack.
4) IP is loaded from word location (interrupt type) + 04.
5) CS is loaded from the next weird location.
6) Interrupt and TRAP flag are reset to 0.

Ans 5. WAP in 8086 to sort the following array in ascending order (All numbers in hexadecimal format) 11, 05, 08, 55, 33, 58, 85, 53

```
MOV SI, 500  : Point 500 using SI register
MOV CL, [SI] : Load the block size into CL register
MOV CH, 00   : Clear CH Register
INC SI       : Increase SI to point next location
MOV AL, [SI] : Load data from array to AL
DEC CL       : decrease CL by 1
INC SI       : Point to next next location
H: CMP AL, [SI] : If CY=0, jump skip otherwise take the
Baby Link :       memory element.
JNC SKIP  : If CY=0
            jump to skip
MOV AL, [SI]
SKIP: INC SI   : Point to next location
      LOOP L1  : Go to loop until CL is not 0
      MOV [100], AL : Store AL into memory
      HLT      : Terminate the program.
```

Address	data
500	11
501	05
502	08
503	55
504	33
505	58
506	85
507	53

Ans 6. How will 8086 use a byte from EVEN and ODD memory banks. Explain?

Ans The 8086 processor provides a 16-bit data bus. So it is capable of transferring 16-bits in one cycle but each memory location is only of a byte (8 bit), therefore we need two access cycles to access 16 bit data (8 bits each), therefore we need two cycles of access 16 bits from different memory location. The solution to this is memory banking. Through memory banking, goal is to access 2 consecutive memory location in one cycle (transfer 16 bits). The memory chip is divided equally into parts (banks) One of the banks contains even addresses called even bank and the other called / contain odd bank. Even bank always gives lower bytes so, even bank is also called lower bank. and Odd bank is also high band (HB)

The last significant bit of address (A_0 is what is needed for byte selection) is reserved for bank selection. Therefore $A_0 = 0$ will select ~~even~~ Bank. The BHE signal is used for the selection of odd banks. The processor will use a combination of these 2 signals to divide type of data transfer

BHE	A_0	Type of transfer
0	0	16-bit transfer from both HB & LB
0	1	8-bit data transfer from HB
1	0	8-bit data transfer from LB
1	1	None

the interrupt response sequence of 8086.

In this case, the first machine cycle generate an odd address ($A_0 = 1$) transfer lower order 8 bit data bus on a higher order 8-bit data bus or a higher order data bus. In the second machine cycle the higher order data bus will be transferred to the lower order data bus

Ques 7. Draw and explain the flag register of 8086

Bits	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Flags					O	D	I	T	S	Z		AC		P		CY

the flag register is one of the special purpose register. The flag bits are changed to 0 or 1 depending upon the value of result after arithmetic or logical operations

STATUS FLAG. S – After any operation if MSB is 1, then indicates the number is -ve and flag is set to 1

Z – If total register is 0, then only Z flag is set.

AC – When some arithmetic operations generates carry after half and sends it to upper half. the A will be 1.

P – This is even parity flag when result have even number of 1 it will be set to 1 otherwise 0.

CY – This is carry bit if some operation generating carry after operation this flag is set to 1.

O – The overflow flag is set to 1 when result of signed operation is too large to fit.

CONTROL FLAGS:

D – This is direction flag. This is used in string related operations D=1, then string will be accessed from higher memory address to lower address if D=0, this up will do reverse.

I – This is interrupt flag. If I = 1, the up will recognize the interrupts from peripheral for I = 0, the interrupt will be ignored.

T – The TRAP flag is used for on-chip debugging. When T=1 it will work in a single step mode. After each instruction, one internal interrupt is generated it helps to execute our program instructions

Ans 8. What are logical and physical address? How the physical address are generated?

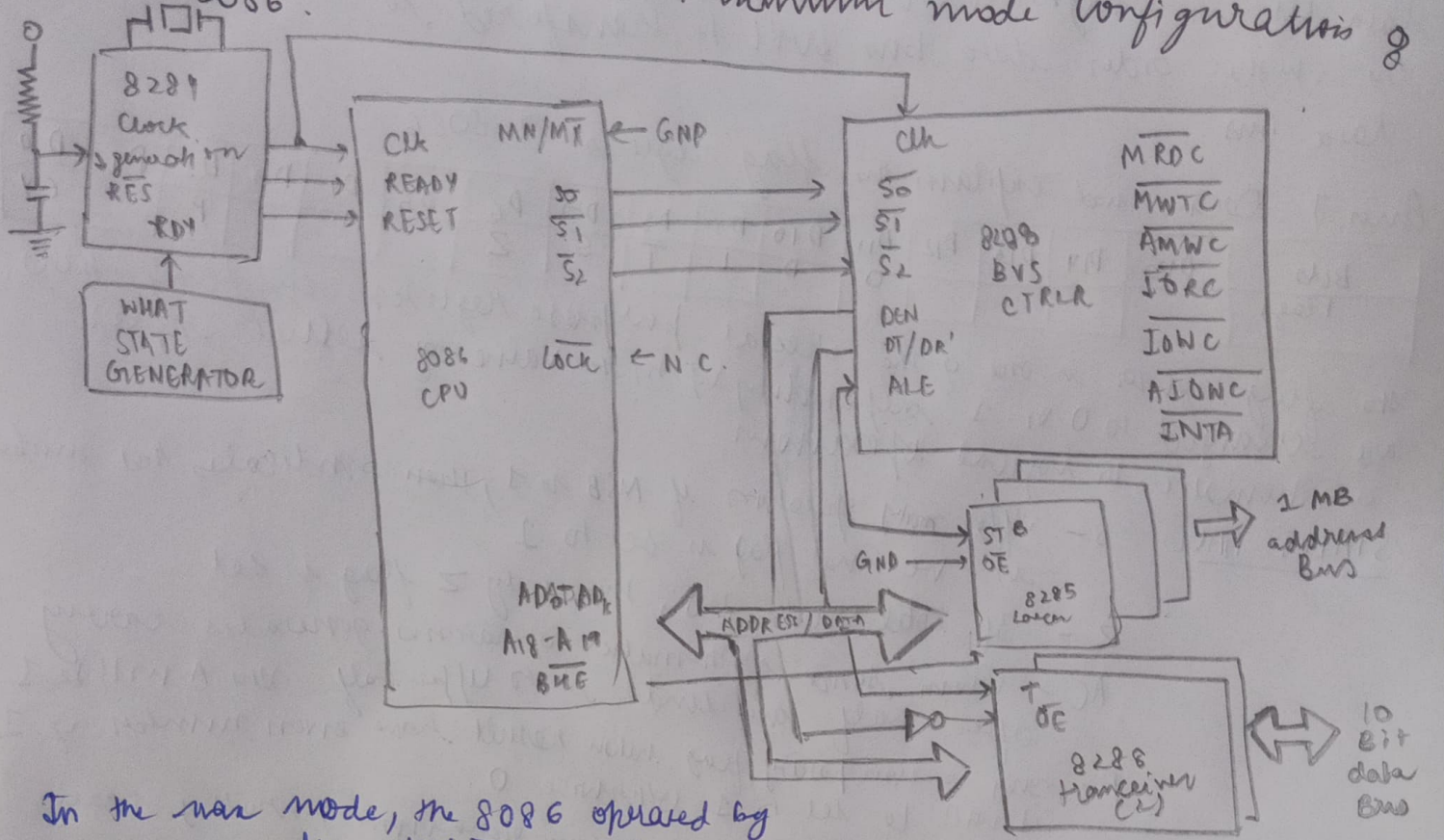
The logical address is generated by the processors for the execution of program. Logical address contained in one of 16-bit contents of the segment registers Cs, Ds, Es and Ss

The base segment is contained in one of the 16 bit content of segment registers Cs, Ds, Es and Ss.

The physical address or the real address is formed by the

and is primarily used for accessing memory.

Ans 9. Draw and explain maximum mode configuration of 8086.



In the max mode, the 8086 operated by ~~loading~~ strapping the MN/$\overline{MX}$ p/n to ground. In this mode, the processor derives the status signal S_2, S_1 and S_0. Another chip called bus controller derives the control signals using this status information. In the max mode, there may be more than 1 processor. In the system configuration the other components system organization is shown in figure and are same as minimum mode system.

The basic functions of the bus controller chip IC8288, is to derive control signals like RD* and WR* (for memory and I/O devices), DEN* DT/R*, ALE etc. using the information made available by the CPU. It derives the O/P of ALE, DEN*, DT/R*, MWTC*, AMWC*, IORC*, IOWC* and AIOWC*. The AEN*, IOB and CEN pin are especially useful for mp systems. AEN* and IOB generally grounded CEN pin is usually tied to +5 V.