ASSIGNMENT -4

EC7

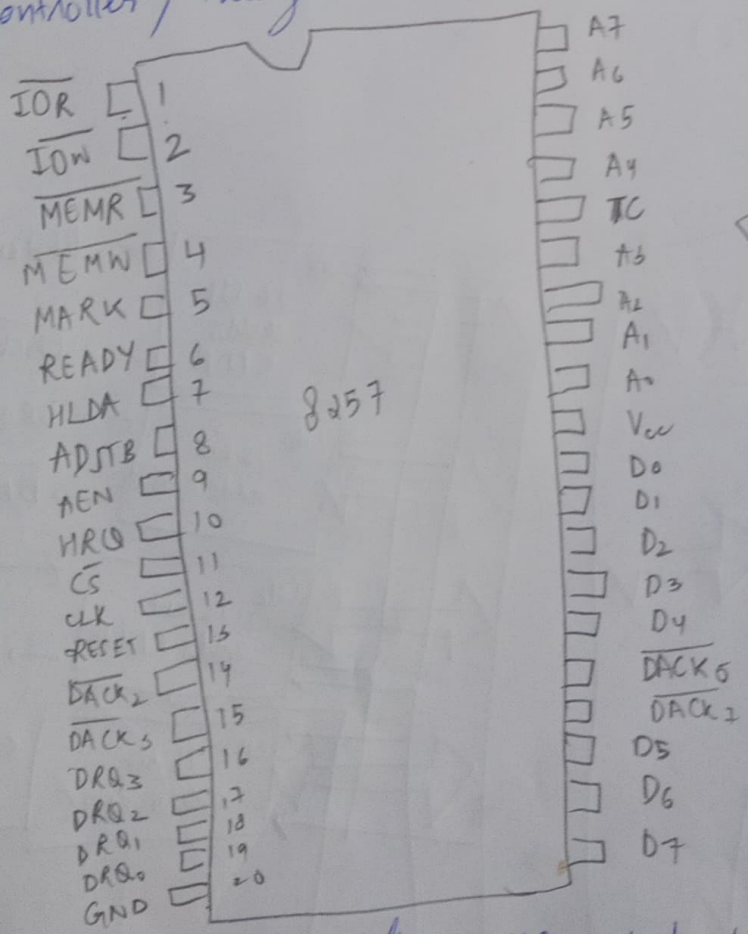
Microprocessor & Micro controller (CETEE-310)

(Name - Syeda Reeha Qusar) (Roll no. - 14114802719)

Q1 Explain the functional block diagram of 8257 with pin details.

Ans 8257 Pin diagram

Data Bus ($D_0 - D_7$): These are bi-directional tri-state signals connected to the system data bus. When CPU is having control of system bus it can access contents of address register, status register, mode set register of a channel count registers of it can also program, control registers of DMA controller, through the data bus.



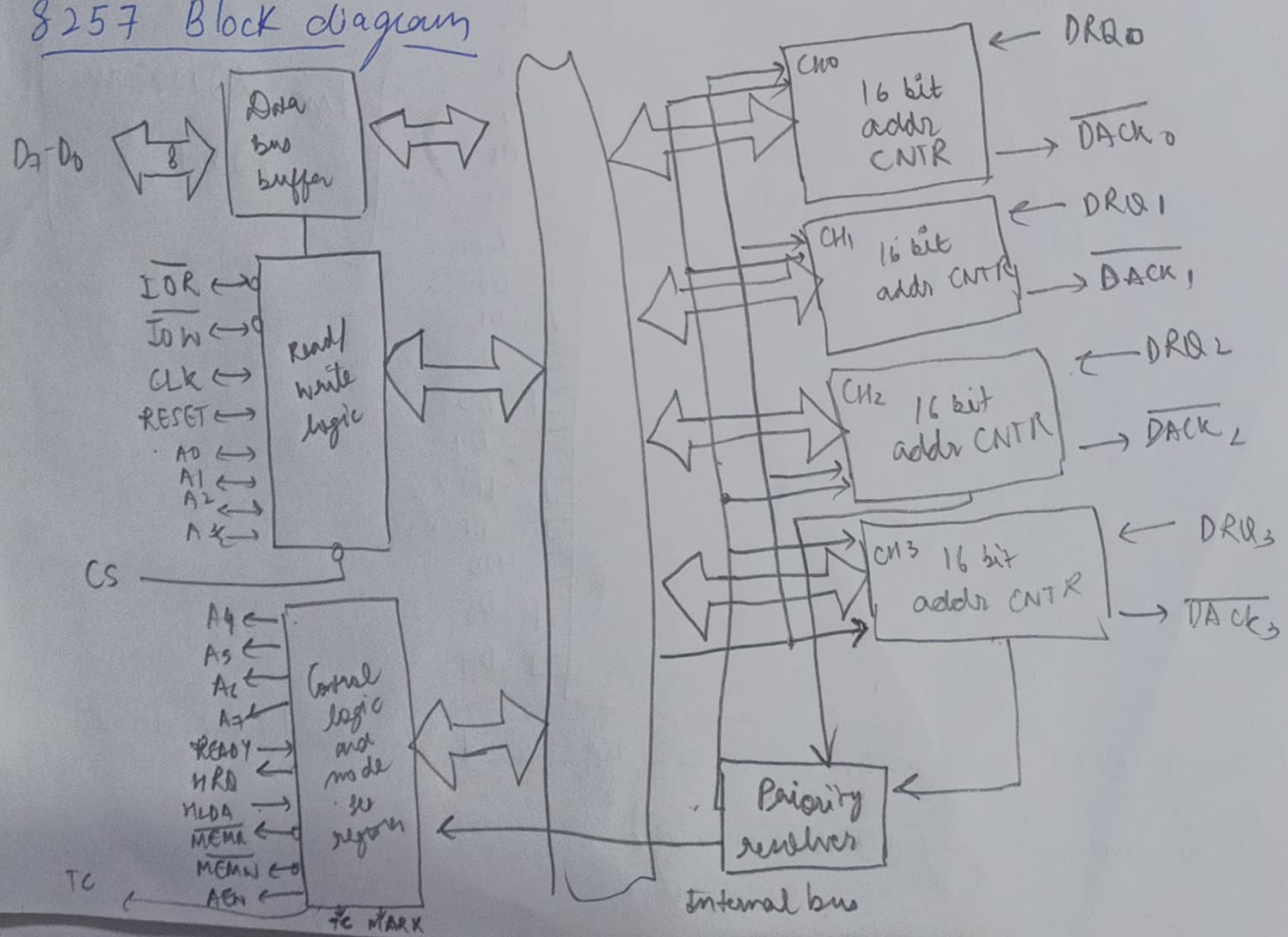
[Pin Diagram 8257.]

During DMA cycles these line are used to send the most significant bytes of the memory.

8257 Pin description

- → Address Bus ($A_0 - A_3$ & $A_4 - A_7$)
- → Address Strobe (ADSTB)
- → Address Enable (AEM)
- → Memory Read & Memory Write (MEMR, MEMW)
- → I/O Read & I/O Write (IOR & IOW)
- → Chip Select (CS)
- → Reset
- → Ready
- → Hold Request (HRQ)
- → Hold Acknowledge (HLDA)
- → $DREQ_0 - DREQ_3$
- → $DACK_0 - DACK_3$
- → Terminal Count (TC)
- → Mark

8257 Block diagram



Data Bus Buffer

It is a tri-state, bi-directional, eight bit buffer which interfaces the 8257 to the system data bus. In the slave mode, it is used to transfer data between microprocessor & internal register of 8257. In master mode, it is used to send higher byte address (A_8-A_{15}) on the data bus.

Write logic

When the CPU is programming or reading one of the internal register of 8257 Pin diagram, the Read/Write logic accept the I/O Read or I/O Write signal, decodes the least significant four address bits (A_0-A_3) & either write the content of the data bus into the addressed register or places the content of the addressed register onto the bus.

During DMA cycles the Read/write logic generates the I/O read & memory write or I/O write & memory read signal which control the data transfer b/w peripheral & memory device.

8257 DMA Controller operating Modes

The 8257 Pin diagram provides four identical channels, labeled CH_0 to CH_3. Each channel has two sixteen bit register

(1) A DMA address register
(2) A terminal count register

DMA address register

shows the format of DMA address register. It specifies the address of the first memory location to the accessed.

The value into the low Order 14 bits (C_{13}-C_0) of the terminal count register specifies the no. of DMA cycles minus one before the terminal count (TC) output is activated.

Control logic

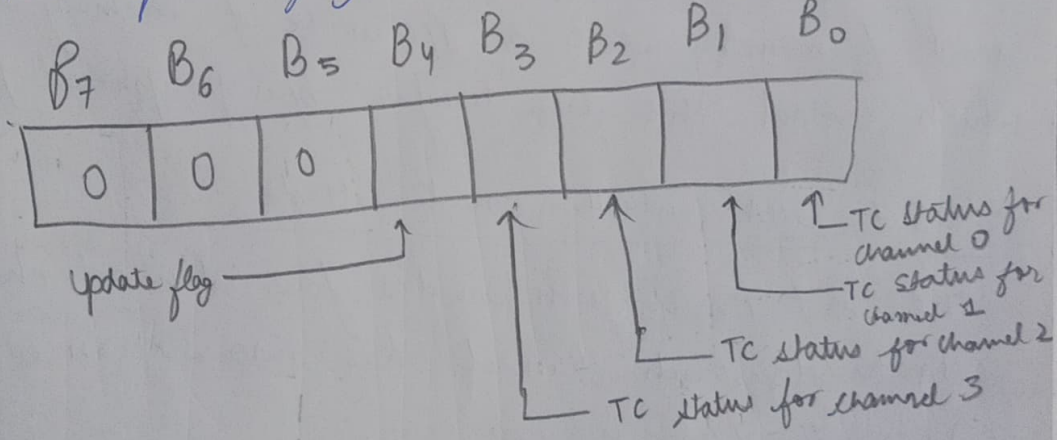
It controls the sequence of operations during all DMA cycle by generating the appropriate control signal & the 16-bit address that specifies the memory location to be accessed.

Mode Set Register

Gives the format of mode set register. Least significant four bits of mode set register, when set, enable each of the four DMA channels. Most significant four bits allow four different options for the 8257 P.I.C diagram

Status Register

Shows the Register format. As said earlier, it indicates which channels have reached a terminal count condition & includes the update flag described previously.



Status Register

Priority Resolver

It resolves the peripherals request. It can be programmed to work in two modes, either in fixed mode or rotating priority mode.

Q2 what are the additional features of 80186 compared to 8086.

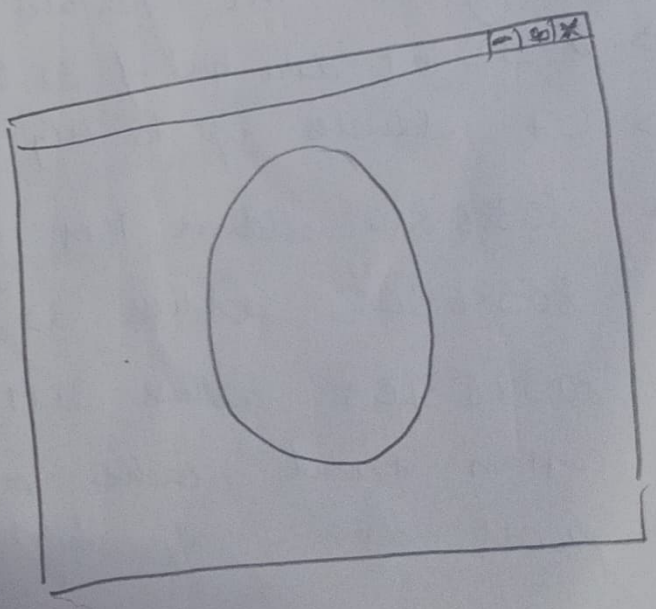
Ans The 80186 inst a processor, it's a micro controller. It integrates things like the interrupt controller on the chip. The 8086, with a number of enhancements like a multi-bit immediate shift instruction.

The 80286 is a whole diffuent beast. It adds 16-bit protected mode, & could address 16 MiB instead of the just 1 MiB of the 8086/80186. It shared the extented instruction of the 80186 & has a number of extra instruction itself, mostly ones concerning the protected mode.

Q3 Write a program to calculate Area of a circle ceprocesser 8087.

Ans

```
diamtr  Real 4  12.93
;Get area of circle:  ,Area = PI * (D/2)2
        fld1
        fadd    st,st
        fdivr   diamtr
        fmul    st,st
        fldpi
        fmuL
```



Q4. Discuss the basic differences b/w 80286 & 80386 microprocessor.

Ans

Specifications	80286	80386
CPU Speed	6 to 25 MHz	12 to 40 MHz
Cores	1	1
RAM	16 MB	4 GB
Functional Units	4	6
Pipeline Stages	3	3
Cache off chip	0	Yes (support)
Cache on chip	0	0
Transistor	134,000	275,000

80386 microprocessor

Following are the features of 80386 microprocessor

→ 32 bit data bus & 32 bit memory address

→ It addresses up to 4G bytes of memory

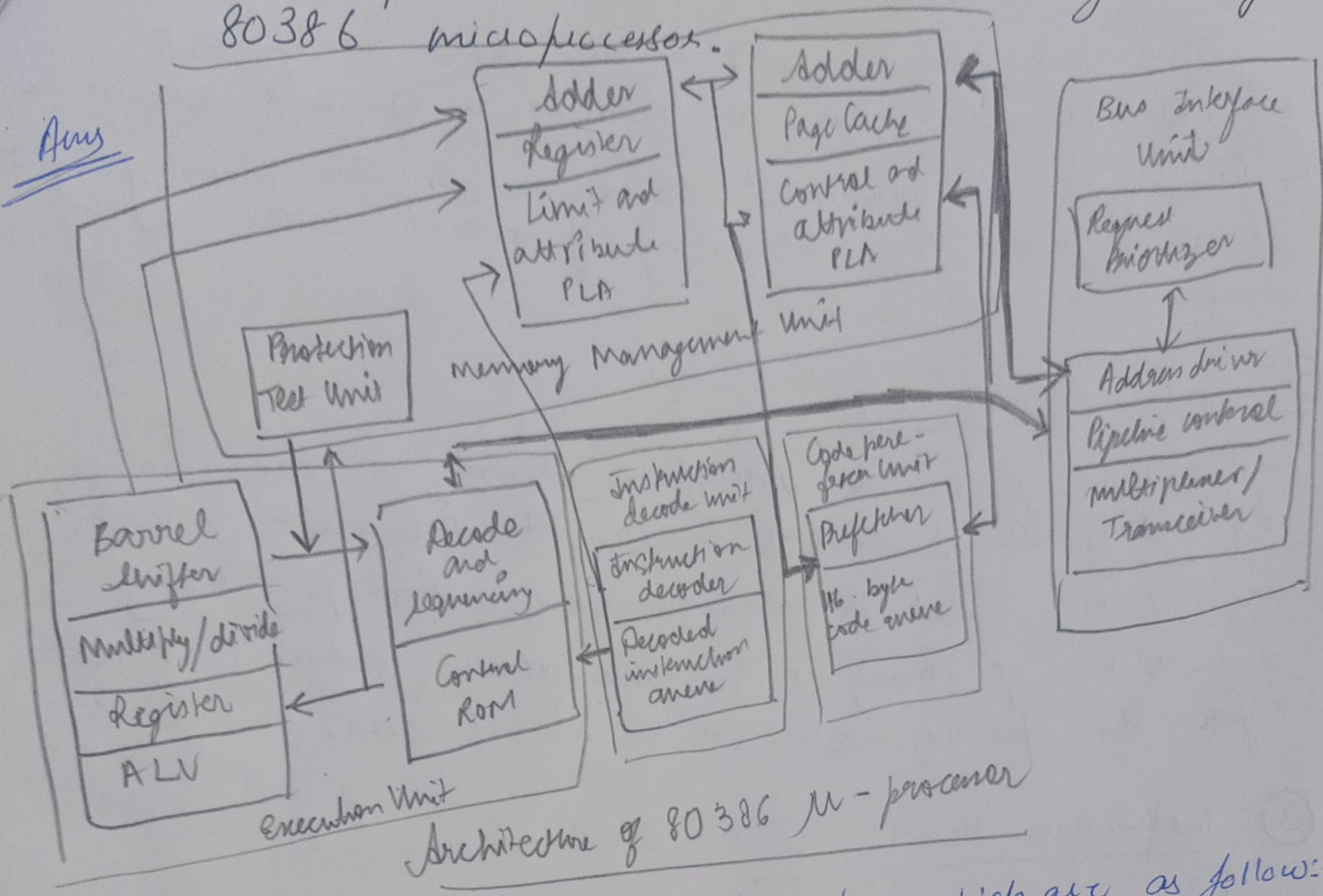
→ 80386 SX: address 16M bytes of memory

→ 80386 SL: address 32 M bytes of memory

→ 80386 SLC: address 32 M bytes of memory. It contain internal cache memory which allow it to process data at higher rates.

Q5 Draw & Explain the block diagram of 80386 microprocessor.

Ans



Architecture of 80386 M-processor

Basically, it has 6 functional units which are as follow:-

1. Bus Interface Unit
2. code fetch Unit
3. Instruction Decode Unit
4. Execution Unit
5. Memory Managment Unit

As we already discussed that the 80386 processes the ability of 3 stage pipelining thus performs fetching, decoding & execution simultaneously along with memory mangment & bus accessing.

(1) Bus Interface Unit

The bus interface unit or BIU holds a 32-bit bidirectional data bus as well as a 32-bit address bus. The BIU connects the peripheral devices through the memory Unit & also control the interfacing of external buses with the coprocessors.

(2) Code Prefetch Unit

This Unit fetches the instructions stored in the memory by making use of system buses. As the unit fetches one double word in a single access. But prefetching of instruction & storing it in the queue reduce the wait for the upcoming instruction to almost zero.

(3) Instruction Decode Unit

We know that instruction in the memory is stored in the form of bits. So this unit decodes the instruction stored in the prefetch queue.

(4) Execution Unit

The decoded instructions are stored in the decoded instruction queue. So, these instruction are provided to the execution Unit in order to execute the instructions.

(5) Memory Management Unit

This unit has two separate unit within it.

1. Segmentation Unit
2. Paging Unit

Segmentation Unit

The Segmentation Unit plays a vital role in the 80836 microprocessor. It offers a protection mechanism in order to protect the code or data present in the memory from application programs.

Paging Unit

The paging Unit operates only in protected mode & it changes the linear address into a physical address. As the programmer only provides the virtual address & not the physical address.

Q6 Discuss in detail, the evolution of Pentium processors with regards to the new features added in every model, ie Pentium I to Pentium IV.

Ans

1971-81 - The 4004, 8008 & 8800
1978-82 - iAPX 86, 8088 & 80186
1981 - iAPX 432
1982 - 80286
1985-94 - 386 & 376
1989 - 486 & i860
1993 - Pentium
1994-99 - Bumps in the road
1995 - Pentium Pro
1997 - Pentium II & Pentium II Xeon
1998 - Celeron
1999 - Pentium III & pentium III Xeon
2000 - Pentium 4
2001 - Xeon
2001 - Itanium