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MPMC (Microprocessors and Micro Controllers)
Assignment - 1

Ques 1. Why lower order address buses ($A_0 - A_7$) is multiplexed with data bus ($D_0 - D_7$) and how it is demultiplexed?

Ans The main reason of multiplexing address and data bus is to reduce the number of pins for address and data and dedicated those pins for other several functions of microprocessor. These multiplexed set of lines used to carry the lower order 8-bit address as well as data bus.
They are demultiplexed using ALE (Address Latch Enable) pin.

Ques 2. How many machine cycles are required for executing JNC instruction in both cases when condition is true or false?

Ans JNC (Jump Not Carry) required 3-bytes, 3-Machine cycles (opcode fetch, Memory read, Memory Read) and 10-T states for the execution.

Ques 3. Explain the difference b/w hardware & software interrupts.

Ans

Hardware Interrupts	Software Interrupts
1) An interrupt that is generated from external device.	1) A type of interrupt caused by an instruction in the program.
2) Asynchronized events	2) Synchronized events
3) Do not increment the program counter	3) Increase the program counter
4) Do not get a higher priority	4) Get a higher priority

Ques 5. Write a program in 8085 to convert BCD number to binary number.

Ans
```
LXI  SP, 80FFH
LXI  H, 802BH
LXI  B, 802CH
MOV  A, M
CALL BCDBIN
STAX B
HLT
```

```
PUSH B
MOV B,A
ANI 0FH
MOV C,A
MOV A,B
ANI F0H
RRC
RRC
RRC
RRC
MOV D,A
XRAA
MVI E,0AH
ADD E
DCR D
JNZ LOOP
ADD C
POP B
RET
```

Ans 6. Explain the following Instructions

Ans 1) LHLD: Load the HL pair using direct addressing from the memory location so, previous content of HL pair will get updated with new 16-bits value.

2) XCHG: Used to exchange contents of HL pair with DE register pair

3) XTHL: This instruction exchanges the contents of the top 2 locations of the stack with contents of HL pair register.

4) PCHL: The control of program is transferred to memory address equivalent to HL register pair content.

5) DAA: It exchanges binary value to BCD in the accumulator

6) SIM: Set interrupt mask. For partially disabling interrupts like RST 7.5, RST 6.5, RST 5.5.

Ans 7. Indentify the content of accumulator of following instruction:

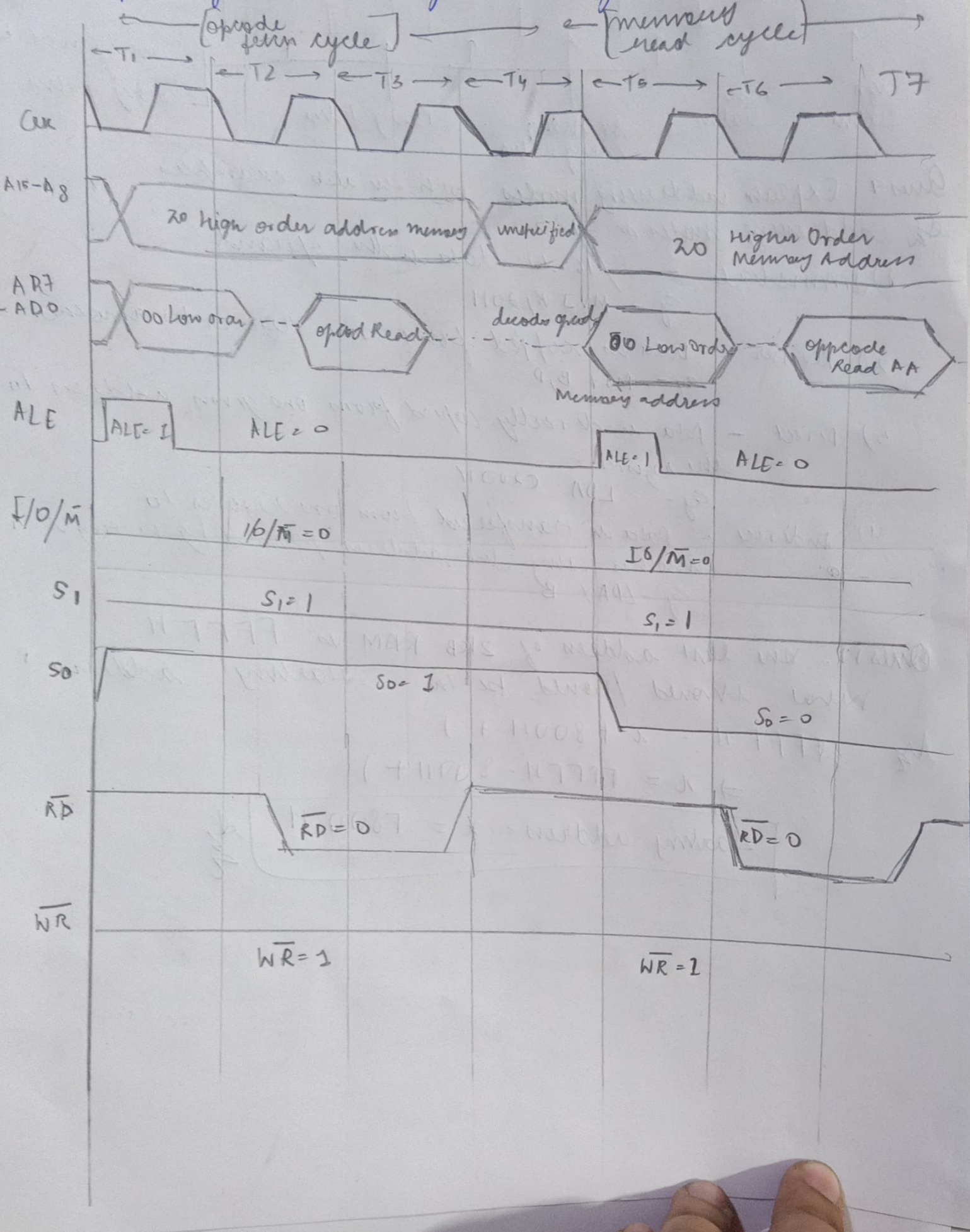
```
MVI A, 7FH
DAA A
CPI A2H
```

A = 7F
S = 1
Z = 0
Cy = 1

Ques 4. Draw the timing diagram for the instruction:

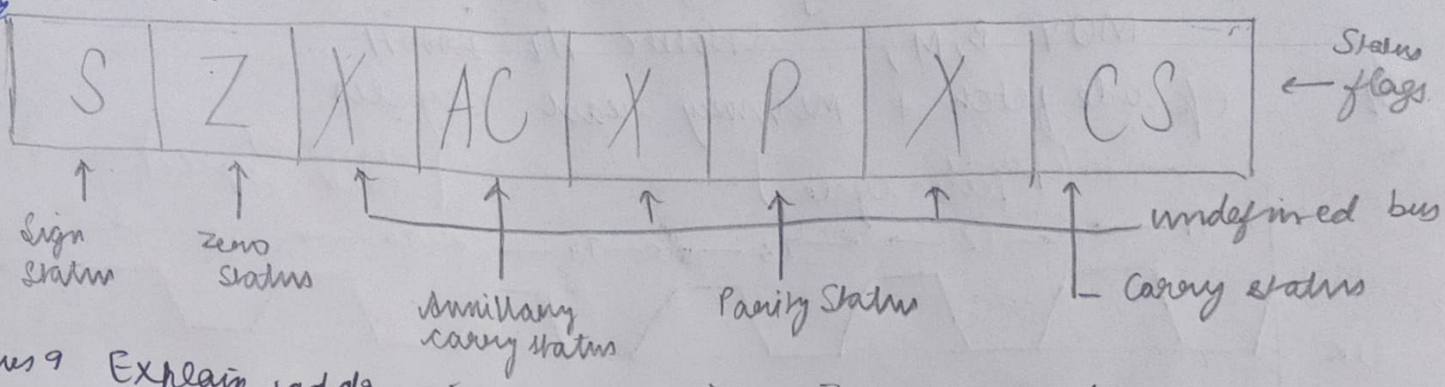
MOV B, M; Assume HL = 2000H

Opcode fetch + Memory read cycles



Ques 8. Draw format for PSW in 8085

Ans



Ques 9 Explain addressing modes with suitable examples.

Ans Addressing modes in 8085:

1) Immediate – 8/16 bit data is the operand
   eg – MVI B, 20H

2) Register – Data is copied from one register to another
   eg – MOV B, D

3) Direct – Data is directly copied from one given address to the register.
   eg – LDA C200H

4) Indirect or: Data is transferred from one register to another using the address pointed by the register
   eg – LDAX B

Ques 10. The last address of 2kB RAM is FFFFH what should/would be the starting address?

Ans FFFFH = x + 800H + 1

⇒ x = FFFFH − 800H + 1

Starting address = x = F800H

Ans