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group - 6C7

Assignment - 3

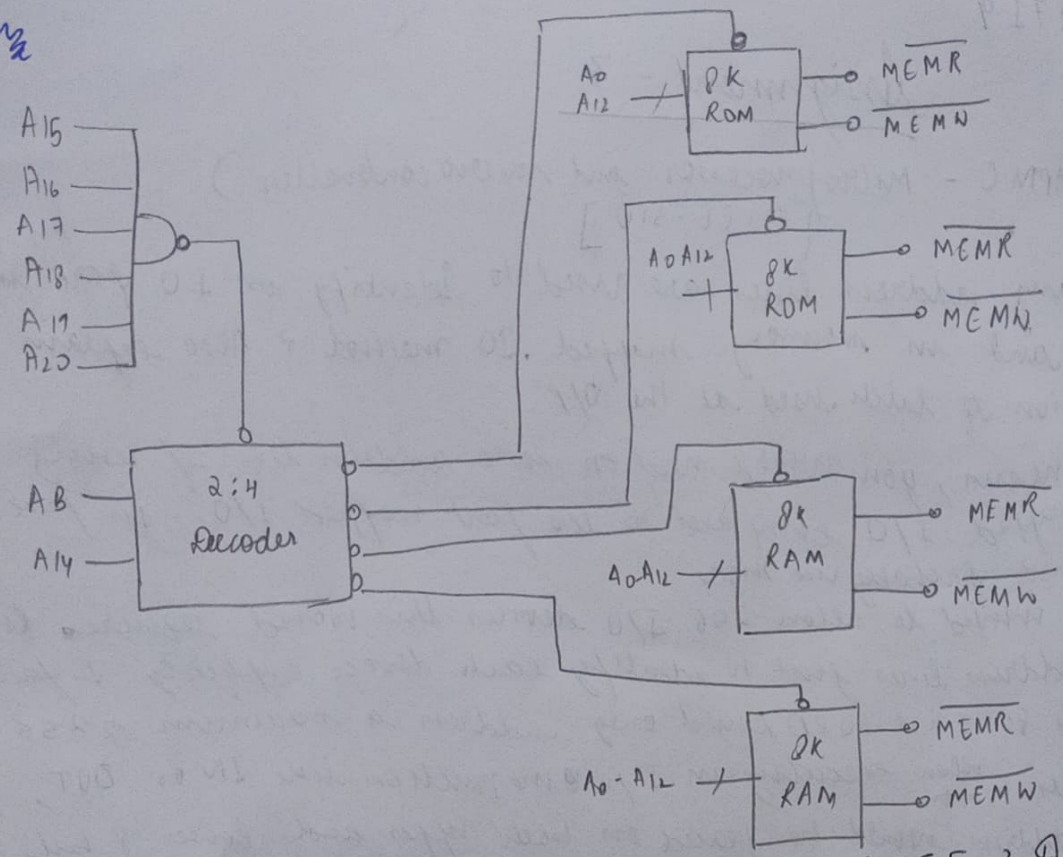
(MPMC - Microprocessor and microcontroller)
[ETEE-310]

Ans 1. How many address lines are used to identify an IO port in peripheral and in memory mapped IO method? Also explain the function of latch used at the O/P.

Ans As a minimum, you would need an extra address line if using memory-mapped I/O compared to the port mapped I/O. In practice you would probably use more.
Let's say you wanted to allow 256 I/O devices this would require decoding of 8 address lines just to identify each device explicitly. In fact processors like 8085 and 8080 could only address a maximum of 256 different ports - ~~when~~ when executing an I/O instruction like IN or OUT, the same address would be placed on both upper and lower 8 bits of 16-bit address bus (So IN 5 would actually place 0505 H on the bus).
On processors that use port-mapped I/O, there is a separate signal (such as IO/M on 8085) that asserted when an instruction is referencing an I/O port, rather than a memory location. (One might think of IO/M as 17th address line in that regard.)
In memory-mapped I/O, ports are accessed using load and store instruction, just like regular memory. So it is necessary to reserve a seperate area to place I/O ports, that won't conflict with memory. The easiest way to do this, which requires only 1 address line, is to split the address space itself in half, and use highest address line (Eg. - A15 in system with 64k of memory) to act as sort of IO/M line - When it is high (address 0x8000 to 0xFFFF) I/O is being addressed and the lowest 8-bits are used to decode the port's and when A15 is low memory is being addressed (0x0000 - 0x7FFF) But this wastes 32,512 addresses. At the opposite end of this spectrum, fully decoded all 16 address lines would waste no memory addresses. Most systems using some sort of compromise between the two. For example, fully decoding the upper 4 address lines would split memory space into 4k blocks wasting total 12 address lines in 64k memory space.
Note that any processor that uses port-mapped I/O can also have memory mapped I/O too.

Ans 2. Draw the diagram to interface 2 chips of 8k ROM and 2 chips

of 8k RAM consecutively with up 8086.



Ques 3. What are different operating modes in 8255 ? Discuss how to determine the control word for 8255.

Ans The 8255 is a general purpose programmable IO device. It is designed to interface the CPU with some external devices like ADC, DAC, Keyboard etc. We can program it.

There are 2 operational modes in 8255

→ Bit Set Reset Mode (BSR)

→ Input / Output mode

BSR Mode:

This mode is used to set or reset the bits of Port-C only. For BSR mode always D7 will be 0. The control register is looking like this.

Bits	D7	D6 D5 D4	D3 D2 D1	D0
Values	0	x	PC bit number	0 or 1

The (D_3, D_2, D_1) will be 000 to 111. In this mode it affects only one bit of Port C at a time. When user set the bit, it remains set until user insert it. The user needs to load the bit pattern in control register to change the bit.

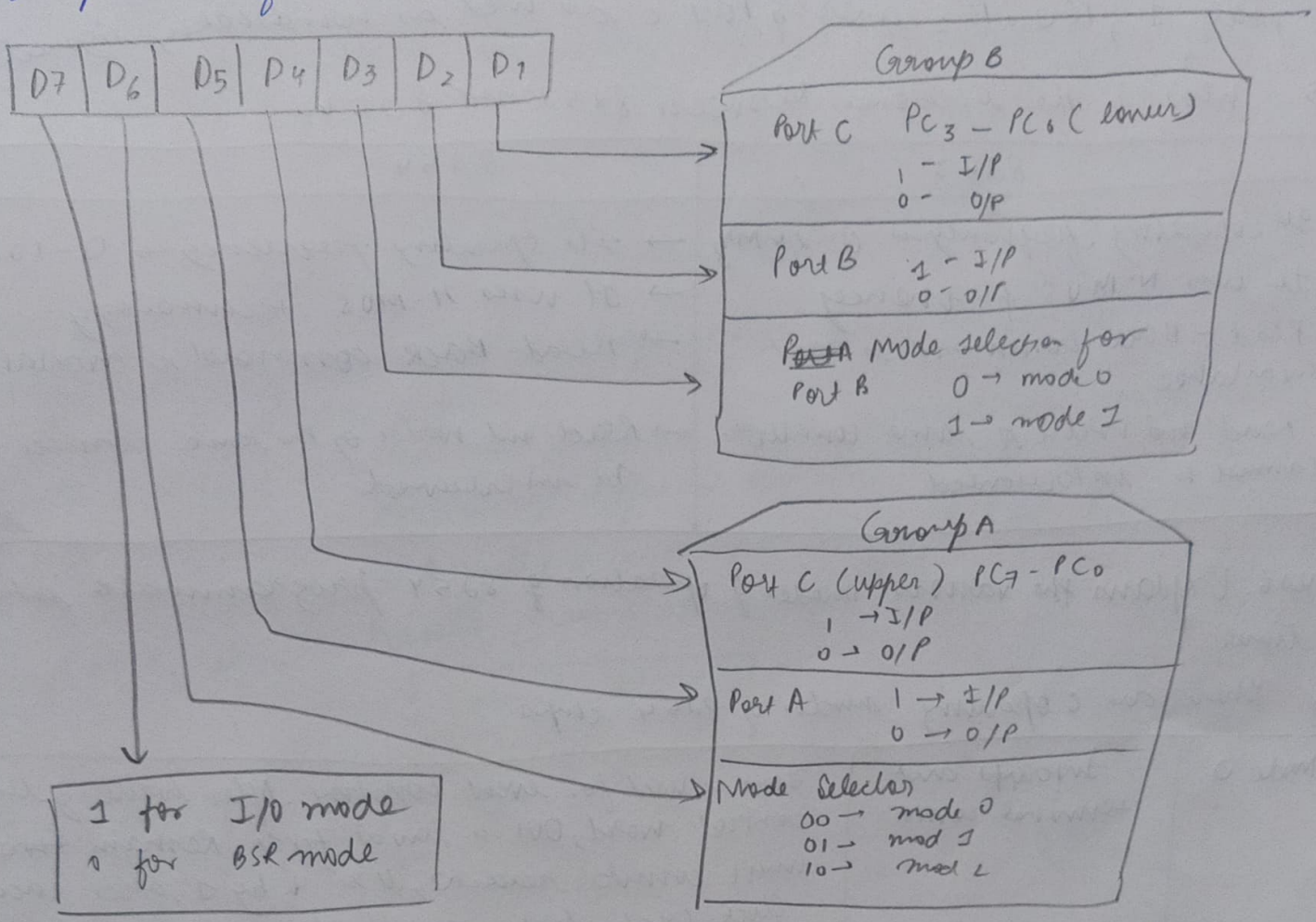
INPUT / OUTPUT MODE

This mode selected when the D7 bit of the control register is 1. The mode has also three different modes. These modes are Mode 0 and Mode 1 and Mode 3

Mode 0 - Simple or basic I/O Mode
Mode 1 - Handshake or Strobed I/O
Mode 3 - Bidirectional I/O

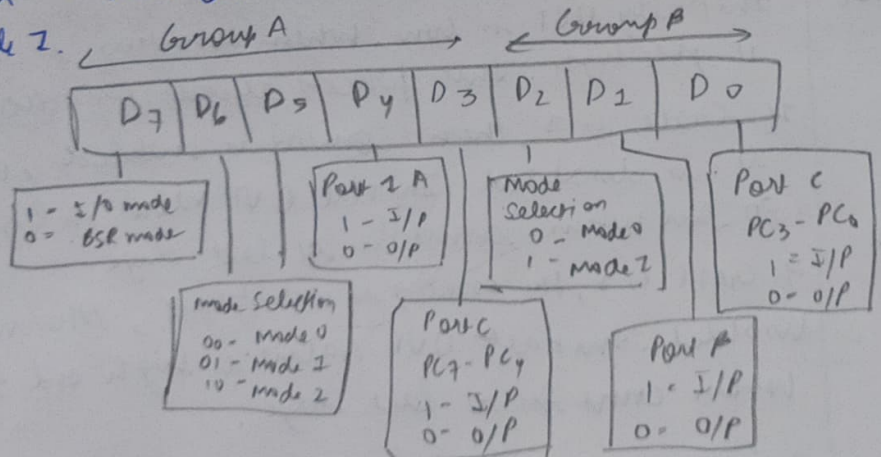
} OPERATIONAL Modes

The format of control word is as per the requirements of programmer. The control word is written into the control word register of 8255A. No read operation of control word is allowed.

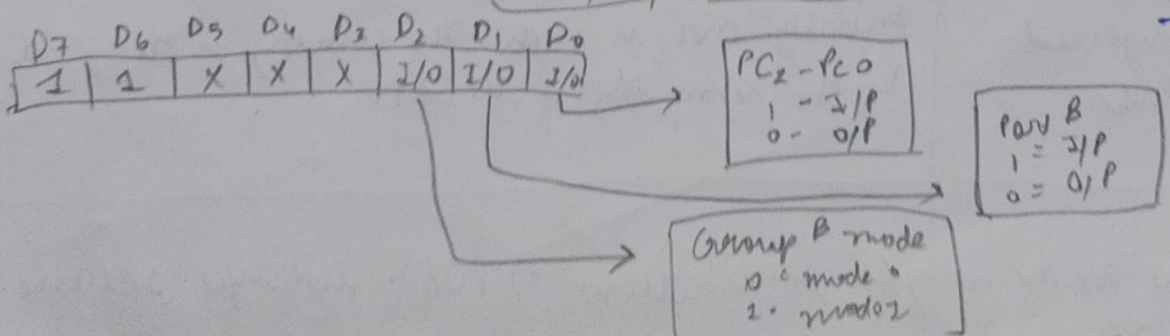


Ans 4. Write a short note on programming in 8255 in mode 2

In mode 2, port A can be used as a bidirectional I/O port into hand shaking capabilities whose signals are provided by port C. Port B can be used either in simple I/O mode or handshaking mode 1.



Mode 2 Control word



When the 8255 programming and operation is operated in mode 2. Port A can be used as a bi-directional 8-bit I/O bus using for handshaking. Port B can be programmed in mode 0 or in mode 1. When port B is programmed in mode 1, $PC_0 - PC_2$ lines of Port C are used as handshaking signal

Ques 5. What is the difference between 8253 and 8254?

Ans

8253	8254
→ Its operating frequency is 0-2.5 MHz	→ Its operating frequency is 0-10 MHz
→ It uses N-MOS frequency	→ It uses H-MOS technology
→ Read-Back command is not available.	→ Read-Back command is available
→ Read and write of same counter cannot be interleaved.	→ Read and write of the same counter can be interleaved

Ques 6. Explain the various modes of operation of 8254 programmable interval timer

Ans There are 6 operating modes of 8254 chips

Mode 0	Interrupt and terminal count	This is used for event counting. After writing the control word, OUT is low at first. Remain low until counter reaches 0, it is ↓ by 1 after each clock cycle. Gate = 1 indicates enable counting and 0 indicates disable counting.
Mode 1	Hardware Retriggerable one shot	OUT will be high at first, It will go low on clock pulse following trigger to begin one shot pulse Remain 0 until C. counter reaches 0
Mode 2	Rate Generator	Initially OUT is low. When counting is enabled it goes high. This process repeat periodically
Mode 3	Square wave generator	If Gate is 1, then counting is enabled, otherwise it is disabled. Initial OUT value is high and go low when count is at last stage.
Mode 4	Software triggered strobe	If GATE is 1, the counting is enabled, otherwise it is disabled. Initial OUT value is high and go low when count is at last stage.
Mode 5	Hardware triggered strobe	Initially OUT is high. The counting is triggred by the rising edge of the GATE

Ques 7, What are the major limitations of 8085 interrupt scheme? How

are the limitations overcomed by 8259? Explain with help of 8259 block diagram?

Ans → In 8085, processor can perform any arithmetic and logical operation only on 8 bit data at a time.

→ In 8085, only 16 bit address lines we can address only upto 64Kb of memory

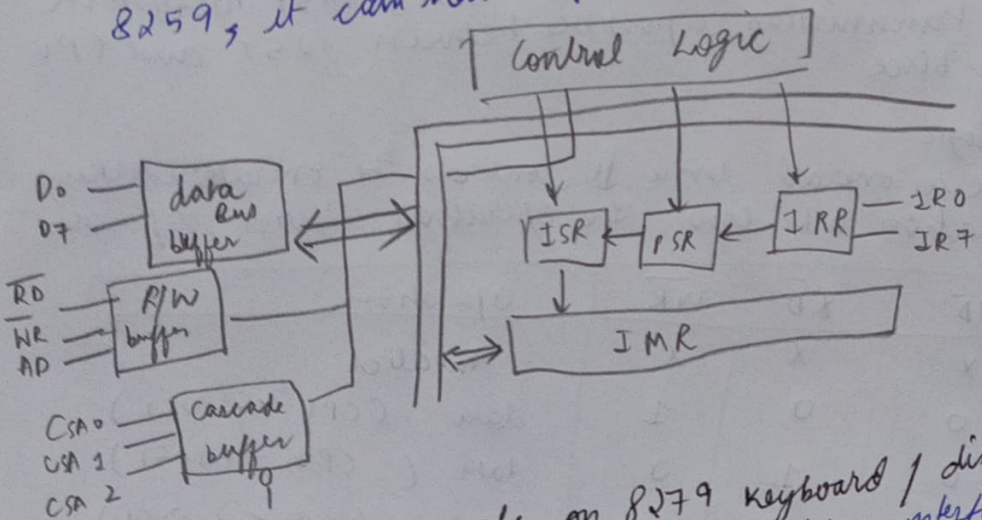
→ 8085 MP has multiplexed address and data bus, so extra hardware is required to seprate address and data signals.

Overcome by 8259

→ The 8259 progarammable interrupt control has 8 interrupt pins thus can handle 8 interrupt inputs.

→ The priority of interrupts in 8259 can be programmed. The priority of interrupts is decided by different operating modes.

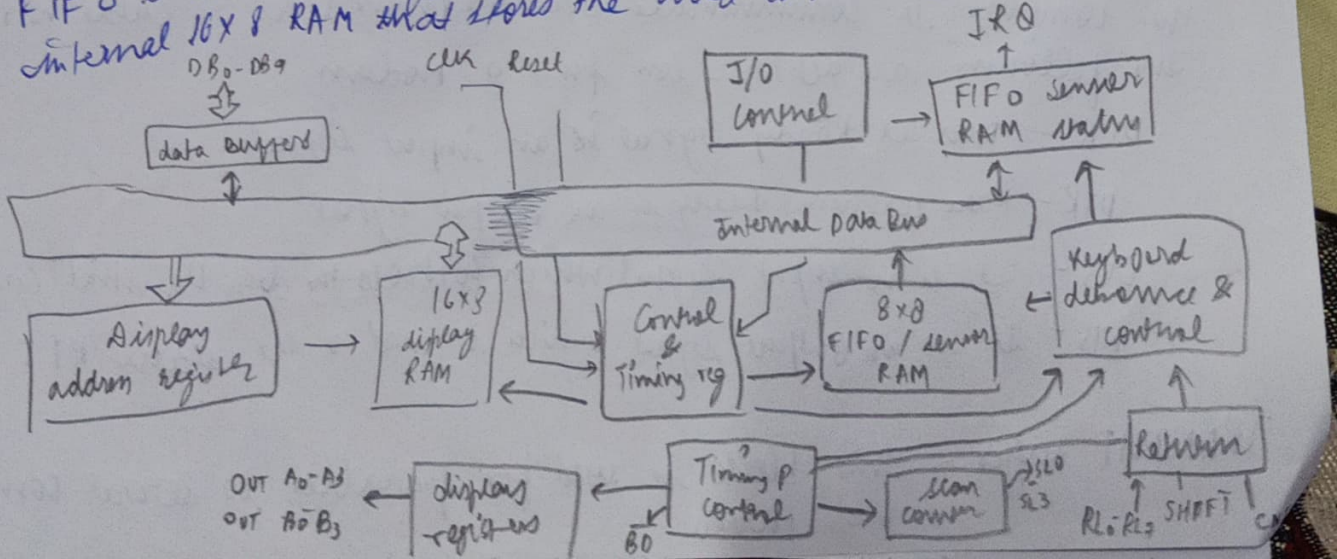
→ A single 8259 can handle 8 interrupt inputs but by Cascading multiple 8259's it can handle maximal 64 interrupt inputs.



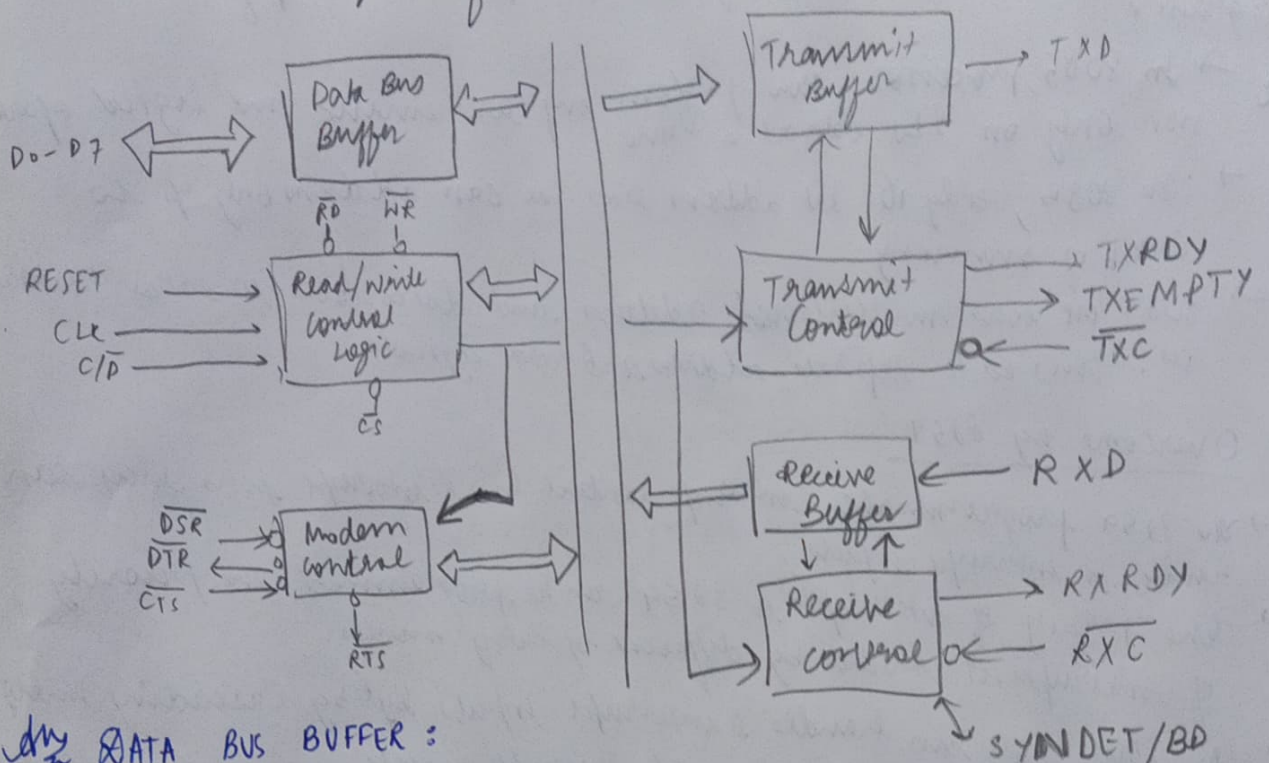
8259 Block Diagram

Ques 8, Write a short note on 8279 keyboard / display interface.

Ans A programmable keyboard and display interfacing chip. Scans and encodes upto a 64 key keyboard controls upto 16-bits digit numerical display keyboard section has a built in FIFO 8 character buffer. The display is controlled from an internal 16X8 RAM that stores the coded display information.



Ques 9. Draw block diagram of 8251 and describe its components



DATA BUS BUFFER :
This block helps in interfacing the internal data bus of 8251 to system data bus. The data transmission is possible between 8251 and CPU by data bus buffer block

READ/WRITE control logic :
It is a control block for overall device. It controls the overall working by selecting the operation to be done. The operation selection depends upon signal as :

CS	C/D	RD	WR	Operation
1	X	X	X	Invalid
0	0	0	1	data (CPU ← 8251)
0	0	1	0	data (CPU → 8251)
0	1	0	1	Status word (CPU ← 8251)
0	1	1	0	Control word (CPU → 8251)

MODEM CONTROL (MODULATOR / DEMODULATOR)
A device converts analog to digital signal and vice versa and helps the computer to communicate over telephone lines or cable wires.
The following are active - low pins of modem.
DSR - Data set Ready signal is an input signal
DTR - Data terminal Ready is an output signal
CTS - It is an input signal which controls the data transmit circuit
RTS - It is an output signal which is used to set status RTS.

TRANSMIT buffer - This block is used for parallel to serial converter and vice

transmission onto the common channel.

-TXD: It is an output signal, if its value is one, means transmitter will transmit the data.

TRANSMIT CONTROL:

The block is used to control the data transmission with the help of following pins:

TXRDY: It means transmitter is ready to transmit data character.

TXEMPTY: An output signal which indicate that TXEMPTY pin has transmitted all the data characters and transmitter is empty now.

RECEIVED BUFFER:

This block acts as a buffer for the received data.

RXD: An input signal which receives the data.

RECEIVE CONTROL:

The block controls the receiving data.

RXRDY: An input signal indicates that it is ready to receive the data.

RXC: An active-low input signal which controls the data transmission rate of received data.

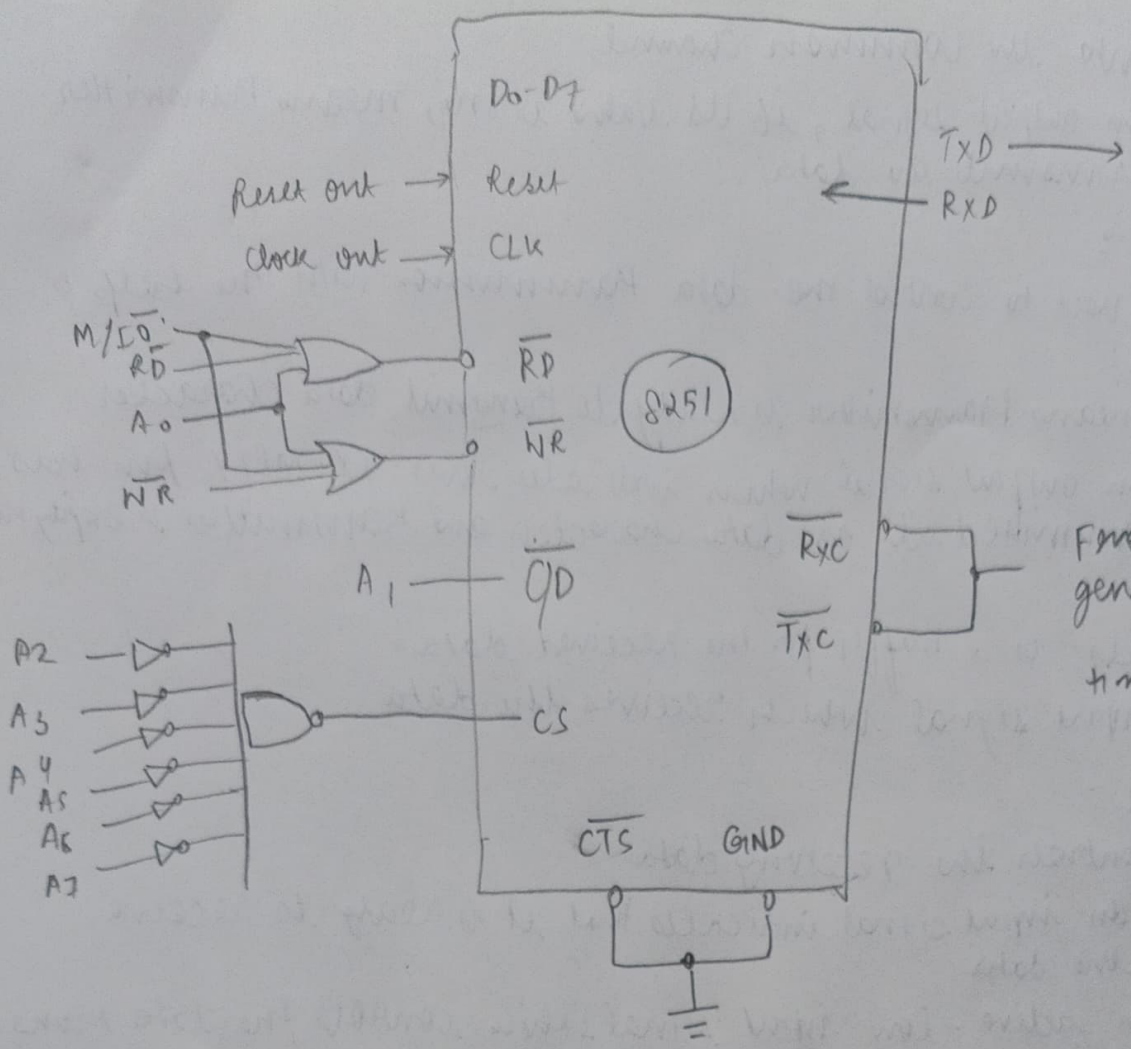
SYNDET/BD: An input or output terminal. External synchronous mode input terminal and asynchronous mode - output terminal.

Ques10. Draw the interface of 8251 with 8086 in IO mapped IO mode.

Ans Here, RD and WR signals are activated when M/IO signal is low, indicating I/O bus cycle. Only lower data bus (D_0-D_7) is used as 8251 is 8 bit device. Reset out signal from clock generator is connected to the reset signal of the 8251

I/O map:

Register	Address lines								Address
	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
Data Register	0	0	0	0	0	0	0	0	00H
control Register	0	0	0	0	0	0	1	0	02H



I/O mapped I/O interface of 8251 with 8086