EXPERIMENT - 11

Switching Theory and Logic Design (STLD)

Aim

To realize J-K flip flop using logic gates or by using kit.

Syeda Reeha Quasar
14114802719
3C7

EXPERIMENT - 11

AIM:

To realize J-K flip flop using logic gates or by using kit.

Hardware and Software Apparatus Required

Hardware:

Breadboard, IC 7400 (NAND), IC 7410 (3 input NAND), LEDs, resistor(1k), capacitor(.1uF), diode, 5V power supply, connecting wires or Omega LTB-826, patch cords.

Software Simulation:

The schematic models of the desired circuits will be stimulated on MULTISIM (Free Software), easily accessible at www.multisim.com.

Components used – Source (Clock Voltage), Passive elements (resistor), Digital components (AND, OR, NAND, NOR, XOR, XNOR, Inverter), Probe for Analysis and annotation (Digital), Schematic connectors (Ground)

Theory:

The **JK Flip Flop** is the most widely used flip flop. The sequential operation of the JK Flip Flop is same as for the RS flip-flop with the same **SET** and **RESET** input. The difference is that the JK Flip Flop does not the invalid input states of the RS Latch (when S and R are both 1).The JK Flip Flop name has been kept on the inventor name of the circuit known as **Jack Kilby.** S and R inputs of the RS bistable have been replaced by the two inputs called the J and K input respectively. Here J = S and K = R. The two input AND gates of the RS flip-flop is replaced by the two 3 inputs NAND gates as shown in figure 7.1(a) ,with the third input of each gate connected to the outputs at Q and $\bar{Q}$. This cross coupling of the RS Flip-Flop is used to produce toggle action. Clock will be provided by R-C circuit followed by diode as shown in figure 7.1(b).

Logic Diagram of J-K Flip Flop-

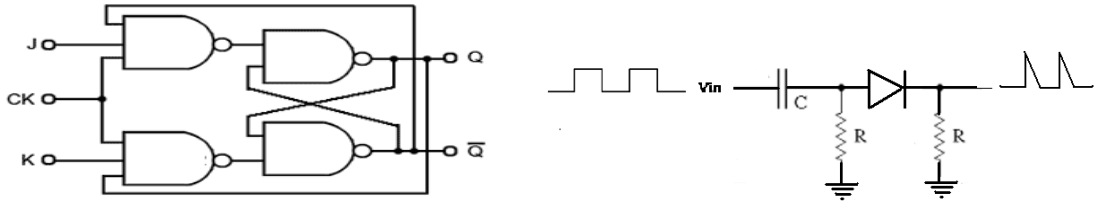


Fig 7.1 a) J-K Flip Flop b) clock provider circuit

Working of flip flop is depicted in truth table given below

Truth Table For J-K Flip Flop:

J	K	CLK	Q	$\overline{Q}$	*Comment*
0	0	↑	Q	$\overline{Q}$	Latch
1	0	↑	1	0	SET
0	1	↑	0	1	RESET
1	1	↑	$\overline{Q}$	Q	TOGGLE
X	X	0	Q	$\overline{Q}$	*NO Change !*

Pin Configuration of IC 7410

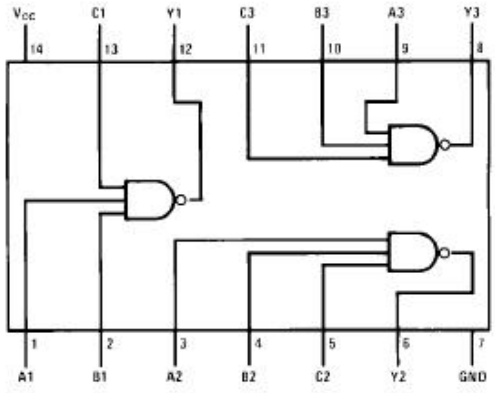


Fig 7.2 Pin configuration of IC used

Procedure:

1. Check all the components for their working.
2. Insert the appropriate IC into the IC base.
3. Make connections as shown in the circuit diagram.
4. Verify the results and observe the outputs.
5. While working on kit
6. Made connections as shown in circuit diagram on kit using patch cords.

Multisim:

1. Click on the 'Create Circuit' option on the top right corner of the profile in NI
2. Multisim webpage.
3. The schematic representation opens in a new tab.
4. Place three 'Ground' Schematic connector on the screen.
5. Place the logic gates from the digital section on the board, as per the required circuit diagram for circuits given.
6. Now, add clock voltages to the input of the logic gate and connect them with the help of Ground present in 'Schematic Connectors'.
7. Change the frequency of clock voltages e.g V1(say=5kHz) and V2(say=3kHz) etc.
8. Connect a resistor to the output of the logic gate and then, Ground it with the help of Ground Schematic Connector.
9. Connect the components with connecting wires.
10. Add digital probes to both input and output connections.
11. Set the display to 'Transient' from Interactive and press the 'Start
12. Simulation' button.
13. Note the graph

PRECAUTIONS:

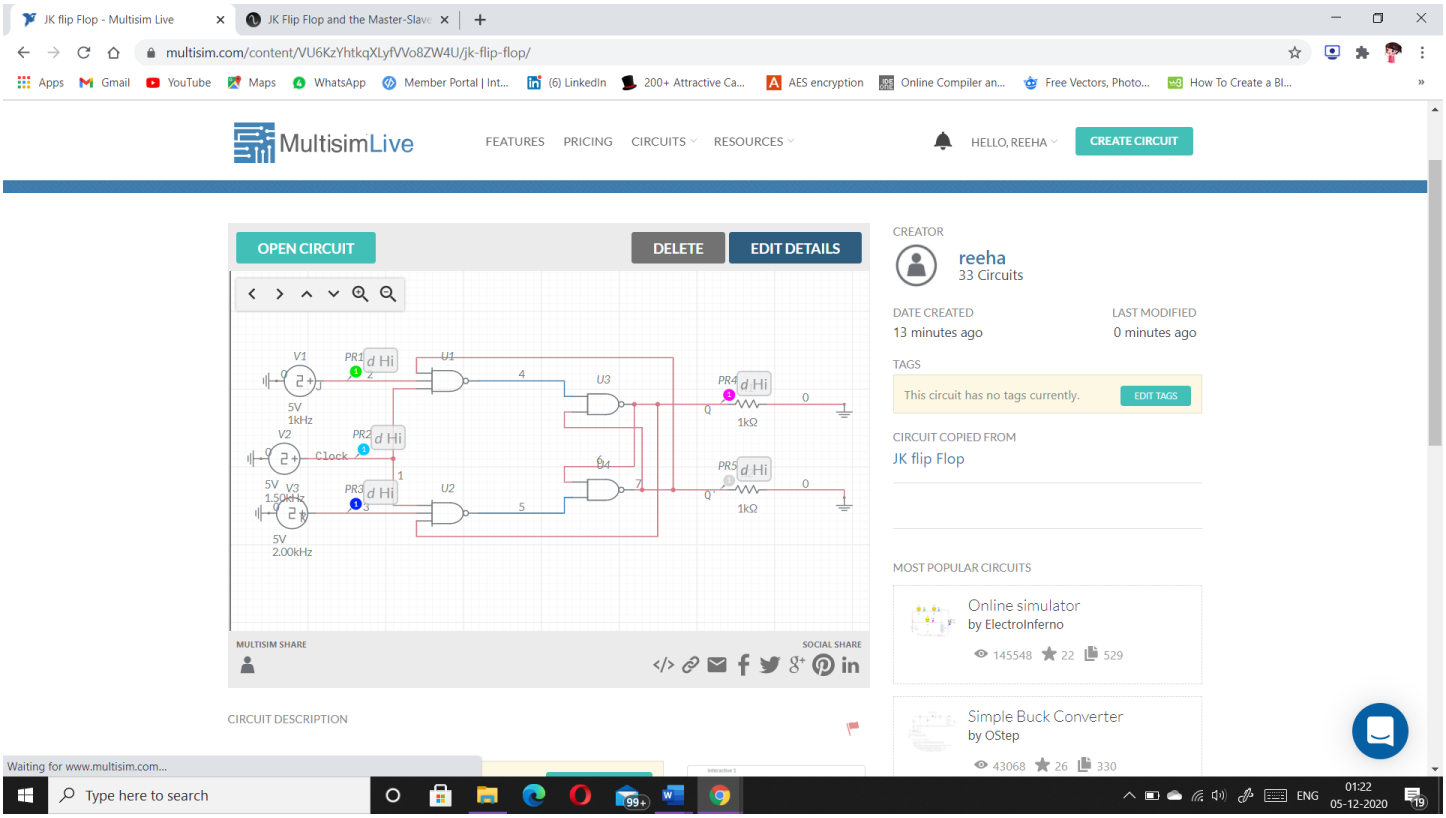
1. All ICs should be checked before starting the experiment.
2. All the connection should be tight.
3. Always connect ground first and then the supply.
4. Switch off the power supply after completion of the experiment.

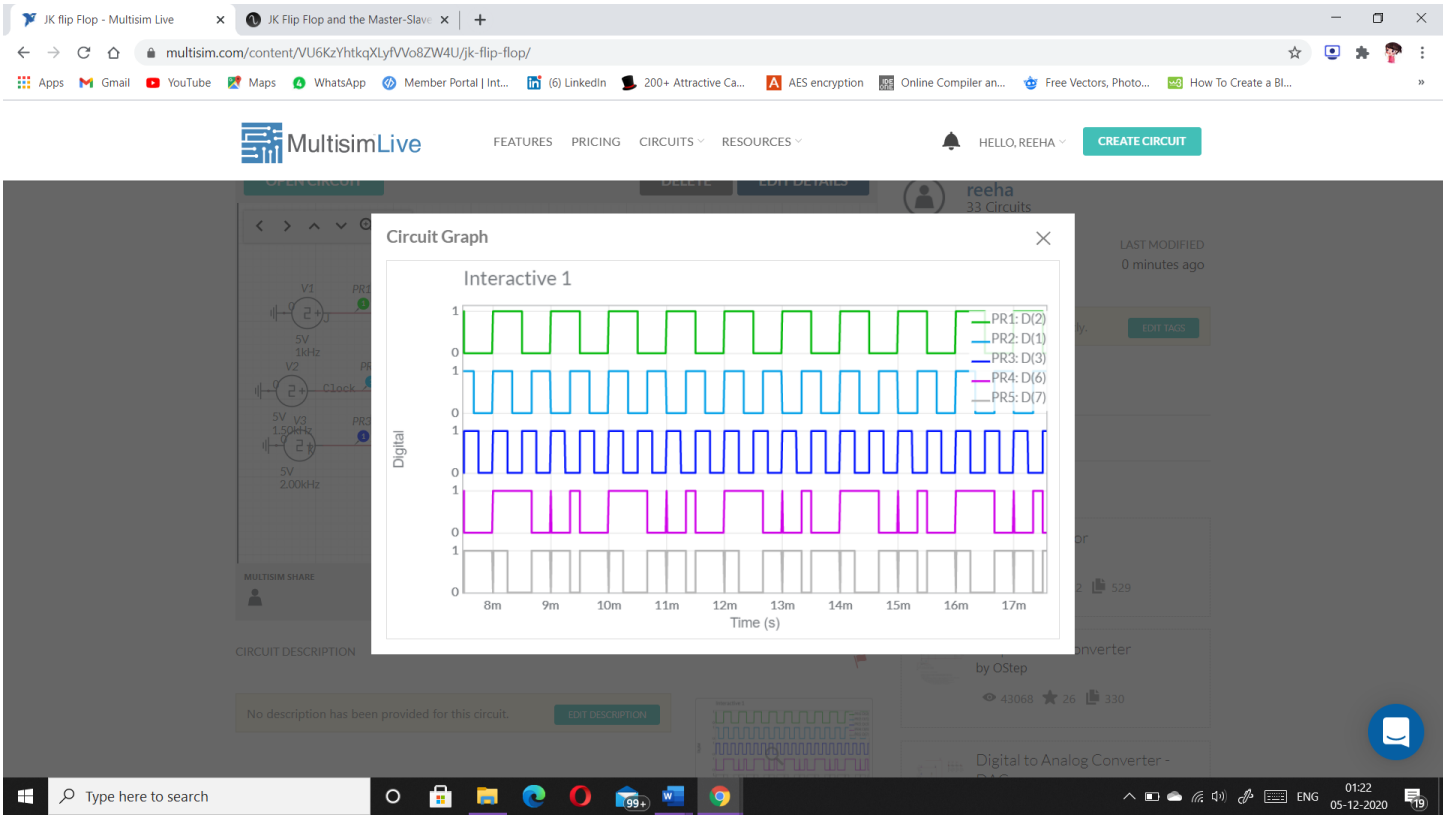
RESULT:

The J-K flip flop has been studied and its truth table has been verified.

Circuits and Output waveform

JK Flip Flop


JK flip Flop - Multisim Live
JK Flip Flop and the Master-Slave
multisim.com/content/VU6KzYhtkqXLyfVVo8ZW4U/jk-flip-flop/
MultisimLive
FEATURES
PRICING
CIRCUITS
RESOURCES
HELLO, REEHA
CREATE CIRCUIT
OPEN CIRCUIT
DELETE
EDIT DETAILS
CREATOR
reeha
33 Circuits
DATE CREATED
13 minutes ago
LAST MODIFIED
0 minutes ago
TAGS
This circuit has no tags currently.
EDIT TAGS
CIRCUIT COPIED FROM
JK flip Flop
MOST POPULAR CIRCUITS
Online simulator
by ElectroInferno
145548 22 529
Simple Buck Converter
by OStep
43068 26 330
MULTISIM SHARE
SOCIAL SHARE
CIRCUIT DESCRIPTION
Waiting for www.multisim.com...
Type here to search
ENG
01:22
05-12-2020


JK flip Flop - Multisim Live
JK Flip Flop and the Master-Slave
multisim.com/content/VU6KzYhtkqXLyfVVo8ZW4U/jk-flip-flop/
MultisimLive
FEATURES
PRICING
CIRCUITS
RESOURCES
HELLO, REEHA
CREATE CIRCUIT
Circuit Graph
Interactive 1
PR1: D(2)
PR2: D(1)
PR3: D(3)
PR4: D(6)
PR5: D(7)
Digital
Time (s)
8m
9m
10m
11m
12m
13m
14m
15m
16m
17m
reeha
33 Circuits
LAST MODIFIED
0 minutes ago
CIRCUIT DESCRIPTION
No description has been provided for this circuit.
EDIT DESCRIPTION
Digital to Analog Converter -
Type here to search
ENG
01:22
05-12-2020

VIVA-VOCE QUESTIONS:

Q1. Difference between sequential and combinational circuits.

Ans.

Combinational circuits are defined as the time independent circuits which do not depends upon previous inputs to generate any output are termed as combinational circuits. **Sequential circuits** are those which are dependent on clock cycles and depends on present as well as past inputs to generate any output.

Combinational Circuit –

1. In this output depends only upon present input.
2. Speed is fast.
3. It is designed easy.
4. There is no feedback between input and output.
5. This is time independent.
6. Elementary building blocks: Logic gates
7. Used for arithmetic as well as boolean operations.
8. Combinational circuits don't have capability to store any state.
9. As combinational circuits don't have clock, they don't require triggering.
10. These circuits do not have any memory element.
11. It is easy to use and handle.

Examples – Encoder, Decoder, Multiplexer, Demultiplexer

Block Diagram –

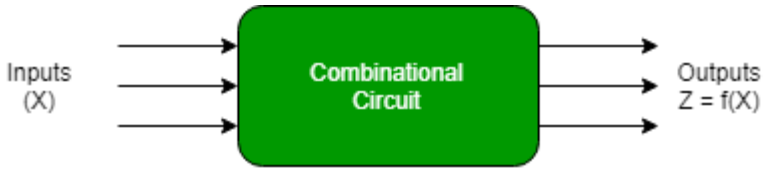


Figure: Combinational Circuits

Sequential Circuit –

1. In this output depends upon present as well as past input.
2. Speed is slow.
3. It is designed tough as compared to combinational circuits.

4. There exists a feedback path between input and output.
5. This is time dependent.
6. Elementary building blocks: Flip-flops
7. Mainly used for storing data.
8. Sequential circuits have capability to store any state or to retain earlier state.
9. As sequential circuits are clock dependent they need triggering.
10. These circuits have memory element.
11. It is not easy to use and handle.

Examples – Flip-flops, Counters

Block Diagram –

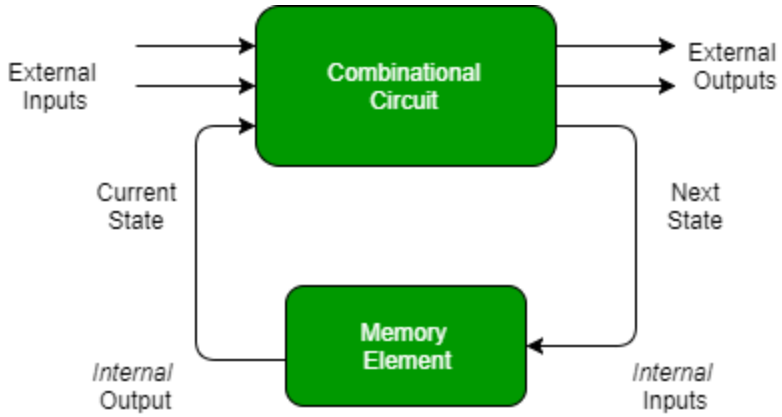


Figure: Sequential Circuit

Q2. List four Basic Flip-flop applications.

Ans.

Application of the flip flop circuit mainly involves in bounce elimination switch, data storage, data transfer, latch, registers, counters, frequency division, memory, etc.

Some of the most common applications of flip – flops are

- Counters
- Registers
- Frequency Divider circuits
- Data transfer

Q3. What advantage does a J-K Flip-flop have over an S-R?

Ans.

The J-K flip-flop is much faster. The J-K flip-flop does not have propagation delay problems. The J-K flip-flop has a toggle state.

The RS flip-flop has a “forbidden input state” with S and R both 1. In this state both Q and Not Q outputs will be 1 - which is bad enough - and the state of the flip-flop after R and S return to more sensible inputs depends on the order in which that happens.

The big difference of the JK flip-flop is, that the case J = K = 1 is allowed and toggles the output state. In everything else it works like a RS flip-flop.

So the JK flip-flop is a slightly enhanced version of the RS flip-flop. But better yet are gated flip-flops - they need slightly more gates but you have a lot better control over when the output changes.

Q4. What is meant by Race around condition and how we can overcome this problem?

Ans.

If the clock is High for a time interval less than the propagation delay of the flip flop then racing around condition can be eliminated. This is done by using the edge-triggered flip flop rather than using the level-triggered flip-flop.

When the input to the JK flip-flop is j=1 and k=1, the race around condition occurs, i.e it occurs when the time period of the clock pulse is greater than the propagation delay of the flip flop. so the output changes or toggles in a single clock period.