VIVA-VOCE QUESTIONS:

Q1. Write down expressions for 4-bit magnitude comparator.

Ans.

- If A3 = 1 and B3 = 0, then A is greater than B (A>B). Or
- If A3 and B3 are equal, and if A2 = 1 and B2 = 0, then A > B. Or
- If A3 and B3 are equal & A2 and B2 are equal, and if A1 = 1, and B1 = 0, then A>B. Or
- If A3 and B3 are equal, A2 and B2 are equal and A1 and B1 are equal, and if A0 = 1 and B0 = 0, then A > B.

From the above statements, the output A > B logic expression can be written as

$$G = A3\,\overline{B3} + (A3 \text{ Ex-NOR } B3)\,A2\,\overline{B2} + (A3 \text{ Ex-NOR } B3)\,(A2 \text{ Ex-NOR } B2)\,A1\,\overline{B1} + (A3 \text{ Ex-NOR } B3)\,(A2 \text{ Ex-NOR } B2)\,(A1 \text{ Ex-NOR } B1)\,A0\,\overline{B0}$$

Similarly the logic expression for the L or A<B output can be expressed as

$$L = \overline{A3}\,B3 + (A3 \text{ Ex-NOR } B3)\,\overline{A2}\,B2 + (A3 \text{ Ex-NOR } B3)\,(A2 \text{ Ex-NOR } B2)\,\overline{A1}\,B1 + (A3 \text{ Ex-NOR } B3)\,(A2 \text{ Ex-NOR } B2)\,(A1 \text{ Ex-NOR } B1)\,\overline{A0}\,B0$$

The equal output is produced when all the individual bits of one number are exactly coincides with corresponding bits of another number. Then the logical expression for A=B output can be written as

$$E = (A3 \text{ Ex-NOR } B3)\,(A2 \text{ Ex-NOR } B2)\,(A1 \text{ Ex-NOR } B1)\,(A0 \text{ Ex-NOR } B0)$$

Q2. What are applications of magnitude comparator?

Ans.

Digital comparator and magnitude comparator is used in different applications where data comparison is mostly required in many of the activities, and these hold many benefits too.

- Now, look into few of the applications of comparators
- Used for authorization purposes (such as password management) and biometric applications.
- These are implemented in process controllers and also in servo motor controls.
- Implemented for the data comparison of variables like temperature, the pressure is compared with that of reference values.
- Used to address decoding circuitry in computers.

Thus, this is all about digital comparator and magnitude comparator. So, the augmented performance of comparators allowed these devices to gain more prominence in the electronics industry and let them be implemented in many applications.

Q3. What are Magnitude comparators?

Ans.

A magnitude digital Comparator is a combinational circuit that compares two digital or binary numbers in order to find out whether one binary number is equal, less than or greater than the other binary number. We logically design a circuit for which we will have two inputs one for A and other for B and have three output terminals, one for A > B condition, one for A = B condition and one for A < B condition.

EXPERIMENT - 9

Switching Theory and Logic Design (STLD)

Aim

To realize 4-Bit Binary to BCD Convertor.

Syeda Reeha Quasar
14114802719
3C7

EXPERIMENT - 9

AIM:

To realize 4-Bit Binary to BCD Convertor.

Hardware and Software Apparatus Required

Hardware:

Breadboard, IC 7400 (NAND), IC 7410 (3 input NAND), IC 7404(NOT), LEDs, 5V power supply, connecting wires.

Software Simulation:

The schematic models of the desired circuits will be stimulated on MULTISIM (Free Software), easily accessible at www.multisim.com.

Components used – Source (Clock Voltage), Passive elements (resistor), Digital components (AND, OR, NAND, NOR, XOR, XNOR, Inverter), Probe for Analysis and annotation (Digital), Schematic connectors (Ground)

Theory:

BCD is binary coded decimal number, where each digit of a decimal number is respected by its equivalent binary number. That means, LSB of a decimal number is represented by its equivalent binary number and similarly other higher significant bits of decimal number are also represented by their equivalent binary numbers.

For example, BCD Code of 14 is-

Let us design a 4 bit **binary to BCD code converter**. As the 4 bit can

represent 0 to 15, we can draw the conversion table as follows,

Binary Code A B C D	Decimal Number	BCD Code B_5 B_4 B_3 B_2 B_1
0 0 0 0	0	0 0 0 0 0
0 0 0 1	1	0 0 0 0 1
0 0 1 0	2	0 0 0 1 0
0 0 1 1	3	0 0 0 1 1
0 1 0 0	4	0 0 1 0 0
0 1 0 1	5	0 0 1 0 1
0 1 1 0	6	0 0 1 1 0
0 1 1 1	7	0 0 1 1 1
1 0 0 0	8	0 1 0 0 0
1 0 0 1	9	0 1 0 0 1
1 0 1 0	10	1 0 0 0 0
1 0 1 1	11	1 0 0 0 1
1 1 0 0	12	1 0 0 1 0
1 1 0 1	13	1 0 0 1 1
1 1 1 0	14	1 0 1 0 0
1 1 1 1	15	1 0 1 0 1

Here, B_5 bit represents MSB of decimal number and B_4, B_3, B_2, B_1 represents 4 bit binary equivalent of LSB of decimal number.
From, above conversion table, we can write SOP form for different bits of BCD code.

$$B_5 = \sum m(10,11,12,13,14,15),\ B_4 = \sum m(8,9),\ B_3 = \sum m(4,5,6,7,14,15),$$
$$B_2 = \sum m(2,3,6,7,12,13),\ B_1 = \sum m(1,3,5,7,9,11,13,15)$$

TRUTH TABLE :

AND

INPUT		OUTPUT
A	B	
0	0	0
1	0	0
0	1	0
1	1	1

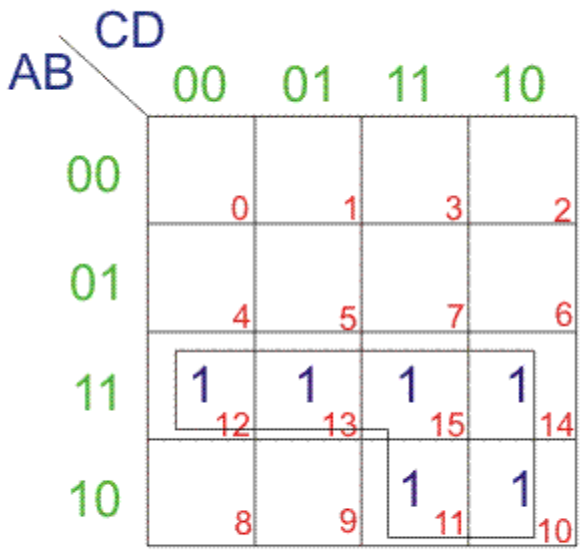
NOT

INPUT	OUTPUT
A	
0	1
1	0

OR

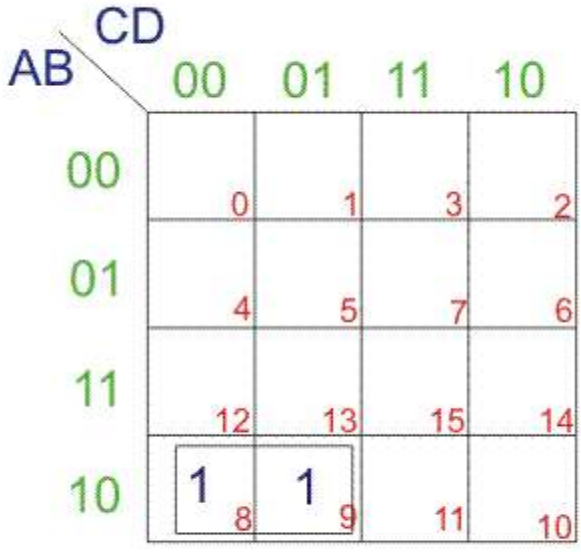
INPUT		OUTPUT
A	B	
0	0	0
1	0	1
0	1	1
1	1	1

K - map for B_5



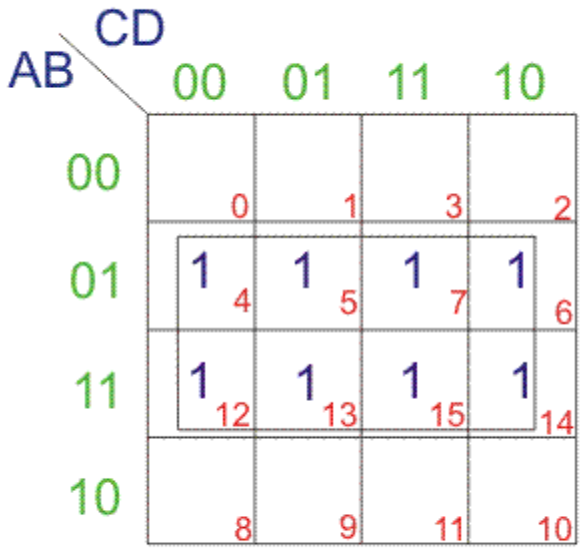
$B_5 = AB + BC$

K - map for B_4



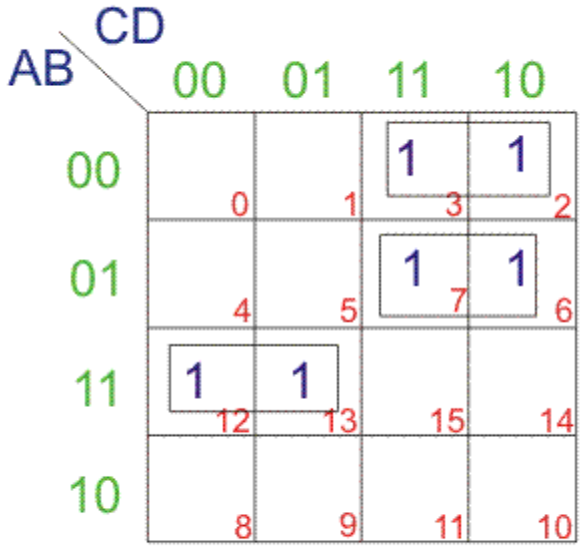
$B_4 = A\overline{B}\,\overline{C}$

K - map for B_3



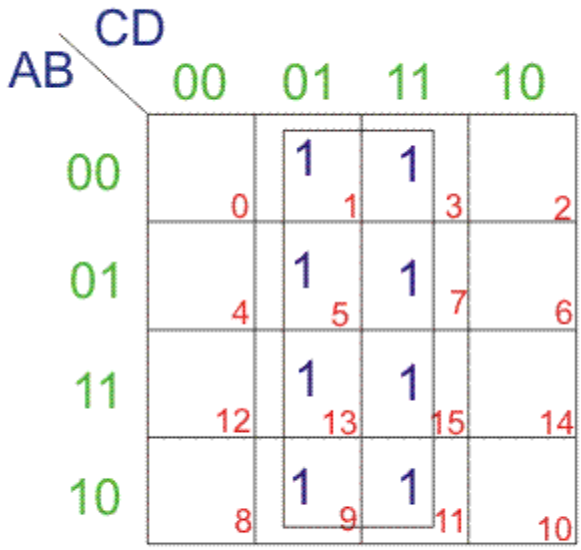
$B_3 = \overline{A}B + CB$

K - map for B_2



$B_2 = AB\overline{C} + \overline{A}C$

K - map for B_1



$B_1 = D$

Procedure:

1. Check all the components for their working.
2. Insert the appropriate IC into the IC base.
3. Make connections as shown in the circuit diagram.
4. Verify the results and observe the outputs.

Multisim:

1. Click on the 'Create Circuit' option on the top right corner of the profile in NI
2. Multisim webpage.

3. The schematic representation opens in a new tab.
4. Place three 'Ground' Schematic connector on the screen.
5. Place the logic gates from the digital section on the board, as per the
6. required circuit diagram for 4-bit Binary to BCD Converter
1. Now, add clock voltages to the input of the logic gate and connect them
7. with the help of Ground present in 'Schematic Connectors'.
2. Change the frequency of clock voltages e.g V1(say=5kHz) and V2(say=3kHz)
8. etc.
3. Connect a resistor to the output of the logic gate and then, Ground it with
9. the help of Ground Schematic Connector.
4. Connect the components with connecting wires.
5. Add digital probes to both input and output connections.
6. Set the display to 'Transient' from Interactive and press the 'Start
10. Simulation' button.
11. Note the graph

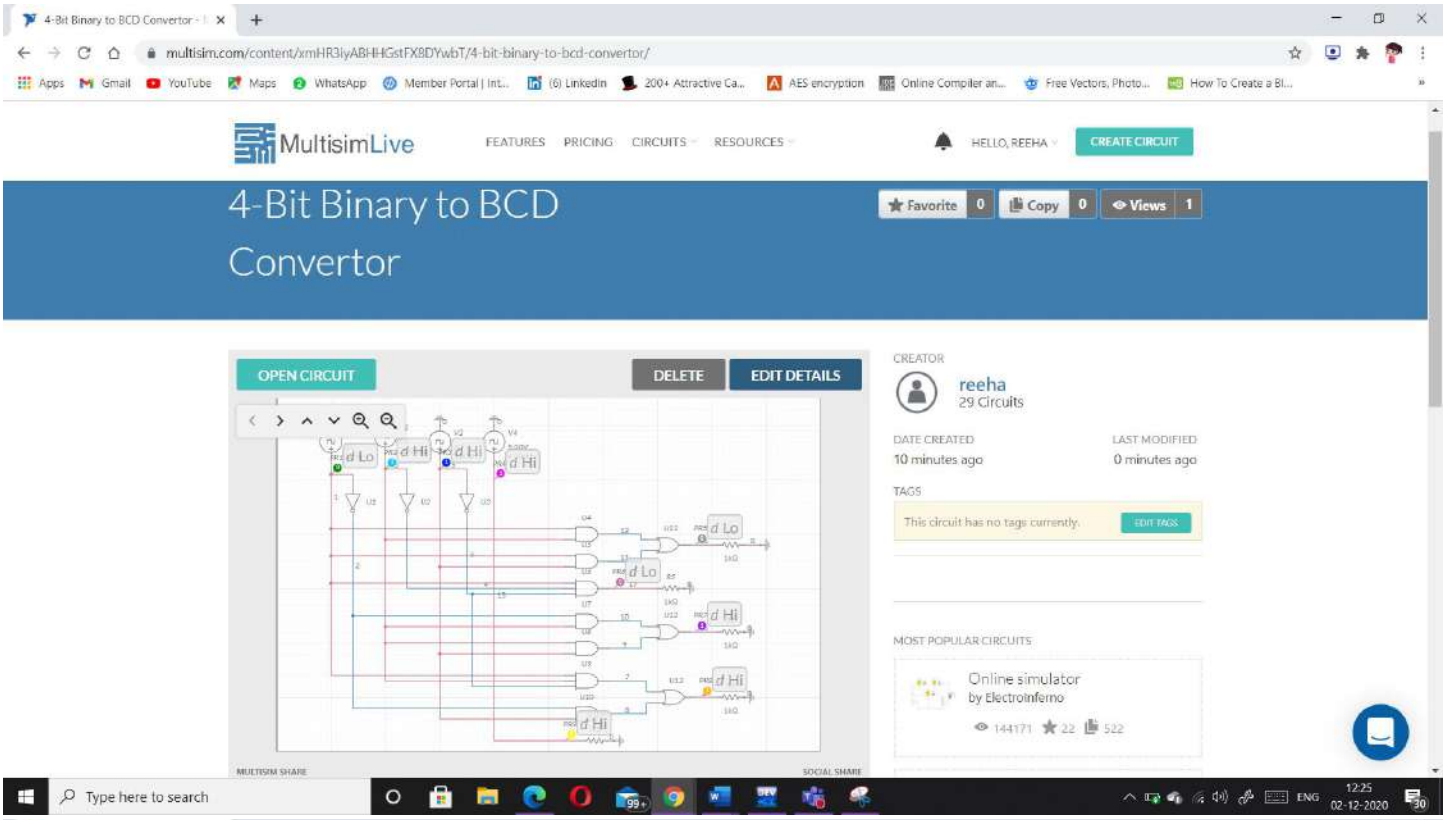
PRECAUTIONS:

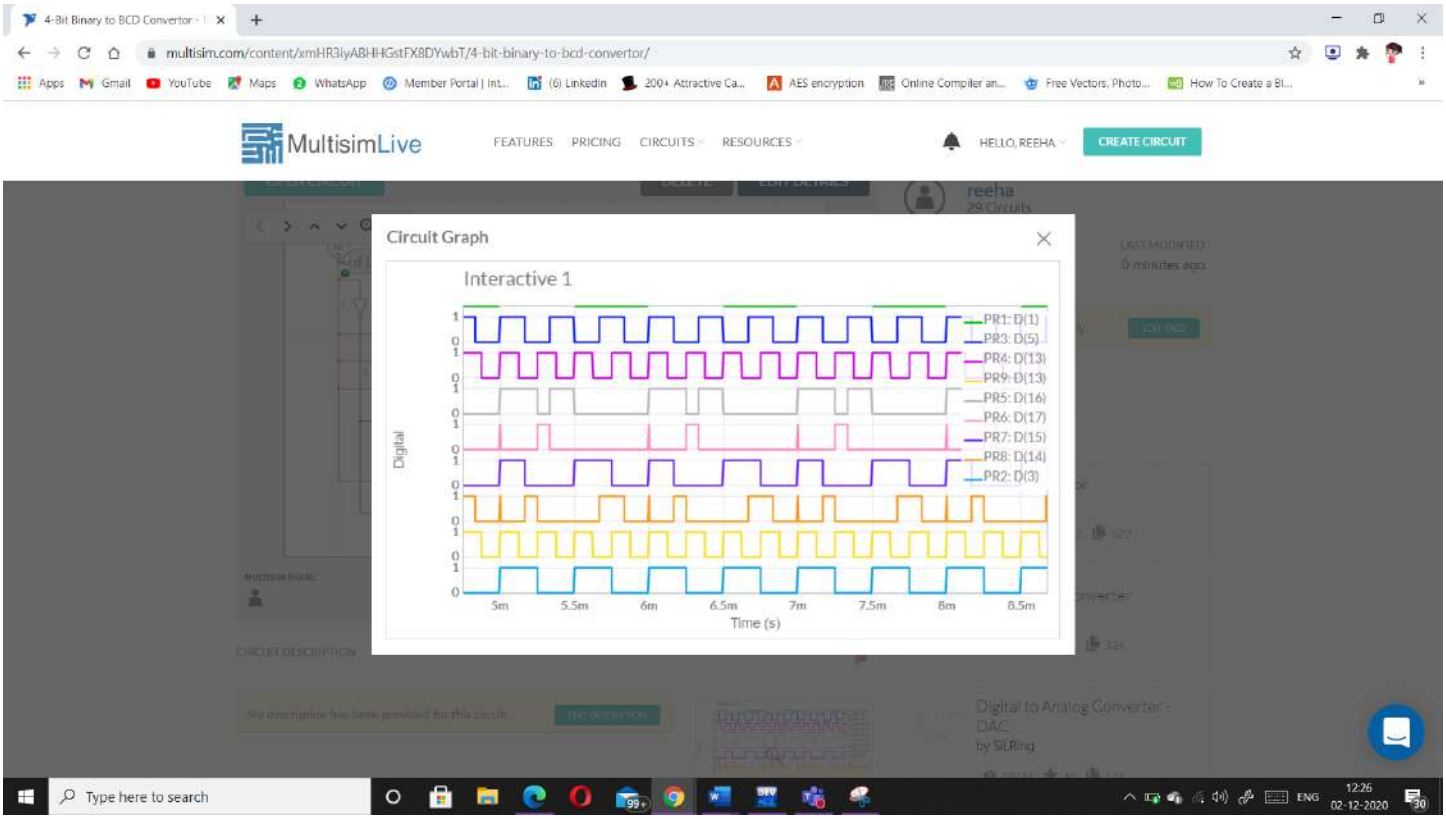
1. All ICs should be checked before starting the experiment.
2. All the connection should be tight.
3. Always connect ground first and then the supply.
4. Switch off the power supply after completion of the experiment.

RESULT:

4-Bit Binary to BCD Convertor has been studied and its truth table is verified.

Circuits and Output waveform





VIVA-VOCE QUESTIONS:

Q1. (10110)2 = (?)BCD

Ans.

(10110)2 = (_____)BCD

Q2. Convert decimal to BCD $(22)_{10}$ = (_____)$_{BCD}$

2	2
0010	0010

$\therefore (22)_{10} = (\underline{00100010})_{BCD}$

$\therefore$ **$(10110)_2 = (\underline{00100010})_{BCD}$**

Q3. Write the algorithm to convert binary to BCD.

Ans.

Algorithm:

1. If any column (100's, 10's, 1's, etc.) is 5 or greater, add 3 to that column.
2. Shift all #'s to the left 1 position.
3. If 8 shifts have been performed, it's done! Evaluate each column for the BCD values.
4. Go to step 1.

100's	10's	1's	Binary	Operation
			1010 0010	162
		1	010 0010	<< #1
		10	10 0010	<< #2
		101	0 0010	<< #3
		1000		add 3
	1	0000	0010	<< #4
	10	0000	010	<< #5
	100	0000	10	<< #6
	1000	0001	0	<< #7
	1011			add 3
1	0110	0010		<< #8
1	6	2		

Q4. Why do we convert Binary to BCD?

Ans.

Conversion of a binary number into separate binary numbers representing digits of the decimal number.
(this example is for 8-bits, other sizes follow the same pattern)

```
for(i=0; i<8; i++) {
	//check all columns for >= 5
	for each column {
		if (column >= 5)
			column += 3;

	//shift all binary digits left 1
	Hundreds <<= 1;
	Hundreds[0] = Tens[3];
	Tens << = 1;
	Tens[0] = Ones[3];
	Ones << = 1;
	Ones[0] = Binary[7];
	Binary <<= 1;
}
```

EXPERIMENT - 10

Switching Theory and Logic Design (STLD)

Aim

To realize Multiplexer and Demultiplexer using only NAND gates.

Syeda Reeha Quasar
14114802719
3C7

EXPERIMENT - 10

AIM:

To realize Multiplexer and Demultiplexer using only NAND gates.

Hardware and Software Apparatus Required

Hardware:

Breadboard, IC 7400 (NAND), LEDs, 5V power supply, connecting wires.

Software Simulation:

The schematic models of the desired circuits will be stimulated on MULTISIM (Free Software), easily accessible at www.multisim.com.

Components used – Source (Clock Voltage), Passive elements (resistor), Digital components (AND, OR, NAND, NOR, XOR, XNOR, Inverter), Probe for Analysis and annotation (Digital), Schematic connectors (Ground)

Theory:

Multiplexers are very useful components in digital systems. They transfer a large number of information units over a smaller number of channels, (usually one channel) under the control of selection signals. Multiplexer means many to one. A multiplexer is a circuit with many inputs but only one output. By using control signals (select lines) we can select any input to the output. Multiplexer is also called as data selector because the output bit depends on the input data bit that is selected. The general multiplexer circuit has 2n input signals, n control/select signals and 1 output signal.

De-multiplexers perform the opposite function of multiplexers. They transfer a small number of information units (usually one unit) over a larger number of channels under the control of selection signals. The general de-multiplexer circuit has 1 input signal, n control/select signals and 2n output signals. De-multiplexer circuit can also be realized using a decoder circuit with enable.

REALIZATION OF 2:1 MUX

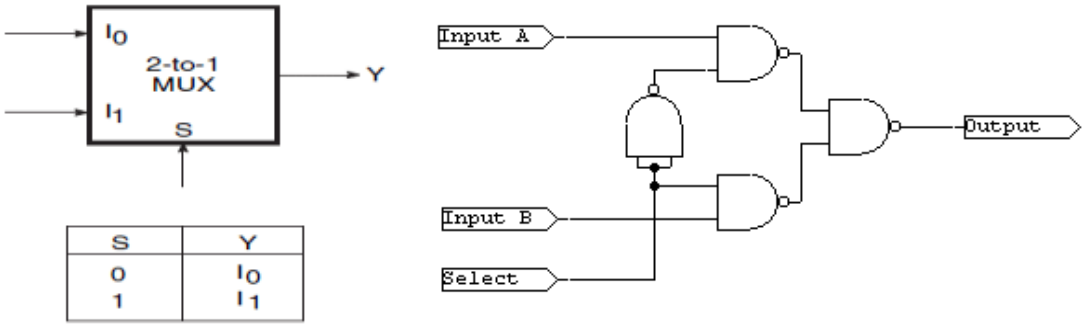


Fig 6.1 Truth Table and circuit implementation of 2:1 mux

REALIZATION OF 1:2 DEMUX

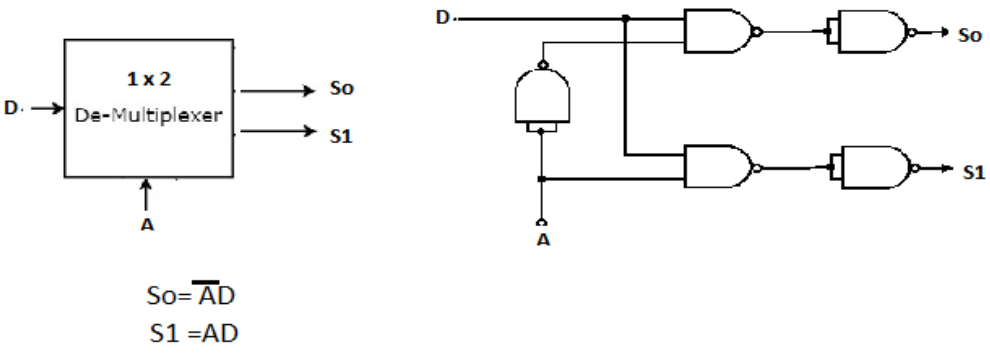


Fig 6.2 Logic Diagram and Circuit of 1:2 DMUX

Procedure:

1. Check all the components for their working.
2. Insert the appropriate IC into the IC base.
3. Make connections as shown in the circuit diagram.
4. Verify the results and observe the outputs.

Multisim:

1. Click on the 'Create Circuit' option on the top right corner of the profile in NI
2. Multisim webpage.
3. The schematic representation opens in a new tab.
4. Place three 'Ground' Schematic connector on the screen.
5. Place the logic gates from the digital section on the board, as per the required circuit diagram for MUX and DEMUX circuits.
6. Now, add clock voltages to the input of the logic gate and connect them with the help of Ground present in 'Schematic Connectors'.

7. Change the frequency of clock voltages e.g V1(say=5kHz) and V2(say=3kHz) etc.
8. Connect a resistor to the output of the logic gate and then, Ground it with the help of Ground Schematic Connector.
9. Connect the components with connecting wires.
10. Add digital probes to both input and output connections.
11. Set the display to 'Transient' from Interactive and press the 'Start
12. Simulation' button.
13. Note the graph

PRECAUTIONS:

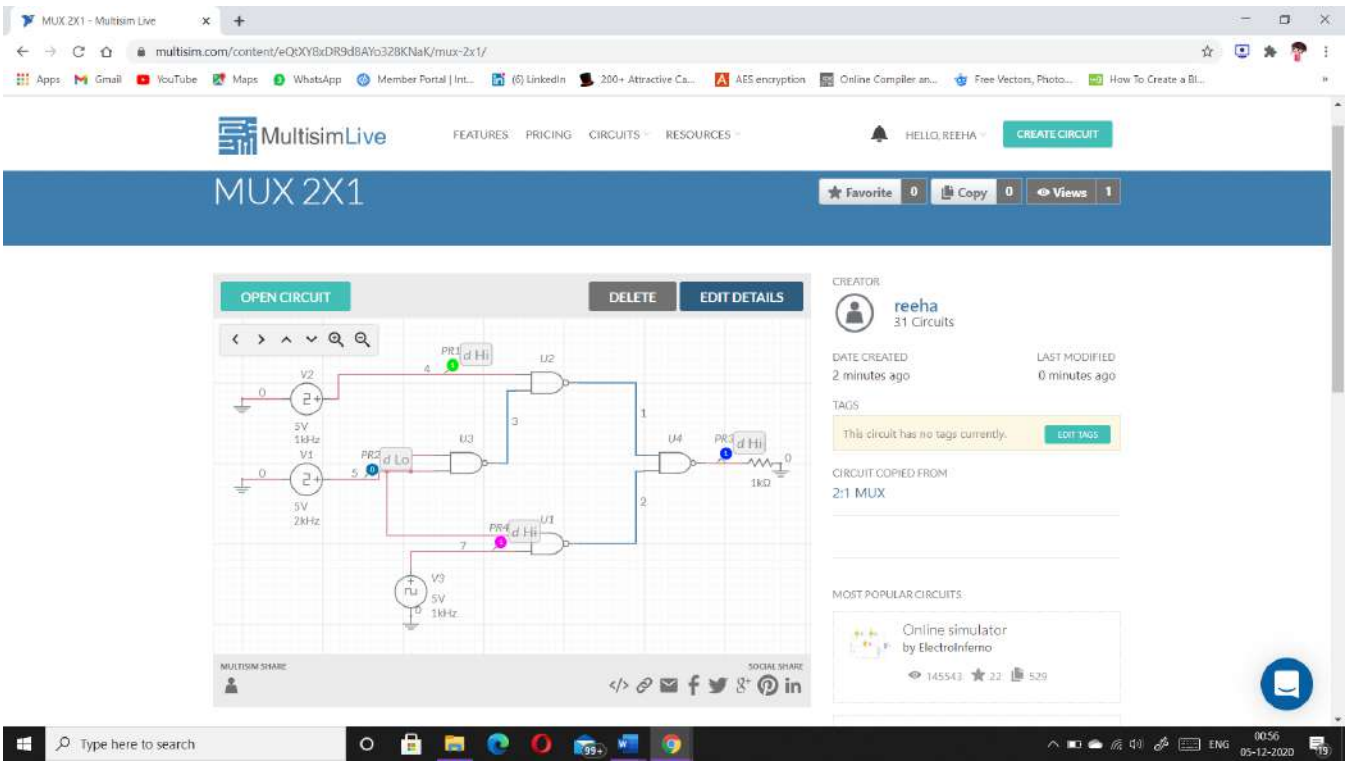
1. All ICs should be checked before starting the experiment.
2. All the connection should be tight.
3. Always connect ground first and then the supply.
4. Switch off the power supply after completion of the experiment.

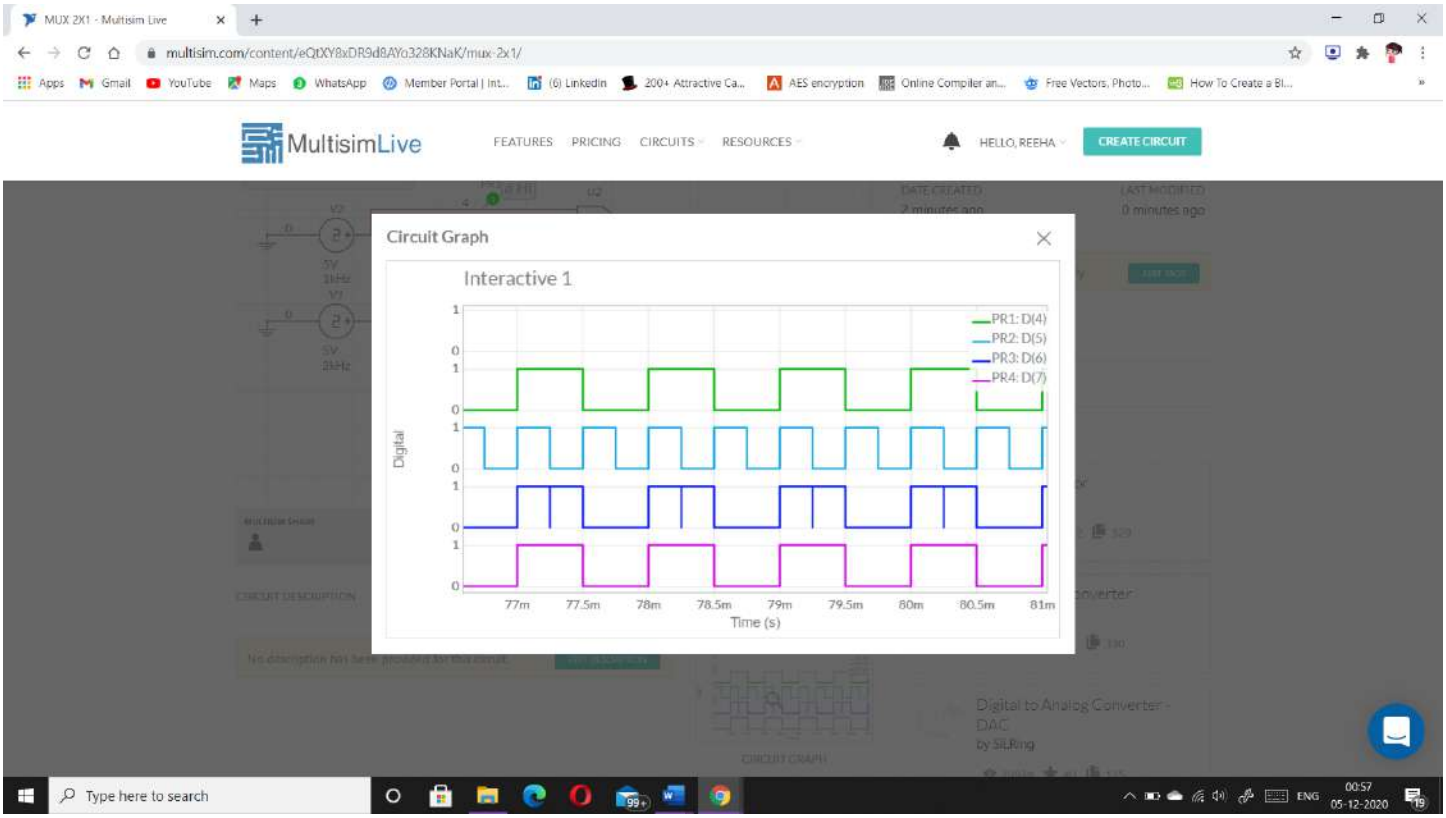
RESULT:

Multiplexer and Demultiplexer have been studied and their truth table has been verified.

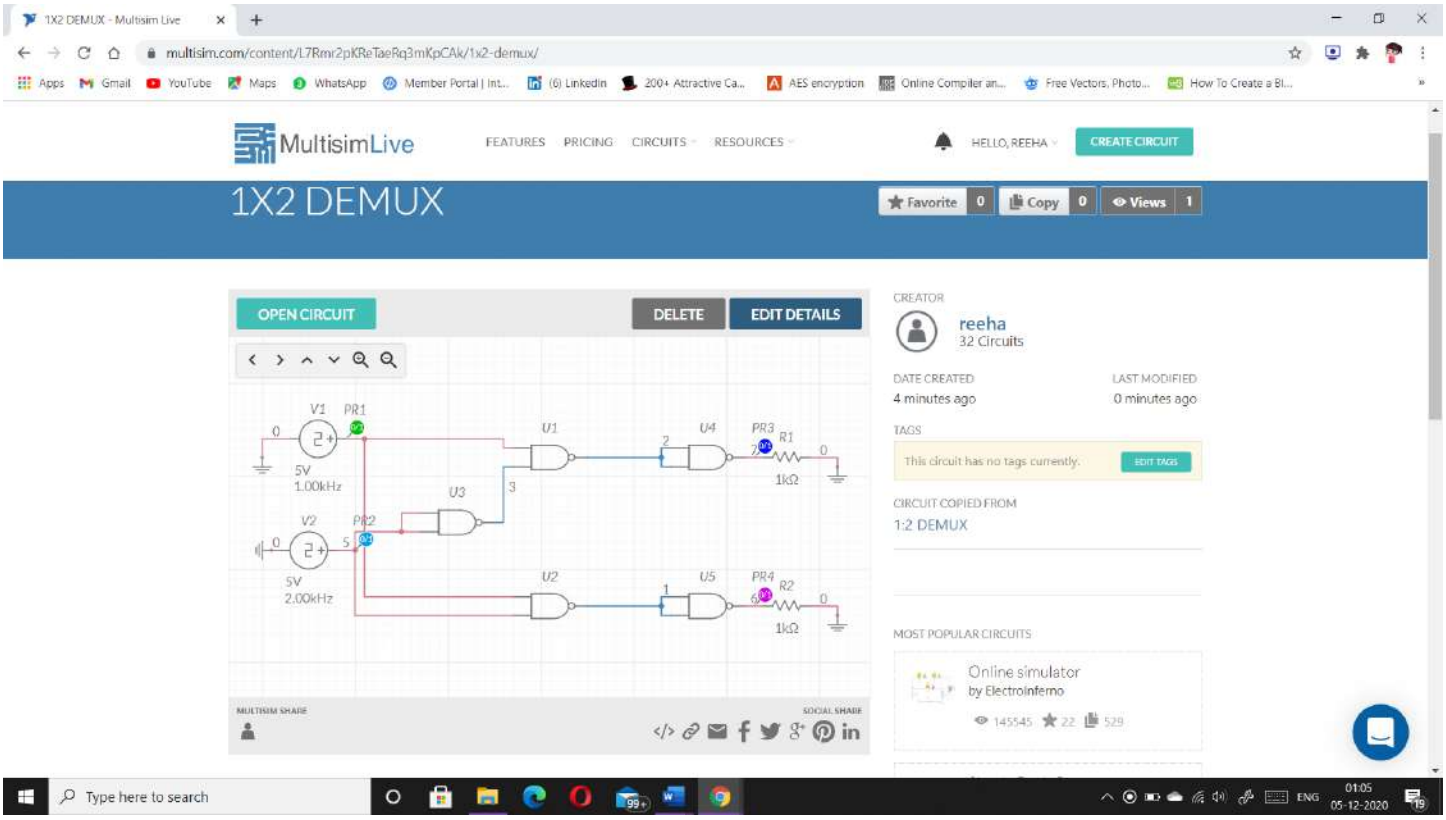
Circuits and Output waveform

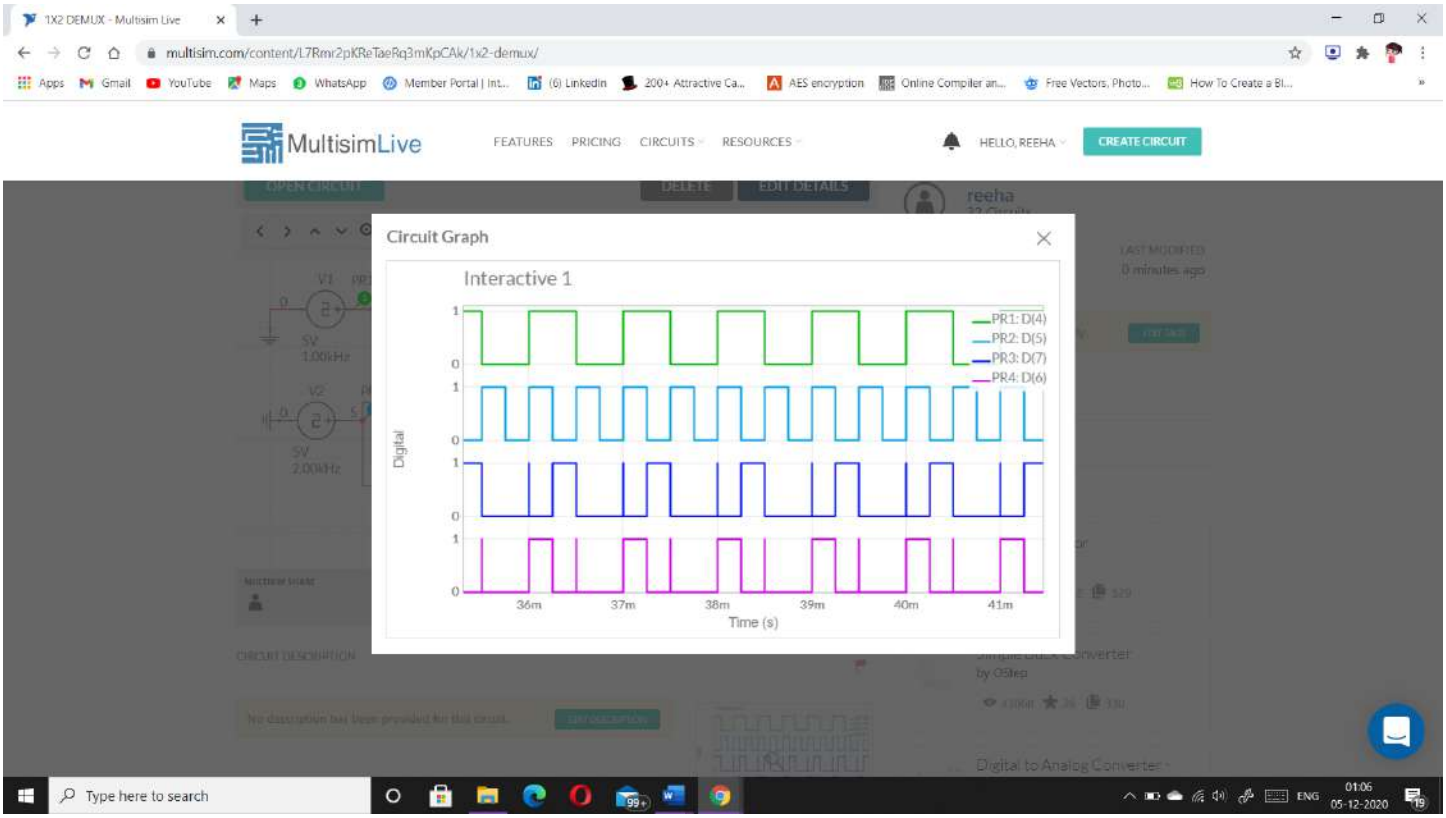
2 X 1 MUX




MUX 2X1 - Multisim Live
multisim.com/content/eQtXY8xDR9d8AYo328KNaK/mux-2x1/
MultisimLive
FEATURES
PRICING
CIRCUITS
RESOURCES
HELLO, REEHA
CREATE CIRCUIT
Circuit Graph
Interactive 1
PR1: D(4)
PR2: D(5)
PR3: D(6)
PR4: D(7)
Digital
Time (s)
77m
77.5m
78m
78.5m
79m
79.5m
80m
80.5m
81m
Digital to Analog Converter - DAC
by SILRing
Type here to search
ENG
00:57
05-12-2020

1 X 2 DEMUX


1X2 DEMUX - Multisim Live
multisim.com/content/L7Rmr2pKReTaeRq3mKpCAk/1x2-demux/
MultisimLive
FEATURES
PRICING
CIRCUITS
RESOURCES
HELLO, REEHA
CREATE CIRCUIT
1X2 DEMUX
Favorite 0
Copy 0
Views 1
OPEN CIRCUIT
DELETE
EDIT DETAILS
V1
PR1
5V
1.00kHz
V2
PR2
5V
2.00kHz
U1
U2
U3
U4
U5
PR3
PR4
R1
R2
1kΩ
CREATOR
reeha
32 Circuits
DATE CREATED
4 minutes ago
LAST MODIFIED
0 minutes ago
TAGS
This circuit has no tags currently.
EDIT TAGS
CIRCUIT COPIED FROM
1:2 DEMUX
MOST POPULAR CIRCUITS
Online simulator
by ElectroInferno
MULTISIM SHARE
SOCIAL SHARE
Type here to search
ENG
01:05
05-12-2020



VIVA-VOCE QUESTIONS:

Q1. What is multiplexer?

Ans.

Multiplexer means many into one. A multiplexer is a circuit used to select and route any one of the several input signals to a signal output. An simple example of an non electronic circuit of a multiplexer is a single pole multiposition switch.

Q2. What is difference between decoder and demultiplexer?

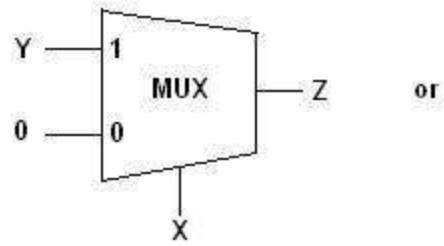
Ans.

S.NO.	COMPARISON	DECODER	DEMULTIPLEXER
1.	Basic	These are Logic circuit which decodes an encrypted input stream from one to another format.	It is a Combination circuit which routes a single input signal to one of several output signals.
2.	Input/Output	n number of input lines and 2n number of output lines.	n number of select lines and 2n number of output lines.
3.	Inverse of	Encoder.	Multiplexer.

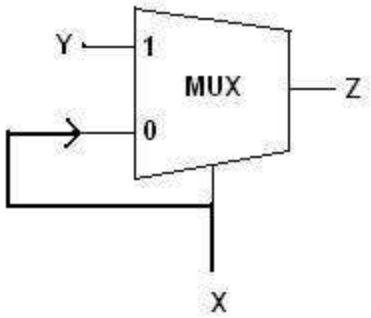
4.	Application	In Detection of bits, data encoding.	In Distribution of the data, switching.
5.	Use	It is used for changing the format of the instruction in the machine specific language.	It is used as a routing device to route the data coming from one signal into multiple signals.
6.	Select Lines	Not contains.	Contains.
7.	Implementation	Majorly implemented in the networking application.	Employed in data-intensive applications where data need to be changed into another form.

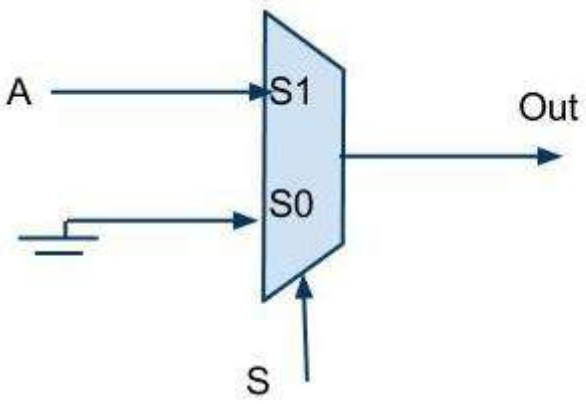
Q3. Implement a AND gate with multiplexers.

Ans.



or



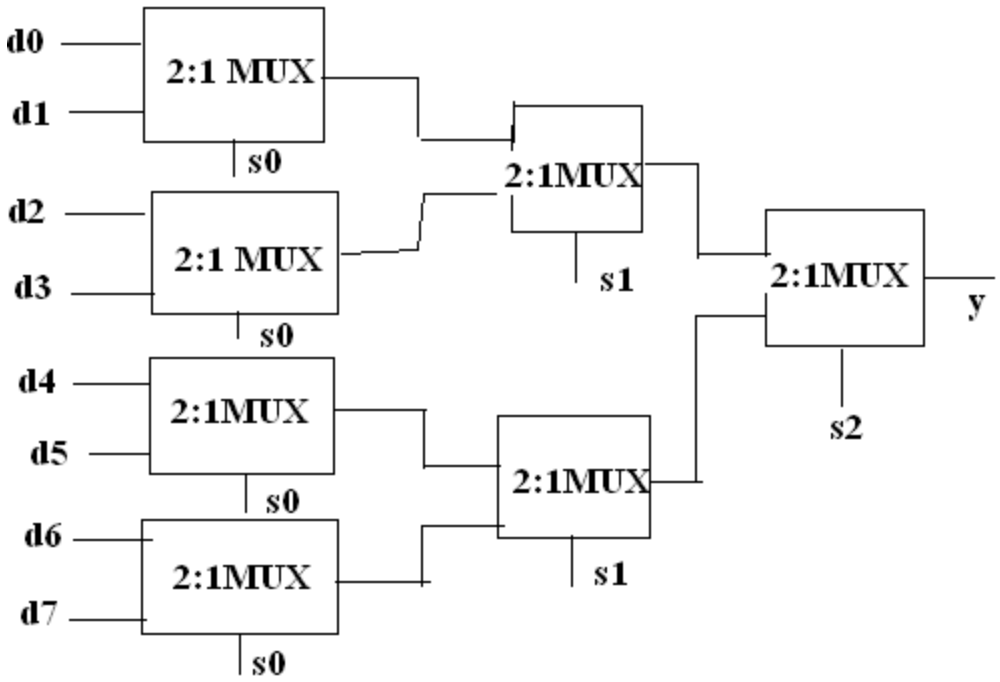


S	A	Out
0	0	0
0	1	0
1	0	0
1	1	1

Q4. How many 2x1 mux required to make 8x1 mux?

Ans.

Seven 2X1 MUX are required.


d0
d1
2:1 MUX
s0
d2
d3
2:1 MUX
s0
d4
d5
2:1MUX
s0
d6
d7
2:1MUX
s0
2:1MUX
s1
2:1MUX
s1
2:1MUX
y
s2

EXPERIMENT - 11

Switching Theory and Logic Design (STLD)

Aim

To realize J-K flip flop using logic gates or by using kit.

Syeda Reeha Quasar
14114802719
3C7

EXPERIMENT - 11

AIM:

To realize J-K flip flop using logic gates or by using kit.

Hardware and Software Apparatus Required

Hardware:

Breadboard, IC 7400 (NAND), IC 7410 (3 input NAND), LEDs, resistor(1k), capacitor(.1uF), diode, 5V power supply, connecting wires or Omega LTB-826, patch cords.

Software Simulation:

The schematic models of the desired circuits will be stimulated on MULTISIM (Free Software), easily accessible at www.multisim.com.

Components used – Source (Clock Voltage), Passive elements (resistor), Digital components (AND, OR, NAND, NOR, XOR, XNOR, Inverter), Probe for Analysis and annotation (Digital), Schematic connectors (Ground)

Theory:

The **JK Flip Flop** is the most widely used flip flop. The sequential operation of the JK Flip Flop is same as for the RS flip-flop with the same **SET** and **RESET** input. The difference is that the JK Flip Flop does not the invalid input states of the RS Latch (when S and R are both 1).The JK Flip Flop name has been kept on the inventor name of the circuit known as **Jack Kilby.** S and R inputs of the RS bistable have been replaced by the two inputs called the J and K input respectively. Here J = S and K = R. The two input AND gates of the RS flip-flop is replaced by the two 3 inputs NAND gates as shown in figure 7.1(a) ,with the third input of each gate connected to the outputs at Q and $\bar{Q}$. This cross coupling of the RS Flip-Flop is used to produce toggle action. Clock will be provided by R-C circuit followed by diode as shown in figure 7.1(b).

Logic Diagram of J-K Flip Flop-

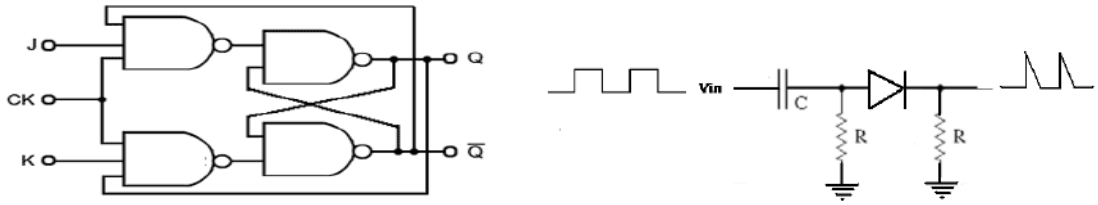


Fig 7.1 a) J-K Flip Flop b) clock provider circuit

Working of flip flop is depicted in truth table given below

Truth Table For J-K Flip Flop:

J	K	CLK	Q	$\overline{Q}$	*Comment*
0	0	↑	Q	$\overline{Q}$	Latch
1	0	↑	1	0	SET
0	1	↑	0	1	RESET
1	1	↑	$\overline{Q}$	Q	TOGGLE
X	X	0	Q	$\overline{Q}$	*NO Change !*

Pin Configuration of IC 7410

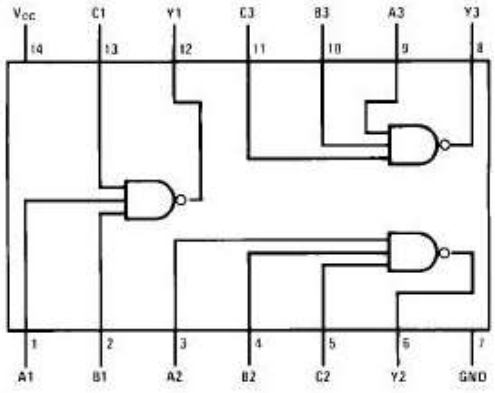


Fig 7.2 Pin configuration of IC used

Procedure:

1. Check all the components for their working.
2. Insert the appropriate IC into the IC base.
3. Make connections as shown in the circuit diagram.
4. Verify the results and observe the outputs.
5. While working on kit
6. Made connections as shown in circuit diagram on kit using patch cords.

Multisim:

1. Click on the 'Create Circuit' option on the top right corner of the profile in NI
2. Multisim webpage.
3. The schematic representation opens in a new tab.
4. Place three 'Ground' Schematic connector on the screen.
5. Place the logic gates from the digital section on the board, as per the required circuit diagram for circuits given.
6. Now, add clock voltages to the input of the logic gate and connect them with the help of Ground present in 'Schematic Connectors'.
7. Change the frequency of clock voltages e.g V1(say=5kHz) and V2(say=3kHz) etc.
8. Connect a resistor to the output of the logic gate and then, Ground it with the help of Ground Schematic Connector.
9. Connect the components with connecting wires.
10. Add digital probes to both input and output connections.
11. Set the display to 'Transient' from Interactive and press the 'Start
12. Simulation' button.
13. Note the graph

PRECAUTIONS:

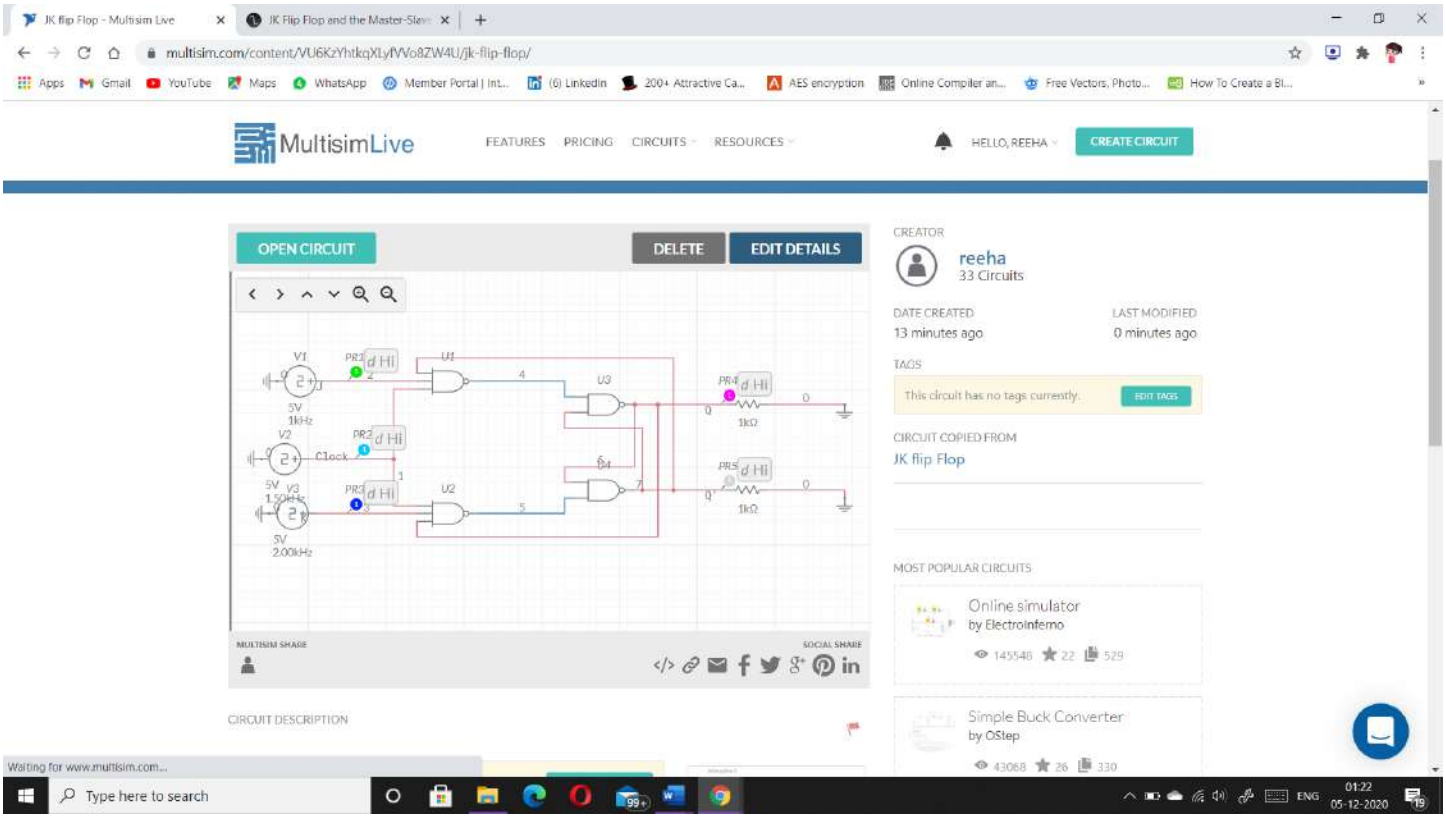
1. All ICs should be checked before starting the experiment.
2. All the connection should be tight.
3. Always connect ground first and then the supply.
4. Switch off the power supply after completion of the experiment.

RESULT:

The J-K flip flop has been studied and its truth table has been verified.

Circuits and Output waveform

JK Flip Flop


JK flip Flop - Multisim Live
JK Flip Flop and the Master-Slave
multisim.com/content/VU6KzYhtkqXLyfVVo8ZW4U/jk-flip-flop/
MultisimLive
FEATURES
PRICING
CIRCUITS
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HELLO, REEHA
CREATE CIRCUIT
OPEN CIRCUIT
DELETE
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CREATOR
reeha
33 Circuits
DATE CREATED
13 minutes ago
LAST MODIFIED
0 minutes ago
TAGS
This circuit has no tags currently.
EDIT TAGS
CIRCUIT COPIED FROM
JK flip Flop
MOST POPULAR CIRCUITS
Online simulator
by ElectroInfemo
Simple Buck Converter
by OStep
CIRCUIT DESCRIPTION
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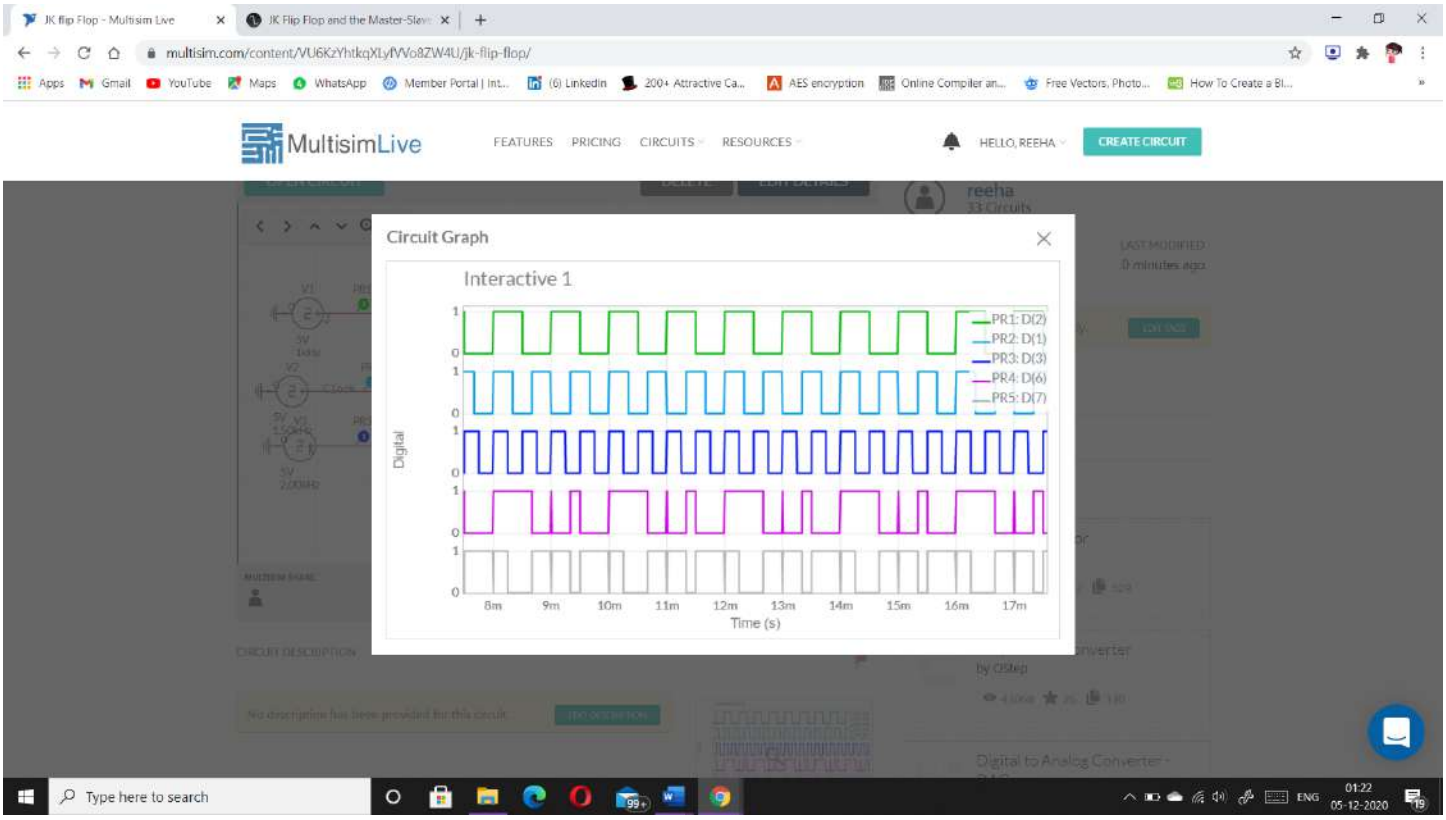
JK flip Flop - Multisim Live
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FEATURES
PRICING
CIRCUITS
RESOURCES
HELLO, REEHA
CREATE CIRCUIT
Circuit Graph
Interactive 1
PR1: D(2)
PR2: D(1)
PR3: D(3)
PR4: D(6)
PR5: D(7)
Digital
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VIVA-VOCE QUESTIONS:

Q1. Difference between sequential and combinational circuits.

Ans.

Combinational circuits are defined as the time independent circuits which do not depends upon previous inputs to generate any output are termed as combinational circuits. **Sequential circuits** are those which are dependent on clock cycles and depends on present as well as past inputs to generate any output.

Combinational Circuit –

1. In this output depends only upon present input.
2. Speed is fast.
3. It is designed easy.
4. There is no feedback between input and output.
5. This is time independent.
6. Elementary building blocks: Logic gates
7. Used for arithmetic as well as boolean operations.
8. Combinational circuits don't have capability to store any state.
9. As combinational circuits don't have clock, they don't require triggering.
10. These circuits do not have any memory element.
11. It is easy to use and handle.

Examples – Encoder, Decoder, Multiplexer, Demultiplexer

Block Diagram –

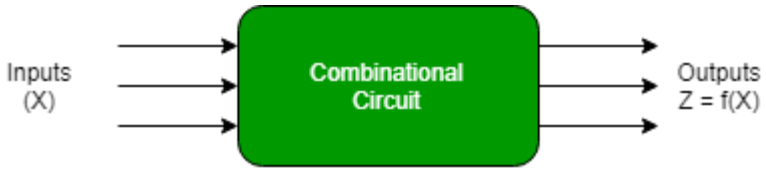

Figure: Combinational Circuits

Sequential Circuit –

1. In this output depends upon present as well as past input.
2. Speed is slow.
3. It is designed tough as compared to combinational circuits.

4. There exists a feedback path between input and output.
5. This is time dependent.
6. Elementary building blocks: Flip-flops
7. Mainly used for storing data.
8. Sequential circuits have capability to store any state or to retain earlier state.
9. As sequential circuits are clock dependent they need triggering.
10. These circuits have memory element.
11. It is not easy to use and handle.

Examples – Flip-flops, Counters

Block Diagram –

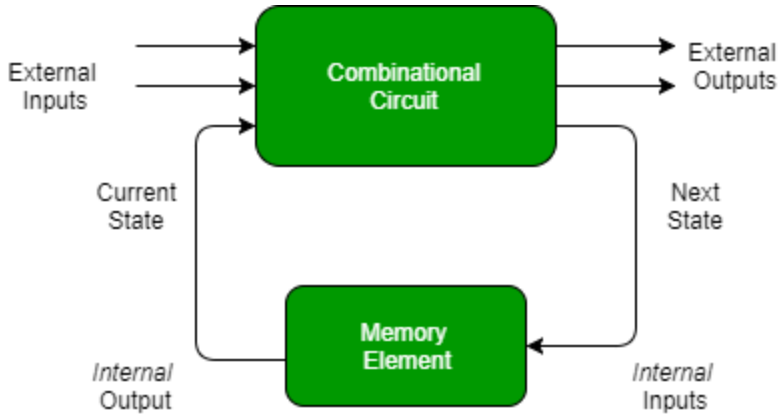

Figure: Sequential Circuit

Q2. List four Basic Flip-flop applications.

Ans.

Application of the flip flop circuit mainly involves in bounce elimination switch, data storage, data transfer, latch, registers, counters, frequency division, memory, etc.

Some of the most common applications of flip – flops are

- Counters
- Registers
- Frequency Divider circuits
- Data transfer

Q3. What advantage does a J-K Flip-flop have over an S-R?

Ans.

The J-K flip-flop is much faster. The J-K flip-flop does not have propagation delay problems. The J-K flip-flop has a toggle state.

The RS flip-flop has a “forbidden input state” with S and R both 1. In this state both Q and Not Q outputs will be 1 - which is bad enough - and the state of the flip-flop after R and S return to more sensible inputs depends on the order in which that happens.

The big difference of the JK flip-flop is, that the case J = K = 1 is allowed and toggles the output state. In everything else it works like a RS flip-flop.

So the JK flip-flop is a slightly enhanced version of the RS flip-flop. But better yet are gated flip-flops - they need slightly more gates but you have a lot better control over when the output changes.

Q4. What is meant by Race around condition and how we can overcome this problem?

Ans.

If the clock is High for a time interval less than the propagation delay of the flip flop then racing around condition can be eliminated. This is done by using the edge-triggered flip flop rather than using the level-triggered flip-flop.

When the input to the JK flip-flop is j=1 and k=1, the race around condition occurs, i.e it occurs when the time period of the clock pulse is greater than the propagation delay of the flip flop. so the output changes or toggles in a single clock period.