EXPERIMENT - 4

Switching Theory and Logic Design (STLD)

Aim

To realize the circuit for Half Adder and Full Adder using logic gates.

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3C7

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AIM:

To realize the circuit for Half Adder and Full Adder using logic gates.

Hardware and Software Apparatus Required

Hardware:

- ❖ Power supply, Bread Board, Connecting Wires, respective IC, LED, Wire Cutter.
- ❖ Circuit is designed on bread board using Integrated Chips (ICs), Voltage supply and LEDS.
- ❖ The set-up of apparatus and working of the circuit were demonstrated via recorded videos.

Software Simulation:

The schematic models of the desired circuits will be stimulated on MULTISIM (Free Software), easily accessible at www.multisim.com.

Components used – Source (Clock Voltage), Passive elements (resistor), Digital components (AND, OR, NAND, NOR, XOR, XNOR, Inverter), Probe for Analysis and annotation (Digital), Schematic connectors (Ground)

Theory:

An Adder is a device that can add two binary digits. It is a type of digital circuit that performs the operation of additions of two number. It is mainly designed for the addition of binary number, but they can be used in various other applications like binary code decimal, address decoding, table index calculation, etc. There are two types of Adder. One is Half Adder, and another one is known as Full Adder.

Half Adder

There are two inputs and two outputs in a Half Adder. Inputs are named as A and B, and the outputs are named as Sum (S) and Carry (C). The Sum is X-OR of the input A and B. Carry is AND of the input A and B. With the help of half adder, one can design a circuit that is capable of performing simple addition with the help of logic gates. Let us first take a look at the addition of single bits.

$$0 + 0 = 0$$

$$0 + 1 = 1$$

$$1 + 0 = 1$$

$$1 + 1 = 10$$

These are the least possible single bit combinations. But the result for 1 + 1 =10. This problem can be solved with the help of an EX – OR gate. The sum results can be re-written as a 2-bit output. Thus the above combination can be written as

$$0 + 0 = 00$$

0 + 1 = 01

1 + 0 = 01

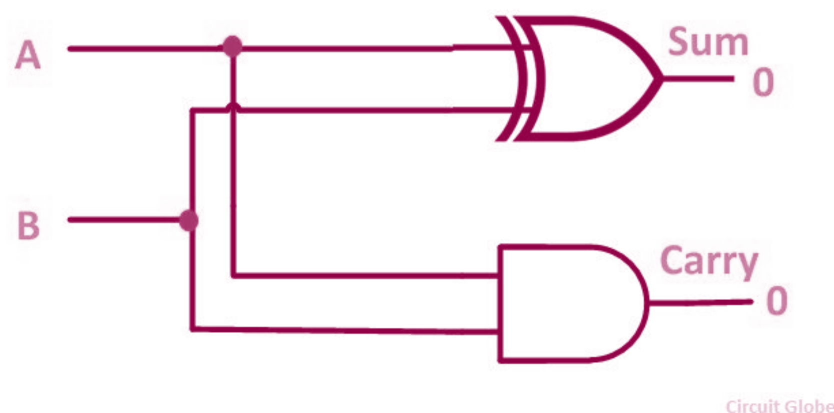
1 + 1 = 10

Here the output "1" of "10" becomes the carry-out. **SUM** is the normal output and the **CARRY** is the carry-out.

The **truth table** of the half adder is shown below.

Inputs		**Outputs**	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

The **Half Adder Circuit** is shown below.



The main disadvantage of this circuit is that it can only add two inputs and if there is any carry it is neglected. Thus, the process is incomplete. To overcome this difficulty Full Adder is designed. While performing complex addition, there may be cases when you have to add two 8 bit bytes together. This can be done with the help of Full Adder.

Full Adder

The full adder is a little more difficult to implement than a half adder. The main difference between a half adder and a full adder is that the full adder has three inputs and two outputs. The two inputs are A and B, and the third input is a carry input C_{IN}. The output carry is designated as C_{OUT}, and the normal output is designated as S.

The **truth table** of the Full Adder Circuit is shown below.

Inputs			**Outputs**	
A	B	CIN	COUT	S
0	0	0	0	0
0	0	1	0	1

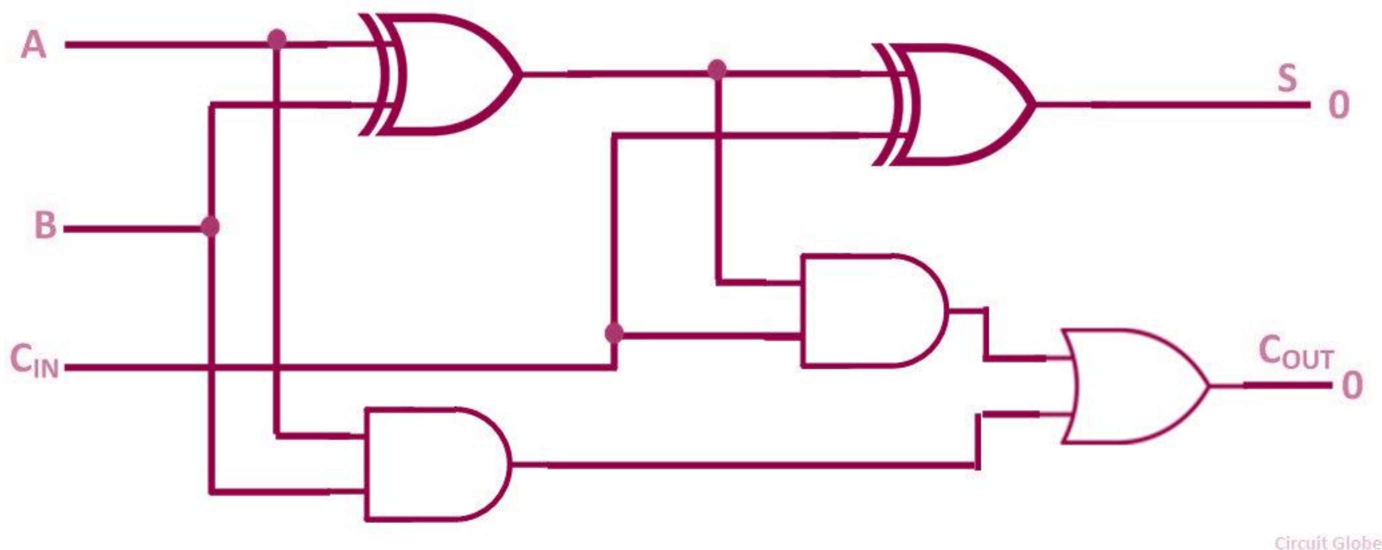
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

The output S is an EX – OR between the input A and the half adder SUM output B. The C_{OUT} will be true only if any of the two inputs out of the three are HIGH or at logic 1.

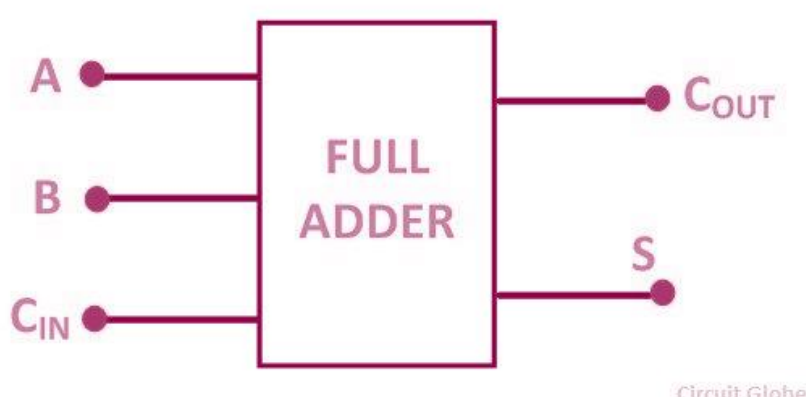
Thus, a full adder circuit can be implemented with the help of two half adder circuits. The first half adder circuit will be used to add A and B to produce a partial sum. The second half adder logic can be used to add C_{IN} to the sum produced by the first half adder circuit. Finally, the output S is obtained.

If any of the half adder logic produces a carry, there will be an output carry. Thus, C_{OUT} will be an OR function of the half adder CARRY outputs.

The **Full adder circuit diagram** is shown below.

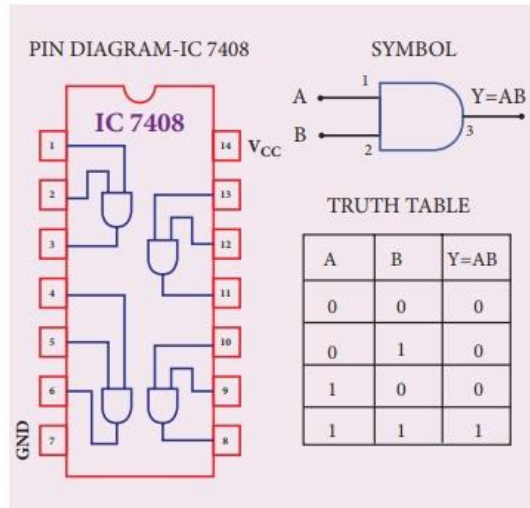


The schematic representation of a single bit Full Adder is shown below.

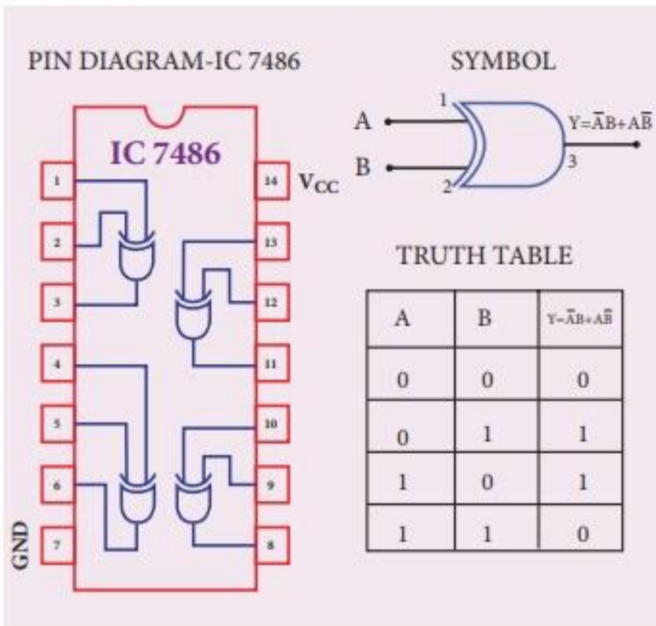


Circuit Symbol, pin diagram and Truth table of gates used:

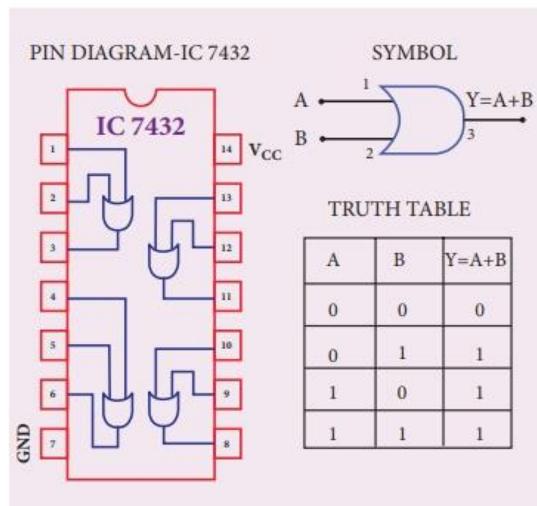
AND Gate:



X-OR Gate :



OR Gate:

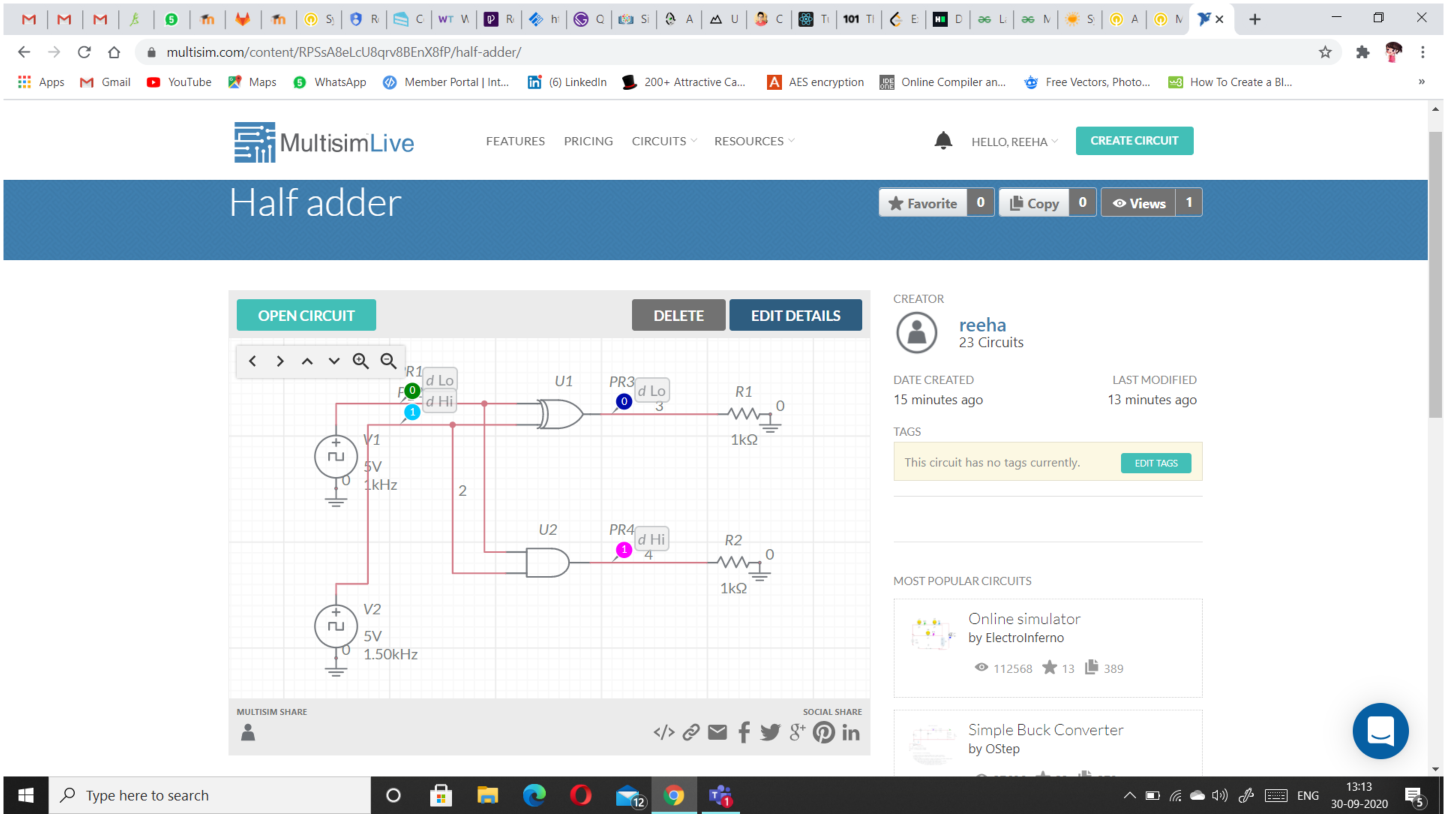


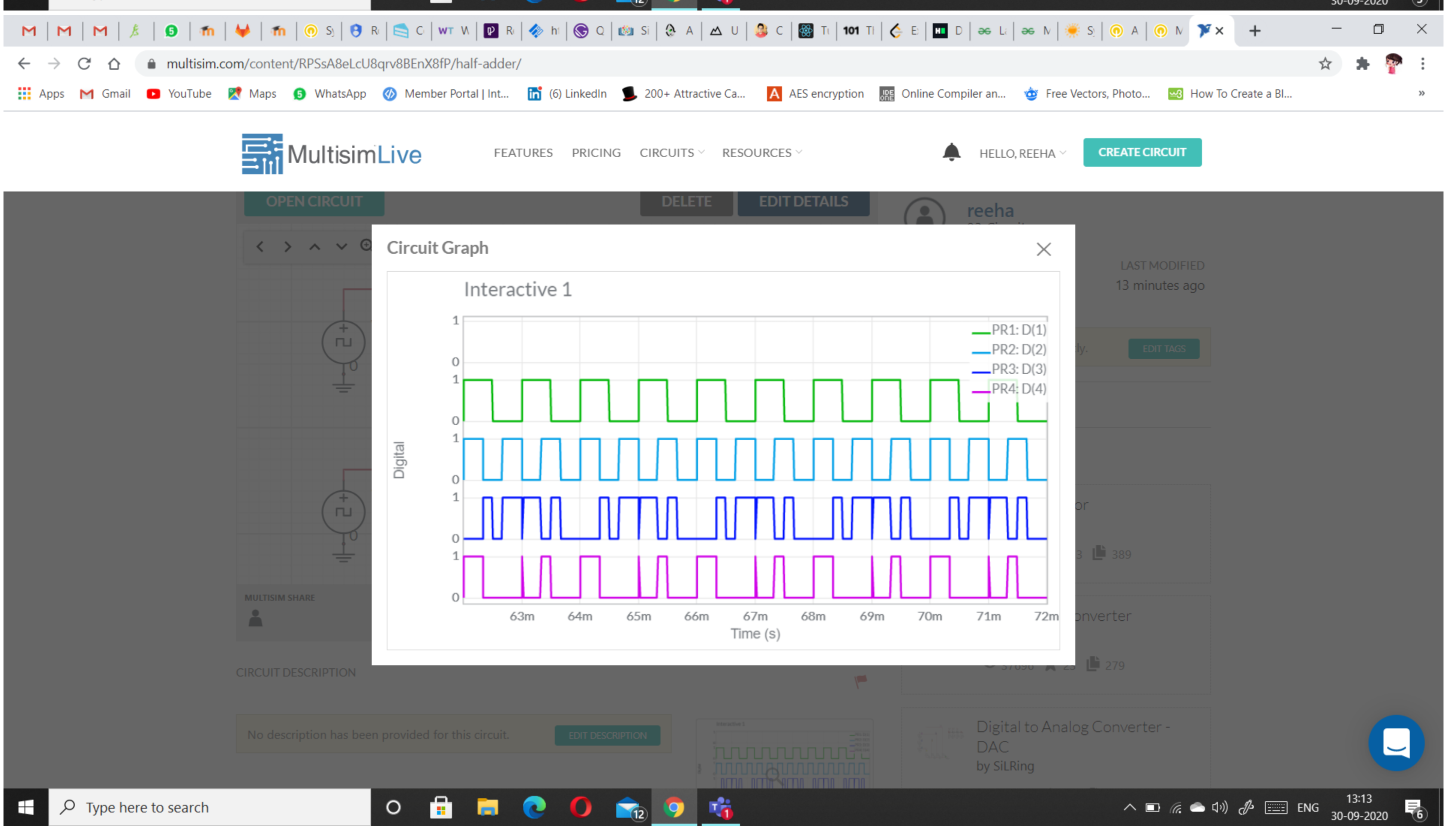
Procedure followed on MULTISIM:

1. LOG IN ON www.multisim.com
2. CREATE THE CIRCUIT
3. SAVE THE CIRCUIT
4. SAVE THE SCREENSHOTS FOR
   i. INPUT & OUTPUT WAVEFORMS (ALONG WITH YOUR ID ON TOP LEFT)
   ii. CIRCUIT (ALONG WITH YOUR ID ON TOP LEFT)

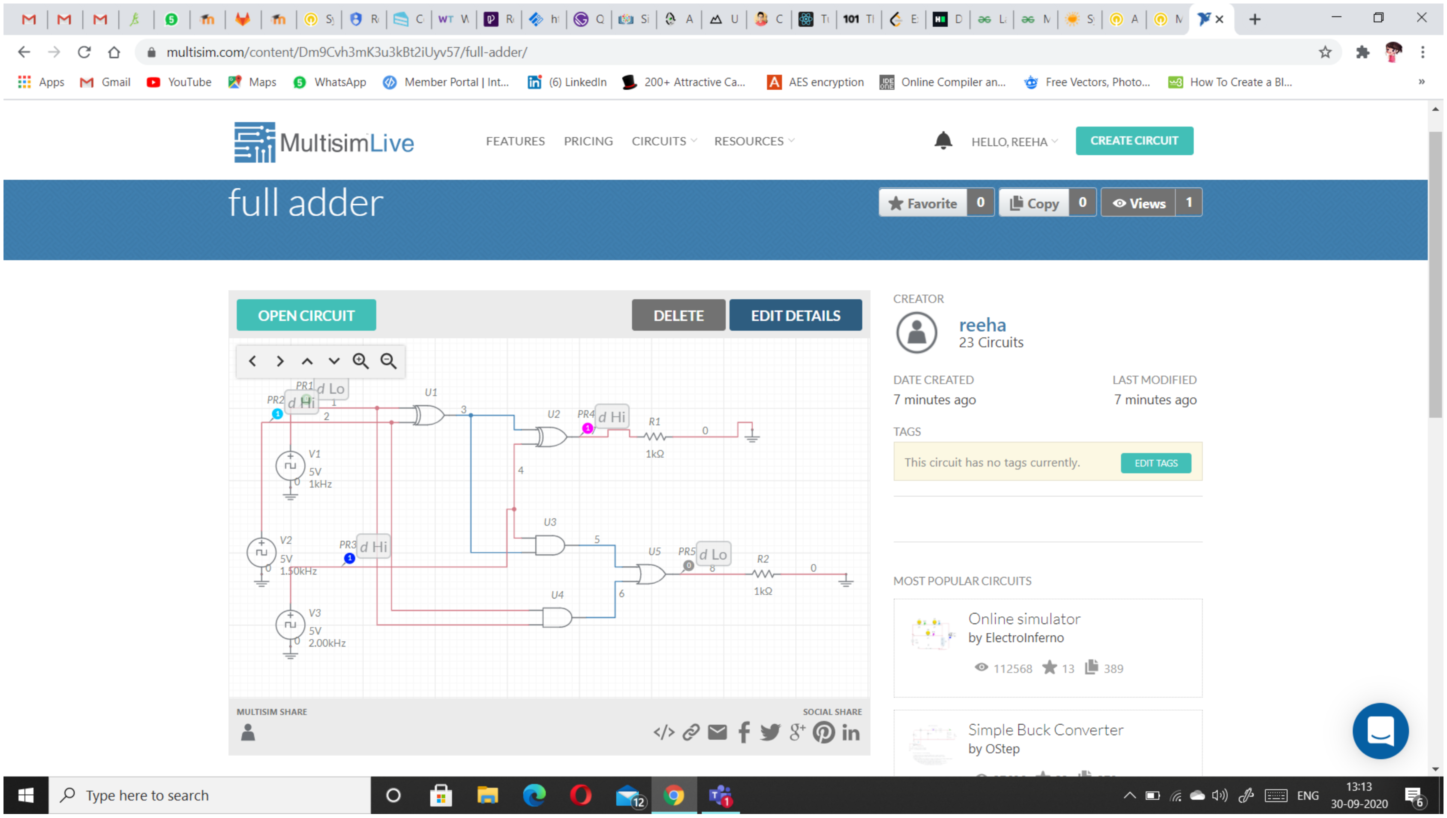
Circuits and Output waveform

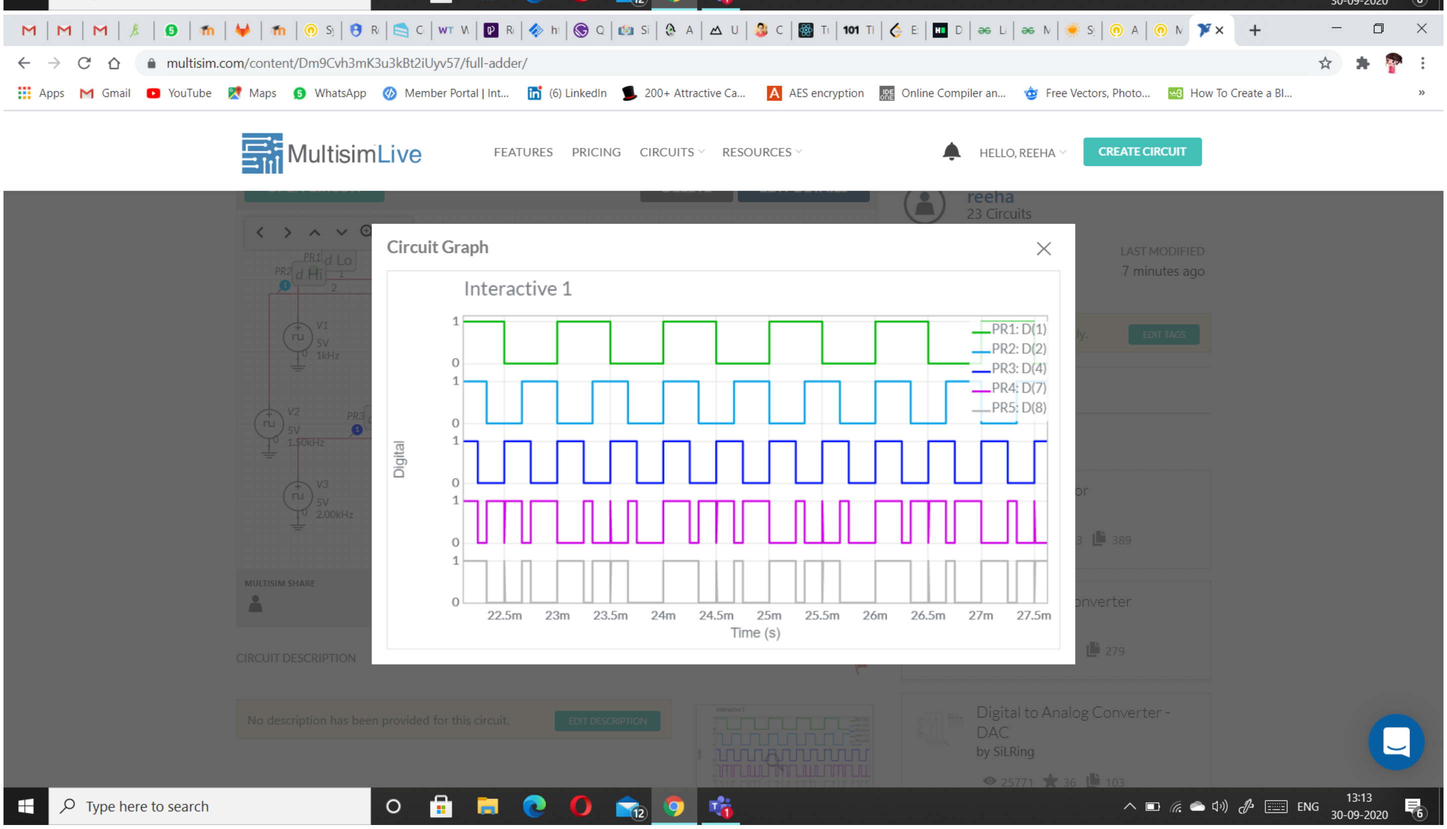
Half Adder


multisim.com/content/RPSsA8eLcU8qrv8BEnX8fP/half-adder/
MultisimLive
FEATURES
PRICING
CIRCUITS
RESOURCES
HELLO, REEHA
CREATE CIRCUIT
Half adder
Favorite 0
Copy 0
Views 1
OPEN CIRCUIT
DELETE
EDIT DETAILS
U1
PR3
R1
1kΩ
V1
5V
1kHz
U2
PR4
R2
1kΩ
V2
5V
1.50kHz
CREATOR
reeha
23 Circuits
DATE CREATED
15 minutes ago
LAST MODIFIED
13 minutes ago
TAGS
This circuit has no tags currently.
EDIT TAGS
MOST POPULAR CIRCUITS
Online simulator
by ElectroInferno
Simple Buck Converter
by OStep
Type here to search
13:13
30-09-2020


multisim.com/content/RPSsA8eLcU8qrv8BEnX8fP/half-adder/
MultisimLive
Circuit Graph
Interactive 1
PR1: D(1)
PR2: D(2)
PR3: D(3)
PR4: D(4)
Digital
63m
64m
65m
66m
67m
68m
69m
70m
71m
72m
Time (s)
Type here to search
13:13
30-09-2020

Full Adder




Circuit Graph
Interactive 1
PR1: D(1)
PR2: D(2)
PR3: D(4)
PR4: D(7)
PR5: D(8)
Digital
Time (s)