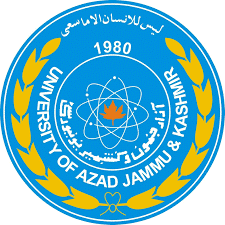
**The University of Azad Jammu and Kashmir, Muzaffarabad.**

**Computer Architecture & Logic Design**

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|  |  |
| --- | --- |
| Students Name: | Syed Abdulrehman Naseem |
| Roll No: | 2024-SE-18 |
| Instructor: | Engr.Dr. Sidra Rafique |
| Lab Title | **Full & Half Adders, Full & Half Subtractors** |
| Submission Date: | 09-August-2025 |

**Department of Software Engineering**

**1.Full-Adder Circuit**



**Using Logic**

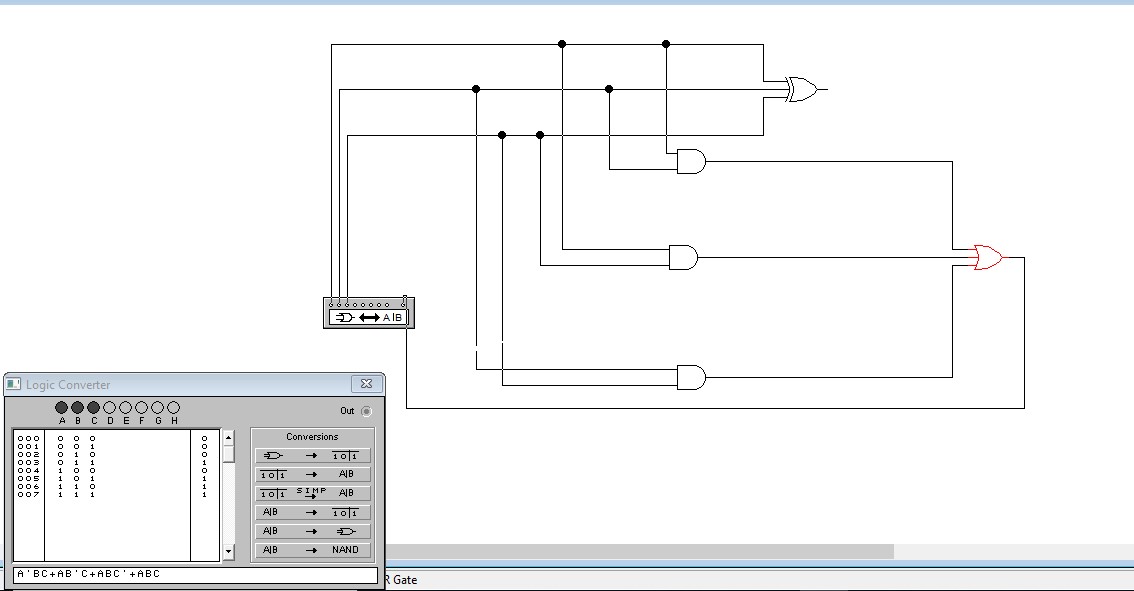
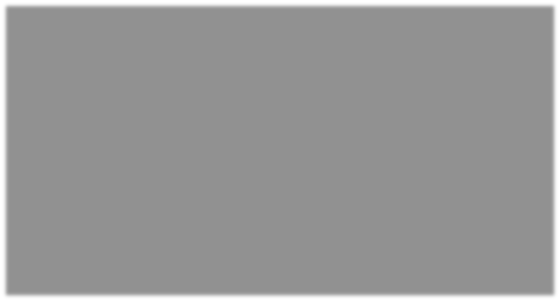
**Gates**

***Figure***

***1***

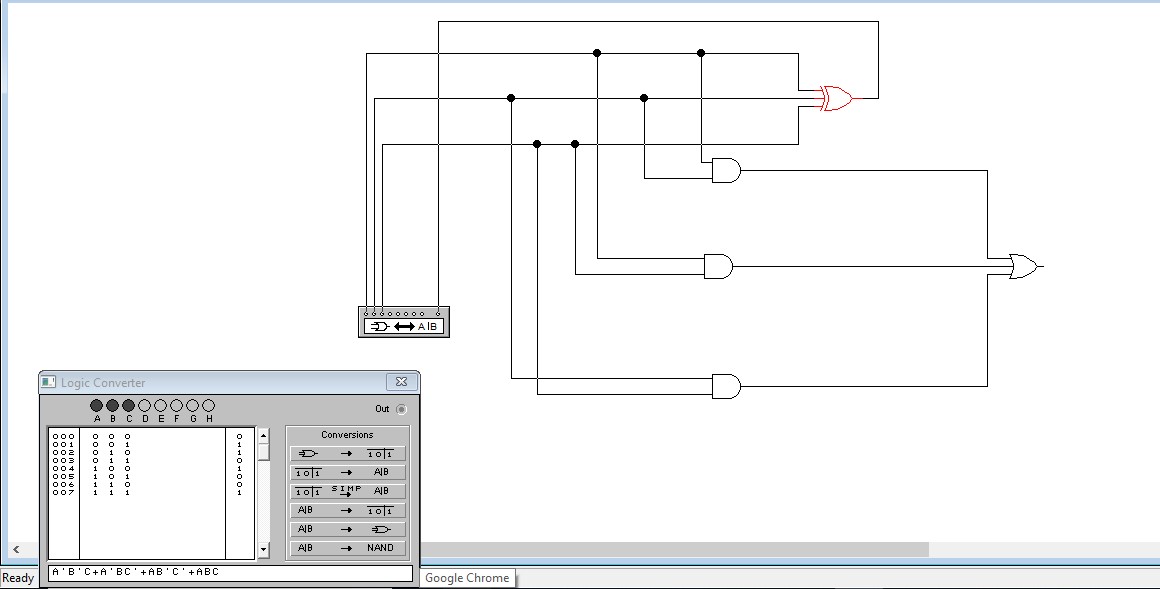
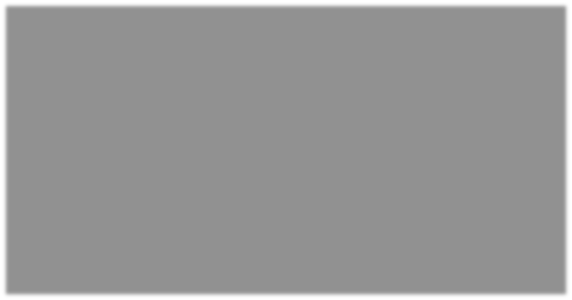
***:***

***carry output***



***Figure 2:***

***sum output***

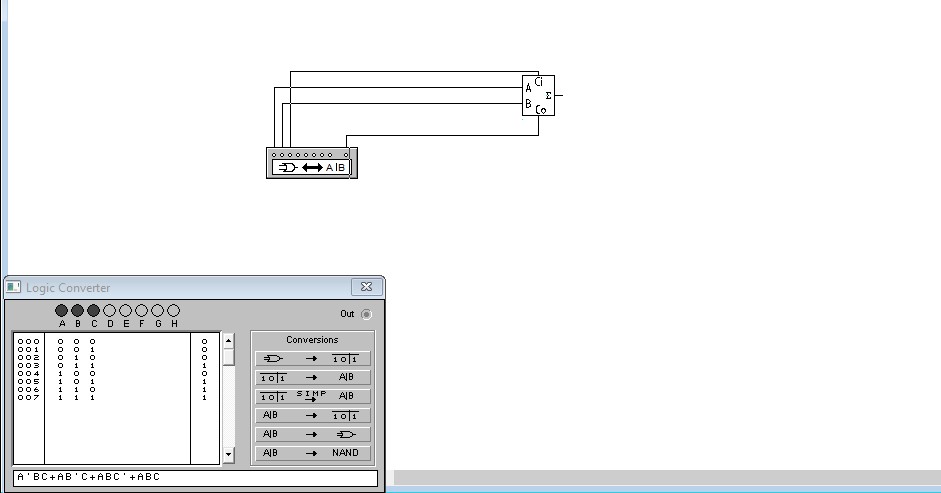
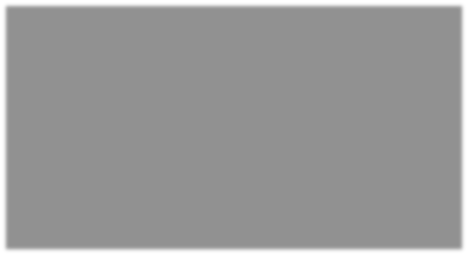


## Using built-in Full Adder

***Figure***

***3:***

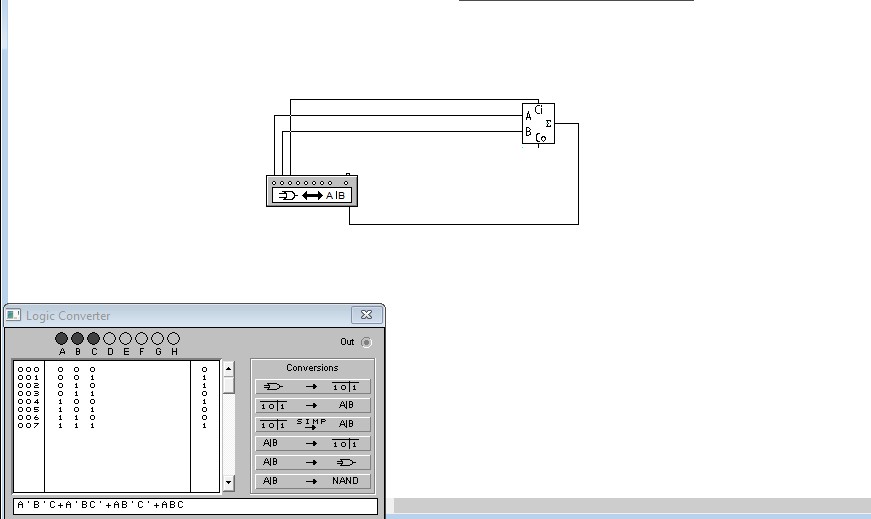
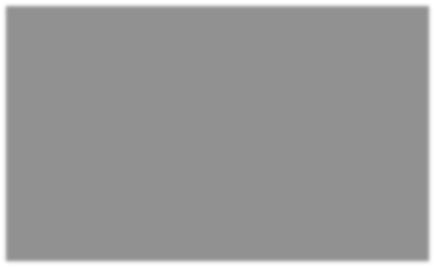
***carry output***



***Figure***

***4:***

***sum output***



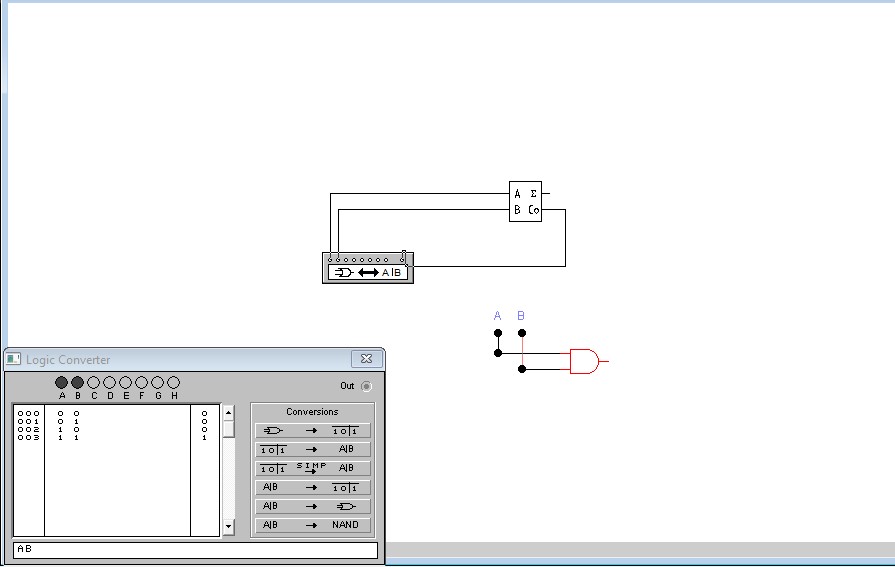
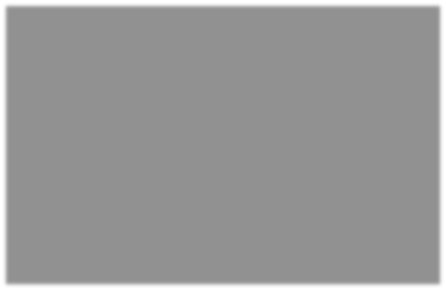
**2.Half Adder**

## Using built-in Half Adder

***Figure***

***5:***

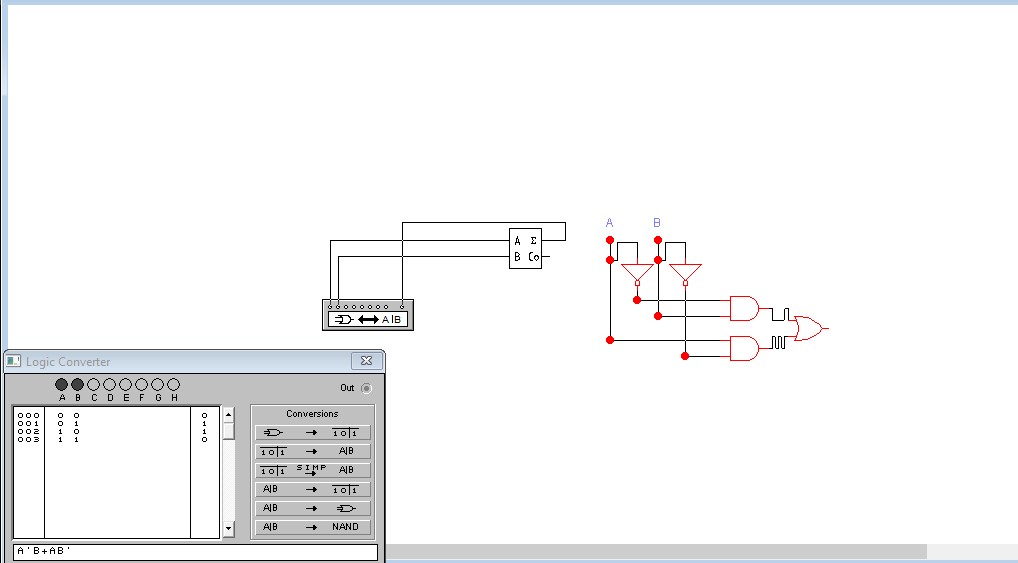
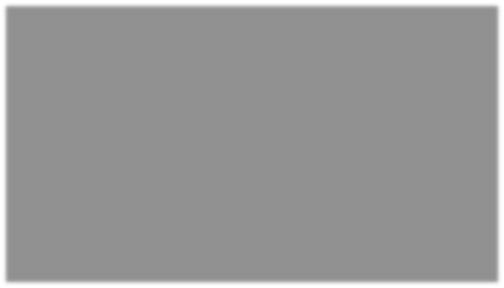
***carry output***



***Figure***

***6:***

***sum output***

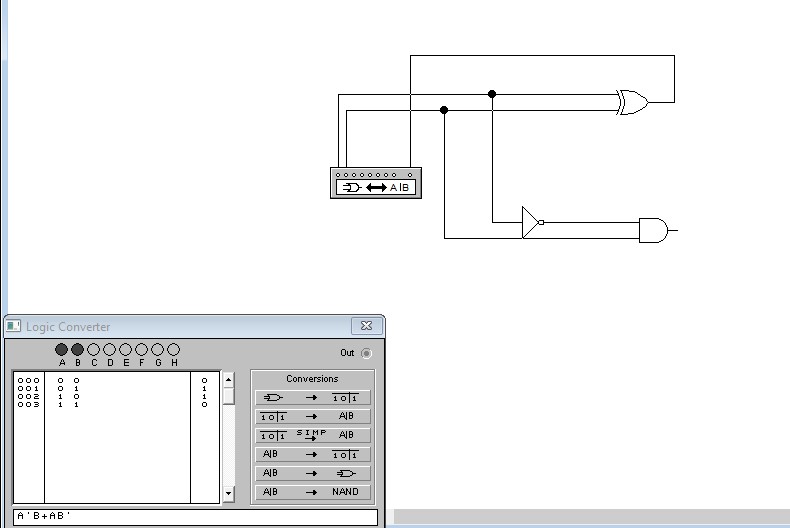
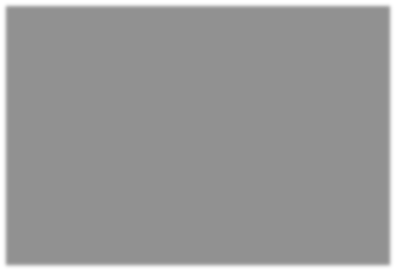


**3.Half Subtractor**  **Using Logic Gates**

***Figure***

***7:***

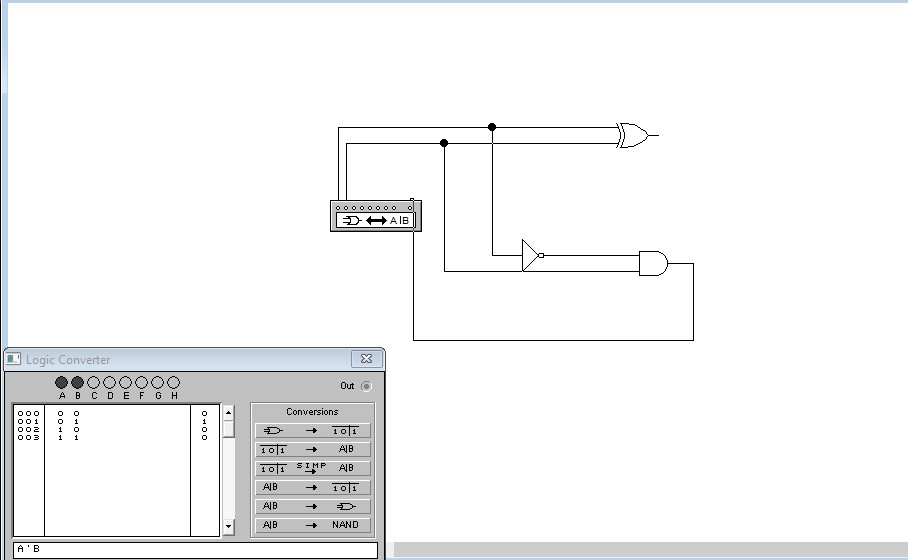
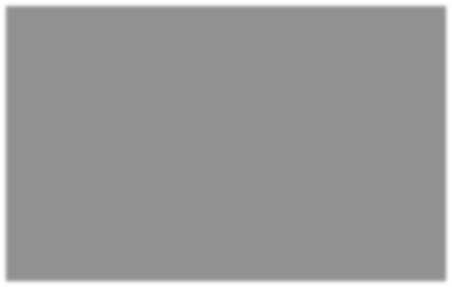
***difference output***



***Figure***

***8:***

***borrow output***



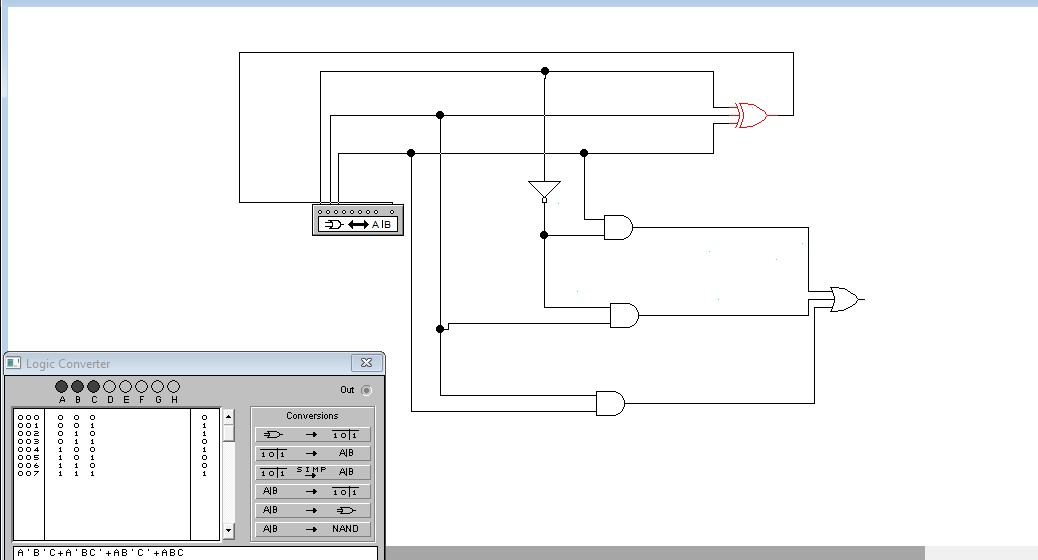
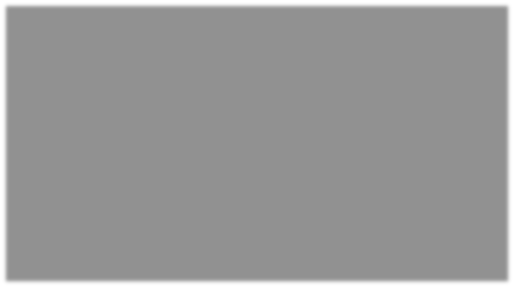
**4.Full Subtractor**

 **Using Logic Gates**

***Figure***

***9:***

***difference output***



***Figure***

***10:***

***borrow output***

