Digital Logic Design

Title	Digital Logic Design
Code	CS -
Credit hours	3 + 1
Prerequisite	None
Follow Up	CS-, CS-
Objective	The course aims at providing knowledge of various logic gates and flip flops and their characteristic truth tables to enable students to design and analyze combinational and sequential circuits. The important combinational circuits e.g., encoders, decoders, multiplexer, de-multiplexer and their applications are discussed in length. Students should be able to design a simple ALU using these standard circuits. In sequential circuits, construction and design of various registers, counters, memories and their applications are discussed.
Text Book	Digital Logic and Computer Design M. Morris Mano Eleventh Impresion,2009 Pearson Prentice Hall
Reference Book/s	Digital Fundamentals T. L. Floyd Prentice Hall, 8th Edition, 2002

Lecture #	TOPICS	Remarks
1	Introduction of Digital Computer. Binary, Octal, Decimal and Hexadecimal Number Systems. Conversion among various Number Systems.	
2	r's and r-1's Complements Subtractions using r's and r-1's Complements	
3	Binary Codes. (BCD, Excess-3, Biquinary, 84-2-1, 2421, Gray and ASCII. Introduction to Error Detection Codes. Binary storage and Registers	
4	Binary logic Switching circuits and binary signals Behavior of standard digital Gates and their pin configurations. (NOT, AND, OR, XOR, NAND, NOR, XNOR). Representing input and output of Digital Logic Gates using wave forms. Introduction to Integrated circuits	Assignment 1
5	Introduction to Boolean Algebra Basic theorems and properties of Boolean Algebra Boolean Functions	Quiz 1
6	Complement of a Function Concept of Minterms and Maxterms Representation of Function in Sum of Minterms or Product of Maxterms	
7	Conversion between Canonical Forms Standard Forms	
8	Introduction to Karnaugh Map Two-,Three- and Four- variable Maps Sum of Products Simplification	

9	Product of Sum Simplification NAND and NOR Implementation	
10	Don't care Conditions The Tabulation Method	
11	Determination of Prime-Implicants Selection of Prime Implicants	Assignment 2
12	Introduction to Combinational Logic Design of Adders Design of Subtractors	Quiz 2
13	Code Convertors	Assignment 3
14	Analysis Procedure of Combinational Circuits	
15	Multilevel NAND Circuits Multilevel NOR Circuits	
16	Revision	
17	Binary Parallel Adders Decimal Adders	
18	Magnitude Comparator	
19	Decoders Implementation of Boolean Functions using Decoders Decoder Expansion	Assignment 4
20	Multiplexers Implementation of Boolean Functions using Multiplexers Demultiplexers Encoders	
21	ROM Implementation of Boolean Functions using ROM	
22	Programmable Logic Array (PLA) Implementation of Boolean Functions using PLA	
23	Introduction to Sequential Circuits Basic Flip Flop	Quiz 3
24	Clocked RS Flip Flop Clocked D Flip Flop Clocked JK Flip Flop Clocked T Flip Flop	
25	Analysis of Clocked Sequential Circuits	
26	State Reduction and Assignment Flip Flop Excitation tables Design Procedure	Assignment 5
27	Introduction to Registers Representation of Unsigned numbers and Range of n-bit register Representation of signed numbers. (sign magnitude, 2's comp and 1's complement) and range of n-bit registers Design of a Register with parallel load	
28	Shift Registers Bidirectional Shift register with parallel load	Quiz 4
29	Ripple Counters	
30	Synchronous Counters	
31	Memory Unit	
32	Revision	