**

**ECE 4960: Computational and Software Engineering**

**Spring 2016**

**Programming Assignment 4: Compact SPICE for ODE Solution**

**1. Goal**

1. Write the transient simulation of SPICE
2. Use the error estimator to learn validation and adaptivity in physical simulations
3. Learn about version control system and concurrent software development

**2 Background preparation**

**2.1 Introduction of SPICE**

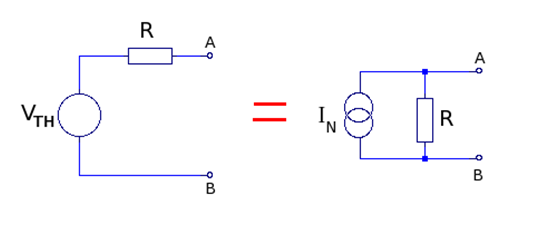
You probably have used SPICE for circuit simulation since your sophomore year. SPICE stands for Simulation Program with Integrated Circuits Emphasis. The integrated circuits (IC) in the naming means that all components in SPICE are much smaller than the shortest wavelength in consideration, where the wavelength is defined as *c/freq* with *c* being the speed of light and *freq* being the highest frequency of the circuit functions.

The regular SPICE contains three major part: the netlist (describing the circuits), the control (parameters for the solution method) and the output (print and plot of the nodal solutions). In our compact SPICE exercise, we will only implement the transient part of the SPICE simulation with some restriction on the netlist to ease up the implementation. However, most of the essence in the SPICE transient analysis is included, so SPICE is demystefied for you after knowing it for so long.

**2.2 Circuit elements in nodal analysis**

One of the ways to transform a topological description of circuits to the ODE formulation is the nodal analysis, where the voltage on each circuit node is the dependent variable in the ODE *dx/dt = f(x, t)*, and the function *f(x, t)* is derived from KCL. All nodal voltage is referenced to a ground node 0. We will implement only a few element types in the conventional nodal analysis: resistor *R*, capacitor *C*, current source *i(t)* and NMOS transistors with the EKV large-signal model in Program Assignment 3. The nodal voltages will be the unknown variables, and the current on each element branch will be assembled to the equations to be solved. Furthermore, we will assume that every node will have a capacitance to ground. This is the reality in integrated circuits, as no nodal voltage can respond instantaneously. However, the SPICE is also used to teach circuits, so not every node has a grounded capacitor in the regular SPICE. The selection and constraint are meant to make your ODE assembly easier, but without losing the general traits in the transient nodal analysis. For *R, C, i(t)* and NMOS, the current on the branch can be readily expressed. For example, the currents on *R* and *C* will be: *(V1 – V2)/R* and *C⋅d(V1 – V2)/dt*.

We do not include ideal voltage source here. Any realistic voltage source will have a source resistance, and then we can transfer the voltage source to a current source with the Norton equivalent circuits, as shown in Fig. 1. For ideal voltage sources, as the connected nodal voltage will be known but the branch current is unknown, a substitution of variables is needed. This will increase your implementation complexity, although it is not a difficult thing to program.



**Fig. 1.** The Thevenin and Norton equivalent circuits where IN (Norton) = VTH/R (Thevenin). Notice that the nodal voltage solutions of nodes A and B are identical in these two circuits, but not the power to be provided by the independent sources.

*R, C* and *i(t)* are two terminal devices, so they are not difficult in the assembly of KCL assuming the nodal voltage is the unknown depedent variables in the ODE. However, the transistor will be a three-terminal device (no further simplification possible in general), and we will use the following circuits in Fig. 2 for the transistor connection. The current source *ID, EKV* will be implemented as in Program Assignment 3. We will assume there is no direct DC current to the gate node (i.e., G will only have the *RC* displacement current).

*ID, EKV(VGS, VDS)*

*vgs*

***G***

***S***

***D***

*+*

*−*

**Fig. 2**. The MOSFET large-signal π model.

*VDS*

*+*

*−*

 (1)

The nodal voltages here are *VG* and *VD* for nodes G and D, with the node S assumed to be at ground (node 0). Surely there are transistor circuits when S is not grounded (say common-gate amplifiers and source followers), but the additional transformation is again not difficult to modify in your program.

**2.3 From SPICE to ODE: Assembly of ODE from nodal analysis by KCL**

We will use a simple RC circuit to illustrate the ODE assembly from KCL. In Fig. 3, we have two nodes, three resistors, 2 grounded capacitors on the two nodes, and one time-dependent current source.

*R1*

*R2*

*i(t)*

**1**

*R3*

**2**

**0**

*C1*

*C2*

**Fig. 3**. Simple RC circuits to illustrate the ODE assembly from the circuit schematic.

KCL on node 1: ;

KCL on node 2: ;

To cast these two KCL equations in the form of :

We will give another example of a common-source (CS) amplifier with gate resistance in Fig. 4. The CS amplifier is a fundamental building block for many analog circuit, which provides a very large voltage gain in the small-signal range of *vin(t)*. We will now try to transform the circuits into an ODE description.

*RG*

*RL*

**1**

**2**

**0**

**Fig. 4**. A common-source amplifier

*vout*

*vin(t)*

*+*

*−*

*+*

*−*

From the equivalent circuits in Fig. 5(a) as transformed from Fig. 2,

KCL on node 1: ;

KCL on node 2: ;

To cast these two KCL equations in the form of : (notice that due to the nonlinear *ID,EKV* term, we cannot express the system in the array form.

;

;

*iin(t)*

*RL*

*C1*

*C2*

**Fig. 5**. Two possible equivalent circuits for the common-source amplifier: (a) Unilateral; (b) Bilateral coupling due to the Miller capacitance *CGD*.

*ID, EKV*

*RG*

*iDD*

**1**

**0**

**2**

*RL*

*C1*

*C2*

*ID, EKV*

*RG*

*iDD*

**1**

**0**

**2**

*CGD*

**(a)**

**(b)**

*iin(t)*

Notice that the equivalent circuits in Fig. 5(a) is unilateral, so *f1(V1, V2)* does not depend on *V2*, as the CS amplifier can have input mostly isolated from output in low frequencies. However, if we consider the Miller capacitance *CGD*, we will have one more current component for the nodal equations on 1 and 2:, which will add to both KCL before formulating .

**3 Tasks**

1. Construct the top-down functions to solve the generic ODE in the form of . The rank of the solution vector should be flexible. We will have larger rank to solve in Program Assignment 5. As we will perform only one-step methods in the following, you will create a general time stepping scheme of *xi+1 = xi + φh*. Different methods will call the corresponding increment function *φ*.
2. Perform a validation of your ODE solver by the test problem of , with the exact solution for *x(0)* = 2 as: . We will implement the three Euler methods (forward, backward, and trapezoidal) and the RK34 methods without time adaptation and with time adaptation. In RK34 time adaptation, try out different relative and absolute tolerance for your most efficient time stepping. Validate your results from the computation listed in Table 1 and 2 to roughly match |*εx*| in different methods. Notice that the number may not be exact, as we are using double precision in C++. In the SPICE language, this transient analysis is:

.TRAN x START=0s STOP=5s STEP=1s

1. For the circuits in Fig. 3, use *R1 = R2 = R3* = 10kΩ, and *C1 = C2* = 1pF. *V1(0) = V2(0)* = 0. The current source is described by Fig. 6 as a large-signal transient. You should simulate from 0ns to 100ns with 0.2ns and 1ns step size (500 and 100 steps for methods without adaptation). Print out *V1(t)* and *V2(t)* to be used in the plot program of your choice. The RC circuits will be like a low-pass filter, and the time constant given here is about 10ns. Compare the results from all five one-step methods.

.TRAN V1 V2 START=0s STOP=100ns STEP=0.2ns

*1ns*

*10ns*

**Fig. 6**. Transient *i(t)* for the circuits in Fig. 3.

*9ns*

*11ns*

*9ns*

*20ns*

*21ns*

*30ns*

*31ns*

*0.1mA*

1. For the circuits in Fig. 5(a), use *IS* = 5μA, *κ* = 0.7, and *Vth* = 1.5V for the EKV model. *VDD* = 5V. *RG = RL* = 10kΩ. *C1 = C2* = 1pF.  *V1(0) = V2(0)* = 2.5V. Use the same *iin(t)* as in Fig. 6, and simulate the same period. Print out *V1(t)* and *V2(t)* to be used in the plot program of your choice. The CS amplifier will amplify *ΔV1* to *ΔV2*, but *V2*(t) will be bounded between 0 and 5V (voltage undershoot and overshoot possible with *CCG*, which is however not included here). Compare the transient results from all five one-step methods.

**4 Execution**

* This project can be done by groups of 2 students, but each student needs to know how to run the program as it would be used in later assignments.
* I expect the time of your programming to be similar, but may be shorter than, Program Assignment 3.

**5 Due dates and grading**

* No proposal needed.
* Export your .cpp, .h, and short report with output to be contained in one zip file, and send them by email before 4/30 5pm.

**6. Some comments in SPICE linearization for forming ODE**

In SPICE version 2 and before, the circuits are linearized before “integration” (the increment function accumulates the time steps to *x*, and therefore is equivalent to integration). When the circuits are linear, we can see that the nodal analysis will assemble to the conductance matrix as in the circuits of Fig. 3. If the circuits are linearized, we can view the capacitance as a current source in parallel with a resistance by the following transformation:

; 

An integration method needs to be chosen here. The trapezoidal rule is used as an example:

;



Although this is a convenient view, the linear circuits depend on the numerical scheme, which makes the implementation of different discretizations more difficult. Later SPICE has changed to more generic ODE solution hierarchy.