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Analysis of Continuous Class-F Mode in Load Modulated Back-off

*Abstract*—This paper presents a novel reformulation of continuous Class-F (CCF) mode by including non-linear I-V knee interaction on transistor’s drain waveforms. Load-pull emulation based on this theory is performed across α spaces, resulting into 20% drain efficiency (DE) difference at 8dB output back-off (OPBO) between α=0 and α=-1/+1 where it is at the peak. Fundamental load-pull simulation and measurement on 10W GaN HEMT device with sweep phase of 2nd harmonic impedances show similar trend, although DE at 8dB OPBO is 40% lower at α=0 compared to α=-1/+1. Maximum DE measured at 7.6dB OPBO for α=-1 is 83.5% while it drops to 45.3% at 8dB OPBO for α=0 This theory is implemented for designing broadband 10W power amplifier (PA) by restricting phase of 2nd harmonic impedances around α=-1 across bandwidth. The PA achieved 73% DE measured using CW signal on 50Ω termination at 2.0 GHz. Fundamental load-pull is performed on this PA, resulting into maximum DE of >60% and >70% at 8dB and 6dB OPBO respectively.

*Index Terms*—GaN, waveform engineering, high-efficiency amplifiers, power amplifier (PAs)

# INTRODUCTION

P

OWER amplifiers (PA) are the main energy consumed in RF communication systems where DC power supply is used to convert small RF input signal into a larger signal with certain gain. Future communication systems are becoming more complex, thus, PA designers are looking to improve the performances by maximizing the efficiency while operating it with good linearity within broadband frequencies.

Several techniques have been proposed to design high efficiency PA by means of harmonic tuning [1]-[4]. More recently, a generic trends of connecting waveforms theory into PA design such as continuous class-F (CCF) and continuous class B/J have been preferred by many designers as it offers both high efficiency and broadband performances [5]-[12]. From the original ideal class-F mode in [1] and [3], the voltage waveform of this mode is expanded using CCF mode operator,

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resulting into new sets of voltage waveforms. These waveforms engineering techniques leads to a new design space that has a theoretical constant high output power (Pout) and drain efficiency (DE) [5]-[7].

Although the efficiency and bandwidth of PAs have been maximized through waveform engineering and harmonics tuning techniques, however, the maximum performances can only be obtained when the PA is operated at its peak power. Current modulated signal that is used for mobile communication using LTE standards has peak-to-average-ratio (PAPR) of signal output about 7.6 dB. A high PAPR leads to a lower average efficiency performance compared to peak efficiency measured in CW tests. To put this into comparison, PAs in [8], [9] and [12] has a peak DE up to 83.4% measured with CW tests, however the average efficiency has been reduced to 29-48% under LTE signal.

Several design techniques have been described in [3] and [4] to improve back-off efficiency using different PA architecture that has been recently popular to encounter high PAPR signal in recent 4G and future 5G communication. Some of these original PA architectures in favors are Doherty, envelope tracking and outphasing amplifier. In outphasing amplifier [13]-[15], 2 identical PAs are connected and load-pulling each other through a combiner. A trajectory of impedances is presented at the devices through different phase of input signal applied, creating a load modulation. The combiner is designed such that it moves the load modulation trajectory impedances between optimum Pout and DE impedances. In order to achieve maximum DE at high output back-off (OPBO), the optimum Pout and DE impedances from single transistor must be separated apart.

In this paper, a new approach of emulating load-pull for CCF mode to obtained optimum Pout and DE impedances is presented. In Section II, an ideal CCF mode is reformulated to generate power and efficiency contours through Pedro’s load line model [16] and [17]. The previous work in [12], has introduced I-V knee scaling on CCF mode, resulting into symmetrical performances across α space. This work is then used to further improvise Pedro’s linear knee model to generate Pout and DE contours by including operational knee behavior. In Section III, verification of the new theory is performed through simulation and experimental characterization on single packaged GaN device. Section IV shows the design of broadband PA using the proposed theory and finally Section V drawn the conclusion.

# C:\Users\SYED\OneDrive - Cardiff University\PhD\MATLAB\IdealCCFWaveform.pngGenerating Power and Efficiency Contours for CCF Mode

## Ideal CCF Mode

The initial ideal drain voltage waveform of Class-F mode [1] -[4] in (1) is multiplied with the continuous operator (1 – α Cos()) [5]-[7] giving an ideal expanded voltage waveform for CCF mode in (2). The additional α term in (2) gives new set of drain voltage waveform that are only valid for range of α between -1 to +1 to keep the waveform above zero to obey the device’s physics.

Ideal voltage waveform for class F mode:

Ideal voltage waveform for CCF mode:

Meanwhile, the drain current waveform is a half rectified sinusoidal shape shown in (3). Both (2) and (3) represents ideal CCF mode, in which the minimums of the waveforms are at zero, neglecting the operational knee voltage [3], [12], and [18]-[21]. For plotting the current and voltage waveforms, values of a 10W GaN Wolfspeed packaged device, CGH40010F, are utilized with the Vdc and Imax values of 28V and 2.33A, respectively. Both ideal drain voltage and current waveform for CCF mode are shown in Fig. 1. The voltage waveform varied with different values of α while the current waveform is fixed. Constant output power and drain efficiency is theoretically achieved across α space as investigated in [5]-[7]. These performances depend on the number of harmonics contain in the waveforms.

## Using Pedro’s Linear Knee Load-line Method

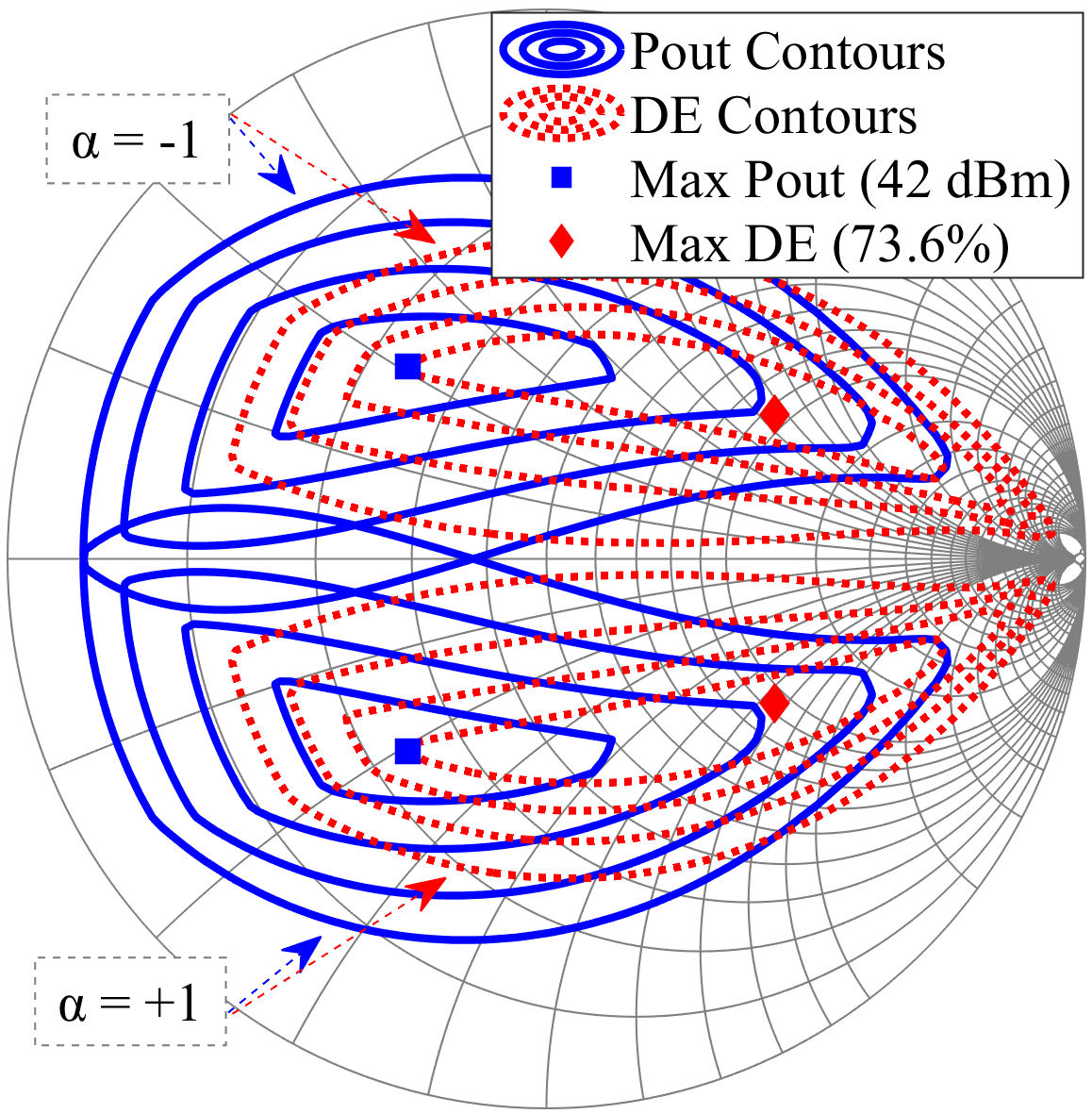
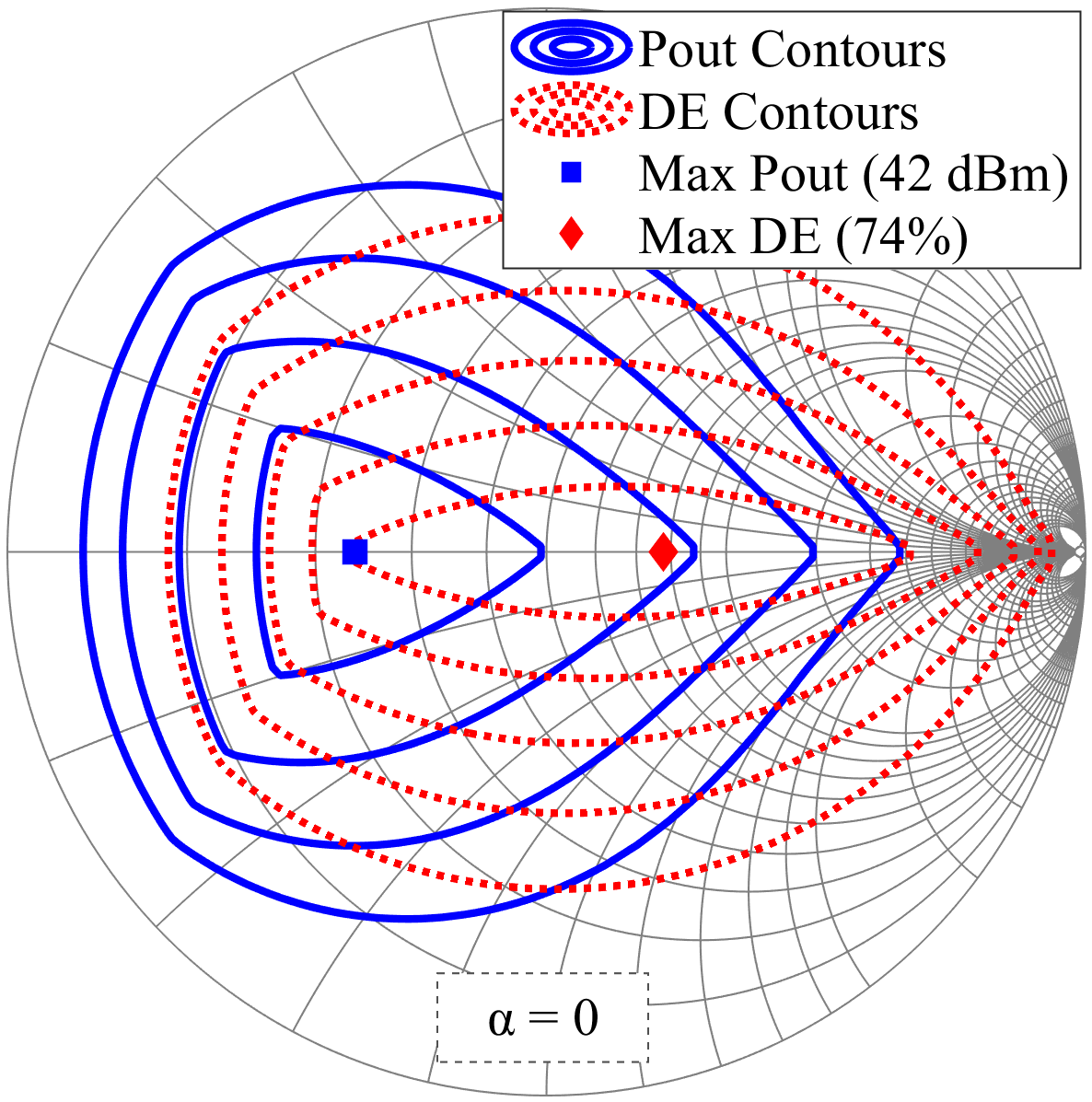
The optimum fundamental impedances for CCF mode based on the ideal waveforms can only be predicted at single impedances for each α values. In recent publication, the transistor has 2 optima; power and efficiency [16], [17] and [21]. An evaluation using Pedro’s load-line method [16]-[17] is used to generates power and efficiency contours for CCF mode. This method includes the soft turn-on region of the device’s knee region to extend the original load-pull method proposed using Cripps load-line theory [3] that able to predict the optimum output power but poor prediction on the optimum efficiency. Instead of zero knee voltage in (2), the drain voltage waveform is modified into (4) to emulate the drain voltage behavior within the knee region. The knee voltage from the 10W device is approximately 8V to be used in this evaluation and by default values, the minimum of the drain voltage waveform in (4) is equal to the knee voltage. Load pull

Fig. 1. Ideal drain waveforms for CCF mode.

emulation is performed by varying the magnitude and phase of the fundamental component of the voltage waveform in (4). For each of the voltage waveforms evaluated, the drain current waveform in (3) is evaluated with respect to the minimum of the drain voltage waveform. These changes apply to the maximum current, Imax that depends on the minimum of voltage waveform, Vmin as simplified in 5(a) and 5(b).

Fig. 2(a) and 2(b) shows the resulting fundamental load-pull contours for α=0 and α =-1/+1 case respectively using the linear knee model analysis. Pout contours are in steps of 2 dB while DE contours are in steps of 10%. Two optimum impedances are obtained at both maximum Pout and DE. The advantage of using Pedro’s linear knee load-line model enable the prediction of separation between power and efficiency optima for CCF mode through waveforms engineering only. Back-off efficiency is improved due to the separation between optimum impedances of Pout and DE. Fig. 3 shows optimum Pout and DE impedances and DE at 8dB OPBO impedances for all computed values of α. These performances, as summarized in Fig. 7, showing the maximum Pout and DE from the load-pull emulation computed using this method are constant across α ranges, which is contradicted to the performances obtained in [12], which obtained symmetrical maximum DE across α values. Meanwhile, DE at 8dB BO varies between 61% to 65%, showing less significant changes over α values.

(a) (b)



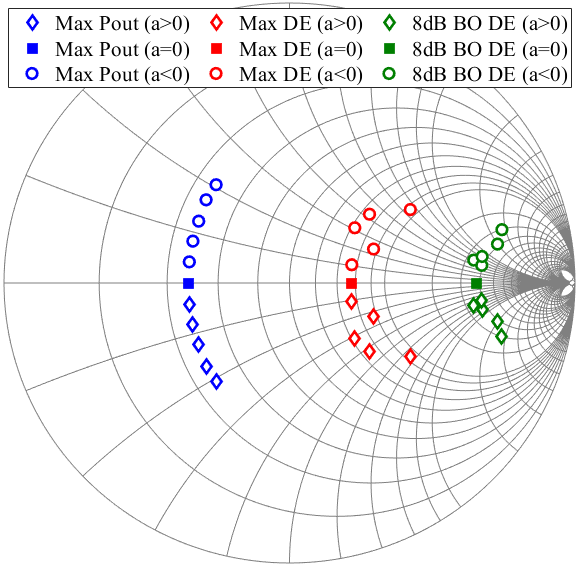
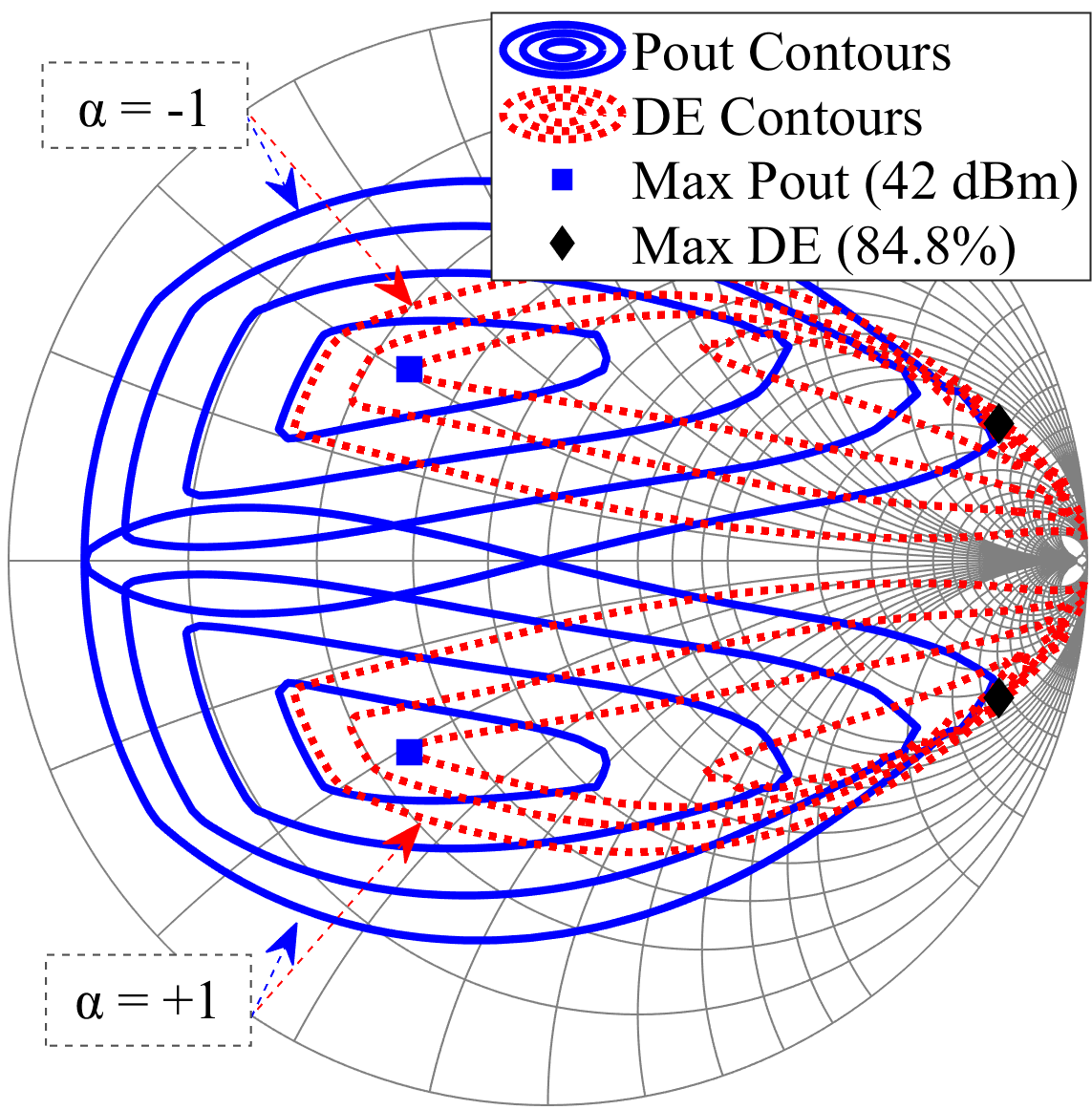
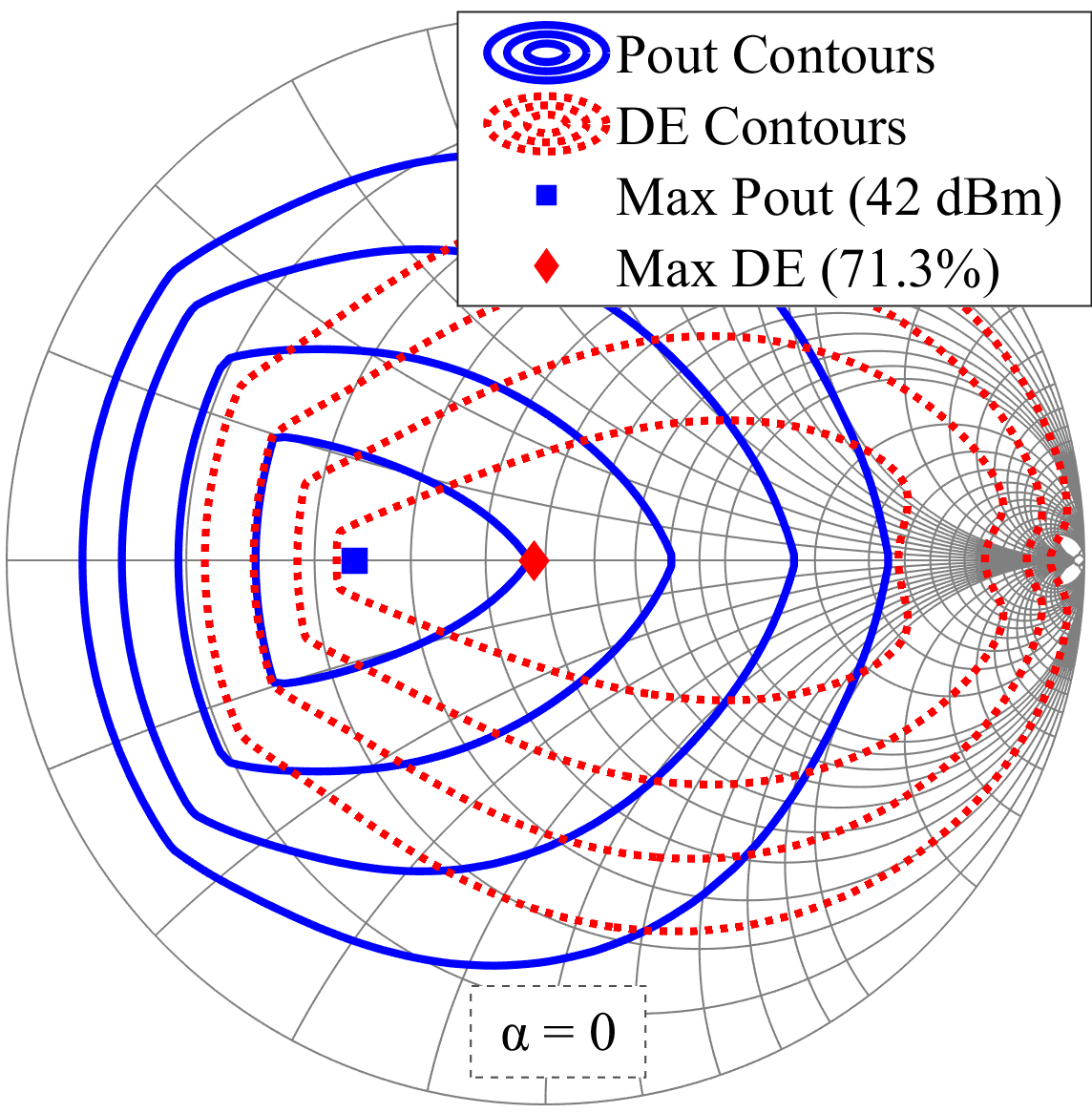
Fig. 2. Pout and DE contours from linear knee model.

Fig. 3. Optimum Pout, DE and DE at 8dB OPBO impedances from load-pull of CCF mode using linear knee model for -1 ≤ α ≤ +1.

## Using Non-linear Knee Load-line Model

While the analysis of CCF mode using Pedro’s linear knee load-line method in previous section enables the prediction of separation between optimum Pout and DE contours computed using load-pull emulation, however, the maximum of these two parameters across α ranges are almost constant in contrast to recent finding in [12]. A non-linear scaling of current waveform is introduced based on the clipping from the drain voltage waveform and knee voltage [3]. The general I-V knee scaling on the drain current waveform is simplified in (6) [3]. A modification in (6) is made for the load-pull emulation by inserting the drain voltage waveforms generated in previous section into (7a). The constant Vknee in (6) is modified so that it is a function of minimum of voltage waveform as shown in (7b).

(a) (b)



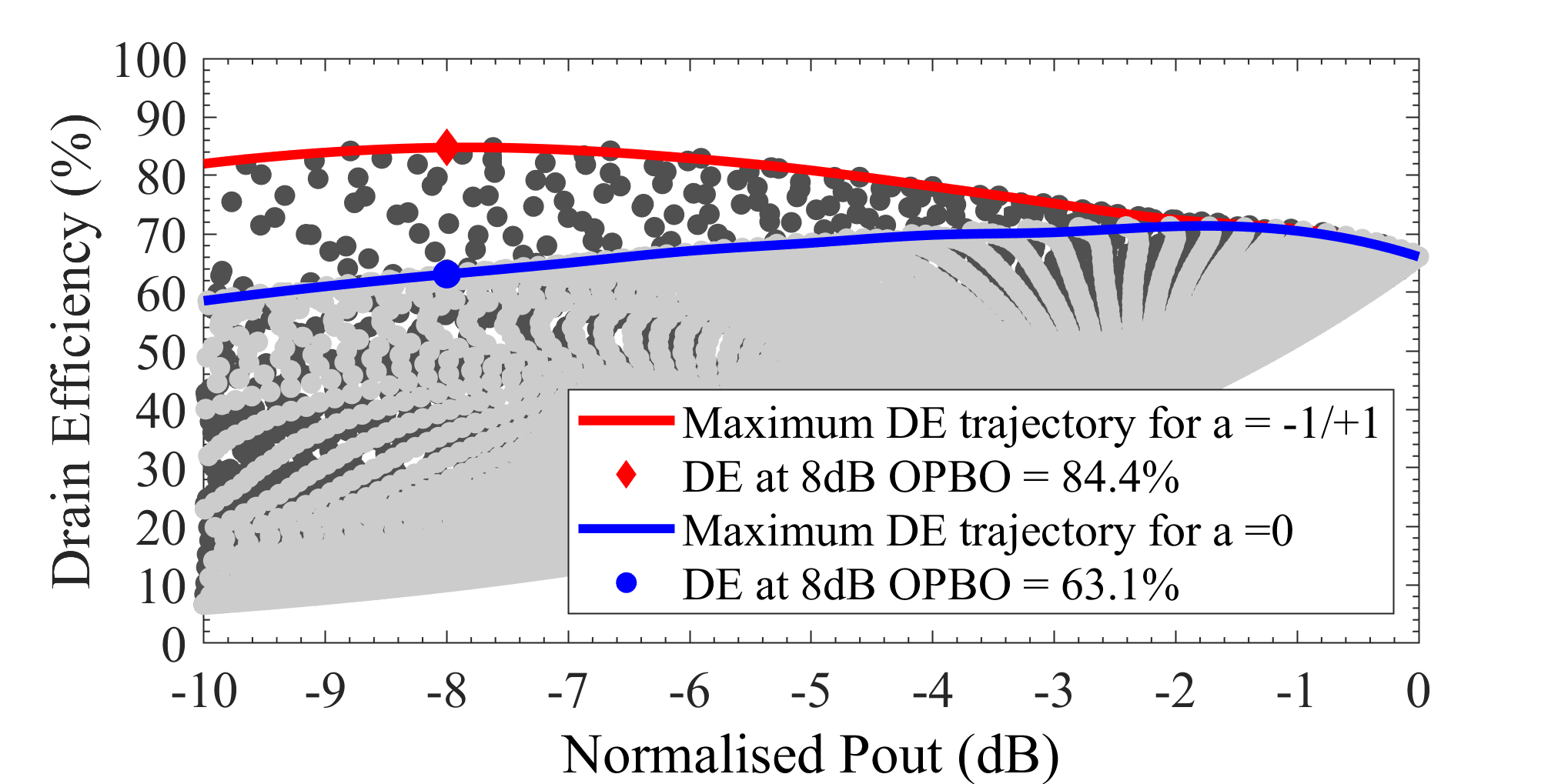
 Fig. 4. Pout and DE contours from non-linear knee model.

Fig. 5. DE vs Pout from fundamental load-pull using non-linear knee model for α =0 and α = -1/+1. Higher DE at 8 dB OPBO is obtained for α = -1/+1.

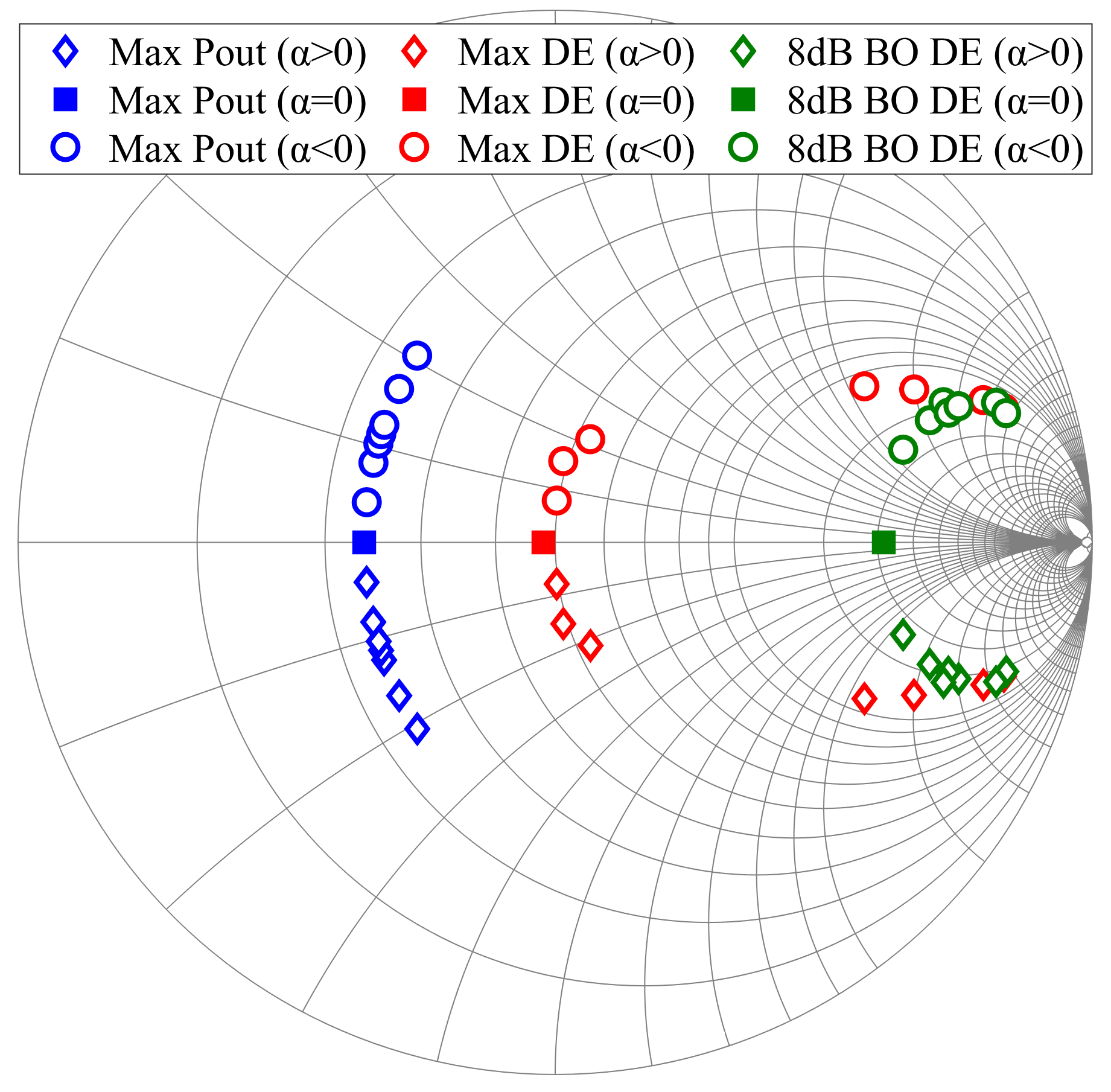
The contours generated from the load pull emulation of CCF mode using this non-linear knee model are shown in Fig. 4. The optimum Pout ant DE for α=0 in Fig. 4(a) shows a closer impedances separation compared in Fig. 2(a). In contrast, the separation between optimum Pout and DE impedances for α =-1 and +1 in Fig. 4(b) are larger than a=0 case. This indicates that the back-off efficiencies are much higher for α=-1/+1 compared to α=0, as shown in Fig. 5. The efficiency at 8dB OPBO are 20% higher at α=-1/+1 compared to α =0. A higher efficiency at 8dB OPBO is obtained for these values of α because these impedances are the same as the max DE impedances, shown in Fig. 6.

Fig. 7 shows the comparisons for max Pout, DE and DE at 8dB OPBO between emulation of CCF mode using linear knee and non-linear knee model. A symmetrical max DE are obtained as investigated in [12], with the lowest max DE of 71.3% calculated at α=0 and increases to 84.8% at α =-1/+1. The efficiency at 8dB OPBO also varied symmetrically with the lowest value of 63.1% obtained at α=0. This efficiency increases as α value decreases or increases to -1 and +1 respectively, peaking at 84.4% at α=-1/+1.

# Experimental Verifications

## Simulation

The new reformulation of CCF mode theory presented in previous section is verified through GaN HEMT device (10W CGH40010) simulation using available non-linear device model from Wolfspeed. The simulation is set up as follows. The device is biased with 28 V at drain and deep Class-AB (10mA) at the gate with frequency of operation of 915 MHz. Load



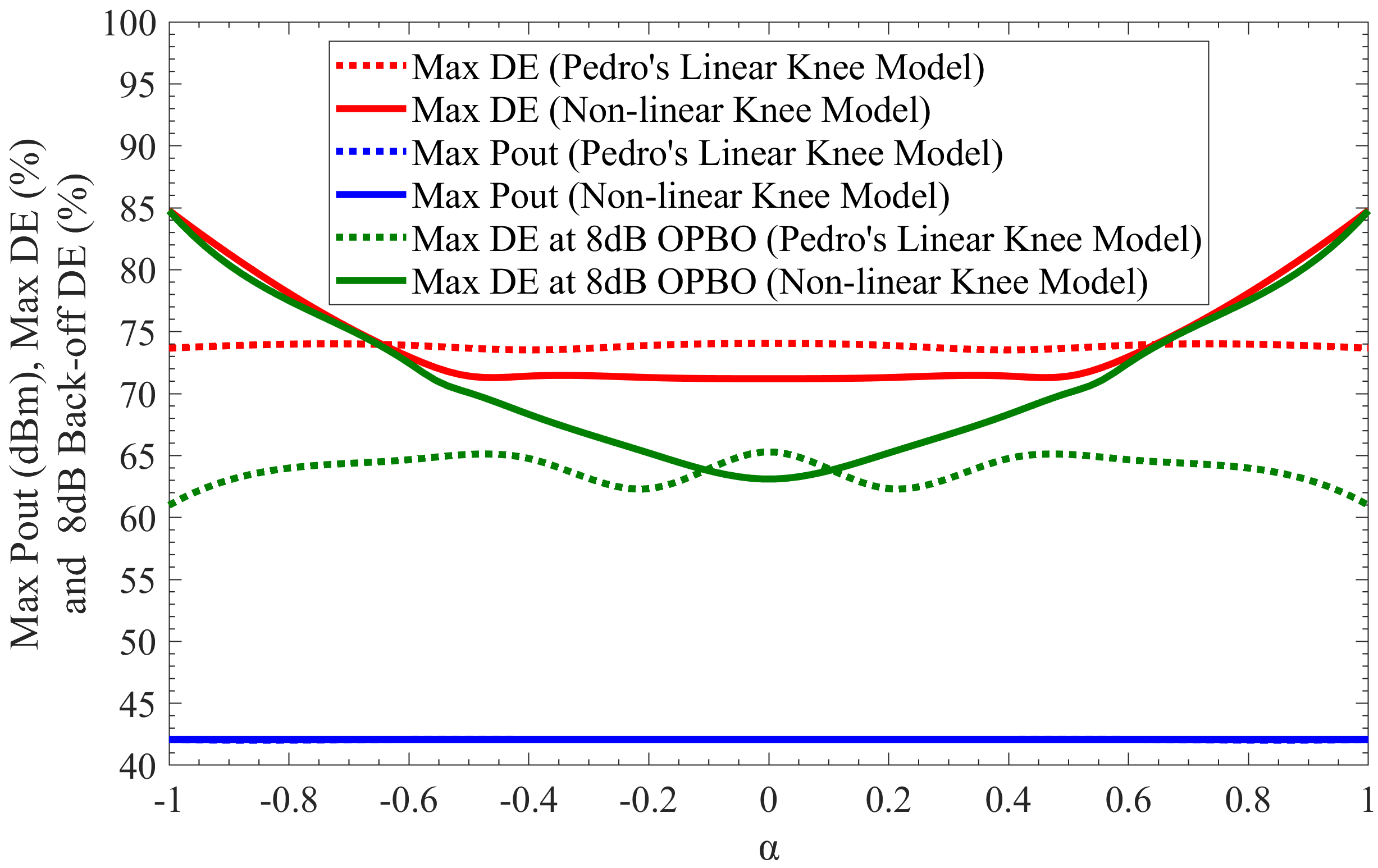
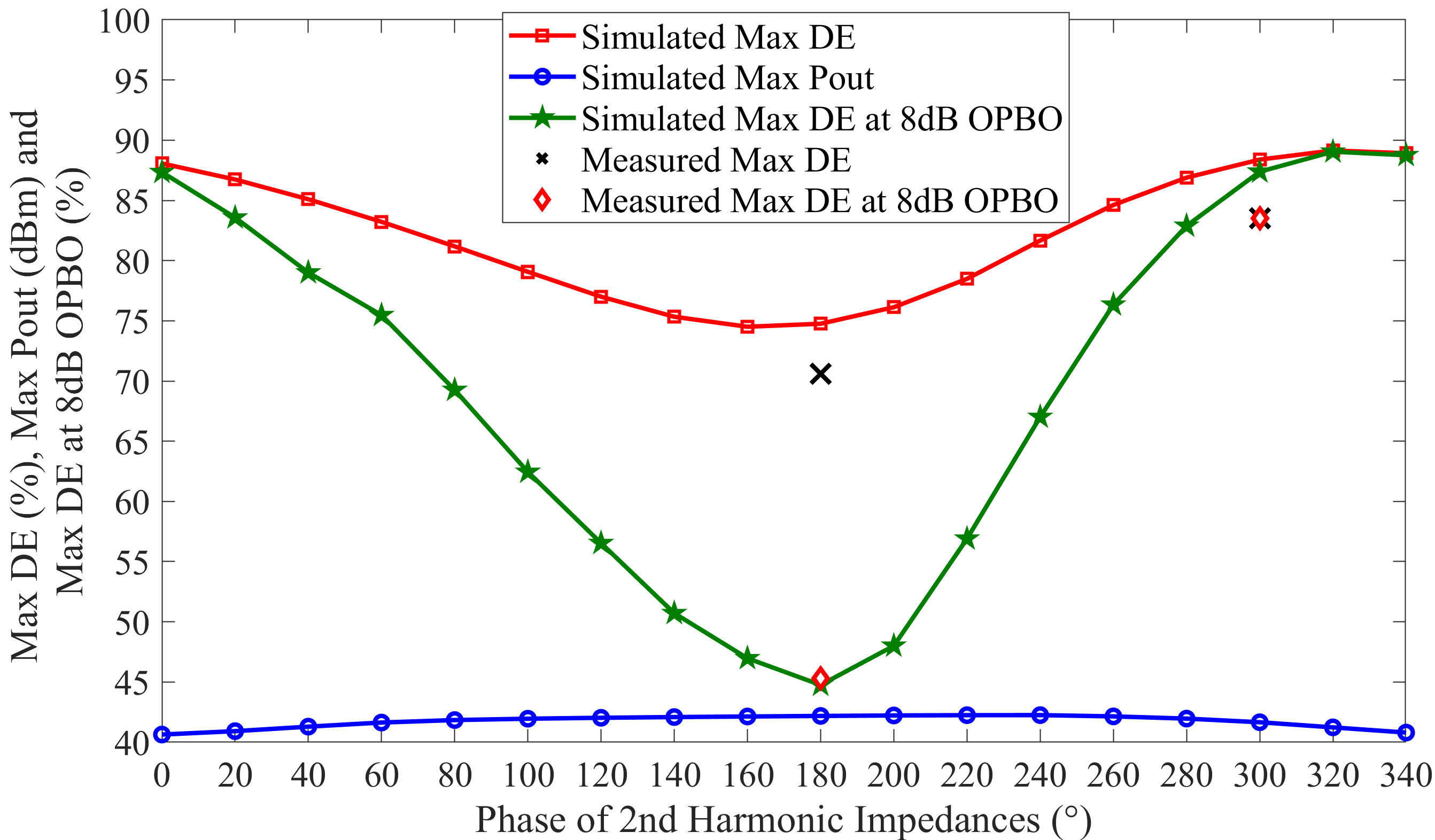
Fig. 6. Optimum Pout, DE and max DE at 8dB OPBO impedances from load-pull of CCF mode using non-linear knee model for -1 ≤ α ≤ +1.

Fig. 7. Comparisons for max Pout, DE and DE at 8dB OPBO from load-pull emulation of CCF mode using Pedro’s linear knee (dotted lines) and non-linear knee (solid lines) model.

plane by de-embedding the device’s output parasitic. Fundamental load pull is performed while sweeping phase of 2nd harmonic impedances along the edge of Smith Chart. The input power from signal generator is set to 26 dBm with 50Ω characteristic impedance.

Fig. 8 shows the max Pout, DE and DE at 8dB OPBO impedances from the fundamental load pull for various phase of 2nd harmonic impedances. The 2nd harmonic impedance is shorted at 180° phase, indicating that the device is operating in Class-F mode. The optimum impedances for both Pout and DE are closed to the real axis of the Smith Chart. The separation between the optimum Pout and DE also closer when 2nd harmonic impedance is shorted, similar to previous emulation for α=0. This separation increases as the phase of 2nd harmonic is moved further from short to open circuit, either through capacitive or inductive region.

Fig. 9 shows the performances obtained from the load-pull simulation of 10W device for full range of 2nd harmonic impedances rotation along Smith Chart. Both max DE and DE at 8dB OPBO varies symmetrically with the lowest value obtained when 2nd harmonic is shorted as expected from previous emulation. Max DE varies from 74.5% to 89.1% while max DE at 8dB OPBO varies from 44.7% to 89% at different phase of 2nd harmonic impedances setting. However, the back-off efficiency is simulated lower than in previous calculation for α=0 case, indicating that the separation between optimum

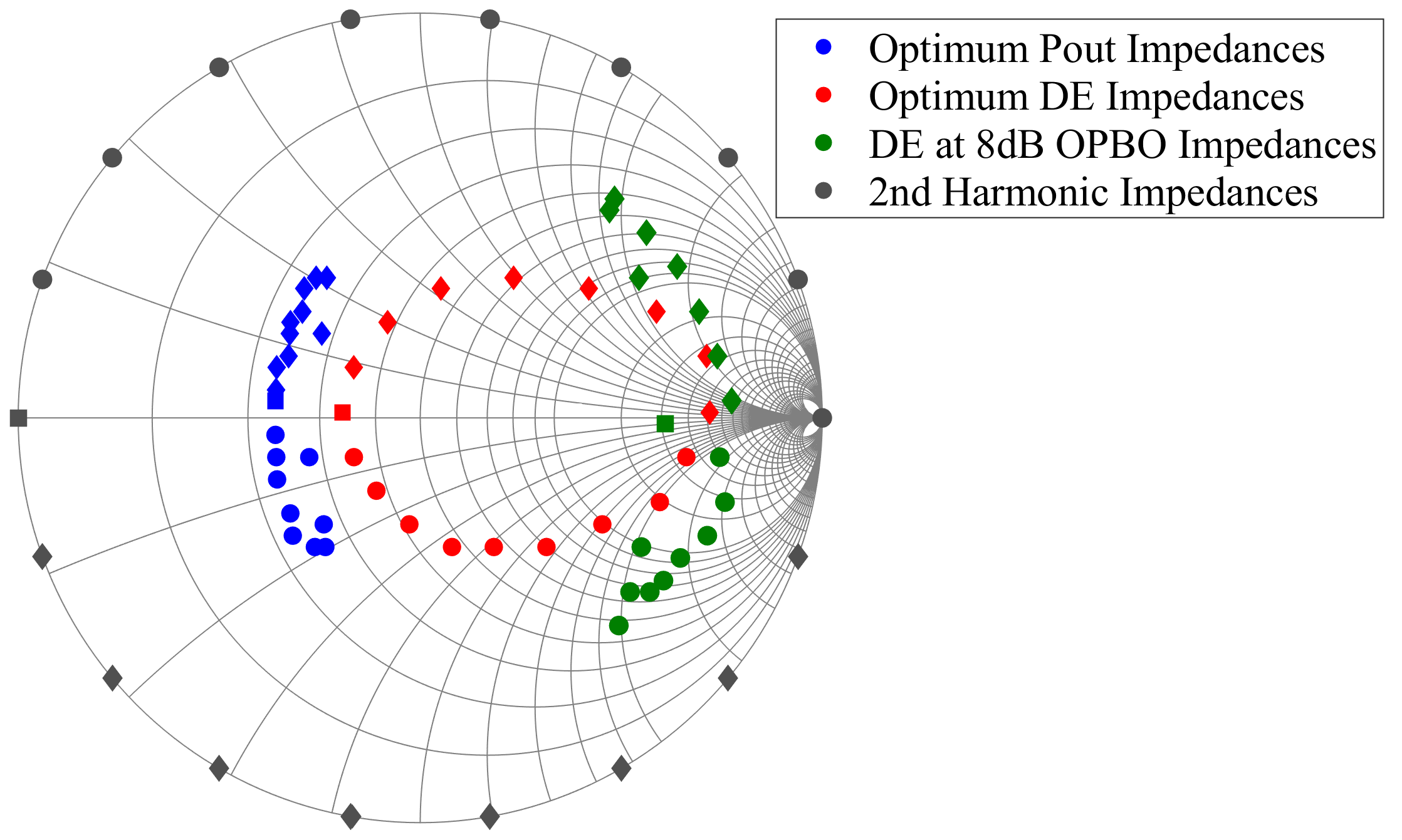


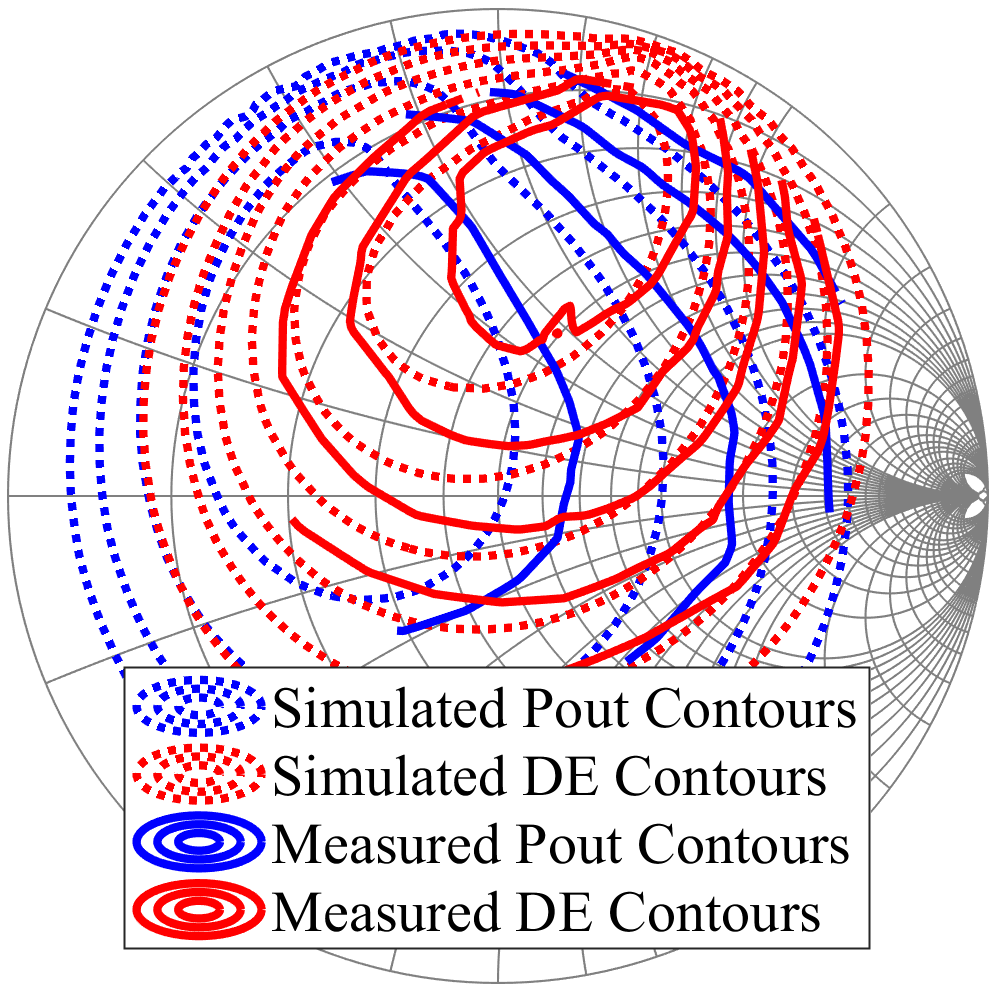
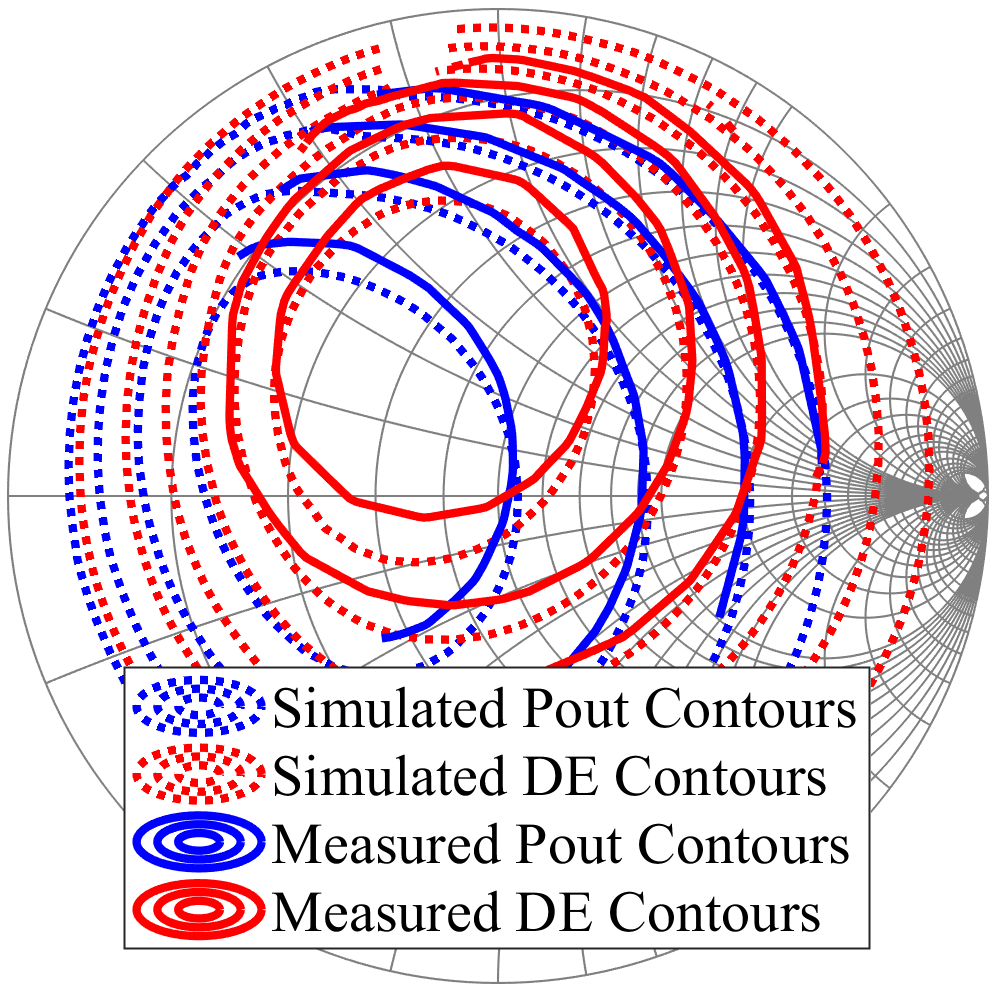
Fig. 8. Simulated max DE, Pout and DE at 8dB OPBO impedances from fundamental load-pull with sweep phase of 2nd harmonic impedances presented on device’s current generator plane.

Fig. 9. Simulated max DE, Pout at DE at 8dB OPBO from fundamental load-pull with different phase of 2nd harmonic impedances termination on device’s current generator plane.

Pout and DE is closer when actual device model is used. DE at 8dB OPBO increases almost symmetrically when 2nd harmonic impedance is moved closer to open circuit, reaching almost similar value to the max DE. On the other hand, the max Pout stays relatively constant above 40.6 dBm across all sweep phase of 2nd harmonic impedances.

## Load-pull Measurement

The same device is measured using active load-pull system on a test fixture with the same bias and frequency of operation. Two signal generators are used at the device’s output to generate fundamental impedances while controlling the 2nd harmonic impedances. Another signal generator is used as a source signal that is connected through a driver amplifier into the device’s input to generate constant input power available to the device (25.5 dBm) to drive the device up to 3 dB compression at optimum Pout impedance. Bias tees are used for both input and output of the device to provide isolation for RF signal into the DC supply while blocking DC into input and output RF signal generator. Two couplers are used at both test set’s input and output terminal to measure the input and output’s impedances and power level using a PNA. The test set is de-embedded to present the fundamental and load impedances at the device’s package plane. As this measurement is not de-embedded to the device’s current generator plane, the required phase of 2nd harmonic impedances are shifted from the   
 (a) (b)



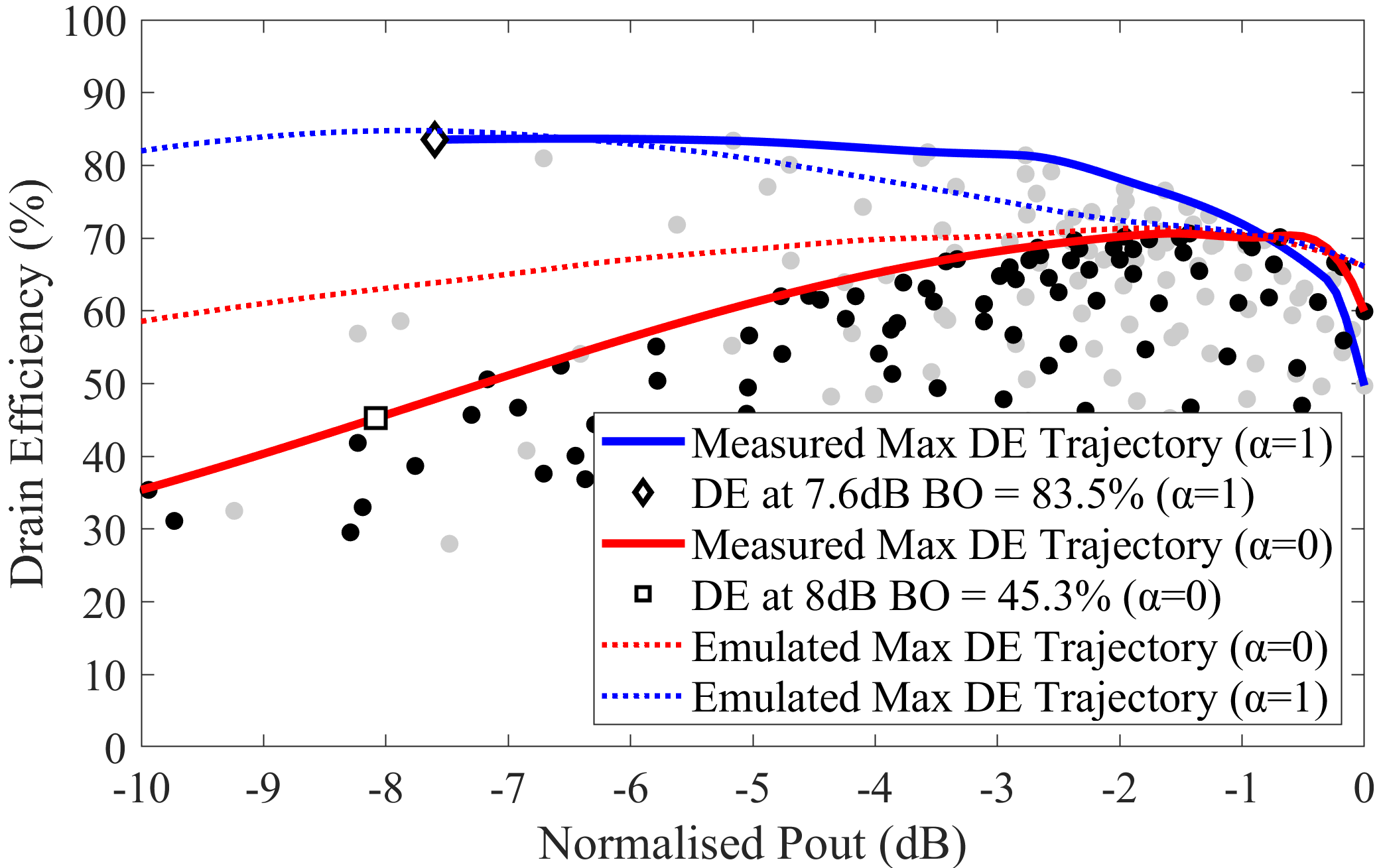
Fig. 10. Simulated and measured Pout and DE contours for (a) α = 0 and (b)   
α = -1.

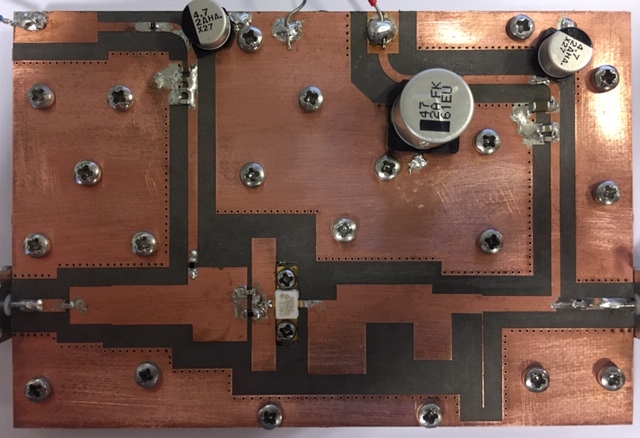
Fig. 11. Measured max DE trajectory for α = 0 and -1.

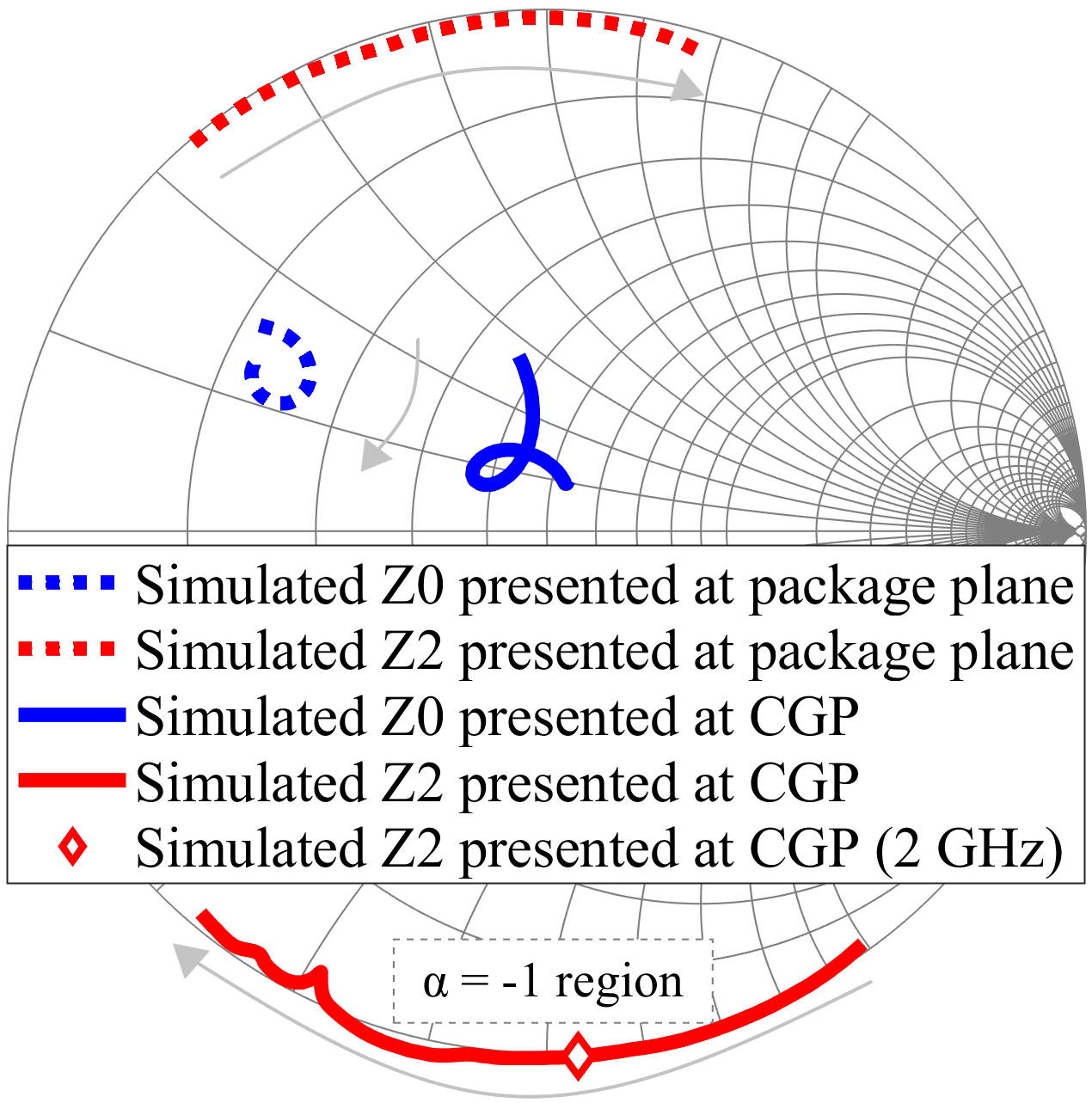
previous simulation. By using the available device’s model, it is found that the phase of 2nd harmonic impedances needed to present α=0 at the device’s package plane is 200°, that is equal to presenting short circuit at CGP. Meanwhile, phase of 2nd harmonic impedance needed for α=-1 at device’s package plane is 40°. Fundamental load-pull measurements are performed on the device by setting the magnitude of 2nd harmonic impedance to 0.98 while the phases are set to the aforementioned values.

Fig. 10 shows comparison of Pout and DE contours between measurement and simulation for 2 cases of α values. Optimum Pout and DE contours are much closer for α=0 while it largely separated for α=-1. Fig.11 shows the max DE trajectory between the 2 measured case obtained when DE is plotted against normalized Pout. Max DE measured for α=0 is up to 70.6% while the value increased by 13% to 83.5% for α=-1. Maximum DE at 8dB OPBO measured for α=0 is 45.3% while the value increased by almost 40% for α=-1 at 7.6 dB OPBO. Although the max DE at 8dB OPBO for α=0 is significantly lower than the emulated calculation result, however, the measured value corresponds well with the device simulation.

# Design of Broadband PA with Restricted 2nd Harmonic Phase Rotation

New theoretical and experimental analysis of CCF mode in the previous section shows that the peak efficiencies at max Pout and OPBO are reached for α=-1/+1 when it is operated in the non-linear knee region. Therefore, limiting the α space to maintain the high efficiencies at max Pout and OPBO is an attractive design approach. A similar 10W GaN device (CG2H40010F) is used to a design broadband PA by exploiting



Fig. 12. Fabricated 10W broadband GaN (CG2H40010F) PA circuit

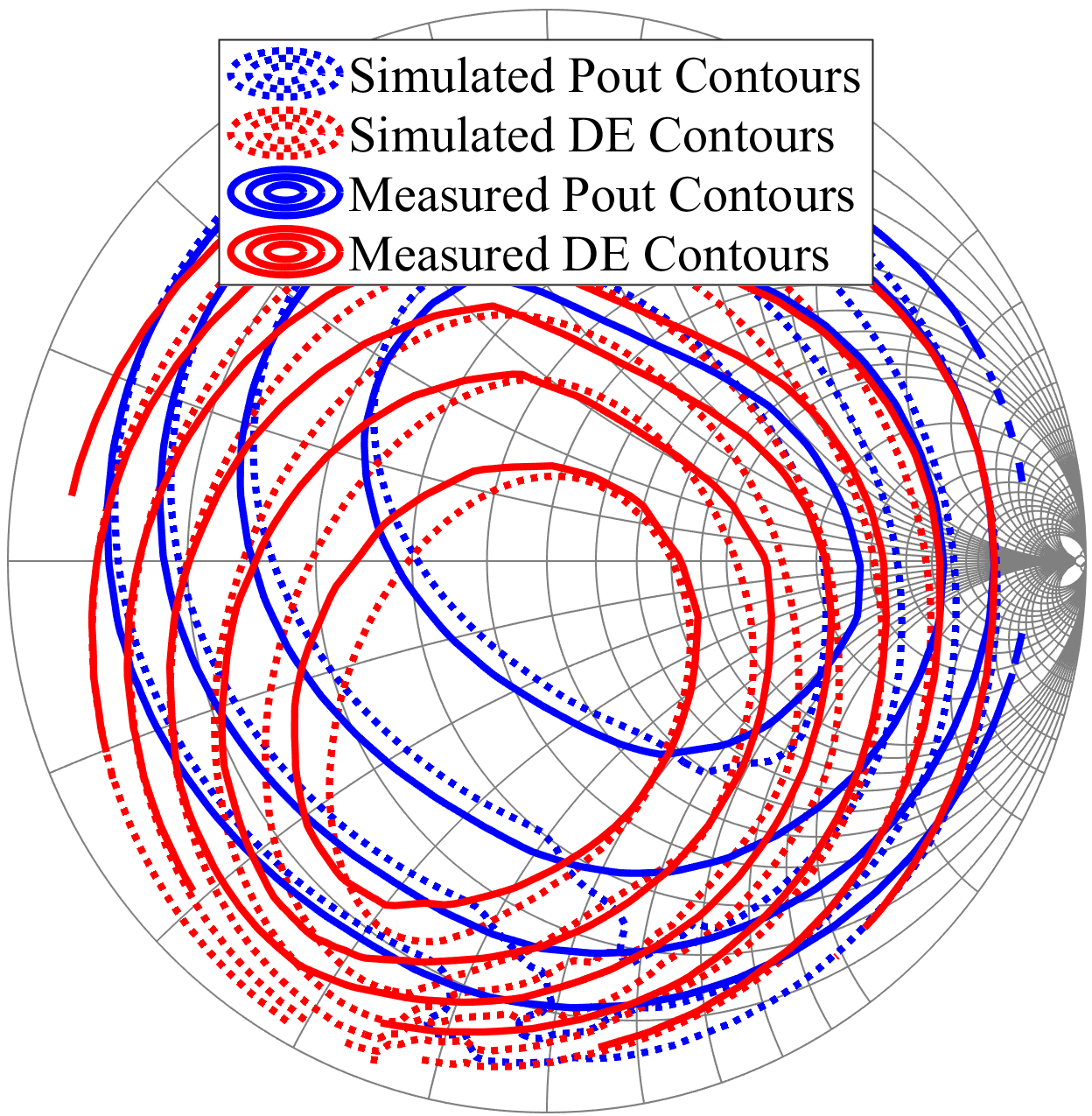
Fig. 13. Simulated impedances presented at the device across bandwidth.

Fig. 14. Simulated and measured Pout and DE contours from load-pulling 10W PA at 2.0 GHz

CCF mode with a restricted 2nd harmonic impedance rotation to keep the efficiencies high. Fig. 12 shows the fabricated PA circuit layout. The design of this circuit focuses on controlling the fundamental and 2nd harmonic impedances to be within the optimum α=-1 throughout the bandwidth. Fig. 13 shows the simulated fundamental (1.7-2.7 GHz) and 2nd harmonic impedances (3.4-5.4 GHz) presented at the package and current generator plane of the device. The impedances at CGP are obtained from available voltage and current nodes at the intrinsic plane provided within the device’s model. The rotation of 2nd harmonic impedances at CGP are within α=-1 across design bandwidth.

The PA is biased with 28V at the drain and -3V at the gate, drawing 10mA current. A CW measurement is performed on the PA at 2.0 GHz and the max Pout obtained at 3dB

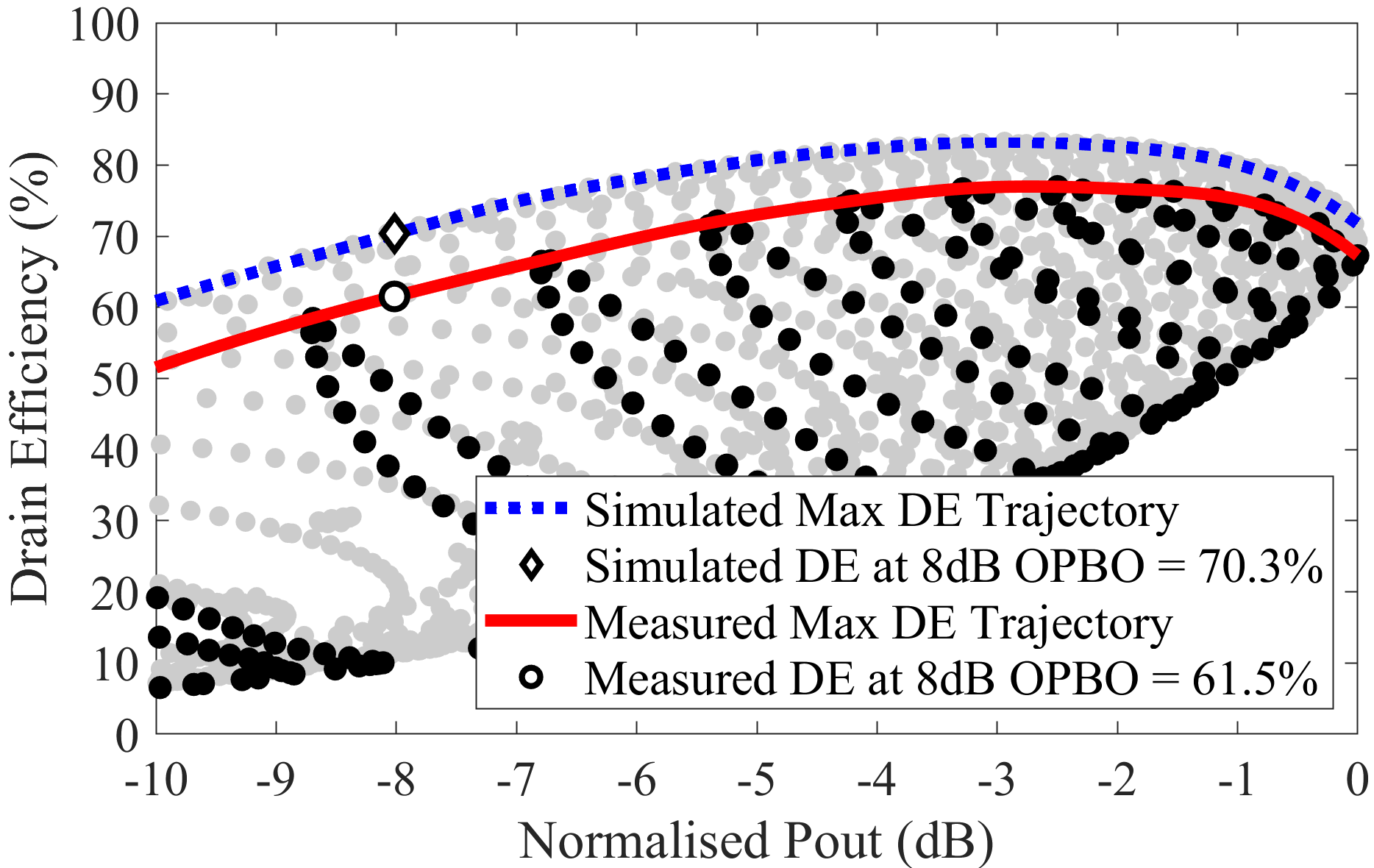


Fig. 15. Simulated and measured max DE trajectory from load-pulling 10W PA at 2.0 GHz

compression is 15.6W with 73.4% DE. Next, the input power at these performances is fixed while fundamental load-pull measurement is performed at the 50Ω load using an active load-pull system. In Fig. 13, the termination of 2nd harmonic impedance in the output matching network at 2GHz is closed to α=-1 region, resulting into large separation between Pout and DE contours from the load-pull measurement shown in Fig. 14. A comparison is made between simulation and measurement result by keeping the max Pout at the same value. Fig. 15 shows comparison of the max DE trajectory between simulation and measurement. Interestingly, the measured efficiency performances are less than simulated values, that is 9% less at 8dB OPBO. This is due to power losses within the PA circuit, which is found to be approximately -0.3dB. Nevertheless, the measured max DE is >60% and >70% at 8dB and 6dB OPBO.

# Conclusion

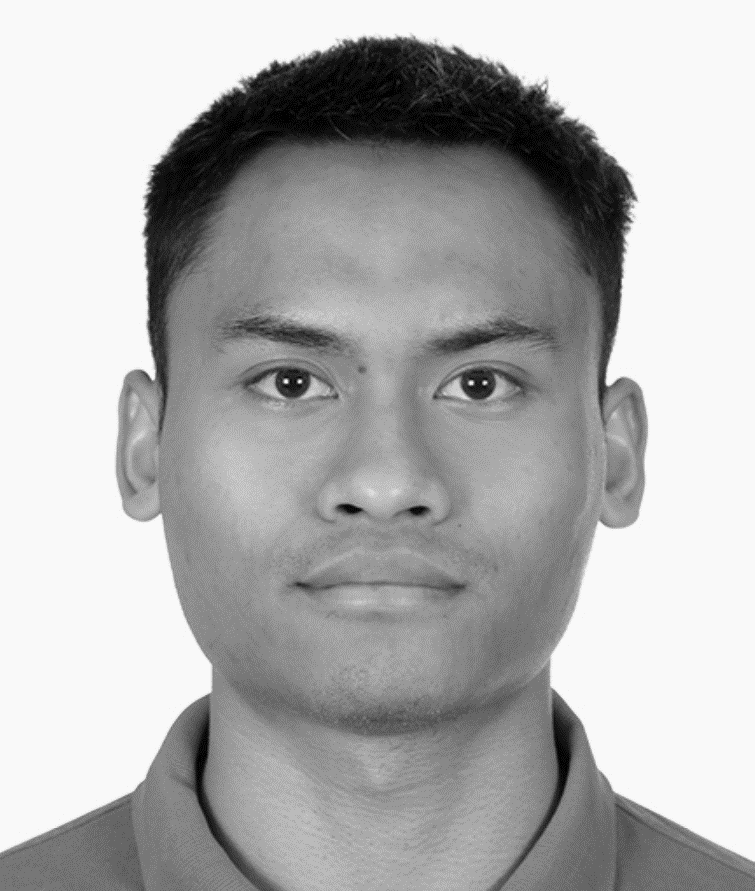
New reformulation of CCF mode shows a significant improvement of device’s performances by including non-linear I-V knee relationship to the waveform theory. Optimum Pout and DE impedances are closer together for α=0 showing poor DE at OPBO. In contrast, these impedances are largely separated for α=-1/+1 resulting into improvement of max DE at OPBO. The similarities between the emulation using waveform theory and device simulation and measurement have been verified, showing a good agreement. It has been demonstrated that a broadband single stage PA with restricted 2nd harmonic impedance rotation within α=-1 resulted into high DE at OPBO. This design theory is useful for PA designer to design high efficiency PA using Doherty or outphasing architecture by specifically tuning the harmonic terminations.

Acknowledgements

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References

1. F. H. Raab, “Maximum efficiency and output of class-F power amplifiers, *IEEE Trans. Microw. Theory Techn.*, vol. 49, no. 6, pp. 1162–1166, June 2001.
2. P. Colantonio, F. Giannini, E. Limiti, and V. Teppati, “An approach to harmonic load– and source–pull measurements for high-efficiency PA design,” *IEEE Trans. Microw. Theory Techn.*, vol. 52, no. 1, pp. 191–198, Jan. 2004.
3. S. C. Cripps, *RF Power Amplifier for Wireless Communication*, 2nd ed. Norwood, MA: Artech House, 2006.
4. P. Colantonio, F. Giannini, and E. Limiti, *High Efficiency RF and Microwave Solid State Power Amplifiers*, London, U.K.: Wiley, 2009.
5. S. C. Cripps, P. J. Tasker, A. L. Clarke, J. Lees, and J. Benedikt, “On the continuity of high efficiency modes in linear RF power amplifiers,” *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 10, pp. 665–667, Oct. 2009.
6. V. Carrubba, A. L. Clarke, M. Akmal, J. Lees, J. Benedikt, P. J. Tasker, and S. C. Cripps, “On the extension of the continuous class-F mode power amplifier,” *IEEE Trans Microw. Theory and Tech*., vol. 59, no. 5, pp. 1294-1303, May 2011.
7. V. Carrubba, J. Lees, J. Benedikt, P. J. Tasker, S. C. Cripps, “A novel highly efficient broadband continuous class-F RFPA delivering 74% average efficiency for an octave bandwidth*,*” *IEEE MTT-S Int. Microw. Symp. Dig.*, pp. 1-4, June 2-10, 2011.
8. N. Tuffy, L. Guan, A. Zhu, and T. J. Brazil, “A simplified broadband design methodology for linearized high-efficiency continuous class-F power amplifiers,” *IEEE Trans. on Microw. Theory and Tech.*, vol. 60, no.6, pp. 1952-1963, June 2012.
9. K. Chen and D. Peroulis, “Design of broadband highly efficient harmonic-tuned power amplifier using in-band continuous class-F-1/F mode transferring,” *IEEE Trans Microw. Theory Tech.*, vol. 60, no. 12, pp. 4107-4116, Dec. 2012.
10. J. Chen, S. He, F. You, R. Tong, and R. Peng, “Design of broadband high-efficiency power amplifiers based on a series of continuous modes,” *IEEE Microw. Comp. Lett.*, vol. 24, no. 9, pp. 631-633, Sep. 2014.
11. S. Saxena, K. Rawatt, and P. Roblin, “Continuous class-B/J power amplifier using a nonlinear embedding technique,” *IEEE Trans. on Circuits and Systems*, vol. 64, no. 7. Pp. 837-841, Nov. 2016.
12. S. M. H. Syed Anera, T. Husseini, S. Alsahali, J. J. Bell, R. Quaglia, M. Kermalli, P. J. Tasker and J. Benedikt, “High-efficiency broadband PA design based on continuous class-F mode with compression,” to be published in *IEEE MTT-S* *Int. Microw. Symp. 2019*, June 2019.
13. K. Mimis, G. T. Watkins, A. Yamaoka, and K. Yamaguchi, “Output harmonic optimisation of dynamically load modulated power amplifiers,” in *Proc. Eur. Microw. Conf.*, Oct. 2016, pp. 1071–1074.
14. P. E. de Falco, K. Mimis, G. T. Watkins, A. Yamaoka and K. Yamaguchi, “Load modulation of harmonically tuned amplifiers and application to outphasing systems,” Trans. Microw. Theory Techn., vol. 65, no. 10, pp. 3596–3612, Oct 2017.
15. P. E. de Falco, K. Mimis, S. Ben-Smida, K. Morris, G. Watkins, A. Yamaoka and K. Yamaguchi, “Single-ended branch PA characterisation for outphasing amplifiers,” in *Proc. Eur. Microw. Integrated Circuit Conf.*, Sept. 2018, pp. 178–181.
16. J. C. Pedro, L C. Nunes, and P. M. Cabral, “A simple method to estimate the output power and efficiency load-pull contours of class-B power amplifiers,” *IEEE Trans. on Microw. Theory and Tech.*, vol. 63, no. 4, pp.1239-1249, April 2015.
17. X. Du, C. J. You, X. Li, M. Helaoui, J. Cai and F. M. Ghannouchi, “Evaluation of knee voltage effect and soft turn-on characteristic on the load modulated continuous class-B/J power amplifier,” IEEE MTT-S Int. Wireless Symp., May 6-10, 2018.
18. F. You and J. Benedikt, “An optimized-load-impedance calculation and mining method based on I-V curves: using broadband class-E power amplifier as example,” *IEEE Trans on Industrial Electronics*, vol. 66, no. 7, pp. 5254-5263, July 2019.
19. R. Quaglia, D. J. Shepphard, and S. Cripps, “A reappraisal of optimum output matching conditions in microwave power transistors,” *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 3, pp. 838–845, Mar. 2017.
20. R. Quaglia, J. J. Bell, S. C. Cripps, “New general formulation and experimental verification of harmonic clipping contours in high frequency high power devices,” *IEEE Trans Microw. Theory and Tech.*, vol. 65, no. 10, pp. 3903-3909, Oct. 2017.
21. A. Bogusz, Z. Costello, R. Quaglia, J. Bell, J. Lees, P. Tasker and S. Cripps, “Power and efficiency continuous modes in saturated GaN HEMT devices,” in *Int. Workshop on Integrated Nonlinear Microwave and Millimeter-wave Circuits*, July 2018.

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