4-Bit Asynchronous Up Counter using Mixed Signal

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***Abstract*—Asynchronous counters have recently gained popularity due to their low power consumption and low noise emissions. Furthermore, they are used as frequency dividers, as divide-by-N counters. This project involves the design of a 4-bit asynchronous up counter using eSim and Ngspice tools. Specifically, it focuses on the development of a mixed signal circuit for a 4-bit asynchronous up counter. There are T flip-flops, a ring oscillator, an Analog to Digital Converter (ADC), and a Digital to Analog Converter (DAC) in the circuit. This design uses Verilog for the T flip-flops and Sky130 components for the ring oscillator.**

I. Circuit Details

A 4-bit Asynchronous up counter contains four T flip-flops (digital block) and a ring oscillator (analog block) as shown in Figure 1. It counts from 0 to 2^4-1, i.e. 15. All flip-flops have their T-input connected to 1. In each flip-flop, the output changes asynchronously on the negative edges of its clocks. In the first T flip-flop, the clock signal is directly applied, which is the output of the ring oscillator signal converted to digital by ADC. When the clock signal is on a negative edge, the output of the first T flip-flop toggles. A second T flip-flop is controlled by the output of the first T flip-flop. Thus, every negative edge of the output of the first T flip-flop toggles the output of the second T flip-flop. In the same way, the third and fourth T flip-flops toggle for every negative edge of clock of the second and third T flip-flops, respectively.

II. Circuit Design

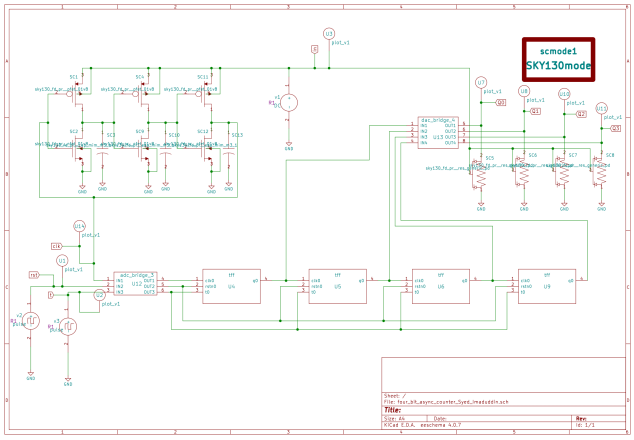

Fig. 1. Schematic of 4-bit asynchronous up counter in eSim

III. Circuit Waveform

In the case of T flip-flops, assume the initial status from rightmost to leftmost is $Q_3Q_2Q_1Q_0$=0000. Here, Q_3 & Q_0 are MSB & LSB respectively. In Figure 2, we can see the output waveforms of Q_0, Q_1, Q_2, and Q_3, and the working of the 4-bit asynchronous up counter is described in Table I.

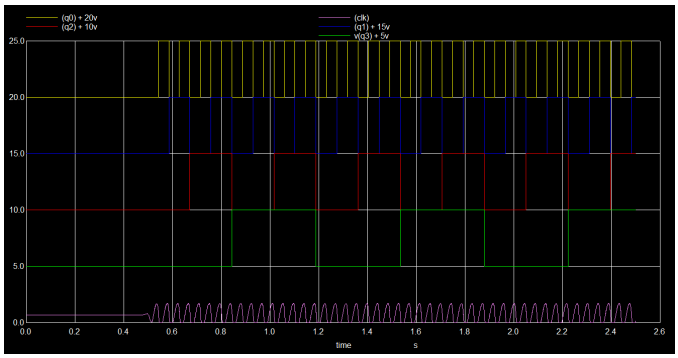

Fig. 2. Output waveforms of Q_0, Q_1, Q_2, and Q_3 in Ngspice

TABLE I
Working of 4-bit asynchronous up counter

No of negative edge of Clock	Q_0 (LSB)	Q_1	Q_2	Q_3 (MSB)
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1
16	0	0	0	0

References

[1] Digital Electronics: 4 Bit Asynchronous Up Counter, Neso Academy, https://www.youtube.com/watch?v=eEeBh8jfDjg
[2] Cadence Tutorial for Ring Oscillator with Parametric sweep, GoldLighT Technologies Pvt. Ltd., https://youtu.be/t5emusIwI70