CDA-5106 Assignment 1

2.8 Latency on a row buffer miss = 13+13+13 = 39ns

2.9 Latency on a row buffer hit = 13ns

2.10 Since the controller is occupied with only tRP, tRCD and CL, utilization = 4/39

2.11 utilization = (transfer_time*number_of_banks)/(latency)

$1 = 4*a/39$

$a = 39/4$

$a \sim 10$

2.12 $0.5 = 4*a/39$

$a = (50*39)/(100*4)$

$a \sim 5$

2.13 Let T_i be the number of the thread. Then,

$Latency(T_1) = 1*39$ ns

$Latency(T_2) = 2*39 + 4$ns

$Latency(T_3) = 3*39 + 2*4$ns

$Latency(T_4) = 4*39 + 3*4$ns

Average latency = Total Latency/Number of threads

$= 414/4$

$= 103.5$ns

If the bank supports 4 banks, then each of the thread's request can execute in parallel in which case the latency will be equal to 39ns (as calculated in 2.8).

2.14 Growing the number of banks reduces the latency observed by allowing multiple request to execute in parallel. However, doing so increases the complexity of the circuit and the power consumption as well. The complexity is increased because addressing the banks requires greater number of bits in the address bus.