QubiC 2.0: An Extensible Open-Source Qubit Control System Capable of Mid-Circuit Measurement and Feed-Forward

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Abstract—**Researchers manipulate and measure quantum processing units via the classical electronics control system. We developed an open-source FPGA-based quantum bit control system called QubiC for superconducting qubits. After a few years of qubit calibration and testing experience on QubiC 1.0, we recognized the need for mid-circuit measurements and feed-forward capabilities to implement advanced quantum algorithms effectively. Moreover, following the development of RFSoC technology, we upgraded the QubiC system to QubiC 2.0 on an Xilinx ZCU216 evaluation board and developed all these enriched features. The system uses portable FPGA gateware with a simplified processor to handle commands on-the-fly. For design simplicity and straightforward scaling, we adopted a multi-core distributed architecture, assigning one processor core per qubit. The actual pulses combine the unique pulse envelope and carrier information specified in a command. Each pulse envelope is pre-stored on FPGA's block RAMs, ensuring the speed and reusability during the whole quantum circuit. The pulse parameters including amplitude, phase, and frequency can be updated from pulse to pulse. The software stack is developed in Python, running on both the FPGA's ARM core and host computer via XML-RPC. The quantum circuit can be described in a high-level language, which supports programming at both the pulse-level and native-gate level, and includes high-level control flow constructs. The QubiC software stack compiles these quantum programs into binary commands that can be loaded into the FPGA. With Qubic 2.0, we successfully achieved multi-FPGA synchronization in bench tests and demonstrated simplified feed-forward experiments on conditional circuits. The enhanced QubiC system represents a significant step forward in quantum computing, providing researchers with powerful tools to explore and implement advanced quantum algorithms and applications.**

I. INTRODUCTION

Quantum computing is a revolutionary field of computing that leverages the principles of quantum mechanics to process information in ways unimaginable by classical computers [1]. By utilizing the quantum bit (qubit), which can exist in multiple states simultaneously, quantum computers have the potential to solve complex problems exponentially faster than classical computers [2]. In recent years, the quantum computing sparked the development of groundbreaking advances in science [3], [4]. Quantum control, the ability to manipulate and steer quantum systems with precision, lies at the heart of quantum technology advancements [5], [6]. The field of quantum control has witnessed remarkable progress in recent years [7]–[10], driven by a deep understanding of quantum mechanics, novel control techniques, and advancements in experimental capabilities.

As quantum information processors continue to advance, with increasing quantum bit count and complexity, ensuring synchronization among multiple devices becomes crucial for scaling up the system effectively [11]. Additionally, the potential to utilize mid-circuit measurement with qubit reset is key to reusing qubits and condensing larger circuits to operate efficiently on smaller quantum devices [12], [13]. Mid-circuit measurement plays a important role in quantum error correction, where repeated measurements on ancilla qubits are required [14], [15]. This raises the requirement for a control system to enable a single qubit to be measured at real-time during the execution of the circuit, and further multiple measurements in a circuit and at any point throughout the circuit.

Following the development of the new radio frequency system-on-chip (RFSoC) technique [16], we upgraded the QubiC system to QubiC 2.0, fulfilling the need for real-time computation and feedback [17]. This paper aims to provide an overview of the recent advances in QubiC 2.0 system and highlight the key methodologies and techniques that have emerged to manipulate and exploit quantum systems. We delve into the electronics hardware, field-programmable gate array (FPGA) gateware, and engineering software, synchronization design of QubiC 2.0, examining the strategies employed to achieve real-time control over qubits. Moreover, we highlight state-of-art fast control technique and the experimental advancements in mid-circuit measurement and feed-forward over the QubiC 2.0 system.

By exerting fast control over quantum systems, researchers and engineers can harness their unique properties for a wide range of applications, including quantum computing, quantum communication, and quantum sensing. As an extensible and open source toolbox for the quantum community, QubiC 2.0 is capable of accommodating users and developers from different layers to enable efficient co-design. Researchers can unlock the full potential of quantum technology, leading to groundbreaking applications and transformative advancements in quantum computing.

II. ELECTRONICS HARDWARE

The QubiC system, deployed on the ZCU216 platform, offers advanced radio frequency (RF) data processing and synchronization capabilities. With its high-speed digital-to-analog converter (DAC), analog-to-digital converter (ADC) channels, and multi-tile synchronization (MTS), the system provides a powerful and flexible solution for RF data manipulation and adaptive computing. Moreover, the integral design of the RFSoC makes the control extensibility cost affordable. The QubiC system on the ZCU216 platform represents a significant step towards efficient and seamless RF data processing in quantum computing, opening doors to run advanced real-time experiments on RFSoC system.

A. ZCU216

ZCU216 is an evaluation board featuring the Gen 3 ZU49DR Zynq UltraScale+ RFSoC, which provides 930 K system logic cells, 16-ch 14-bit RF-DAC @ 9.85 giga samples per second (GSPS) and 16-ch 14-bit RF-ADC @ 2.5 GSPS [18]. To accommodate ZCU216 to control and measure the qubits, the digital signal processing (DSP) frequency is set to be 500 MHz on ZCU216 in the QubiC system. The QubiC 2.0 system integrates a 16-channel 14-bit DAC capable of operating at a high-speed sampling rate of 8 GSPS, and a 2-channel 14-bit ADC with a sampling rate of 2 GSPS, enabling high-fidelity data acquisition. CLK104 RF clock add-on card is used for internal or external reference clocking, while a quad zSFP/zSFP+ connector is equipped on the ZCU216 board to accept zSFP/zSFP+ modules for data communication between boards. RFMC 2.0 interfaces are employed as the I/O expansion options for DAC and ADC analog front-end (AFE).

B. Analog Front-End

To fan out / collect signals to / from the fridge, we developed a customized analog front-end board for ZCU216, as shown in Fig. 1. This board features two RFMC 2.0 connectors, accommodating 16 DAC and 16 ADC channels respectively. A balun is incorporated to convert differential signals to single-ended and vice versa. To enhance signal quality, the board includes low-noise amplifiers to amplify the DAC signals. For power management, we employ switching pre-regulators to ensure power efficiency, while linear low-dropout (LDO) post-regulators provide low-noise power sources. Moreover, the analog front-end board shares the same physical size as the XM655 breakout add-on card that comes with the ZCU216 kit, making them compatible and interchangeable for enhanced flexibility and ease of integration.

III. FPGA GATEWARE

Fully open-source QubiC gateware provides the low level access to the researchers, and is capable of generating waveform form parameters, which leads to the benefit of pulse sequence reuse. The gateware is designed with low latency, and optimized to do the real-time control on FPGA for mid-circuit measurement and feed-forward. As shown in Fig. 2, the QubiC 2.0 FPGA gateware contains the a Python Productivity for
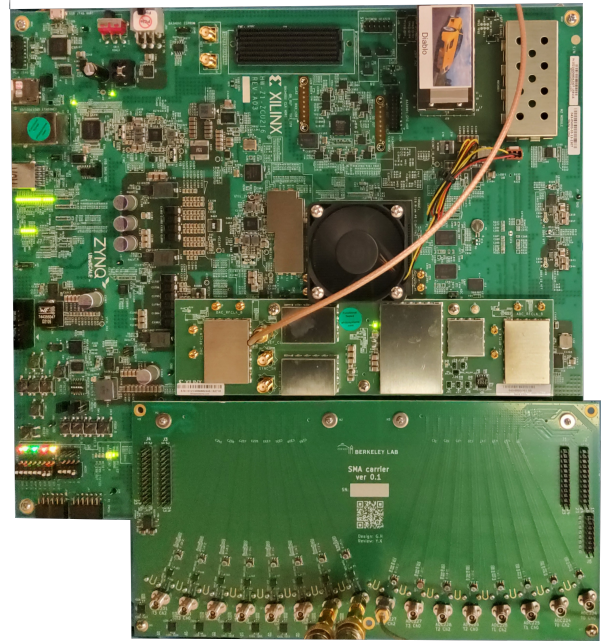

Fig. 1. Customized analog front-end board and Xilinx ZCU216 evaluation board.

Zynq (PYNQ) framework on Zynq, advanced extensible interface (AXI) interconnection, a customized intellectual property (IP) for programmable logic (PL) / processing system (PS) units, and RF data converter (RFDC). We will mainly discuss the board support package and the digital signal processing (DSP) in the section.

A. Board Support Package

QubiC 2.0 utilizes the PYNQ 3.0 framework [19] on Zynq UltraScale+ to deliver a user-friendly software platform and a suite of libraries for seamless development of embedded systems and reconfigurable computing applications. PYNQ streamlines the development process by providing an accessible programming interface and a comprehensive set of libraries tailored for RFSoC-based systems. Additionally, it offers a specialized overlay that allows users to effortlessly access and control the RF components, high-speed data converters, and FPGA fabric integrated within the RFSoC device.

The implementation of the advanced extensible interface (AXI), a communication bus protocol integrated on-chip, facilitates interconnection between the Zynq and essential components such as the RFDC, DSP register block, configuration register block, and block random-access memory (BRAM) control block.

The ZCU216 board integrates robust PS and PL units within a single device. QubiC 2.0 takes advantage of a parameterized IP tailored for the PL and PS, providing the flexibility to accommodate various application requirements effectively. The DSP registers, configuration registers, and BRAM control blocks are transported to the PLPS block through the local bus, ensuring efficient communication and data access.

As shown in Fig. 2, in the PLPS block, we integrate programmable logic, clock management / buffer, FPGA pin
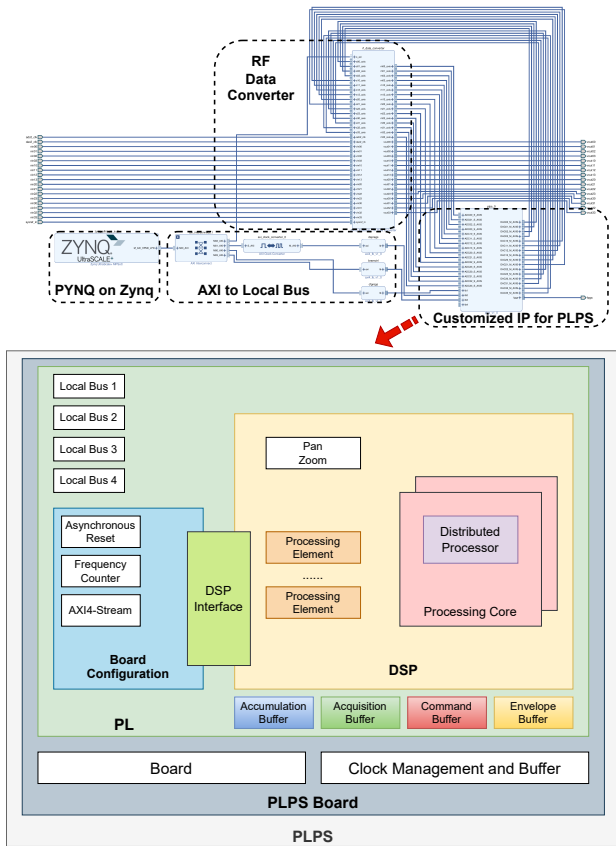
Fig. 2. QubiC gateware.

instantiation, and other hardware connectivity elements. To facilitate efficient communication between blocks, we employ SystemVerilog [20], leveraging its interface encapsulation capabilities. On the PL side, we utilize local buses, board configuration, and the DSP. Four local buses are instantiated here for the information exchange with AXI. The board configuration block comprises the AXI4-Stream interface, meticulously implemented for the data handshake between the DAC/ADC on AXI and the DSP block. Additionally, the board configuration block incorporates asynchronous reset logic to minimize latency and a frequency counter, essential for verifying the accuracy of clock frequency generation. The DSP interface serves as a bridge between the board configuration and the DSP block.

RF data converter is an Xilinx IP configured with multi-tile synchronization to enable high sampling rate DACs and ADCs. To cater to diverse quantum application needs, we offer various variations of RF data converters. These variations are carefully designed to strike a balance between qubit drive channels, readout data rate, and FPGA resources, ensuring optimal performance for different quantum computing scenarios.

B. Digital Signal Processing

The superconducting qubits are precisely controlled and measured using RF pulses, typically amplitude-modulated signals with parameterized frequency, initial phases, and predefined envelopes. To digitally generate the pulses, we employ complex multiplication of the carrier and the modulation envelope. Each qubit has its dedicated DAC channel, while the readout drive outputs are combined and directed to a single readout drive DAC, known as multiplexed readout.

The qubit readout signal from the fridge undergoes digitization by ADC. Next, it is mixed with a digital local oscillator, and the resulting signal is integrated during the duration of the readout pulse to obtain the IQ data. The accumulation process acts as a low-pass filter, down-converting the signal to the frequency of interest, and the filtered data is then stored in the corresponding buffer for subsequent qubit state discrimination.

There is a bank of soft-processor cores capable of parameterizing and triggering RF control/measurement pulses synthesized using direct digital synthesis (DDS)-based pulse generators on the FPGA gateware DSP. The cores are simple and lightweight, so each core is intended to only connect to a small number of signal generators. Since the processor is distributed in nature, with one core per arbitrary waveform generator (AWG), simplifying the design and allowing for straightforward scaling, we call it the distributed processor [21], as shown in Fig. 3. Feedback is implemented at the lowest level of the classical electronics to give highest bandwidth.

The distributed processor consists of a set of cores, along with interfaces for receiving processed quantum measurement results and synchronization among different cores. Each processor core executes a program consisting of timed pulse commands for its AWG(s), as well as instructions for implementing arbitrary control flow within the program (e.g. conditional branching) based on either external input or internal state. For the timed pulse commands, we largely use the same design as the existing QubiC command buffer [22]: a 72-bit command specifying pulse characteristics (such frequency, phase, length, and pointer to a buffer containing the envelope shape) is sent to the AWG at a specified time, referenced to an internal counter. To implement control flow instructions, we include a 16x 32-bit register bank along with an arithmetic logic unit (ALU) that implements comparisons, addition, and subtraction on signed 32-bit integers. ALU outputs can be used to write to registers, increment the time reference counter, and set the instruction pointer. In the current version of the processor (running at 500 MHz), pulse commands can execute in ≥ 4 clock cycles, and most register writes/control flow instructions execute in 4-7 clock cycles.

In each processor core, we include a function processor interface for connecting it to external computational resources. This external result could be a state-discriminated measurement, or a more complex computation, such as the output of a decoder for an error correction algorithm. The interface is triggered by a special instruction, which halts the execution inside the core until the result returns, at which point the data is either read into a register or used immediately as the input to a branch conditional.

A synchronization interface, along with a special instruction, is employed to allow for the internal time references from different cores to be synchronized. Once all of the cores referenced have reached the corresponding sync instruction, program execution within all cores is resumed, and each core's internal time reference is reset.
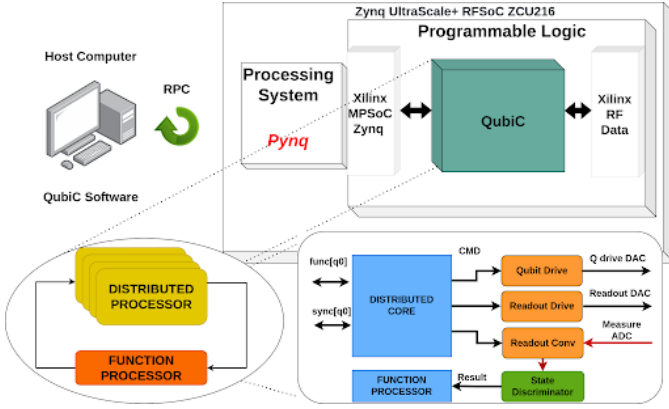
Fig. 3. QubiC architecture.

Fig. 4. QubiC software stack.

The processing elements play a pivotal role as up or down converters in the digital domain, efficiently bridging the DSP interface with the distributed processors. Within the DSP, we incorporate the command buffer and the envelope buffer to facilitate parameterized pulse generation. Furthermore, the accumulation buffer stores the accumulated values resulting from the integration of the baseband I/Q series over the corresponding digital local oscillator (DLO). Additionally, the acquisition buffer functions as a live oscilloscope, enabling real-time observation of the ADC/DLO/DAC raw data, enhancing the system's versatility and usability.

Notably, the QubiC 2.0 gateware DSP empowers the parameterized pulse generation feature. It enables the efficient reuse of sequences by updating waveform parameters through commands without the need for recompiling or resending all the waveform data. The pulse envelope is carefully optimized during the qubit gate calibration process and is stored in the FPGA memory as complex numbers, with each point containing in-phase and quadrature-phase terms. This stored pulse envelope can be conveniently reused by indexing the same address area, even if there are changes in the carrier frequency or phase. Running a quantum circuit on QubiC 2.0 is remarkably efficient as it loads only the required commands instead of the entire waveform data points, streamlining the computational process and maximizing system performance.

IV. ENGINEERING SOFTWARE

The low level toolchain contains the compiler and the assembler, as shown in Fig. 4. The input to the compiler is a high level program or circuit description as a sequence of gates and/or pulses together with high level control flow (e.g. if/else for branching) structures. The compiler converts this description into a custom intermediate representation (IR), then implements a series of passes to resolve gates into pulses, apply virtual phases, schedule pulses. After all IR passes are complete, the compiler generates a pulse level program for each distributed processor core. The current QubiC system uses a mapping of one core per qubit, but this configuration is arbitrary and can be specified as an option to the compiler. The assembler converts each pulse level program to program binaries for the distributed processor to execute on the FPGA.
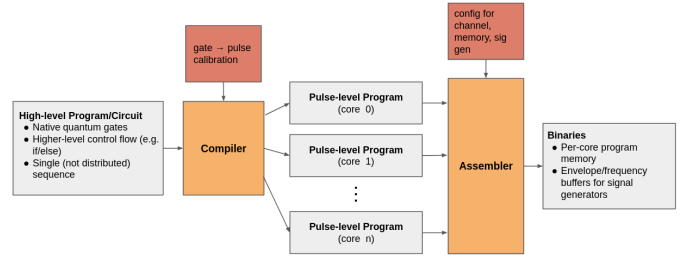
The hardware configuration for each channel is used in the assembling process to determine channel mapping and pulse-generator parameters.

The compiler and assembler can be executed either on the advanced RISC machines (ARM) core on the Zynq for the simple system configuration or on a host computer for the more advanced computational power compare to the embedded core. A simple XML-RPC is used for the host-embedded core communication. User can execute the code on a Jupyter Notebook hosted on the host computer, control and read the results by read and write the FPGA buffers.

V. SYNCHRONIZATION

The number of channels can easily exceed the capability of a single FPGA or RFSoC to handle, making synchronization among multiple devices vital for scaling up the system effectively. Regarding clock synchronization, the primary objective is to achieve precise phase alignment for all clock signals in each module. This ensures that the DAC and ADC signals are perfectly synchronized in phase, and the clock counter is accurately aligned [23].

A. Deterministic Clock Distribution

To achieve synchronization, the clock must be distributed to each node through matched-length cables, ensuring aligned and deterministic phase relationships. Nested dual phase-locked loop (PLL) in zero-delay mode (ZDM) is employed in LMK04828 of ZCU216 for deterministic clock distribution [24]. The PLLs' input and feedback frequencies are set to the greatest common divisor among all frequencies, and SYSREF serves as the feedback signal. It is essential to implement divider reset after the ZDM configuration, as this step is critical for the proper functioning of the clock synchronization system.

B. Multi-DAC Synchronization on Single FPGA

Multi-tile synchronization (MTS) is a vital feature to synchronize operation across multiple tiles, and facilitate seamless coordination and data transfer between different DAC and ADC elements [25]. To achieve deterministic latency, MTS utilizes an external SYSREF signal distributed to each device as a trigger, aligning frame and local multiple frame clocks to it. To perform MTS on ZCU216, the first step involves enabling all clocks and SYSREF generators, followed by SYSREF analog capture. Subsequently, the clock divider must be reset, and FIFO latency should be measured and adjusted
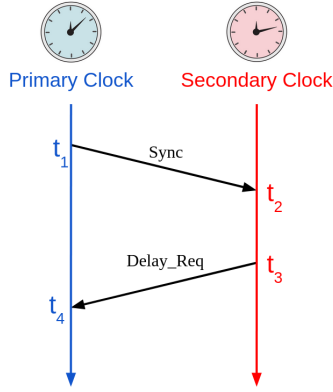
Fig. 5. Simplified precision time protocol.

Fig. 6. Multi-FPGA synchronization hardware.

accordingly. Finally, digital features are synchronized with SYSREF dynamic update events to complete the MTS setup.

C. Multi-FPGA Synchronization

To achieve multi-FPGA synchronization, the FPGAs should share an identical reference clock. Following the deterministic clock distribution process, we proceed to implement the simplified precision time protocol [26].

As illustrated in Fig. 5, to synchronize the primary and secondary clocks on two FPGAs, a *Sync* message is transmitted at t_1 in the primary clock domain, and the secondary FPGA receives it at t_2 in the secondary clock domain. Subsequently, the secondary FPGA responds with a *Delay_Req* message at t_3 in the secondary clock domain, and the primary FPGA receives it at t_4 in the primary clock domain. The transit time for the *Sync* message can be calculated as $delay = \frac{(t_4-t_1)-(t_3-t_2)}{2}$, while the constant offset between the primary and secondary clocks can be determined as $offset = \frac{(t_2-t_1)-(t_4-t_3)}{2}$. To synchronize the secondary clock with the primary clock, one can apply the offset correction in software, ensuring precise synchronization between the two clock domains.

D. Bench Test

We configured the multi-FPGA hardware setup, as depicted in Fig. 6, to conduct the bench test. With the synchronized clocks on the FPGAs, we measured the output RF signal noise using a signal source analyzer across multiple FPGAs. The signal root mean square (RMS) jitter @ 6.50 GHz on ZCU216 was measured to be 1.8 ps (integrating from 10 Hz to 100 MHz) and 7.4 ps (integrating from 0.1 Hz to 100 MHz), which effectively meets the requirements for quantum experiments.

VI. DEMONSTRATION ON QUBITS

A. Fast Reset

Fast reset is a technique utilized to swiftly and efficiently restore a quantum system to a well-defined initial state, commonly the ground state [27]. This process of resetting qubits plays a vital role in quantum computing, enabling researchers and engineers to prepare quantum states and execute quantum algorithms with greater efficiency. Conventional quantum reset
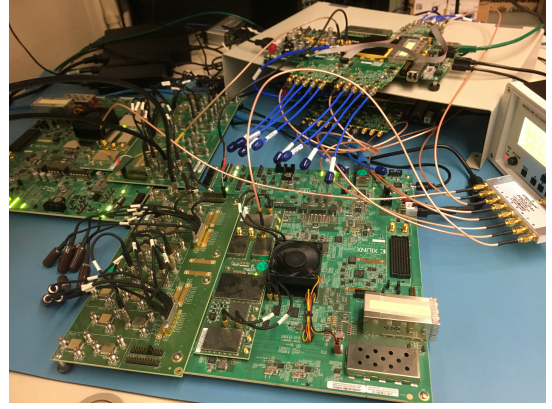

(a) Fast reset circuit.
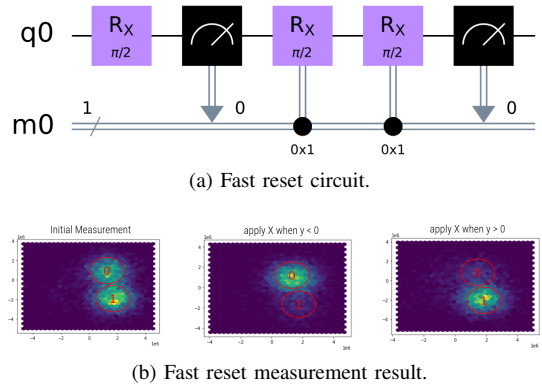

(b) Fast reset measurement result.

Fig. 7. Fast reset.

procedures are often time-consuming and involve dissipative methods that result in the loss of coherence and valuable quantum information. In contrast, fast reset techniques aim to overcome these limitations by employing non-dissipative and expedited methods to reset qubits while preserving their coherence and quantum properties.

Fast reset is a fundamental qubit control feedback loop, where low hardware latency is of utmost importance. On the QubiC 2.0 system, we developed fast reset logic by implementing qubit status classification and the feedback loop within the FPGA gateware, ensuring minimal latency. The method involves a single-shot measurement of the qubit state, followed by a conditional single-qubit gate operation. If the qubit is found in an excited state, this gate operation rotates it into the ground state. To enhance the effectiveness of qubit reset, the feedback cycle can be repeated as needed, ensuring the qubits are in a well-defined initial state for subsequent quantum computations.

As illustrated in Fig. 7a, the qubit is initialized with an X90 gate, positioning it at the equator of the sphere. The blobs on the IQ plane are shifted and rotated to create a decision boundary along the X-axis. The states $|0>$ and $|1>$ are initially equally weighted in the measurement. In the left plot of Fig. 7b, the decision criterion for state $|0>$ is $y > 0$, whereas state $|1>$ is determined by $y < 0$. To test the functionality of fast reset, when the mid-measurement state is $|1>$, we apply two consecutive X90 gates, rotating the
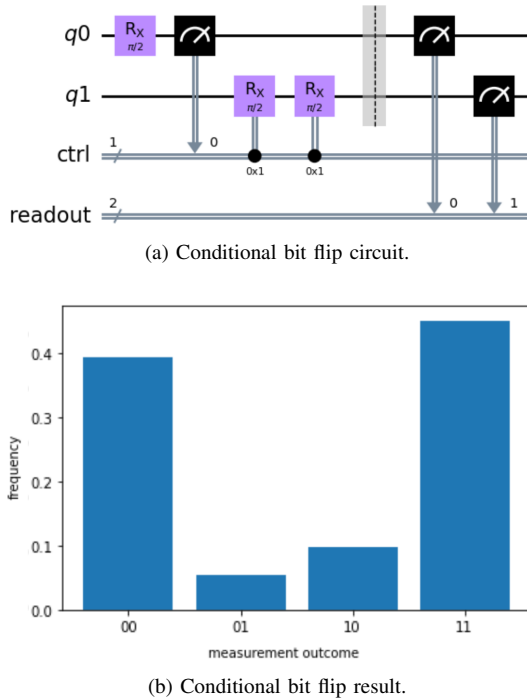
(a) Conditional bit flip circuit.

(b) Conditional bit flip result.

Fig. 8. Conditional bit flip.

measurement outcome, showcasing the successful mid-circuit measurement and feed-forward functionality of the system.

VII. CONCLUSION

We developed and upgraded the QubiC 2.0, which is an extensible open-source qubit control system capable of mid-circuit measurement and feed-forward. The system was built on the Xilinx RFSoC ZCU216 together with a customized AFE board. A portable FPGA gateware with distributed processors is implemented to handle the commands on-the-fly. QubiC 2.0 gateware enables the parameterized pulse generation, and reuses sequences by updating waveform parameters via commands without recompiling or resending all the waveform data. The full software stack is developed using Python on top of the PYNQ platform, running on the FPGA's ARM core, while an XML-RPC protocol is adopted to communicate between the host computer and the ARM core. The quantum circuit can be described in the high level language with gate and/or pulse information, and got compiled/assembled to the binary commands which is loaded to the FPGA. We successfully achieved multi-FPGA synchronization in bench tests and demonstrated the fast reset and conditional bit flip experiments on superconducting qubits. The extensible QubiC system with mid-circuit measurement and feed-forward capabilities provides researchers with powerful tools to explore and implement advanced quantum algorithms and applications.

qubit state back to $|0>$. As shown in the middle plot of Fig. 7b, state $|0>$ is observed, aligning with our expectations. Conversely, when the mid-measurement state is $|0>$, we apply two consecutive X90 gates, rotating the qubit state to $|1>$. As illustrated in the right plot of Fig. 7b, state $|1>$ is observed as anticipated, further validating the effectiveness of the fast reset process. Preliminary experiments reveal significant reductions in experiment run-time due to the active reset, all while maintaining accuracy and preserving quantum coherence.

B. Conditional Bit Flip

Mid-circuit measurement involves performing measurements on specific qubits at designated times during the execution of a quantum circuit. Feed-forward is a technique that enables the implementation of conditional operations based on the outcomes of previous quantum measurements. Mid-circuit measurement and feed-forward experiment hold significant implications for quantum algorithms and computations, including state projection, branching, measurement-based quantum computing, and error correction.

With QubiC 2.0's capabilities, mid-circuit measurement and feed-forward experiments are achievable, enabling the realization of advanced quantum algorithms. As an example, a simplified conditional bit flip circuit is demonstrated on two qubits [28].

As depicted in Fig. 8a, one qubit (Q0) is initialized to a state on the equator, and a mid-circuit measurement is performed to condition the gate operation on another qubit (Q1). If Q0 mid-circuit measurement yields $|1>$, two consecutive X90 gates will be applied on Q1. Conversely, if Q0 is measured to be $|0>$, no operation is performed on Q1. As observed in Fig. 8b, both $|00>$ and $|11>$ states evenly dominate the final

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