DIGITAL ELECTRONICS

Interview Questions and Solutions

With Detailed Explanations,
Company-wise Curation, and Expert Pro Tips

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About Me

Hello! I'm **KITTU K PATEL**, an Verification Engineer with a passion for VLSI and digital systems. I've helped many engineers break into the semiconductor industry through online mentorship, technical lectures, and curated learning content.

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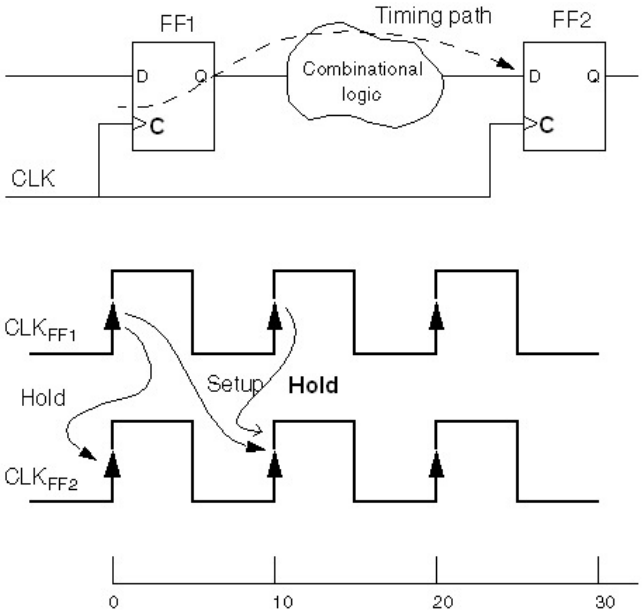
This document compiles handpicked interview questions with solutions from real company interviews like Intel, Qualcomm, AMD, and more.

Question 1: What is setup time and hold time?

Company: Intel

Answer:

Setup time is the minimum time before the clock edge by which the data input to a flip-flop must be stable. The hold time is the minimum time after the clock edge during which the data input must remain stable.



These timings ensure reliable data capture. Violating them causes metastability .

Pro Tip

Always draw a timing diagram in interviews to support your explanation!

Question 2: What is the difference between combinational and sequential circuits?

Company: Qualcomm

Answer:

- Combinational circuits produce output based only on the current input. - Sequential circuits produce output based on both current input and past input (i.e., they use memory elements like flip-flops).

Examples: - Combinational: Multiplexer, Adder - Sequential: Counter, FSM

Pro Tip

In interviews, always mention real-life applications to impress the interviewer.

Question 3: Explain the working of a D Flip-Flop.

Company: AMD

Answer:

A D (Data) Flip-Flop captures the input value of 'D' at the rising (or falling) edge of the clock and holds it until the next active clock edge. It ensures no race condition and is widely used for registers, counters, etc.

Characteristic Equation: Q(next) = D

Pro Tip

Mention how D Flip-Flop removes ambiguity in SR Flip-Flop.

Question 4: What is the difference between latch and flip-flop?

Company: Texas Instruments

Answer:

- Latch: Level-sensitive (output changes as long as enable is active) - Flip-Flop:Edge-sensitive (output changes only at clock edge)

Latches are faster but can cause timing issues. Flip-flops are safer in synchronous design.

Pro Tip

Draw both latch and flip-flop symbols during an interview to explain better.

Question 5: What is a multiplexer?

Company: Broadcom

Answer:

A multiplexer (MUX) is a combinational circuit that selects one of many inputs and routes it to a single output line, based on select lines.

2:1 MUX Equation: $Y = A.\bar{S} + B.S$

Pro Tip

Always explain real use-cases like data routing or ALU operations.

Question 6: Difference between Mealy and Moore FSM?

Company: NXP Semiconductors

Answer:

- Mealy Machine: Output depends on current state and input - Moore Machine: Output depends only on current state

Moore: Output changes with clock **Mealy:** Output changes immediately with input

Pro Tip

Mention that Moore is safer and preferred in glitch-sensitive systems.

Question 7: What is metastability in flip-flops?

Company: Qualcomm

Answer:

Metastability occurs when setup or hold time is violated, causing the flip-flop to enter an undefined or unstable state.

It may lead to uncertain logic levels or oscillation for a short period.

Pro Tip

Mention use of synchronizers to reduce metastability risk in design.

Question 8: What is a race condition?

Company: Intel

Answer:

Race condition happens when multiple signals change simultaneously and the final output depends on the order of execution.

In asynchronous systems or bad latch designs, race conditions can lead to unpredictable behavior.

Pro Tip

Say: "Avoid latches and use edge-triggered flip-flops to prevent race conditions."

Question 9: Why are flip-flops preferred over latches in digital design?

Company: STMicroelectronics

Answer:

Flip-flops are edge-sensitive and easier to control in clocked systems. Latches can cause race conditions and are harder to time in large synchronous systems.

Pro Tip

Always mention "synthesis-safe design" to show practical awareness.

Question 10: What is the difference between a decoder and a demultiplexer?

Company: Micron

Answer:

- Decoder: Converts binary code to a single active output - Demux: Routes a single input to one of many outputs using select lines

Decoder: No input data **Demux:** Has input data

Pro Tip

Add truth tables or mention decoder use in memory address decoding.

Question 11: What is a hazard in digital circuits?

Company: Infineon

Answer:

Hazards are unwanted transitions or glitches in output due to different propagation delays in logic paths.

Types: - Static hazard - Dynamic hazard - Functional hazard

Pro Tip

Mention "K-map based logic optimization" to reduce static hazards.

Question 12: What is clock skew and how to avoid it?

Company: MediaTek

Answer:

Clock skew is the difference in timing of clock signals reaching different parts of a circuit. It can lead to hold/setup violations.

Fixes: - Use proper clock tree synthesis (CTS) - Clock buffers or PLLs

Pro Tip

Add: "Balanced clock trees reduce skew and improve design robustness."

Question 13: Convert 101101 from binary to decimal.

Company: Intel

Answer:

To convert binary to decimal, multiply each bit with powers of 2:

$$1 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 = 45$$

Result: 101101 (binary) = 45 (decimal)

Pro Tip

Always write power-of-two weights above binary digits in interviews.

Question 14: What is the 2's complement of 1001?

Company: AMD

Answer:

Steps: 1. Invert the bits: 1001 → 0110 2. Add 1: 0110 + 1 = 0111

Result: 2's complement = 0111

Pro Tip

Explain that 2's complement is widely used for negative binary representation.

Question 15: What is the Gray code of binary 1011?

Company: STMicroelectronics

Answer:

Steps: 1. MSB remains same: 1 2. Next bits: XOR of previous and current bits - 10 = 1 - 01 = 1 - 11 = 0

Gray Code: 1110

Pro Tip

Mention Gray codes are useful in minimizing errors in rotary encoders.

Question 16: Convert $(27)_{10}$ to binary.

Company: Qualcomm

Answer:

Divide 27 by 2 repeatedly:

$$27/2 = 13\ rem\ 113/2 = 6\ rem\ 16/2 = 3\ rem\ 03/2 = 1\ rem\ 11/2 = 0\ rem\ 1$$

Reading in reverse: 11011

Pro Tip

Show each step clearly during interviews to get full marks.

Question 17: What is the difference between combinational and sequential logic?

Company: TI

Answer:

- Combinational: Output depends only on present input - Sequential: Output depends on present input and past history

Example: Combinational – Adder, MUX — Sequential – Flip-Flop, FSM

Pro Tip

Draw a simple block diagram of both to make the answer visual.

Question 18: Why is NAND called a universal gate?

Company: Samsung

Answer:

NAND can be used to construct all other gates: AND, OR, NOT, NOR, XOR. That's why it's called a universal gate.

Pro Tip

Draw NOT, AND, and OR using NAND logic to impress the interviewer.

Question 19: Realize XOR using only NAND gates.

Company: Cadence

Answer:

$$A \oplus B = (A \cdot \overline{B}) + (\overline{A} \cdot B)$$

Can be implemented using 4-6 NAND gates. Show intermediate steps in logic conversion.

Pro Tip

Mention that XOR is not directly synthesizable in some tools.

Question 20: What is the output of a NAND gate if both inputs are 1?

Company: Intel

Answer:

NAND means NOT of AND. 1 AND 1 = 1 $\rightarrow$ NOT(1) = 0

Result: 0

Pro Tip

Don't forget to explain truth table if asked for multiple input values.

Question 21: Draw truth table of a 2-input NOR gate.

Company: Qualcomm

Answer:

A	B	Y (NOR)
0	0	1
0	1	0
1	0	0
1	1	0

Pro Tip

Explain NOR as an inverted OR gate in your answer.

Question 22: What is the logic expression of a 4:1 MUX?

Company: Microchip

Answer:

$$Y = \overline{S1} \cdot \overline{S0} \cdot I0 + \overline{S1} \cdot S0 \cdot I1 + S1 \cdot \overline{S0} \cdot I2 + S1 \cdot S0 \cdot I3$$

Pro Tip

Always write MUX expression in SOP form with selection logic.

Question 23: What is fan-in and fan-out in logic gates?

Company: Analog Devices

Answer:

- Fan-in: Number of inputs a gate can accept - Fan-out: Number of gates a gate's output can drive

Pro Tip

Mention that high fan-out can cause signal degradation.

Question 24: Difference between active high and active low signals?

Company: Infineon

Answer:

- Active High: Logic '1' activates the function - Active Low: Logic '0' activates the function (usually denoted with bubble or underscore)

Pro Tip

Explain RESET_n signal as real-world active low example.

Question 25: What is Boolean Algebra and why is it important?

Company: Synopsys

Answer:

Boolean algebra is the mathematical framework for binary variables and logic operations. It helps to simplify digital circuits.

Pro Tip

Mention use of Boolean laws in logic simplification and minimization.

Question 26: Simplify the expression: A + AB

Company: Cadence

Answer:

Using Absorption Law:

$$A + AB = A$$

Pro Tip

Mention common identities like A + AB = A and A + A'B = A + B

Question 27: What is DeMorgan's Theorem?

Company: Intel

Answer:

DeMorgan's Theorem:

1. $\overline{A \cdot B} = \overline{A} + \overline{B}$ 2. $\overline{A + B} = \overline{A} \cdot \overline{B}$

Pro Tip

Use DeMorgan's laws to convert logic between NAND and NOR.

Question 28: Convert $(AF)_{16}$ to binary.

Company: Qualcomm

Answer:

A = 1010, F = 1111 $\rightarrow$ AF = 10101111

Result: $(AF)_{16} = 10101111_2$

Pro Tip

Mention HEX to Binary uses 4-bit chunks per hex digit.

Question 29: How many select lines are needed for a 16:1 MUX?

Company: Texas Instruments

Answer:

Number of select lines = $\log_2(16) = 4$

Pro Tip

Always mention log base 2 while calculating select lines.

Question 30: What is propagation delay in a logic gate?

Company: Analog Devices

Answer:

Propagation delay is the time taken by a signal to pass from input to output of a gate. It is measured in nanoseconds and affects timing in circuits.

Pro Tip

High propagation delay can reduce max frequency of operation.

Question 31: What is a half adder?

Company: Intel

Answer:

A Half Adder adds two single-bit binary numbers A and B.

$$Sum = A \oplus B, \quad Carry = A \cdot B$$

Pro Tip

Mention that half adder doesn't consider carry-in; that's why it's used for LSB.

Question 32: What is a full adder?

Company: AMD

Answer:

A Full Adder adds 3 bits (A, B, and Carry-in).

$$Sum = A \oplus B \oplus C_{in} Carry = (A \cdot B) + (B \cdot C_{in}) + (A \cdot C_{in})$$

Pro Tip

Mention full adders are used in cascaded form to build multi-bit adders.

Question 33: Design a 4-bit ripple carry adder.

Company: Qualcomm

Answer:

It's formed by connecting four 1-bit full adders in series. Each carry-out is fed into the next carry-in.

Pro Tip

Discuss the delay due to carry ripple and the concept of propagation delay.

Question 34: What is a carry look-ahead adder?

Company: MediaTek

Answer:

It calculates carry bits in advance using:

$$G = A \cdot B, \quad P = A \oplus B$$

Carry is calculated as:

$$C_{n+1} = G + P \cdot C_n$$

Pro Tip

Highlight it's faster than ripple adder and reduces critical path delay.

Question 35: Difference between decoder and encoder?

Company: STMicroelectronics

Answer:

- Decoder: Converts n-bit input to 2 outputs - Encoder: Converts 2 inputs to n-bit output

Pro Tip

Mention priority encoder as a special case to handle multiple inputs.

Question 36: What is a priority encoder?

Company: Synopsys

Answer:

It outputs the binary code of the highest-priority active input. If multiple inputs are high, the one with the highest priority is considered.

Pro Tip

Mention use in interrupt handling systems.

Question 37: What is a 7-segment decoder?

Company: Microchip

Answer:

It converts 4-bit binary input into control signals for 7-segment display (a-g). Used in digital clocks and calculators.

Pro Tip

Mention common cathode and common anode display types.

Question 38: What is the function of a comparator?

Company: NXP

Answer:

A comparator compares two binary numbers and outputs: $A > B$ $A = B$ $A < B$

Pro Tip

Use combinational logic like XOR and AND gates to implement 1-bit comparator.

Question 39: Design a 2-bit magnitude comparator.

Company: Analog Devices

Answer:

Compare A1A0 and B1B0:

- **A > B**: **A1 > B1** or (**A1 = B1** *and* **A0 > B0**)
- **A < B**: vice versa
- **A = B**: **A1 = B1** and **A0 = B0**

Pro Tip

Draw the truth table and K-maps to derive the logic.

Question 40: What is the role of select lines in a MUX?

Company: Intel

Answer:

Select lines decide which input line is passed to output. For 2^n inputs, n select lines are needed.

Pro Tip

Show a 4:1 MUX example with S1 and S0.

Question 41: Design a 3-to-8 line decoder.

Company: Qualcomm

Answer:

3 input lines produce 8 outputs based on binary value. Each output = one AND gate with select and inverted signals.

Pro Tip

Mention enable pin usage in hierarchical decoder design.

Question 42: What is a demultiplexer?

Company: Broadcom

Answer:

A demux sends a single input to one of many outputs based on select lines. Opposite of a multiplexer.

Pro Tip

Explain with 1:4 demux circuit.

Question 43: Why is XOR used in adders?

Company: Cadence

Answer:

XOR acts as a sum output for binary addition:

$$A \oplus B = Sum(withoutcarry)$$

Pro Tip

Use XOR in error detection, parity generation too.

Question 44: Explain combinational circuit delay.

Company: TI

Answer:

Delay = time for input change to reflect at output. Depends on gate delays and critical path.

Pro Tip

Explain timing violation risks due to delay in long combinational paths.

Question 45: Real-time applications of MUX.

Company: Microsemi

Answer:

Used in: - Data selection in ALU - Bus communication - Digital signal routing

Pro Tip

Explain 2:1 MUX as controlled switch using select.

Question 46: Implement 2-bit binary adder using full adders.

Company: Intel

Answer:

Connect two full adders: - FA1: A0, B0, Cin $\rightarrow$ S0, C1 - FA2: A1, B1, C1 $\rightarrow$ S1, Cout

Pro Tip

Draw the block diagram and label carries properly.

Question 47: What is logic minimization and its importance?

Company: Xilinx

Answer:

It reduces the number of logic gates used in a circuit. Helps in: - Reducing area - Lower power - Faster operation

Pro Tip

Use K-map and Boolean laws for minimization.

Question 48: Draw truth table of 4:1 multiplexer.

Company: NXP

Answer:

Inputs: I0–I3, Select S1–S0 Output: Y based on selected input.

S1	S0	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3

Pro Tip

Mention MUX is also used in implementing Boolean functions.

Question 49: Realize a 4:1 MUX using basic gates.

Company: Infineon

Answer:

Use 4 AND gates, 1 OR gate, and NOT gates for select line inversions.

$$Y = \overline{S1}\,\overline{S0}I0 + \overline{S1}S0I1 + S1\overline{S0}I2 + S1S0I3$$

Pro Tip

Draw gate-level schematic and explain select logic clearly.

Question 50: Difference between combinational and sequential hazards.

Company: TI

Answer:

- Combinational hazard: Due to gate delay differences in logic paths - Sequential hazard: Due to improper clocking or synchronization in sequential circuits

Pro Tip

Use redundant logic or synchronous design to avoid hazards.

Question 51: What is a sequential circuit?

Company: Intel

Answer:

A sequential circuit's output depends on both current inputs and past inputs (stored in memory). It includes storage elements like latches and flip-flops.

Pro Tip

Always contrast it with combinational circuits for clarity.

Question 52: Difference between synchronous and asynchronous sequential circuits?

Company: AMD

Answer:

- Synchronous: State transitions occur with clock edges - Asynchronous: State transitions happen immediately based on inputs

Pro Tip

Mention glitches and timing issues in asynchronous designs.

Question 53: What is a latch?

Company: Qualcomm

Answer:

A latch is a level-sensitive storage element that stores 1-bit data when enabled.

$$SRLatch : Q = S + \overline{R}Q$$

Pro Tip

Explain latch sensitivity to input glitches.

Question 54: What is a flip-flop?

Company: TI

Answer:

Flip-flop is an edge-triggered memory device that stores 1 bit. Changes output only on clock edge (positive/negative).

Pro Tip

Mention flip-flops are used in synchronous circuits for predictable behavior.

Question 55: Explain SR flip-flop.

Company: Microchip

Answer:

Has two inputs: Set (S) and Reset (R). Output logic: - S=1, R=0 → Set (Q=1) - S=0, R=1 → Reset (Q=0) - S=1, R=1 → Invalid

Pro Tip

Explain invalid condition and how D flip-flop avoids it.

Question 56: What is a T Flip-Flop?

Company: STMicroelectronics

Answer:

T (Toggle) Flip-Flop changes its state if T=1, else holds previous state.

$$Q_{next} = T \oplus Q_{current}$$

Pro Tip

Used in counters for toggling and frequency division.

Question 57: Difference between edge-triggered and level-triggered devices?

Company: Xilinx

Answer:

- Edge-triggered: Trigger only on rising/falling clock edge - Level-triggered: Output changes as long as enable level is active

Pro Tip

Always relate it to latches (level) and flip-flops (edge).

Question 58: Define setup and hold time.

Company: Synopsys

Answer:

- Setup time: Minimum time before clock edge that input must be stable - Hold time: Minimum time after clock edge that input must remain stable

Pro Tip

Use waveform diagram if possible to score bonus in interviews.

Question 59: What is clock skew and its impact?

Company: MediaTek

Answer:

Clock skew is the time difference between arrival of clock signal at different components. It may lead to timing violations.

Pro Tip

Mention clock tree synthesis (CTS) to fix skew in design.

Question 60: What is metastability?

Company: Intel

Answer:

A condition where flip-flop enters undefined state due to setup/hold violations. It may take longer to settle at logic high or low.

Pro Tip

Mention use of 2-stage synchronizers to reduce risk.

Question 61: What is a finite state machine (FSM)?

Company: Cadence

Answer:

FSM is a sequential circuit that transitions between finite states based on inputs and current state.

Two types: - Mealy - Moore

Pro Tip

Draw state diagram for better understanding.

Question 62: Difference between Mealy and Moore machines?

Company: TI

Answer:

- Moore: Output depends only on state - Mealy: Output depends on state and input

Pro Tip

Moore is glitch-free but Mealy is faster.

Question 63: Design a JK flip-flop using SR flip-flop.

Company: Qualcomm

Answer:

Inputs: - J = S - K = R Add feedback from output to create toggle behavior.

Pro Tip

Explain that JK overcomes invalid state of SR.

Question 64: What is a counter in sequential circuits?

Company: Broadcom

Answer:

A counter counts clock pulses and stores binary count. Types: Up, Down, Up-Down, Ring, Johnson

Pro Tip

Mention use in timers, event counting, frequency division.

Question 65: Explain synchronous vs asynchronous counter.

Company: Micron

Answer:

- Synchronous: All flip-flops triggered by same clock - Asynchronous: Triggered one after another (ripple effect)

Pro Tip

Synchronous counters are faster and glitch-free.

Question 66: Design a 3-bit up counter.

Company: NXP

Answer:

Use 3 T flip-flops: - First toggles every clock - Second toggles when first = 1 - Third toggles when both lower bits = 1

Pro Tip

Draw timing waveform or state table for better clarity.

Question 67: What is a shift register?

Company: Microchip

Answer:

Sequential circuit that shifts data left or right on each clock pulse. Used for serialization and delay circuits.

Pro Tip

Mention SISO, SIPO, PISO, PIPO types.

Question 68: What is the difference between register and counter?

Company: TI

Answer:

- Register: Stores data - Counter: Increments/decrements value with clock

Pro Tip

Mention both use flip-flops but have different logic around them.

Question 69: Real-time applications of sequential circuits.

Company: Analog Devices

Answer:

Used in: - Traffic light controllers - CPU registers - Timers and Counters - FSM controllers in VLSI chips

Pro Tip

Always quote an example from industry or personal project.

Question 70: Difference between Moore machine and FSM-based design in RTL?

Company: Synopsys

Answer:

Moore-based FSMs generate output in states and hence require fewer transitions. FSM in RTL is a standard structure with: - State encoding - Next state logic - Output logic

Pro Tip

Mention how coding style changes for synthesis and simulation.

Question 71: What is the difference between RAM and ROM?

Company: Intel

Answer:
- RAM (Random Access Memory): Volatile, used for temporary data storage - ROM (Read-Only Memory): Non-volatile, used for permanent storage

Pro Tip

Mention RAM is used for runtime data, while ROM stores firmware.

Question 72: What is the difference between SRAM and DRAM?

Company: Micron

Answer:
- SRAM: Faster, uses flip-flops, expensive, no refresh needed - DRAM: Slower, uses capacitors, cheaper, needs periodic refresh

Pro Tip

Mention SRAM is used in cache; DRAM in main memory.

Question 73: What is a memory cell?

Company: STMicroelectronics

Answer:
A memory cell is the smallest unit of memory that stores 1 bit. SRAM uses 6T (transistors), DRAM uses 1T1C (1 transistor + 1 capacitor).

Pro Tip

Explain how write/read access works in memory cells.

Question 74: Define volatile and non-volatile memory.

Company: AMD

Answer:
- Volatile: Loses data when power is off (e.g., RAM) - Non-volatile: Retains data without power (e.g., ROM, Flash)

Pro Tip

Mention EEPROM and Flash as programmable non-volatile types.

Question 75: What is the role of address lines in memory?

Company: Texas Instruments

Answer:

Address lines specify the memory location for accessing data. If there are n address lines, memory can store 2^n locations.

Pro Tip

For 16 address lines, memory has 64KB capacity.

Question 76: What is the purpose of control signals in memory?

Company: Cypress

Answer:

Control signals manage the read and write operations. Common signals: - CS (Chip Select) - WE (Write Enable) - OE (Output Enable)

Pro Tip

Explain active high/low control signal conventions.

Question 77: What is ROM? Name its types.

Company: Microchip

Answer:

ROM stores data permanently. Types: - PROM (Programmable) - EPROM (Erasable) - EEPROM (Electrically Erasable)

Pro Tip

Mention EPROM uses UV light to erase.

Question 78: Explain Flash Memory.

Company: Intel

Answer:

Flash is a type of EEPROM with faster access. Used in USB drives, SSDs, embedded systems.

Pro Tip

Mention NAND and NOR Flash differences.

Question 79: What is Cache Memory?

Company: Qualcomm

Answer:

Cache is a small, fast memory between CPU and RAM. Stores frequently accessed data for quick access.

Pro Tip

Levels: L1 (smallest, fastest), L2, L3 (shared).

Question 80: What is memory latency?

Company: Synopsys

Answer:

Latency is the time delay between memory request and data access. Lower latency means faster performance.

Pro Tip

Mention latency in DRAM is higher due to refresh cycles.

Question 81: What is burst access in memory?

Company: MediaTek

Answer:

Burst mode allows multiple memory locations to be read/written with one command, increasing speed.

Pro Tip

Used in SDRAM and DDR to improve bandwidth.

Question 82: Define access time and cycle time.

Company: TI

Answer:

- Access Time: Time to read data from memory - Cycle Time: Minimum delay between two successive memory operations

Pro Tip

Cycle time access time in most cases.

Question 83: What is memory mapping?

Company: Infineon

Answer:

Memory mapping associates memory addresses with hardware or program locations. Used in embedded systems for I/O interfacing.

Pro Tip

Mention difference between memory-mapped I/O and isolated I/O.

Question 84: How is data read from memory?

Company: Xilinx

Answer:

Steps: 1. Apply address 2. Enable chip and output 3. Data appears on output bus

Pro Tip

Mention tristate buffers are used during data read.

Question 85: What is address decoding in memory?

Company: Analog Devices

Answer:

It selects a specific memory location or chip based on the input address. Uses logic gates or decoders.

Pro Tip

Show address map in embedded memory design.

Question 86: What is the difference between static and dynamic RAM refresh?

Company: Micron

Answer:

- Static RAM: No refresh needed - Dynamic RAM: Periodic refresh to retain charge in capacitors

Pro Tip

Mention refresh overhead in DRAM affects performance.

Question 87: What is virtual memory?

Company: Intel

Answer:

Virtual memory uses secondary storage to simulate more RAM. Managed by OS using page tables and swapping.

Pro Tip

Mention TLB (Translation Lookaside Buffer) speeds up translation.

Question 88: Explain CAM (Content Addressable Memory).

Company: NXP

Answer:

CAM returns address when data is input (opposite of normal memory). Used in search operations like cache and TLB.

Pro Tip

Mention used in networking hardware (fast lookups).

Question 89: What is dual-port RAM?

Company: Xilinx

Answer:

Dual-port RAM allows two independent read/write operations at the same time using separate ports.

Pro Tip

Used in FIFO designs and multi-core processors.

Question 90: What is ECC in memory?

Company: Synopsys

Answer:

ECC (Error Correcting Code) detects and corrects memory errors using parity and Hamming codes.

Pro Tip

Mention it's used in server-grade memory for reliability.

Question 91: What is Static Timing Analysis (STA)?

Company: Synopsys

Answer:

STA is a method to validate timing of digital circuits without applying test vectors. It checks worst-case delays and ensures setup/hold timing constraints are met.

Pro Tip

Mention STA uses timing models, not simulation data.

Question 92: What is setup time violation?

Company: Cadence

Answer:

Setup time is the minimum time data must be stable before the clock edge. If not satisfied, flip-flop may capture wrong data.

Pro Tip

Mention setup check: `Data Arrival Time  Clock Edge - Setup Time`

Question 93: What is hold time violation?

Company: Intel

Answer:

Hold time is the minimum time data must remain stable after the clock edge. Violation occurs if data changes too early, leading to incorrect capture.

Pro Tip

Hold check: `Data Arrival Time  Clock Edge + Hold Time`

Question 94: What is clock skew?

Company: Micron

Answer:

Clock skew is the timing difference in clock signal arrival at different flip-flops. It may cause setup or hold violations.

Pro Tip

Mention positive skew helps hold; negative skew helps setup.

Question 95: What is slack in STA?

Company: AMD

Answer:

Slack = Time available – Time required - Positive Slack → No violation - Negative Slack → Timing violation

Pro Tip

Show example of setup slack = Required Arrival - Actual Arrival

Question 96: Define launch and capture edge.

Company: STMicroelectronics

Answer:

- Launch edge: Clock edge at start point (flip-flop sending data) - Capture edge: Clock edge at endpoint (flip-flop capturing data)

Pro Tip

Always show data path and clock path in a diagram.

Question 97: What is timing path in STA?

Company: Texas Instruments

Answer:

A timing path is from: - Launch flip-flop clock pin → through combinational logic → to capture flip-flop D pin

Pro Tip

Include data delay, clock delay, setup/hold in full path analysis.

Question 98: What is a false path?

Company: NXP

Answer:

False path is a timing path that is not exercised during normal operation. It's ignored in timing analysis using constraints.

Pro Tip

Use set$_{f}alse_{p}athinSDCtopreventfalseviolations.$

Question 99: What is multicycle path?

Company: Infineon

Answer:

Multicycle path requires more than one clock cycle for data to propagate. Used to relax timing in long combinational paths.

Pro Tip

Use set$_m ulticycle_p athtoadjustsetup/holdchecks$.

Question 100: What is the role of constraints in STA?

Company: Synopsys

Answer:

Constraints like clock definitions, I/O delays, false/multicycle paths define timing environment in STA. They guide analysis and ensure realistic checking.

Pro Tip

Constraints are written in .SDC format for most STA tools.

Congratulations!

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"Success doesn't come from what you do occasionally, it comes from what you do consistently."

– **Marie Forleo**

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