THOUGHT RECOGNITION USING BRAIN COMPUTER INTERFACE

CAPSTONE PROJECT REPORT

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August to November, 2017

DECLARATION

We, hereby, declare that the project work entitled **"Thought Recognition using Brain Computing Interface"** is an authentic record of our own work carried out as a requirement of six months Capstone Project for the award of degree of B.E. Electronics and Communication Engineering, PEC University of Technology, Chandigarh, under the guidance of **Mr. Anshul Kumar**, from August to November, 2017.

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Certified that the above statement made by the students is correct to the best of my knowledge and belief.

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ACKNOWLEDGEMENT

We avail this prospect to express our thoughtful sense of sincerity, earnestness and deep gratitude to all those who have performed a vital role in the achievement of the project "**Thought Recognition using Brain Computing Interface**" by providing their alacritous guidance and support.

We wish to express our sincere and heartfelt obligation to **Mr. Anshul Kumar**, Assistant Professor and Capstone Coordinator for his incessant encouragement and inspiration throughout the project. Without his enduring spur, generous guidance and help, we would not have been able to cope up with the project work.

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1 ABSTRACT

Brain Computer Interfaces (BCI) is a thought-provoking area for researchers as, according to recent developments, it is found to unravel many problems, which seemed impossible, earlier. The main purpose of BCI applications is to renovate thoughts of a handler to perform an act in a device, machine or a computer, and control these devices. Majority of the applications of BCI are aimed at the patients suffering from Disorders of Consciousness (DOC). Patients with DOC are unable to communicate with the outer world and find trouble fitting in the environment. By using BCI, a user can control certain devices or machines to perform some of the basic and important jobs that are required without taking help from some other person. These actions range from moving a wheelchair, getting something for eating or drinking by using robotic arms or wheels controlled by brain. BCI is also used to help provide vision to blind people by connecting an external camera with brain as it can be seen in the case of 'Jans Naumann'. Device control using BCI not only include patients, but healthy people can also employee it, who need to perform many jobs simultaneously like divers, astronauts etc. where they keep their hands on operating equipment and the steering wheel. Rabie et al. developed a BCI based system that can help a disabled person to use the web through his brain only. Other applications of Brain Computer Interface include neuroscience research, development in medical technologies which are related to brain or the central nervous system directly or indirectly.

2 INTRODUCTION

1.1 DEFINITION

Brain Computer Interface (BCI) can be said as a collaboration between a brain and a device that enables signals from the brain to direct some external activity, such as control of a cursor or a prosthetic limb. The interface enables a direct communications pathway between the brain and the object to be controlled. A brain–computer interface (BCI) is sometimes referred as Mind Machine Interface (MMI), Direct Neural Interface (DNI), Synthetic Telepathy Interface (STI) and Brain Machine Interface (BMI).

1.2 A BASIC BCI SYSTEM

A basic BCI System can be constructed in the following steps.

Step 1: Signal Acquisition

- Capturing the electrical signals from brain
- Amplification and Digitization

Step 2: Signal Processing

- Preprocessing
  - Enhancement for making the features clear for detection
  - Filtering
- Feature extraction
  - Extraction of specific signal features
  - Removal of unwanted signals
- Signal Classification
  - Translation algorithm
  - Features extracted from the signal are translated into device commands

Step 3: Data Manipulation

- Output is manipulated according to the standards of output devices.

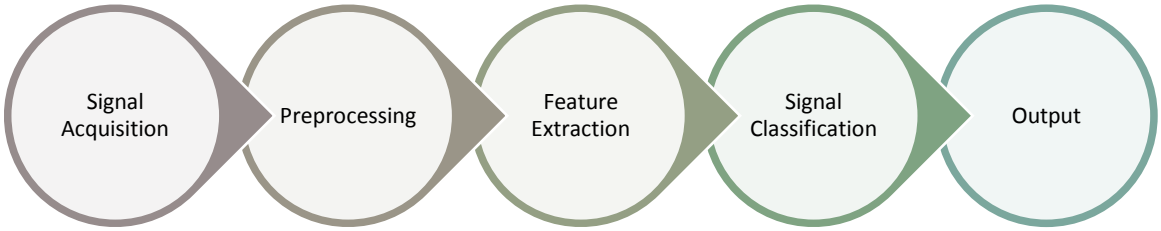


FIGURE 1 : A BASIC BCI SYSTEM

1.3 TYPES OF BCI SYSTEM

1.3.1 CLASSIFICATION BASED ON PLACEMENT OF ELECTRODES

1.3.1.1 Invasive BCI

Invasive BCI devices are implanted directly into the grey matter of the brain and provides the highest quality of signals. But this technique is prone to scar-tissue build-up, which results in weakening of the signal. Moreover, the immune system sometimes reacts to it as a foreign entity.

1.3.1.2 Partially Invasive BCI

Unlike Invasive BCI technique, partially invasive BCI devices are entrenched under the scalp. It can be either outside or inside the skull, but rests outside the grey matter of brain. Unlike Invasive BCI, signal strength using this type of BCI device is a little weaker. It produces better resolution signals than noninvasive. In this technique, there is less risk of scar tissue formation when compared with Invasive BCI.

1.3.1.3 Non-invasive BCI

In Non-Invasive BCI technique, the measuring sensors are mounted on caps or headbands, which record the signals generated by brain. This approach is not so indiscreet but reads the signals less effectively, because the electrodes are not placed on required part of the brain but on the scalp. An example of this category is the EEG or electroencephalography, which is capable of providing a fine temporal resolution. These are inexpensive, transferable and can be used easily.

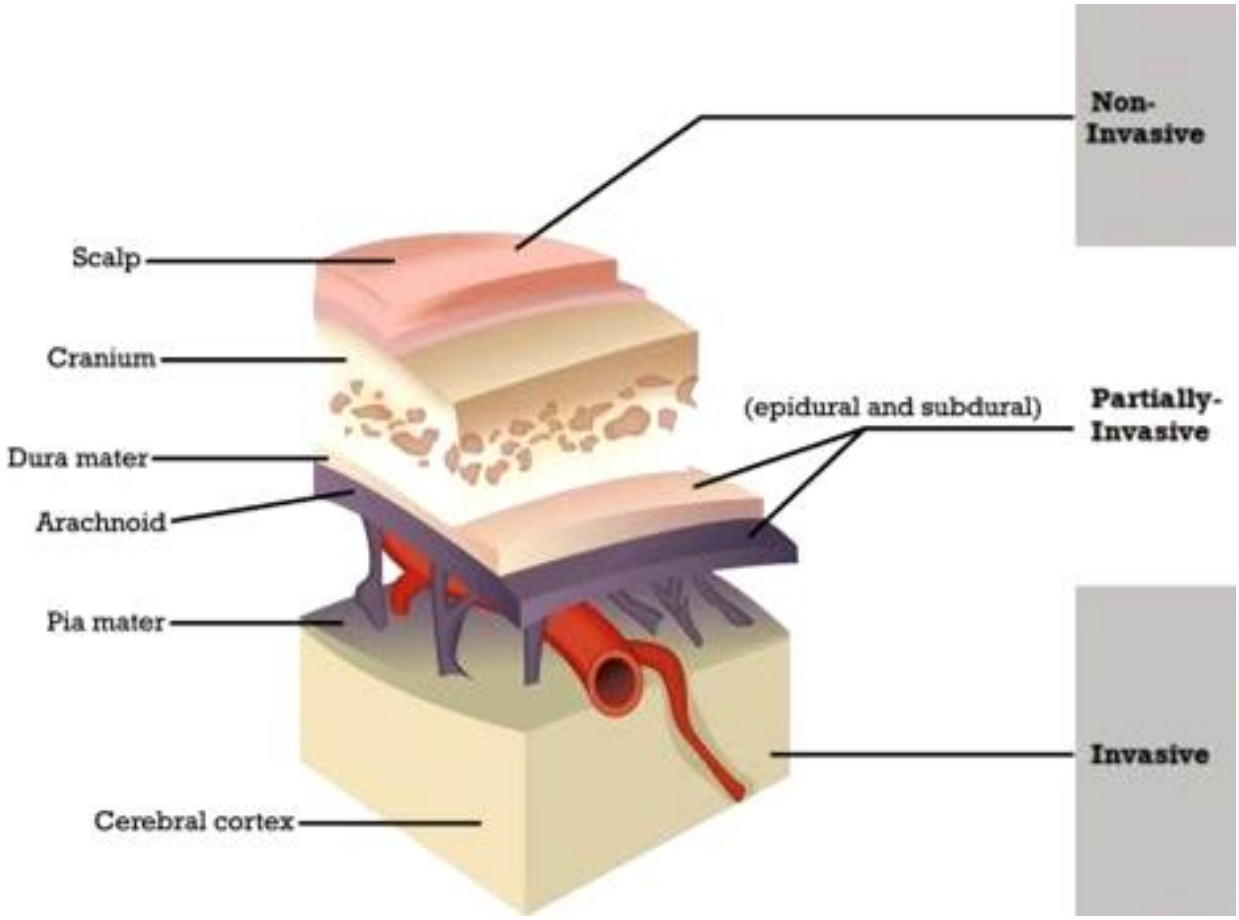


FIGURE 2 : CLASSIFICATION BASED ON PLACEMENT OF ELECTRODES

1.3.2 CLASSIFICATION BASED ON TYPE OF STIMULUS

a. SSVEP

SSVEP type of BCI entails a number of visual or pictorial stimuli. Each stimulus is related with a precise command, which is associated with an output, which the BCI can produce. The stimuli flicker unceasingly with diverse frequencies ranging from 6 to 30 Hz. Paying attention to one of the flickering stimuli elicits an SSVEP in the visual cortex of the brain that has the same frequency as the target flicker.

b. P300

P300 wave elicits when an unlikely event occurs randomly between events with high probability. In the EEG signal the P300 appears as a positive wave about 300 ms after stimulus onset. Its main usage in BCIs is for spelling devices, but one can also use it for control tasks or navigation.

c. Motor Imagery

When subjects perform or only imagine motor tasks, an event related desynchronization (ERD) and an event related synchronization (ERS) is detectable by changes of EEG rhythms on electrodes close to the respective sensorimotor areas. The ERD is indicated by a decrease of power in the upper alpha band and lower beta band, starting 2 seconds before movement onset on the contra lateral hemisphere and becomes bilaterally symmetrical immediately before execution of movement. An ERS appears either after termination of the movement, or simultaneously to the ERD, but in other areas of the cortex.

1.4 BIO-AMPLIFIER

Biological signals are chronicled as potential levels, voltage levels, and electrical field strengths which are generated by nerves and muscles. Their measurements involve voltage which is at very low level, characteristically, it ranges from 1μV to a maximum of 100mV, with a high source impedance and overlaid high level interfering signals and noises. First, the signals are required to be amplified, to make them compatible with devices such as displays, recorders, or A/D converters for computerized equipment. Bio Amplifiers have to provide a particular level of amplification discerning to the functional signal, discard overlaid noise and interfering signals, and assured protection from voltage and current surge for the user as well as the electronic equipment. The basic requirements that a bio amplifier has to satisfy are:

- The functional processes that are needed to be scrutinized, should not be predisposed by the amplifier
- Signal that is measured should not be distorted
- There should also be the best conceivable separation between signals and interferences
- Protection from electrical shock to the patient should be provided
- The amplifier is required to be protected against damages resulting from high input voltages

1.5 BEHAVIOR OF AN EEG SIGNAL

Differentiation of alpha (α), beta (β), delta (δ), and theta (Θ) waves can be done by EEG signals. The range of these waves is stated as follows:

- Alpha Waves: 8-13Hz, occipital region in an awake person with eyes closed
- Beta Waves: 13-30Hz, found in the parietal and frontal lobe of the brain

- Delta Wave: 0.5-4Hz, found in sleeping adults and infants
- Theta Wave: 4-8Hz, sleeping adults as well as sleeping children

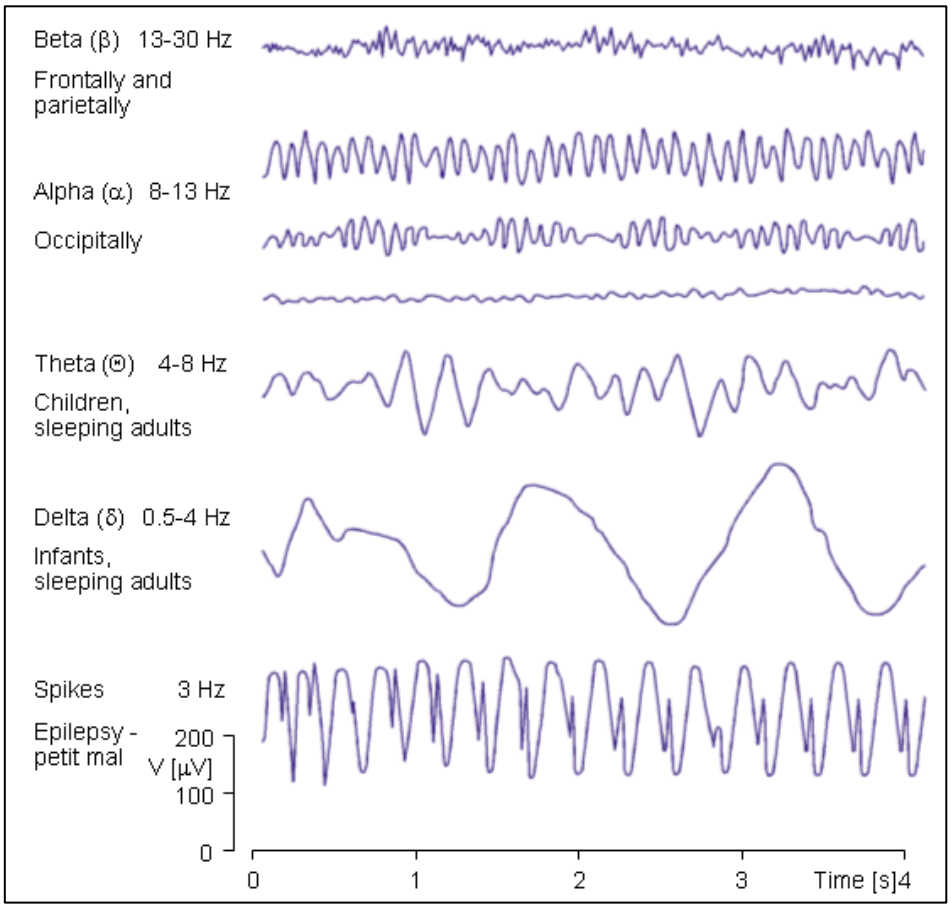


FIGURE 3 : VARIOUS COMPONENTS OF AN EEG SIGNAL

Alpha waves are neural oscillations in the frequency range of 7.5–12.5 Hz arising from synchronous and coherent (in phase or constructive) electrical activity of thalamic pacemaker cells in humans. They are also called Berger's wave in memory of the founder of EEG.

Alpha waves are one type of brain waves detected by electroencephalography (EEG) and predominantly originate from the occipital lobe during wakeful relaxation with closed eyes. Alpha waves are reduced with open eyes, drowsiness and sleep. Historically, they were thought to represent the activity of the visual cortex in an idle state. More recent papers have argued that they inhibit areas of the cortex not in use, or alternatively that they play an active

role in network coordination and communication. Occipital alpha waves during periods of eyes closed are the strongest EEG brain signals.

Alpha waves are present at different stages of the wake-sleep cycle. The most widely researched is during the relaxed mental state, where the subject is at rest with eyes closed, but is not tired or asleep. This alpha activity is centered in the occipital lobe, and is presumed to originate there, although there has been recent speculation that it instead has a thalamic origin. This wave begins appearing at around four months, and is initially a frequency of 4 waves per second. The mature alpha wave, at 10 waves per second, is firmly established by age 3.

1.5.1 OCCIPITAL LOBE

The cerebral cortex of the brain—a part of the brain shared by all vertebrates—is the newest part of the brain, evolutionarily speaking. All mammalian brains have four distinct lobes, but the brain itself—as well as the lobes it contains—is divided into right and left hemispheres.

This means that each lobe can actually be divided into two parts. The occipital lobe includes right and left lobe that interact with one another, each controlling a range of visual functions.

Like other lobes of the brain, the occipital lobe does not have clear internal boundaries separating it from the rest of the brain. Instead, neuroscientists use the skull's bones as their guide, so the occipital lobe rests underneath the occipital bone.

The occipital lobe is the rearmost lobe of the brain, located in the forebrain. It rests upon the tentorium cerebelli, a thick membrane of tissue the separates the cerebrum from the evolutionarily older cerebellum.

The occipital lobe is dedicated to vision, this process is highly complex, and includes a number of separate functions. Those include:

- Mapping the visual world, which helps with both spatial reasoning and visual memory. Most vision involves some type of memory, since scanning the visual field requires you to recall that which you saw just a second ago.
- Determining color properties of the items in the visual field.
- Assessing distance, size, and depth.
- Identifying visual stimuli, particularly familiar faces and objects.
- Transmitting visual information to other brain regions so that those brain lobes can encode memories, assign meaning, craft appropriate motor and linguistic responses, and continually respond to information from the surrounding world.
- Receiving raw visual data from perceptual sensors in the eyes' retina.

The occipital lobe contains a number of structures and neuronal tracts that work together to enable vision. Those include:

- Brodmann area 17: Known as V1, this region is located in the occipital lobe's calcarine sulcus, and serves as the brain's primary visual cortex. It aids the brain to determine location, spatial information, and color data.
- The ventral stream: Known sometimes as V2, this is a secondary visual cortex that helps the brain assign meaning to what it is seeing. Without V2, you would still be able to see, but would have no conscious awareness of or understanding of the sights your eyes took in.
- The dorsomedial stream: Neuroscientists don't yet have a strong understanding of this brain region, which connects to both V1 and V2, as well as other brain regions.
- The lateral geniculate bodies: These structures take in optic information from retinal sensors in each eye, sending raw information to each visual cortex.
- Lingula: this area receives information from the contralateral inferior retina to gather information about the field of vision.

1.6 EEG DIAGNOSTICS

Whenever, the activity of a person increases, the EEG shifts to higher governing frequency and lower level of amplitude. Thus, it can be said that, EEG signals are closely associated to the conscious level of a person.

- The alpha waves begin to govern the EEG signals, when eyes are closed.
- The dominating EEG frequency decreases, when the person is asleep.
- In Rapid Eye Movement (REM) sleep, the person dreams and has active movements of the eyes. This gives a different output signal.
- During deep sleep, the EEG shows delta waves.
- No intellectual activity can be perceived from a patient, with complete cerebral death.

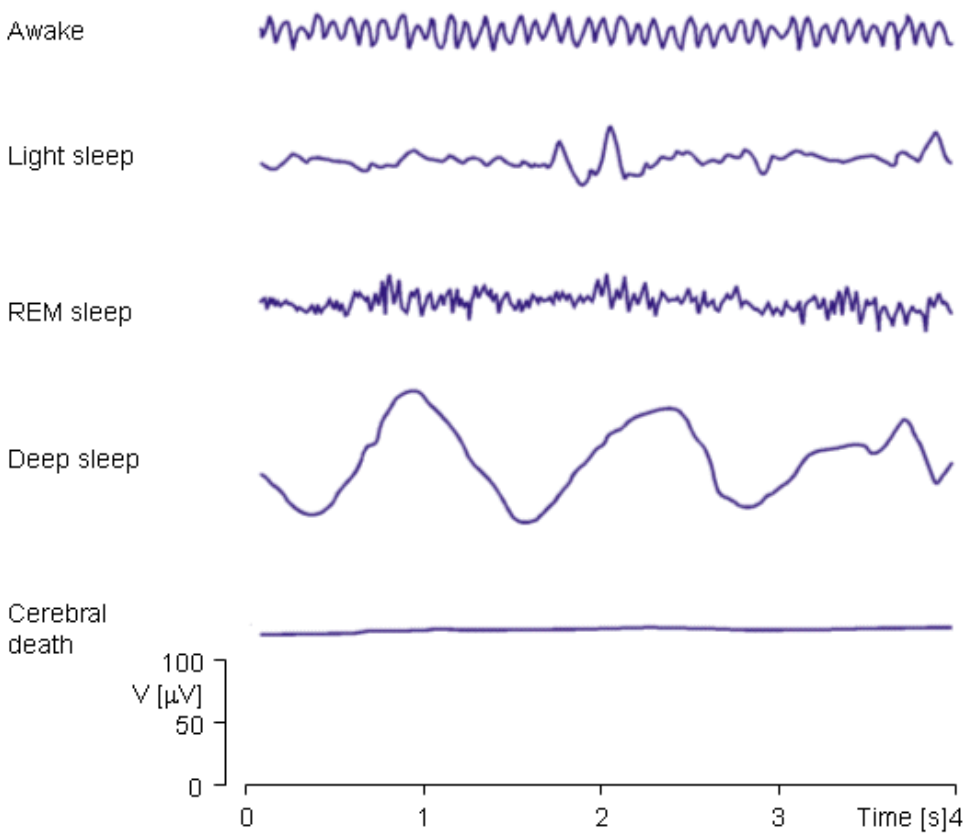


FIGURE 4 : VARIOUS STATES OF THE EEG SIGNAL

2 COMPONENTS USED

2.1 LIST OF COMPONENTS USED

Sr No.	*Component*
1	INA 128
2	OP AMP 741
3	Capacitors
4	General Purpose Board
5	Jumper wires
6	Burg Strip
7	EEG Electrode
8	UPS
9	Resistors
10	STM32F103C8T6

FIGURE 5 : BILL OF MATERIALS

2.2 INA128

The INA128 and INA129 are low-power, general purpose instrumentation amplifiers offering excellent accuracy. The versatile 3-op amp design and small size make these amplifiers ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (200 kHz at G = 100).

A single external resistor sets any gain from 1 to 10,000. The INA128 provides an industry-standard gain equation. The INA128 is laser-trimmed for very low offset voltage (50 µV), drift (0.5 µV/°C) and high common mode rejection (120 dB at G ≥ 100). The INA128 operates with power supplies as low as ±2.25 V, and quiescent current is only 700 µA, ideal for battery operated systems. Internal input protection can withstand up to ±40 V without damage.

The INA128 is available in 8-pin plastic DIP and SO-8 surface-mount packages, specified for the –40°C to 85°C temperature range. The INA128 is also available in a dual configuration, the INA2128.

FEATURES

- Low Offset Voltage: 50 µV Maximum
- Low Drift: 0.5 µV/°C Maximum accuracy.
- Low Input Bias Current: 5 nA Maximum
- High CMR: 120 dB minimum applications.
- Inputs Protected to ±40 V
- Wide Supply Range: ±2.25 V to ±18 V
- Low Quiescent Current: 700 µA
- 8-PIN Plastic Dip, SO-8

APPLICATIONS

- Bridge Amplifier
- Thermocouple Amplifier
- RTD Sensor Amplifier
- Medical Instrumentation
- Data Acquisition

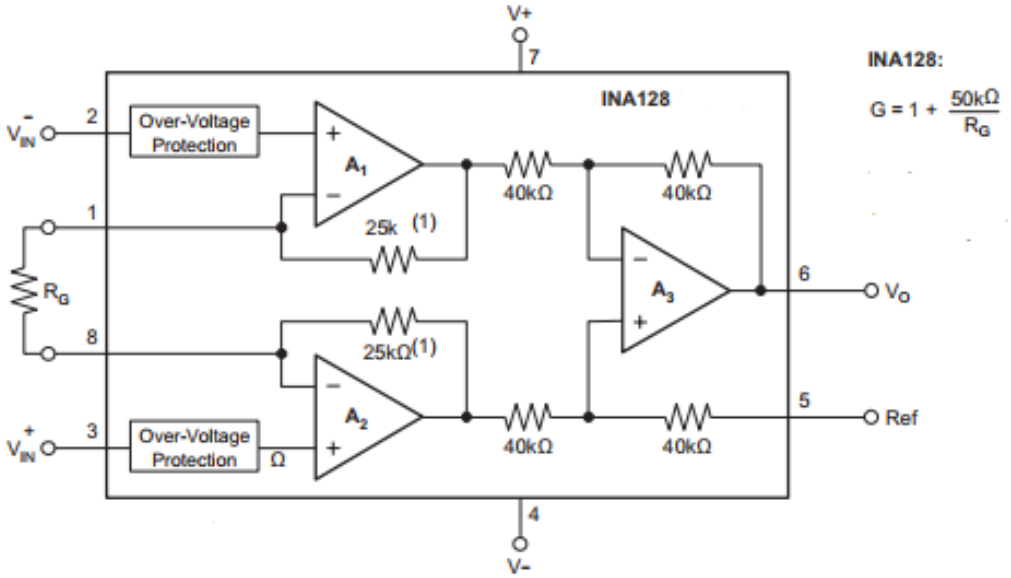


FIGURE 6 : INA128 INTERNAL CIRCUIT DIAGRAM

2.3 OP-AMP 741

The OP-AMP 741 is a high performance monolithic operational amplifier constructed on a single silicon chip. It is intended for a wide range of analog applications.

- Summing amplifier
- Voltage follower
- Integrator
- Active filter
- Function generator

The high gain and wide range of operating voltages provide superior performances in integrator, summing amplifier and general feedback applications. The internal compensation network (6dB/octave) insures stability in closed loop circuits.

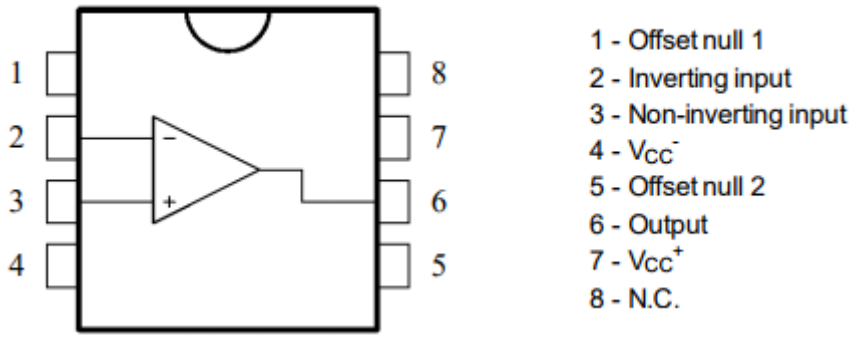


FIGURE 7 : PIN LAYOUT FOR 741C OP-AMP

2.4 STM32F103C8T6

The STM32F103C8 medium-density performance line family incorporates the high-performance ARM Cortex-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory up to 128 Kbytes and SRAM up to 20 Kbytes), and an extensive range of enhanced I/O and peripherals connected to two APB buses. All devices offer two 12-bit ADCs, three general purpose 16-bit timers plus one PWM timer, as well as standard and advanced communication interfaces: up to two I^2Cs and SPIs, three USARTs, an USB and a CAN.

The devices operate from a 2.0 to 3.6 V power supply. They are available in both the –40 to +85 °C temperature range and the –40 to +105 °C extended temperature range. A comprehensive set of power-saving mode allows the design of low-power applications.

These features make the STM32F103xx medium-density performance line microcontroller family suitable for a wide range of applications such as motor drives, application control, medical and handheld equipment, PC and gaming peripherals, GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms, and HVACs.

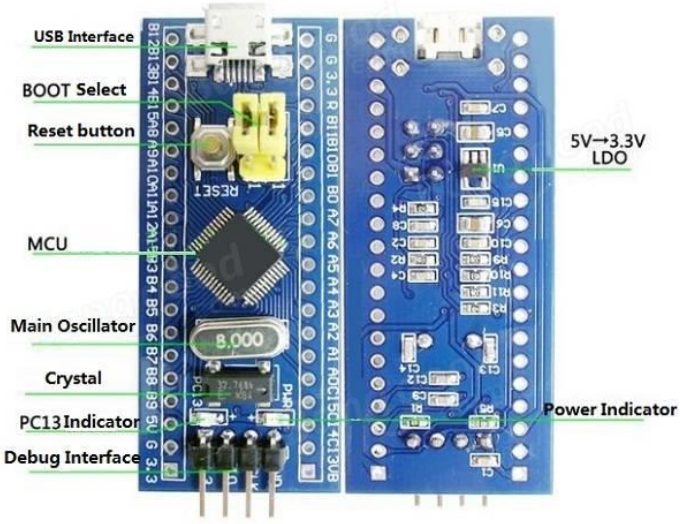


FIGURE 8 : STM32F103C8T8 BOARD

3 WORKING

Before analyzing the brain signals for any application, the signals have to go through the following steps namely: Amplification, Filtering, Classification and Control. The following section deals with the steps which explains the complete path for signal retrieval to processing and application.

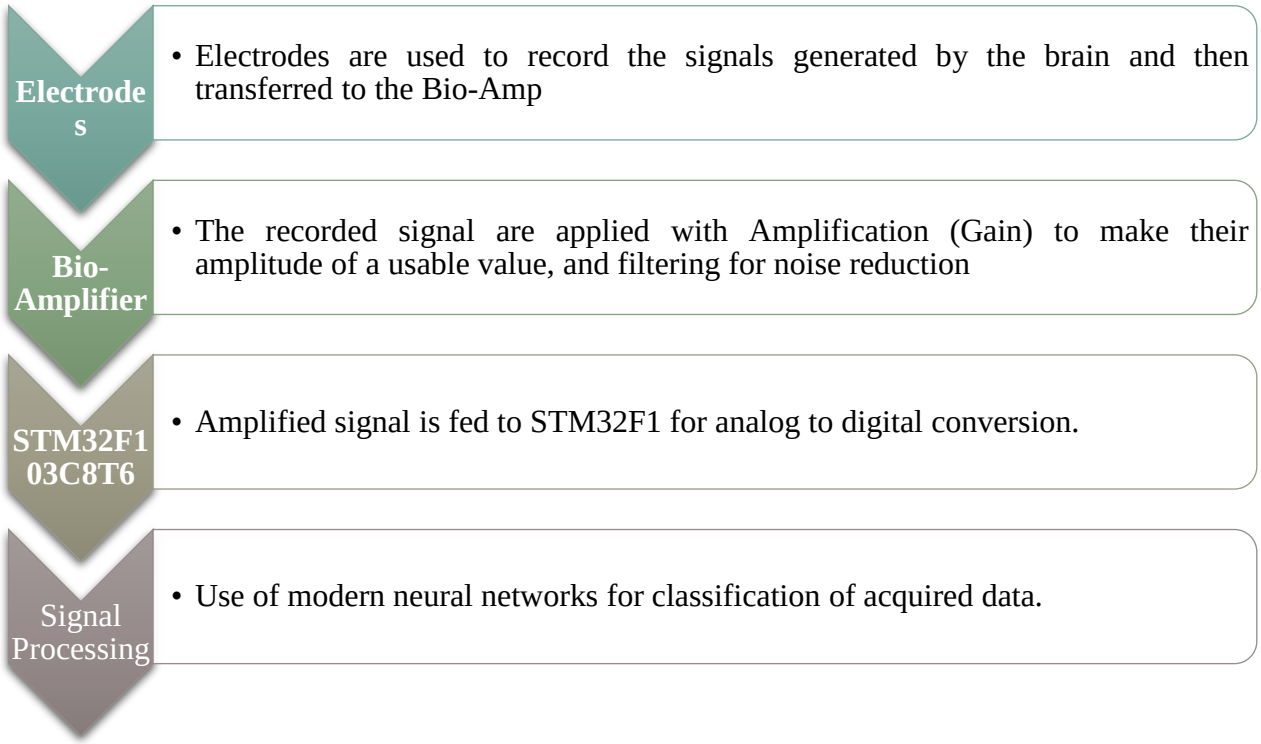


FIGURE 9 : STEPS INVOLVED FROM DATA ACQUISITION TO PROCESSING

3.1 ELECTRODE SYSTEM

The EEG recording electrodes and their proper function are critical for acquiring appropriately high-quality data for interpretation. Many types of electrodes exist, often with different characteristics. The internationally standardized "10-20 system" is usually employed to record the EEG signals.

In the 10-20 system, a set of 21 electrodes is placed on of the scalp. The positions include:

- *Nasion*: It is probed at the top of the nose and in level with the eyes; and
- *Inion*: It is placed at the base of the skull and in the midline at the back of the head.

From these points, the skull boundaries are measured in the transverse and median planes. Electrode are placed by dividing these boundaries at intervals of 10% and 20%. Three other electrodes are placed on each side equidistant from the neighboring points. In addition to these electrodes, the intermediate 10% electrode positions are also used. The locations and nomenclature of these electrodes is standardized by the “American Electroencephalographic Society”.

In addition to the international 10-20 system of 21 electrodes, many other electrode systems exist for recording purposes on the scalp. The “Queen Square System” of electrode placement has been projected as a standard in recording the pattern of evoked potentials in biological testing.

Bipolar or unipolar electrodes can be used in the EEG measurement. In bipolar electrode method, the potential difference between a pair of electrodes is measured and in the unipolar electrode method the potential of each electrode is compared either to a neutral electrode or to the average of all electrodes.

We have used 10-20 electrode system for placement of electrodes in occipital region and for reference region.

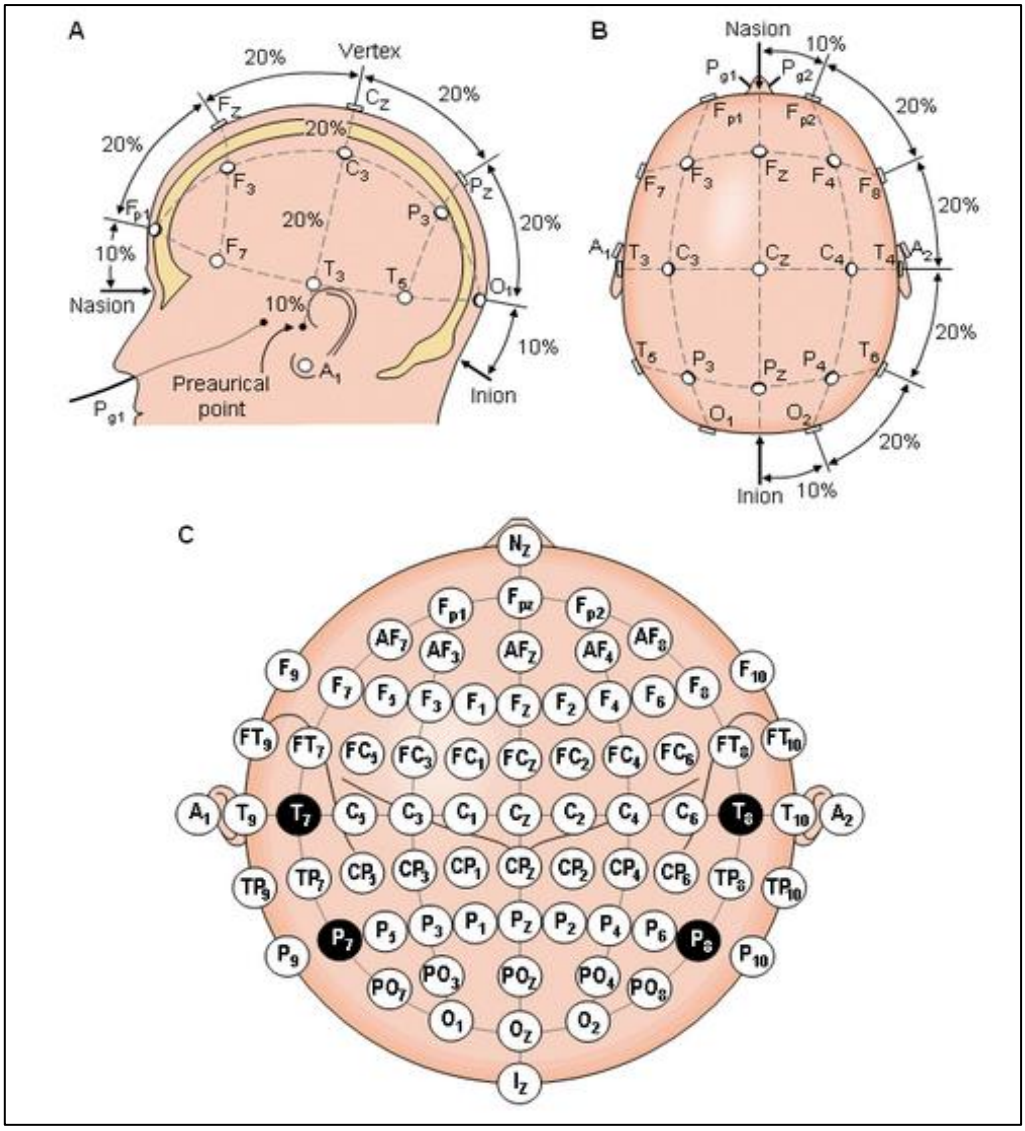


FIGURE 10 : THE INTERNATIONAL 10-20 SYSTEM AS SEEN FROM LEFT(A) AND ABOVE THE HEAD(B). A IS THE EAR LOBE, C IS CENTRAL, PG. IS NASOPHARYNGEAL, P IS PARIETAL, F IS FRONTAL, F_P IS FRONTAL POLAR AND O IS OCCIPITAL.

3.1.1 AMPLIFIER CIRCUIT

The amplifier circuit is divided into four stages:

i. Instrumentation amplifier stage
ii. Notch filter
iii. Low pass filter
iv. Amplification stage
v. Clamping

3.1.1.1 INSTRUMENTATION AMPLIFIER STAGE

The reason to use INA128 stage is that this provides high gain with low noise.

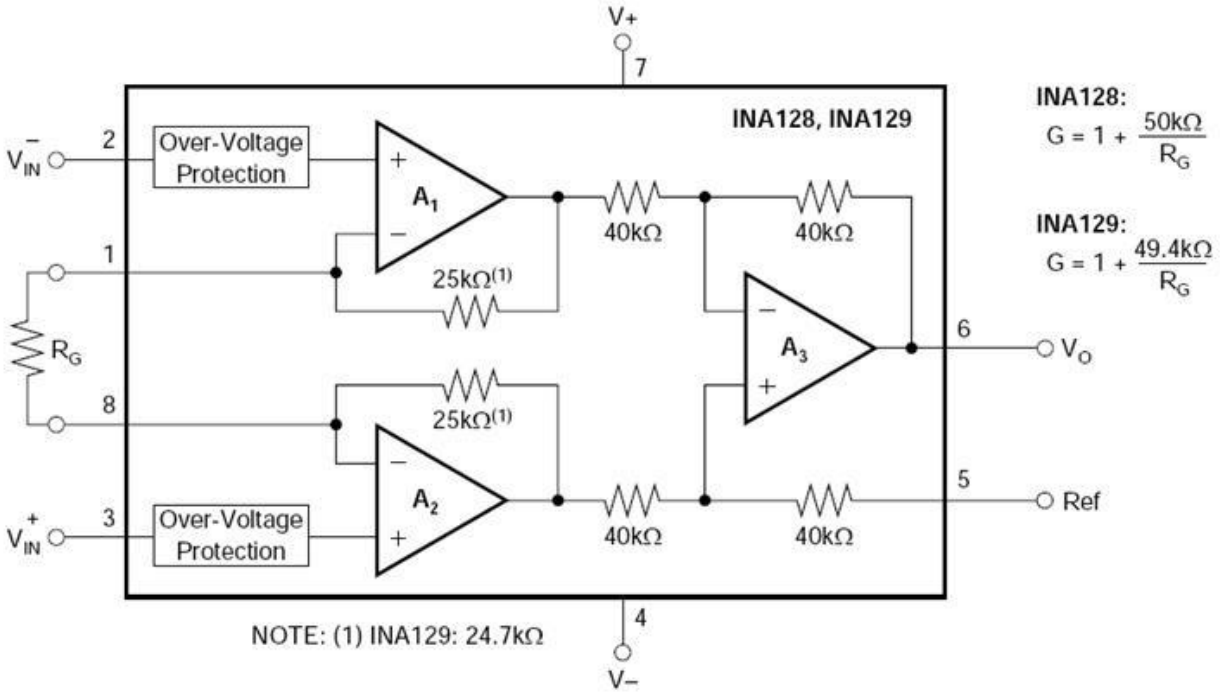


FIGURE 11 : INA128 GAIN CALCULATION

INA128 can provide the gain up to 10,000 based upon the value of resistor used.

In the circuit we have used 470 ohms resistor to have a gain of 100 approximately, 106 to be precise for subsequent stages.

This step is followed by notch filter to reduce 50Hz noise.

Simulation Result:

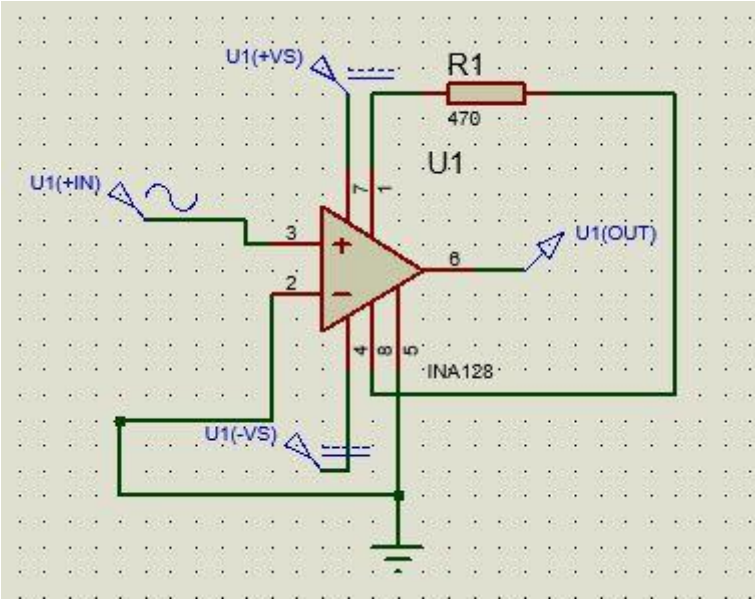


FIGURE 12 : INA128 SCHEMATIC

Analog Analysis

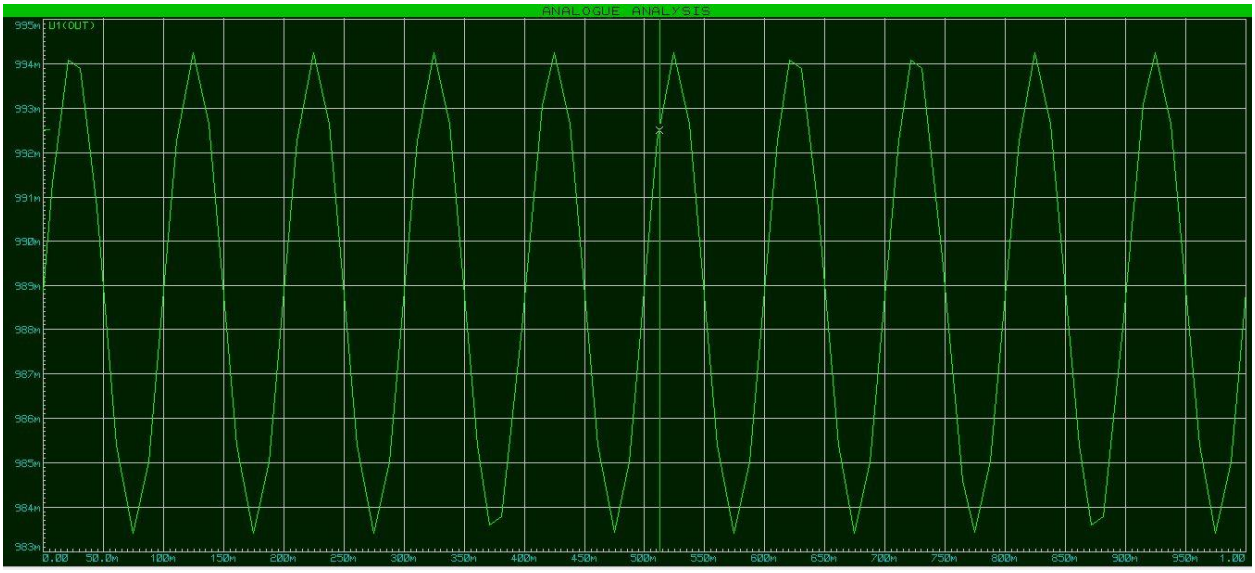


FIGURE 13 : TIME DOMAIN RESPONSE OF THE INSTRUMENTATION AMPLIFIER STAGE

The currents create different potentials at different parts of the body, which are sensed by electrodes on the skin surface via biological transducers made of metals and salt. A typical electric potential is a 0.5- to 1.5-mV AC signal with a bandwidth of 0.05 to 100 Hz and sometimes up to 1 kHz. This signal is superimposed by a large electrode DC offset potential of ±500 mV and a large common-mode voltage of up to 1.5 V. The common-mode voltage comprises two parts: 50- to 60-Hz interference and DC electrode offset potential.

To overcome this DC offset the circuit had to be modified. An inverting low pass filter is placed at the output of the instrumentation amplifier whose output is fed back into the reference pin of the IC. This reduces the effective DC offset to 0.

3.1.1.2 MODIFIED INSTRUMENTATION AMPLIFIER STAGE:

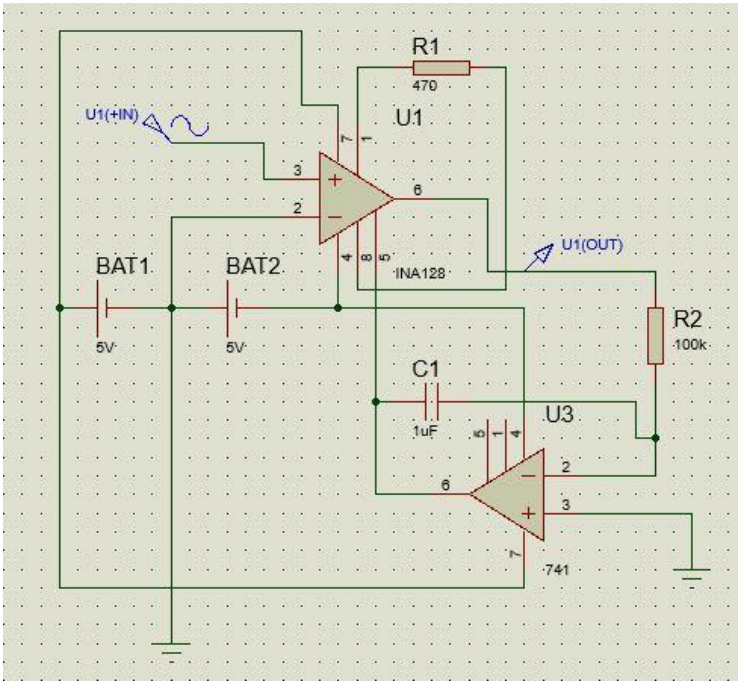


FIGURE 14 : MODIFIED INSTRUMENTATION AMPLIFIER STAGE WITH AUTOMATIC REFERENCE ADJUSTMENT TO REMOVE DC OFFSET VOLTAGE AT THE OUTPUT

Analog Analysis

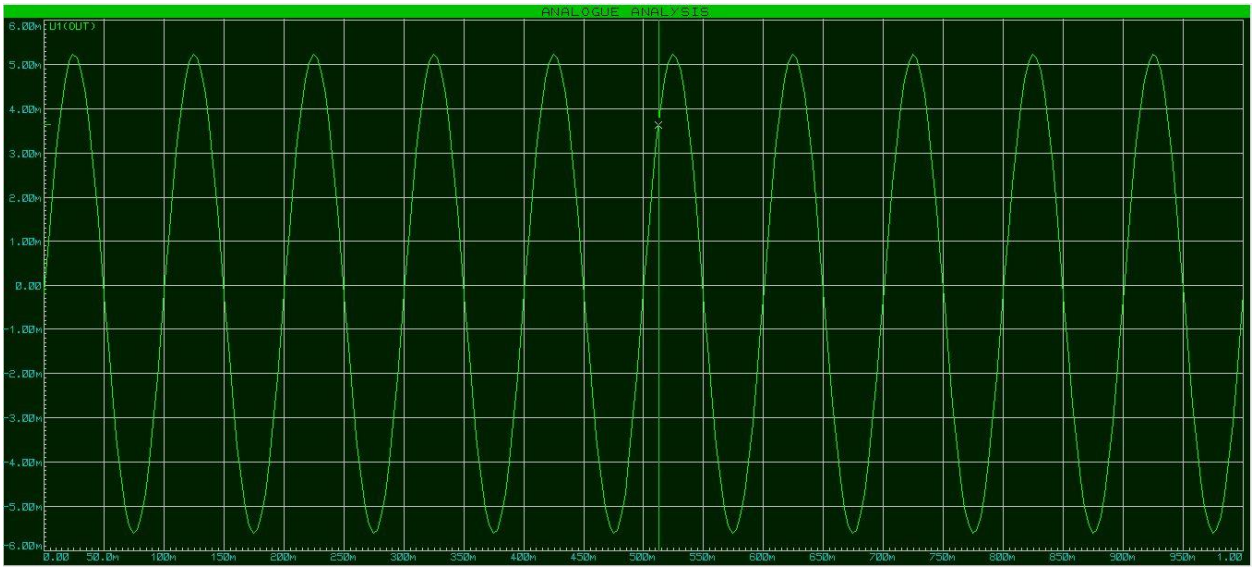


FIGURE 15 : TIME DOMAIN ANALYSIS OF THE MODIFIED INSTRUMENTATION STAGE

3.1.1.3 NOTCH FILTER:

The following circuit was constructed using Op-Amp 741C to decrease any noise in the signal at 50Hz frequency. 50Hz noise is induced due to the main power supply and components used.

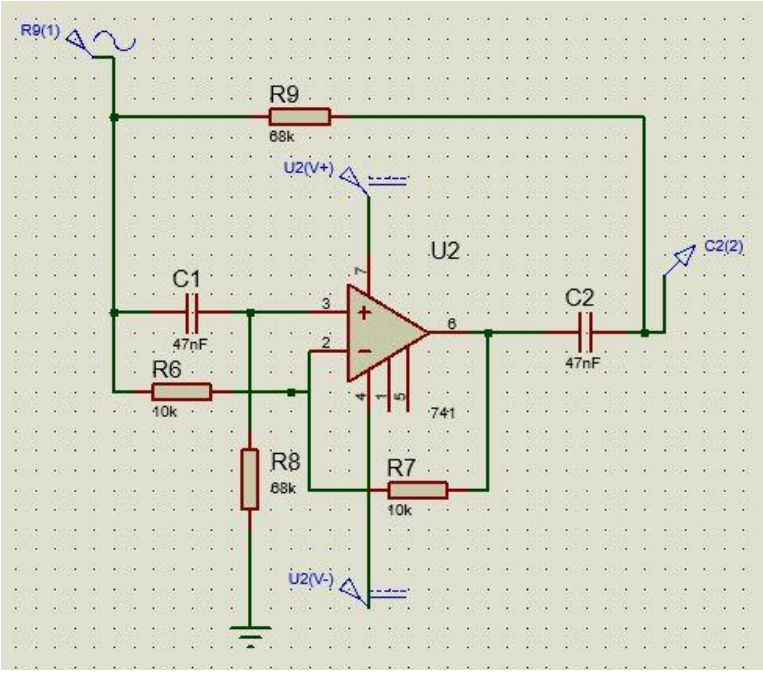


FIGURE 16 : 50 HZ NOTCH FILTER SCHEMATIC

Calculation and Formulas:

$$\frac{Vout}{Vin} = \left(1 - \frac{f}{f_c}\right)^2 \Big/ \left(1 - \frac{f}{f_c}\right)^2 + j\frac{f}{Qf_c}$$

$$f_c = \frac{1}{2\pi RC}$$

For the circuit we used values of capacitances and resistances at fc=50Hz.

Response of Notch filter:

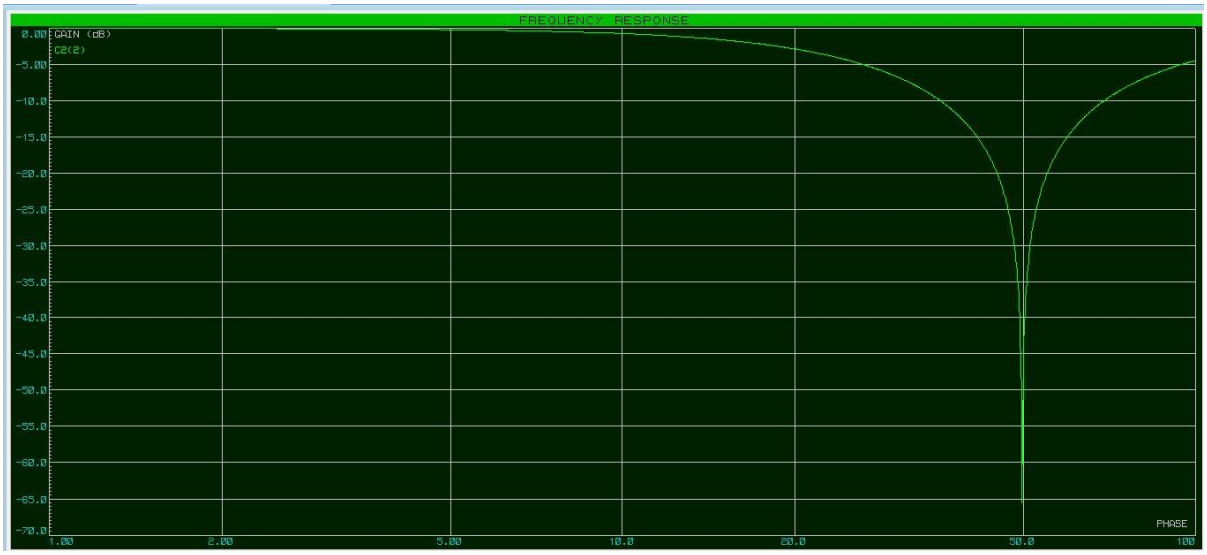


FIGURE 17 : FREQUENCY DOMAIN ANALYSIS OF THE NOTCH FILTER STAGE

3.1.1.4 LOW PASS FILTER

This filter is used to remove any noises above 30Hz of frequency, as frequency of signal from brain ranges from 8-30 Hz.

We are using an active Butterworth filter because we need to amplify mV signals but a passive filter would have attenuated the signal and we would not have got any usable output. Op-Amp is used in a non-inverting configuration in this circuit.

For the circuit, second order low pass filter circuit was used constructed with the help of op amp 741

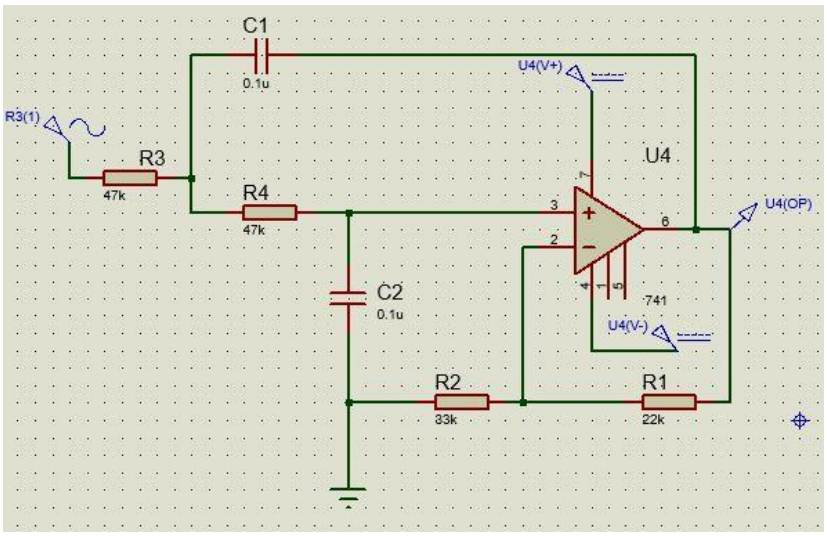


FIGURE 18 : SCHEMATIC FOR LOW PASS FILTER

Formulas and Calculation:

$$A_v = 1 + \frac{R_2}{R_1}$$

$$f_c = \frac{1}{2\pi\sqrt{R_3 R_4 C_1 C_2}}$$

For Butterworth filter Av = 1.586

Therefore, R=22kΩ and R1

R3 = R4 = 47KΩ

C1 = C2 = 0.1uF

Cutoff frequency = 33.86 Hz

Simulation Result:

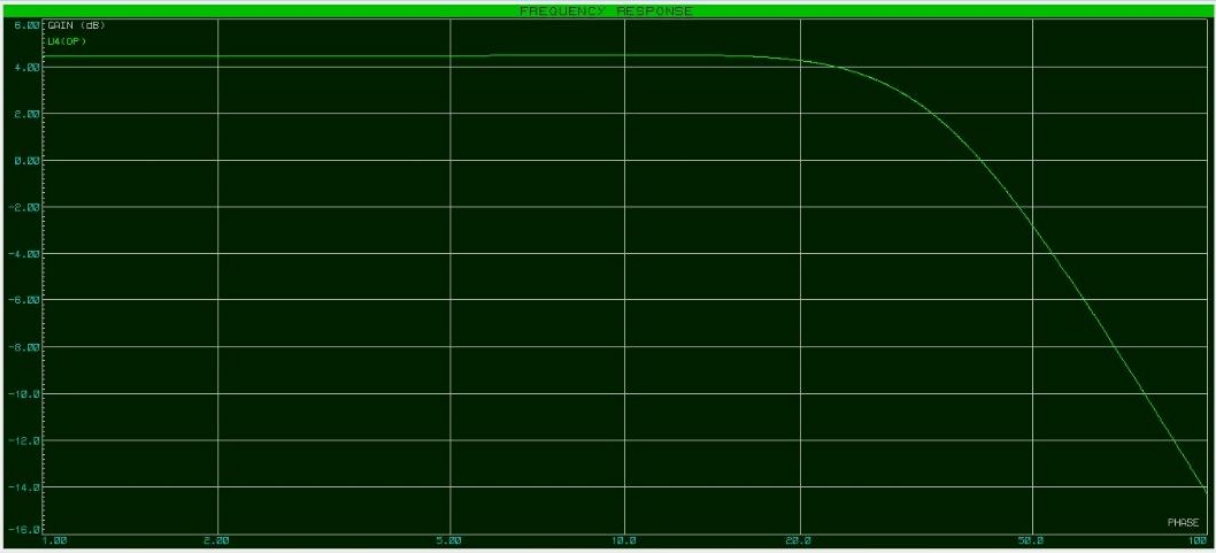


FIGURE 19 : FREQUENCY DOMAIN RESPONSE OF THE LOW PASS FILTER

Output on Oscilloscope:

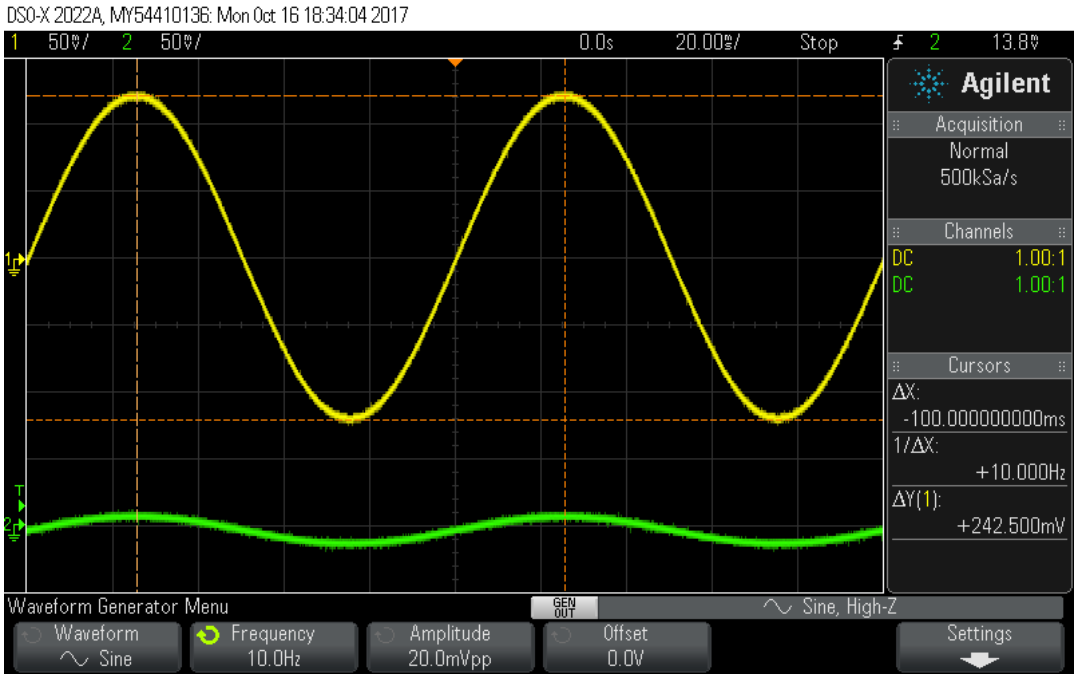


FIGURE 20 : LOW PASS FILTER TIME DOMAIN RESPONSE FOR 10 HZ SIGNAL

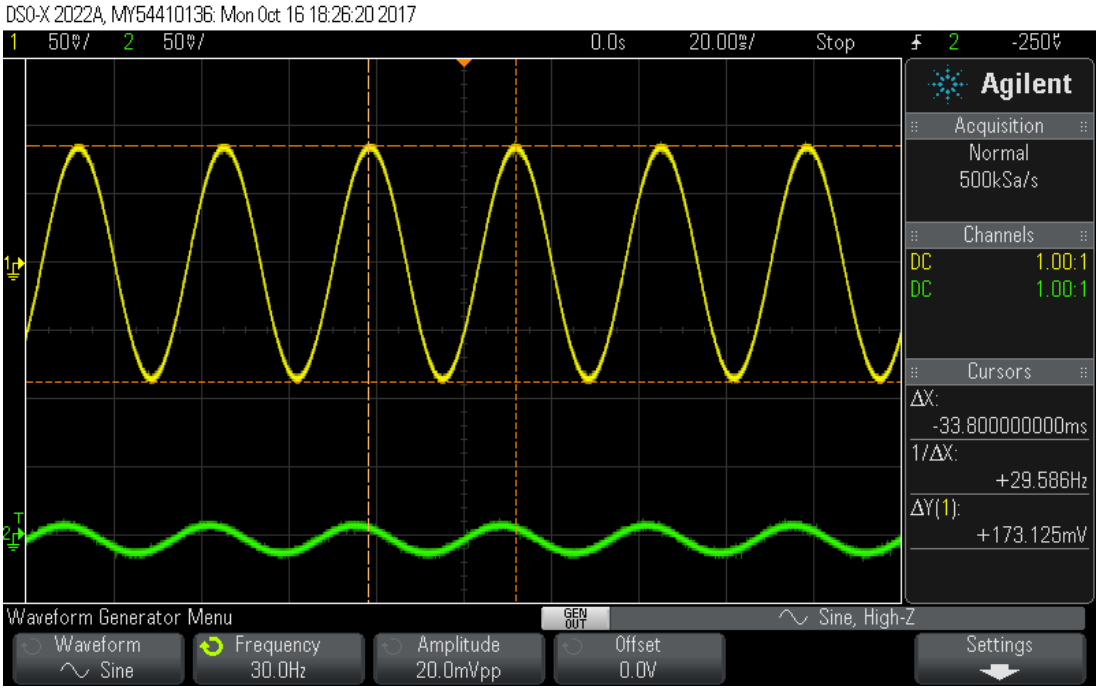


FIGURE 21 : LOW PASS FILTER TIME DOMAIN RESPONSE FOR 30 HZ SIGNAL

3.1.1.5 POST-AMPLIFICATION STAGE

In this stage, op amp 741 was used to provide gain of 60 to the signal obtained from the low pass filter.

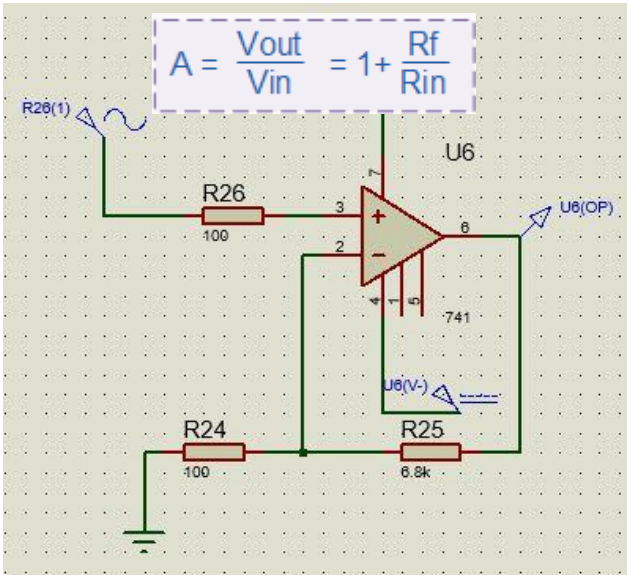


FIGURE 22 : AMPLIFICATION STAGE SCHEMATIC

$$Rf = 6.8k\Omega$$

$$R1 = 100\Omega$$

$$A = 69$$

Simulation Result:

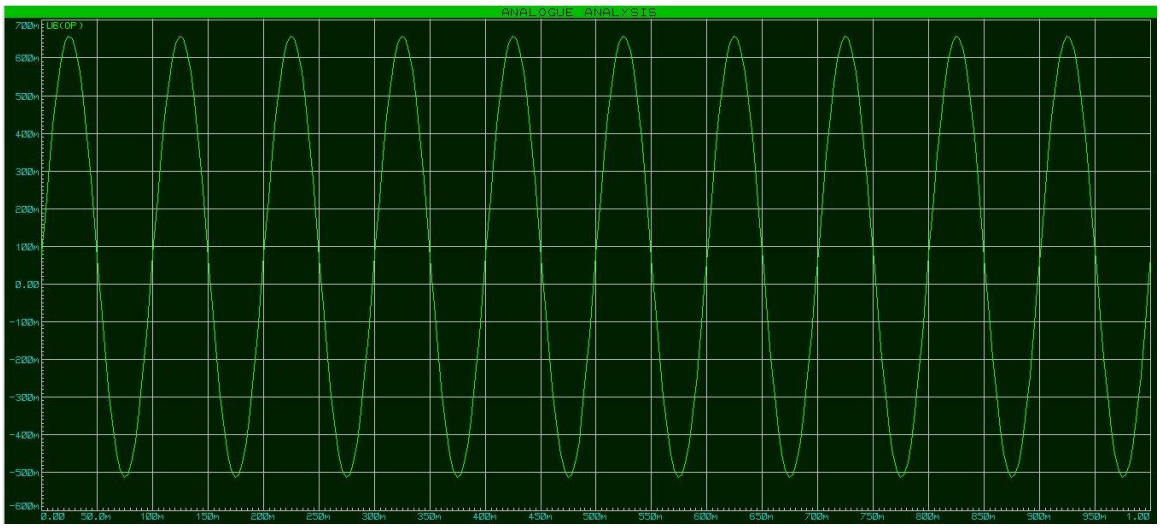


FIGURE 23 : TIME DOMAIN RESPONSE OF POST-AMPLIFIER STAGE

3.1.1.6 LEVEL SHIFTER STAGE

The amplification stage results in an output range from 500mv to -500mv. STM32F1 takes an input ranging from 0 to 3.3V. So, the output needs to be shifted about 1.6 V. In order for the output to not exceed the range 0 and 3.3 V, a diode is used to limit it to 0 V and Zener diode with reverse voltage of 3.3V is used to limit the max output to 3.3V.

A summing amplifier is used to clamp the output to 1.6V offset.

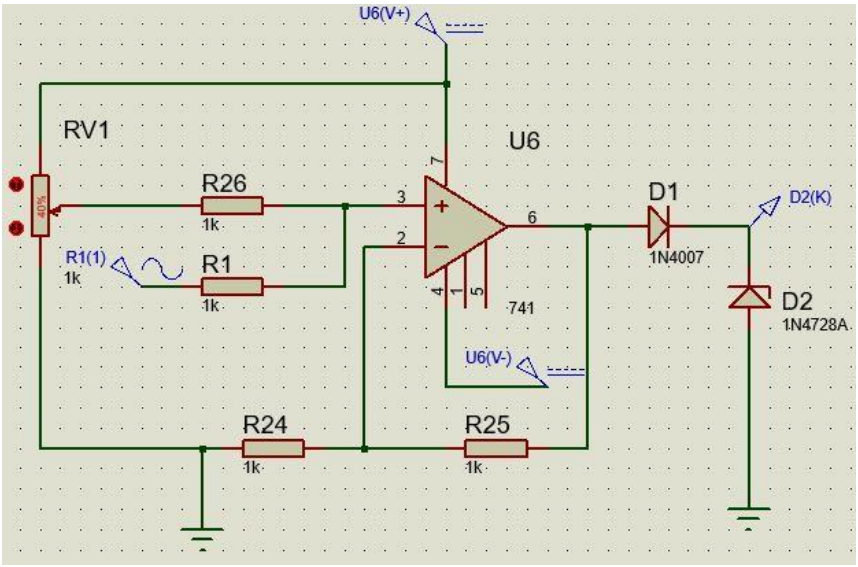


FIGURE 24 : LEVEL SHIFTER AND CLIPPING STAGE SCHEMATIC

Simulation:

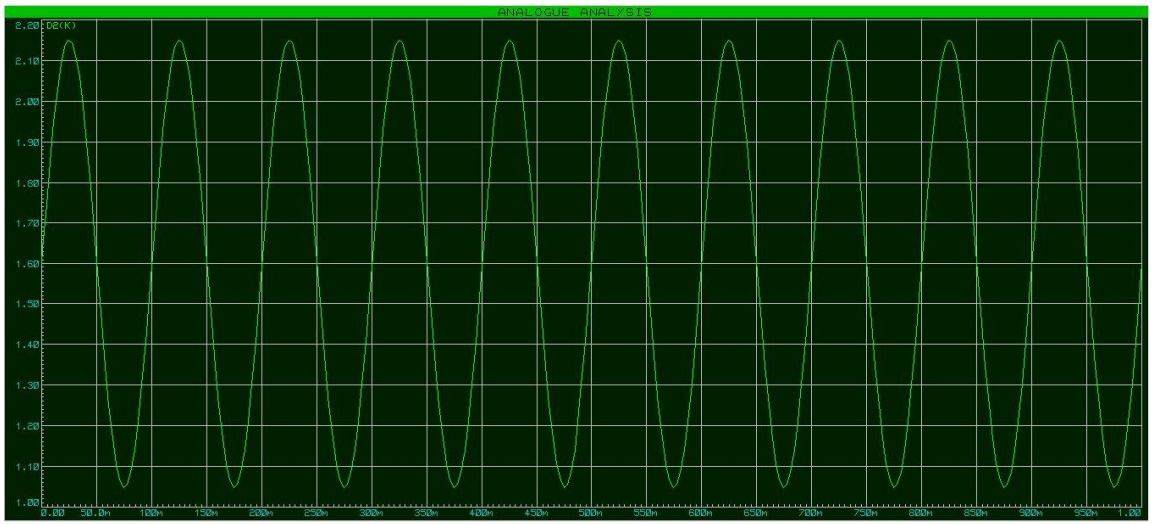


FIGURE 25 : LEVEL SHIFTING TIME DOMAIN RESPONSE

3.2 CASCADING ALL STAGES

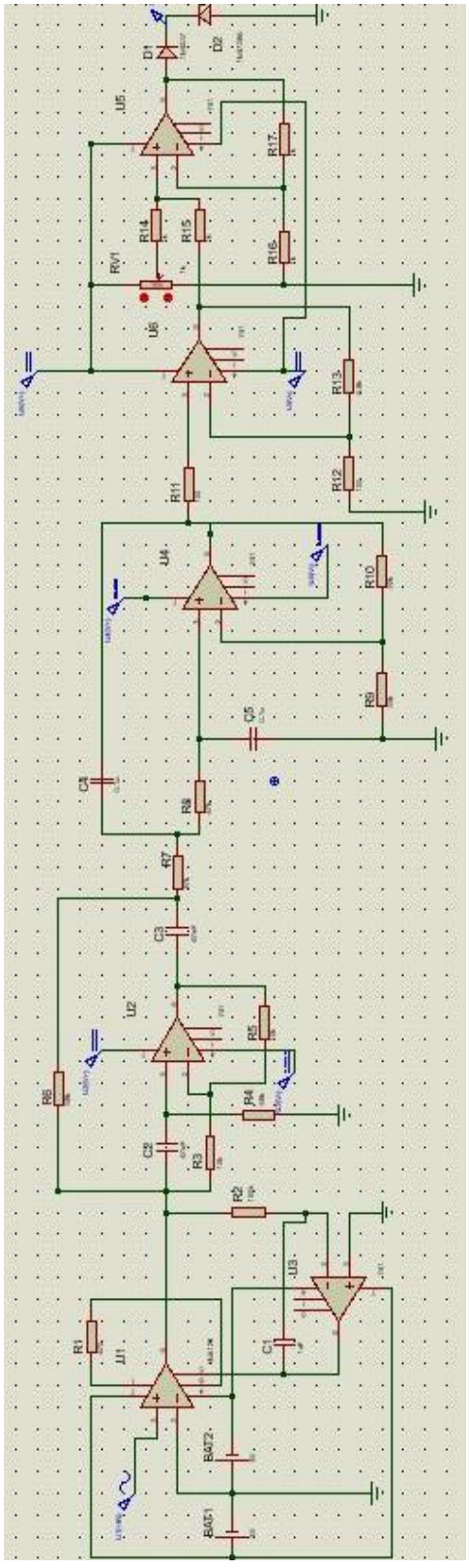


FIGURE 26 : CASCADED SCHEMATIC OF ALL THE STAGES

Frequency Response

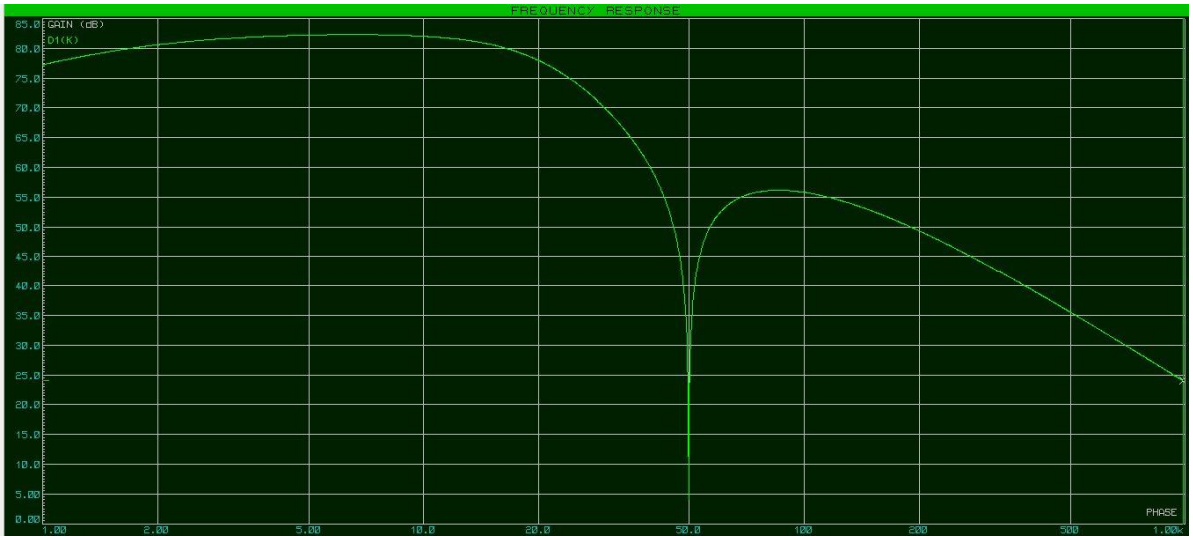


FIGURE 27 : FREQUENCY DOMAIN RESPONSE OF THE CASCADED SCHEMATIC

AC Sweep Analysis

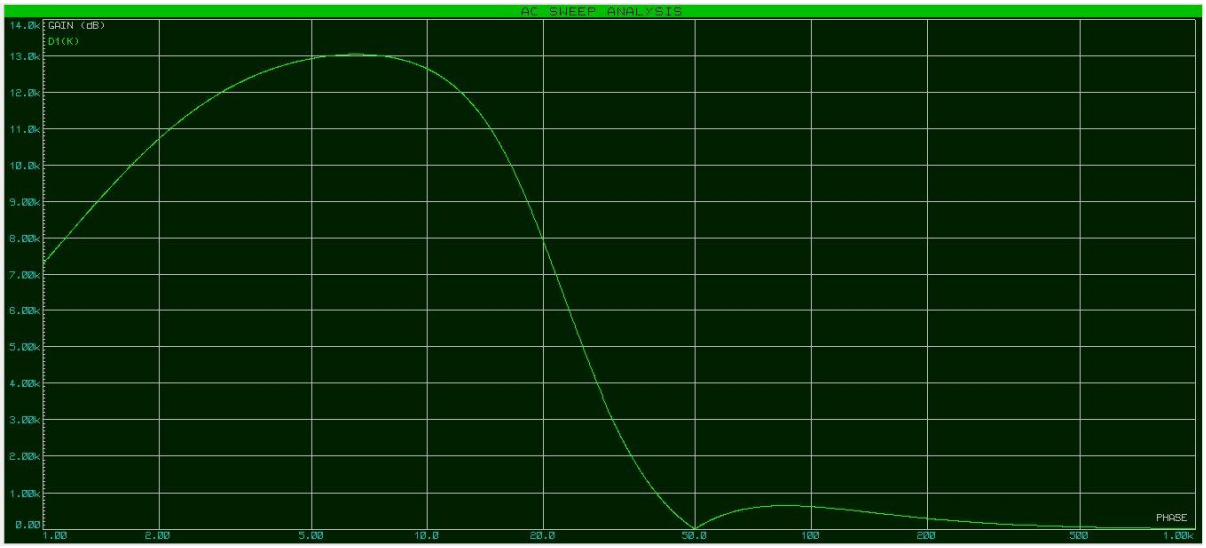


FIGURE 28 : AC FREQUENCY SWEEP ANALYSIS OF THE CASCADED SCHEMATIC

3.3 OUTPUT ON OSCILLOSCOPE

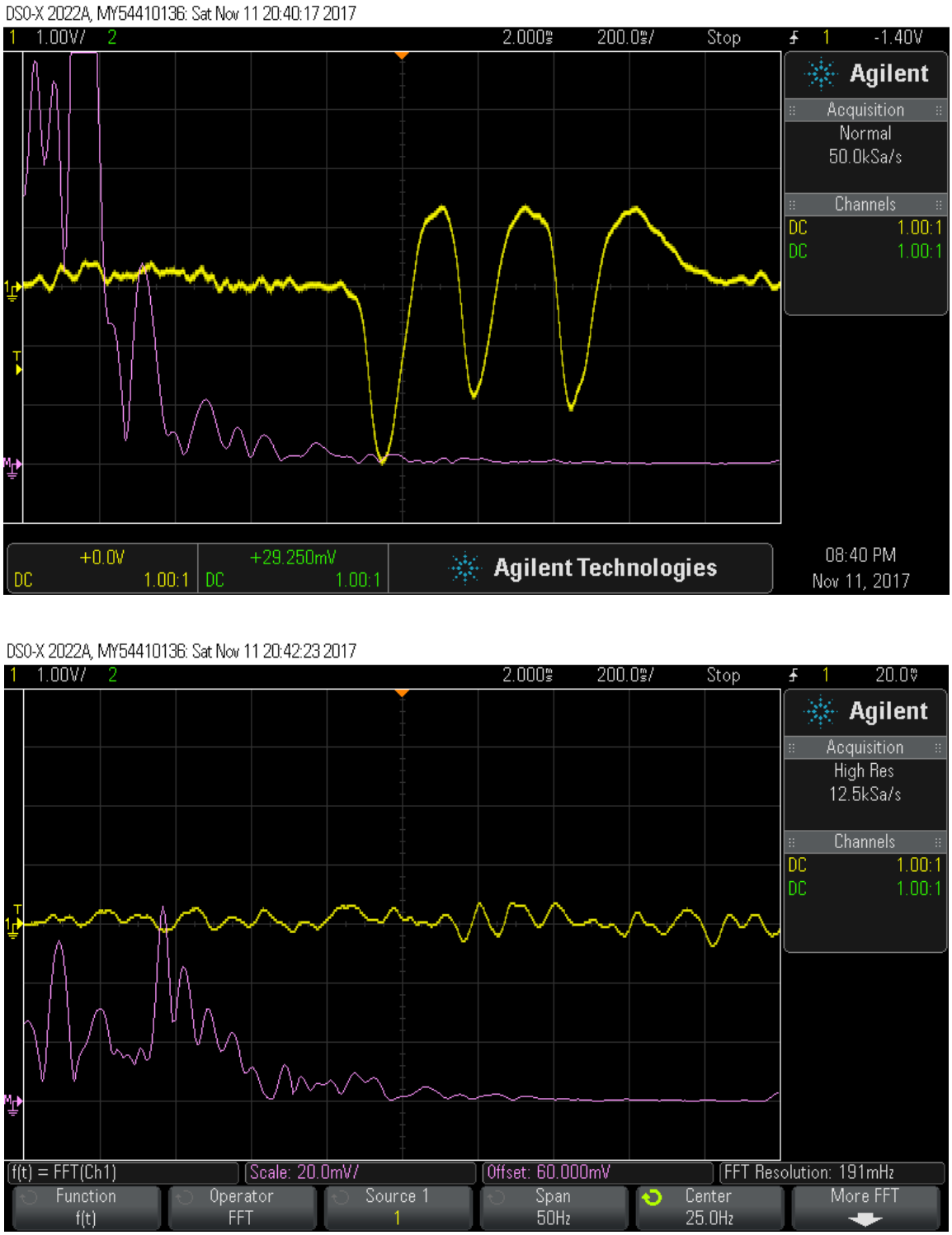


FIGURE 29 : OSCILLOSCOPE OUTPUT, YELLOW LINE REPRESENTS THE TIME DOMAIN SIGNAL AND THE VIOLET LINE REPRESENTS THE FREQUENCY DOMAIN RESPONSE

4 ADC SAMPLING AND PROCESSING STAGE

The analog data from the first stage is captured with the help of an ADC. For this purpose, STM32 ARM M0 based microcontroller is used. The part number is STM32F103C6T8. This microcontroller provides a 10-channel general-purpose ADC which is 12-bit in resolution. Thus, the samples captured are 4-times more resolved as compared to other alternative microcontrollers like the ATMega32 or ATMega16 series.

The ADC channel 0 and channel 1 are bound to GPIO using the HAL or Hardware Abstraction Library provided along with the SDK (Software Development Kit). Additionally, GPIO is configured as analog input which automatically selects analog coupling mode. This enables a separate GPIO channel which can be connected to the ADC with the help of the APB or the Advanced Peripheral Bus.

The firmware is programmed in a multi-rate mode, thus allowing us to capture various frequency components. The sampling frequency is derived from the expression

$$sampling\ period = 1 + (multiplier\ \times 4)$$

The value $multiplier$ is an 8-bit number and the sampling period can range from 1 ms to 1021 ms.

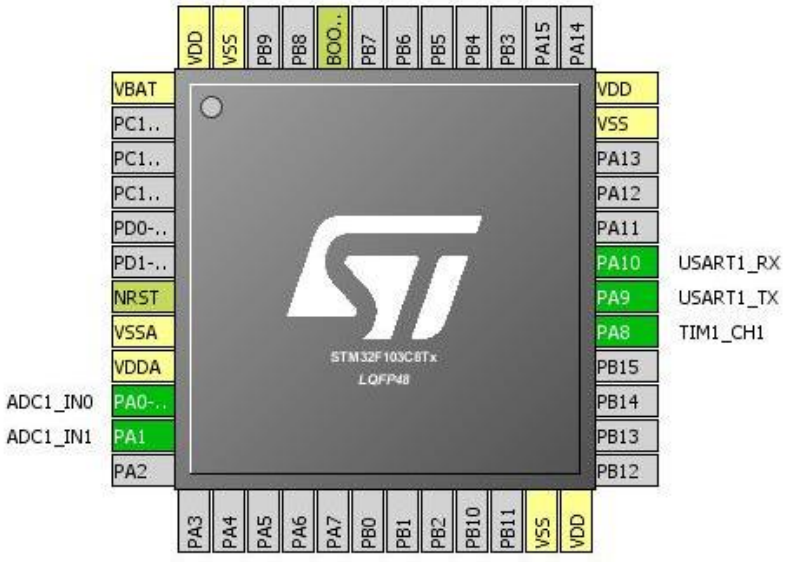


FIGURE 30 : SCHEMATIC AND PIN LAYOUT OF STM32F1 MICROCONTROLLER

As apparent from the schematic diagram the pins PA0 and PA1 are used as the inputs to ADC channels 0 and 1 and pins PA10 and PA9 are used for USART transmission. The GPIO PA8 is bound to a timer peripheral used to generate the system clock frequency of 1kHz.

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
10	PA0-WKUP	I/O	ADC1_IN0	
11	PA1	I/O	ADC1_IN1	
23	VSS	Power		
24	VDD	Power		
29	PA8	I/O	TIM1_CH1	
30	PA9	I/O	USART1_TX	
31	PA10	I/O	USART1_RX	
35	VSS	Power		
36	VDD	Power		
44	BOOT0	Boot		
47	VSS	Power		
48	VDD	Power		

FIGURE 31 : PIN CONFIGURATION OF STM32F1 FOR THIS PROJECT

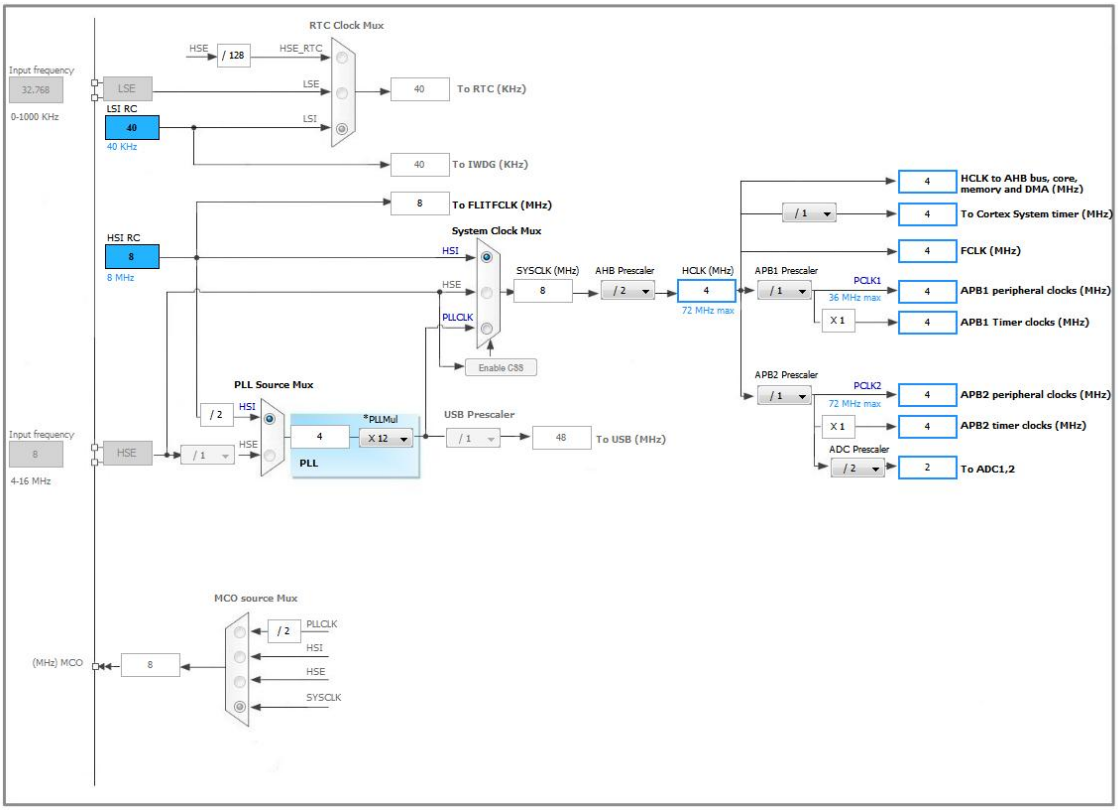


FIGURE 32 : CLOCK TREE CONFIGURATION FOR STM32

4.1 ADC PARAMETERS

ADCs_Common_Settings:	
Mode	Independent mode
ADC_Settings:	
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	**Enabled** *
Discontinuous Conversion Mode	Disabled
ADC_Regular_ConversionMode:	
Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
Rank	1
Channel	Channel 0
Sampling Time	1.5 Cycles
ADC_Injected_ConversionMode:	
Number Of Conversions	0
WatchDog:	
Enable Analog WatchDog Mode	false

FIGURE 33 : PARAMETERS FOR ADC

The ADC is being used in Independent mode, which runs all the onboard ADCs independent of each other. Continuous conversion mode is enabled which allows the ADC to continuously scan a number of samples and maintain a FIFO for the samples. The sampling time is set to 1.5 cycles i.e. 1.5 times the time period of the system clock for ADC peripheral which is set to 4 MHz.

```
    sConfig.Rank = 1;
    sConfig.SamplingTime = ADC_SAMPLETIME_1CYCLE_5;
    int i;
    for (i=0;i<adc_no_of_conversions;i++) {
      if (HAL_ADC_Init(&hadc1) != HAL_OK)
      {
        _Error_Handler(__FILE__, __LINE__);
      }
      sConfig.Channel = adc_channels_to_scan[i];
      if (HAL_ADC_ConfigChannel(&hadc1, &sConfig) != HAL_OK)
      {
        _Error_Handler(__FILE__, __LINE__);
      }

      HAL_ADC_Start(&hadc1);
```

```
      if (HAL_ADC_PollForConversion(&hadc1, 1000) == HAL_OK)
      {
          aADCxConvertedValues[i] = HAL_ADC_GetValue(&hadc1);
      }
      HAL_Delay(adc_conversion_period/adc_no_of_conversions);
      // ADC Deinit for stable readings of VRefInt
      HAL_ADC_DeInit(&hadc1);
    }
    ch0_read = (uint32_t)((1212.0 * ((double)aADCxConvertedValues[0]/ 1000.0) * 1250.0)
/ aADCxConvertedValues[2]);
    ch1_read = (uint32_t)((1212.0 * ((double)aADCxConvertedValues[1]/ 1000.0) * 1250.0)
/ aADCxConvertedValues[2]);

    if (ch0_read>4095) {ch0_read = 4095;}
    if (ch1_read>4095) {ch1_read = 4095;}

    if (ch1_read<1000) {
      HAL_GPIO_TogglePin(GPIOC, GPIO_PIN_13);
    }

    uart_tx_buffer[1] = ch0_read >> 8;
    uart_tx_buffer[2] = ch0_read;
    uart_tx_buffer[4] = ch1_read >> 8;
    uart_tx_buffer[5] = ch1_read;

    HAL_UART_Transmit(&huart1, &uart_tx_buffer[0], UART_TX_BUFFER_SIZE, 1000);
    HAL_UART_Receive_IT(&huart1, &uart_rx_buffer, 1);
```

FIGURE 34 : CODE FOR ADC SAMPLING FIRMWARE

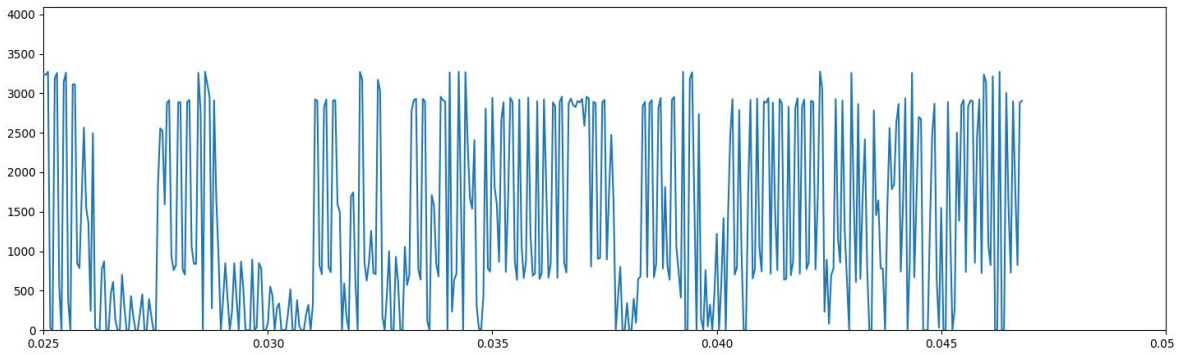


FIGURE 35 : TIME DOMAIN PLOT OF THE SAMPLES OBTAINED FROM THE ADC

5 CONCLUSION

The project can be divided into three modules namely Bio Amplifier, Signal acquisition and Robot control respectively. A new design of Bio Amplifier has been developed and tested using DSO and signal generator.

The design has been validated using LabVIEW. First order RC filter is employed, 4 stage OP-Amp circuit is used for designing Bio Amplifier. The circuit provides a gain of about 1000 without any distortion or noise.

6 FUTURE SCOPE

The aim of our project is to integrate Neural Networks and Machine Learning systems to identify artifacts in the input waveform. The artifacts will be extracted from various time-domain and frequency domain parameters like rise-time, time-difference between peaks, the frequency of occurrence between peaks and troughs, etc. The FFT of frequency domain signal are also analyzed. This data will be used to train a set of neural networks to identify or classify the incoming waveform to a particular class of thoughts.

With that said, the bioamplifier apparatus itself has much scope for advancement and improvement, like

- Making the bio amplifier with up to 16 or 24 channels
- Using active electrode cap for signal acquisition
- Implementing a real-life application – Anesthesia
- Controlling the robot with a wireless connection
- Improving the filter design by replacing the current design with a higher order filter

7 APPENDIX

INA12x Precision, Low Power Instrumentation Amplifiers

1 Features

- Low Offset Voltage: 50 µV Maximum
- Low Drift: 0.5 µV/°C Maximum
- Low Input Bias Current: 5 nA Maximum
- High CMR: 120 dB minimum
- Inputs Protected to ±40 V
- Wide Supply Range: ±2.25 V to ±18 V
- Low Quiescent Current: 700 µA
- 8-PIN Plastic Dip, SO-8

2 Applications

- Bridge Amplifier
- Thermocouple Amplifier
- RTD Sensor Amplifier
- Medical Instrumentation
- Data Acquisition

3 Description

The INA128 and INA129 are low-power, general purpose instrumentation amplifiers offering excellent accuracy. The versatile 3-op amp design and small size make these amplifiers ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (200 kHz at G = 100).

A single external resistor sets any gain from 1 to 10,000. The INA128 provides an industry-standard gain equation; the INA129 gain equation is compatible with the AD620.

The INA12x is laser-trimmed for very low offset voltage (50 µV), drift (0.5 µV/°C) and high common-mode rejection (120 dB at G ≥ 100). The INA12x operates with power supplies as low as ±2.25 V, and quiescent current is only 700 µA, ideal for battery-operated systems. Internal input protection can withstand up to ±40 V without damage.

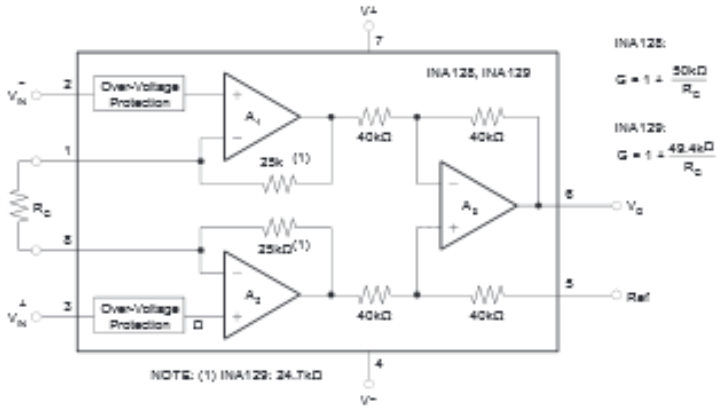
The INA12x is available in 8-pin plastic DIP and SO-8 surface-mount packages, specified for the –40°C to 85°C temperature range. The INA128 is also available in a dual configuration, the INA2128.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA128 INA129	SOIC (8)	3.91 mm × 4.9 mm
	PDIP (8)	6.35 mm × 9.81 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



5 Pin Configuration and Functions

D and P Packages
8 Pin SOIC and PDIP
Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
REF	5	I	Reference input. This pin must be driven by low impedance or connected to ground.
R_G	1,8	—	Gain setting pin. For gains greater than 1, place a gain resistor between pin 1 and pin 8.
V-	4	—	Negative supply
V+	7	—	Positive supply
V_{IN-}	2	I	Negative input
V_{IN+}	3	I	Positive input
V_O	6	I	Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

		MIN	MAX	UNIT
	Supply voltage		±18	V
	Analog input voltage		±40	V
	Output short circuit (to ground)		continuous	
	Operating temperature	−40	125	°C
	Junction temperature		150	°C
	Lead temperature (soldering, 10s)		300	°C
T_{stg}	Storage temperature	−55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±50	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V power supply	±2.25	±15	±18	V
Input common-mode voltage range for V_O = 0	V − +2 V		V + −2 V	
T_A operating temperature INA128-HT	−55		175	°C
T_A operating temperature INA129-HT	−55		210	°C

6.4 Thermal Information

THERMAL METRIC(1)		INA12x		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110	46.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57	34.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54	23.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	11	11.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	53	23.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At TA = 25°C, VS = ±15 V, RL = 10 kΩ, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
Offset Voltage, RTI	Initial	T_A = 25°C	INA128P, U INA129P, U		±10±100/G	±50±500/G	µV
			INA128PA, UA INA129PA, UA		±25±100/G	±125±1000/G	
	vs Temperature	T_A = T_{MIN} to T_{MAX}	INA128P, U INA129P, U		±0.2±2/G	±0.5±5/G	µV/°C
			INA128PA, UA INA129PA, UA		±0.2±5/G	±1±20/G	
	vs Power Supply	V_S = ±2.25 V to ±18 V	INA128P, U INA129P, U		±0.2±20/G	±1±100/G	µV/V
			INA128PA, UA INA129PA, UA			±2±200/G	
	Long-Term Stability				±0.1±3/g		µV/mo
Impedance	Differential				10^{10} || 2		Ω || pF
	Common-Mode				10^{11} || 9		
Common-Mode Voltage Range(1)		V_O = 0 V		[V+] − 2	(V+) − 1.4		V
				[V−] + 2	(V−) + 1.7		
Same-Side Voltage						±40	V

(1) Input common-mode range varies with output voltage - see Typical Characteristics.

Electrical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Common-Mode Rejection		V_{CM} = ±13 V, ΔR_S = 1 kΩ	G = 1	INA128P, U INA129P, U	80	86		dB
				INA128PA, UA INA129PA, UA	73			
			G = 10	INA128P, U INA129P, U	100	106		
				INA128PA, UA INA129PA, UA	93			
			G = 100	INA128P, U INA129P, U	120	125		
				INA128PA, UA INA129PA, UA	110			
			G = 1000	INA128P, U INA129P, U	120	130		
				INA128PA, UA INA129PA, UA	110			
Bias Current		INA128P, U INA129P, U				±2	±5	nA
		INA128PA, UA INA129PA, UA					±10	
Bias Current vs Temperature						±30		pA/°C
Offset Current		INA128P, U INA129P, U				±1	±5	nA
		INA128PA, UA INA129PA, UA					±10	
Offset Current vs Temperature						±30		pA/°C
Noise Voltage, RTI	f = 10 Hz	G = 1000, R_S = 0Ω				10		nV/√Hz
	f = 100 Hz					8		
	f = 1 kHz					8		
	f_B = 0.1 Hz to 10 Hz					0.2		μV_{pp}
Noise Current	f = 10 Hz					0.9		pA/√Hz
	f = 1 kHz					0.3		
	P_B = 0.1 Hz to 10 Hz					30		pA_{pp}
GAIN								
Gain Equation	INA128					1 + (50 kΩ/R_G)		V/V
	INA129					1 + (49.4 kΩ/R_G)		
Range of Gain					1		10000	V/V
Gain Error		G = 1		INA128P, U INA129P, U		±0.01%	±0.024%	
				INA128PA, UA INA129PA, UA			±0.01%	
		G = 10		INA128P, U INA129P, U		±0.02%	±0.4%	
				INA128PA, UA INA129PA, UA			±0.5%	
		G = 100		INA128P, U INA129P, U		±0.05%	±0.5%	
				INA128PA, UA INA129PA, UA			±0.7%	
		G = 1000		INA128P, U INA129P, U		±0.5%	±1%	
				INA128PA, UA INA129PA, UA			±2%	

Electrical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Gain vs Temperature[3]		G = 1			±1	±10	ppm/°C
		50-kΩ (or 49.4-kΩ) Resistance[2][3]			±25	±100	
Nonlinearity		V_O = ±13.6 V, G = 1	INA128P, U INA129P, U		±0.0001	±0.001	% of FSR
			INA128PA, UA INA129PA, UA			±0.002	
		G = 10	INA128P, U INA129P, U		±0.0003	±0.002	
			INA128PA, UA INA129PA, UA			±0.004	
		G = 100	INA128P, U INA129P, U		±0.0005	±0.002	
			INA128PA, UA INA129PA, UA			±0.004	
		G = 1000			±0.001		
[4]OUTPUT							
Voltage	Positive	R_L = 10 kΩ		(V+) – 1.4	(V+) – 0.9		V
	Negative	R_L = 10 kΩ		(V–) + 1.4	(V–) + 0.8		
Load Capacitance Stability					1000		pF
Short Circuit Current					6/–15		mA
FREQUENCY RESPONSE							
Bandwidth, –3 dB		G = 1			1.2		MHz
		G = 10			700		kHz
		G = 100			200		
		G = 1000			20		
Slew Rate		V_O = ±10 V, G = 10			4		V/µs
Settling Time, 0.01%		G = 1			7		µs
		G = 10			7		
		G = 100			9		
		G = 1000			50		
Overload Recovery		50% Overdrive			4		µs
POWER SUPPLY							
Voltage Range				±2.25	±15	±18	V
Current, TOTAL		V_{IN} = 0 V			±700	±750	µA
TEMPERATURE RANGE							
Specification				–40		85	°C
Operating				–40		125	°C

(2) Specified by wafer test.
(3) Temperature coefficient of the 50 kΩ (or 49.4 kΩ) term in the gain equation.
(4) Nonlinearity measurements in G = 1000 are dominated by noise. Typical non-linearity is ±0.001%.

LM741 Operational Amplifier

1 Features

- Overload Protection on the Input and Output
- No Latch-Up When the Common-Mode Range is Exceeded

2 Applications

- Comparators
- Multivibrators
- DC Amplifiers
- Summing Amplifiers
- Integrator or Differentiators
- Active Filters

3 Description

The LM741 series are general-purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439, and 748 in most applications.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common-mode range is exceeded, as well as freedom from oscillations.

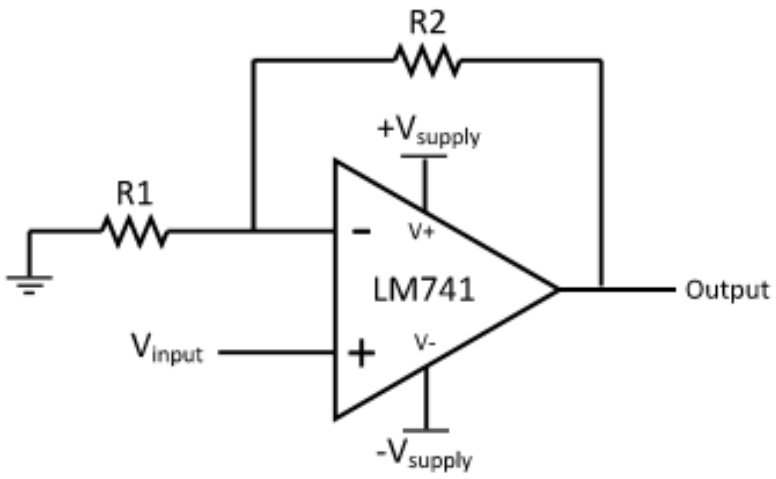
The LM741C is identical to the LM741 and LM741A except that the LM741C has their performance ensured over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM741	TO-99 (8)	9.08 mm × 9.08 mm
	CDIP (8)	10.16 mm × 6.502 mm
	PDIP (8)	9.81 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2][3]

		MIN	MAX	UNIT
Supply voltage	LM741, LM741A		±22	V
	LM741C		±18	
Power dissipation [4]			500	mW
Differential input voltage			±30	V
Input voltage [5]			±15	V
Output short circuit duration		Continuous		
Operating temperature	LM741, LM741A	−55	125	°C
	LM741C	0	70	
Junction temperature	LM741, LM741A		150	°C
	LM741C		100	
Soldering information	PDIP package (10 seconds)		260	°C
	CDIP or TO-99 package (10 seconds)		300	°C
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For military specifications see RETS741X for LM741 and RETS741AX for LM741A.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(4) For operation at elevated temperatures, these devices must be derated based on thermal resistance, and T_j max. (listed under "Absolute Maximum Ratings"). $T_j = T_A + (\theta_{JA} P_D)$.
(5) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	±400	V

(1) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage (VDD-GND)	LM741, LM741A	±10	±15	±22	V
	LM741C	±10	±15	±18	
Temperature	LM741, LM741A	−55		125	°C
	LM741C	0		70	

6.4 Thermal Information

THERMAL METRIC[1]		LM741			UNIT
		LMC (TO-99)	NAB (CDIP)	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	170	100	100	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

Electrical Characteristics, LM741A[1] (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage swing		V_S = ±20 V	R_L ≥ 10 kΩ	±16			V
			R_L ≥ 2 kΩ	±15			
Output short circuit current		T_A = 25°C		10	25	35	mA
		$T_{AMIN} \le T_A \le T_{AMAX}$		10		40	
Common-mode rejection ratio		$R_S \le 50\ \Omega$, V_{CM} = ±12 V, $T_{AMIN} \le T_A \le T_{AMAX}$		80	95		dB
Supply voltage rejection ratio		V_S = ±20 V to V_S = ±5 V, $R_S \le 50\ \Omega$, $T_{AMIN} \le T_A \le T_{AMAX}$		86	96		dB
Transient response	Rise time	T_A = 25°C, unity gain			0.25	0.8	µs
	Overshoot				6%	20%	
Bandwidth [2]		T_A = 25°C		0.437	1.5		MHz
Slew rate		T_A = 25°C, unity gain		0.3	0.7		V/µs
Power consumption		V_S = ±20 V	T_A = 25°C		80	150	mW
			$T_A = T_{AMIN}$			165	
			$T_A = T_{AMAX}$			135	

(2) Calculated value from: BW (MHz) = 0.35/Rise Time (µs).

6.7 Electrical Characteristics, LM741C[1]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input offset voltage		$R_S \le 10$ kΩ	T_A = 25°C		2	6	mV
			$T_{AMIN} \le T_A \le T_{AMAX}$			7.5	mV
Input offset voltage adjustment range		T_A = 25°C, V_S = ±20 V			±15		mV
Input offset current		T_A = 25°C			20	200	nA
		$T_{AMIN} \le T_A \le T_{AMAX}$				300	
Input bias current		T_A = 25°C			80	500	nA
		$T_{AMIN} \le T_A \le T_{AMAX}$				0.8	µA
Input resistance		T_A = 25°C, V_S = ±20 V		0.3	2		MΩ
Input voltage range		T_A = 25°C		±12	±13		V
Large signal voltage gain		V_S = ±15 V, V_O = ±10 V, R_L ≥ 2 kΩ	T_A = 25°C	20	200		V/mV
			$T_{AMIN} \le T_A \le T_{AMAX}$	15			
Output voltage swing		V_S = ±15 V	R_L ≥ 10 kΩ	±12	±14		V
			R_L ≥ 2 kΩ	±10	±13		
Output short circuit current		T_A = 25°C			25		mA
Common-mode rejection ratio		$R_S \le 10$ kΩ, V_{CM} = ±12 V, $T_{AMIN} \le T_A \le T_{AMAX}$		70	90		dB
Supply voltage rejection ratio		V_S = ±20 V to V_S = ±5 V, $R_S \le 10\ \Omega$, $T_{AMIN} \le T_A \le T_{AMAX}$		77	96		dB
Transient response	Rise time	T_A = 25°C, Unity Gain			0.3		µs
	Overshoot				5%		
Slew rate		T_A = 25°C, Unity Gain			0.5		V/µs
Supply current		T_A = 25°C			1.7	2.8	mA
Power consumption		V_S = ±15 V, T_A = 25°C			50	85	mW

(1) Unless otherwise specified, these specifications apply for V_S = ±15 V, −55°C ≤ T_A ≤ +125°C (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to 0°C ≤ T_A ≤ +70°C.

8 REFERENCES:

[1] Low Cost Instrumentation Amplifier: http://www.analog.com/media/en/technical-documentation/data-sheets/AD620.pdf

[2] The IC 741 Op-Amp tutorial and Characteristics: https://www.elprocus.com/ic-741-op-amp-tutorial-and-characteristics/

[3] brain-computer interface (BCI): http://whatis.techtarget.com/definition/brain-computer-interface-BCI

[4] Biopotential Amplifiers: http://www.fis.uc.pt/data/20062007/apontamentos/apnt_134_6.pdf

[5] OPAMP 741C Datasheet: http://www.datasheetcafe.com/ic741-datasheet-pdf/

[6] Getting the most out of your instrumentation amplifier design: http://www.ti.com/jp/lit/an/slyt226/slyt226.pdf