NCF215A / NCF215B

NCF215A (ACTIC-SRX-VW 3D) / NCF215B (ACTIC-SRX-VW 1D)

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NCF215A_NCF215B COMPANY PROPRIETARY

Document information

Information	Content
Keywords	Car key, Vehicle Immobilization (IMMO), Passive Keyless Entry (PKE), Remote Keyless Entry (RKE), MRK III
Abstract	The NCF215A / NCF215B is a fully integrated single-chip solution combining RKE, PKE and IMMO functionality designed for use in automotive environments.

1 General information

1.1 General description

The NCF215A / NCF215B is an extremely compact single chip solution, ideally suited for automotive applications with combined vehicle immobilization and keyless entry / start functions. The device incorporates a security transponder and a RISC controller on the same chip and requires only a few external components. The security transponder operation is granted with depleted or even without external battery supply. The device is intended to operate in combination with an external UHF transmitter, typically a 2-way transceiver, such as NXP's NCF2984. The NCF2984 device is a 2-way UHF transceiver with embedded micro-controller intended for use in an automotive environment.

The RISC controller is powered by NXP's low power hardware extended (MUL/DIV) 16-Bit MICRO RISC KERNEL (MRK IIIe) employing a 2-stage pipeline architecture in order to improve performance. For transponder, keyless entry / start operations, the on-chip hardware calculation unit or any user-defined software based algorithm can be employed for data communication.

The device comes in a 40 pin HVQFN package and features 19 I/O ports allowing for up to 19 command button inputs.

The device provides up to 2048 bytes of EEPROM for data storage with access control as defined by the application. In addition, the device supports a sophisticated EEPROM access scheme when operating as security transponder during immobilizer operation.

The device can be used in combination with an external MEMS type motion sensor (e.g. NXP's FXLS8962) or with a mechanical motion sensor. The information from the motion sensor can be used to disable the LF active receiver block as long as motion is not detected, e.g. to protect the car key against relay station attacks when it is in rest position. Furthermore, this reduces the device's current consumption to prolong the battery life time.

The device provides means for capacitive LF tuning for maintaining an optimal resonance frequency and optimize reception of an incoming LF signal in order to save cost in the bill of material.

2 Features and benefits

2.1 General

- Single chip security transponder and keyless entry solution
- Interface (SPI) for external UHF transceiver (e.g. NCF2984 for 2-way RF communication)
- Port wake-up function for command buttons and external peripherals
- Programmable current source for direct LED drive
- RISC programmable device operation
- 32 bit quasi unique device and product type identification
- Single Lithium cell operation, 2.0 V to 3.6 V
- C-Compiler supported software development
- 40 pin compact HVQFN package (6 mm x 6 mm)
- On-chip temperature sensor
- Motion sensor interface for MEMS type and mechanical motion sensor
- Excellent ESD protection at all pins: ±4 kV HBM, ±500 V CDM

2.2 Security Transponder

- Operating frequency: 125 kHz
- 3D LF transponder operation (NCF215A only)
- BPLM modulation (base station to transponder)
- Passive load modulation (transponder to base station); 4 kbit/s Manchester encoded
- Built-in WFS-5d immobilizer protocol
- Fast mutual authentication
- 2 ms LF carrier detection
- EEPROM read/write protection capability
- Capacitive antenna tuning for transponder operation

2.3 3D LF active interface

- Operating frequency: 125 kHz
- Programmable wake-up receiver sensitivity
- Low supply current for wake-up receiver
- Excellent selectivity for superior jamming robustness (e.g. electrical vehicle charging or Qi charger)
- 4 kbit/s data rate Manchester encoded
- 3 programmable wake-up patterns with up to 41 bit
- Low power LF wake-up and data processing
- LF event triggered timer (post-wake-up timer) running with crystal clock for accurate protocol handling
- Adjustable Q-factor with switchable internal resistors
- Capacitive antenna tuning for LF active operation

2.4 3D narrowband LF RSSI

- Three axis (3D) narrowband LF signal strength indication and measurement (RSSI)

- 16 bit digital RSSI with configurable hardware averaging
- 4 different digital filter settings
- Fast measurement time: 2.6 ms for 3 input channels (filter setting A, 16 times averaging per channel)
- High RSSI accuracy due to factory calibration procedure

2.5 Calculation Unit

- AES128 with 128 bit Secret Key
- Fully configurable CRC hardware co-processor unit (1 to 16 bit CRC)
- Non-deterministic (true) and pseudo random number generator (16 bit)

2.6 RISC Controller

- 16 Bit Harvard Architecture (RISC)
- Hardware supported MUL/DIV instructions
- Two CPU clock cycles per instruction (2-stage instruction pipeline)
- Short instruction execution time (0.125 μs @ 16 MHz CPU clock)
- System ROM for device firmware
- Up to 64 kByte user EROM for application (code and data space)
- Up to 2048 Byte Ultra Low Power (ULP) Serial EEPROM for extended user data
- 4 kByte RAM (3840 bytes USER RAM and 256 bytes used for SYSTEM RAM)
- Single level interrupt architecture
- On-chip low tolerance RC Oscillator (< ±10%)
- Three 16-Bit Timer/Counter
- Watchdog
- Low power consumption

2.7 Peripherals

- 19 general purpose I/Os with wake-up and interrupt function
- Fail-safe port wake-up support with two general purpose I/Os
- Software configurable pull-up or pull-down resistor (for all but fail-safe I/Os)
- Software configurable pull-up strength: strong (27 kΩ) or weak pull up (115 kΩ)
- Software configurable wake-up/interrupt either on high to low or low to high transition (for all but fail-safe I/Os)
- Optional clock/event input for Timer/Counter
- General purpose ADC supporting various analogue sources (including external source) with optional multiple conversion support with averaging function
- Two synchronous serial peripheral interfaces SPI 0 and SPI 1 with a baud rate selectable between 125 kHz and 4 MHz
- Battery Voltage Sensor with programmable battery low threshold
- 32.768 kHz crystal oscillator with low power interval timer and real time clock

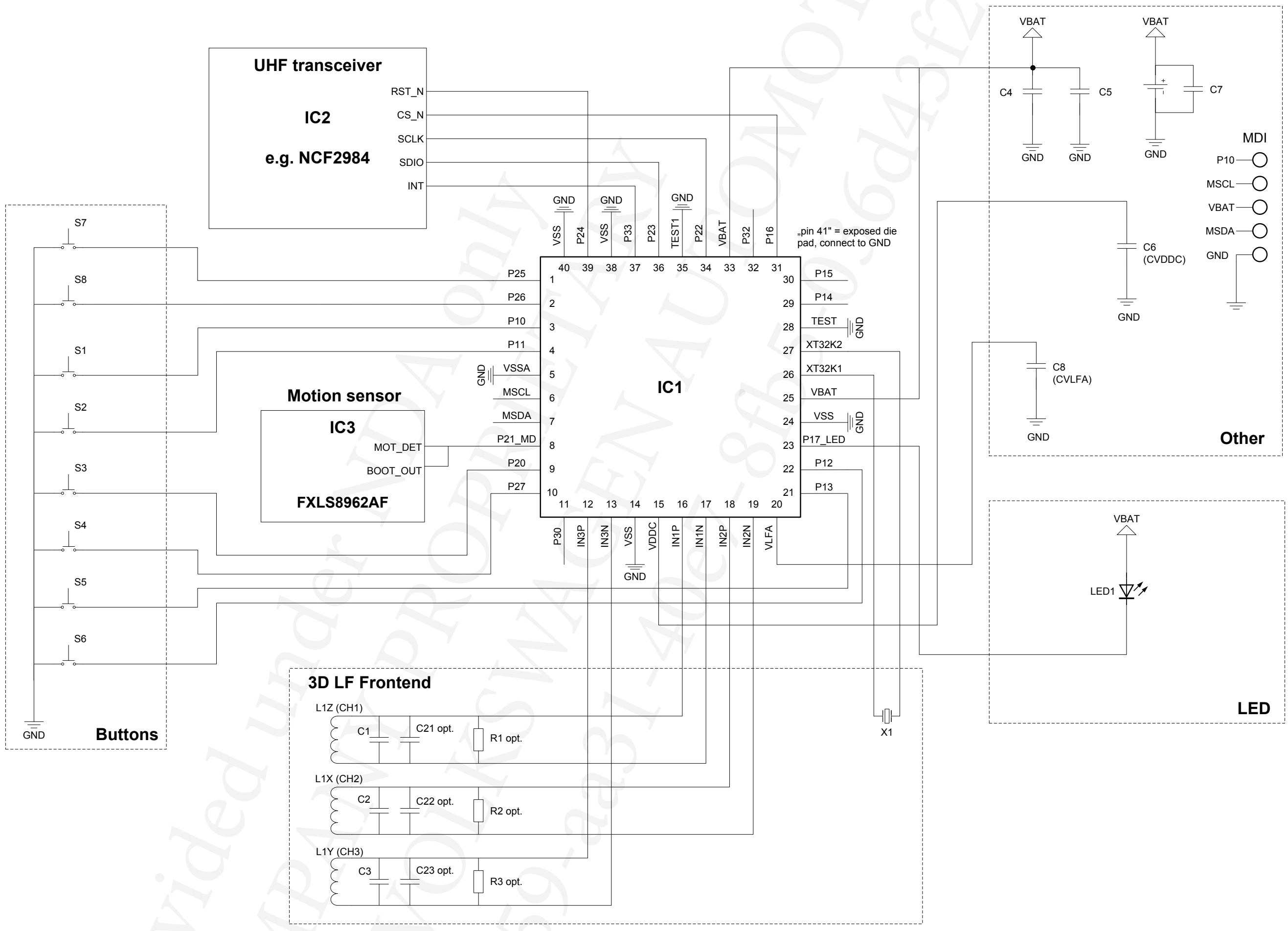
3 Applications

The NCF215A / NCF215B is a compact single chip solution, ideally suited for automotive applications with combined vehicle immobilization and keyless entry / start functions. The device incorporates a Security Transponder and a RISC Controller on the same chip and requires only a few external components.

3.1 Application areas

- Remote Keyless Entry (RKE)
- Passive Keyless Entry (PKE) and/or Passive Keyless Go (PKG)
- Immobilization

3.2 Typical application diagram



(1) IC1 = NCF215A / NCF215B

Figure 1. Typical application diagram

4 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
NCF215AWHN4 [1]	HVQFN40	Plastic thermal enhanced very thin quad flat package; 40 terminals; body 6 x 6 x 0.85 mm; terminal pitch 0.5 mm; wettable flanks	SOT618-7
NCF215BWHN4 [1]	HVQFN40	Plastic thermal enhanced very thin quad flat package; 40 terminals; body 6 x 6 x 0.85 mm; terminal pitch 0.5 mm; wettable flanks	SOT618-7

[1] WHN version contains a WFS-5d based transponder emulation

4.1 Ordering options

Every NCF215A / NCF215B product gets assigned a commercial type name, which includes also customer and application specific data and has the following format:

NCF21ttxHNp/vvffs

'**NCF21**' and '**HN**' are constants, all other letters are variables, which are explained in Table 2. Please contact the local NXP sales representative for available product options.

Table 2. NCF215A / NCF215B type name format

Variable	Meaning	Values	Description
tt	Product basic type name	5B	NCF215B (1D immobilizer)
		5A	NCF215A (3D immobilizer)
x	Supported transponder emulation	W	WFS-5d transponder
p	Package	4	HVQFN40
vv	Product version code and ROM code identifier	[1]	
ff	Fab-key identifier	[1]	
s	Code for available amount of EROM and EEPROM	[1]	The available amount of EROM and EEPROM is adaptable on request. Up to 64 kByte user EROM and up to 2048 Byte EEPROM is supported.

[1] Please contact the local NXP sales representative for details regarding the coding.

5 Marking

Table 3. NCF215A / NCF215B marking codes

Type number	Marking code
NCF215AxHN4 [1]	Line A: 215Axnn [1][2] Line B: db__as [3] Line C: ZSywwr [4] [5] Line D: HN4sF [6]
NCF215BxHN4 [1]	Line A: 215Bxnn [1] [2] Line B: db__as [3] Line C: ZSywwr [4] [5] Line D: HN4sF [6]

[1] "x" is a code in the product type name indicating the supported transponder emulation:

- W: WFS-5d based transponder emulation

[2] "nn" is a two digit code referring to a specific rom code version, to a specific fabkey data image and the supported feature set. For details contact your local NXP sales representative.

[3] "db_as" is a five digit batch code: first two digits for DBSN followed by '_' and last two digits for ASID.

The Assembly Sequence ID (ASID) is a 2-digit indicator that counts the number of assembly batches (transport lots) within one diffusion batch id and one weekly date code. The week start and end dates are defined by the assembly center algorithm. The ASID is assigned sequentially starting with 01 and ranging through 99, then each digit ranges upper case alphabet letters in combination with numeric, then numeric in combination with upper case alphabet letters, then upper case alphabet letters in combination with upper case alphabet letters providing 1175 possible values within a week-code. The numeric zero '0' is only allowed within the sequence of 01 to 99. The alphabet letter 'O' is not allowed to avoid confusion with numeric '0'.

The Diffusion Batch Sequence Number (DBSN) is a 2-digit indicator that counts the number of diffusion batches (DBID) within one Package Type (i.e. HVQFN40) and one weekly date code. The DBSN is assigned sequentially starting with 01 and ranging through 99, then each digit ranges upper case alphabet letters in combination with numeric, then numeric in combination with upper case alphabet letters, then upper case alphabet letters in combination with upper case alphabet letters providing 1175 possible values within a week-code. The numeric zero '0' is only allowed within the sequence of 01 to 99. The alphabet letter 'O' is not allowed to avoid confusion with numeric '0'.

[4] "yww" is a three digit Date code: "YWW", ** refers to a two digit arbitrary character

"Y" is a code indicating the year in which the IC is assembled. Examples: for year 2009 is Y = 9, for year 2010 is Y = 0, for year 2011 is Y = 1. "WW" is a code indicating the week in which the IC is assembled. It is determined from the date the assembly transport lot is created or alternately the date die is issued from die stores to assembly start or the date die attach (Diebond) occurs or the date encapsulation occurs. Examples: for week 01 is WW = 01, for week 52 is WW = 52, for week 53 is WW = 53.

[5] "r" is the product version code referring to the mask and package versions.

[6] "s" is the memory size code referring to the available amount of EROM and EEPROM.

6 Block diagram

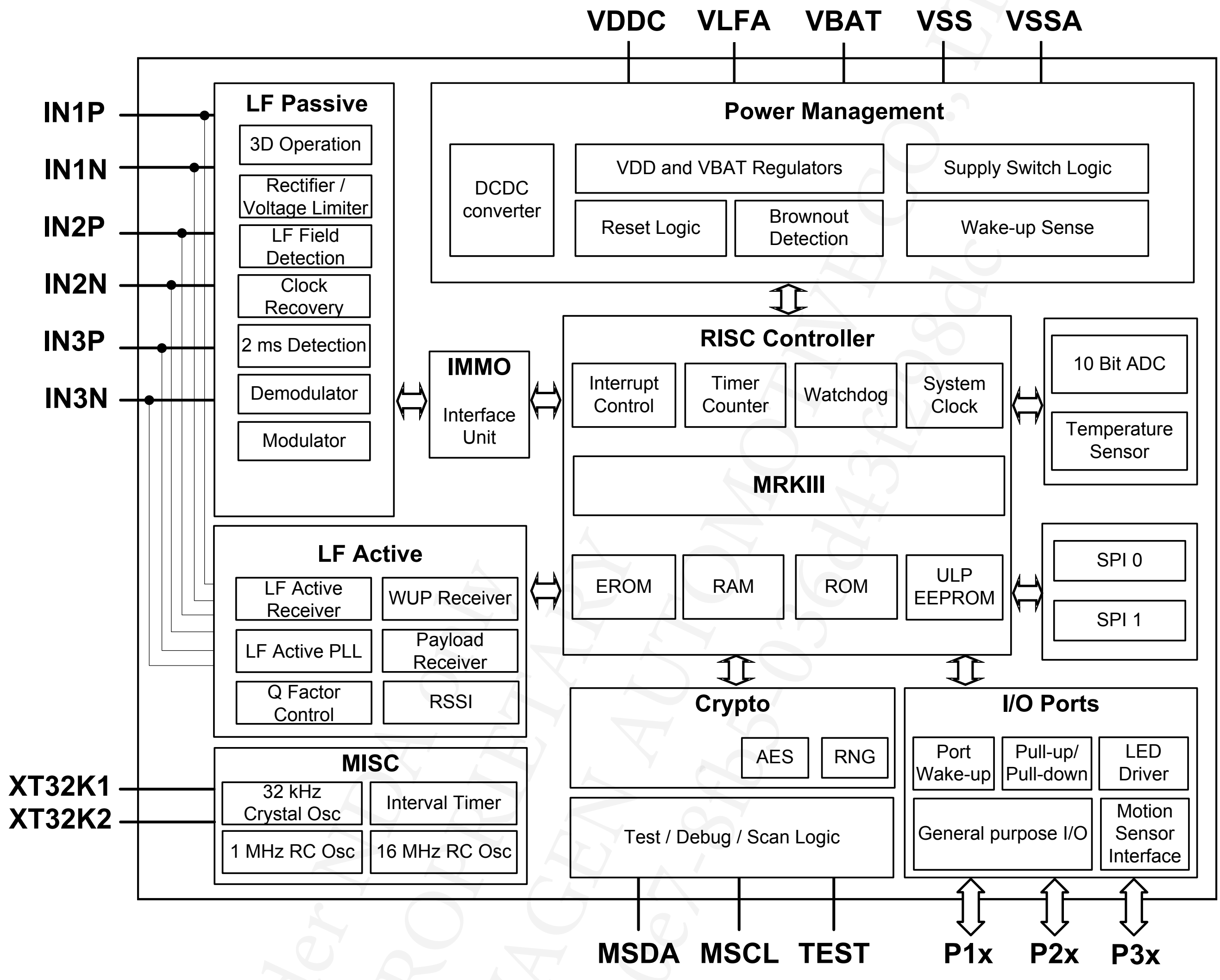


Figure 2. NCF215A / NCF215B block diagram

7 Pinning information

7.1 Pinning

Figure 3 shows the pin configuration of NCF215A / NCF215B in the HVQFN40 package.

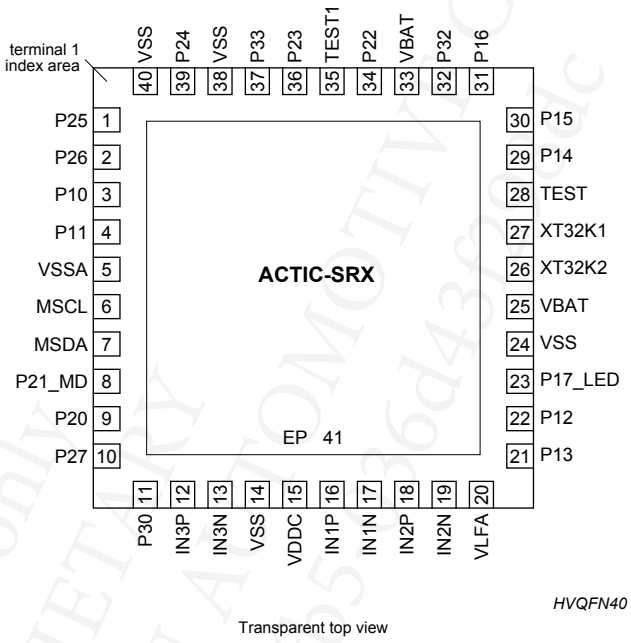


Figure 3. Pin configuration HVQFN40 (SOT618-7)

7.2 Pin description

Table 4. Pin description

Symbol	HVQFN40	Description
P25	1	General purpose digital IO, pull-up/pull-down resistor Port wake-up and interrupt SPI0 SDI - serial data input
P26	2	General purpose digital IO, pull-up/pull-down resistor Port wake-up and interrupt SPI0 SDIO - serial data output or input/output SPI0 SCK - serial clock
P10	3	General purpose digital IO, pull-up resistor Fail-safe port wake-up, port interrupt SPI0 SCK - serial clock [1] Timer 0 output
P11	4	General purpose digital IO, pull-up resistor Fail-safe port wake-up, port interrupt SPI0 SDIO - serial data output or input/output [1] Timer 1 output ADC negative input
VSSA	5	Common ground
MSCL	6	Debug interface—MSCL is an output and shall be unconnected in the application.
MSDA	7	Debug interface—MSDA features an on-chip pull-up to VBAT and may be left unconnected or terminated to VBAT as desired by the application.
P21_MD	8	General purpose digital IO, pull-up/pull-down resistor Port wake-up and interrupt Motion sensor interface SPI0 SDI - serial data input Timer 2 output Timer 1 capture input
P20	9	General purpose digital IO, pull-up/pull-down resistor Port wake-up and interrupt SPI0 SDI - serial data input SPI0 SCK - serial clock Timer 1 output
P27	10	General purpose digital IO, pull-up/pull-down resistor Port wake-up and interrupt SPI0 SDIO - serial data output or input/output
P30	11	General purpose digital IO, pull-up/pull-down resistor Port wake-up and interrupt
IN3P	12	LF input, transponder and active interface (LF antenna) [2]
IN3N	13	LF input, transponder and active interface (LF antenna) [2]
VSS	14	Common Ground
VDDC	15	Device LF field supply voltage

Symbol	HVQFN40	Description
IN1P	16	LF input, transponder and active interface (LF antenna) [2]
IN1N	17	LF input, transponder and active interface (LF antenna) [2]
IN2P	18	LF input, transponder and active interface (LF antenna) [2]
IN2N	19	LF input, transponder and active interface (LF antenna) [2]
VLFA	20	Supply for LF active receiver [3]
P13	21	General purpose digital IO, pull-up/pull-down resistor Port wake-up and interrupt SPI1 SCK - serial clock TMUX0CLK clock multiplexer output Timer 1 capture input
P12	22	General purpose digital IO, pull-up/pull-down resistor Port wake-up and interrupt SPI1 SDI - serial data input TMUX0CLK clock multiplexer output Timer 2 output ADC reference voltage negative input
P17_LED	23	General purpose digital IO, pull-up/pull-down resistor Port wake-up and interrupt LED driver pin Timer 1 capture input ADC reference voltage positive input
VSS	24	Common ground
VBAT	25	Battery supply
XT32K2	26	Crystal oscillator interface (LF active, 32768 Hz crystal)
XT32K1	27	Crystal oscillator interface (LF active, 32768 Hz crystal)
TEST	28	Test terminal—must be connected to VSS in the application
P14	29	General purpose digital IO, pull-up/pull-down resistor Port wake-up and interrupt SPI1 SDI - serial data input SPI1 SDIO - serial data output or input/output TMUX1CLK clock multiplexer output
P15	30	General purpose digital IO, pull-up/pull-down resistor Port wake-up and interrupt SPI1 SCK - serial clock XCLK external clock input ADC negative input
P16	31	General purpose digital IO, pull-up/pull-down resistor Port wake-up and interrupt SPI0 SDIO - serial data output or input/output SPI1 SDIO - serial data output or input/output Timer 0 output ADC positive input

Symbol	HVQFN40	Description
P32	32	General purpose digital IO, pull-up/pull-down resistor Port wake-up and interrupt ADC negative input
VBAT	33 [4]	Battery supply
P22	34	General purpose digital IO, pull-up/pull-down resistor Port wake-up and interrupt SPI0 SCK - serial clock SPI1 SCK - serial clock Timer 0 output
TEST1	35	Test terminal—must be connected to VSS in the application
P23	36	General purpose digital IO, pull-up/pull-down resistor Port wake-up and interrupt SPI0 SDIO - serial data output or input/output SPI1 SDIO - serial data output or input/output Timer 1 output
P33	37	General purpose digital IO, pull-up/pull-down resistor Port wake-up and interrupt
VSS	38	Common ground
P24	39	General purpose digital IO, pull-up/pull-down resistor Port wake-up and interrupt SPI0 SDI - serial data input SPI1 SDI - serial data input Timer 2 output
VSS	40	Common ground
EP	41 [5]	Exposed die pad—must be connected to common ground

[1] SPI configurations that would require a pull-down resistor are not supported

[2] NCF215B (1D) supports transponder operation with one LF antenna. The input channel (IN1P/IN1N, IN2P/IN2N, or IN3P/IN3N) is selectable.

[3] VLFA is an internal supply and shall only be connected to an external buffer capacitor with effective capacitance of C_{VLFA}. Do not use VLFA to supply external devices.
VLFA must not be pulled to high voltages or VSS.

[4] Pin 33 is internally connected with pin 25. Pin 33 may be left unconnected in the application, which limits the allowed maximum number of simultaneously switching outputs to 16.

[5] Exposed die pad

8 Functional description

This section describes briefly the functional building blocks of NCF215A / NCF215B. More detailed information including the device special function register description is given in the user manual (see [1]).

8.1 Power management

8.1.1 Power supply domains

The NCF215A / NCF215B features several power supply domains (see Figure 4). A versatile power management (see Figure 5) enables the device to derive its power supply from two different energy sources

- External battery (VBAT)
- Low frequency field (VFLDLF)

The two corresponding power supply domains VBAT and VFLDLF are unregulated. The device is able to operate when any of the energy sources is available regardless the presence or absence of the other.

Derived from either of the two unregulated domains are the regulated power supply domains:

- Digital core supply (VDD)
- Analogue core supply (VDDA)

Derived from the unregulated VBAT domain are the regulated power supply domains:

- Digital regulated battery supply (VBATREG)
- LF active supply (VLFA)
- LF active digital supply (VLFADIG)
- Sigma-Delta ADC supply (VSDADC)

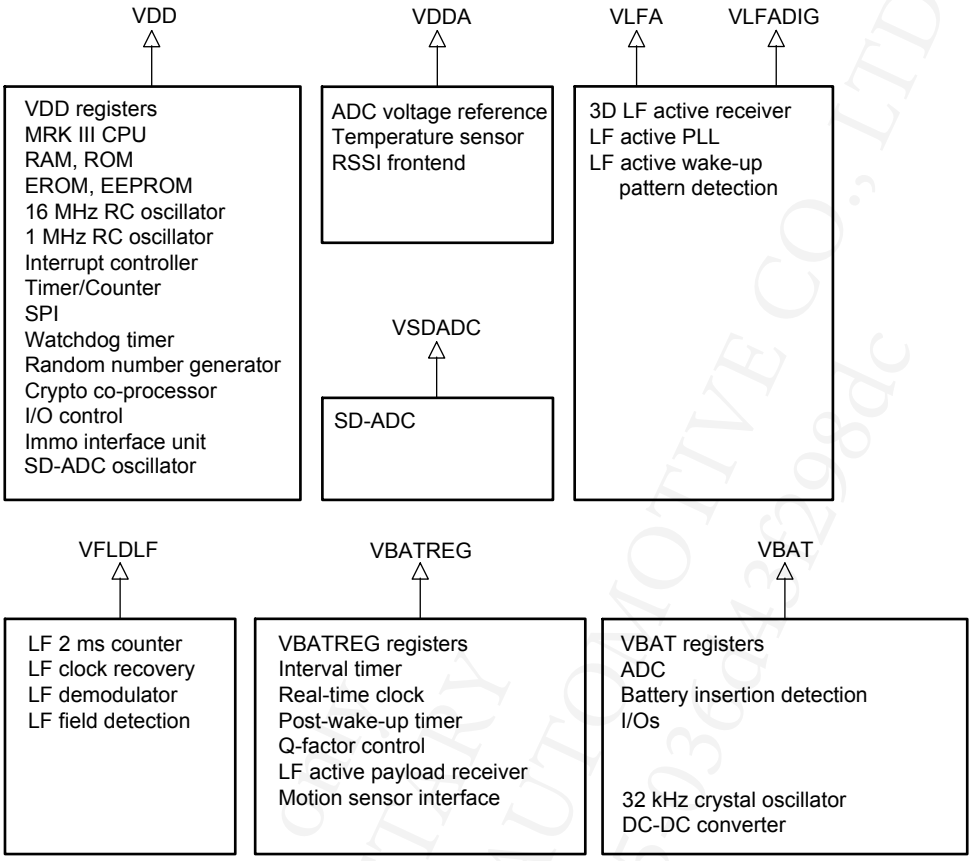


Figure 4. Power supply domains

Except VDD, the voltage regulators for all supplies are turned off after first device start-up. In order to employ the blocks supplied with these voltages, the respective dedicated voltage regulators have to be activated first.

Determining the appropriate supply configuration is accomplished by means of the power supply control (Figure 5).

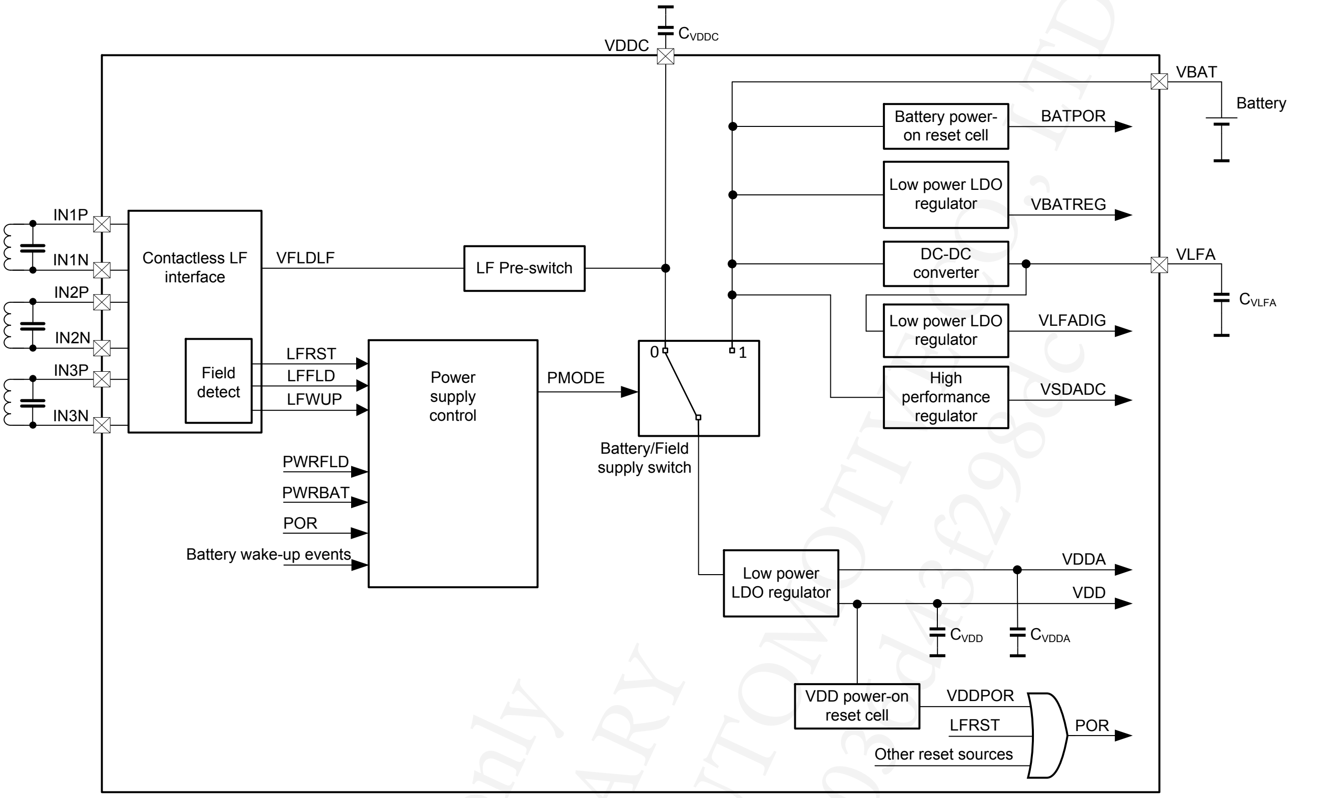


Figure 5. Power supply control

8.1.2 Power supply control

8.1.2.1 Power supply switch

The NCF215A / NCF215B provides several switches for power supply selection of the core. The main supply switch selects between battery and field supply.

The field supply is generated with one pre-switch for the LF. The LF pre-switch features a current limitation in order to limit the energy transferred from the field into the supply capacitor at VDDC. This avoids deep dips in the field supply, which might be erroneously interpreted as a load modulation by the base station.

When the power supply state is changed the device supply switch opens the existing connection before connecting the new supply. The device is powered for a short period of time from the internal supply capacitor C_{VDD}. Therefore, the application must minimize the current consumption when changing the supply state to prevent an accidental power-on reset.

8.1.2.2 Device wake-up

The following wake-up events terminate the POWER OFF state and switch to the LF FIELD- or BATTERY state (see Figure 7):

- LF field wake-up events
  – Presence of LF field (LFWUP)
- Battery wake-up events

- Battery insertion (BATPOR)
- Port wake-up (e.g. button press)
- Detection of valid LF active wake-up pattern
- Interval timer or real-time clock wake-up
- Motion sensor interface wake-up
- LF active monitors: VLFA brownout, 32 kHz crystal oscillator clock fail detected, DC-DC converter fail detected
- Watchdog time-out event

If a wake-up event emerges, the power management selects the corresponding power supply. If more than one wake-up event is pending at the same time, the power management automatically selects the strongest available supply source related to the wake-up event.

Once the supply voltage VDD exceeds the power-on reset threshold voltage V_{POR}, the power-on reset comparator output signal (VDDPOR) becomes low after a short delay t_{POR_HLD}, whereupon the power management state is locked, the RISC becomes operational and the device enters RUN mode (Section 8.6.1.1). All further supply state changes are under control of the application (Figure 6).

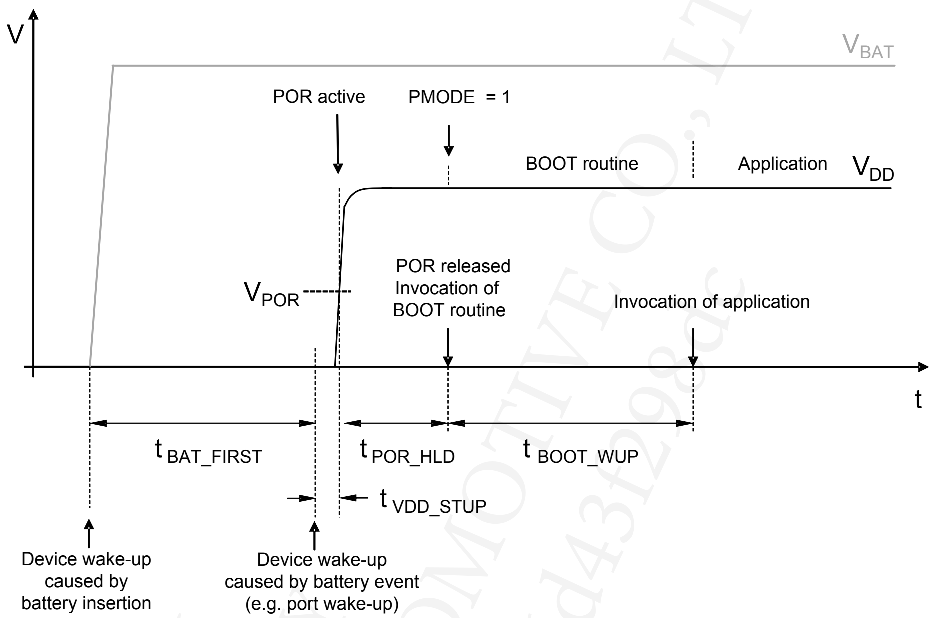
Starting with the boot sequence, the power supply state of the VDD supplied part can be monitored and controlled via the power control registers. A change of the supply configuration may apply e.g. in case an LF Field and a button press are detected at the same time or in case an LF Field is being detected while battery supply has been utilized. If during the boot sequence an LF field and a battery wake-up event are pending at the same time, then the LF Field wake-up is given precedence and will commence.

8.1.2.3 Device reset

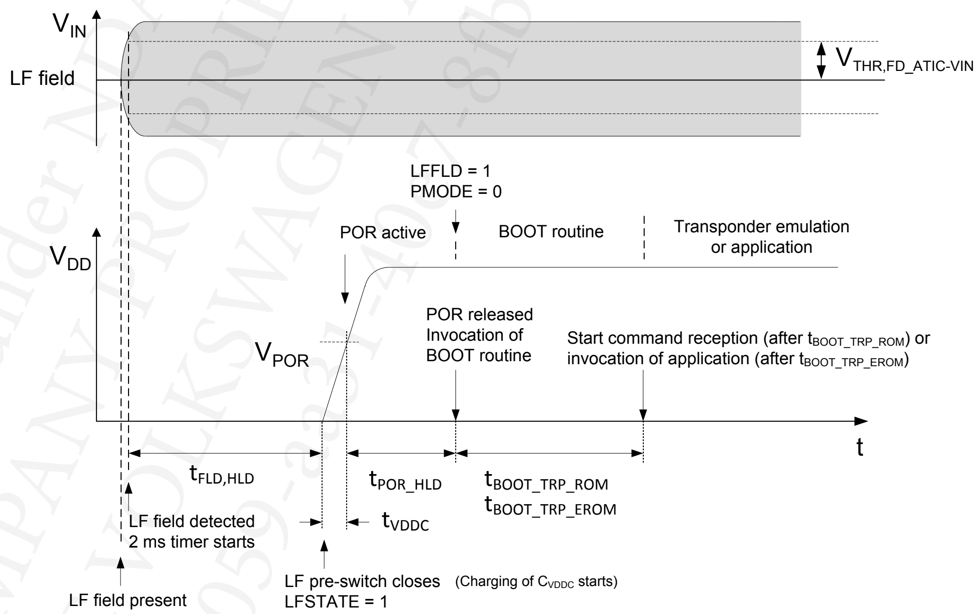
A power-on reset (POR) for the core is generated under the following conditions:

- The device is in the POWER OFF state
- The voltage level at VDD is below the power-on reset threshold V_{POR} (VDDPOR)
- An LF field emerges and the device is configured for a reset (LFRST)
- The voltage level at VDD falls below the VDD brownout threshold $V_{BO,VDD}$ and
  i) code is executed from the EROM, or
  ii) the CPU clock source is set to a frequency greater than 8 MHz
- A watchdog timer overflow occurs
- A reset of the VDD domain is triggered by the application (software reset)
- A CPU/MMU exception occurs and the device is configured for a reset

Upon a device reset the power management logic is released and starts with a new evaluation of the supply condition.



a) Device wake-up caused by battery insertion or another battery wake-up event (e.g. a port wake-up)



b) Device wake-up cause by LF field

Figure 6. Power-up timing

8.1.2.4 Power supply states

The device support two different core supplies, depending on where whether the device power is derived from the external battery or the LF field:

- Battery supply (BATTERY state)
- LF field supply (LF FIELD state)

In these two supply states the RISC is functional. In the POWER OFF state, the device remains in a third very low power state and the RISC is not functional (see Figure 7).

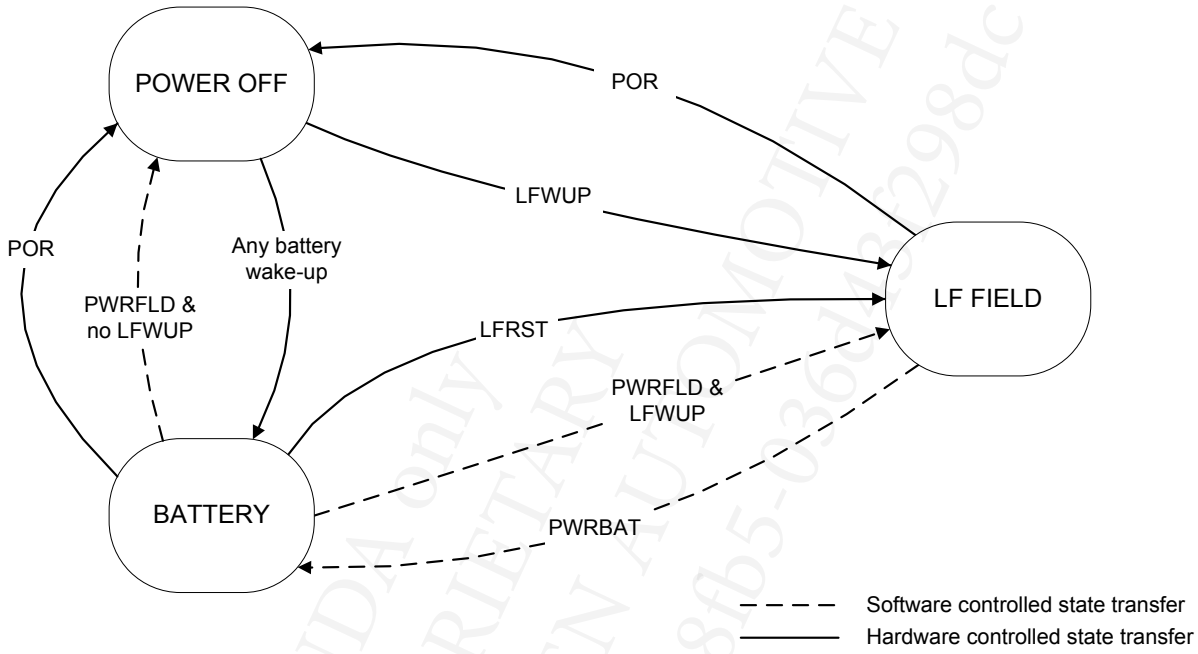


Figure 7. Power Supply States

8.1.2.5 POWER OFF state

In the POWER OFF state, most blocks are internally disconnected from the battery supply, resulting in a very low current consumption. The internal device supply voltage (VDD) stays below the power-on reset threshold voltage and device operation is halted. Only a minimum of circuitry remains operational, like the power management and I/O ports (configured as input).

The device resides in the POWER OFF state any time a power-on reset comparator indicates (VDDPOR) a weak supply condition. The POWER OFF state is terminated by a wake-up event, such as detected presence of an LF field (LFWUP) or any battery wake-up event.

Once the supply condition is evaluated during device power-up and the boot sequence is completed, the device will start execution of the application program in either the BATTERY state or the LF FIELD state.

8.1.2.6 BATTERY state

In the BATTERY state, the device is powered from the external battery. After execution of the boot sequence, device operation is controlled by the RISC and the program code

starts at the BATTERY WARM boot vector. The application code can terminate the BATTERY state.

In case an LF field is detected when the device is in the BATTERY state, the device behavior depends on the configuration. If according to the configuration a non-maskable interrupt (NMI) is caused after field detection, the BATTERY state is kept and control is still with the RISC. The application program can activate the LF field switch (PWRFLD) to provoke a change to the LF FIELD state. If according to the configuration field detect causes a reset (LFRST), the state is changed to LF FIELD and the boot routine is invoked again.

Once in the BATTERY state, any further battery wake-up event does not cause a state change and has to be handled via the RISC.

If the device wants to terminate the BATTERY state, it has to activate the LF field switch (PWRFLD). If no LF supply is present, the device enters the POWER OFF state as soon as VDD falls below the power-on reset threshold (VDDPOR event).

8.1.2.7 LF FIELD state

In LF FIELD state the device supply is derived from the LF Interface.

After execution of the boot sequence, device operation is controlled by the RISC and the program code starts at the LF FIELD WARM boot vector (unless a built-in LF transponder emulation is selected in the boot routine).

In case a weak LF field supply condition causes a power-on reset (VDDPOR), the LF FIELD state is left and the device enters the POWER OFF state.

If the device is in the LF FIELD state and the application program activates the battery supply switch (PWRBAT), the device changes to the BATTERY state.

8.1.3 Battery supply states

The battery supply domains VBATREG, VLFA, and VLFADIG can be programmed individually by the application program and they support the following combinations of battery supply states:

- VBATREG = OFF, VLFA = OFF, VLFADIG = OFF
- VBATREG = ON, VLFA = OFF, VLFADIG = OFF
- VBATREG = ON, VLFA = ON, VLFADIG = OFF
- VBATREG = ON, VLFA = ON, VLFADIG = ON

The supply domain VLFA is generated by a highly efficient multi-ratio DC-DC converter, which controls the conversion ratio continuously based on the available supply voltage VBAT and the actual load current. The DC-DC converter is fully integrated and requires only one external buffer capacitor C_{VLFA}.

The battery supply states are independent of the power supply states which are related to the core.

8.2 System clock

The clock generation unit provides versatile means to select the clock source and the clock speed for the CPU and the peripheral components.

8.2.1 Clock sources

The NCF215A / NCF215B provides several clock sources based on internal oscillators and external sources, which are summarized in Table 5.

Table 5. Clock sources

Symbol	Description
RCCLK	Clock from 16 MHz main RC oscillator
AUXCLK	Clock from 1 MHz auxiliary RC oscillator
LFCLK	Clock from 125 kHz LF field
XO32KCLK	Clock from 32 kHz crystal oscillator
SDADCCLK	SD-ADC clock source from 16 MHz precision RC oscillator
XCLK	External clock at P15

8.2.1.1 RCCLK, clock from 16 MHz main RC oscillator

The 16 MHz main RC oscillator is the main clock source for high speed CPU and peripheral operation. The oscillator starts up when it is activated and can be selected independently of the available core supply state.

8.2.1.2 AUXCLK, clock from 1 MHz auxiliary RC oscillator

The 1 MHz auxiliary RC oscillator is intended for auxiliary tasks and low speed CPU and peripheral operation. The oscillator is used by several peripherals and requires a start-up time $t_{AUXCLK,PON}$.

8.2.1.3 LFCLK, clock from 125 kHz LF field

The selection of the 125 kHz clock (LFCLK) is intended for transponder applications with ultra low current consumption, where even the current consumption of the auxiliary RC oscillator shall be avoided.

8.2.1.4 XO32KCLK, clock from 32 kHz crystal oscillator

The clock of the 32 kHz (32768 Hz) crystal oscillator is required for the LF active receiver, the interval timer, the real-time clock, the post-wake-up timer, and the motion sensor interface. The 32 kHz crystal oscillator requires a start-up time t_{XO32K_set}. The supply for the crystal oscillator is derived from the unregulated battery supply VBAT; hence, the clock is available in POWER OFF state, too.

8.2.1.5 SDADCCLK, SD-ADC clock source

SDADCCLK, derived from a 16 MHz precision RC oscillator, is the clock source for the SD-ADC, which is part of the narrowband RSSI block. The precision RC oscillator must be calibrated to the target frequency $f_{OSC,SDADC}$ prior to every use by means of a built-in autocalibration block. This is required to calibrate out initial frequency tolerances and deviations caused by temperature and supply voltage variations. The reference clock for the autocalibration is the 32 kHz crystal oscillator clock, XO32KCLK, and the required calibration time is $t_{SDADCCLK,CAL}$.

8.2.1.6 XCLK, external clock at P15

An external clock XCLK with a frequency of f_{XCLK} can be connected at P15. This clock is intended as external clock source for timer 0, timer 1 and timer 2 as well as for the monitor and debug interface.

8.2.2 Clock domains

Based on the clock sources, clock domains are derived to provide the clock for the CPU and the peripheral components as depicted in Figure 8.

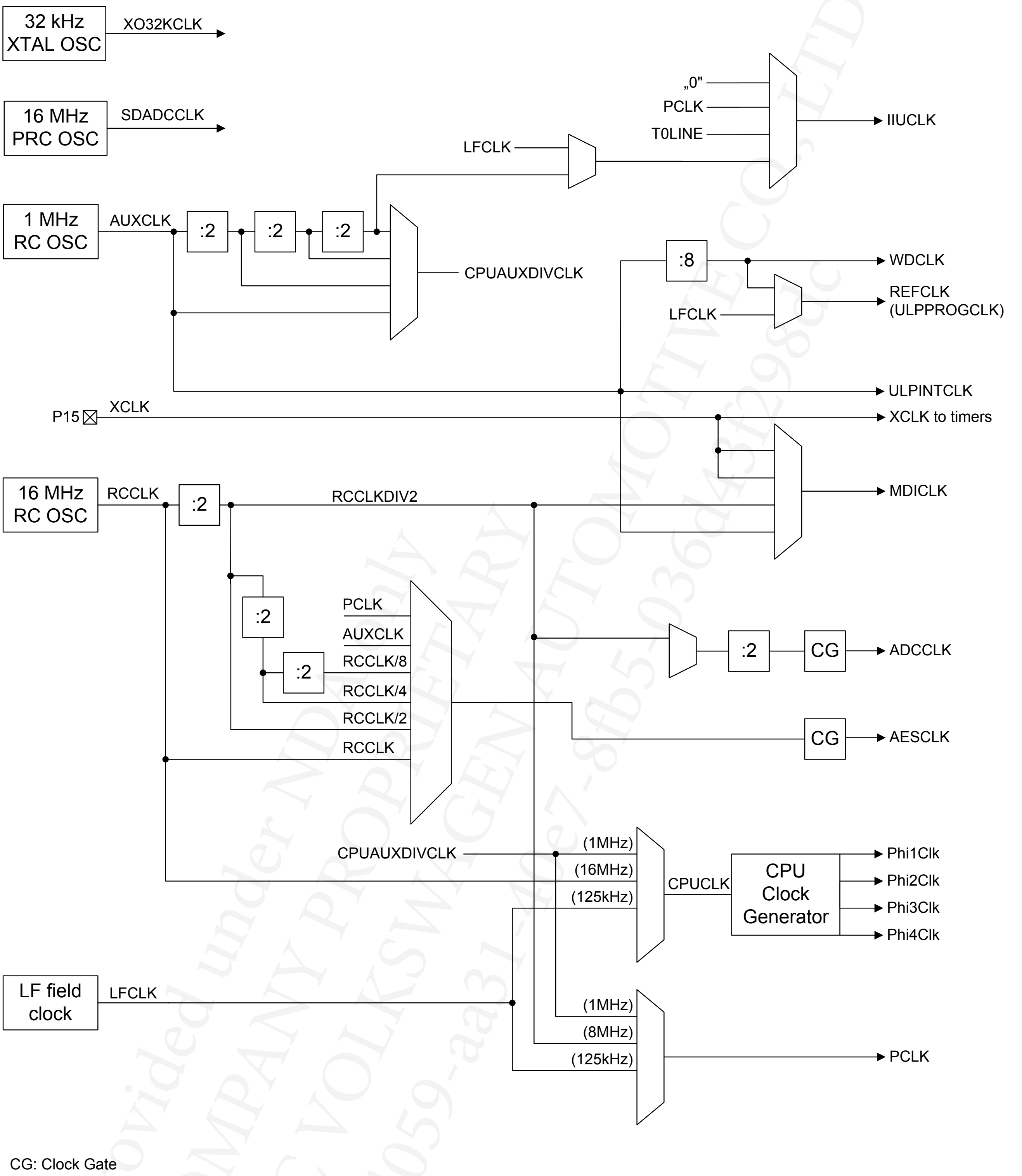


Figure 8. Clock domains for CPU and peripherals

Additional clock domains are provided for timer 0, timer 1 and timer 2, based on two central timer clock multiplexers delivering TMUX0CLK and TMUX1CLK according to Figure 9.

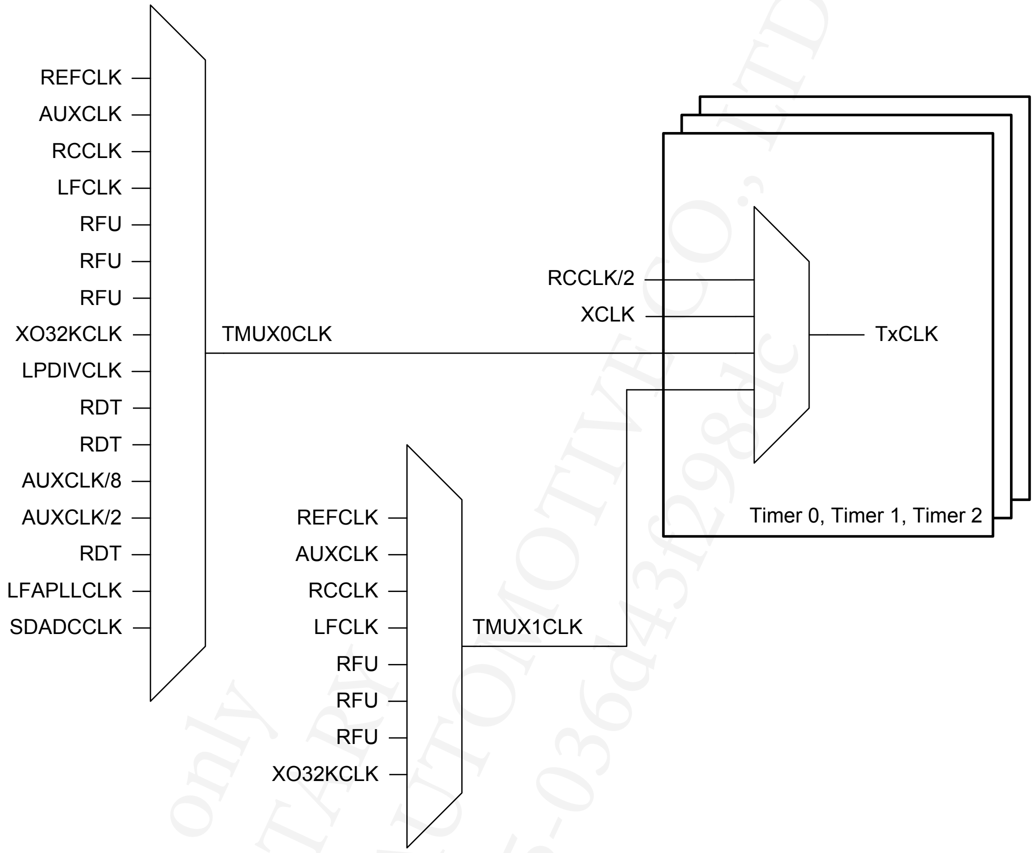


Figure 9. Clock domains for timer 0, timer 1 and timer 2

8.2.2.1 CPUCLK, CPU clock

Three clock sources are selectable for the CPU via system calls, the 16 MHz main RC oscillator RCCLK, the 1 MHz auxiliary RC oscillator AUXCLK, and the clock derived from the LF Field LFCLK. The main and the auxiliary RC clock are always selectable, even for LF field supplied operation.

The CPU clock domain has interfaces to the ROM, RAM, EROM and ULP EEPROM. The clocks for all these modules are generated by a central CPU clock generation unit. The actual execution speed of the CPU is controlled by insertion of additional wait states, dependent on the accessed memories.

Some standard peripherals use the same clock source as the CPU whereas others have only a limited selection of clock sources.

The boot routine always starts using the auxiliary RC clock, CPUAUXDIVCLK. After completion of the boot routine, all other available clock sources can be selected by the application via system calls in order to balance CPU speed and power consumption.

8.2.2.2 PCLK, peripheral clock

The PCLK domain is used by peripherals like the SPI interface and the random number generator. These peripherals usually run with the same clock source as the CPU.

8.2.2.3 AESCLK, AES clock

The AES calculation unit operates either with the same source as the CPU, the auxiliary RC oscillator or a (divided) clock of the main RC oscillator.

The faster clock speed can be used to speed up the calculation time for the LF transponder without the necessity to switch to a faster CPU clock. The AES clock period is $T_{REF,AES}$.

8.2.2.4 ADCCLK, ADC clock

The ADC operates on the clock sourced by the main RC Oscillator, RCCLK/2. Note that the actual ADC clock is divided by two after clock source selection, thus actual ADC clock is RCCLK/4, see also Figure 8.

8.2.2.5 WDCLK, watchdog clock

The watchdog uses the clock from the auxiliary RC oscillator independent of the selected CPU clock source. When the watchdog is enabled, the auxiliary RC oscillator is conditionally enabled too.

8.2.2.6 REFCLK, reference clock

The reference clock is a 125 kHz clock source (clock period $T_{REF,LF}$), which is intended for the timers. It is either derived from the auxiliary RC oscillator or from the LF clock.

8.2.2.7 ULPINTCLK, ULP EEPROM interface clock

The clock for the ULP EEPROM interface (read/write access) is derived from the auxiliary RC oscillator independent of the selected CPU clock source.

8.2.2.8 ULPPROGCLK, ULP EEPROM programming clock

The 125 kHz ULP EEPROM programming clock is either derived from the auxiliary RC oscillator or from the LF clock. The correct clock source is always selected automatically, based on the selected CPU clock source.

8.2.2.9 MDICLK, monitor and download interface clock

Clock sources for the monitor and debug interface are the auxiliary RC clock, the main RC clock and the external clock XCLK. The MDI clock is independent of the selected CPU clock source.

8.2.2.10 IIUCLK, immobilizer interface unit clock

Clock sources for the immobilizer interface unit are the LF clock for the immobilizer and the overflow of timer 0 for the modulator operation. The IIU has a local clock selection unit independent of the selected CPU clock source.

8.2.2.11 XCLK, external clock

The external clock XCLK is provided to timers 0, 1 and 2.

8.2.2.12 TMUX0CLK, timer multiplexer 0 clock

The timer multiplexer 0 clock, TMUX0CLK, is provided to timers 0, 1 and 2. The multiplexer concept allows these timers to operate with and to synchronize to several clock sources.

8.2.2.13 TMUX1CLK, timer multiplexer 1 clock

The timer multiplexer 1 clock, TMUX1CLK, is provided to timers 0, 1 and 2. The multiplexer concept allows these timers to operate with and to synchronize to several clock sources.

8.3 LF Passive interface (Immobilizer)

The contactless passive LF interface provides means to utilize the NCF215A / NCF215B as a contactless transponder, capable to derive its power supply and system clock by inductive coupling to an LF field generated by a corresponding base station. The same LF field is used to receive data from and transmit data to the base station via load modulation under control of the RISC controller. An external LC resonant circuit needs to be connected to the coil inputs (INxP and INxN) of the LF passive interface (Figure 10).

The NCF215A features a 3D contactless transponder. The NCF215B supports transponder communication on one channel only. The required channel 1, 2 or 3 can be configured.

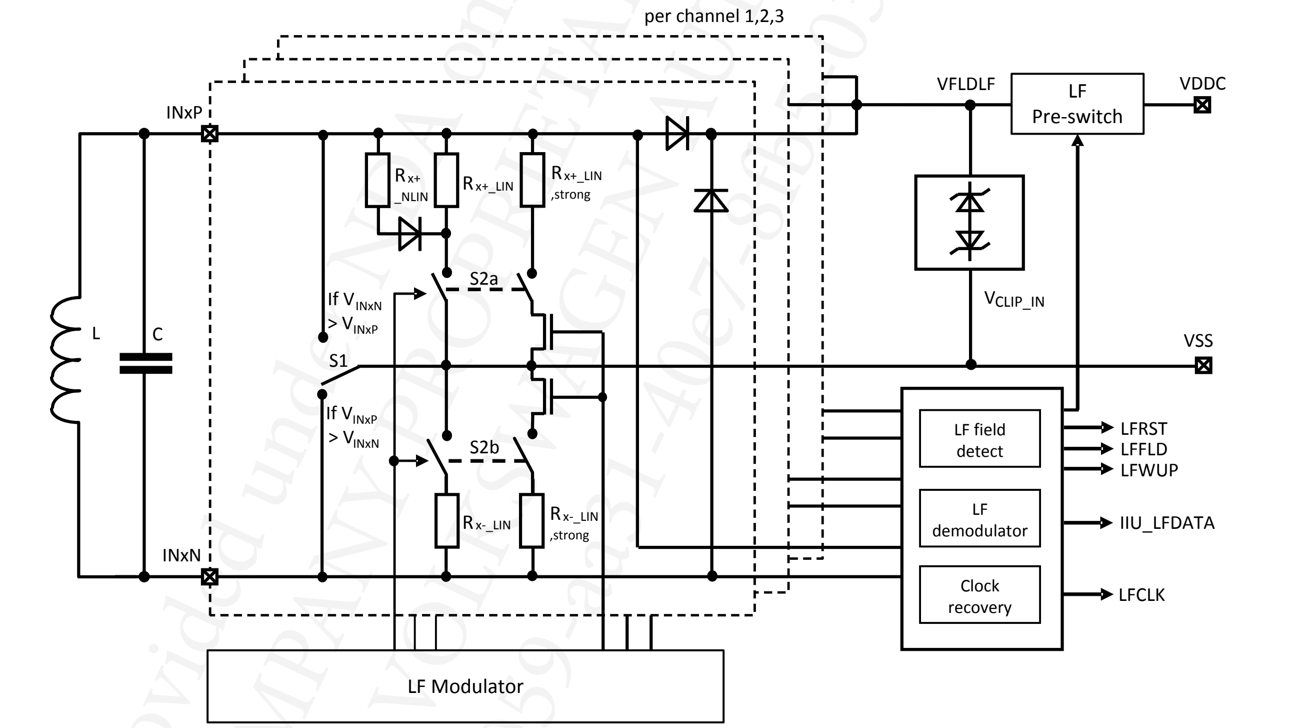


Figure 10. 3D LF passive interface front end circuitry

Independent of the device operating mode, the LF passive interface can detect the presence of an LF field on any channel and providing a corresponding signal to wake-up the device from POWER OFF state, or to interrupt device operation.

The NCF215A / NCF215B features a constant carrier detection before invocation of passive mode (see $t_{FLD,HLD}$ in Figure 6).

8.3.1 Rectifier and limiter

The NCF215A / NCF215B front end features three independent LF rectifier circuits, one per channel. Each rectifier operates in full-bridge configuration, the outputs of the rectifiers are shorted and charge an external capacitor connected to the common pin VDDC. A shunt voltage limiter connected to the output of the rectifiers is provided to ensure that the voltage at pin VDDC does not exceed the specification. The interface input current must not exceed the specified limits.

The LF passive communication with the device employs on-off keying (OOK) of the LF field. The modulation duration and LF field strength shall be chosen such that the rectified supply voltage at VDD stays above the power-on reset threshold V_{POR} during the LF field low condition (see Figure 11).

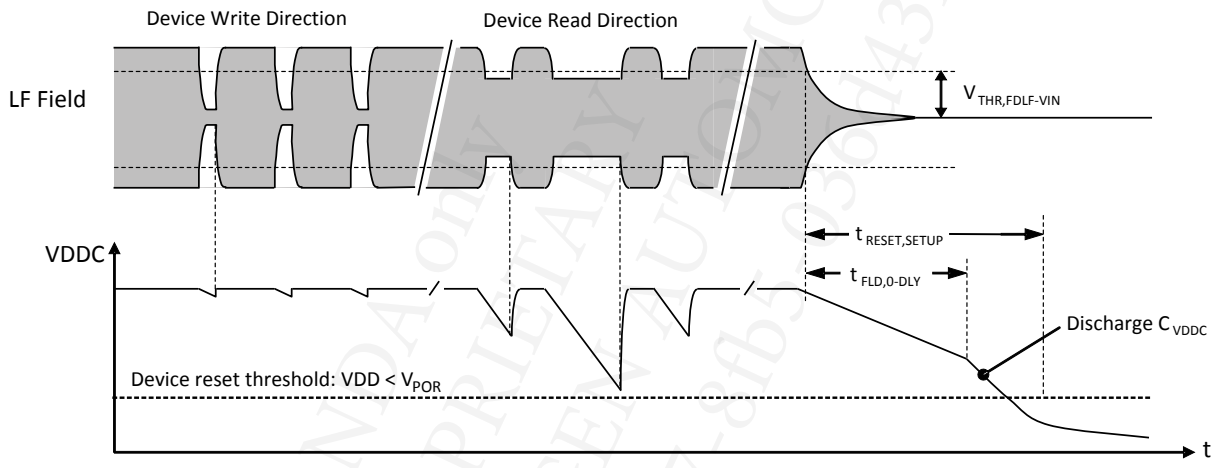


Figure 11. LF field reset timing

8.3.2 Demodulator

The front end features an envelope ASK demodulator able to detect the on-off keying (OOK) signal provided by the base station. The envelope is tracked on all three channels simultaneously and a combined demodulation signal derived from all three channels is provided to the immobilizer interface unit (IIU). The IIU performs serial to parallel conversion of the demodulator output signal, which is then provided to the CPU.

The demodulator circuitry (Figure 12) has been designed to fit the modulation characteristics of the WFS-5d transponder.

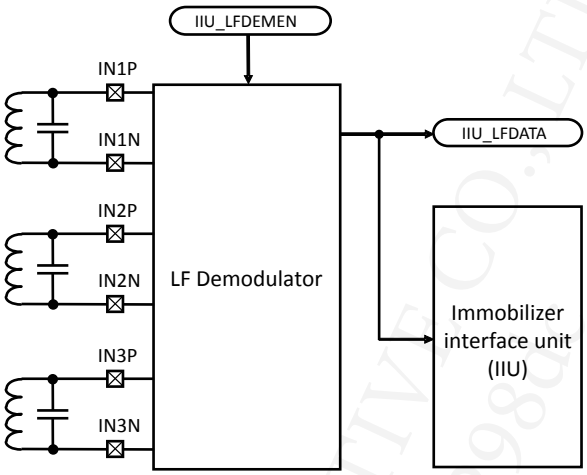


Figure 12. Demodulator Block Diagram

Once enabled, the demodulator tracks the input signal as long as no modulation is detected. The internal demodulator threshold is frozen automatically with the first received modulation and it is released again after the reception of a stop condition. The LF demodulator requires the settling time t_{ADLY} (Figure 13).

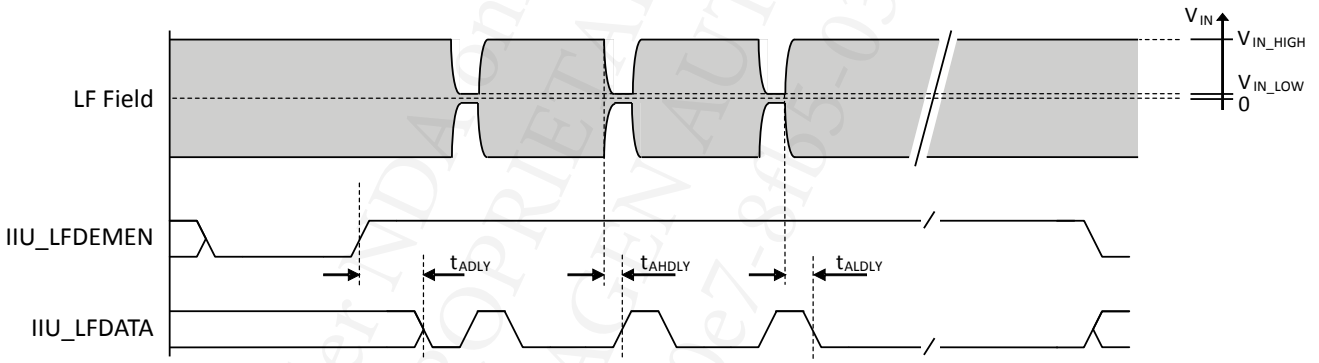


Figure 13. Demodulator Timing

The demodulator sensitivity applicable in write direction is illustrated in Figure 14 requiring a modulation index MI_{WR_LF} according to Equation 1.

$$MI_{WR\_LF} = \frac{V_{IN\_HIGH} - V_{IN\_LOW}}{V_{IN\_HIGH} + V_{IN\_LOW}} \quad (1)$$

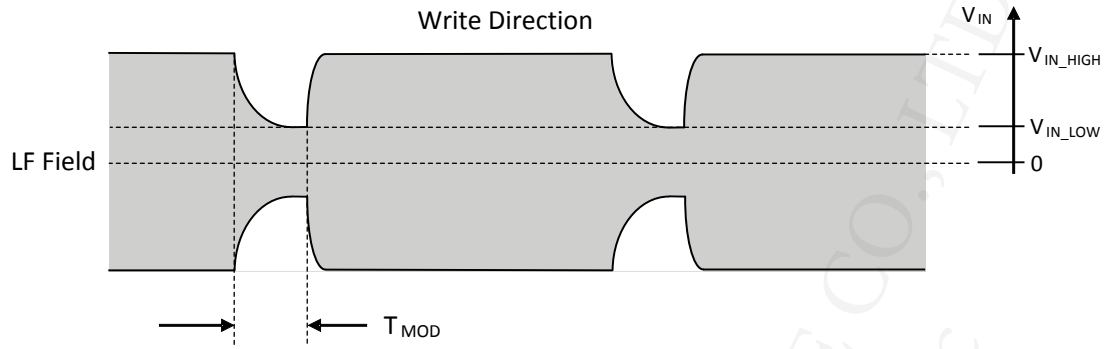


Figure 14. Demodulator Specification

The demodulator shall be disabled during an LF Field modulation phase.

8.3.3 Field detection

Independent of the device operating mode, the LF passive interface can detect the presence of an LF field on any channel and providing a corresponding signal to wake-up the device from POWER OFF state, or to interrupt device operation (see Figure 15).

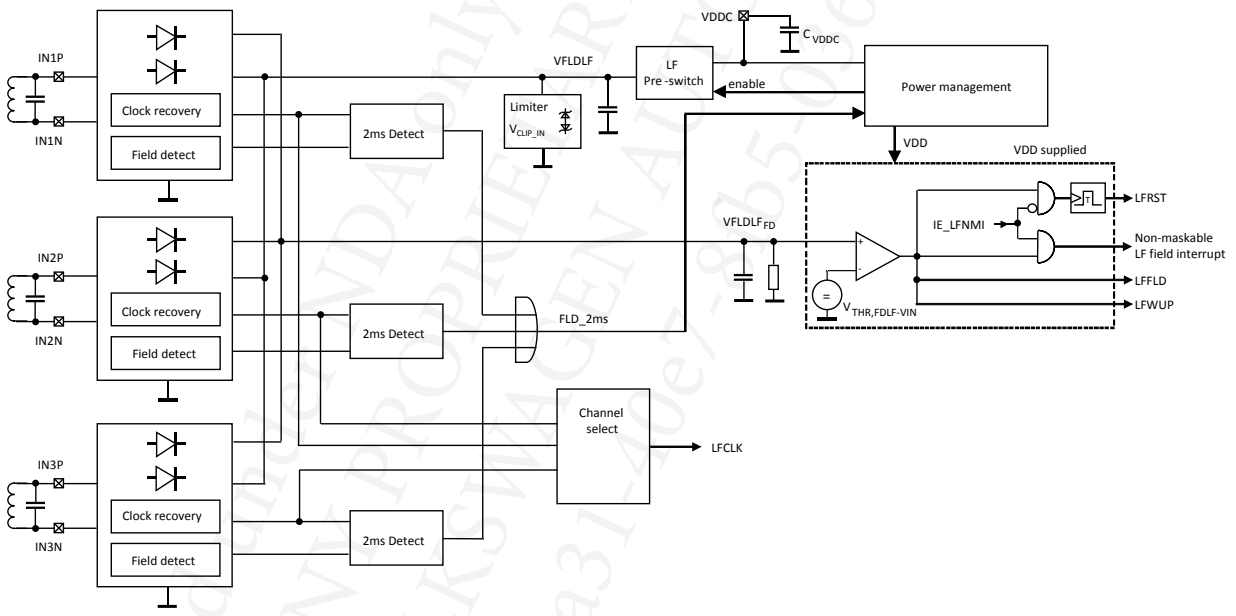


Figure 15. LF field detection circuitry

After a constant carrier is detected for the time $t_{FLD,HLD}$ at any channel, the LF pre-switch between VFLDLF and VDDC is closed and the field detection circuitry gets activated. It features an independent envelope detector that senses the voltage $VFLDLF_{FD}$ across the coil inputs (pins INxP and INxN) followed by a comparator. The LF field envelope is compared with a certain threshold, which is greater than the power-on reset threshold V_{POR}, forming the field detect flag (LFFLD). LFFLD turns high when the LF field on at least one channel exceeds the field detection threshold ($V_{THR,FDLF-VIN}$). LFFLD may be tested by the RISC controller when desired.

The output signal of the field detection circuit can be configured as reset or interrupt source (non-maskable interrupt).

In case the non-maskable interrupt is selected and considered operating from battery supply (BATTERY state) it is up to the application whether to force an LF field supply condition (LF FIELD state) or not. However, LFFLD being set is no guarantee that the available LF field is sufficient to power the device. A device power-on reset (VDDPOR) may occur in case of a weak LF field, which needs to be taken into account once the LF field supply condition is forced.

LFFLD goes low, if the input voltage on all three channels is below the field detect threshold $V_{THR,FDLF-VIN}$ for at least $t_{FLD,0-DLY}$ (see Figure 11). This triggers an active discharge of the capacitor connected to VDDC and consequently the device performs a power-on reset (VDDPOR) as soon as VDD falls below the power-on reset threshold V_{POR}. The base station can enforce a power-on reset (VDDPOR) of the device, if the applied LF field is below $V_{THR,FDLF-VIN}$ for the time $t_{RESET,SETUP}$.

8.3.4 Detection of 2 ms constant carrier

In order to activate the immobilizer, a constant carrier has to be applied to the LF input pins for 256 LF clock cycles ($t_{FLD,HLD}$). The LF field voltage has to exceed the 'active' field detection threshold $V_{THR,FD\_ATIC-VIN}$. After valid 256 LF clock cycles detection, the LF pre-switch is activated, the constant carrier detection is deactivated and the device commences with the immobilizer.

The demodulator is active during the constant carrier detection phase. If an ASK modulation is detected, the constant carrier detection is reset and starts over again. This mechanism ensures that the immobilizer is not activated during an LF active protocol.

8.3.5 Clock recovery

Every LF input channel has its own clock recovery. The channel selection block (see Figure 15) selects one channel with sufficient signal strength to drive the channel's clock recovery and forwards this clock as LFCLK to the rest of the system.

The NCF215B takes the clock always from the preconfigured channel.

8.3.6 Modulator (load modulation transponder)

The LF passive interface utilizes load modulation (absorption modulation) of the LF Field on all three channels simultaneously to send data to the base station. The modulation timing is determined by the RISC controller.

The NCF215B supports load modulation on the preconfigured channel only.

Load modulation is accomplished by applying an additional load (S2 closed, see Figure 10) across the coil inputs. The LF field modulator contains a standard modulator and a strong modulator. If the standard modulator is selected, the high ohmic path (R_{x+_LIN}, R_{x+_NLIN} and R_{x-_LIN}) is turned on (weak modulation), while selecting the strong modulator, both the low-ohmic path ($R_{x+\_LIN,strong}$ and $R_{x-\_LIN,strong}$) and the high ohmic path are enabled (strong modulation).

Besides the modulation load impedance, the load modulation characteristics depend on the source impedance of the external resonance circuit, the voltage limiter and the internal power consumption of the device. The applied load (S2) is different for each of the two half waves of the carrier to support clock recovery. The resistors R_x and the switches S1, S2 are implemented for each channel.

8.3.7 Immobilizer interface unit (IIU)

The immobilizer interface unit (IIU) allows convenient buffered read and write access to the immobilizer LF demodulator and LF modulator. With its various data path selection capabilities the IIU minimizes the CPU load for most power efficient immobilizer implementations.

The IIU allows an autonomous bit handling for transmission/reception/shifting of 1 to 8 bit. The HT calculation unit is not supported and must be bypassed. The controlling of the data transfer is supported by the generation of an interrupt or wake-up event (see Figure 16).

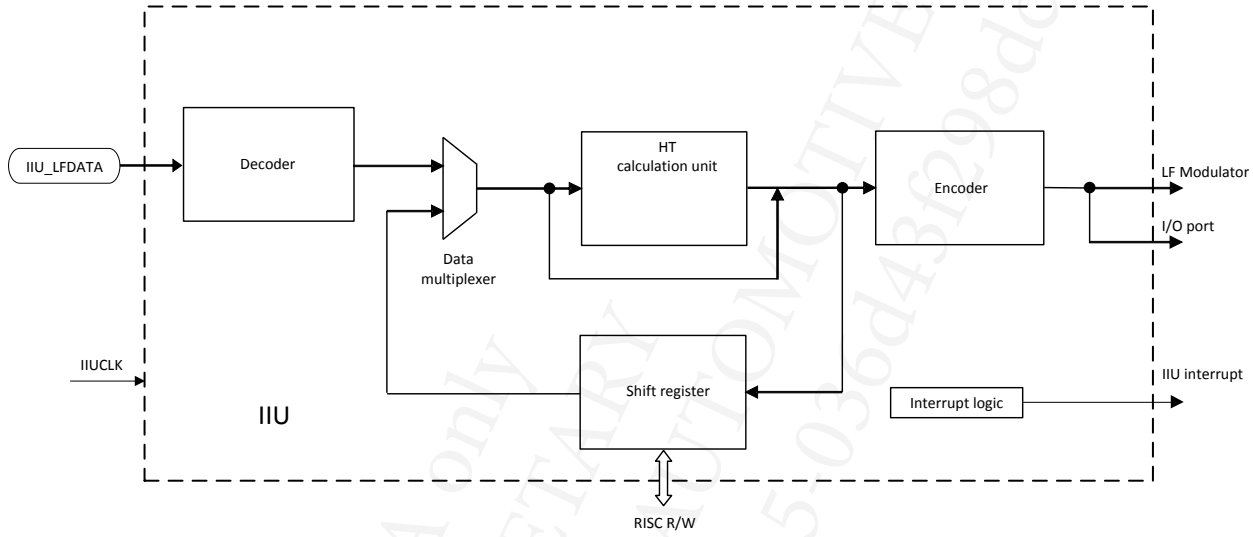


Figure 16. IIU block diagram

Several IIU clock sources can be selected. For WFS-5d compatible timing either the LFCLK or a 125 kHz clock source shall be selected.

With the help of an integrated timer, the time base for the LF demodulator (zero bit, one bit, stop bit) is controlled. The timer is also responsible to generate the LF modulator baudrate and to control the timing between data reception and transmission ($t_{WAIT,TR}$).

The encoded IIU output signal can be selected to modulate the LF field or to be directed to a port pin for general purpose use.

8.3.7.1 IIU decoder and encoder

For data reception the IIU applies binary pulse length modulation (BPLM) decoding (Figure 17) and converts the decoded bits via the 8 bit shift-register into byte format.

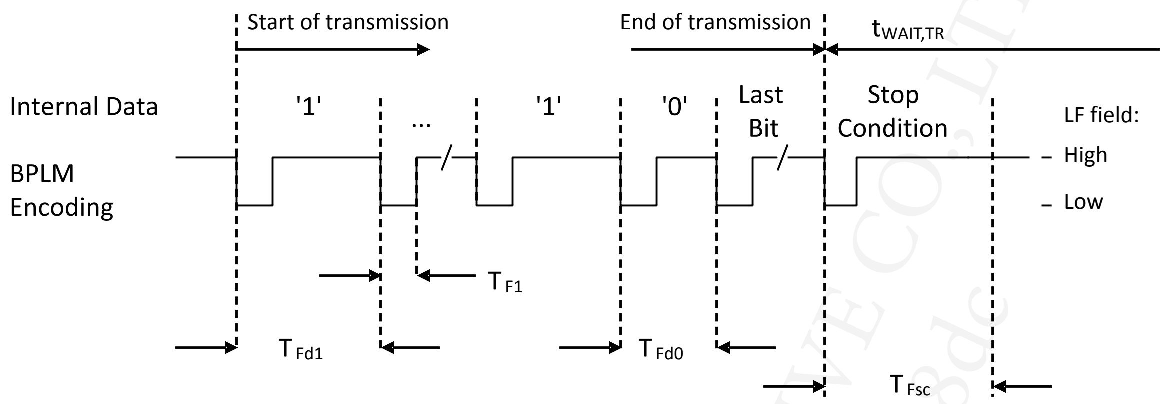


Figure 17. Data encoding - base station to NCF215A / NCF215B

For data transmission the IIU converts the bytes via the shift register into a bit stream and applies Manchester, CDP or NRZ encoding. Load modulation typically employs Manchester or CDP encoding (see Figure 18).

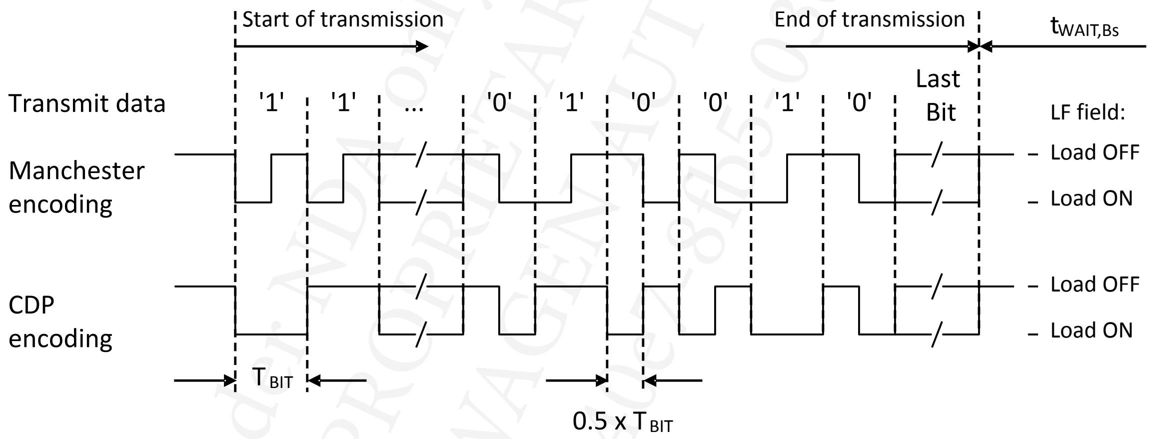


Figure 18. Data encoding load modulation transponder - NCF215A / NCF215B to base station

8.3.7.2 IIU general purpose mode

If not occupied by the immobilizer application, the IIU can be used for general purpose applications like implementation of a custom LF protocol. The shift register allows flexible control of transmitted data between 1 and 8 bits. Manchester, CDP, and NRZ encoding run with the same data rate T_{BIT}. This allows for convenient four state Manchester generation (Manchester zero and one generated with Manchester encoding, Manchester mark and space generated with NRZ encoding) with a constant data rate.

Access to the demodulated data line is given via the dedicated register bit IIU_LFDATA. The timer capture function can be used for demodulation. Besides the LF field clock and the peripheral clock a general purpose timer can be used for baudrate generation.

In order to implement variable transponder wait times $t_{WAIT,TR}$, transmission can be started on user request.

8.4 LF active interface (PKE receiver)

8.4.1 Introduction

The device supports communication for passive keyless entry (PKE) applications by a high sensitive 3D LF active interface that receives data with high selectivity around the nominal carrier frequency $f_{CARR,nom}$.

The 3D LF active interface consists of three identical LF active receiver channels, a baseband processing unit, wake-up pattern detection, and a payload receiver (see Figure 19). It uses a superheterodyne receiver architecture, which employs a highly integrated frequency synthesizer consisting of a 32 kHz crystal oscillator and a phase locked loop (PLL). The frequency synthesizer requires a 32.768 kHz crystal as sole external component.

The LF active interface autonomously monitors all three coil inputs for a modulated LF carrier and, if a pre-configured LF telegram is detected, a device wake-up is triggered and subsequent payload data will be buffered for post-processing with the micro-controller.

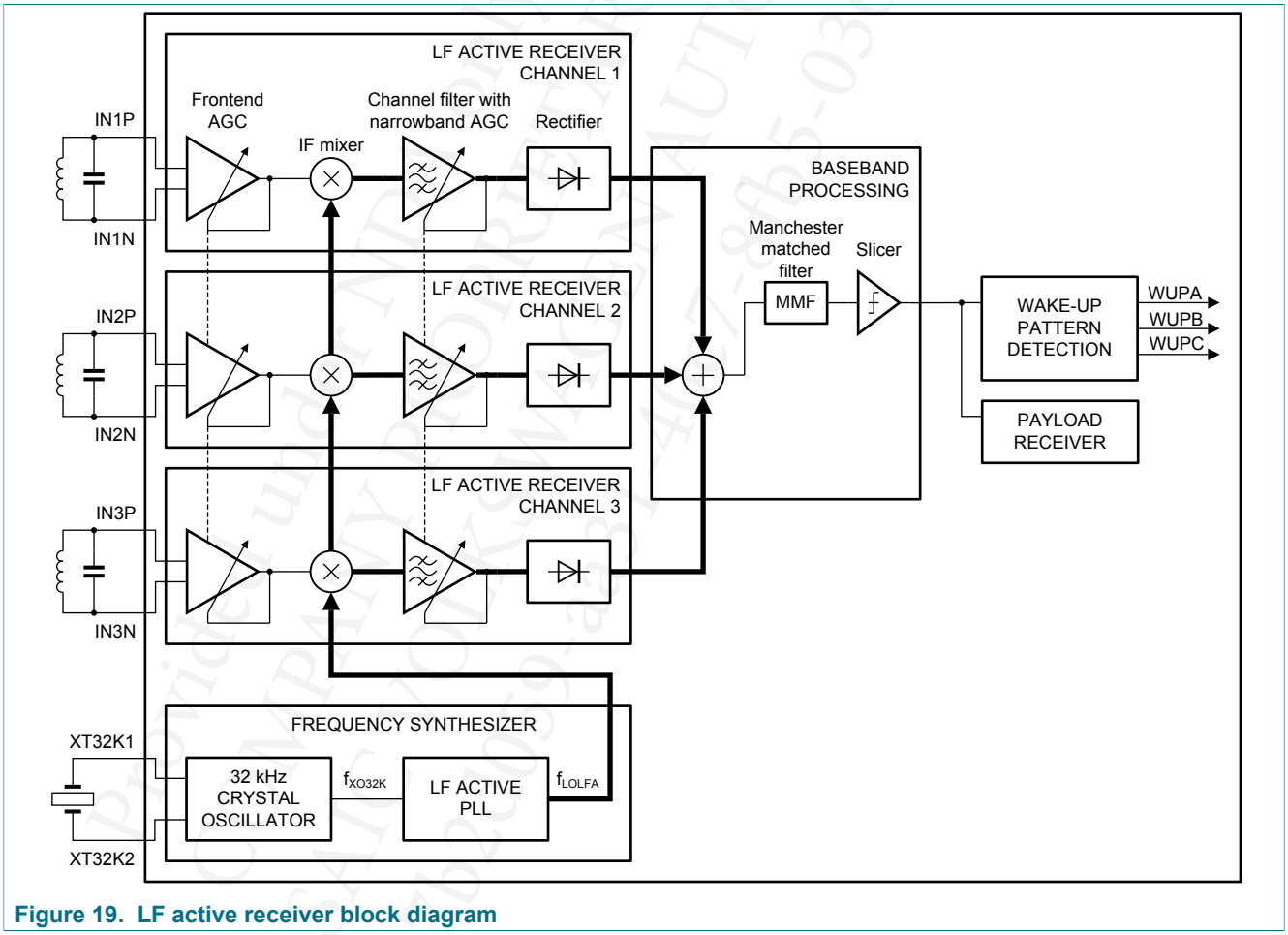


Figure 19. LF active receiver block diagram

8.4.2 LF telegram definition

The LF active interface supports LF telegrams with the following properties:

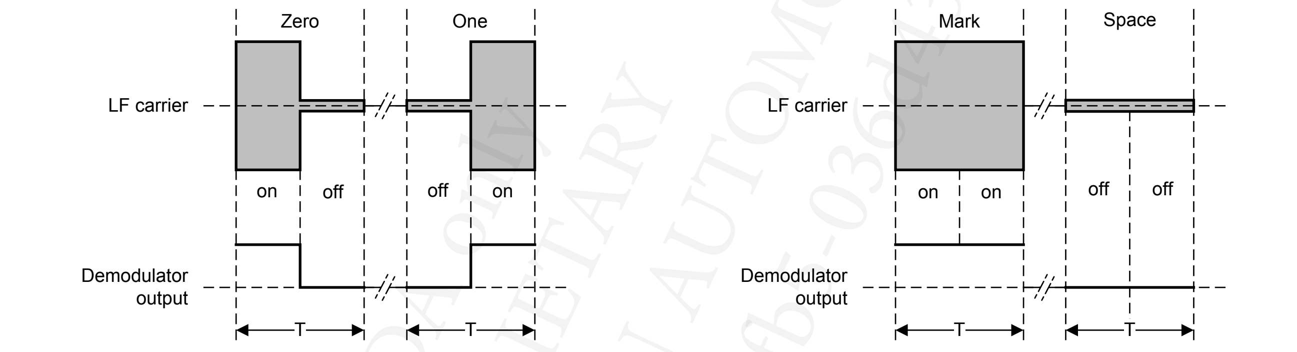
- LF carrier signal with carrier frequency f_{CARR}:

$$f_{CARR} = f_{CARR,nom} + \Delta f_{CARR} \quad (2)$$

- On-off keying (OOK) of the LF carrier signal
  - Signal shaping caused by the bandwidth limitation due to the transmitter and receiver coils' quality factor may apply.
- Manchester encoding according to Figure 20(a) with a bit period T:

$$T = T_{nom} + \Delta T \quad (3)$$

- The code violation section contains Manchester code violations according to Figure 20(b).



1. The waveforms shown here are for demonstration purpose only. The actual waveforms may deviate.

Figure 20. Regular Manchester code and Manchester code violations

The LF telegram structure consists of the run-in pattern, the wake-up pattern, and optional payload (see Figure 21):

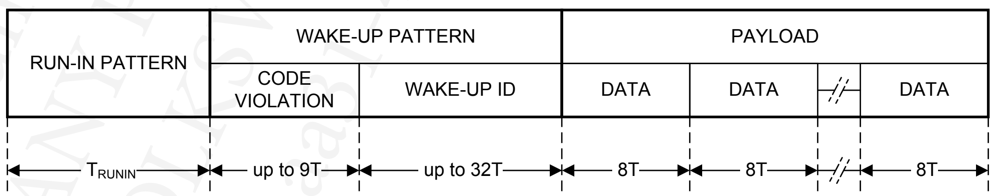


Figure 21. LF telegram structure

- **Run-in pattern**
  The run-in pattern is required for receiver settling and it shall preferably consist of Manchester zeros. The content of the run-in pattern is not evaluated. The run-in pattern shall have a minimum length T_{RUNIN}:

$$T_{RUNIN} = n_{RUNIN} \cdot T \quad (4)$$

- **Wake-up pattern**

The whole wake-up pattern is used for the wake-up pattern detection. The wake-up pattern consists of the code violation pattern and the wake-up ID.
The bits in the code violation pattern can be configured as regular Manchester code (zero or one) or as Manchester code violation (mark or space). The length of the code violation pattern is configurable and may contain up to 9 bits.
The length of the wake-up ID is configurable and it may contain up to 32 bits of regular Manchester code (zero or one).
Code violations in the wake-up pattern help to support telegram synchronization and to avoid that a wake-up pattern is found erroneously in a regular Manchester encoded data stream.

- **Payload data**
  The LF telegram may include payload data after the wake-up pattern. The payload is optional and may be omitted. Payload data is Manchester encoded (zeros and ones) and it is only supported in byte granularity (8T). The recommended maximum payload length shall not exceed 32 bytes.

NCF215A / NCF215B fully supports the LF telegram used by predecessor devices—e.g. NCF21A1/A2, NCF2157/58—as depicted in Figure 22.

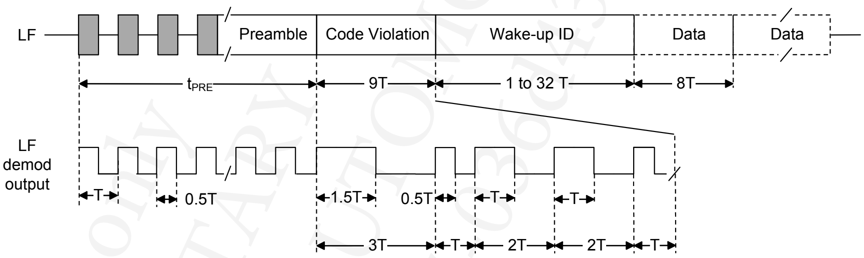


Figure 22. Legacy LF telegram

Please note that NCF215A / NCF215B requires some bits of the legacy code violation as additional run-in bits. Thus, the first few bits of the legacy code violation are not used for wake-up detection as depicted in Figure 23.

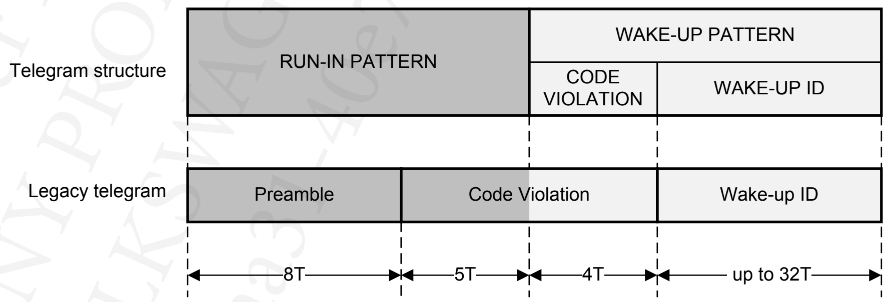


Figure 23. Mapping of legacy LF telegram

8.4.3 Frequency synthesizer

8.4.3.1 32 kHz crystal oscillator

The 32 kHz crystal oscillator can be operated independently of the LF active receiver and requires the supply voltages VBAT and VBATREG. The 32 kHz crystal oscillator uses a Pierce oscillator cell with gain control and features integrated load capacitors for the

external crystal. It is intended for the operation with an external crystal with a nominal frequency of $f_{XO32K,nom}$ and a nominal load capacitance of C_{L_XO32K}.

For LF active operation, the crystal oscillator frequency f_{XO32K} must always stay within the following boundaries:

$$f_{XO32K,nom} + \min(\Delta f_{XO32K}) \le f_{XO32K} \le f_{XO32K,nom} + \max(\Delta f_{XO32K}) \quad (5)$$

The device supports a clock fail detection, which is able to detect any stoppage of the 32 kHz crystal clock. This clock fail information can be configured as wake-up condition from the POWER OFF state or as interrupt source. The detection circuit requires a settling time of $t_{XO32KFAIL\_set}$ after it is enabled, during which time its output is invalid.

8.4.3.2 LF active PLL

The device features a fully integrate phase locked loop (PLL) to generate the local oscillator frequency $f_{LOLFA} = 3 \cdot f_{XO32K}$ for the superheterodyne receiver. Furthermore, the PLL provides clock outputs for the DC-DC converter and the timer system (LFAPLLCLK). The LF active PLL requires the supply sources VBAT, VBATREG, VLFA and VLFADIG.

8.4.4 LF active receiver channel and baseband processing

The LF active receiver has three identical receiver channels consisting of a frontend AGC, an IF mixer, a channel filter with narrow band AGC, and a rectifier section. It requires the supplies VBAT, VBATREG, VLFA and VLFADIG.

The frontend AGC is a controllable attenuator operated in a closed loop. It includes a level detector which adjusts the attenuation of the incoming signal in order to create an optimal signal level for the IF mixer.

The IF mixer is implemented as quadrature (IQ) image rejection mixer. By multiplication of the incoming signal with f_{LOLFA}, the IF mixer creates in-phase (I) and quadrature (Q) output signals, which are fed into the subsequent channel filter.

The channel filter is centered around the IF frequency $f_{IFLFA} = f_{CARR,nom} - f_{LOLFA}$. The channel filter is responsible for the selectivity around the wanted signal f_{CARR} and attenuates other unwanted signals outside the wanted band—in particular signals from wireless electrical vehicle chargers located around 85 kHz, which are attenuated with $a_{CF,85k}$. Simultaneously, the channel filter acts as baseband filter for the OOK modulated signal thanks to its narrow filter bandwidth B_{CF}.

The channel filter has an integrated narrowband AGC loop, which supports a constant level at the filter output going to the subsequent rectifiers. The AGC loop influences only the gain of the filter while the actual filter characteristics are maintained over the whole dynamic range.

The narrowband AGC reacts on the channel-filtered signal, i.e. the gain is mainly determined by the wanted signal. This is in contrast to the frontend AGC, which operates on the whole input spectrum and can therefore be driven by a strong unwanted signal. This is an intended behavior, as the frontend AGC must limit the input signal for the IF mixer. As a consequence, the frontend AGC and the narrowband AGC have their own control loop and they operate fully independently of each other.

The AGC supports a fast attack mode to ensure that any wanted signal is acquired quickly. After the end of the protocol, the AGC regulates back to the sensitivity level, which is reached after the AGC recovery time t_{AGC_REC} at the latest.

The rectifiers operate as envelope detectors retrieving the baseband information for further processing. The in-phase and quadrature signals are rectified separately.

The device supports common baseband processing of all three receiver channels by combining all six rectified signals (I and Q of channel 1 to 3, respectively) into one common baseband signal. The common baseband ensures rotation independent LF receiver performance provided that all three LF active inputs use similar LF antennas.

The common baseband signal is processed with a Manchester matched filter (MMF), whose output feeds into the slicer to digitize the signal. The digital slicer outputs are used as input signals for the wake-up pattern detection and the payload receiver.

In order to support common baseband processing, it is mandatory that all three LF active receiver channels operate at the same total gain. This is achieved by a common control of the frontend AGC and the narrowband AGC, respectively, in all three channels. Hence, the attenuation of the frontend AGC is determined by the strongest input signal of all three channels and the gain of the narrowband AGC by the strongest channel-filtered signal of all three channels. Please note that the frontend AGC and the narrowband AGC are still independent as mentioned above.

The LF active interface supports two different sensitivity modes G1M and G3M plus two desensitization modes D1M and D2M, which can be used to reduce the sensitivity temporarily in the application. The application shall consider a waiting time t_{ACT_set} after changing the receiver sensitivity.

8.4.5 Wake-up pattern detection

The wake-up pattern detection supports three independent wake-up patterns with identical configuration possibilities. Every wake-up pattern can be enabled, disabled, and configured individually. The individual configuration includes the content and the length of the wake-up pattern. Additional configurations are available to improve the pattern detection behavior under specific conditions, e.g. for high data rate offset (segmented correlator) or for very short wake-up patterns (strict correlation modes).

If the LF active receiver is enabled, the wake-up pattern detection searches continuously for all enabled wake-up patterns in parallel. If the incoming signal matches any of the enabled user programmed wake-up patterns, a wake-up event and an interrupt request is generated. If the device is in POWER OFF state, the wake-up brings it into BATTERY state.

The wake-up pattern detection features an optional error tolerance, which, when activated, tolerates between 1 and 7 wrong bits in the received LF signal. The error tolerance can support successful wake-up pattern detection in case single bits are destroyed by pulsed disturbers. Alternatively, it can be used to improve the sensitivity of the wake-up pattern detection. Please note that the activation of the error tolerance introduces ambiguity in the pattern matching process; e.g. if the error tolerance is configured to tolerate 1 wrong bit, a wake-up event is not only triggered when the programmed wake-up pattern is received but also if a pattern is received that differs by 1 bit from the programmed one.

8.4.6 Payload receiver

The payload receiver is only activated after a successful wake-up pattern match. It receives the payload data and buffers it in an 8 bit data register for further processing by the micro-controller. The micro-controller must fetch the received data byte in time before it is overwritten with the next received data byte. It is in the responsibility of the micro-controller to stop the payload receiver once all expected data bytes are received.

The application can configure whether the wake-up pattern detection searches for a wake-up pattern in parallel to the payload reception or not. In the latter case, the wake-up pattern detection becomes active, only after the payload receiver was stopped by the application.

8.4.7 Narrowband received signal strength indication (RSSI)

The narrowband received signal strength indication (RSSI, see Figure 24) supports LF input signal strength measurement over a wide dynamic range, starting below the sensitivity limit of the LF active interface and going up to $V_{RSSI,max}$. The measurement range can be extended on application level for very strong magnetic fields by use of the channel shorting resistors. The RSSI analog frontend is connected directly to the LF input pins and is arranged in parallel to the LF active interface (PKE receiver) and the LF passive interface (immobilizer). The RSSI analog frontend conditions the input signal for the subsequent Sigma-Delta ADC (SD-ADC) and the RSSI digital part. The steep digital filters allow excellent narrowband performance and suppress unwanted signals outside the wanted band. At the same time, the selected RSSI architecture excels with outstanding linearity and measurement accuracy.

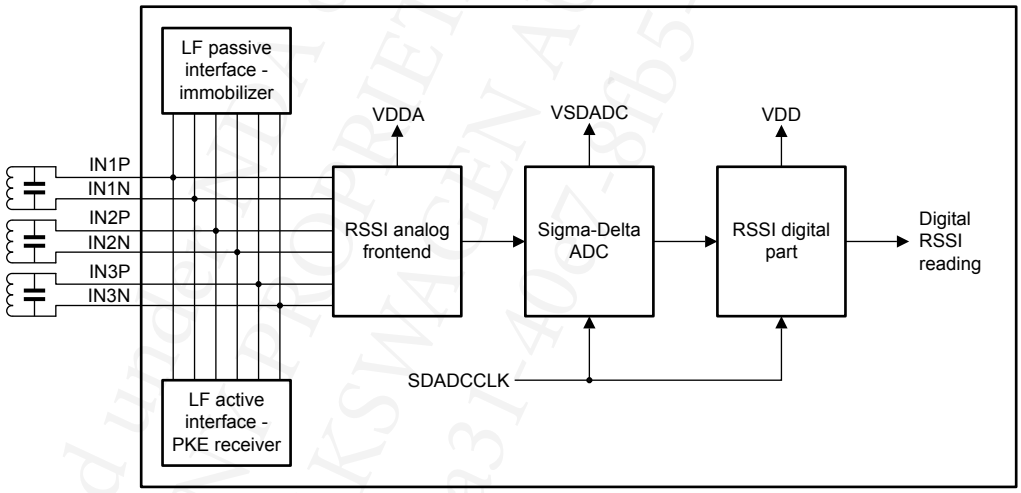


Figure 24. Narrowband RSSI block diagram

An RSSI measurement sequence consists in general of three consecutive single channel RSSI measurements. A precondition for the RSSI measurement is a constant carrier input signal on the selected LF input channel. Modulated input signals will lead to lower RSSI values caused by narrowband filtering and averaging over the measurement time.

Activation of the RSSI analog frontend turns off the frontend AGC of the LF active interface to avoid disturbance. The LF active interface can be kept on, however, reception of LF active protocols is not supported in this case.

8.4.7.1 RSSI analog frontend

The RSSI analog frontend in Figure 25 consists of:

- Channel shorting resistors
- Q factor adjustment
- RSSI attenuator
- Input signal selection
- Programmable gain selection
- Range overflow detector

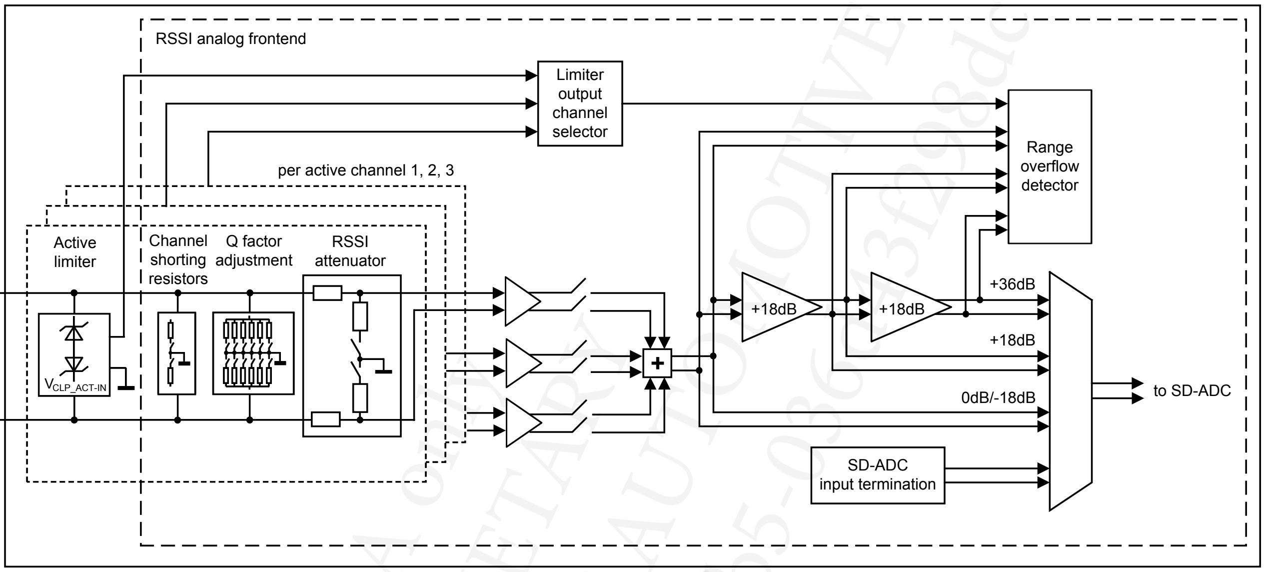
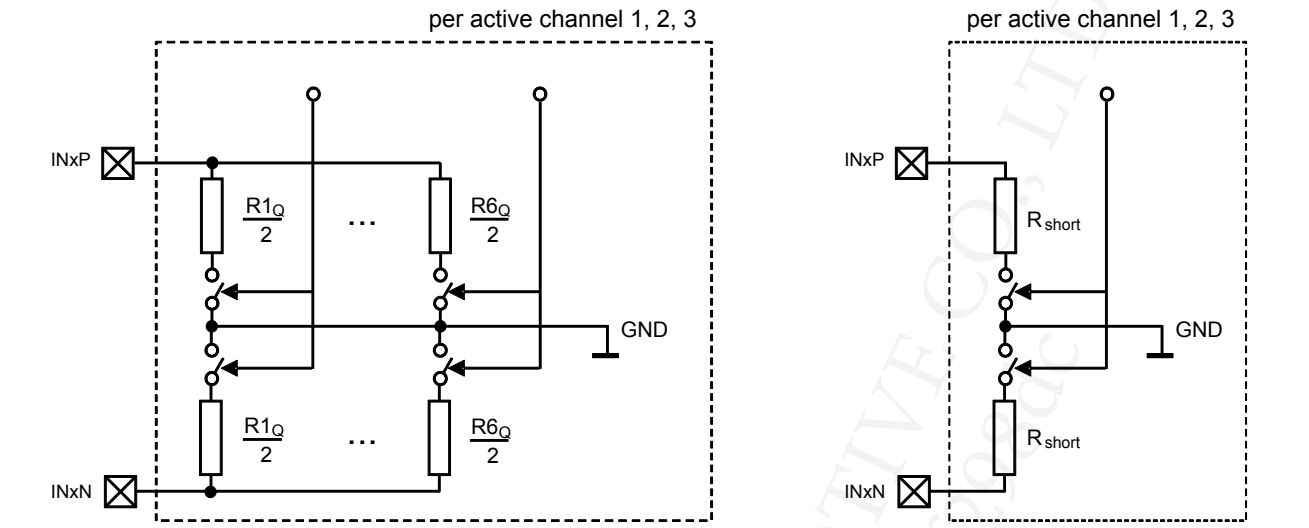


Figure 25. RSSI analog frontend

Channel shorting resistors

The channel shorting resistors R_{short} load the external resonant circuit and they are provided to attenuate the LF signal on individual RSSI channels (Figure 26b). When doing an RSSI measurement on one LF channel it is recommended to activate the channel shorting resistors on the other two LF channels to minimize errors caused by crosstalk between the three external coils. Additionally, the channel shorting resistors can be activated on the measured LF channel to extend the measurement range for very strong LF input signals that would otherwise exceed the range of the lowest gain stage.



a. Q-factor adjustment

b. Channel shorting resistors

Figure 26. Q-factor adjustment and channel shorting resistors

Q factor adjustment

The Q factor adjustment (Figure 26a) is provided to allow control of the Q factor of the external resonant circuit during RSSI measurement. The external resonant circuit is loaded with configurable resistors, which are divided into two equal parts that are connected to ground via switches. By providing six weighted resistors ($R1_Q$ to $R6_Q$) in parallel, meaningful resistor values can be chosen by switching on/off various combinations.

Optionally, the Q factor adjustment may be used for LF active protocol reception as well. In this case it is recommended to select the automatic Q factor adjustment deactivation when an LF passive protocol is detected. This avoids negative influence on the immobilizer performance which might be caused by additional loading of the external resonant circuit.

Input signal selection

The RSSI analog frontend allows the selection of one individual LF channel (IN1P/IN1N, IN2P/IN2N, IN3P/IN3N) or the sum of two or all three LF channels. For normal RSSI measurement only one LF channel shall be selected at a time. The summation of multiple LF channels can be used to assess the phase relationship between different LF channels.

Gain selection, RSSI attenuator, range overflow detector (indicator)

The device supports different gain stages—referred to as +36 dB, +18 dB, 0 dB, and -18 dB modes—to cope with the wide dynamic range of the input signal. The appropriate gain setting is identified with the help of fast range overflow detectors (indicators). Once the correct gain setting is found, the amplified signal is switched to the input of the SD-ADC for further processing.

The -18 dB mode is implemented by means of the RSSI attenuator. The application may decide to use the channel shorting resistor instead of the RSSI attenuator as range extension for strong input signals.

The range overflow detection operates on the whole frequency spectrum of the applied input signal, i.e. the wanted signal and potential interferers, and has configurable thresholds. In addition to finding the correct gain setting at the beginning of the measurement, the range overflow detection runs throughout the whole RSSI measurement cycle to check for any overflow condition. An overflow condition can appear, if the input signal increases significantly during the RSSI measurement cycle (e.g. caused by an increase of an interferer).

One part of the range overflow detection reuses active limiter output signals from the LF active interface (see Figure 25) to signal an overflow condition for very strong input signals.

Every device stores individual RSSI calibration values to correct gain errors of the different gain stages in order to get one continuous measurement range. Software routines for RSSI measurement and calibration are provided as C library functions to be linked to the application program.

8.4.7.2 RSSI digital processing

The digitized output from the SD-ADC is first filtered with a narrow digital bandpass filter centered around $f_{CARR,nom}$ (see Figure 27). Four different filter settings A to D are available to balance the wanted filter bandwidth ($B_{RSSI\_FILT\_A} > B_{RSSI\_FILT\_B} > B_{RSSI\_FILT\_C} > B_{RSSI\_FILT\_D}$) and filter settling time ($t_{RSSI\_FILT\_A} < t_{RSSI\_FILT\_B} < t_{RSSI\_FILT\_C} < t_{RSSI\_FILT\_D}$). All four filter settings are designed to suppress signals from wireless electrical vehicle chargers located around 85 kHz in an optimal way. Narrower filter settings can be selected to suppress other interferers, which are closer to the target frequency.

The digital bandpass filter is followed by an amplitude measurement unit, measuring the peak amplitude, and an averaging unit. The averaging factor is configurable and a higher number gives more accurate and stabler RSSI readings.

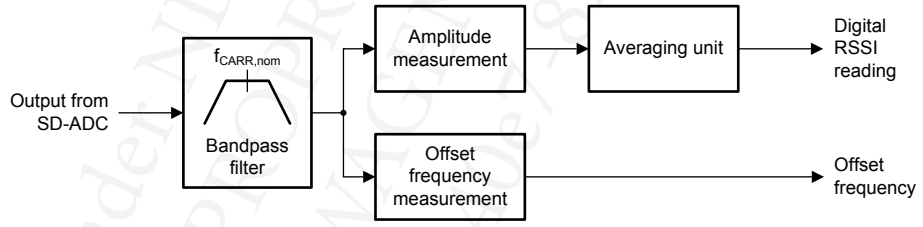


Figure 27. RSSI digital processing

The device supports a unique method for interferer detection within the filter bandwidth. Using different amplitude measurement methods, the device can reliably detected whether one or several signals are present. If only one signal is present, the offset frequency measurement unit distinguishes, if it is a wanted signal around the nominal frequency or an interferer with a different frequency. If an interferer is detected, the application may perform a second RSSI measurement with the wanted signal turned off to measure only the interferer amplitude. The amplitude of the wanted signal can then be calculated from the RSSI readings of the two measurements.

8.4.8 Interval timer and real-time clock

The interval timer can generate periodical events in order to wake-up the device from POWER OFF state. The wake-up time is configurable.

The real-time clock features a 16 bit register holding minutes, seconds, and fractions of seconds with a resolution of nominal 1/16th of a second. The register content can be used as a time stamp in protocols or to display the time. The application can extend the time stamp interval with additional software counters stored in battery supplied registers. The real-time clock supports wake-up events independently from the interval timer.

The interval timer and the real-time clock use the same counter chain, which is operated with the 32 kHz crystal clock (XO32KCLK). Due to the continuous operation in the regulated battery supply domain VBATREG, both timers operate independently of the supply state.

When the interval timer is running it provides a divided clock (LPDIVCLK) with 2 kHz nominal clock speed.

8.4.9 LF active post-wake-up timer

The LF active post-wake-up timer is intended to support protocol timings which use the incoming LF protocol as timing reference. Typical reference time points are the detection of the wake-up pattern or the end of the LF protocol.

The LF active post-wake-up timer is an incrementing timer with a compare register. Most of the time the timer is off and held in reset. The timer starts counting automatically, when a valid LF active wake-up pattern is recognized. If the timer value reaches the value stored in the compare register, an interrupt is raised and the timer is reset again. The timer supports a single shot and a multi shot mode. In single shot mode, the timer is stopped after the compare match, whereas the timer starts incrementing again in multi shot mode to support the generation of back-to-back timing intervals. The application can modify the compare register or stop the timer at any time.

Optionally, it is possible to select the reception of a new data byte by the LF active receiver as an additional reset source. This is required, if the end of the protocol is requested as reference time point. The LF active post-wake-up timer is then reset with the reception of every single data byte and it starts incrementing again immediately thereafter.

The LF active post-wake-up timer is clocked with the accurate 32 kHz crystal clock (XO32KCLK) and it is supplied by the regulated battery supply domain VBATREG.

8.5 LF tuning capacitors

The LF tuning function provides a facility for adjusting the input capacitance seen at the LF input pins, INxP and INxN. This allows fine tuning of the resonant frequency of the external antenna circuit to optimize the reception of an incoming LF signal.

The tuning capacitance is implemented as a configurable array of capacitors connected between the LF input pins INxP, INxN, and ground as depicted in Figure 28. The tuning capacitors support a resolution of C_{STEP} and they can be set for each LF input individually in 32 steps from 0 to $31 \cdot C_{STEP}$.

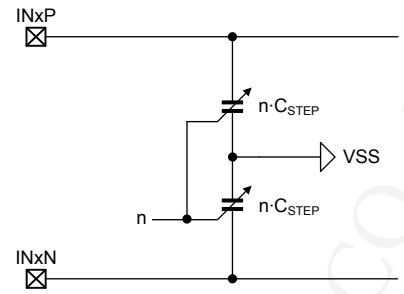


Figure 28. LF tuning capacitors

The effect of the LF tuning capacitors depends on the input signal strength. For weak input signals—typical for LF Active operation—the LF front-end rectifier has no influence. The tuning capacitors operate in series to the LF input, thus, their effective capacitance seen at the LF input pins is halved. The effective input capacitance C_{IN} for this case is given in Equation 6:

$$C_{IN} = C_{IN\_ACT} + (n \cdot C_{STEP}) / 2 \quad (6)$$

For strong input signals—like for LF Passive (immobilizer) operation—the LF front-end rectifier connects one LF input to ground during every half-wave. This means that one side of the LF tuning capacitor is grounded as well and, thus, does not contribute. The effective input capacitance C_{IN} seen between the pins INxP/INxN for this case is given in Equation 7:

$$C_{IN} = C_{IN\_PAS} + n \cdot C_{STEP} \quad (7)$$

To account for this behavior, the device supports two different user configurable sets of tuning values, which are optimized for LF Active operation with weak input signals and LF Passive (immobilizer) operation with strong input signals. The selection between these two settings is done automatically dependent on the battery supply level and the recognition of an LF Passive protocol.

8.6 RISC controller

The NCF215A / NCF215B is powered by NXP's 3rd generation low power 16 bit extended Micro RISC Kernel (MRK III) with enhanced instruction set (MRK III-e), which controls device operation in LF FIELD and BATTERY state.

The MRK III utilizes a Harvard architecture featuring a 16 bit ALU and supports hardware extended MUL and DIV operations. The instruction set supports 8 bit and 16 bit operations and is optimized for C programming. Due to the efficient 2-stage pipeline (fetch/execute), most instructions execute in a single machine cycle (two clock cycles), resulting in ultra-low power consumption.

The MRK III provides 64 kByte linear data address range and 128 kByte linear code address range, powerful addressing modes and high code density. Besides, the MRK III supports a power saving mode and code/data protection mechanisms (privilege modes).

8.6.1 Power saving modes

8.6.1.1 RUN mode

In RUN mode the MRK III is regularly clocked and processes the program instructions.

8.6.1.2 IDLE mode

The IDLE mode is a power saving mode and invoked via the command IDLE. In IDLE mode the MRK III CPU is halted by gating the internal clock signal for the MRK III CPU.

IDLE mode can only be entered, if the level sensitive wake-up signal of the MRK III controller is not active. As soon as the wake-up signal becomes active, the MRK III resumes operation and switches to RUN mode.

8.6.2 Privilege modes

8.6.2.1 SYSTEM mode

In SYSTEM mode, the NXP implemented firmware (system code, e.g. transponder emulation) is processed. SYSTEM mode is entered by a software interrupt via the SYS command or by serving a system interrupt request. SYSTEM mode is also used while executing the BOOT routine and during MDI operation.

After completing the system routines, the MRK III switches back to USER mode and control is given back to the application program.

8.6.2.2 USER mode

The application program is executed in USER mode. In USER mode, all MRK III instructions can be processed. If the MRK III is in SYSTEM mode, USER mode is entered via the USR command or by serving a user interrupt request.

8.6.3 Memory organization

The memory management unit (MMU) provides access to the different memories for code and data storage. It supports strict separation between memory areas assigned to SYSTEM or USER mode.

8.6.3.1 System code memory

The NXP implemented system ROM functions contain (see Section 8.22)

- Boot routine
- Transponder emulation functions
- In-circuit Monitor and Download Interface

The system code memory is not visible for the application.

8.6.3.2 System data memory

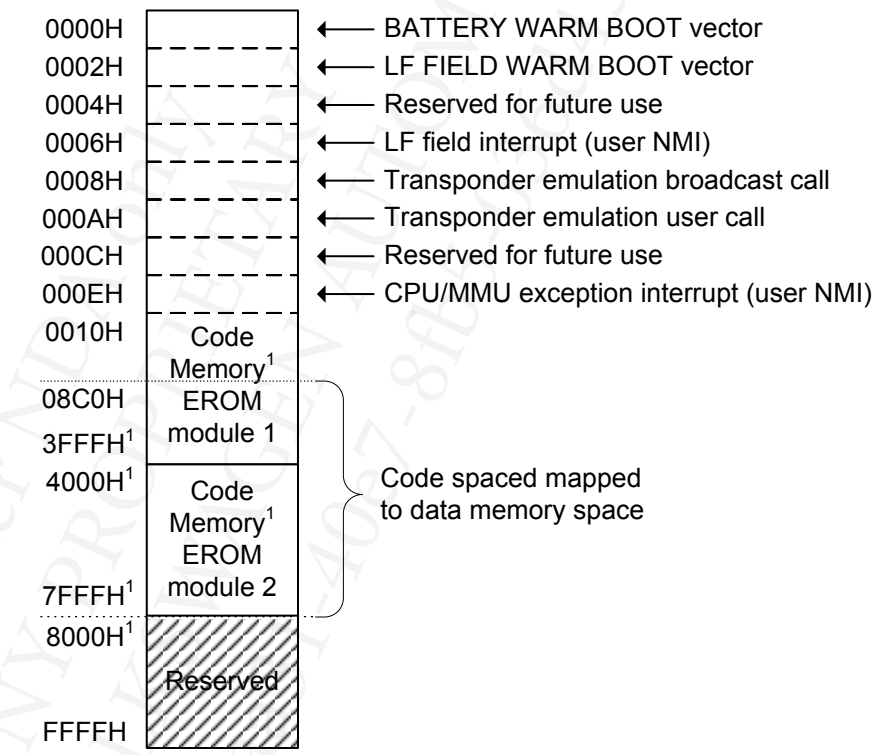
The NCF215A / NCF215B has a dedicated data memory area including system RAM for device execution in SYSTEM mode. The system data memory area is not visible for the application. All system calls, the built-in transponder emulations and the in-circuit debugging functions use the system RAM.

8.6.3.3 Application code memory

Application code and read-only data reside in EROM memory. Each application code instruction is either 16 or 32 bit long and thus occupies two or four bytes of EROM memory, respectively (see Figure 29).

For a battery wake-up event or in a case EROM execution of the immobilizer is selected, the application code is started at the corresponding BATTERY or LF FIELD WARM BOOT vector after the BOOT routine.

The EROM has a size of 64 kBytes and consists of two identical memory modules, 1 and 2, with a size of 32 kBytes each. EROM module 1 is unconditionally available upon each entry to EROM application code. EROM module 2 is conditionally enabled depending on an EEPROM device configuration. In addition, the application can make use of a provided system call to enable or disable EROM module 2, based on the application needs. As EROM module 2 requires a static bias current of ΔI_{DD_EROM2} when powered up, it is strongly advised to keep EROM module 2 disabled if not needed, which is e.g. recommended for a custom EROM immobilizer implementation.



1. The NCF215A / NCF215B can support up to 64 kByte of application code memory. The actual amount of available application code memory and the end address of the code memory space may vary depending on an orderable type number. For details contact your local NXP sales representative.

Figure 29. Application code memory

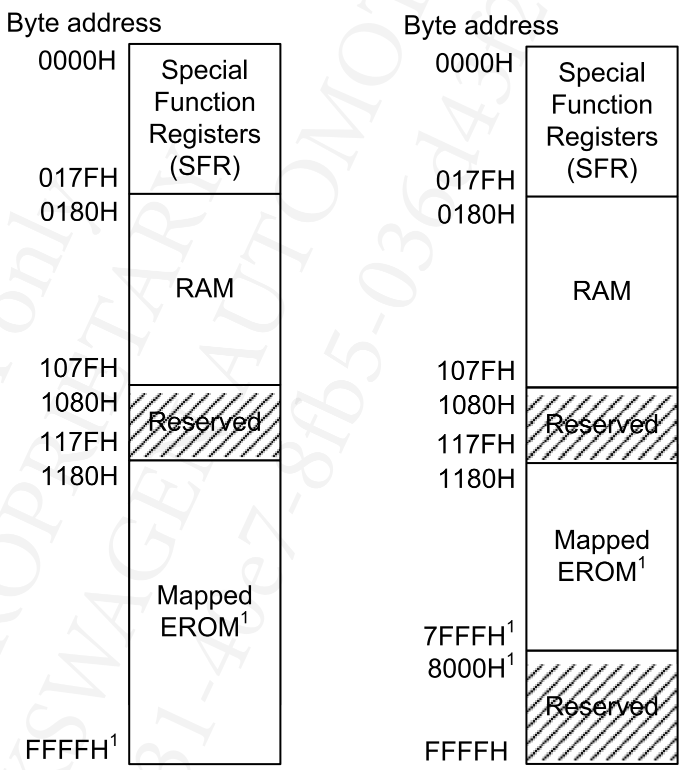
8.6.3.4 Application data memory

The data memory address space is split to cover the Special Function Registers (SFR) and the User RAM (Figure 30). The SFR enable full read/write access to the peripherals. The User RAM provides memory for volatile application data and stack storage and is

available for the application program without any limitations, because device execution in SYSTEM mode uses system RAM only. The stack starts at the end of the User RAM and grows with decreasing addresses.

In order to give access to constant data stored in the EROM (like look-up tables, constants, etc.) the unoccupied data address range is mapped to the code memory with the same logical address. Since the lower addresses of the application data memory are already used by the SFR and RAM, the EROM mapping starts at addresses after the RAM section. Thus, the EROM code memory content at addresses corresponding to the SFR and RAM sections in the data memory cannot be accessed via data mapping. Although the instructions in the code memory have word granularity, read-only data can also be accessed with byte granularity (byte address = 2 × word address).

The memory mapping scheme supports the standard ANSI-C memory model and avoids performance losses caused by generic pointer types, which are able to address different memory types dynamically.



1. The NCF215A / NCF215B can support up to 64 kByte of application code memory. The actual amount of available application code memory and the end address of the code memory space may vary depending on an orderable type number. For details contact your local NXP sales representative. The left figure shows 64 kByte and the right one 32 kbyte of application code memory as examples.

Figure 30. Application data memory

The NCF215A / NCF215B provides ultra-low power (ULP) serial EEPROM for persistent application data storage. The ULP EEPROM is intended for the immobilizer and remote keyless entry applications.

The ULP EEPROM is not mapped into the application data memory. It is only accessible via the ULP EEPROM interface.

8.6.4 CPU/MMU exceptions

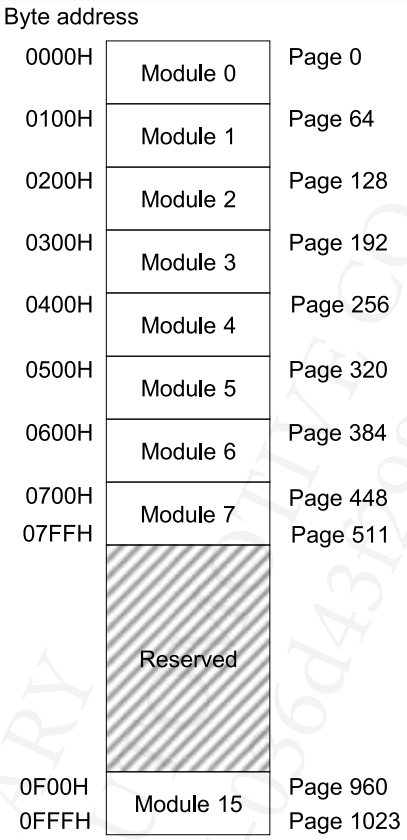
The CPU and the MMU provide means to detect forbidden execution attempts. This function can be enabled and disabled by means of an EEPROM configuration. If it is enabled, either a device reset or the CPU/MMU exception NMI is generated if one of the following conditions is detected:

- Attempt to execute an illegal command code
- Attempt to make a stack access with the stack pointer unequal to a word address
- Attempt to access an unassigned memory range
- Attempt to access EROM module 2 when it is powered down

8.7 ULP EEPROM

The ultra-low power (ULP) serial EEPROM is intended for persistent data storage for the immobilizer, boot routine and system functions in ROM and the application software. The ULP EEPROM consists of up to 9 modules (module 0 to 7 and module 15). In Figure 31 the ULP EEPROM data memory map is given in case 2048 Byte EEPROM (module 0 to 7) plus 256 Bytes for module 15 is actually available. In this case the application has full read/write/program access to modules 0 to 7. The only exception is pages 0 to 7, which are specially protected and do not allow direct read access or alteration. Module 15 holds trim and configuration data and can only be read but not written or programmed by the application (note: some specific locations may be programmed with a dedicated system call).

Each ULP module consists of 64 pages containing 4 byte (32 bit) each. The ULP modules are optimized in terms of power consumption for read access and programming by having a separate power-on bit for each module.



1. The NCF215A / NCF215B can support up to 2048 Byte of ULP EEPROM (excluding module 15). The actual amount of available ULP EEPROM and the available modules may vary depending on the type number. Here the ULP EEPROM data memory map is given in case the actual available EEPROM is 2048 Bytes. For details contact your local NXP sales representative.

Figure 31. ULP EEPROM data memory map (2048 Byte EEPROM configuration)

8.7.1 Available ULP EEPROM modules

The NCF215A / NCF215B supports up to 2048 Byte ULP Serial EEPROM (excluding module 15). The actual amount of available ULP Serial EEPROM and thus the number of available EEPROM pages may vary depending on the type number. For details contact your local NXP sales representative. The actual ULP EEPROM data memory map is dependent on the actual amount of available ULP Serial EEPROM.

8.7.2 ULP module 15

Independent from the actual amount of available ULP Serial EEPROM supported, ULP module 15 is always available and contains the 64 bit chip information consisting of the 32 bit serial number (SN) and the 32 bit chip information (CINF). Further, ULP module 15 locates the device configuration pages. Module 15 contains trim and configuration data in the reserved areas.

All pages except 1004 to 1007 are readable by the MRK III CPU core. The pages 960 to 975 and 992 to 1023 contain factory programmed data which can not be altered. The pages 976 to 991 locate the device configuration data (DCFG) which can only be modified in INIT mode (see Section 8.21) via the Monitor and Download Interface (MDI).

To enable compatibility to future devices, it is not recommended to store any other data into the DCFG area.

8.7.3 ULP EEPROM interface

The access to the NCF215A / NCF215B memory modules is restricted to system call functions only. Please refer for detailed description of these application software calls to the WFS-5c_MRKIII-ROM-LIB documentation ([3]).

The memory modules consist of 256 bytes each and are essentially bit oriented (Figure 32). The ULP EEPROM interface provides byte oriented read access via an 8 bit data register to minimize the CPU load. Programming of the ULP serial EEPROM is supported on 32 bit pages only. An internal state machine handles the low level access to the module. The interface performs the read/write and programming operations autonomously and indicates the status via busy flag and optional wake-up from idle mode.

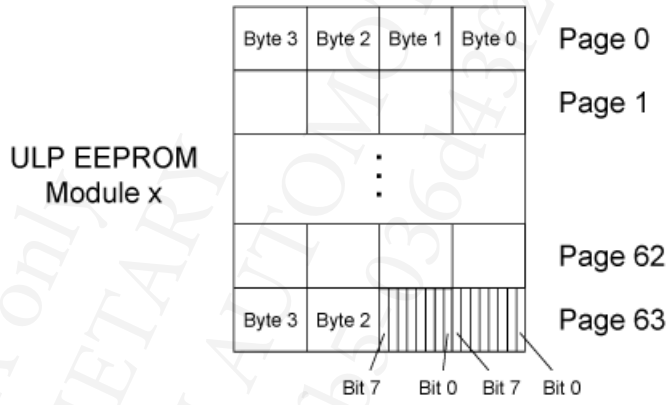


Figure 32. ULP EEPROM module

The internal ULP EEPROM interface contains an address register with bit addressing capabilities and auto-increment feature (modulo 32 bit for write access). The auto increment function allows reading of consecutive bytes/bits without additional access to the address register.

8.8 Interrupt system

The NCF215A / NCF215B contains an interrupt controller featuring 15 hardware interrupt priority levels. If more than one hardware interrupt request is pending at the same time the source with the highest request level is selected, independent of the RISC controller privilege mode (SYSTEM or USER mode).

The priority levels for LF field detection, CPU/MMU exception and user hardware interrupts are fixed. All user hardware interrupts use one common interrupt vector, which address is defined by the application via a dedicated SFR. This allows flexible software controlled handling of interrupt priorities, dynamic assignment of different interrupt service routines and the definition of distinct interrupt service routines for different applications.

The application can switch dynamically between single or nested interrupt execution and it can decide whether a selected event causes an interrupt or a wake-up event.

8.8.1 Interrupt sources

The interrupt sources are summarized in Table 6. Every interrupt source has a dedicated interrupt request flag. Maskable interrupts have additionally an interrupt enable bit. If an interrupt source is used as user and system interrupt two different interrupt enable bits are provided to allow separate control in every mode.

The supported interrupt types are maskable system interrupts (System), maskable user interrupts (User) and non-maskable user interrupts (User NMI). Interrupt sources can be level sensitive or edge sensitive.

Table 6. Interrupt sources

Interrupt Description	Interrupt type	Sensitivity
LF field interrupt	User NMI, System	Edge
CPU/MMU exception interrupt	User NMI, System	Edge
Port interrupt	User	Edge
Timer 0 interrupt	User, System	Edge
Timer 1 compare interrupt	User, System	Edge
Timer 1 capture interrupt	User, System	Edge
Alternative port interrupt	User	Edge
System timer 0 interrupt	System	Level
Immobilizer interface unit interrupt	User, System	Level
ULP EEPROM interrupt	User, System	Edge
ADC interrupt	User, System	Edge
AES calculation unit interrupt	User, System	Edge
Random number generator interrupt	User, System	Edge
RSSI interrupt	User	Level
Interval timer and real time clock interrupt	User	Level
LF active preprocessor interrupt	User	Level
SPI 0 interrupt	User	Level
SPI 1 interrupt	User	Level
Timer 2 interrupt	User	Edge
LF active monitors interrupt	User	Level
Motion sensor interface interrupt	User	Level
VBAT brownout monitor interrupt	User	Level

8.9 Timer/Counter 0, 2

Timer/Counter 0 and Timer/Counter 2 are identical.

Timer/Counter 0/2 is a 16 bit timer/counter with 12 bit pre-scaler and can operate as interval and event counter, as digital modulator or as clock divider. Timer 0/2 is also suitable as alternative clock source for the immobilizer interface unit and digital modulator.

Timer 0/2 has two operating modes, auto-reload mode and single shot mode. For auto-reload mode, a 16 bit reload register is provided (see Figure 33).

Different clock sources can be applied (RCCLK/2, XCLK, TMUX0CLK, TMUX1CLK). The timer can run with the undivided clock to achieve a best possible resolution even with slow clock sources.

If Timer 0/2 reaches the zero value, an interrupt is generated and a control line (TxLINE) can be set, cleared or toggled. This allows the creation of a synchronized digital bit stream or a divided clock output. The output TxLINE of Timer 0/2 is connected to selected I/O ports and it is available as capture input for Timer 1.

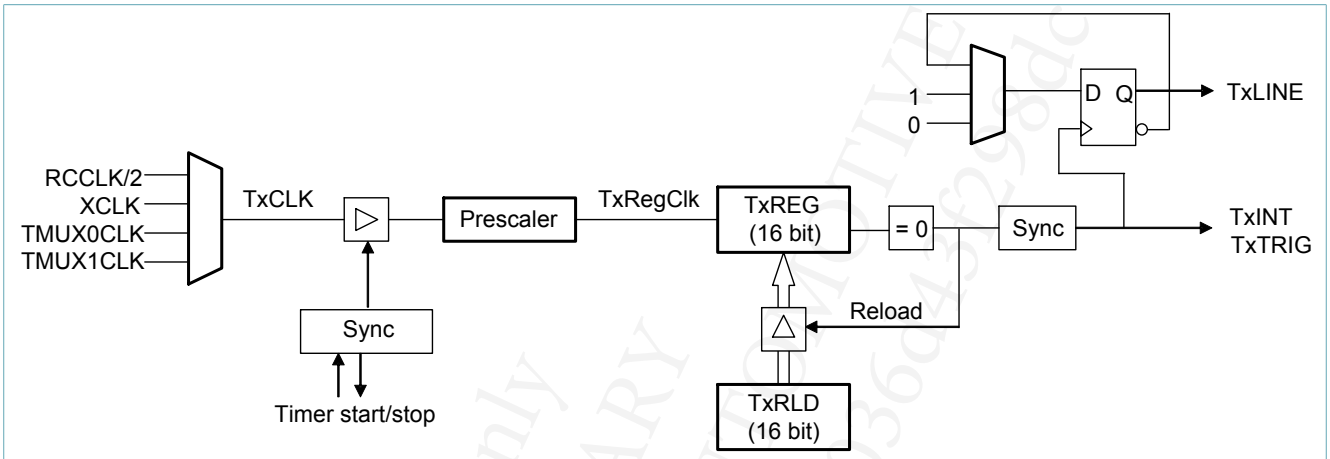


Figure 33. Block diagram of Timer 0/2

The timer starts by loading the reload value from register TxRLD into register TxREG. Afterwards, it counts down automatically. Reaching the zero value, timer register TxREG is reloaded with the value from reload register TxRLD, an interrupt request is generated and other peripheral functions are triggered.

8.10 Timer/Counter 1

Timer 1 is an 8/16 bit timer with 12 bit prescaler and is intended as interval and event counter for general purpose applications, as demodulator or signal generator and modulator. Together with Timer 0 it can be used as versatile clock measurement and/or trimming unit. Timer 1 features four operating modes (see Table 7).

Table 7. Operating Modes

Mode	Mode description
0	16 bit timer register with 16 bit compare and 16 bit capture register
1	16 bit timer register with 16 bit compare and 16 bit capture register in single shot operation
2	8 bit timer register with two 8 bit compare and two 8 bit capture registers
3	8 bit timer register with one 8 bit compare register, two 8 bit capture registers and one 8 bit guard time register for capture event processing

In all modes, an interrupt is generated if a compare event or a capture event is generated. Further, a reset upon capture and/or compare event is selectable. A capture event can be triggered on the signals rising edge, falling edge or on both signal edges, dependent on the configuration.

The input signal which is used as capture source is sampled with the gated timer clock T1CLK. Two samples are necessary to decide whether the input has a rising or falling edge. Thus, the low and the high pulse of this signal shall be longer than 1/T1CLK in order to be properly processed.

When selected, the capture mechanism is only active, if the timer is running. The first sample after start is discarded and the capture logic is initialized instead, i.e. no capture event will be generated, even if the first sample after start is different to the last sample of the previous run.

8.10.1 Operating modes

8.10.1.1 Mode 0

In Mode 0 Timer 1 is a synchronous 16 bit timer / counter with 12 bit prescaler, providing a 16 bit compare and a 16 bit capture register. The timer is operating continuously in auto reload mode, thus allowing generating a divided clock output at an I/O port. On a timer event, a control line or an I/O pin can be set, cleared or toggled (see Figure 34).

The timer register T1REG is implemented as incrementing counter and its content is continuously compared to the buffered compare value T1CMPSync. If both registers match an interrupt request is generated and the peripheral functions are triggered.

T1REG is cleared automatically, if selected. The compare register T1CMP has an internal synchronization stage, ensuring safe operation even if the value of T1CMP is changed when the timer is running.

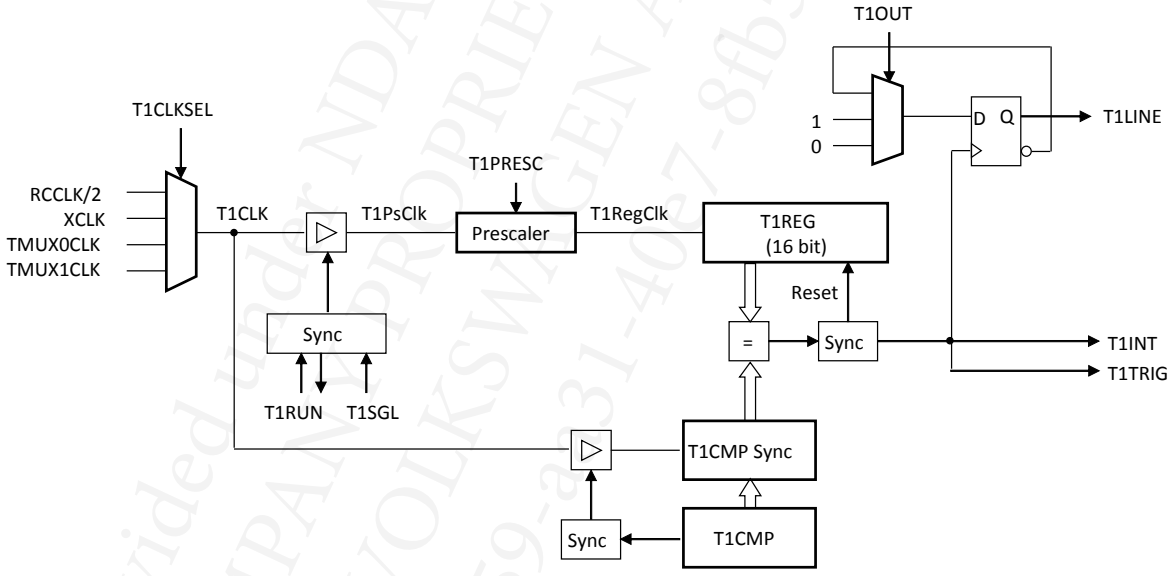


Figure 34. Block diagram of Timer 1 configured in Mode 0 and 1

8.10.1.2 Mode 1

Mode 1 has the same properties as Mode 0 with the exception that the timer automatically stops when the first compare match occurs. If bit T1RSTCMP is set, the timer register is cleared when the timer stops.

8.10.1.3 Mode 2

In Mode 2, Timer 1 is operating as 8 bit timer / counter with 12 bit prescaler, providing two 8 bit compare and two 8 bit capture registers.

Mode 2 is intended to generate flexible bit sequences and PWM signals. Both 8 bit timer registers T1REGL and T1REGH run in parallel. It is recommended to clear the timer register prior to start to ensure that both timer registers contain the same value (see Figure 35).

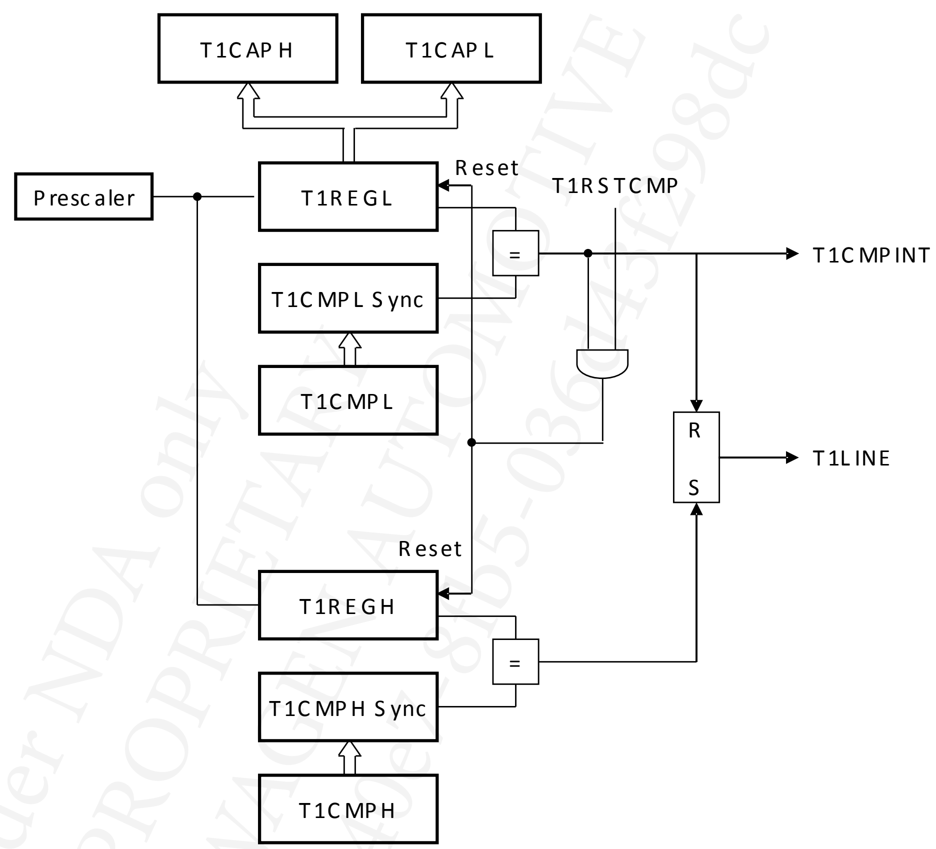


Figure 35. Block diagram of Timer 1 configured in Mode 2

With the two compare registers T1CMPL and T1CMPH it is possible to select two different values. When register T1REGH matches T1CMPH the output line T1LINE is set, whereas it is cleared upon a match between T1REGL and T1CMPL. If bit T1RSTCMP is set, it is possible to generate a PWM signal with variable pulse length and duty cycle.

A match between T1REGL and T1CMPL generates a compare interrupt request.

If both registers T1CMPL and T1CMPH match at the same time T1CMPL has priority. The reset signal upon compare is derived from T1REGL for both timer registers.

The capture interrupt is generated, if T1CAPL is loaded.

It is possible to generate a pulse position like bit sequence by use of the output signal of an additional timer as capture source. If the reset upon capture feature is used this

defines the period. With T1CMPL and T1CMPH it is possible to place a single pulse within this interval.

8.10.1.4 Mode 3

As in Mode 2, in Mode 3 Timer 1 is operating as 8 bit timer / counter with 12 bit prescaler, providing two 8 bit compare and two 8 bit capture registers.

The capture event processing with programmable guard time is useful for signal de-spiking and debouncing as well as for convenient signal demodulation.

The timer is running in 8 bit mode with T1REGL as main timer register. Both capture registers T1CAPL and T1CAPH are connected to T1REGL. A match between T1REGL and T1CMPL generates a compare interrupt request. A capture interrupt is generated, if T1CAPL is loaded. With the help of the two capture registers continuous pulse interval, pulse width and duty cycle measurements can be realized, allowing the implementation of an efficient pulse width demodulator with time-out notification (see Figure 36).

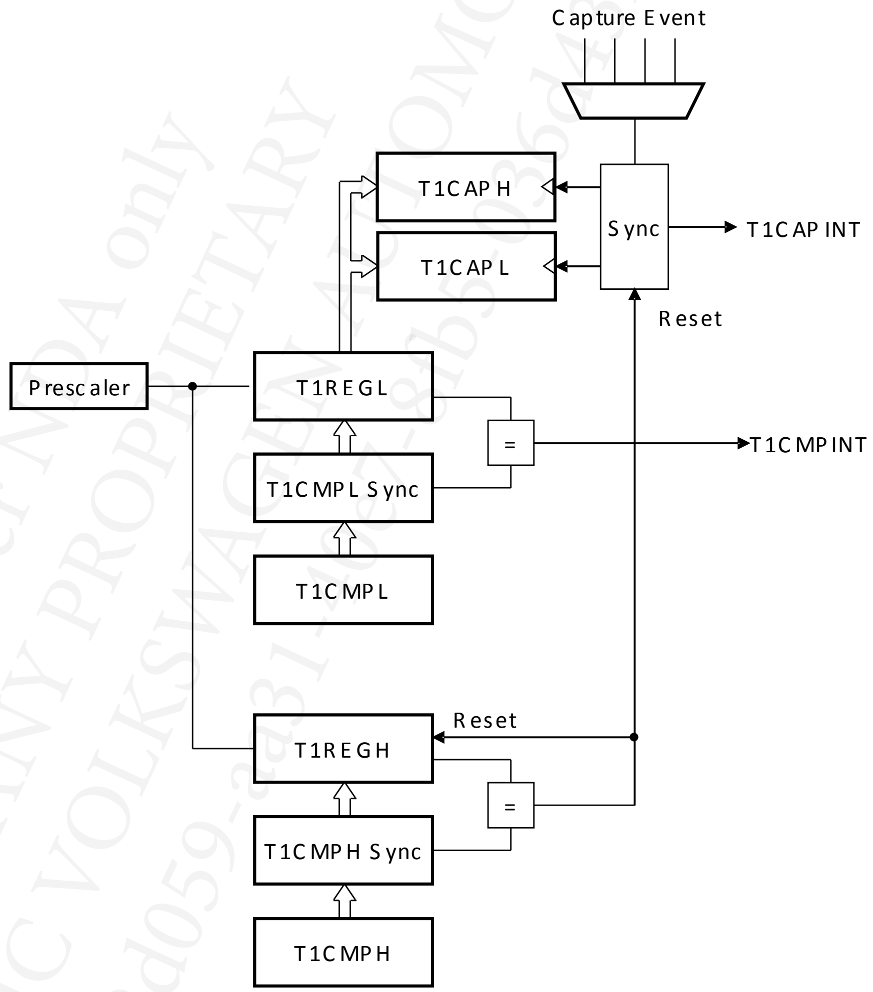


Figure 36. Block diagram of Timer 1 configured in Mode 3

It is possible to specify a guard time after every capture event or signal transition. This is useful if the timer is used to demodulate noisy signals. Only the first transition triggers the capture logic. Any other signal transition is ignored until the guard time elapses.

8.11 Watchdog timer

The device incorporates a watchdog timer to recover the system from application program deadlocks. This avoids that the connected battery is unnecessarily discharged.

The watchdog timer is active when the device is supplied from the battery (BATTERY state), while it is disabled when the device is supplied from the LF field (LF FIELD state). The watchdog timer stops automatically in debug mode.

If the watchdog timer is active and not periodically restarted, a time-out event forces the device from the BATTERY state into the LF FIELD state and generates a device reset. If the watchdog time-out event is configured as wake-up source, the device switches back to the BATTERY state, executes the boot routine and continues with the program execution. Please refer to Section 8.1.2.2 to determine the device behavior in case an LF wake-up event is pending after the watchdog time-out reset.

If the watchdog time-out event is not configured as wake-up source, the system behavior after the watchdog time-out reset depends on the field supply condition and the voltage at pin VDDC. The device may continue program execution, starting with the boot routine, as long as the field supply is sufficient.

A battery buffered flag indicates a previous watchdog time-out event and, as a potential device wake-up source, is evaluated by the boot routine.

The clock for the watchdog timer is derived from the auxiliary RC oscillator and runs at a frequency of $1/T_{REF,LF}$. The watchdog timer consists of a 16 bit incrementing main timer with 11 bit prescaler. The timeout is selectable in 16 steps from approximately 16 ms to 537 s. The selected time-out value can be locked.

In single shot mode, the clearing of the watchdog is prevented, thus the application shall finish prior to the selected fixed watchdog time-out. This mode is intended for applications which do not handle the watchdog at all.

8.12 I/O ports

8.12.1 I/O port functions

The device incorporates three I/O ports—P1, P2, and P3—with up to 8 independently configurable bidirectional port pins per port. All I/O port pins can be controlled individually.

Features:

- User configurable push-pull output or digital input in BATTERY state
- Digital input in POWER OFF state
- All port pins have port wake-up and port interrupt capabilities
- Two fail-safe port wake-up pins P10 and P11
  - Permanent pull-up resistor in input mode
  - Pull-up resistor disabled in output mode
  - Two different pull-up strengths: strong (R_{PU_STR}) and weak (R_{PU_WK})
  - Port wake-up and port interrupt on high to low transition

- Standard port pins (all pins except P10, P11)
  - User configurable pull-up or pull-down resistor in input mode; resistors can be fully disabled
  - Pull-up/pull-down resistor disabled in output mode
  - Two different pull-up strengths: strong (R_{PU_STR}) and weak (R_{PU_WK})
  - User configurable port wake-up and port interrupt on high to low or low to high transition or port wake-up and port interrupt can be disabled
- VBAT buffered pull-up/pull-down resistor settings and port wake-up configuration—port configuration is maintained in POWER OFF state
- Selected port pins are shared with digital and/or analogue alternative port function
- Very weak pull-up resistors (R_{PU_MD1}, R_{PU_MD2}, R_{PU_MD3}) at pin P21_MD for use with an external motion sensor

8.12.2 Port wake up

The port wake up logic can wake up the device from POWER OFF state or triggers a corresponding interrupt request during program execution. The wake-up feature is supported by all I/O pins. A port wake up from POWER OFF state transits the device to the BATTERY state. If the device is field supplied (LF FIELD state), the port wake-up information is stored and can be used for branch decision in the boot routine. For all wake-up ports, the wake-up mono-flop is triggered for the specified time t_{PSMF} in input mode and disabled if the port operates in output mode. Due to spurious events, the port wake-up mono-flop can be triggered if the direction of a port pin changes.

For P10 and P11, the port wake-up is sensitive at high to low transitions of the port pin. These ports feature permanent pull-up resistors in input mode. The pull-up resistor can be configured between strong and weak for every port pin separately. The wake-up mono-flop is enabled, if the port pin is in input mode. Due to this, P10 and P11 support a fail-safe wake-up from POWER OFF state regardless of the setting of any battery supplied control register. It is strongly recommended that every application uses at least one of these two ports for wake-up generation in order to avoid deadlock situations if the battery supplied registers are not correctly configured.

All other port pins except P10 and P11 feature a selectable pull-up (weak or strong) or pull-down resistor and a user selectable wake-up either on high to low or low to high transition of the port. The wake-up on low to high transition of the port can be used by the application to detect the release of a button. Either the internal pull-up resistor or an external pull-up device shall be used for correct operation. If a port pin is needed as general purpose pin and not as button input it is possible to disable the wake-up function.

8.13 LED driver

The NCF215A / NCF215B features an integrated LED driver to directly drive an external LED connected to VBAT. Port P17_LED can be configured as a current sink to drive an LED without the need for external current limitation or pull-up resistors.

The LED driver supports 12 different current settings in two different ranges - low and high. The low range supports 8 steps with an LED drive current ranging from 1 × $I_{LED\_STEP\_L}$ to 8 × $I_{LED\_STEP\_L}$ and the high range 4 steps ranging from 5 × $I_{LED\_STEP\_H}$ to 8 × $I_{LED\_STEP\_H}$.

8.14 SPI 0 and 1

The NCF215A / NCF215B provides two identical synchronous, full duplex or half duplex serial peripheral interfaces SPI 0 and SPI 1 (SPI 0/1) with a baud rate selectable between 125 kHz and 4 MHz (with 8 MHz clock). The SPI 0/1 interfaces can be used to connect the PCx7900 (FraNTIC), PQx7980/81 (LoPSTer) or NCK2984 (MantraF). In full duplex mode, each interface uses three port pins, SCKx (serial clock), SDOx (serial data output master) and SDIx (serial data input master). Configuring the SPI 0/1 interfaces in half duplex mode, each interface requires two port pins SCKx and SD(I)Ox by sharing the data line for serial data input and output.

The SPI 0/1 interfaces allow 1 to 8 bit data transfer and provide double buffered operation with separate receive and transmit registers. The clock polarity, clock phase and shift direction (left or right) is configurable. The SPI 0/1 data transfer can be controlled via interrupt processing.

The SPI 0/1 controller supports a master mode, where the master provides the serial clock SCKx. An SPI 0/1 slave mode is not provided. It is possible to connect different slaves to the single bus, but only one slave at the time can communicate with the master. Hence, different slaves shall be enabled with separate slave select signals. The slave select signals must be implemented with general purpose I/O pins and must be controlled by the application program.

The controller supports also a modified SPI 0/1 communication in a pseudo slave mode or externally clocked master mode. In this mode the clock is derived from the slave, while the NCF215A / NCF215B communication control is still in the responsibility of the master device. The pseudo slave mode supports either full duplex or half duplex mode. This mode can be used to implement a software controlled SPI 0/1 slave mode and is optimized for interfacing with PCx7900 (FraNTIC) and PQx7980/81 (LoPSTer).

8.14.1 Interaction with I/O port interface

The SPI 0/1 block interacts with 2 (half duplex mode) or 3 (full duplex mode) I/O pins, when enabled.

8.14.1.1 SDIx

In full duplex mode, the SDIx port is configured as input. If an internal pull-up/pull-down resistor is selected, it is active.

In half duplex mode, the SDIx port is not controlled by the SPI 0/1 block and can be used as standard I/O.

8.14.1.2 SDOx or SD(I)Ox

In both full duplex mode and half duplex transmit mode, the SDOx or SD(I)Ox port is configured as output. The values of the corresponding port output and direction flags are ignored. If no transfer is active the port drives the value stored in the output flip-flop, which in general corresponds to the last transmitted bit.

In half duplex receive mode, the SD(I)Ox port is configured as input. If an internal pull-up/pull-down resistor is selected, it is active. If the application switches between half duplex transmit mode and receive mode the port direction is changed automatically.

8.14.1.3 SCKx

In master mode, the SCKx port is configured as output. The values of the corresponding port output and direction flags are ignored. If no transfer is active the port drives the value selected with the clock polarity bit SPIxCLKPOL.

In pseudo slave mode, the SCKx port is configured as input. If an internal pull-up/pull-down resistor is selected, it is active.

8.15 General purpose A/D converter

The NCF215A / NCF215B has a Successive Approximation Analog to Digital Converter (ADC) which can be used to measure voltage levels (battery voltage or external voltage levels) and temperature. The ADC is optimized regarding conversion time and overall power consumption. It supports automatic averaging over a configurable number of consecutive measurements.

8.15.1 Battery voltage measurement

The NCF215A / NCF215B features battery voltage measurement to analyze and track the condition and life cycle status of the battery.

The voltage at pin VBAT is internally scaled to match with the internal reference voltage for the A-D conversion.

8.15.2 Temperature measurement

The NCF215A / NCF215B contains a built-in temperature measurement unit to get feedback of the environmental conditions of the device.

The internal reference voltage is scaled to match with the output voltage of the temperature sensor.

8.15.3 External voltage measurement

The NCF215A / NCF215B in package HVQFN40 features an external voltage measurement for voltage levels applied between P16 (positive input) and P11, P15 or P32 (negative input).

Three different voltage references are available for the external voltage measurement to exploit the dynamic range of the ADC in a best possible way. The reference voltages are VBAT, $V_{ADC,REF}$ or an external reference applied at pins P17_LED and P12.

8.16 AES calculation unit

The devices which support built-in WFS-5d based transponder emulations employ the AES co-processor unit for hardware accelerated device authentication, message encryption and rolling code generation.

The hardwired AES co-processor provides encryption with a fixed secret key length of 128 bits and forward encryption.

8.17 Random number generator

The device features a random number generator for seed generation of AES calculations.

The random number generator can be used as non-deterministic random number generator (NRNG) as well as pseudo random number generator (PRNG). All generated random numbers have a size of 16 bits.

The NRNG is also suitable to generate a seed for the PRNG for fast generation of subsequent random numbers.

8.18 Registers for mathematical/logical operations

8.18.1 Bit swap register BITSWAP

The bit swap register BITSWAP is provided to change the bit order of a byte. A byte is written to register BITSWAP first. After writing, it is swapped. If it is read again from the same location, the bit order is reversed.

8.18.2 Bit count register (parity generator) BITCNT

The bit count register BITCNT counts the number of bits being '1' in an input byte or input word.

The list below provides examples for tasks that can be accomplished with this register:

- Determine the parity of a byte/word
- Check a data byte/word versus a known bit mask
- Determine whether a byte is fully set
- Determine whether a word is fully set

8.18.3 Generic CRC register

The NCF215A / NCF215B supports a generic, fully configurable CRC register with the following features:

- Configurable CRC length from 1 to 16 bits (CRC1 to CRC16)
- Configurable CRC polynomial
- Configurable CRC start value
- Configurable input data bit width between 1 and 8 bits
- Support for LSBit/MSBit first and right/left aligned input data

The CRC register is intended for CRC generation and CRC checking tasks. The CRC calculation is executed in one instruction cycle regardless of the selected input data bit width.

8.18.4 CRC8 register

The NCF215A / NCF215B supports an 8 bit CRC generator for backward compatibility with WFS-5d transponder applications and user defined RKE frames. The generator is based on the polynomial $x^8 + x^2 + x + 1$ and it processes a complete input data byte in one instruction cycle.

8.19 Motion sensor interface

The device provides the capability to operate with an external MEMS type motion sensor (e.g. FXLS8962AF) or an external mechanical motion sensor component (rolling ball movement sensor) via the dedicated GPIO pin P21_MD. The main anticipated use of

this feature is to deactivate the LF active interface if the key has not been moved for a specific period of time. The primary benefits of this feature are:

- Reduction in standby current when the key is known to be inactive, leading to increased battery life and/or smaller batteries
- Increased resistance against relay station attacks

8.19.1 Operation with a MEMS sensor

The motion sensor interface is optimized for operation with NXP's MEMS sensor FXLS8962AF. The MEMS sensor can be connected with the one-wire interface or, if wanted, with an additional SPI interface to support extended configuration possibilities of the MEMS sensor.

The motion sensor interface supports the following functions in conjunction with the MEMS sensor:

- Autonomous operation in the VBATREG supply domain
- Detection of interrupt pulses from the MEMS sensor at pin P21_MD
- Automatic pulse length evaluation to distinguish between motion detect and boot pulses
- Configurable length of motion absent detection
- Configurable device wake-up and interrupt control for motion absence detection and boot pulse detection

After motion absence detection, the motion sensor interface can be deactivated to save power. A new motion detection pulse from the MEMS sensor is then handled via the standard port wake-up function of P21_MD.

8.19.2 Operation with a mechanical sensor

It is assumed that the external mechanical motion sensor behaves like a digital switch and the rest position may be either open or closed.

The motion sensor interface supports the following functions in conjunction with the mechanical sensor:

- Autonomous operation in the VBATREG supply domain
- Internal switchable pull-up resistor and pull-down resistor at P21_MD
- Optional operation with an external pull-up resistor
- Detection of rising and falling edges on P21_MD
- Configurable length of motion absent detection (i.e. no edge detected at P21_MD)
- Configurable device wake-up and interrupt control for motion detection (Motion event) and motion absence detection (No-motion event)

8.20 User data registers

The NCF215A / NCF215B provides 16 user registers, 8 of which are supplied by the unregulated battery supply VBAT and the other 8 by the regulated battery supply VBATREG. Each user register has a length of one byte.

These user registers keep their content during RISC power-down mode and can be accessed for customer applications.

8.21 Device modes

The NCF215A / NCF215B features the Device Modes

- VIRGIN
- INIT
- PROTECTED
- TAMPERED

The Device Modes affect the overall device behavior, the Monitor and Download Interface operation and the user ability to access the EEPROM and EROM. A Device Mode is controlled by a set of configuration bytes, which are located in the EEPROM.

The configuration bytes may not be altered by the user directly, instead the corresponding Monitor and Download Interface command has to be used.

8.21.1 VIRGIN

After manufacturing, the device operates in VIRGIN mode, enabling extended device test and device configuration. Finally, NXP forces the device into INIT mode and the VIRGIN mode is irreversibly locked in order to ensure it cannot be activated again.

8.21.2 INIT

When the device is supplied from NXP, it is configured in INIT mode by default.

The INIT mode shall be used during software development only. The Monitor and Download Interface is fully operational, enabling the customer to initialize the EEPROM and EROM as desired for the application.

To protect the EEPROM and EROM from readout and to disable the debug features, the device shall be forced into PROTECTED mode.

Leaving the device in INIT mode may cause the device to execute a software break, in case a stop command is detected at pin MSDA (for details see [2]). Such a command would terminate execution of the application program and would call the built-in debug program. In this case, execution of the application program is interrupted until a proper debug command is issued or a device reset is applied.

8.21.3 PROTECTED

In the moment the device is set into PROTECTED mode, the EEPROM and EROM are protected against altering and readout via the Monitor and Download Interface, and the debug features are disabled. The PROTECTED mode has to be used during system testing and in the final application.

The device may be forced into INIT mode again by issuing a corresponding command via the Monitor and Download Interface. This command sets the EEPROM and the EROM to a predefined state before the INIT mode is resumed. Hence, all application related EEPROM data and the EROM based application program are discarded. In case this sequence does not complete successfully, the device enters TAMPERED mode.

8.21.4 TAMPERED

The TAMPERED mode is entered temporarily during the sequence that forces the device from PROTECTED mode back into INIT mode. If this sequence does not complete successfully, the TAMPERED mode is entered.

The device may be forced into INIT mode by again issuing a corresponding command via the Monitor and Download Interface. This command sets the EEPROM and the EROM to a predefined state first, before the INIT mode is resumed. Hence, all application related EEPROM data and the EROM based application program are discarded. In case this sequence does not complete successfully, the device remains in TAMPERED mode until a new attempt is made.

8.22 System routines

8.22.1 Boot routine

The ROM based boot routine is called immediately after a device reset. A device reset can be forced either by a Port Wake-Up condition or a LF Field Reset or can be interrogated by the application program.

The boot routine executes a sequence of instructions to evaluate the device mode and configures the device, e.g. determines the supply condition, evaluates device protection flags, calls transponder emulation modes according to the EEPROM configuration and passes control to the application code accordingly.

The boot routine has to process information about the presence of LF field and battery supply. Further, the boot routine evaluates wake-up events initiated by pressed buttons or the interval timer.

8.22.2 Transponder emulation

The NCF215A / NCF215B features a set of functions to emulate the WFS-5d transponder protocol. The transponder emulation is called directly from the boot routine or it can be called from the application program with a system call (SYS instruction, [3]).

8.22.3 Monitor and download interface

The in-circuit Monitor and Download Interface is intended for non-intrusive debugging during application program development. The interface allows manipulating the embedded peripherals and provides means to initialize the EEPROM and EROM. It is implemented as two-wire serial interface using the dedicated pins MSDA and MSCL.

The Monitor and Download Interface contains a 16 Bit Real Time Monitor containing Watches. Besides several HW/SW Break Points and single step operation, the interface contains an HW accelerator and allows autonomous operation.

The majority of the features provided by the Monitor and Download Interface are available only, if the device is set into INIT mode, which is the factory default setting. When performing system tests and field trials, the device shall be set to PROTECTED mode. Latter one locks the EEPROM and EROM content, protecting it against alteration and read out, as well as disables the debug features. The device may be forced back into INIT mode by a dedicated monitor command, which will set the EEPROM and EROM to a predefined state.

A detailed description about the operation and the command set of the Monitor and Download interface is given in [2].

9 Characterization information

9.1 Limiting values

Table 8. Limiting values [1]

In accordance with the Absolute Maximum Rating System (IEC 60134)

Symbol	Parameter	Conditions		Min	Max	Unit
T_{amb}	Operating temperature			-40	85	°C
T_{sto}	Storage temperature			-55	125	°C
$V_{max,BAT}$	Voltage at any VBAT pin to VSS			-0.3	3.6	V
$V_{max,IO}$	Voltage at any general purpose I/O pin Pxx, pins MSDA, MSCL, and TEST to VSS		[2]	-0.3	V_{BAT}+0.3	V
$V_{max,IN}$	Voltage at pins IN1P, IN1N, IN2P, IN2N, IN3P, IN3N, and VDDC to VSS		[3]	-0.5	7.5	V
$V_{max,LFA}$	Voltage at pin VLFA to VSS			-0.3	1.95	V
$V_{max,XT32K}$	Voltage at pins XT32K1 and XT32K2 to VSS			-0.3	3.6	V
$V_{max,TEST1}$	Voltage at pin TEST1 to VSS			-0.05	0.05	V
$I_{peak,IN}$	Peak input current for pins IN1P, IN1N, IN2P, IN2N, IN3P and IN3N				±30	mA
$I_{peak,IO}$	Peak output current for any general purpose I/O pin Pxx, pins MSDA and MSCL				±15	mA
$I_{latch-up}$	Latch-up current		[4]	±100		mA
$V_{ESD,HBM}$	ESD, human body model		[5]	±4		kV
$V_{ESD,CDM}$	ESD, charged device model		[6]	±500		V
P_{diss}	Power dissipation				120	mW

[1] Proper device operation outside the characteristic values specified under Section 9.3 and Section 9.4 is not implied and such operation may lead to unpredictable device behavior, causing permanent alterations of the device state, memory content or characteristics.
[2] 3.6 V must not be exceeded under any circumstances.
[3] Due to device concept and design, IN1P, IN1N, IN2P, IN2N, IN3P and IN3N may show a higher peak voltage during normal device operation, caused by a corresponding input signal applied to the LF input pins.
[4] According to AEC-Q100-004
[5] According to AEC-Q100-002
[6] According to AEC-Q100-011

9.2 Recommended operating conditions

Table 9. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb}	Ambient temperature			-40	25	85	°C
V_{BAT}	Battery supply voltage	LF FIELD state (transponder operation)	[1]	0		3.6	V
		BATTERY state		2.0	3.0	3.6	V
		POWER OFF state (LF active receiver operation)		2.0	3.0	3.6	V
V_{BAT_EXT}	Extended battery supply voltage range	BATTERY state	[2]	$V_{BO,VBAT\_EXT}$		2.0	V
		POWER OFF state (LF active receiver operation)	[2]	$V_{BO,VBAT\_EXT}$		2.0	V

[1] External measures for reverse battery connection must be applied to ensure transponder operation.
[2] When the device is operated in the extended battery supply voltage range, the characteristics can deviate from the values given in Section 9.3 and Section 9.4, unless these characteristics are explicitly specified for the extended supply voltage range.

9.3 Static characteristics

Table 10. Static characteristics

T_{amb} = -40 to +85 °C, V_{SS} = 0 V, V_{BAT} = 3.0 V, f_{C_LF} = 125 kHz, T_0 = 1/f_{C_LF}, C_{VDDC} = 22 nF connected between pins VDDC and VSS.

Unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
LF FIELD state (transponder operation)							
V_{BAT}	Battery supply voltage		[1]	0		3.6	V
I_{IN_LF}	Coil input peak current	$\|I_{IN}\|$				15	mA
MI_{WR_LF}	Minimum modulation index, write direction	$V_{IN\text{-}HIGH}$ = 5 V_p, T_{TMOD} = 8 T_0	[2]		100	95	%
V_{DDC_LF}	Rectified supply voltage	$\|I_{IN}\|$ = 150 µA				5.7	V
$V_{THR,FDLF\text{-}VIN}$	LF field detect threshold voltage, (V_{IN}, peak), rising threshold, flagged in VDD domain	$\|V_{INx+,peak}\|$, $\|V_{INx-,peak}\|$		2.1	2.5	2.9	V
$V_{THR,FDLF\text{-}VIN\_HYST}$	LF field detect threshold voltage, (V_{IN}, peak), hysteresis, flagged in VDD domain	$\|V_{INx+,peak}\|$, $\|V_{INx-,peak}\|$	[3]		500		mV
$V_{THR,FD\_ATIC\text{-}VIN}$	LF field detect threshold voltage, (V_{IN}, peak), rising threshold, flagged in VFLDLF domain	$\|V_{INx+,peak}\|$, $\|V_{INx-,peak}\|$		2.20	2.75	3.05	V
$V_{THR,FD\_ATIC\text{-}VIN\_HYST}$	LF field detect threshold voltage, (V_{IN}, peak), hysteresis, flagged in VFLDLF domain	$\|V_{INx+,peak}\|$, $\|V_{INx-,peak}\|$	[4]		150		mV
Device executes from ROM (transponder emulation), V_{DDC_LF} = 3.0 V							
$I_{CC\_LF\_R}$	Supply current (wait for command)		[5]		20	40	µA
Device executes from EROM (transponder application, EROM module 1 off), V_{DDC_LF} = 3.0 V							
$I_{CC\_LF\_2M}$	RUN mode, main RC oscillator as CPU clock source, f_{CPU} = 2 MHz		[5]		360	410	µA
$I_{CC\_LF\_500k}$	RUN mode, auxiliary RC oscillator as CPU clock source, f_{CPU} = 500 kHz		[5]		90	110	µA
$I_{CC\_LF\_IDLE}$	IDLE mode, auxiliary RC oscillator as clock source, f_{CPU} = 500 kHz		[5]		35	55	µA
POWER OFF state (battery supply for LF active receiver)							
V_{BAT}	Battery supply voltage			2	3	3.6	V
I_{QQ_OFF}	Quiescent current (VBATREG regulator off)				0.35	2.2	µA

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{QQ_PD}	Quiescent current with LF active receiver in power-down (VBATREG regulator on, 32 kHz crystal oscillator off, DCDC converter off)				0.45	2.7	µA
I_{QQ_XO32K}	Quiescent current with 32 kHz crystal oscillator on (VBATREG regulator on, interval timer off, DCDC converter off)	T_{amb} = -40 °C				3.1	µA
		T_{amb} = 25 °C			1.0	3.1	µA
		T_{amb} = 85 °C				3.9	µA
I_{QQ_IT}	Quiescent current with activated interval timer (VBATREG regulator on, 32 kHz crystal oscillator on, interval timer on, real-time clock off, DCDC converter off)	T_{amb} = -40 °C				3.2	µA
		T_{amb} = 25 °C			1.1	3.2	µA
		T_{amb} = 85 °C				4.0	µA
I_{QQ_DCDC}	Quiescent current with activated DCDC converter (VBATREG regulator on, 32 kHz crystal oscillator on, LFA PLL on, interval timer and real-time clock off)	T_{amb} = -40 °C			2.4	4.8	µA
		T_{amb} = 25 °C			2.7	4.7	µA
		T_{amb} = 85 °C			3.9	5.8	µA
$I_{QQ\_LFACT\_G1M}$	Quiescent current LF active receiver application configuration, gain mode G1, MMF (interval timer and real-time clock off)	T_{amb} = -40 °C			5.1	8.9	µA
		T_{amb} = 25 °C			5.9	7.9	µA
		T_{amb} = 85 °C			7.8	10.5	µA
$I_{QQ\_LFACT\_G3M}$	Quiescent current LF active receiver application configuration, gain mode G3, MMF (interval timer and real-time clock off)	T_{amb} = -40 °C			5.7	9.6	µA
		T_{amb} = 25 °C			6.6	8.6	µA
		T_{amb} = 85 °C			8.6	11.2	µA
$I_{QQ\_LFACT\_D1M}$	Quiescent current LF active receiver application configuration, desensitization mode D1, MMF (interval timer and real-time clock off)	T_{amb} = -40 °C			4.5		µA
		T_{amb} = 25 °C			5.3		µA
		T_{amb} = 85 °C			7.1		µA
$I_{QQ\_LFACT\_D2M}$	Quiescent current LF active receiver application configuration, desensitization mode D2, MMF (interval timer and real-time clock off)	T_{amb} = -40 °C			4.4		µA
		T_{amb} = 25 °C			5.2		µA
		T_{amb} = 85 °C			7.0		µA
ΔI_{QQ_MSI}	Delta quiescent current when Motion Sensor Interface is enabled		[6]				
		T_{amb} = -40 °C				0.6	µA
		T_{amb} = 25 °C			0.05	0.3	µA
		T_{amb} = 85 °C				0.6	µA
BATTERY state (battery supply)							
V_{BAT}	Battery supply voltage			2	3	3.6	V
Device executes from ROM							

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{BAT_R2M}	RUN mode, main RC oscillator as CPU clock source, f_{CPU} = 2 MHz, EROM turned off				200	255	µA
I_{BAT_R500k}	RUN mode, auxiliary RC oscillator as CPU clock source, f_{CPU} = 500 kHz, EROM turned off				40	60	µA
I_{BAT_RIDLE}	IDLE mode, auxiliary RC oscillator as CPU clock source, f_{CPU} = 500 kHz, EROM turned off				20	35	µA
Device executes from EROM (EROM module 1 off)							
I_{BAT_4M}	RUN mode, main RC oscillator as CPU clock source, f_{CPU} = 4 MHz				550	665	µA
I_{BAT_2M}	RUN mode, main RC oscillator as CPU clock source, f_{CPU} = 2 MHz				340	435	µA
I_{BAT_500k}	RUN mode, auxiliary RC oscillator as CPU clock source, f_{CPU} = 500 kHz				80	130	µA
I_{BAT_IDLE}	IDLE mode, auxiliary RC oscillator as CPU clock source, f_{CPU} = 500 kHz				35	48	µA
ΔI_{DD_RSSI}	RSSI supply current (RSSI analog frontend on, SDADCCLK and SD-ADC on, VDDA regulator and bandgap reference on, digital RSSI processing running), 1 LF channel selected		[7]		3.5	4.2	mA
$\Delta I_{DD\_RSSI\_3CH}$	RSSI supply current (RSSI analog frontend on, SDADCCLK and SD-ADC on, VDDA regulator and bandgap reference on, digital RSSI processing running), 3 LF channels selected		[7]		4.8	6	mA
$\Delta I_{DD\_ADC\_4M}$	Supply current ADC measurement (including VDDA regulator and bandgap reference), main RC oscillator as CPU clock source, f_{CPU} = 4 MHz		[7]		230	310	µA
ΔI_{DD_TEMP}	Supply current temperature sensor		[7]		27	40	µA
$\Delta I_{DD\_VBATSENS}$	Supply current VBAT sensor for battery voltage measurement		[7]		46	65	µA
LF FIELD state or BATTERY state							
ΔI_{DD_ULPRD}	Supply current ULP-EEPROM (Read)	Single module	[7]			2.75	µA

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\Delta I_{DD\_ULPPROG}$	Supply current ULP-EEPROM (Erase/Write)	Single module	[7]		20	35	µA
ΔI_{DD_EROM2}	Static bias current for EROM module 2		[7]		15	20	µA
ΔI_{DD_MRC}	Supply current main RC oscillator		[8]		20	60	µA
ΔI_{DD_AES}	Supply current AES calculation unit	AESCLK = RCCLK	[7]		22	26	µA/MHz
Power-on reset (POR) and brownout detectors							
V_{POR}	Power-on reset falling threshold			1.25	1.30	1.35	V
$V_{BO,VDD}$	VDD brownout falling threshold			1.43	1.50	1.57	V
$V_{BO,VDDA}$	VDDA brownout falling threshold			1.50	1.60	1.72	V
V_{BATPOR}	VBAT power-on reset falling threshold			1.35	1.55	1.80	V
$V_{BO,VBAT\_STD}$	VBAT standard brownout falling threshold			2.20	2.30	2.40	V
$V_{BO,VBAT\_EXT}$	VBAT extended brownout falling threshold			1.90	1.95	2.00	V
$V_{VBATIND}$	Low battery indicator detection falling threshold			2.2	2.4	2.6	V
$V_{VBATIND\_HYST}$	Low battery indicator detection hysteresis			30	50	80	mV
$R_{VBATIND}$	Low battery indicator resistive load on VBAT			100	150	300	kΩ
$V_{BO,VLFA}$	VLFA brownout falling threshold			1.1	1.2	1.3	V
Immobilizer / LF passive interface							
C_{IN_PAS}	Effective differential input capacitance between INxP, INxN	125 kHz, V_{IN} = 2 V_{rms}, LF tuning capacitors off			29		pF
R_{x+_LIN}	Input resistance at INxP, linear (standard LF modulator)	V_{INx+} = 0.5 V, V_{INx-} = 0 V, V_{FLD} = 3 V	[9]	1.4	2.0	2.6	kΩ
$R_{x+\_LIN,strong}$	Input resistance at INxP, linear (strong LF modulator)	V_{INx+} = 0.5 V, V_{INx-} = 0 V, V_{FLD} = 3 V	[9]	300	550	700	Ω
R_{x+_NLIN}	Input resistance at INxP, non-linear (standard LF modulator)	V_{INx+} = 1.5 V, V_{INx-} = 0 V, V_{FLD} = 3 V	[9]	0.65	1.00	1.35	kΩ
R_{x-_LIN}	Input resistance at INxN, linear (standard LF modulator)	V_{INx+} = 0 V, V_{INx-} = 0.5 V, V_{FLD} = 3 V	[9]	3.0	4.1	5.4	kΩ
$R_{x-\_LIN,strong}$	Input resistance at INxN, linear (strong LF modulator)	V_{INx+} = 0 V, V_{INx-} = 0.5 V, V_{FLD} = 3 V	[9]	300	550	700	Ω
V_{CLP-IN}	Input limiter clamp voltage	I_{IN} = ±15 mA		5.8	6.7	7.8	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		I_{IN} = ±150 µA		5.5	6.4	7.6	V
Tuning capacitor for LF interface							
C_{STEP}					2		pF
LF active interface							
C_{IN_ACT}	Effective differential input capacitance between INxP, INxN	125 kHz, V_{IN} ≤ 200 mV_{pp}, LF tuning capacitors off			15		pF
R_{IN_ACT}	Effective differential input resistance between INxP, INxN	125 kHz, V_{IN} ≤ 200 mV_{pp}			1.5		MΩ
V_{CLP_ACT-IN}	Input limiter clamp voltage	I_{IN} = ±15 mA		5.8	6.7	7.8	V
		I_{IN} = ±150 µA		5.5	6.5	7.8	V
V_{SENS_G3M}	Sensitivity active protocol, gain G3, MMF, signal applied at all three channels		[10] [11]		70	140	$µV_{pp}$
$V_{SENS\_G3M\_SINGLE}$	Sensitivity active protocol, gain G3, MMF, signal applied at one channel		[10] [11]		120	240	$µV_{pp}$
V_{SENS_G1M}	Sensitivity active protocol, gain G1, MMF, signal applied at all three channels		[10] [11]		100	200	$µV_{pp}$
$V_{SENS\_G1M\_SINGLE}$	Sensitivity active protocol, gain G1, MMF, signal applied at one channel		[10] [11]		175	350	$µV_{pp}$
$V_{SENS\_D1M\_SINGLE}$	Sensitivity active protocol, desensitization mode D1, MMF, signal applied at one channel		[10] [11]		500	1000	$µV_{pp}$
$V_{SENS\_D2M\_SINGLE}$	Sensitivity active protocol, desensitization mode D2, MMF, signal applied at one channel		[10] [11]		1250	2500	$µV_{pp}$
B_{CF}	Channel filter bandwidth				12		kHz
$a_{CF,85k}$	Channel filter attenuation at 85 kHz relative to 125 kHz		[12]				
		T_{amb} = -40 °C		35	60		dB
		T_{amb} = 25 °C, 85 °C		45	62		dB
RSSI							
ACC_{RSSI}	RSSI accuracy, wanted signal ≥ 1 mV_{pp}	RSSI filter setting C, 32 times averaging, 3 σ stochastic error, V_{BAT} = 2.0 to 3.6 V	[13] [14] [15]				
		T_{amb} = 25 °C			± 2	± 4.5	%
		T_{amb} = -40 to +85 °C				± 9	%

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ACC_{RSSI_INT1}	RSSI accuracy with CW interferer at 85 kHz, wanted signal = 1 mV_{pp}, interferer/wanted = 40 dB	RSSI filter setting C, 32 times averaging, 3 σ stochastic error, V_{BAT} = 2.0 to 3.6 V	[13] [14]				
		T_{amb} = 25 °C			± 3	± 7.5	%
		T_{amb} = -40 to +85 °C				± 12	%
ACC_{RSSI_INT2}	RSSI accuracy with CW interferer at 85 kHz, wanted signal = 100 μV_{pp}, interferer/wanted = 40 dB	RSSI filter setting C, 32 times averaging, 3 σ stochastic error, V_{BAT} = 2.0 to 3.6 V	[13] [14]				
		T_{amb} = 25 °C			± 8	± 13	%
		T_{amb} = -40 to +85 °C				± 20	%
$V_{RSSI,max}$	Maximum RSSI input voltage			13			V_{pp}
G_{RSSI_36dB}	Nominal RSSI gain 36 dB range		[16]		64		
G_{RSSI_18dB}	Nominal RSSI gain 18 dB range		[16]		8		
G_{RSSI_0dB}	Nominal RSSI gain 0 dB range		[16] [15]		1		
G_{RSSI_-18dB}	Nominal RSSI gain -18 dB range		[16] [15]		0.125		
K_{SDADC}	Nominal SD-ADC conversion gain		[16]		37		μV/LSB
R_{short}	Nominal RSSI shorting resistance INxP, INxN to ground	V_{BAT} = 3.0 V, T_{amb} = 25 °C, V_{IN} = 100 mV_{DC}	[16]		100		Ω
ΔR_{short}	Temperature and supply voltage variation of RSSI shorting resistance INxP, INxN to ground	Referred to V_{BAT} = 3.0 V and T_{amb} = 25 °C; V_{IN} = 100 mV_{DC}					
		T_{amb} = 25 °C, V_{BAT} = 2.3 to 3.6 V		-2.5		3.5	%
		T_{amb} = 25 °C, V_{BAT} = 2.0 to 3.6 V		-2.5		5	%
		T_{amb} = -40 to +85 °C, V_{BAT} = 2.3 to 3.6 V		-4		6	%
		T_{amb} = -40 to +85 °C, V_{BAT} = 2.0 to 3.6 V		-4		8	%
R_{IN_RSSI}	RSSI input resistance INxP, INxN	125 kHz; V_{IN} ≤ 200 mV_{pp}; 36 dB, 18 dB, 0 dB range; all Rx_Q off			1.5		MΩ
$R1_Q$	Resistor 1 for Q factor adjustment		[17]	112.5	150	187.5	kΩ
$R2_Q$	Resistor 2 for Q factor adjustment		[17]	90	120	150	kΩ
$R3_Q$	Resistor 3 for Q factor adjustment		[17]	75	100	125	kΩ
$R4_Q$	Resistor 4 for Q factor adjustment		[17]	60	80	100	kΩ

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R5_Q$	Resistor 5 for Q factor adjustment		[17]	37.5	50	62.5	kΩ
$R6_Q$	Resistor 6 for Q factor adjustment		[17]	15	20	25	kΩ
Rx_QdT	Temperature variation of resistors for Q factor adjustment	T_{amb} = -40 to +85 °C, referred to T_{amb} = 25 °C		-5		5	%
$B_{RSSI\_FILT\_A}$	Bandwidth of digital RSSI filter A				31.0		kHz
$B_{RSSI\_FILT\_B}$	Bandwidth of digital RSSI filter B				17.6		kHz
$B_{RSSI\_FILT\_C}$	Bandwidth of digital RSSI filter C				9.4		kHz
$B_{RSSI\_FILT\_D}$	Bandwidth of digital RSSI filter D				9.4		kHz
32 kHz crystal oscillator							
C_{L_XO32K}	Load capacitance of external 32 kHz crystal				12.5		pF
DCDC converter							
C_{VLFA}	Effective capacitance of buffer capacitor for VLFA		[18] [19]	0.5	1	2	µF
ADC							
RES_{ADC}	Resolution ADC					10	Bit
DNL_{ADC}	Differential nonlinearity ADC				± 0.5		LSB
INL_{ADC}	Integral nonlinearity ADC		[20] [21] [22]		± 0.6		LSB
$V_{ADC,REF}$	Reference voltage – full scale value			1.215	1.25	1.285	V
VIN_{ADC}	Input voltage of ADC positive input and ADC negative input to VSS		[23]	0.2		1.1	V
Battery measurement							
G_{VBAT}	Battery measurement gain	V_{BAT} = 3.0 V, T_{amb} = 25 °C, reference $V_{ADC,REF}$			3.66		mV/LSB
OFF_{VBAT}	Battery measurement offset at 3 V	V_{BAT} = 3.0 V, T_{amb} = 25 °C, reference $V_{ADC,REF}$		800	818	836	LSB
Temperature measurement							
T_{ACC_CAL}	Temperature measurement accuracy calibrated	Offset compensated T_{amb} = -40 to +85 °C		-5		5	K
G_{TADC}	Temperature measurement gain				6.19		LSB/K
OFF_{TADC}	Temperature measurement offset at 25 °C			440	512	592	LSB
P1x, P2x, P3x (general purpose I/Os), MSDA[24], MSCL[25]							
C_I	Pin capacitance	V_{IN} = 0.1 V_{RMS}, f = 1 MHz			9		pF
V_{IL}	Input low voltage					0.3 V_{BAT}	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	Input high voltage			0.7 V_{BAT}			V
I_{IL}	Input low current	V_{IL} = 0 V	[26]			0.5	µA
I_{IH}	Input high current	V_{IH} = V_{BAT}	[27]			0.5	µA
V_{OL}	Output low voltage	I_O = 1 mA				0.4	V
V_{OH}	Output high voltage	I_O = -1 mA		V_{BAT} -0.4			V
I_{OL}	Maximum allowed current when driving output low to an external LED (any GPIO incl. P17_LED when LED Driver is disabled)	30 sec/day for single GPIO operation	[28]			5	mA
R_{PU_STR}	Pull-up resistance strong	V_I = 0 V, V_{BAT} = 2.0 to 3.6 V		18	28	40	kΩ
R_{PU_WK}	Pull-up resistance weak	V_I = 0 V, V_{BAT} = 2.0 to 3.6 V		65	115	160	kΩ
I_{PD}	Pull-down current	V_I = V_{BAT}, V_{BAT} = 2.0 to 3.6 V		10	50	150	µA
Motion sensor interface (P21_MD)							
R_{PU_MD1}	Pull-up resistor for motion sensor interface	V_I = 0 V, V_{BAT} = 2.0 to 3.6 V		1.4	2.0	2.5	MΩ
R_{PU_MD2}	Pull-up resistor for motion sensor interface	V_I = 0 V, V_{BAT} = 2.0 to 3.6 V		2.8	4.0	5.0	MΩ
R_{PU_MD3}	Pull-up resistor for motion sensor interface	V_I = 0 V, V_{BAT} = 2.0 to 3.6 V		350	500	625	kΩ
LED driver (P17_LED)							
$I_{LED\_STEP\_L}$	LED driver current step size in low range				0.75		mA
$I_{LED\_STEP\_H}$	LED driver current step size in high range				1.5		mA
I_{LED}	LED driving current, 2 × $I_{LED\_STEP\_L}$	V_o = 100 mV to V_{BAT}, V_{BAT} = 2.0 to 3.6 V		1.1	1.5	1.8	mA
I_{LED}	LED driving current, 6 × $I_{LED\_STEP\_L}$	V_o = 100 mV to V_{BAT}, V_{BAT} = 2.0 to 3.6 V		3.6	4.5	5.4	mA
I_{LED}	LED driving current, 6 × $I_{LED\_STEP\_H}$	V_o = 200 mV to V_{BAT}, V_{BAT} = 2.0 to 3.6 V		7	9	10.8	mA

[1] External measures for reverse battery connection must be applied to ensure transponder operation in such case.
[2] The demodulator sensitivity applicable in write direction is defined according Figure 14
[3] Measured based on LFFLD flag (see Figure 15) read by the CPU (in boot code) to determine that LF Passive mode has started and transponder emulation is possible. This flag can only assert after the 2 ms count.
[4] Measured based on field detect flag, which is the first indicator that a field is present. This flag starts the 2 ms count. Internal signal, not available as SFR bit. See Figure 15, Field Detect block on the left.
[5] Specifies the internal chip operating current that needs to be supplied from the rectified supply voltage. Input/output current of general purpose ports are zero.
[6] Specifies the additional internal chip quiescent current caused by the corresponding circuitry, if enabled, which has to be added to the device quiescent current (I_{QQ}) in order to determine the total device quiescent current.

[7] Specifies the additional internal chip operating current caused by the corresponding circuitry, if enabled, which has to be added to the device operating current (I_{CC} or I_{BAT}, respectively) in order to determine the total device operating current.
[8] Specifies the additional internal chip operating current caused by the main RC oscillator, if enabled, which has to be added only to device operating currents (I_{CC} or I_{BAT}, respectively) which do not use the main RC oscillator as CPU clock source in order to determine the total device operating current.
[9] Measured while the internal modulator is active, thus the additional load is ON (S2 closed), according to Figure 10.
[10] Protocol with legacy code violation and 32 bit wake-up pattern, error tolerance off.
[11] The sensitivity can depend on the application. Especially the antenna Q factor influences the sensitivity in general. The values are anticipated for Q = 5 with a wake-up probability of 50 %. For further information, please refer to the Application note.
[12] The attenuation is calculated as the ratio between the channel filter gain at 125 kHz – f_{LOLFA} and 85 kHz – f_{LOLFA}.
[13] RSSI calibration values applied.
[14] Only one LF input channel selected per measurement
[15] Measured with low ohmic input signal, damping of coil in application to be considered. For details, refer to Application Note.
[16] Nominal value as reference point for the calibration; no min/max values applicable.
[17] Resistor values in case of weakly-coupled signals when the LF front-end rectifier has no effect and the voltages on INxP and INxN are differential with a common-mode voltage around ground.
[18] The effective capacitance of the external capacitor must stay within the specified limits over the full device operating range and over lifetime: T_{amb} = -40 to +85 °C, DC bias condition: V_{LFA} = 1.65 to 1.95 V_{DC}
[19] The buffer capacitor must be a ceramic type.
[20] A typically missing code at ADC output 511 is not considered.
[21] The INL [LSB] is measured at a resolution of 10 bit.
[22] The ADC specification is valid for the specified common-mode input range. The ADC will still be operational outside the specified range but with limited linearity and accuracy.
[23] The ADC specification is valid for the specified differential input range. The ADC will still be operational outside the specified range (including VSS) but with limited linearity and accuracy.
[24] MSDA features an internal pull-up resistor to VBAT
[25] MSCL is configured statically as output
[26] Not applicable if internal pull-up resistor is active.
[27] Not applicable if internal pull-down resistor is active.
[28] The parameter is only valid for driving the maximum current for one GPIO for maximum 30 seconds per day over a lifetime of 15 years. Simultaneous LED drive operations (up to three GPIOs) is supported, but the maximal driver on-time of 30 seconds/day has to be divided by the number of simultaneously driven GPIOs. In case of continuous LED drive operation going beyond these conditions performance degradation can not be excluded. Note that the output low voltage level V_{OL} may exceed 0.4 V as specified for 1 mA output current when used as digital output.

9.4 Dynamic characteristics

Table 11. Dynamic characteristics

T_{amb} = -40 to +85 °C, V_{SS} = 0 V, V_{BAT} = 2.0 to 3.6 V, f_{C_LF} = 125 kHz, $T_0 = 1/f_{C\_LF}$, C_{VDDC} = 22 nF connected between pins VDDC and VSS.

Unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Power management							
t_{POR_HLD}	Power-on reset hold time	via MSCL pin after button press			300	800	µs
$t_{VDDA,PON}$	VDDA regulator power-on to operation delay				10	30	µs
$t_{VBATREG,PON}$	VBATREG regulator power-on to operation delay				0.15	0.5	ms
t_{DCDCBG_set}	DC-DC converter bandgap reference settling time					400	µs
$t_{DCDC,PON}$	DC-DC converter power-on to operation delay with internal clock					200	ms
t_{DCDC_set}	DC-DC converter settling time when switching from internal clock to LFAPLL clock					1	ms
$t_{VLFADIG,PON}$	VLFADIG regulator power-on to operation delay					6	ms
$t_{VBATMON\_SETT}$	Battery brownout detector settling time					15	µs
t_{BAT_FIRST}	Initial delay after battery insertion					1	ms
t_{VDD_STUP}	Device wake-up to POR active delay				50		µs
t_{PSMF}	Port sense mono-flop duration				25	100	µs
$t_{BO,VDDA\_RST}$	VDDA brownout detector reset time					30	µs
On-chip RC oscillators							
$f_{OSC,RC}$	Main RC oscillator clock frequency			14.4	16.0	17.6	MHz
$f_{OSC,AUX}$	Auxiliary RC oscillator clock frequency			0.9	1	1.1	MHz
$t_{AUXCLK,PON}$	Auxiliary oscillator start up time					35	µs
LF transponder operation							
f_{C_LF}	LF field carrier frequency				125.0		kHz
Transponder demodulator							
t_{ADLY}	Analogue demodulator setup delay					40	µs
t_{AHDLY}	Analog output HIGH setup delay	V_{INpk} = 2.7 V / 7.0 V		4	20	40	µs
t_{ALDLY}	Analog output LOW setup delay	V_{INpk} = 2.7 V / 7.0 V			4	16	µs
LF field power-on							
$t_{FLD,HLD}$	LF field hold time		[1]		2.048		ms

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{VDDC}	C_{VDDC} charging time		[2]		2		ms
LF field power-on reset							
$t_{FLD,0\text{-}DLY}$	LF field low detection delay time	V_{INpk} = 6 V		1	2	5	ms
$t_{RESET,SETUP}$	LF field power-on reset setup time		[3]	10			ms
LF active receiver							
$f_{CARR,nom}$	Nominal input carrier frequency, active protocol				125		kHz
Δf_{CARR}	Tolerance of input carrier frequency, active protocol			-3000		3000	ppm
T_{nom}	Nominal Manchester bit period, active protocol				256		µs
ΔT	Tolerance of Manchester bit period, active protocol	@ V_{SENS}		-100		100	ppm
		@ V_{SENS} + 1 dB	[4]	-3000		3000	ppm
n_{RUNIN}	Number of run-in bits			13			counts
t_{LFAPLL_set}	LF active PLL settling time					11.5	ms
t_{ACT_set}	LF active receiver settling time				9	20	ms
t_{AGC_REC}	AGC recovery time					10	ms
$t_{AGC\_SENSRST}$	AGC sensitivity reset time			3			ms
Active limiter							
t_{LIM_RISE}	Limiter rise time		[5]		70	180	µs
t_{LIM_FALL}	Limiter fall time		[5]		2	3.5	ms
32 kHz crystal oscillator							
$f_{XO32K,nom}$	Nominal frequency of external 32 kHz crystal				32768		Hz
Δf_{XO32K}	Tolerance of 32 kHz crystal oscillator frequency for LF active operation			-250		250	ppm
t_{XO32K_set}	32 kHz crystal oscillator settling time	Reference crystal NDK NX3215SA				750	ms
$t_{XO32KFAIL\_set}$	32 kHz crystal oscillator clock fail detection settling time					250	µs
RSSI							
$t_{RSSI,PON}$	RSSI power-on to operation delay					200	µs
t_{IND}	Range overflow detector (indicator) settling time	125 kHz CW signal	[6]			200	µs
t_{INDRST}	Range overflow detector (indicator) reset time					2	µs
$t_{RANGESEL}$	Range selection settling time					40	µs
$t_{CHANSEL}$	Channel selection settling time					50	µs
$t_{VSDADC,PON}$	SD-ADC supply regulator power-on delay					150	µs

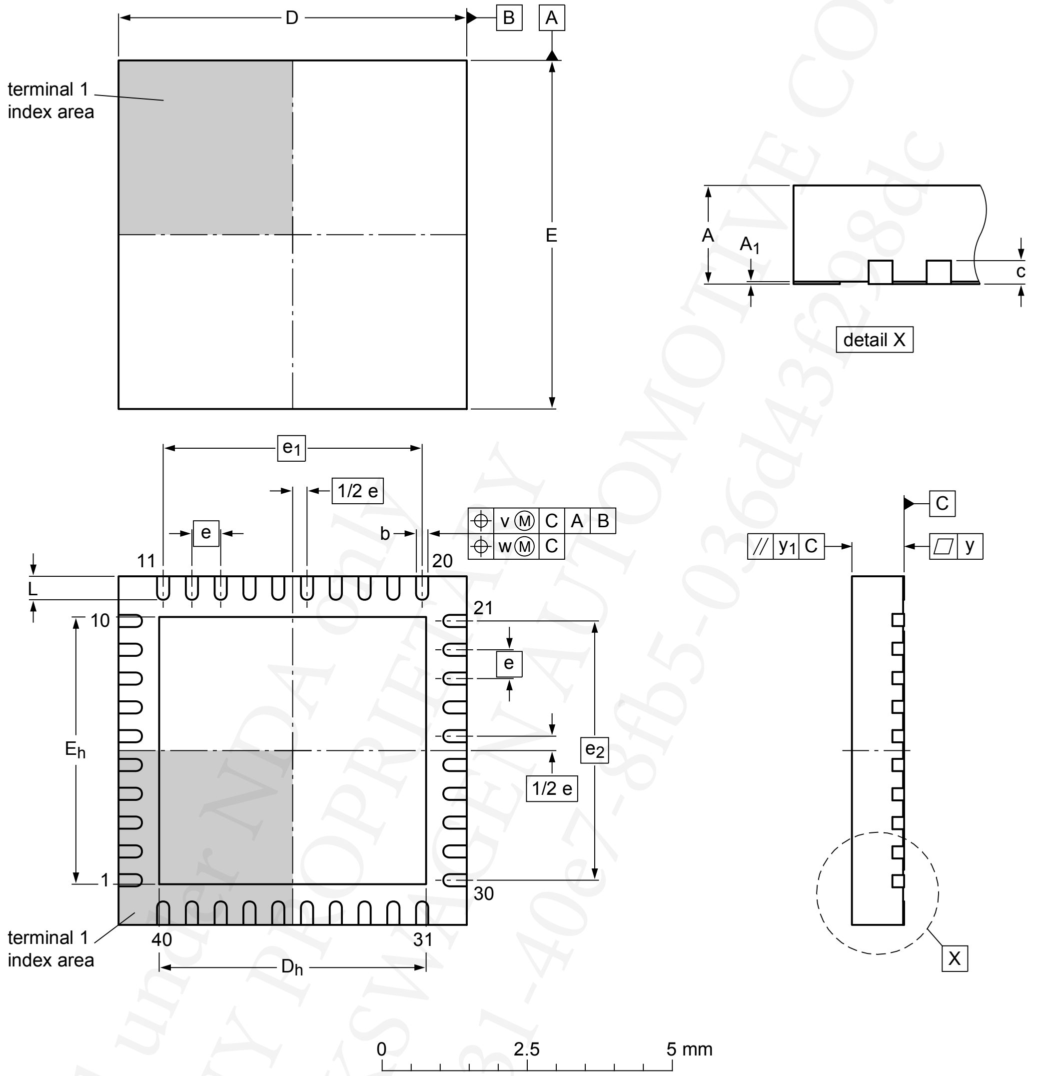
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{SDADC,STUP}$	SD-ADC start-up time					150	μs
$t_{SDADCCLK,CAL}$	SD-ADC clock calibration time					220	μs
$f_{OSC,SDADC}$	SD-ADC oscillator clock frequency	After calibration		15.84	16.00	16.16	MHz
$t_{RSSI\_FILT\_A}$	RSSI digital filter settling time for filter setting A					4992	1/ $f_{OSC,SDADC}$
$t_{RSSI\_FILT\_B}$	RSSI digital filter settling time for filter setting B					6528	1/ $f_{OSC,SDADC}$
$t_{RSSI\_FILT\_C}$	RSSI digital filter settling time for filter setting C					11904	1/ $f_{OSC,SDADC}$
$t_{RSSI\_FILT\_D}$	RSSI digital filter settling time for filter setting D					13440	1/ $f_{OSC,SDADC}$
$t_{RSSI\_DIGPROC}$	RSSI digital processing time		[7]		256		1/ $f_{OSC,SDADC}$
ULP-serial EEPROM							
t_{ULPRET}	Data retention time	T_{amb} = 50 °C		20			years
$N_{ULPWR-CYL}$	Write endurance ULP EEPROM	T_{amb} = 25 °C	[8]	100 k			cycles
$t_{ULP,PON}$	ULP EEPROM power-on to operation delay					100	μs
t_{ULPRD}	Read time ULP EEPROM	1 bit				2	μs
		1 byte				20	μs
t_{ULPWR}	Erase/write time ULP EEPROM	1 page	[7]		536		$T_{REF,LF}$
EROM							
t_{ERET}	Data retention time	T_{amb} = 50 °C		20			years
$N_{EWR-CYL}$	Write endurance EROM	T_{amb} = 25 °C	[8]	10 k			cycles
ADC							
$t_{BG,PON}$	Band gap power-on time	VDDA settled				170	μs
t_{CONV}	ADC conversion time	Single conversion	[7]		21		$1/f_{ADC,CLK}$
P15 (XCLK)							
f_{XCLK}	External clock frequency					5	MHz
t_{XCH}	External clock high time			100			ns
t_{XCL}	External clock low time			100			ns
t_{XCR}	External clock rise time					0.5	μs
t_{XCF}	External clock fall time					0.5	μs
Temperature sensor							
$t_{TEMP,PON}$	Power-on to operation delay (settling time)					20	μs
AES calculation unit							
$t_{AES,CALC}$	Time needed for one 128 bit AES enciphering		[7]		909		$T_{REF,AES}$
Random Number Generator							

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{RNG,CALC}$	Time to compute one 16 bit random number		[7]		136		$1/f_{OSC,AUX}$
$N_{RNG,ENT15}$	Number of computations to compute a 16 bit random number with entropy factor > 15				9		counts
$t_{RNG,Sett}$	Random number generator settling time	Oscillator settling time		69	85	135	µs
Boot routine							
t_{BOOT_WUP}	Device boot time, battery wake-up event					1.95	ms
$t_{BOOT\_WFS5C\_ROM}$	Device boot time, WFS-5d transponder executed in ROM	WFS-5d transponder emulation				20	ms
$t_{BOOT\_TRP\_EROM}$	Device boot time, transponder executed in EROM		[9]			12	ms

[1] $t_{FLD,HLD}$ is derived by division of the LF field clock ($256/f_{C\_LF}$).
[2] t_{VDDC} is application dependent and mainly determined by the coupling factor and C_{VDDC}.
[3] Value holds for a theoretical capacitor value of C_{VDDC} = 330 nF and is approximated by tFLD,0-DLY + 0.015ms * C_{VDDC}/1 nF.
[4] Protocol with legacy code violation and 32 bit wake-up pattern, error tolerance off, segmented correlator mode on (for details see [1]).
[5] Rectifier output current measured at 90 % for rise time and at 10 % for fall time with 125 kHz burst input signal.
[6] The necessary settling time for multitone input signals depends on the beat-note frequencies and the selected range overflow detector settings. The specified value applies for default range overflow detector settings and single tone interferers with frequencies except 62.5 kHz and 120 to 130 kHz. For details see Application Note.
[7] The time is given precisely in cycle numbers, no Min/Max values suitable. The cycle time can vary.
[8] The activation energy equals 0.15 eV. According to Arrhenius' Law, the number of useful cycles at room temperature is about 2.5 times higher than at 85 °C.
[9] Boot time up to invocation of transponder application in EROM (LF FIELD WARM BOOT vector)

10 Package outline

HVQFN40: plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm **SOT618-7**



Dimensions

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	1.00	0.05	0.30		6.1	4.75	6.1	4.75				0.5				
mm	nom	0.85	0.02	0.21	0.2	6.0	4.60	6.0	4.60	0.5	4.5	4.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		5.9	4.45	5.9	4.45				0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot618-7_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT618-7		MO-220	- - -			~~10-11-01~~ 10-11-05

Figure 37. Package outline SOT618-7 (HVQFN40)

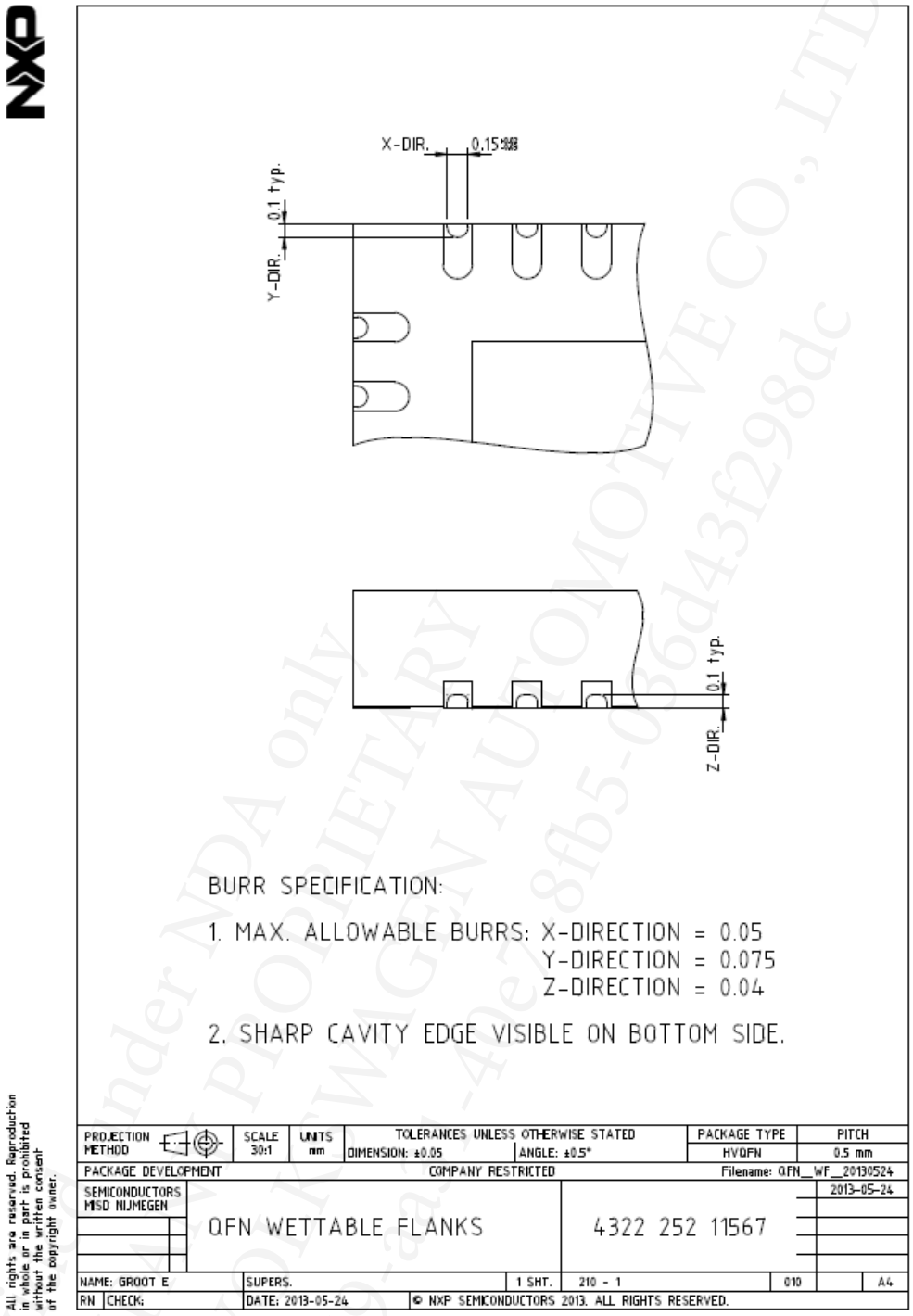


Figure 38. Package detail wettable flanks

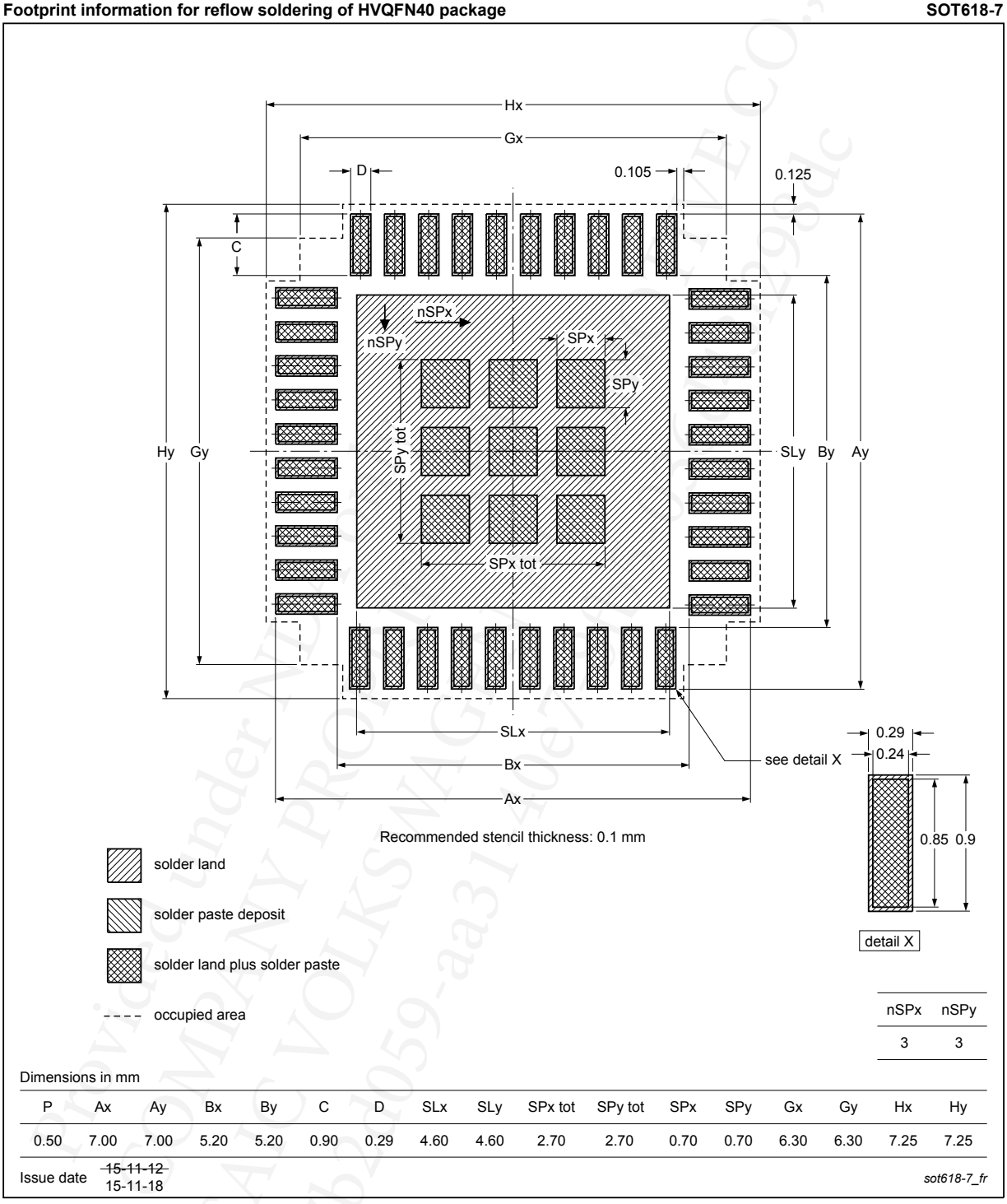
11 Packing information

NCF215A / NCF215B is available on 13" tape on reel with a minimum packing quantity of 4000 pieces per reel.

12 Soldering

12.1 Soldering footprint

Footprint information for reflow soldering of HVQFN40 package **SOT618-7**



nSPx	nSPy
3	3

Dimensions in mm

P	Ax	Ay	Bx	By	C	D	SLx	SLy	SPx tot	SPy tot	SPx	SPy	Gx	Gy	Hx	Hy
0.50	7.00	7.00	5.20	5.20	0.90	0.29	4.60	4.60	2.70	2.70	0.70	0.70	6.30	6.30	7.25	7.25

Issue date ~~15-11-12~~ 15-11-18 *sot618-7_fr*

Figure 39. HVQFN40 package reflow soldering footprint

13 Mounting

For detailed soldering and mounting information please refer to [4]. The application note provides guidelines for the use of HVQFN packages on printed circuit board (PCB), footprint design and reflow soldering.

This application note also provides guidelines for board mounting of surface mount semiconductor packages.

13.1 Pin 1 keep out area

For the purpose of package orientation, so called "pin 1" identification is included. This can either be as an additional small pin / pad as shown in design 1 (left) of Figure 40, or a notch in the die pad as shown in design 2 (right) of Figure 40.

Note that the pin 1 identifier is electrically connected to the exposed die pad.

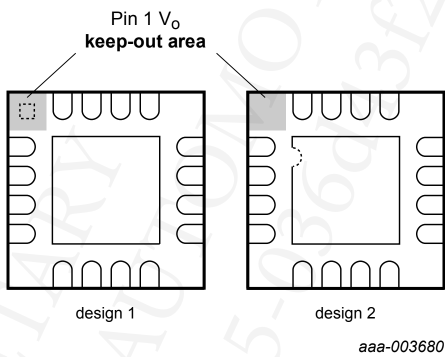


Figure 40. Pin 1 keep out area

In the event of an open trace on the PC-board, there may be unintentional contact between this trace and the pin 1 identification, leading to a malfunction. In order to prevent this, NXP prescribes a so called "keep out" area for the HVQFN corner/pin 1 area of the PC-board, as indicated in Figure 40.

Pin 1 can be identified with the terminal 1 index area depicted in Section 7.1.

14 Glossary

AC

Alternating Current

ADC

Analogue to Digital Converter

AES

Advanced Encryption Standard

AGC

Automatic Gain Control

ASK

Amplitude Shift Keying

BPLM

Binary Pulse Length Modulation

CDM

Charged Device Model

CDP encoding

Conditional DiPhase encoding, also called differential Manchester encoding. It is a line code in which data and clock signals are combined to form a single 2-level self-synchronizing data stream. It is a differential encoding, using the presence or absence of transitions to indicate logical values.

CPU

Central Processing Unit

CRC

Cyclic Redundancy Check

CW

Continuous Wave

DC

Direct Current

DNL

Differential NonLinearity

EEPROM

Electrically Erasable Programmable Read-Only Memory

EMC

ElectroMagnetic Compatibility

EROM

Execution Read-Only Memory (based on EEPROM technology)

ESD

ElectroStatic Discharge

FSM

Finite State Machine

HBM

Human Body Model

INL

Integral NonLinearity

ISM

Industrial, Scientific and Medical

IQ

In-phase/Quadrature phase

LDO

Low Drop-Out regulator

LED

Light Emitting Diode

LF

Low Frequency

LSB

Least Significant Bit

MEMS

Micro-Electro-Mechanical System

MMF

Manchester Matched Filter

MMU

Memory Management Unit

MSB

Most Significant Bit

NC

Not Connected

NRNG

Non-deterministic Random Number Generator

NRZ encoding

Non-Return to Zero encoding

OOK

On-Off Keying

PKE

Passive Keyless Entry

PLL

Phase Locked Loop

POR

Power-On-Reset

POK

Power OK

PRC OSC

Precision RC OSCillator

PRNG

Pseudo-Random Number Generator

RDT

Reserved for Device Test

RF

Radio Frequency

RFU

Reserved for Future Use

RISC

Reduced Instruction Set Computer

RKE

Remote Keyless Entry

ROM

Read-Only Memory

RSSI

Received Signal Strength Indicator

SD-ADC

Sigma-Delta Analog to Digital Converter

SFR

Special Function Register

SPI

Serial Peripheral Interface

TBD

To Be Defined

TX

Transmitter

UHF

Ultra High Frequency

ULP

Ultra Low Power

WUP

Wake-UP

15 References

[1] **UM NCF215A / NCF215B**
User manual including detailed hardware description

[2] **WFS-5c_MRKIII-MDI**
MRK III Monitor and Download Interface WFS-5c

[3] **WFS-5c_MRKIII-ROM-LIB**
MRK III ROM Library for the WFS-5c Device Family

[4] **Application note AN10365**
Surface mount reflow soldering

16 Revision history

Revision	Release date	Data sheet status	Change notice	Supersedes
1.0	12 December 2018	Product data sheet	—	0.4
Modifications:	• Replaced WFS-5c by WFS-5d in whole document • Section 8.2.1.4: Replaced wrong symbol $t_{XO32KCLK,PON}$ by t_{XO32K_set} • Section 8.3.2: Introduced Equation 1 as separate equation outside of Figure 14 • Section 8.4.3.1: Updated Equation 5 for clarity and added clock fail detection settling time $t_{XO32KFAIL\_set}$ • Section 8.4.4: Added description of t_{AGC_REC} • Section 8.4.8: Improved wording, changed resolution from less than 100 ms to 1/16th of a second • Section 9.3: – Updated nominal value and unit of G_{RSSI_36dB}, G_{RSSI_18dB}, G_{RSSI_0dB}, and G_{RSSI_-18dB} – Added new parameter K_{SDADC}			

17 Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

18 Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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