NCF215A / NCF215B

NCF215A (ACTIC-SRX-VW 3D) / NCF215B (ACTIC-SRX-VW 1D)

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Document information

Information	Content
Keywords	Car key, Vehicle Immobilization (IMMO), Passive Keyless Entry (PKE), Remote Keyless Entry (RKE), MRK III
Abstract	The NCF215A / NCF215B is a fully integrated single-chip solution combining RKE, PKE and IMMO functionality designed for use in automotive environments.

1 General information

1.1 General description

The NCF215A / NCF215B is an extremely compact single chip solution, ideally suited for automotive applications with combined vehicle immobilization and keyless entry / start functions. The device incorporates a security transponder and a RISC controller on the same chip and requires only a few external components. The security transponder operation is granted with depleted or even without external battery supply. The device is intended to operate in combination with an external UHF transmitter, typically a 2-way transceiver, such as NXP’s NCF2984. The NCF2984 device is a 2-way UHF transceiver with embedded micro-controller intended for use in an automotive environment.

The RISC controller is powered by NXP's low power hardware extended (MUL/DIV) 16-Bit MICRO RISC KERNEL (MRK IIIe) employing a 2-stage pipeline architecture in order to improve performance. For transponder, keyless entry / start operations, the on-chip hardware calculation unit or any user-defined software based algorithm can be employed for data communication.

The device is available in a 40 pin HVQFN package and features 19 I/O ports allowing for up to 19 command button inputs.

The device provides up to 2048 bytes of EEPROM for data storage with access control as defined by the application. In addition, the device supports a sophisticated EEPROM access scheme when operating as security transponder during immobilizer operation.

The device can be used in combination with an external MEMS type motion sensor (e.g. NXP’s FXLS8962) or with a mechanical motion sensor. The information from the motion sensor can be used to disable the LF active receiver block as long as motion is not detected, e.g. to protect the car key against relay station attacks when it is in rest position. Furthermore, this reduces the device’s current consumption to prolong the battery life time.

Integrated capacitor-based tuning of the LF resonance frequency optimizes receiver sensitivity and reduces bill of material cost.

2 Functional description

2.1 Special function register set

Table 1 summarizes the device Special Function Register (SFR) set. It comprises registers assigned to device hardware functions and accessible to device firmware. Detailed bit description is given in the consecutive sections.

Table 1. Device register set

Peripheral	Register name	Address	Description	Supply domain
EROM	PFCON3	015Fh	EROM control register	VDD
CPU/MMU and Cycle Counter	CXPC	0014h	CPU Exception PC value	VDD
	CXSW	0016h	CPU Exception code	
	CPUMCCCNT0	004Ch	CPU Machine Cycle Counter register 0	
	CPUMCCCNT1	004Eh	CPU Machine Cycle Counter register 1	
	CPUMCCCON	0050h	CPU Machine Cycle Counter control register	
Port 1/2/3	P1INS	0018h	Port 1 input sense register	VDD
	P1OUT	0019h	Port 1 output control register	
	P1DIR	001Ah	Port 1 direction control register	
	P1INTDIS	001Bh	Port 1 Interrupt Disable	
	P2INS	001Ch	Port 2 input sense register	
	P2OUT	001Dh	Port 2 output control register	
	P2DIR	001Eh	Port 2 direction control register	
	P2INTDIS	001Fh	Port 2 Interrupt Disable	
	P3INS	0020h	Port 3 input sense register	
	P3OUT	0021h	Port 3 output control register	
	P3DIR	0022h	Port 3 direction control register	
	P3INTDIS	0023h	Port 3 Interrupt Disable	
	P1ALTF	00C8h	Port 1 alternative digital functions register	
	P2ALTF	00CAh	Port 2 alternative digital functions register	
	P1WRES	00ACh	Port 1 Pull-up Resistor Configuration	VBAT [1]
	P2WRES	00ADh	Port 2 Pull-up Resistor Configuration	
	P3WRES	00AEh	Port 3 Pull-up Resistor Configuration	
	PRESWUP0	00A2h	Port Wake-up Configuration register 0	
	PRESWUP1	00A4h	Port Wake-up Configuration register 1	
	PRESWUP2	00A6h	Port Wake-up Configuration register 2	
	PRESWUP3	00A8h	Port Wake-up Configuration register 3	
	PRESWUP4	00AAh	Port Wake-up Configuration register 4	

Peripheral	Register name	Address	Description	Supply domain
IIU	IIUDAT	0027h	IIU data register	VDD
	IIUCON0	0024h	IIU control register 0	
	IIUCON1	0026h	IIU control register 1	
	IIUCON2	0029h	IIU control register 2	
	IIUSTAT	0025h	IIU status register	
	IIUSTATE	0028h	IIU state register	
	I3DCON	0031h	IMMO 3D control register	
Generic CRC	GCRCCON0	0037h	Generic CRC control register	VDD
	GCRCPOLY	0038h	Generic CRC polynomial register	
	GCRCDAT	003Ah	Generic CRC data register	
	GCRCDIN	003Ch	Generic CRC data input register	
AES	AESDAT	0032h	AES data register	VDD
	AESCON	0034h	AES control register	
Watchdog timer	WDCON	0051h	Watchdog timer control register	VDD
Clock Control	CLKCON0	0052h	Clock Control register 0	VDD
	CLKCON1	0053h	Clock Control register 1	
	CLKCON2	0054h	Clock Control register 2	
	CLKCON3	0055h	Timer multiplexors control register	
	CLKCON4	0057h	Clock Control register 4	
LF Active Interface, Interval Timer, Real-time Clock	LFAEN0	0100h	LF active enable register 0	VBATREG [2]
	LFAEN1	0101h	LF active enable register 1	
	LFAEN2	0102h	LF active enable register 2	
	LFAEN3	0103h	LF active enable register 3	
	LFAEN4	0104h	LF active enable register 4	
	LFACON0	0105h	LF active control register 0	
	LFACON1	0106h	LF active control register 1	
	LFACON2	0107h	LF active control register 2	
	LFACON4	0109h	LF active control register 4	
	LFACON5	010Ah	LF active control register 5	
	LFACON6	010Bh	LF active control register 6	
	LFASTATUS	010Ch	LF active status register	
	LFASENSE	010Dh	LF active sensitivity control register	
	LFACON7	0134h	LF active control register 7	
	LFACON8	013Bh	LF active control register 8	
	WUPCON	010Eh	Wake-up receiver control register	
	WUPPATEVN0	0110h	Wake-up pattern even configuration register 0	

Peripheral	Register name	Address	Description	Supply domain
	WUPPATEVN1	0112h	Wake-up pattern even configuration register 1	
	WUPPATEVN2	0114h	Wake-up pattern even configuration register 2	
	WUPPATODD0	0116h	Wake-up pattern odd configuration register 0	
	WUPPATODD1	0118h	Wake-up pattern odd configuration register 1	
	WUPPATODD2	011Ah	Wake-up pattern odd configuration register 2	
	WUPPATCON	011Ch	Wake-up pattern control register	
	PAYRXCON	011Eh	Payload receiver control register	
	PREDAT	0120h	Pre-processor data register	
	PRECON2	0122h	Pre-processor control register 2	
	PRECON3	0123h	Pre-processor control register 3	
	PRECON4	0124h	Pre-processor control register 4	
	PRECON5	0125h	Pre-processor control register 5	
	PRESTAT	0126h	Pre-processor status register	
	RTCCON	0121h	Real-time clock control register	
	RTCDAT	0128h	Real-time clock data register	
DCDC converter	DCDCCON0	014Ah	DCDC control register 0	VBATREG [2]
	DCDCCON1	014Bh	DCDC control register 1	
	DCDCCON3	014Dh	DCDC control register 3	
	DCDCCON4	014Eh	DCDC control register 4	
	DCDCCON6	0150h	DCDC control register 6	
	DCDCCON7	0151h	DCDC control register 7	
	DCDCCON8	013Eh	DCDC control register 8	
Motion Sensor Interface	MSICON0	0142h	Motion sensor control register 0	VBATREG [2]
	MSICON1	0143h	Motion sensor control register 1	
	MSICON2	0146h	Motion sensor control register 2	
	MSISTAT0	0144h	Motion sensor status register 0	
	MSISTAT1	0145h	Motion sensor status register 1	
Post Wake-Up Timer	POSTWUPCON	0147h	Post-WUP control register	VBATREG [2]
	POSTWUPCOMP	0148h	Post-WUP compare register	
ADC	ADCDAT	005Ah	ADC data / lower sum register	VDD
	ADCSUM	005Ch	ADC sum counter and upper sum register	
	ADCCON	005Eh	ADC control register	
Analogue Inputs (DC bus)	BISTCON	016Ch	DC bus control register	VDD

Peripheral	Register name	Address	Description	Supply domain
RSSI	RSSICON0	0060h	RSSI control register 0	VDD
	RSSICON1	0152h	RSSI control register 1	
	RSSICON2	0153h	RSSI control register 2	
	RSSICON3	0154h	RSSI control register 3	
	RSSICON4	0155h	RSSI control register 4	
	RSSICON5	0156h	RSSI control register 5	
	RSSICON7	015Ah	RSSI control register 7	
	RSSIVAL	0158h	RSSI result register	
ULP EEPROM	ULPDAT	0069h	ULP EEPROM data register	VDD
	ULPCON0	0068h	ULP EEPROM control register 0	
	ULPCON1	006Dh	ULP EEPROM control register 1	
	ULPSEL	0066h	ULP EEPROM selection register	
	ULPADDR	0064h	ULP EEPROM address register	
	ULPHVERR0	006Ch	ULP EEPROM hardware error register 0	
	ULPHVERR1	006Bh	ULP EEPROM hardware error register 1	
	ULPERROR	006Ah	ULP EEPROM error register	
Timer 0	T0REG	0070h	Timer 0 register	VDD
	T0CON0	006Eh	Timer 0 control register 0	
	T0CON1	006Fh	Timer 0 control register 1	
	T0RLD	0072h	Timer 0 reload register	
Timer 1	T1REG	0078h	Timer 1 register	VDD
	T1CON0	0074h	Timer 1 control register 0	
	T1CON1	0075h	Timer 1 control register 1	
	T1CON2	0076h	Timer 1 control register 2	
	T1CMP	007Ch	Timer 1 compare register	
	T1CAP	007Ah	Timer 1 capture register	
Timer 2	T2REG	0080h	Timer 2 register	VDD
	T2CON0	007Eh	Timer 2 control register 0	
	T2CON1	007Fh	Timer 2 control register 1	
	T2RLD	0082h	Timer 2 reload register	
RNG	RNGDAT	0084h	Random number generator data register	VDD
	RNGCON	0086h	Random number generator control register	
Interrupt system	INTEN0	008Bh	User interrupt enable register 0	VDD
	INTEN1	008Ch	User interrupt enable register 1	
	INTEN2	008Dh	User interrupt enable register 2	
	INTCON	0087h	Interrupt control register	

Peripheral	Register name	Address	Description	Supply domain
	SYSINTEN0	008Eh	System interrupt enable register 0	
	SYSINTEN1	008Fh	System interrupt enable register 1	
	INTFLAG0	0088h	Interrupt request flag register 0	
	INTFLAG1	0089h	Interrupt request flag register 1	
	INTFLAG2	008Ah	Interrupt request flag register 2	
	INTSET0	0090h	Interrupt set register 0	
	INTSET1	0091h	Interrupt set register 1	
	INTSET2	0092h	Interrupt set register 2	
	INTCLR0	0093h	Interrupt clear register 0	
	INTCLR1	0094h	Interrupt clear register 1	
	INTCLR2	0095h	Interrupt clear register 2	
	INTVEC	0096h	User interrupt vector address	
Battery Control	BATSYS0	00A0h	Battery domain system control register 0	VBAT [1]
	BATSYS1	00A1h	Battery domain system control register 1	
Regulated Battery Domain user registers	USRBATRGL0	012Ah	Pre-processor user register 0	VBATREG [2]
	USRBATRGL1	012Bh	Pre-processor user register 1	
	USRBATRGL2	012Ch	Pre-processor user register 2	
	USRBATRGL3	012Dh	Pre-processor user register 3	
	USRBATRGL4	012Eh	Pre-processor user register 4	
	USRBATRGL5	012Fh	Pre-processor user register 5	
	USRBATRGL6	0130h	Pre-processor user register 6	
	USRBATRGL7	0131h	Pre-processor user register 7	
Battery Domain user registers	USRBAT0	00B2h	Battery domain user register 0	VBAT [1]
	USRBAT1	00B3h	Battery domain user register 1	
	USRBAT2	00B4h	Battery domain user register 2	
	USRBAT3	00B5h	Battery domain user register 3	
	USRBAT4	00B6h	Battery domain user register 4	
	USRBAT5	00B7h	Battery domain user register 5	
	USRBAT6	00B8h	Battery domain user register 6	
	USRBAT7	00B9h	Battery domain user register 7	
LF Tune Active	LFTUNECH1ACT	00AFh	Battery domain LF tuning register	VBAT [1]
	LFTUNECH2ACT	00B0h	Battery domain LF tuning register	
	LFTUNECH3ACT	00B1h	Battery domain LF tuning register	
LF Tune Immo	LFTUNECH1IMMO	00BAh	Vdd domain LF tuning register	VDD
	LFTUNECH2IMMO	00BBh	Vdd domain LF tuning register	
	LFTUNECH3IMMO	00BCh	Vdd domain LF tuning register	

Peripheral	Register name	Address	Description	Supply domain
LF Short	LFSHCON	0098h	LF Channels short control register	VDD
Power management	PCON0	0099h	Power control register 0	VDD
	PCON1	009Ah	Power control register 1	
	PCON2	009Bh	Power control register 2	
	PCON5	009Eh	Power control register 5	
SPI0	SPI0CON0	00C0h	SPI0 control register 0	VDD
	SPI0CON1	00C1h	SPI0 control register 1	
	SPI0DAT	00C2h	SPI0 data register	
	SPI0STAT	00C3h	SPI0 status register	
SPI1	SPI1CON0	00C4h	SPI1 control register 0	VDD
	SPI1CON1	00C5h	SPI1 control register 1	
	SPI1DAT	00C6h	SPI1 data register	
	SPI1STAT	00C7h	SPI1 status register	
LED control	LEDCON	00CFh	LED current range control register	VDD
Mathematical/ logical registers	BITSWAP	00CEh	Bit swap register	VDD
	BITCNT	00CCh	Bit count register	
	CRCDAT	0035h	CRC data register	
	CRC8DIN	0036h	CRC data input register	
Device Identification	IDENT	00FEh	Device identification register	VDD

[1] Under normal operating conditions all registers belonging to VBAT domain keep their content as long as VBAT power supply is maintained and BATPOR is not asserted. It is recommended that the application software refreshes these registers to improve the system robustness in case of EMC stress conditions.

[2] Under normal operating conditions all registers belonging to VBATREG domain keep their content as long as VBATREG power supply is maintained. It is recommended that the application software refreshes these registers to improve the system robustness in case of EMC stress conditions.

2.1.1 Register access definition

Different register fields support different read/write access mechanisms. The symbols defined in Table 2 are used throughout all register description tables to describe the supported access mechanisms.

Table 2. Register access definition

Symbol	Read access	Write access
-/-	Undefined, reading may return any value	Not supported, writing has no effect
R/-	Supported	Not supported, writing has no effect
R0/-	Supported, reading returns always ‘0’	Not supported, writing has no effect
R1/-	Supported, reading returns always ‘1’	Not supported, writing has no effect
R&C/-	Supported; the register field is cleared (i.e. set to ‘0’) immediately after reading	Not supported, writing has no effect
-/W	Undefined, reading may return any value	Supported

Symbol	Read access	Write access
-/W0 [1]	Undefined, reading may return any value	The application shall write a ‘0’ for future compatibility
-/W1 [1]	Undefined, reading may return any value	The application shall write a ‘1’ for future compatibility
R/W	Supported	Supported
R0/W0 [1]	Supported, reading returns always ‘0’	The application shall write a ‘0’ for future compatibility
R0/W	Supported, reading returns always ‘0’	Supported
R1/W	Supported, reading returns always ‘1’	Supported
R/W1->0	Supported	Writing a ‘1’ sets the register field to ‘0’; writing a ‘0’ has no effect

[1] This access definition is typically used for register fields that are reserved for future use (RFU) or reserved for device test (RDT) and shall ensure software compatibility with future device versions.

2.2 Power management

2.2.1 Power supply domains

The NCF215A / NCF215B features several power supply domains (see Figure 1). A versatile power management (see Figure 2) enables the device to derive its power supply from two different energy sources

- External battery (VBAT)
- Low frequency field (VFLDLF)

The two corresponding power supply domains VBAT and VFLDLF are unregulated. The device is able to operate when any of the energy sources is available regardless the presence or absence of the other.

Derived from either of the two unregulated domains are the regulated power supply domains:

- Digital core supply (VDD)
- Analogue core supply (VDDA)

Derived from the unregulated VBAT domain are the regulated power supply domains:

- Digital regulated battery supply (VBATREG)
- LF active supply (VLFA)
- LF active digital supply (VLFADIG)
- Sigma-Delta ADC supply (VSDADC)

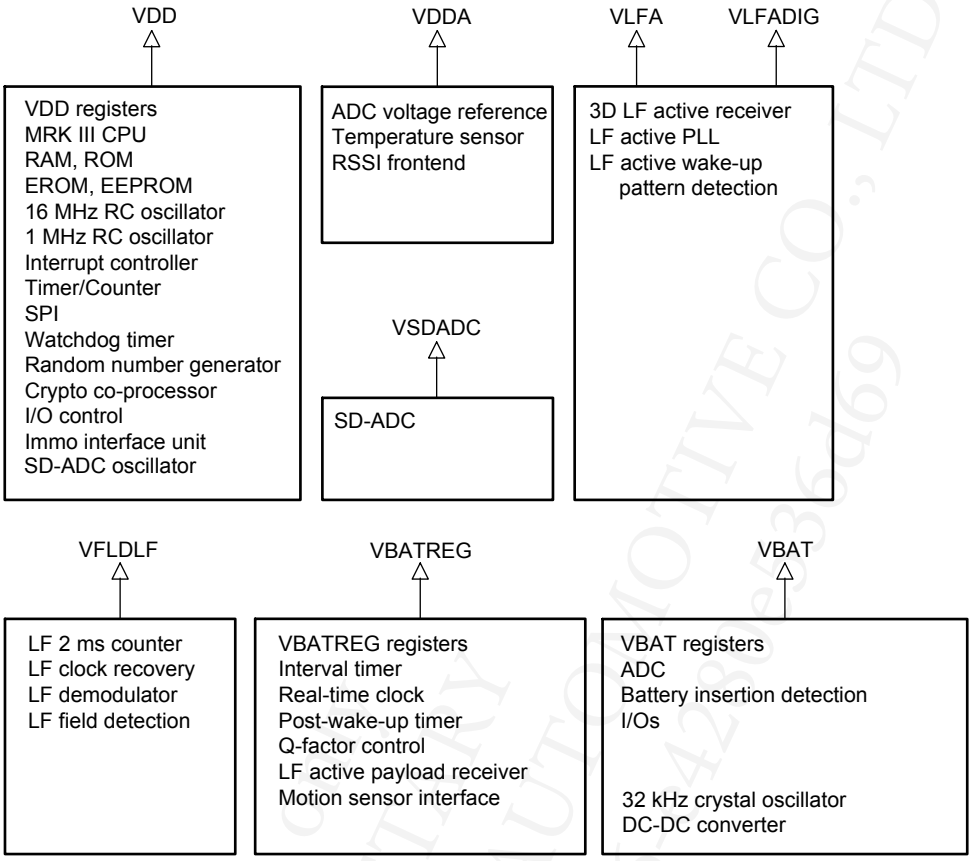


Figure 1. Power supply domains

Except VDD, the voltage regulators for all supplies are turned off after first device start-up. In order to employ the blocks supplied with these voltages, the respective dedicated voltage regulators have to be activated first.

Determining the appropriate supply configuration is accomplished by means of the power supply control (Figure 2).

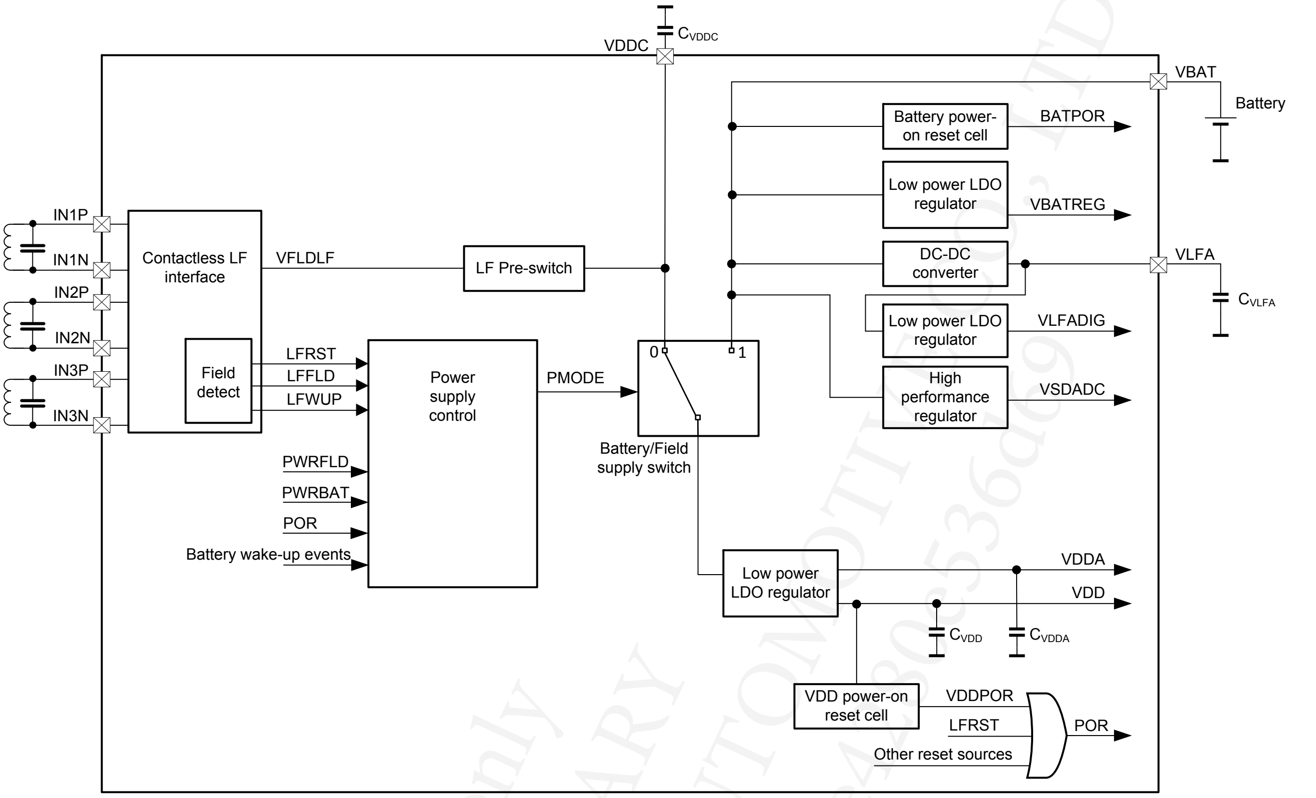


Figure 2. Power supply control

2.2.2 Power supply control

2.2.2.1 Power supply switch

The NCF215A / NCF215B provides several switches for power supply selection of the core. The main supply switch selects between battery and field supply.

The field supply is generated with one pre-switch for the LF. The LF pre-switch features a current limitation in order to limit the energy transferred from the field into the supply capacitor at VDDC. This avoids deep dips in the field supply, which might be erroneously interpreted as a load modulation by the base station.

When the power supply state is changed the device supply switch opens the existing connection before connecting the new supply. The device is powered for a short period of time from the internal supply capacitor C_{VDD}. Therefore, the application must minimize the current consumption when changing the supply state to prevent an accidental power-on reset.

2.2.2.2 Device wake-up

The following wake-up events terminate the POWER OFF state and switch to the LF FIELD- or BATTERY state (see Figure 4):

- LF field wake-up events
  – Presence of LF field (LFWUP)
- Battery wake-up events

- Battery insertion (BATPOR)
- Port wake-up (e.g. button press)
- Detection of valid LF active wake-up pattern
- Interval timer or real-time clock wake-up
- Motion sensor interface wake-up
- LF active monitors: VLFA brownout, 32 kHz crystal oscillator clock fail detected, DC-DC converter fail detected
- Watchdog time-out event

If a wake-up event emerges, the power management selects the corresponding power supply. If more than one wake-up event is pending at the same time, the power management automatically selects the strongest available supply source related to the wake-up event.

Once the supply voltage VDD exceeds the power-on reset threshold voltage V_{POR}, the power-on reset comparator output signal (VDDPOR) becomes low after a short delay t_{POR_HLD}, whereupon the power management state is locked, the RISC becomes operational and the device enters RUN mode (Section 2.7.1.1). All further supply state changes are under control of the application (Figure 3).

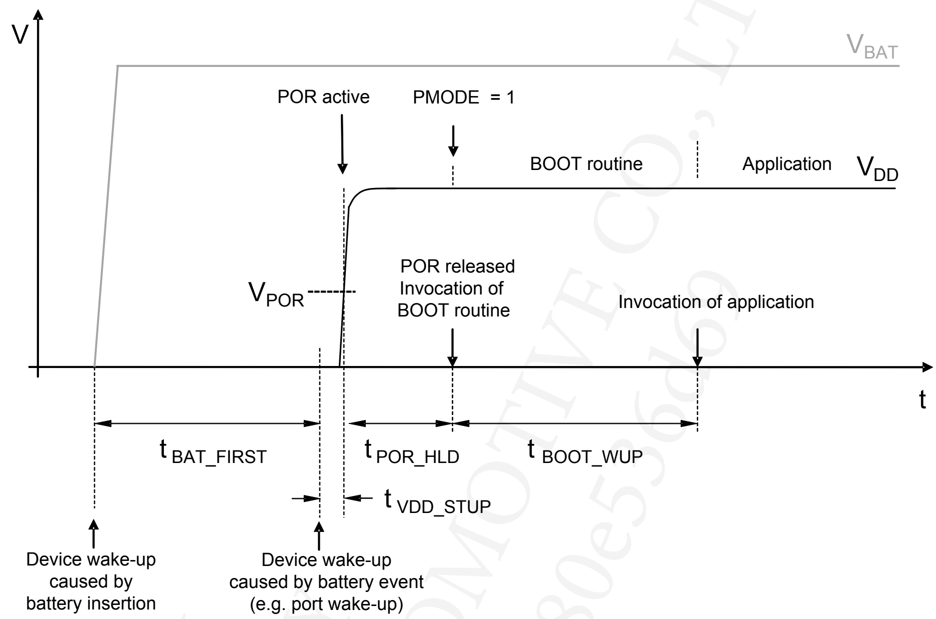
Starting with the boot sequence, the power supply state of the VDD supplied part can be monitored and controlled via the power control registers. A change of the supply configuration may apply e.g. in case an LF Field and a button press are detected at the same time or in case an LF Field is being detected while battery supply has been utilized. If during the boot sequence an LF field and a battery wake-up event are pending at the same time, then the LF Field wake-up is given precedence and will commence.

2.2.2.3 Device reset

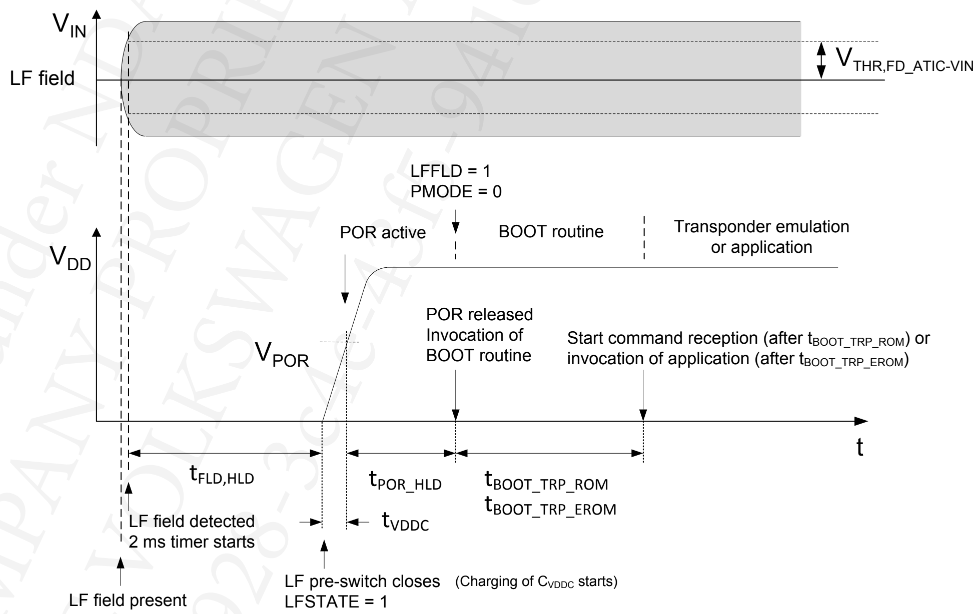
A power-on reset (POR) for the core is generated under the following conditions:

- The device is in the POWER OFF state
- The voltage level at VDD is below the power-on reset threshold V_{POR} (VDDPOR)
- An LF field emerges and the device is configured for a reset (LFRST)
- The voltage level at VDD falls below the VDD brownout threshold $V_{BO,VDD}$ and
  i) code is executed from the EROM, or
  ii) the CPU clock source is set to a frequency greater than 8 MHz
- A watchdog timer overflow occurs
- A reset of the VDD domain is triggered by the application (software reset)
- A CPU/MMU exception occurs and the device is configured for a reset

Upon a device reset the power management logic is released and starts with a new evaluation of the supply condition.



a) Device wake-up caused by battery insertion or another battery wake-up event (e.g. a port wake-up)



b) Device wake-up cause by LF field

Figure 3. Power-up timing

2.2.2.4 Power supply states

The device support two different core supplies, depending on where whether the device power is derived from the external battery or the LF field:

- Battery supply (BATTERY state)
- LF field supply (LF FIELD state)

In these two supply states the RISC is functional. In the POWER OFF state, the device remains in a third very low power state and the RISC is not functional (see Figure 4).

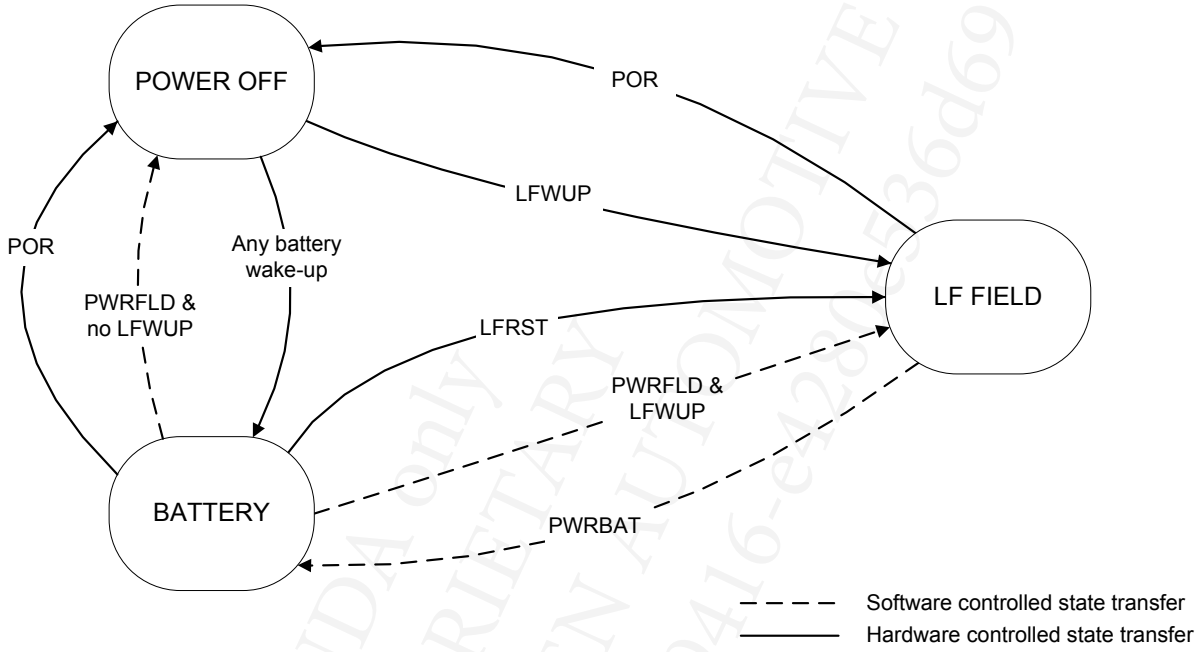


Figure 4. Power Supply States

2.2.2.5 POWER OFF state

In the POWER OFF state, most blocks are internally disconnected from the battery supply, resulting in a very low current consumption. The internal device supply voltage (VDD) stays below the power-on reset threshold voltage and device operation is halted. Only a minimum of circuitry remains operational, like the power management and I/O ports (configured as input).

The device resides in the POWER OFF state any time a power-on reset comparator indicates (VDDPOR) a weak supply condition. The POWER OFF state is terminated by a wake-up event, such as detected presence of an LF field (LFWUP) or any battery wake-up event.

Once the supply condition is evaluated during device power-up and the boot sequence is completed, the device will start execution of the application program in either the BATTERY state or the LF FIELD state.

2.2.2.6 BATTERY state

In the BATTERY state, the device is powered from the external battery. After execution of the boot sequence, device operation is controlled by the RISC and the program code

starts at the BATTERY WARM boot vector. The application code can terminate the BATTERY state.

In case an LF field is detected when the device is in the BATTERY state, the device behavior depends on the configuration. If according to the configuration a non-maskable interrupt (NMI) is caused after field detection, the BATTERY state is kept and control is still with the RISC. The application program can activate the LF field switch (PWRFLD) to provoke a change to the LF FIELD state. If according to the configuration field detect causes a reset (LFRST), the state is changed to LF FIELD and the boot routine is invoked again.

Once in the BATTERY state, any further battery wake-up event does not cause a state change and has to be handled via the RISC.

If the device wants to terminate the BATTERY state, it has to activate the LF field switch (PWRFLD). If no LF supply is present, the device enters the POWER OFF state as soon as VDD falls below the power-on reset threshold (VDDPOR event).

2.2.2.7 LF FIELD state

In LF FIELD state the device supply is derived from the LF Interface.

After execution of the boot sequence, device operation is controlled by the RISC and the program code starts at the LF FIELD WARM boot vector (unless a built-in LF transponder emulation is selected in the boot routine).

In case a weak LF field supply condition causes a power-on reset (VDDPOR), the LF FIELD state is left and the device enters the POWER OFF state.

If the device is in the LF FIELD state and the application program activates the battery supply switch (PWRBAT), the device changes to the BATTERY state.

2.2.3 Battery supply states

The battery supply domains VBATREG, VLFA, and VLFADIG can be programmed individually by the application program and they support the following combinations of battery supply states:

- VBATREG = OFF, VLFA = OFF, VLFADIG = OFF
- VBATREG = ON, VLFA = OFF, VLFADIG = OFF
- VBATREG = ON, VLFA = ON, VLFADIG = OFF
- VBATREG = ON, VLFA = ON, VLFADIG = ON

The supply domain VLFA is generated by a highly efficient multi-ratio DC-DC converter, which controls the conversion ratio continuously based on the available supply voltage VBAT and the load current. The DC-DC converter is fully integrated and requires only one external buffer capacitor C_{VLFA}.

The battery supply states are independent of the power supply states which are related to the core.

2.2.4 Registers

2.2.4.1 Battery system register BATSYS0

The battery system register BATSYS0 controls the VBAT regulator. The VBAT regulator shall be turned on in order to get access to the blocks supplied by the regulated battery supply VBATREG, like the interval timer and LF active preprocessor.

BATSYS0 is fully accessible in SYSTEM mode only. An application executed in USER mode shall use a system call to change the register. A description on how to use the system call can be found in [2].

Table 3. Battery system register BATSYS0 (reset value xxxx_x101b)

Bit	Symbol	Access	Value	Description
7 to 4	RDT	-/-		Reserved for device test
0				
1				
3	RFU	-/-		Reserved for future use
2	BATRGLRST	R/-		Static reset of VBATREG supplied part
			0	Reset released
			1	Reset active
1	BATRGLEN	R/-		VBAT regulator enable
			0	Disabled
			1	Enabled
0	BATPORFLAG	R/-		VBAT power-on reset flag
			0	Cleared
			1	Set

BATRGLRST, static reset of VBATREG supplied part

When set 1, the BATRGLRST resets the battery powered registers in the VBATREG domain. BATRGLRST must be set 0 to release the registers from reset state. Note, if the BATRGLRST is not cleared, read access to VBATREG registers will always return zero, not the reset values.

BATRGLEN, VBAT regulator enable

Power-on and power-off the VBAT regulator is controlled by the BATRGLEN bit.

BATPORFLAG, VBAT power-on reset flag

BATPORFLAG can be set or cleared by dedicated system call. The main purpose of this bit is, when set to 1, to ensure the currently running function by software is completed before a power-down may take place. Hence, if BATPOR is low and BATPORFLAG is high, so if BATPORFLAG was not cleared by software, a battery insertion device wake-up will occur after the next device power-down.

2.2.4.2 Battery system register BATSYS1

The battery system register BATSYS1 controls the battery reset.

BATSYS1 is fully accessible in SYSTEM mode only. An application executed in USER mode shall use a system call to change the register. Description on how to use the system call can be found in [2].

Table 4. Battery system register BATSYS1 (reset value xxxx_xxx0b)

Bit	Symbol	Access	Value	Description
7 to 1	RDT	R/-		Reserved for device test
0	BATRST	R/-		Reset of VBAT supplied part
			0	No effect
			1	Reset

BATRST, reset of VBAT supplied part

Setting this bit has the same effect as a battery reset caused by a battery insertion. All registers supplied with VBAT are initialized to their default states. The VBAT regulator is turned off and BATRGLRST is set.

2.2.4.3 Power control register PCON0

The power control register PCON0 provides means to select the supply state of the device and the behavior of the LF passive mode.

Table 5. Power control register PCON0 (reset value 0100_x000b)

Bit	Symbol	Access	Value	Description
7	VDDRST	R0/W		Reset of VDD supplied part
			0	No effect
			1	Reset
6	VDDARST	R/W		Static reset of VDDA supplied part
			0	Release reset
			1	Reset
5	VDDARGLEN	R/W		Enable VDD regulator for battery and die temperature measurement
			0	Disable
			1	Enable
4	PRESW_MODE	R/W		Pre-switch mode
			0	see Table 6
			1	see Table 6
3	VBATBRNIND	R/-		Low battery brownout indicator flag
			0	The voltage level at VBAT is above $V_{VBATIND}$ [1]
			1	The voltage level at VBAT is below $V_{VBATIND}$ [1]
2	PRESW_LF	R/W		Pre-switch for LF supply
			0	see Table 6
			1	see Table 6
1	PWRBAT [2]	R0/W		Activate power supply from battery

Bit	Symbol	Access	Value	Description
			0	No effect
			1	Activate
0	PWRFLD [2]	R0/W		Activate power supply from field
			0	No effect
			1	Activate

[1] Please consider the hysteresis $V_{VBATIND\_HYST}$ for the dynamic behavior.
[2] If PWRBAT and PWRFLD are set to '1' at the same time, PWRFLD has priority.

VDDRST, Reset of VDD supplied part

By setting VDDRST, a power-on reset (POR) is triggered, the POWER OFF state is entered, a reset of the entire VDD supplied part is executed, the VDDA regulator is powered off and the bit VDDARST is set. VDDRST reads always ‘0’. A pending wake-up triggers an immediate re-boot of the device.

VDDARST, static reset of VDDA supplied part

VDDARST is a static reset signal for the VDDA supplied part. If the VDDA regulator is turned off (VDDARGLEN = '0'), VDDARST is always active.

Setting VDDARST to '0' releases the reset of the VDDA supplied part and is only possible when the VDDA regulator is turned on (VDDARGLEN = '1'). Before VDDARST can be released, the VDDA regulator start-up time $t_{VDDA,PON}$ must be considered.

VDDARGLEN, VDDA regulator enable

The VDDA regulator can be powered on and off by setting and resetting VDDARGLEN, respectively. For VDDARGLEN = '0', VDDARST will become '1' automatically.

Example: In order to turn on the VDDA regulator, execute the following steps:

- Set VDDARGLEN to '1': This activates the VDDA regulator.
- Wait the time $t_{VDDA,PON}$ until the voltage at VDDA has stabilized (do not use the VDDA brownout detector flag VDDABRNFLAG to determine this time).
- Reset VDDARST to release the static reset and to activate the VDDA domain.

The application shall only enable the VDDA regulator, if the voltage at VDD is sufficiently large, i.e. the VDD brownout flag VDDBRNFLAG is '0'. Otherwise the activation of the VDDA regulator can generate a VDD reset.

PRESW_MODE, PRESW_LF, Activate LF field pre-switch

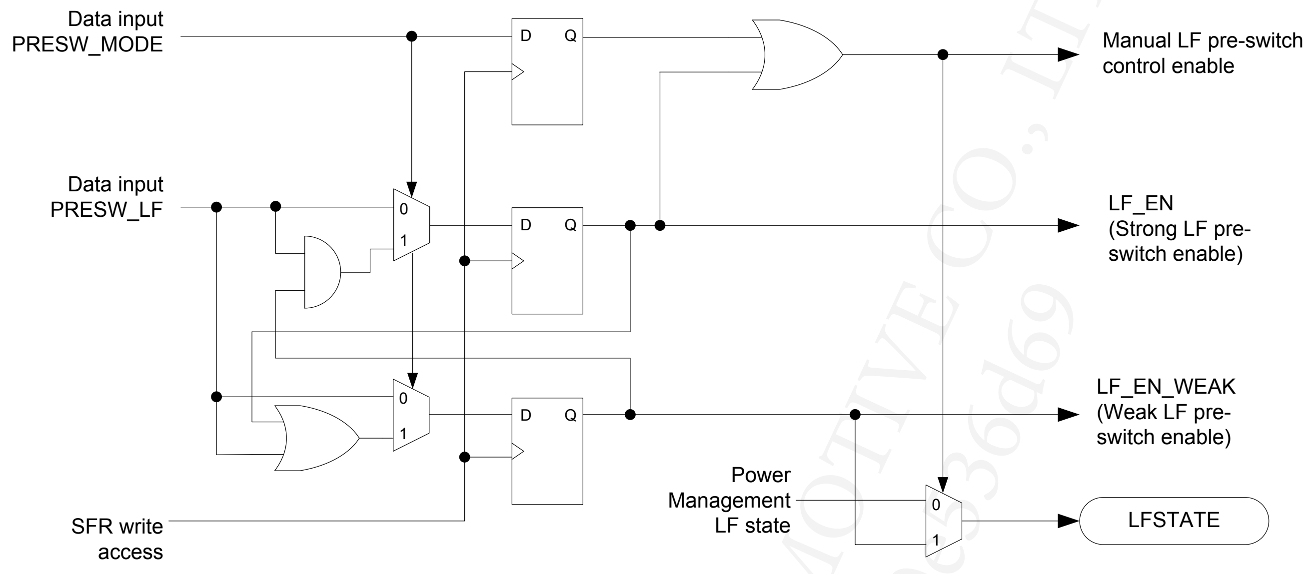


Figure 5. Manual LF pre-switch control

These two control bits are used to activate the pre-switch for LF field supply (Figure 5). If at least one of these bits is set, the LF pre-switch is controlled manually by the application and the state of the power management field selection after device start-up is ignored.

The control of PRESW_MODE and PRESW_LF is organized in a state machine, which valid state transitions are given in Table 6.

Table 6. Valid state transitions for PRESW_MODE, PRESW_LF and LFSTATE

Previous state			New data		Next state		
PRESW _MODE	PRESW_LF	LFSTATE	PRESW-_ MODE	PRESW_LF	PRESW _MODE	PRESW_LF	LFSTATE
X	X	X	0	0	0	0	0
X	X	X	0	1	0	1	1
X	0	0	1	0	1	0	0
X	0	0	1	1	1	0	1
1	0	1	1	0	1	0	0
1	0	1	1	1	1	1	1
X	1	1	1	0	1	0	1
X	1	1	1	1	1	1	1

If PRESW_MODE is equal to '0' the bit PRESW_LF controls the weak and the strong pre-switches directly. It is possible to activate and deactivate the pre-switches with one write access.

If the bit PRESW_MODE is equal to '1' the weak and the strong pre-switch can be activated and deactivated in a sequence. If a '1' is written to PRESW_LF the weak pre-switch is activated, while the register bit PRESW_LF is not yet set. Instead a shadow flag is set, which activates the weak pre-switch. The state of the weak pre-switch can

be observed via the control bit LFSTATE in this case. The strong pre-switch is finally activated, if the application writes another '1' to register PRESW_LF. The de-activation follows the same procedure: The first '0' deactivates the strong pre-switch and the second '0' the weak one.

The value, which is written to PRESW_MODE at the same time when PRESW_LF is written, determines the mode rather than the stored value in the register. The register content of PRESW_MODE is required to ensure the manual pre-switch control in case no strong pre-switch is activated.

Example: In order to switch power supply from battery to LF field, execute the following steps:

- Close the pre-switch of the LF supply by writing a '1' to PRESW_LF. The supply capacitor at pin VDDC gets charged (if the activation of the strong pre-switch causes a too deep dip in the field supply it is also possible to close only the weak pre-switch prior to the strong one).
- Wait until the voltage at VDDC has settled. The waiting time shall be properly determined for specific capacitance values and field strengths by the user.
- Set the bit PWRFLD to '1' to commutate from battery supply to field supply.

VBATBRNIND, Low battery indicator

Battery monitoring used to identify battery end of life ($V_{VBATIND}$), VBATBRNINDEN bit must be set to '1'. The battery indicator connects a resistive load ($R_{VBATIND}$) across the VBAT supply.

PWRBAT, Activate power supply from battery

If the device is supplied by field and a '1' is written to register bit PWRBAT the main supply switch commutates to battery supply. If the device is already supplied by battery writing a '1' has no effect. The bit reads always '0'.

The application shall reduce the power consumption as much as possible when changing the supply condition. Moreover, the CPU shall not run at a clock speed of more than 250 kHz when PWRBAT is set to '1'. These measures avoid an unintentional reset caused by the "break-before-make" mechanism of the supply switches.

If PWRFLD and PWRBAT are set to '1' at the same time, PWRFLD has priority.

In order to enter POWER-OFF state when the device is running with battery supply, set VDDRST to one.

PWRFLD, Activate power supply from field

If the device is supplied by the battery and a '1' is written to register bit PWRFLD the main supply switch commutates to field supply. If the device is already supplied by field, writing a '1' has no effect. The bit reads always '0'.

PWRFLD does not influence the LF field pre-switch.

The application shall reduce the power consumption as much as possible when changing the supply condition. Moreover, the CPU shall not run at a CPU clock speed of more than 250 kHz when PWRFLD is set to '1'. These measures avoid an unintentional reset caused by the "break-before-make" mechanism of the supply switches.

If PWRFLD and PWRBAT are set to '1' at the same time, PWRFLD has priority.

2.2.4.4 Power control register PCON1

The power control register PCON1 provides flags to monitor the current state of the power management, battery voltage and the field supply.

Table 7. Power control register PCON1 (reset value xx0x_xxxxb)

Bit	Symbol	Access	Value	Description
7	VDDBRNFLAG	R/-		VDD brownout detector flag
			0	VDD voltage level is above brownout threshold
			1	VDD voltage level is below brownout threshold
6	VDDABRNFLAG	R/-		VDDA brownout detector flag
			0	VDDA voltage level is above brownout threshold
			1	VDDA voltage level is below brownout threshold
5	VBATMONEN	R/W		Battery monitoring control
			0	Battery brownout disabled
			1	Battery brownout enable
4	PWRMANLFSTATE	R/-		LF field supply state
			0	Device start-up: LF pre-switch open (insufficient LF field) Manual control: LF pre-switch is turned off
			1	Device start-up: LF pre-switch selected by power management Manual control: Weak LF pre-switch is turned on
3	VBATBRNFLAG	R/-		VBAT brownout detector flag
			0	VBAT voltage level is above brownout threshold
			1	VBAT voltage level is below brownout threshold
2	LFFLD	R/-		LF field detection
			0	LF field does not exceed detection threshold for > $t_{FLD,HLD}$ (2 ms)
			1	LF field exceeds detection threshold for > $t_{FLD,HLD}$ (2 ms)
1	PMODE	R/-		Power mode
			0	Device is powered with field supply
			1	Device is powered with battery supply
0	PWUPIND	R/-		Port wake-up indicator
			0	Battery supply: No effect Field supply: No port wake-up request detected
			1	Battery supply: N.A. Field supply: Port wake-up request detected

VDDBRNFLAG, VDD brownout detector flag

The brownout detector at VDD monitors the supply voltage level continuously and it checks, whether VDD is above or below a certain threshold that is necessary for proper EROM read operation and programming of the EROM and the ULP EEPROM modules. The brownout detector uses a hysteresis, thus the activation threshold can be slightly higher than the deactivation threshold.

VDDBRNFLAG influences the bit VDDBRNREG.

A device reset is generated only, if the voltage at VDD drops below the brownout threshold and one of the following conditions are given:

- Code is executed from the EROM
  Note: Any other read/write/program access to the EROM or EEPROM does not generate a device reset. It is up to the application to verify the brownout flag and discard read or programmed data, if the voltage dropped below the brownout threshold.
- A CPU clock source with a frequency greater than 8 MHz is selected (CPUCLKSEL[0] = 1b).

VDDABRNFLAG, VDDA brownout detector flag

The brownout detector at VDDA monitors the supply voltage level continuously and it checks, whether VDDA is above $V_{BO,VDDA}$ that is necessary for proper operation of all VDDA supplied parts. The brownout detector uses a hysteresis, thus the activation threshold can be slightly higher than the deactivation threshold.

The bit VDDABRNFLAG only influences the bit VDDABRNREG and does not generate any reset or interrupt.

VBATMONEN, Battery brownout enabled

The battery brownout detector is enabled when VBATMONEN is set to '1' and after the settling time $t_{VBATMON\_SETT}$ the battery brownout detector is operational. If the battery brownout detector is disabled by clearing the VBATMONEN bit, then VBATBRNFLAG (VBAT brownout detector flag) and VBATBRNREG (VBAT brownout detector register) can not be used by the application software.

PWRMANLFSTATE, power management field supply states

This bit has different meaning dependent on whether manual pre-switch control is assumed (at least one of the bits PRESW_MODE and PRESW_LF is set) or not.

In the first case this flag shows the state of the weak pre-switch, in the latter one the state of the field selection of the power management after device start-up.

VBATBRNFLAG, VBAT brownout detector flag

The brownout detector at VBAT monitors the supply voltage level continuously only if VBATMONEN is set to '1'. It checks whether VBAT is above or below a certain threshold that is necessary for proper operation of all VBAT supplied parts.

The brownout detector can select one of two different brownout thresholds with bit VBATBRNEXT.

LFFLD, LF field detection

This flag signals the presence of an LF Field by monitoring the rectified LF field supply. If this exceeds the LF field detection threshold voltage $V_{THR,FDLF-VIN}$ LFFLD is set, otherwise it is cleared.

PMODE, Power mode

This flag signals the current state of the main supply switch (battery supply switch).

PWUPIND, Port wake-up indicator

The port wake-up indicator flag indicates that a port wake-up request was detected while the device is powered with field supply. The port wake-up indicator flag is active only if the battery supply switch is turned off (PMODE = 0).

The information is used in the boot routine in order to select the correct supply condition. When the battery switch is turned on, the flag is cleared automatically.

If the application program wants to monitor a port wake-up event in the LF FIELD state it is recommended to check the port interrupt flag rather than the port wake-up indicator flag.

2.2.4.5 Power control register PCON2

The power control register PCON2 accommodates additional power supply state registers plus influences the behavior of the LF active and LF passive mode.

Table 8. Power control register PCON2 (reset value xx00_x000b)

Bit	Symbol	Access	Value	Description
7	VDDBRNREG	R/W		VDD brownout detector register
			0	VDDBRNFLAG is / was not set
			1	VDDBRNFLAG is / was set
6	VDDABRNREG	R/W		VDDA brownout detector register
			0	VDDABRNFLAG is/was not set
			1	VDDABRNFLAG is/was set
5	RDT	R/W0		Reserved for device test
4	VBATBRNINDEN	R/W		Low battery indicator control
			0	Low battery sense disabled
			1	Low battery sense enabled
3	VBATBRNREG	R/W		VBAT brownout detector register
			0	VBATBRNFLAG is / was not set
			1	VBATBRNFLAG is / was set
2	VBATBRNEXT	R/W		Extended battery brownout range
			0	Standard battery brownout falling threshold, $V_{BO,VBAT\_STD}$
			1	Extended battery brownout falling threshold, $V_{BO,VBAT\_EXT}$
1	R2MSDET	R0/W		Reset 2 ms detection
			0	No effect
			1	Dynamic reset of the 2 ms detection
0	LOCKP	R/W		Lock passive mode
			0	Release passive mode lock
			1	Keep analogue frontend in passive (transponder) mode

VDDBRNREG, VDD brownout detector register

The VDD brownout detector register is a registered version of the corresponding brownout detector flag. It is set as soon as VDDBRNFLAG becomes '1' and keeps its state, even if VDDBRNFLAG becomes '0' afterwards.

The bit VDDBRNREG can be set and cleared by the application only if the flag VDDBRNFLAG is '0'.

VDDBRNREG can be used to monitor the supply voltage level at VDD over a long period, e.g. to check whether the supply voltage at VDD was sufficient during EEPROM programming.

VDDABRNREG, VDDA brownout detector register

The VDDA brownout detector register is a registered version of the corresponding brownout detector flag. It is set as soon as VDDABRNFLAG becomes '1' and keeps it state, even if VDDABRNFLAG becomes '0' afterwards. The bit VDDABRNREG can be set and cleared by the application only if the flag VDDABRNFLAG is '0'.

VDDABRNREG can be used to monitor the supply voltage level at VDDA over a long period, e.g. to check whether the supply voltage at VDDA was sufficient during RSSI measurements and ADC conversion in general.

Battery brownout extended range, VBATBRNEXT

The battery brownout extended range allows the brownout threshold for VBAT to be extended from $V_{BO,VBAT\_STD}$ falling to $V_{BO,VBAT\_EXT}$ falling.

VBATBRNINDEN, battery indicator monitor enable register

The battery indicator monitor is enabled when VBATBRNINDEN is set to '1'. This powers the VBAT monitoring circuitry in the analogue and connects a resistive load across the battery (VBAT). Battery monitoring is used to identify battery end of life (approximately 2.4V). The status of the battery indicator monitor can be obtained by reading the bit VBATBRNIND (Weak battery indicator).

VBATBRNREG, VBAT brownout detector register

The VBAT brownout detector register is a registered version of the corresponding brownout detector flag. It is set as soon as VBATBRNFLAG becomes '1' and keeps its state, even if VABTBRNFLAG becomes '0' afterwards.

The bit VBATBRNREG can be set and cleared by the application, only if the flag VBATBRNFLAG is '0'.

VBATBRNREG can be used to monitor the supply voltage level at VBAT over a long period, e.g. to check whether the supply voltage at VBAT was sufficient during a complete ADC conversion.

Reset 2 ms detection, R2MSDET

The application can manually reset the 2 ms ($t_{FLD,HLD}$) detection to avoid unintended activation of the LF passive mode. This feature can be used in LF active mode for example during the RSSI measurement when a constant carrier is required.

If a '1' is written to bit R2MSDET a dynamic reset of the 2 ms detection is triggered. The reset request is synchronized to the correct clock automatically without any further

interaction by the application. Writing a '0' has no effect and reading of bit R2MSDET always yields '0'.

The reset of the 2 ms detection is generated temporarily when a '1' is written to bit R2MSDET and the 2 ms detection starts again immediately thereafter. A static reset is not supported in order to avoid unintentional blocking of the LF passive mode. If a constant carrier is applied in LF active mode for more than 2 ms, the application shall reset the 2 ms detection regularly.

Lock passive mode, LOCKP

This control bit overrides the 2 ms detection circuit and keeps the analogue frontend in passive (transponder) configuration. Long modulation pauses during a passive communication might reset the 2 ms detection unit and disturb the passive protocol. It is strongly recommended to set the bit LOCKP after recognition of a passive protocol (un-modulated field > 2 ms) and to release the bit again after the passive protocol is finished.

2.2.4.6 Power control register PCON5

The power control register PCON5 contains the VDDA brownout flag reset bit.

Table 9. Power control register PCON5 (reset value xxx0_0000b)

Bit	Symbol	Access	Value	Description
7 to 5	RFU	-/W0		Reserved for future use
4	VDDABRNRST	R0/W		VDDA brownout reset control bit
			0	No effects
			1	Clear the VDDA brownout flag
3 to 0	RDT	-/W0		Reserved for device test

VDDABRNRST, VDDA brownout reset bit

Brownout detector flag on VDDA, VDDABRNFLAG, and its registered version, VDDABRNREG, can be cleared by setting VDDABRNRST to 1. After clearing, the detector output will recover and the brownout flag will be valid after $t_{BO,VDDA\_RST}$. Note, both flags that are cleared by the application will remain cleared only if the VDDA is above the falling $V_{BO,VDDA}$ threshold level, otherwise, if VDDA is below $V_{BO,VDDA}$, both flags will be re-asserted, at latest after $t_{BO,VDDA\_RST}$.

2.3 System clock

The clock generation unit provides versatile means to select the clock source and the clock speed for the CPU and the peripheral components.

2.3.1 Clock sources

The NCF215A / NCF215B provides several clock sources based on internal oscillators and external sources, which are summarized in Table 10.

Table 10. Clock sources

Symbol	Description
RCCLK	Clock from 16 MHz main RC oscillator
AUXCLK	Clock from 1 MHz auxiliary RC oscillator

Symbol	Description
LFCLK	Clock from 125 kHz LF field
XO32KCLK	Clock from 32 kHz crystal oscillator
SDADCCLK	SD-ADC clock source from 16 MHz precision RC oscillator
XCLK	External clock at P15

2.3.1.1 RCCLK, clock from 16 MHz main RC oscillator

The 16 MHz main RC oscillator is the main clock source for high speed CPU and peripheral operation. The oscillator starts up when it is activated and can be selected independently of the available core supply state.

The main RC oscillator is activated automatically under the following circumstances:

- RCCLK is selected as the CPU clock source
- RCCLK is required for EROM programming
- RCCLK is selected as the ADC clock source and a conversion is running
- RCCLK is selected as the AES calculation unit clock source and the calculation unit is running
- RCCLK is required for the monitor and debug interface

The application has the possibility to activate the main RC oscillator unconditionally, if the clock is needed for any other reason (e.g. timer 0, timer 1 and timer 2).

2.3.1.2 AUXCLK, clock from 1 MHz auxiliary RC oscillator

The 1 MHz auxiliary RC oscillator is intended for auxiliary tasks and low speed CPU and peripheral operation. The oscillator is used by several peripherals and requires a start-up time $t_{AUXCLK,PON}$.

The auxiliary RC oscillator is always running unless the LF clock is selected. The auxiliary RC oscillator is automatically activated under the following circumstances:

- Read/write access to the ULP EEPROM interface
- Device is powered with the battery (then the clock from the RC oscillator is used to operate the watchdog)
- AUXCLK is required for the monitor and debug interface
- AUXCLK is selected for the AES calculation unit and the calculation unit is running

The application has the possibility to activate the auxiliary RC oscillator unconditionally, if the clock is needed for any other reason (e.g. timer 0, timer 1 and timer 2).

2.3.1.3 LFCLK, clock from 125 kHz LF field

The selection of the 125 kHz clock (LFCLK) is intended for transponder applications with ultra low current consumption, where even the current consumption of the auxiliary RC oscillator shall be avoided.

2.3.1.4 XO32KCLK, clock from 32 kHz crystal oscillator

The clock of the 32 kHz (32768 Hz) crystal oscillator is required for the LF active receiver, the interval timer, the real-time clock, the post-wake-up timer, and the motion sensor interface. The 32 kHz crystal oscillator requires a start-up time t_{XO32K_set}. The supply for the crystal oscillator is derived from the unregulated battery supply VBAT; hence, the clock is available in POWER OFF state, too.

2.3.1.5 SDADCCLK, SD-ADC clock source

SDADCCLK, derived from a 16 MHz precision RC oscillator, is the clock source for the SD-ADC, which is part of the narrowband RSSI block. The precision RC oscillator must be calibrated to the target frequency $f_{OSC,SDADC}$ prior to every use by means of a built-in autocalibration block. This is required to calibrate out initial frequency tolerances and deviations caused by temperature and supply voltage variations. The reference clock for the autocalibration is the 32 kHz crystal oscillator clock, XO32KCLK, and the required calibration time is $t_{SDADCCLK,CAL}$.

2.3.1.6 XCLK, external clock at P15

An external clock XCLK with a frequency of f_{XCLK} can be connected at P15. This clock is intended as external clock source for timer 0, timer 1 and timer 2 as well as for the monitor and debug interface.

P15 port wake-ups and interrupts can be disabled if these events are unwanted when XCLK is driving P15. The bits P15C in the PRESWUP0 register configure the P15 port wake-up. The bit P15INTDIS in the P1INTDIS register configures the P15 port interrupts.

2.3.2 Clock domains

Based on the clock sources, clock domains are derived to provide the clock for the CPU and the peripheral components as depicted in Figure 6.

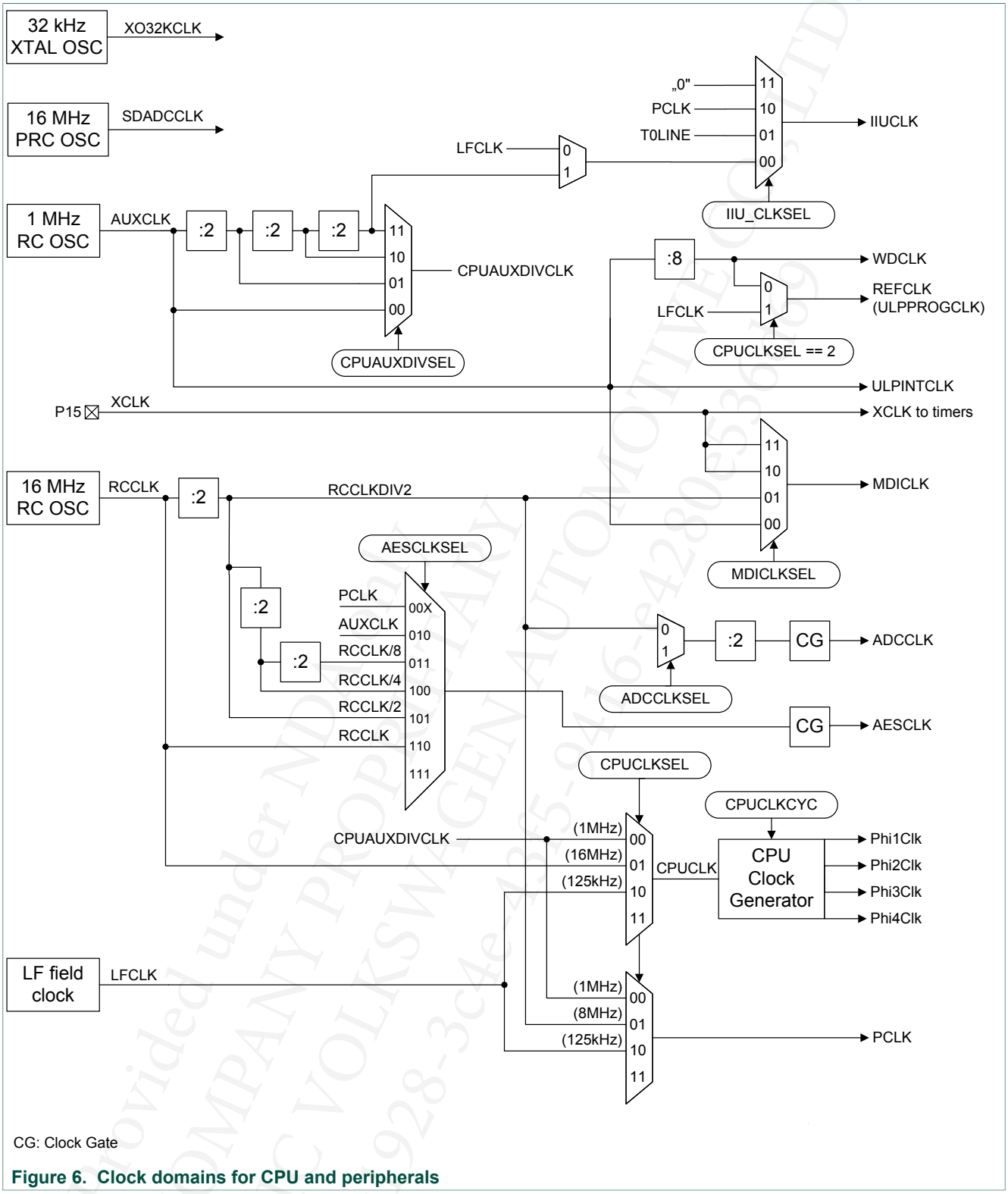


Figure 6. Clock domains for CPU and peripherals

Additional clock domains are provided for timer 0, timer 1 and timer 2, based on two central timer clock multiplexers delivering TMUX0CLK and TMUX1CLK according to Figure 7.

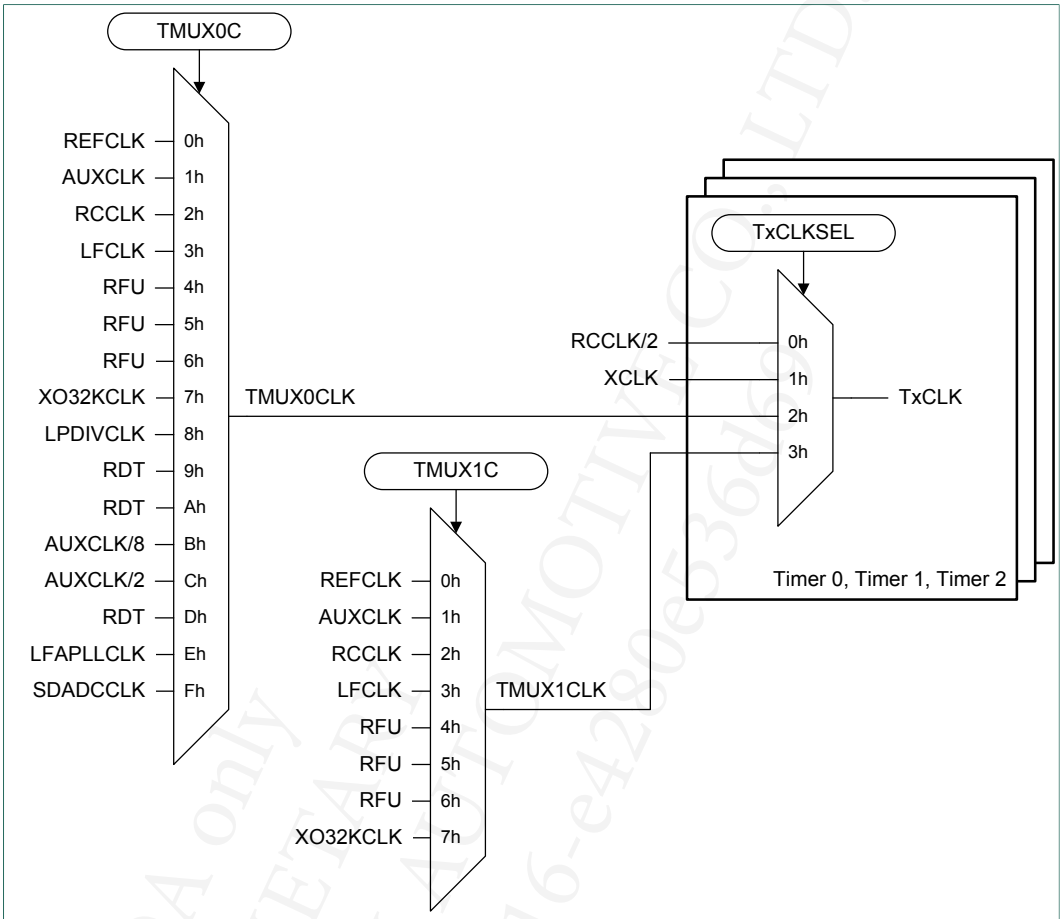


Figure 7. Clock domains for timer 0, timer 1 and timer 2

2.3.2.1 CPUCLK, CPU clock

Three clock sources are selectable for the CPU via system calls, the 16 MHz main RC oscillator RCCLK, the 1 MHz auxiliary RC oscillator AUXCLK, and the clock derived from the LF Field LFCLK. The main and the auxiliary RC clock are always selectable, even for LF field supplied operation.

The CPU clock domain has interfaces to the ROM, RAM, EROM and ULP EEPROM. The clocks for all these modules are generated by a central CPU clock generation unit. The actual execution speed of the CPU is controlled by insertion of additional wait states, dependent on the accessed memories.

Some standard peripherals use the same clock source as the CPU whereas others have only a limited selection of clock sources.

The boot routine always starts using the auxiliary RC clock, CPUAUXDIVCLK. After completion of the boot routine, all other available clock sources can be selected by the application via system calls in order to balance CPU speed and power consumption.

The CPU speed can be chosen dependent on the used clock source. Using the main RC oscillator, the CPU speed can be configured from approximately 485 kHz (16 MHz / 33) to 4 MHz (16 MHz / 4). In high performance mode, a CPU speed of up to 8 MHz is possible when code is executed from the ROM. In this mode, wait states for EROM access and VBATREG supply domain SFR read access are necessary. These wait states are inserted automatically, resulting in an average CPU speed of up to 5.3 MHz

(16 MHz / 3 for 16 bit instructions) when executing code from the EROM and not reading VBATREG supply domain SFRs.

The device supports a ROM/EROM timing compatibility mode in order to allow application code transfer from an EROM version to a ROM coded product version with identical timing behavior even in high performance mode. If the compatibility mode is active in the ROM product version, wait states are inserted at the same positions where they would be inserted in an EROM version. The application program can disable the timing compatibility mode feature in order to get the maximum performance in a ROM version.

By using the auxiliary RC oscillator as clock source, the CPU speed can be set from approximately 3.8 kHz (1 MHz / 264) to 500 kHz (1 MHz / 2).

In case the clock source is derived from the LF field, the CPU speed is selectable between 3.8 kHz (125 kHz / 33) to 62.5 kHz (125 kHz / 2).

2.3.2.2 PCLK, peripheral clock

The PCLK domain is used by peripherals like the SPI interface and the random number generator. These peripherals usually run with the same clock source as the CPU.

2.3.2.3 AESCLK, AES clock

The AES calculation unit operates either with the same source as the CPU, the auxiliary RC oscillator or a (divided) clock of the main RC oscillator.

The faster clock speed can be used to speed up the calculation time for the LF transponder without the necessity to switch to a faster CPU clock. The AES clock period is $T_{REF,AES}$.

2.3.2.4 ADCCLK, ADC clock

The ADC operates on the clock sourced by the main RC Oscillator, RCCLK/2. Note that the actual ADC clock is divided by two after clock source selection, thus actual ADC clock is RCCLK/4, see also Figure 6.

2.3.2.5 WDCLK, watchdog clock

The watchdog uses the clock from the auxiliary RC oscillator independent of the selected CPU clock source. When the watchdog is enabled, the auxiliary RC oscillator is conditionally enabled too.

2.3.2.6 REFCLK, reference clock

The reference clock is a 125 kHz clock source (clock period $T_{REF,LF}$), which is intended for the timers. It is either derived from the auxiliary RC oscillator or from the LF clock.

2.3.2.7 ULPINTCLK, ULP EEPROM interface clock

The clock for the ULP EEPROM interface (read/write access) is derived from the auxiliary RC oscillator independent of the selected CPU clock source.

2.3.2.8 ULPPROGCLK, ULP EEPROM programming clock

The 125 kHz ULP EEPROM programming clock is either derived from the auxiliary RC oscillator or from the LF clock. The correct clock source is always selected automatically, based on the selected CPU clock source.

2.3.2.9 MDICLK, monitor and download interface clock

Clock sources for the monitor and debug interface are the auxiliary RC clock, the main RC clock and the external clock XCLK. The MDI clock is independent of the selected CPU clock source.

2.3.2.10 IIUCLK, immobilizer interface unit clock

Clock sources for the immobilizer interface unit are the LF clock for the immobilizer and the overflow of timer 0 for the modulator operation. The IIU has a local clock selection unit independent of the selected CPU clock source.

2.3.2.11 XCLK, external clock

The external clock XCLK is provided to timers 0, 1 and 2.

2.3.2.12 TMUX0CLK, timer multiplexer 0 clock

The timer multiplexer 0 clock, TMUX0CLK, is provided to timers 0, 1 and 2. The multiplexer concept allows these timers to operate with and to synchronize to several clock sources.

2.3.2.13 TMUX1CLK, timer multiplexer 1 clock

The timer multiplexer 1 clock, TMUX1CLK, is provided to timers 0, 1 and 2. The multiplexer concept allows these timers to operate with and to synchronize to several clock sources.

2.3.3 Registers

The bit IIU_CLKSEL selecting the clock for the immobilizer interface unit is located in register IIUCON0. The bits TxCLKSEL for timers 0, 1 and 2 clock source selection are located in the registers T0CON1, T1CON1 and T2CON1 respectively.

2.3.3.1 Clock control register CLKCON0

The clock control register CLKCON0 selects the CPU clock source and speed.

CLKCON0 is fully accessible in SYSTEM mode only. An application executed in USER mode shall use a system call to change the register.

Table 11. Clock control register CLKCON0 (reset value 00h)

Bit	Symbol	Access SYSTEM mode	Access USER mode	Value	Description
7	RDT	R/W	-/-		Reserved for device test
6 to 5	CPUCLKSEL[1:0]	R/W	R/-		CPU clock source selection
				00	Auxiliary RC oscillator division, CPUAUXDIVCLK, see also CPUAUXDIVSEL in Table 16
				01	Main RC oscillator, RCCLK
				10	Clock from LF field, LFCLK
				11	Reserved for future use
4 to 0	CPUCLKCYC[4:0]	R/W	R/-		See Table 12

CPUCLKSEL[1:0], CPU clock source selection

CPUCLKSEL determines the used clock source for the CPU and the standard peripherals.

CPUCLKCYC[4:0], number of CPUCLK periods per machine cycle

CPUCLKCYC is used to adjust the CPU speed by setting the number of CPU clock periods (T_{CPUCLK}) per command. Normally, one command is executed in CPUCLKCYC + 2 periods of CPUCLK.

In high performance timing mode, CPU wait states are inserted automatically at every command executing an EROM access, independent of whether code or data is accessed, or a VBATREG supply domain SFR read access. The effective number of periods for high performance timing mode is given in Table 12.

Table 12. Effective periods of CPUCLK in case of EROM access or VBATREG supply domain SFR read access

CPUCLKSEL[1:0]	CPUCLKCYC	Effective value of CPUCLKCYC
00	0d … 31d	CPUCLKCYC + 2 (2 … 33)
01	0d … 1d	4
	2d … 31d	CPUCLKCYC + 2 (4 … 33)
10	0d … 31d	CPUCLKCYC + 2 (2 … 33)
11	0d … 1d	4
	2d … 31d	CPUCLKCYC + 2 (4 … 33)

Example: Application with 16 MHz RCCLK and CPUCLKCYC = 0

- The application executes (16 or 32 bit commands) from System ROM. Every command needs 2 T_{CPUCLK}, so the average CPU speed is 8 MHz.
- The application executes code from the EROM. It is assumed that every command is a 32 bit command. Every command shall read 32 bit from the EROM, which needs 4 T_{CPUCLK}. The average speed is 4 MHz.
- The application executes code from the EROM. It is assumed that every command is a 16 bit command. The first command fetches 32 bits from the EROM, which needs 4 T_{CPUCLK}. The second command can execute from the code buffer and, therefore, needs only 2 T_{CPUCLK}. The average speed is 5.3 MHz.

Example: Application with 16 MHz RCCLK and CPUCLKCYC = 2

- The application executes code from the EROM. Since one 32 bit word is read from the EROM per 4 MHz cycle, the instruction rate (for non-branching instructions) is 4 MHz, independent of the command length. Additional read cycles may be inserted in case of branch instructions or interrupts.

Example: Application with 16 MHz RCCLK and CPUCLKCYC = 6

- The instruction rate (for non-branching instructions) is 2 MHz.

2.3.3.2 Clock control register CLKCON1

CLKCON1 selects the clock source for several peripherals and contains the settings for using an external clock.

CLKCON1 is fully accessible in SYSTEM mode only. An application executed in USER mode shall use a system call to change the register.

Table 13. Clock control register CLKCON1 (reset value 00h)

Bit	Symbol	Access SYSTEM mode	Access USER mode	Value	Description
7	RDT	R/W	-/-		Reserved for device test
6	RFU	-/W0	-/-		Reserved for future use
5 to 4	MDICLKSEL[1:0]	R/W	R/-		Monitor and download interface clock selection
				00	1 MHz AUXCLK
				01	8 MHz RCCLK
				10, 11	External clock XCLK
3 to 1	RDT	R/W	-/-		Reserved for device test
0	RER_COMP	R/W	R/-		ROM/EROM timing compatibility mode
				0	Disabled
				1	Enabled

MDICLKSEL[1:0], monitor and download interface clock selection

In general the MDI operates with the clock from the auxiliary RC oscillator. For high speed communication it is possible to switch to 8 MHz of the main RC oscillator.

The setting MDICLKSEL = 1Xb is intended for general applications that want to use a (synchronous) external clock. For example this allows for the parallel initialization of several devices with an external clock.

RER_COMP, ROM/EROM timing compatibility mode

This bit is functional only in the ROM version although for compatibility reasons it is also implemented in the EROM version. It controls the activation of the ROM/EROM timing compatibility mode.

If RER_COMP = ‘0’, any read access to the ROM is accomplished at the maximum possible speed. This setting is provided to benefit from the speed advantage of the ROM version compared to the EROM version.

If RER_COMP is set, any read access to the User ROM area is accomplished with the same timing as if the EROM is present, i.e. the same amount of WAIT CPU clock cycles are inserted as in the EROM version. This setting is provided for 1:1 timing compatibility between EROM and ROM version.

RER_COMP only influences the behavior of the User ROM. This bit does not influence the execution speed of the System ROM.

2.3.3.3 Clock control register CLKCON2

CLKCON2 selects the clock source for the ADC and the AES calculation unit. Control bits for the main RC oscillator and the auxiliary RC oscillator are also included.

Table 14. Clock control register CLKCON2 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	ADCCLKSEL	R/W		ADC clock selection
			0	clock source from the Main RC oscillator, RCCLK/2 further divided by 2 (16 MHz / 4 = 4 MHz)
			1	Reserved for future use
6 to 4	AESCLKSEL[2:0]	R/W		AES calculation unit clock selection
			000	PCLK
			001	Reserved for future use
			010	AUXCLK
			011	Reserved for future use
			100	4 MHz RCCLK
			101	8 MHz RCCLK
			110	16 MHz RCCLK
			111	Reserved for future use
3	RDT	-/W0		Reserved for device test
2	AUXRCOSC_OUTDIS	R/W		Auxiliary RC oscillator clock output disable
			0	Normal operation
			1	Output of auxiliary oscillator is gated to ‘0’ unless it is used as CPU clock source or any automated event requires the auxiliary clock
1	AUXRCOSC_EN	R/W		Auxiliary RC oscillator enable, see also Section 2.3.1.2
			0	Activate oscillator conditionally dependent on selected CPU clock source and peripherals
			1	Activate oscillator unconditionally
0	MRCOSC_EN	R/W		Main RC oscillator enable, see also Section 2.3.1.1
			0	Activate main RC oscillator if used as CPU clock or peripheral clock (PCLK)
			1	Activate main RC oscillator unconditionally

AESCLKSEL[2:0], AES clock selection

In general the clock for the AES calculation unit is derived from the peripheral clock PCLK. If the device is running with a slow clock source (AUXCLK or LFCLK), the available speed of PCLK might not be sufficient. Hence, it is possible to select other clock sources like the main or auxiliary RC clock for the AES calculation unit.

If the RC oscillator is not started up, selecting an RCCLK source for the AESCLK may cause that the RC oscillator does not start up and the AES calculation does not terminate. To prevent such situation, it is recommended to explicitly enable the RCCLK by setting bit MRCOSC_EN to 1 prior to running the AES with RCCLK.

AUXRCOSC_OUTDIS, auxiliary RC oscillator clock output disable

The clock output of the auxiliary oscillator is turned off by setting the bit AUXRCOSC_OUTDIS to '1'. The clock output is gated to '0' in this case. The oscillator

cell itself is not influenced and keeps on running. The value of bit AUXRCOSC_OUTDIS is ignored, if the auxiliary oscillator is used as CPU clock source or if it is activated automatically.

AUXRCOSC_OUTDIS is suitable if the application operates with the clock derived from the LF field but the auxiliary clock is used for certain operations (e.g. ULP EEPROM access). If the start-up time of the auxiliary oscillator is not fast enough the oscillator can stay turned on but the output can be disabled in order to reduce the current consumption when the clock is not needed. An automated event (e.g. ULP EEPROM access) will enable the clock output when required.

AUXRCOSC_EN, Auxiliary RC oscillator enable

Usually the auxiliary RC oscillator is turned off, if the CPU clock is derived from the LF field. If AUXRCOSC_EN is set, the auxiliary RC oscillator is activated independent of the selected clock source for the CPU and the peripherals.

MRCOSC_EN, Main RC oscillator enable

If MRCOSC_EN is set, the main RC oscillator is activated independent of the selected clock source for the CPU and the peripherals.

2.3.3.4 Clock control register CLKCON3

CLKCON3 selects the clock sources for the two central timer clock multiplexers, the output of which can be used as clock source for timer 0, timer 1 and timer 2.

Table 15. Clock control register CLKCON3 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	RFU	-/W0		Reserved for future use
6 to 4	TMUX1C[2:0]	R/W		Timer clock source multiplexer 1 control
			000	REFCLK (nominally 125 kHz)
			001	AUXCLK (nominally 1 MHz)
			010	RCCLK (nominally 16 MHz)
			011	LFCLK (nominally 125 kHz)
			100	Reserved for future use
			101	Reserved for future use
			110	Reserved for future use
			111	XO32KCLK (nominally 32.768 kHz)
3 to 0	TMUX0C[3:0]	R/W		Timer clock source multiplexer 0 control
			0000	REFCLK (nominally 125 kHz)
			0001	AUXCLK (nominally 1 MHz)
			0010	RCCLK (nominally 16 MHz)
			0011	LFCLK (nominally 125 kHz)
			0100	Reserved for future use
			0101	Reserved for future use
			0110	Reserved for future use

Bit	Symbol	Access	Value	Description
			0111	Reserved for future use
			1000	LPDIVCLK (nominally 2 kHz)
			1001	Reserved for device test
			1010	Reserved for device test
			1011	AUXCLK/8 (nominally 125 kHz)
			1100	AUXCLK/2 (nominally 500 kHz)
			1101	Reserved for device test
			1110	LFAPLLCLK (nominally 98.3 kHz)
			1111	SDADCCLK (nominally 16 MHz)

2.3.3.5 Clock control register CLKCON4

CLKCON4 selects the auxiliary RC oscillator division for CPUCLK and PCLK. A clock tree root disable for the AESCLK is also included.

CLKCON4 is fully accessible in SYSTEM mode only. An application executed in USER mode shall use a system call to change the register.

Table 16. Clock control register CLKCON4 (reset value 0000_0x00b)

Bit	Symbol	Access SYSTEM mode	Access USER mode	Value	Description
7 to 3	RFU	-/W0	-/-		Reserved for future use
2	CGAESDIS	R/W	R/-		AESCLK clock tree root disable [1]
				0	AESCLK enabled
				1	AESCLK disabled
1 to 0	CPUAUXDIVSEL[1:0]	R/W	R/-		CPUCLK/PCLK auxiliary RC oscillator division selection
				00	1 MHz AUXCLK
				01	500 kHz AUXCLK/2
				10	250 kHz AUXCLK/4
				11	125 kHz AUXCLK/8

[1] The reset value of CGAESDIS is undefined at the beginning of the EROM application. Please see application note for detailed information.

CGAESDIS, AESCLK clock tree root disable

This bit disables the AESCLK clock tree at its root. This will result in a small power saving even when the AES calculation unit is not being used. This bit must be set to ‘0’ to use the AES calculation unit.

CPUAUXDIVSEL[1:0], CPUCLK/PCLK auxiliary RC oscillator division selection

These bits select the auxiliary RC oscillator division for CPUCLK and PCLK when bits CPUCLKSEL in the CLKCON0 register are set to 0.

2.4 LF Passive interface (Immobilizer)

The contactless passive LF interface provides means to utilize the NCF215A / NCF215B as a contactless transponder, capable to derive its power supply and system clock by inductive coupling to an LF field generated by a corresponding base station. The same LF field is used to receive data from and transmit data to the base station via load modulation under control of the RISC controller. An external LC resonant circuit needs to be connected to the coil inputs (INxP and INxN) of the LF passive interface (Figure 8).

The NCF215A features a 3D contactless transponder. The NCF215B supports transponder communication on one channel only. The required channel 1, 2 or 3 can be configured according to DCFG B, CHAN_SEL[1:0] settings in Table 88.

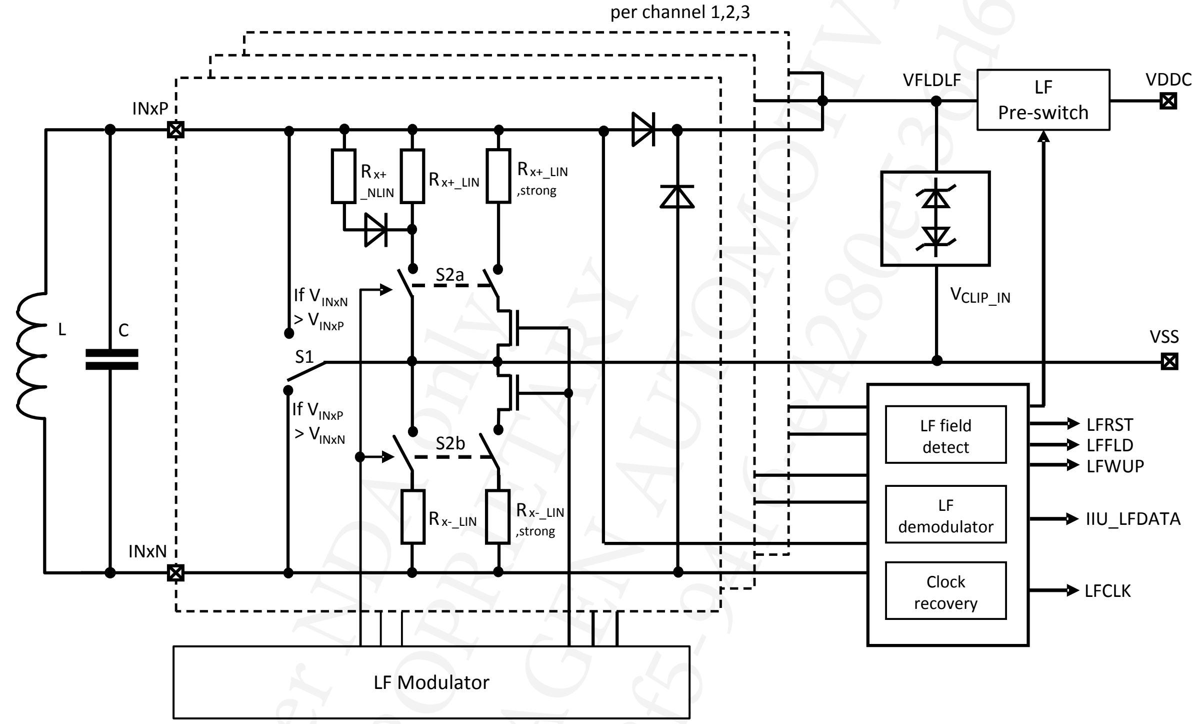


Figure 8. 3D LF passive interface front end circuitry

Independent of the device operating mode, the LF passive interface can detect the presence of an LF field on any channel and providing a corresponding signal to wake-up the device from POWER OFF state, or to interrupt device operation.

The NCF215A / NCF215B features a constant carrier detection before invocation of passive mode (see $t_{FLD,HLD}$ in Figure 3).

2.4.1 Rectifier and limiter

The NCF215A / NCF215B front end features three independent LF rectifier circuits, one per channel. Each rectifier operates in full-bridge configuration, the outputs of the rectifiers are shorted and charge an external capacitor connected to the common pin VDDC. A shunt voltage limiter connected to the output of the rectifiers is provided to ensure that the voltage at pin VDDC does not exceed the specification. The interface input current must not exceed the specified limits.

The LF passive communication with the device employs on-off keying (OOK) of the LF field. The modulation duration and LF field strength shall be chosen such that the rectified supply voltage at VDD stays above the power-on reset threshold V_{POR} during the LF field low condition (see Figure 9).

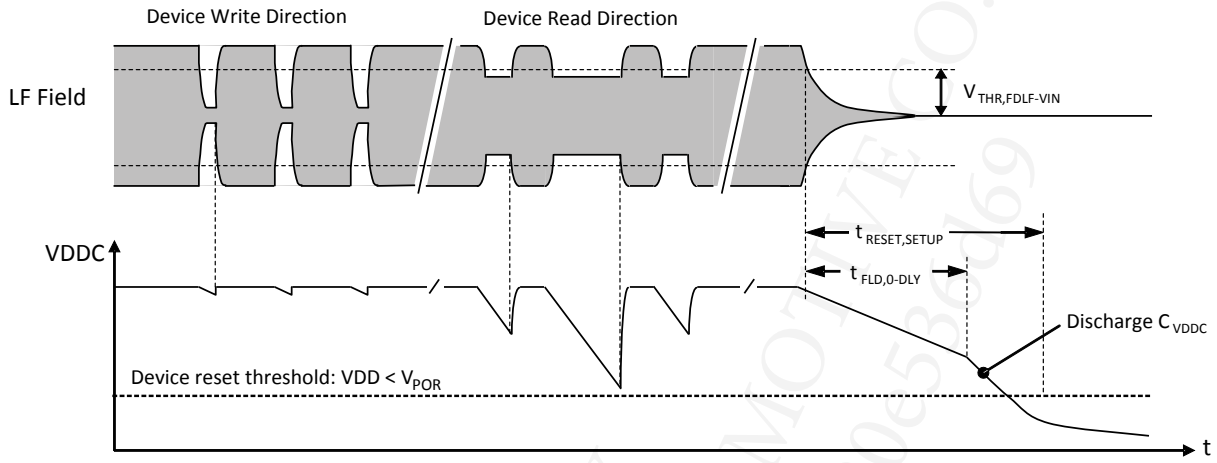


Figure 9. LF field reset timing

2.4.2 Demodulator

The front end features an envelope ASK demodulator able to detect the on-off keying (OOK) signal provided by the base station. The envelope is tracked on all three channels simultaneously and a combined demodulation signal derived from all three channels is provided to the immobilizer interface unit (IIU). The IIU performs serial to parallel conversion of the demodulator output signal, which is then provided to the CPU.

The demodulator circuitry (Figure 10) has been designed to fit the modulation characteristics of the WFS-5d transponder.

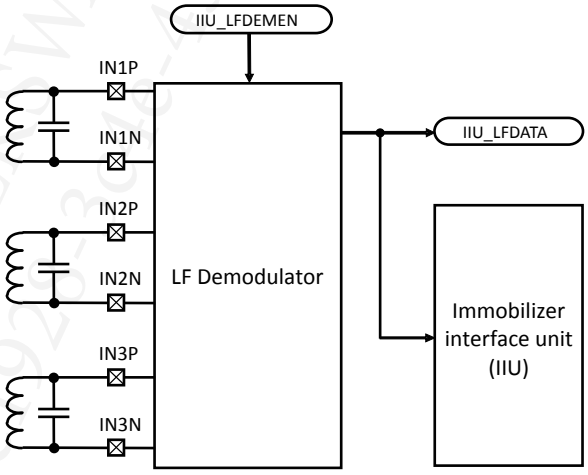


Figure 10. Demodulator Block Diagram

Once enabled, the demodulator tracks the input signal as long as no modulation is detected. The internal demodulator threshold is frozen automatically with the first received modulation and it is released again after the reception of a stop condition. The LF demodulator requires the settling time t_{ADLY} (Figure 11).

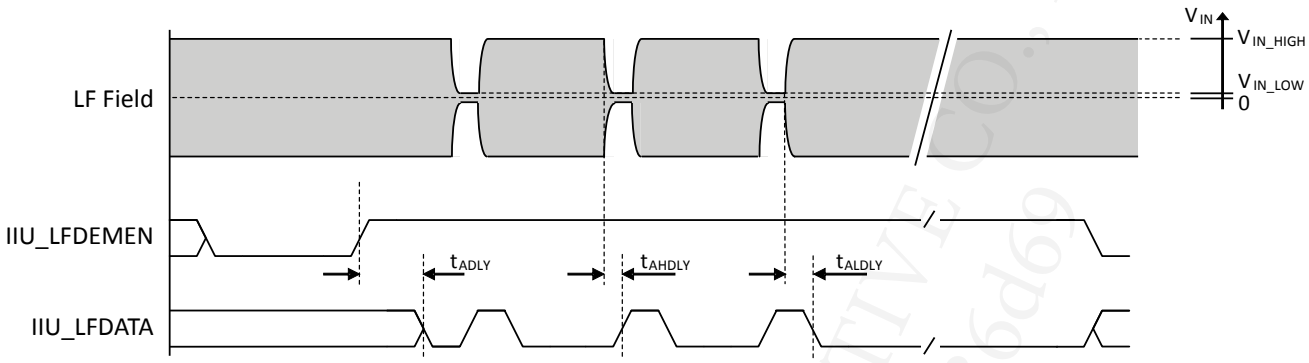


Figure 11. Demodulator Timing

The demodulator sensitivity applicable in write direction is illustrated in Figure 12 requiring a modulation index MI_{WR_LF} according to Equation 1.

$$MI_{WR\_LF} = \frac{V_{IN\_HIGH} - V_{IN\_LOW}}{V_{IN\_HIGH} + V_{IN\_LOW}} \quad (1)$$

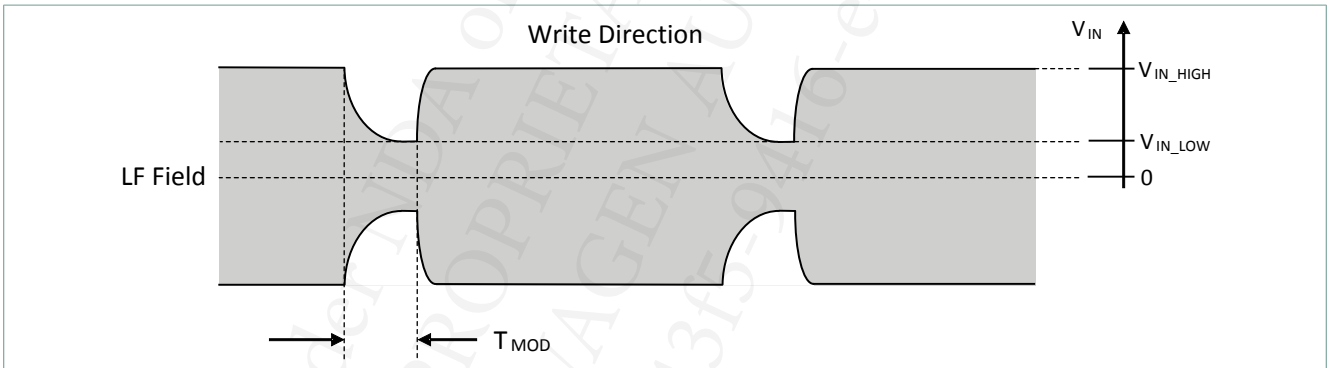


Figure 12. Demodulator Specification

The demodulator shall be disabled during an LF Field modulation phase.

2.4.3 Field detection

Independent of the device operating mode, the LF passive interface can detect the presence of an LF field on any channel and providing a corresponding signal to wake-up the device from POWER OFF state, or to interrupt device operation (see Figure 13).

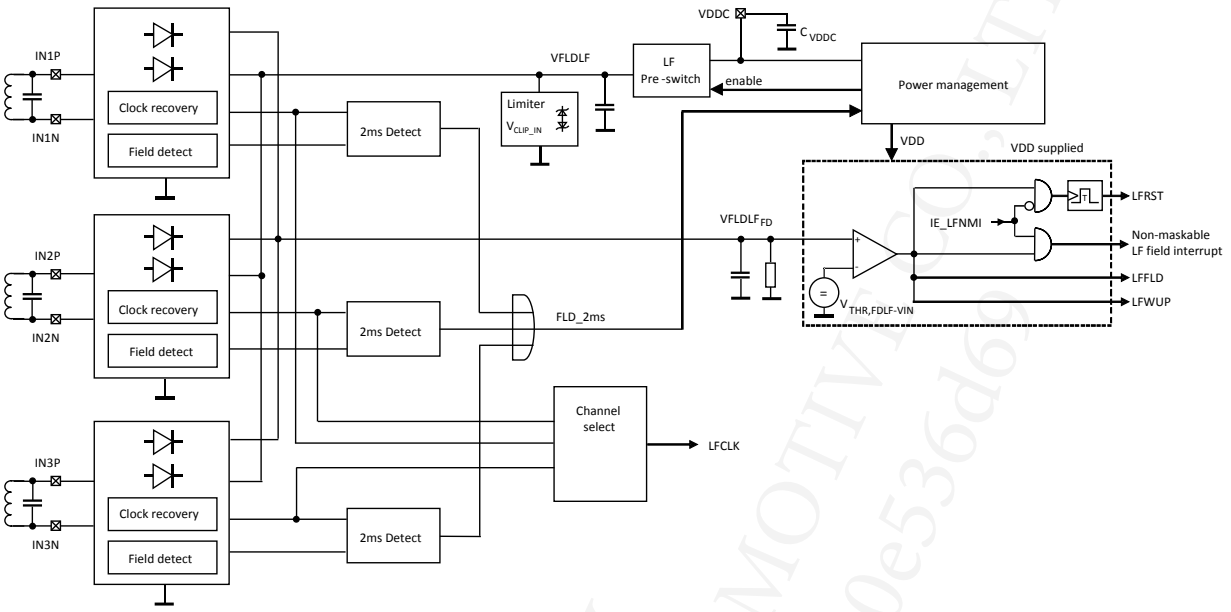


Figure 13. LF field detection circuitry

After a constant carrier is detected for the time $t_{FLD,HLD}$ at any channel, the LF pre-switch between VFLDLF and VDDC is closed and the field detection circuitry gets activated. It features an independent envelope detector that senses the voltage $VFLDLF_{FD}$ across the coil inputs (pins INxP and INxN) followed by a comparator. The LF field envelope is compared with a certain threshold, which is greater than the power-on reset threshold V_{POR}, forming the field detect flag (LFFLD). LFFLD turns high when the LF field on at least one channel exceeds the field detection threshold ($V_{THR,FDLF-VIN}$). LFFLD may be tested by the RISC controller when desired.

The output signal of the field detection circuit can be configured as reset or interrupt source (non-maskable interrupt).

In case the non-maskable interrupt is selected and considered operating from battery supply (BATTERY state) it is up to the application whether to force an LF field supply condition (LF FIELD state) or not. However, LFFLD being set is no guarantee that the available LF field is sufficient to power the device. A device power-on reset (VDDPOR) may occur in case of a weak LF field, which needs to be taken into account once the LF field supply condition is forced.

LFFLD goes low, if the input voltage on all three channels is below the field detect threshold $V_{THR,FDLF-VIN}$ for at least $t_{FLD,0-DLY}$ (see Figure 9). This triggers an active discharge of the capacitor connected to VDDC and consequently the device performs a power-on reset (VDDPOR) as soon as VDD falls below the power-on reset threshold V_{POR}. The base station can enforce a power-on reset (VDDPOR) of the device, if the applied LF field is below $V_{THR,FDLF-VIN}$ for the time $t_{RESET,SETUP}$.

2.4.4 Detection of 2 ms constant carrier

In order to activate the immobilizer, a constant carrier has to be applied to the LF input pins for 256 LF clock cycles ($t_{FLD,HLD}$). The LF field voltage has to exceed the 'active' field detection threshold $V_{THR,FD\_ATIC-VIN}$. After valid 256 LF clock cycles detection, the

LF pre-switch is activated, the constant carrier detection is deactivated and the device commences with the immobilizer.

The demodulator is active during the constant carrier detection phase. If an ASK modulation is detected, the constant carrier detection is reset and starts over again. This mechanism ensures that the immobilizer is not activated during an LF active protocol.

2.4.5 Clock recovery

Every LF input channel has its own clock recovery. The channel selection block (see Figure 13) selects one channel with sufficient signal strength to drive the channel's clock recovery and forwards this clock as LFCLK to the rest of the system.

The NCF215B takes the clock always from the preconfigured channel.

2.4.6 Modulator (load modulation transponder)

The LF passive interface utilizes load modulation (absorption modulation) of the LF Field on all three channels simultaneously to send data to the base station. The modulation timing is determined by the RISC controller.

The NCF215B supports load modulation on the preconfigured channel only.

Load modulation is accomplished by applying an additional load (S2 closed, see Figure 8) across the coil inputs. The LF field modulator contains a standard modulator and a strong modulator. If the standard modulator is selected, the high ohmic path (R_{x+_LIN}, R_{x+_NLIN} and R_{x-_LIN}) is turned on (weak modulation), while selecting the strong modulator, both the low-ohmic path ($R_{x+\_LIN,strong}$ and $R_{x-\_LIN,strong}$) and the high ohmic path are enabled (strong modulation).

Besides the modulation load impedance, the load modulation characteristics depend on the source impedance of the external resonance circuit, the voltage limiter and the internal power consumption of the device. The applied load (S2) is different for each of the two half waves of the carrier to support clock recovery. The resistors R_x and the switches S1, S2 are implemented for each channel.

2.4.7 Immobilizer interface unit (IIU)

The immobilizer interface unit (IIU) allows convenient buffered read and write access to the immobilizer LF demodulator and LF modulator. With its various data path selection capabilities the IIU minimizes the CPU load for most power efficient immobilizer implementations.

The IIU allows an autonomous bit handling for transmission/reception/shifting of 1 to 8 bit. The HT calculation unit is not supported and must be bypassed. The controlling of the data transfer is supported by the generation of an interrupt or wake-up event (see Figure 14).

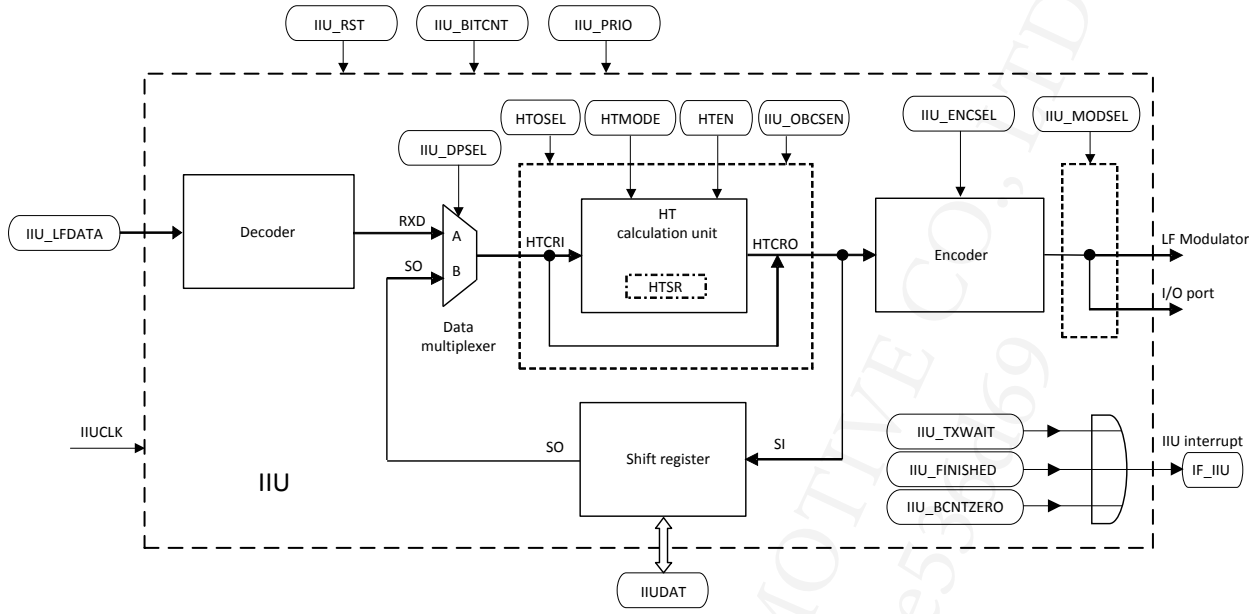


Figure 14. IIU block diagram

Several IIU clock sources can be selected. For WFS-5d compatible timing either the LFCLK or a 125 kHz clock source shall be selected.

With the help of an integrated timer, the time base for the LF demodulator (zero bit, one bit, stop bit) is controlled. The timer is also responsible to generate the LF modulator baudrate and to control the timing between data reception and transmission ($t_{WAIT,TR}$).

The encoded IIU output signal can be selected to modulate the LF field or to be directed to a port pin for general purpose use.

2.4.7.1 IIU decoder and encoder

For data reception the IIU applies binary pulse length modulation (BPLM) decoding (Figure 15) and converts the decoded bits via the 8 bit shift-register into byte format.

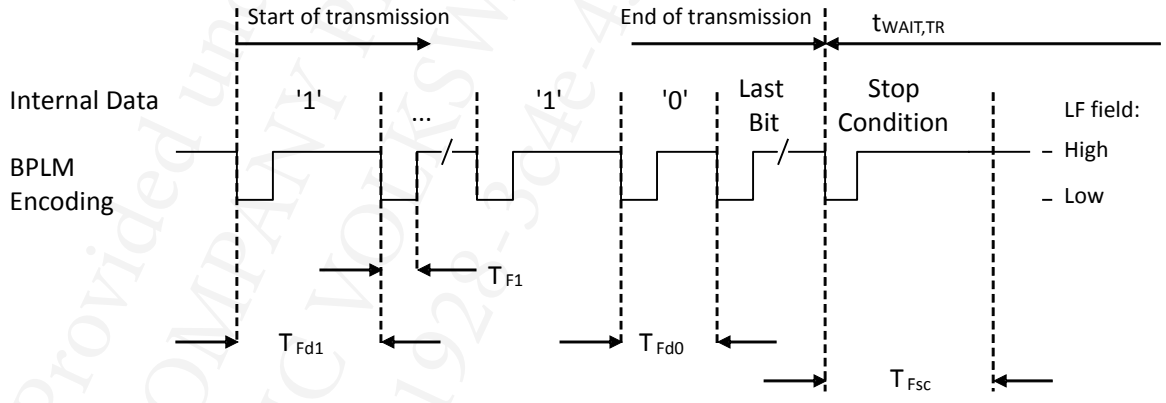


Figure 15. Data encoding - base station to NCF215A / NCF215B

For data transmission the IIU converts the bytes via the shift register into a bit stream and applies Manchester, CDP or NRZ encoding. Load modulation typically employs Manchester or CDP encoding (see Figure 16).

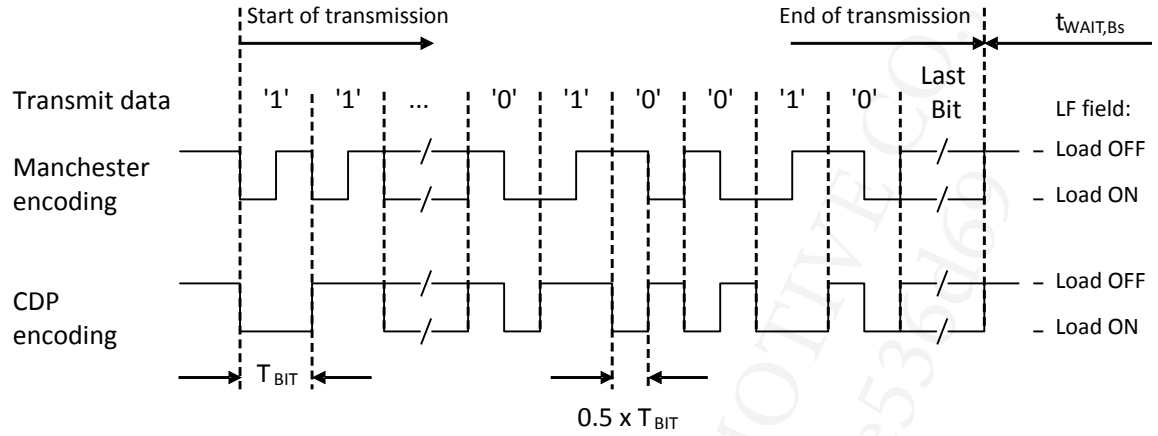


Figure 16. Data encoding load modulation transponder - NCF215A / NCF215B to base station

2.4.7.2 IIU general purpose mode

If not occupied by the immobilizer application, the IIU can be used for general purpose applications like implementation of a custom LF protocol. The shift register allows flexible control of transmitted data between 1 and 8 bits. Manchester, CDP, and NRZ encoding run with the same data rate T_{BIT}. This allows for convenient four state Manchester generation (Manchester zero and one generated with Manchester encoding, Manchester mark and space generated with NRZ encoding) with a constant data rate.

Access to the demodulated data line is given via the dedicated register bit IIU_LFDATA. The timer capture function can be used for demodulation. Besides the LF field clock and the peripheral clock a general purpose timer can be used for baudrate generation.

In order to implement variable transponder wait times $t_{WAIT,TR}$, transmission can be started on user request.

2.4.7.3 IIU states

The IIU state diagram is shown in Figure 17. The states RXWAIT, RXFIRST, RXDATA, TXWAIT and TXDATA are used in LF transponder mode, while the states SHIFT and SHIFTCONT are intended for general purpose applications.

The CPU can control the IIU states by reading from and writing to the state register IIUSTATE. The application has to select any state except IDLE to initiate an automated action. Every action can be interrupted by switching back to IDLE state.

Direct state changes from transponder mode states to general purpose application states and vice versa should be avoided. Instead, IDLE mode shall be selected before such a state change is executed.

IDLE state

In IDLE state all IIU modules are disabled and the IIU clock is turned off. The IIU leaves the IDLE state only if the CPU selects a new IIU state by updating the state register.

RXWAIT

Switching to RXWAIT state initiates the transponder mode. In RX WAIT state the IIU waits for a first rising edge of the demodulated LF data.

RXFIRST and RXDATA

In transponder mode, the IIU is receiving data in RXFIRST and RXDATA states. The decoder is enabled automatically and can be disabled in case custom protocol / general purpose modulation will be implemented.

The RXFIRST state is only used for the first bit received and only if clear text one bit command support is enabled (bit IIU_OBCSEN is set to ‘1’ in register IIUCON2).

The IIU switches to TXWAIT state when a stop condition is received. In this case, a TXWAIT interrupt is generated.

In case the bit counter becomes 0 but no stop condition is received, the IIU switches back to IDLE state as soon as a new rising edge of the demodulated LF data is detected. This indicates that more bits were received than it was expected by the application.

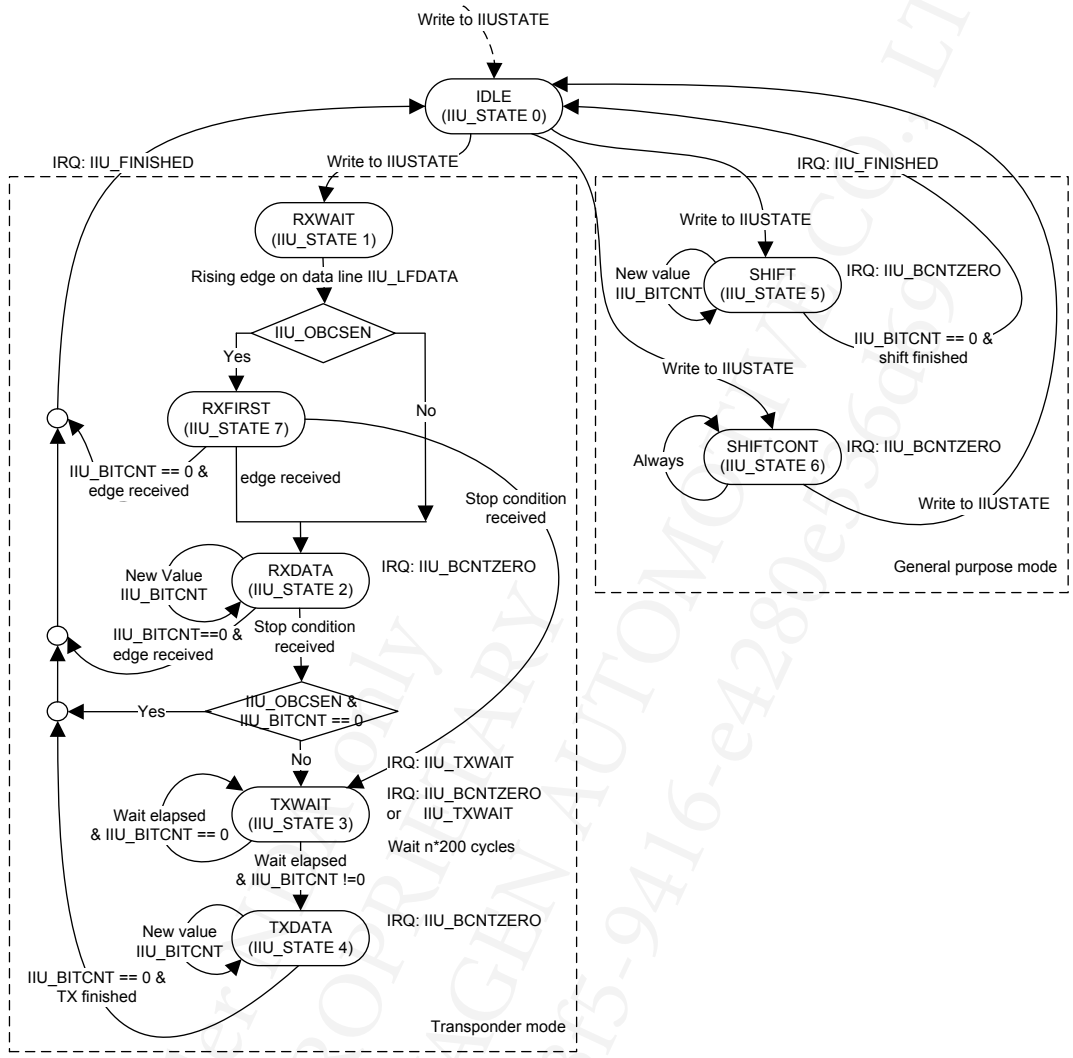


Figure 17. IIU state diagram

TXWAIT

The TXWAIT state is used for implementing the wait time according to the WFS-5d transponder protocol before switching to transmission mode. The wait time is a multiple of 800 cycles and derived from the period counter. Every time the wait time elapses and the IIU does not switch to TXDATA state, the CPU receives an IF_IIU interrupt request (flag IIU_TXWAIT set).

TXDATA

In transponder mode, the IIU is transmitting data in TXDATA state (depending on the settings for encoder and modulator selection). The encoder is enabled automatically.

The CPU receives an IF_IIU interrupt request (flag IIU_BCNTZERO set) when the bit counter becomes zero. If the application does not load new data and a new bit counter

value before the transmission of the current bit has finished, the IIU switches back to IDLE state and signals the end of transmission at the same time with an IF_IIU interrupt request (flag IIU_FINISHED set).

SHIFT and SHIFTCONT state

Both states SHIFT and SHIFTCONT are used for general purpose modulation tasks and for stand-alone usage of the HT calculation unit. In both states the following blocks are enabled automatically:

- shift register
- bit counter
- encoder (enabling depends on IIU_ENCSEL)
- HT calculation unit (enabling depends on HTEN)

When the bit counter reaches the value 0, an IF_IIU interrupt request (flag IIU_BCNTZERO set) is generated. In this case, in SHIFT state the IIU switches back to IDLE state, while in SHIFTCONT state the IIU keeps the state until the CPU changes the state setting.

The SHIFT state is convenient when the HT calculation unit is operated in stand-alone mode or the last byte of a general purpose modulation is processed. The SHIFTCONT state is helpful when implementing general purpose modulation and the CPU requires some time after processing to load new data.

2.4.7.4 IIU wake-up

The IIU provides a signal to wake-up or interrupt the application. Hence, the CPU can enter IDLE mode while the IIU operates autonomously until the desired operation has been finished.

The wake-up or interrupt signal is generated in three cases:

- Bit counter zero: the required number of bits was received / transmitted / shifted.
- Enter/keep TXWAIT state: a stop condition was recognized and the IIU advances to TXWAIT state or the 200 cycle wait time has elapsed without switching to TXDATA state.
- IIU operation finished: the automated IIU operation has been finished and the state machine enters IDLE state automatically.

2.4.8 Registers

2.4.8.1 IIU data register IIUDAT

The IIU data register provides access to the 8 bit shift register, which gives byte-wise access (Table 17) to the received and transmitted data as well as to the HT calculation unit.

While accessing IIUDAT by the CPU it has to be ensured that the register content is stable, otherwise the data may be invalid. IIUDAT is not buffered. Every read or write access is directly accomplished to the internal shift register.

Table 17. IIU data register IIUDAT (reset value xxh)

Bit	Symbol	Access	Value	Description
7 to 0	IIUDATA[7:0]	R/W		Rx/Tx Buffer

Typically during transmission, the MSB (bit 7) of the shift register is shifted out first. In case the number of bits to be transmitted is less than 8, the data bits should be aligned to bit 7. In case of reception of data consisting of less than 8 bits, the LSB is aligned to bit 0 (Table 18). The transmission bit order can be changed to LSB first by setting bit IIU_LSBF to ‘1’ in register IIUCON2.

Table 18. IIU data transfer examples with 3 bits, alignment of transmit and receive data

Transfer bit order	Transfer direction	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MSB first (IIU_LSBF = ‘0’)	Transmit data	T2 (1st)	T1	T0	X	X	X	X	X
	Receive data	X	X	X	X	X	R2 (1st)	R1	R0
LSB first (IIU_LSBF = ‘1’)	Transmit data	X	X	X	X	X	T2	T1	T0 (1st)
	Receive data	R2	R1	R0 (1st)	X	X	X	X	X

2.4.8.2 IIU control register IIUCON0

The IIU Control Register IIUCON0 provides bits to control the selection of data transfer order, modulator, data out and clock. Please note that CPU and IIU shall use the same clock source and IIU clock selection must be set accordingly.

Table 19. IIU control register IIUCON0 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	RFU	-/W0		Reserved for future use
6 to 5	IIU_MODSEL[1:0]	R/W		IIU modulator selection
			00	Port pins Inactive output level: 0
			01	Port pins Inactive output level: 1
			10	Port pins + standard LF load modulator (high-ohmic) Inactive output level: 0
			11	Port pins + strong LF load modulator (high-ohmic + low-ohmic) Inactive output level: 0
4 to 2	IIU_DPSEL[2:0]	R/W		IIU data path selection
			000	RXD (received data)
			001	RXD inverted
			010	SO (shift register serial output)
			011	SO inverted
			100	RXD XOR SO
			101	RXD XNOR SO
			110	Reserved for future use
			111	Reserved for future use
1 to 0	IIU_CLKSEL[1:0]	R/W		IIU clock selection
			00	LFCLK
			01	Timer 0 overflow
			10	Peripheral clock (PCLK)

Bit	Symbol	Access	Value	Description
			11	No clock

IIU_MODSEL[1:0], IIU modulator selection

The encoded data stream can be provided to the LF field load modulator or to a dedicated port pin.

In case the signal is provided to the LF-field load modulator, the LF field can be modulated by switching on/off additional load in the analog front-end. The LF field load modulator contains a standard modulator and a strong modulator. If the standard modulator is selected, the high ohmic path is turned on (weak modulation), while selecting the strong modulator, both the low-ohmic path and the high ohmic path are enabled (strong modulation). If the strong modulator is selected, the low-ohmic path is turned on with a delay of 1 clock cycle to ensure seamless operation of the LF clock recovery.

Selecting the LF load modulator, the inactive IIU output level at the end of the encoding is set to 0, independent whether a port pin is selected additionally or not. In case the signal is provided only to a port pin, the inactive IIU output level can be chosen. The inactive IIU level is also used in IIU IDLE mode or in case the encoder is disabled (IIU_ENCSEL = 00b).

Writing IIU_MODSEL changes the inactive IIU output level immediately unless the IIU is running. The application shall not modify these bits if the IIU is running to avoid any unintentional behavior.

IIU_DPSEL[2:0], IIU data path selection

The IIU data path can be configured to have different input sources for the shift register:

- Received data bit RXD (plain or inverted)
- Shift register output SO (plain or inverted)
- RXD xor SO
- RXD inverted xor SO

IIU_CLKSEL[1:0], IIU clock select

Different clock sources can be selected by IIU_CLKSEL to be used for the shift register / encoder / bit counter. Using Timer 0 overflow supports flexible baud rate generation for custom protocol implementations.

The application shall change the setting of IIU_CLKSEL only, if the IIU is in IDLE state (IIU_STATE[2:0] = 000b). A change of IIU_CLKSEL or CTAUXCLKSEL when the IIU is running can cause unpredictable behavior.

2.4.8.3 IIU control register IIUCON1

The IIU Control Register IIUCON1 provides bits for immediate execution and for the number of bits to be send or received.

Table 20. IIU control register IIUCON1 (reset value 0xh)

Bit	Symbol	Access	Value	Description
7	IIU_PRIO	R/W		Priority for immediate execution
			0	No bit processing during TXWAIT

Bit	Symbol	Access	Value	Description
			1	Immediate bit processing during TXWAIT
6 to 4	RFU	-/W0		Reserved for future use
3 to 0	IIU_BITCNT[3:0]	R/W		Number of bits to be received/transmitted/shifted
			0000	Read access: 0 bit Write access: Invalid
			0001	1 bit
			0010	2 bits
			0011	3 bits
			0100	4 bits
			0101	5 bits
			0110	6 bits
			0111	7 bits
			1000	8 bits
			1001 - 1111	Invalid

IIU_PRIO, IIU priority for immediate execution

IIU_PRIO has only effect in TXWAIT state. With IIU_PRIO it can be specified whether the value written to IIU_BITCNT[3:0] shall be processed immediately or not.

Setting IIU_PRIO to '0' corresponds to "normal" operation, hence in TXWAIT state the shift register and HT calculation unit is not clocked and no shift or load operation is performed.

Setting IIU_PRIO to '1' performs the shift or load operation immediately. In this case, the bit counter content will not be interpreted as state exit condition, but will be used to process immediately the number of specified shifting steps written to the counter. This feature enables the application to use the shift register and/or HT calculation unit in TXWAIT state and is useful e.g. when the HT calculation unit needs to be pre-loaded with a value before the TXDATA state is entered.

The IIU and CPU shall use the same clock source and the same clock speed when setting IIU_PRIO.

IIU_BITCNT[3:0], IIU number of bits received/transmitted/shifted

IIU_BITCNT[3:0] provides access to the IIU bit counter. The value written to the register corresponds to the number of bits to be received/transmitted/shifted. The bit counter counts downwards from the written value to 0. Writing '8' to IIU_BITCNT causes to receive/transmit/shift 8 bits. Once 0 is reached, an IF_IIU interrupt request (flag IIU_BCNTZERO set) is generated.

It has to be considered that the register content can be unstable if IIU_BITCNT is accessed when the IIU is processing data. Hence, the application shall check the flag IBCNTZERO rather than the content of IIU_BITCNT to determine the status of the bit counter.

2.4.8.4 IIU control register IIUCON2

The IIU Control Register IIUCON2 provides a bit to enable clear text one bit command support.

Table 21. IIU control register IIUCON2 (reset value 00h)

Bit	Symbol	Access	Value	Description
7 to 2	RFU	-/W0		Reserved for future use
1	IIU_LSBF	R/W		IIU data transfer order
			0	MSB first
			1	LSB first
0	IIU_OBCSEN	R/W		Enable clear text one bit command support
			0	All received data passes through the normal data path
			1	Received data consisting of a single bit is passed directly from the data path selection multiplexor output to the data shift register input without passing through, or shifting, the HT calculation unit.

IIU_OBCSEN, enable clear text one bit command support

IIU_OBCSEN provides a means of bypassing the HT calculation unit for received data that consists of a single bit. When IIU_OBCSEN is set to ‘1’, one bit received data is passed directly from the data path selection multiplexor output to the data shift register input without passing through, or shifting, the HT calculation unit. If the HT calculation unit is disabled (HTEN set to ‘0’ in HTCON), IIU_OBCSEN has no effect on the IIUDATA.

An example application for this data path mode is in the HT2-E and HT3 transponder protocols where the one bit commands, REFRESH and SOFT_RESET, are always sent in clear text (information that is not encrypted) whereas the multi-bit commands may be in cipher text (information that is encrypted).

2.4.8.5 IIU status register IIUSTAT

The status of the IIU can be monitored via the IIU Status Register.

Table 22. IIU status register IIUSTAT (reset value 00h)

Bit	Symbol	Access	Value	Description
7	IIU_LFDATA	R/-		LF data
			0	LF field unmodulated
			1	LF field LOW modulation
6	IIU_LFDEMEN	R/W		Analog LF demodulator enable
			0	Disable
			1	Enable
5	IIU_RST	R0/W		IIU reset
			0	No effect
			1	Execute reset
4 to 3	IIU_ENCSEL[1:0]	R/W		IIU encoding selection

Bit	Symbol	Access	Value	Description
			00	Disable encoder
			01	NRZ encoding
			10	Manchester encoding
			11	CDP encoding
2	IIU_TXWAIT	R/W1->0		IIU TXWAIT interrupt flag
			0	No interrupt request
			1	Interrupt request
1	IIU_FINISHED	R/W1->0		IIU finished interrupt flag
			0	No interrupt request
			1	Interrupt request
0	IIU_BCNTZERO	R/W1->0		IIU bit counter zero interrupt flag
			0	No interrupt request
			1	Interrupt request

IIU_LFDATA, LF data

IIU_LFDATA allows direct read access to the demodulated data signal coming from the analog LF demodulator.

The analog LF demodulator senses the differential voltage across the coil inputs (pin IN1P and IN1N). When the demodulator detects a LF field LOW modulation, IIU_LFDATA is set, otherwise cleared. While the LF demodulator is disabled, IIU_LFDATA yields a one.

IIU_LFDEMEN, analog LF demodulator enable

IIU_LFDEMEN enables or disables the analog LF demodulator.

After activation the signal IIU_LFDATA is undefined until the LF demodulator settling time $t_{LFDSETUP}$ is elapsed. The application shall reset the LF decoder with bit IRST thereafter to clear any latched spurious event at IIU_LFDATA, which might occur during start-up of the LF demodulator.

IIU_RST, IIU reset

The reset bit IIU_RST can be used to generate an asynchronous reset of the IIU comprising the state machine, the LF decoder with the internal counters, the IIU output signal and the interrupt request flags.

Launching a reset when the IIU is running causes an immediate stop. The IIU enters IDLE state and the IIU output switches to the specified inactive level.

The bit counter value IIU_BITCNT is not influenced by the reset operation as a new value for IIU_BITCNT shall be written anyway in order to start a subsequent operation.

IIU_ENCSEL[1:0], IIU encoding selection

The data encoder can be configured to operate in different encoding modes.

IIU_TXWAIT, IIU TX wait interrupt flag

The IIU_TXWAIT interrupt flag is set under the following two conditions:

- The IIU changes from RXFIRST or RXDATA to TXWAIT state since an LF stop condition is detected
- The IIU stays in TXWAIT state after the TX wait period (200 cycles) has elapsed and the exit condition is not true

IIU_TXWAIT can be cleared either manually by writing a '1' or automatically by writing to register IIU_BITCNT. Manual setting of IIU_TXWAIT is not supported. Writing a zero has no effect and does not alter the stored value.

IIU_FINISHED, IIU finished interrupt flag

The IIU_FINISHED interrupt flag is set if the IIU operation is finished and IDLE state is entered, which occurs under the following two conditions.

- Unexpected end of receive: The IIU is in RXFIRST or RXDATA state, the bit counter IIU_BITCNT is equal to 0 and a LF LOW modulation is again received (stop condition not met).
- End of transmission/shift operation: The bit counter IIU_BITCNT is equal to 0 and the last bit was transmitted (state TXDATA) or shifted (state SHIFT) completely

IIU_FINISHED can be cleared either manually by writing a '1' or automatically by writing to register IIU_BITCNT. Manual setting of IIU_FINISHED is not supported. Writing a zero has no effect and does not alter the stored value.

IIU_BCNTZERO, IIU bit counter zero interrupt flag

The IIU_BCNTZERO interrupt flag indicates that the bit counter has reached the value 0, hence the instructed number of bits was received/transmitted/shifted.

IIU_BCNTZERO can be cleared either manually by writing a '1' or automatically by writing to register IIU_BITCNT. Manual setting of IIU_BCNTZERO is not supported. Writing a zero has no effect and does not alter the stored value.

2.4.8.6 IIU state register IIUSTATE

The IIU state can be monitored and controlled via the IIU state register IIUSTATE. Reading IIUSTATE reflects the actual IIU state, while a value written to IIUSTATE has an immediate effect on the IIU state.

Table 23. IIU state register IIUSTATE (reset value 00h)

Bit	Symbol	Access	Value	Description
7 to 3	RFU	-/W0		Reserved for future use
2 to 0	IIU_STATE[2:0]	R/W		IIU state
			000	IDLE
			001	RXWAIT
			010	RXDATA
			011	TXWAIT
			100	TXDATA
			101	SHIFT

Bit	Symbol	Access	Value	Description
			110	SHIFTCONT
			111	RXFIRST

2.4.8.7 IIU 3D channel control register, I3DCON

The functions described in this section are available for NCF215A in case of a non-proprietary transponder emulation by a user EROM application. In case of the built-in proprietary transponder emulation, the I3DCON functions are used seamlessly. For NCF215B, this register is preconfigured by the boot routine and any write access has no effects.

The I3DCON provides byte entry to the LF channel configuration.

Table 24. IIU 3D channel control, I3DCON (reset value x0xx0xxxb)

Bit	Symbol	Access	Value	Description
7	3DIMMODIS	R/W		Disable 3D immobilizer
			0	No effects
			1	3D interface disabled
6	RFU	-/W0		Reserved for future use
5 to 4	LFCLKSEL[1:0]	R/W		Channel selection control
			00	Reserved for future use
			01	Channel 1 selected
			10	Channel 2 selected
			11	Channel 3 selected
3	LFCLKAUTOSEL	R0/W		Channel auto-selection enable
			0	No effects, channel selected by LFCLKSEL[1:0]
			1	Channel selected by hardware
2	LF3FD	R/-		LF field detection flag (FDATIC), channel 3
			0	No field detected
			1	Field detected
1	LF2FD	R/-		LF field detection flag (FDATIC), channel 2
			0	No field detected
			1	Field detected
0	LF1FD	R/-		LF field detection flag (FDATIC), channel 1
			0	No field detected
			1	Field detected

3DIMMODIS, 3D functionality disable bit

For NCF215A, the default value of 3DIMMODIS after the boot routine is 0 indicating the 3D configuration.

3DIMMODIS set 1 configures LF IMMO front-end into the 1D-mode. When 3DIMMODIS set to 0, all three channel clock recovery circuits are powered up. In this case, channel

selection is following the LFCLKSEL[1:0] and the LFCLKAUTOSEL bit settings configuration.

For NCF215B, the bit 3DIMMODIS is ignored as the 1D configuration is always selected.

LFCLKSEL[1:0], Channel selection settings bits

For NCF215A, the LFCLKSEL[1:0] settings are fully controlled by the built-in transponder emulation. A non-proprietary transponder emulation from EROM is able to select arbitrary channel for clock recovery. However, a random change to LFCLKSEL[1:0] by an application may cause the LFCLK clock from the actually selected channel to be lost if the LF field on that channel is below the clock-detection threshold.

LFCLKAUTOSEL, Automatic channel selection bit

Similar to LFCLKSEL[1:0], the LFCLKAUTOSEL bit can only have effects when 3DIMMODIS is set to 0. LFCLKAUTOSEL is fully controlled by the built-in transponder emulation. When set to 0, LFCLKAUTOSEL will give preference to the LFCLKSEL[1:0] settings to select clock recovery. When LFCLKAUTOSEL bit set to 1, the clock recovery channel will automatically be selected by device-hardware, i.e. the LFCLKSEL[1:0] settings will be overwritten by hardware.

LF1FD, LF2FD and LF3FD, Channel 1, 2 and 3 - LF field detection flags

The LF1FD, LF2FD and LF3FD flags return the field-detection status of related channels.

2.5 LF active interface (PKE receiver)

2.5.1 Introduction

The device supports communication for passive keyless entry (PKE) applications by a high sensitive 3D LF active interface that receives data with high selectivity around the nominal carrier frequency $f_{CARR,nom}$.

The 3D LF active interface consists of three identical LF active receiver channels, a baseband processing unit, wake-up pattern detection, and a payload receiver (see Figure 18). It uses a superheterodyne receiver architecture, which employs a highly integrated frequency synthesizer consisting of a 32 kHz crystal oscillator and a phase locked loop (PLL). The frequency synthesizer requires a 32.768 kHz crystal as sole external component.

The LF active interface autonomously monitors all three coil inputs for a modulated LF carrier and, if a pre-configured LF telegram is detected, a device wake-up is triggered and subsequent payload data will be buffered for post-processing with the micro-controller.

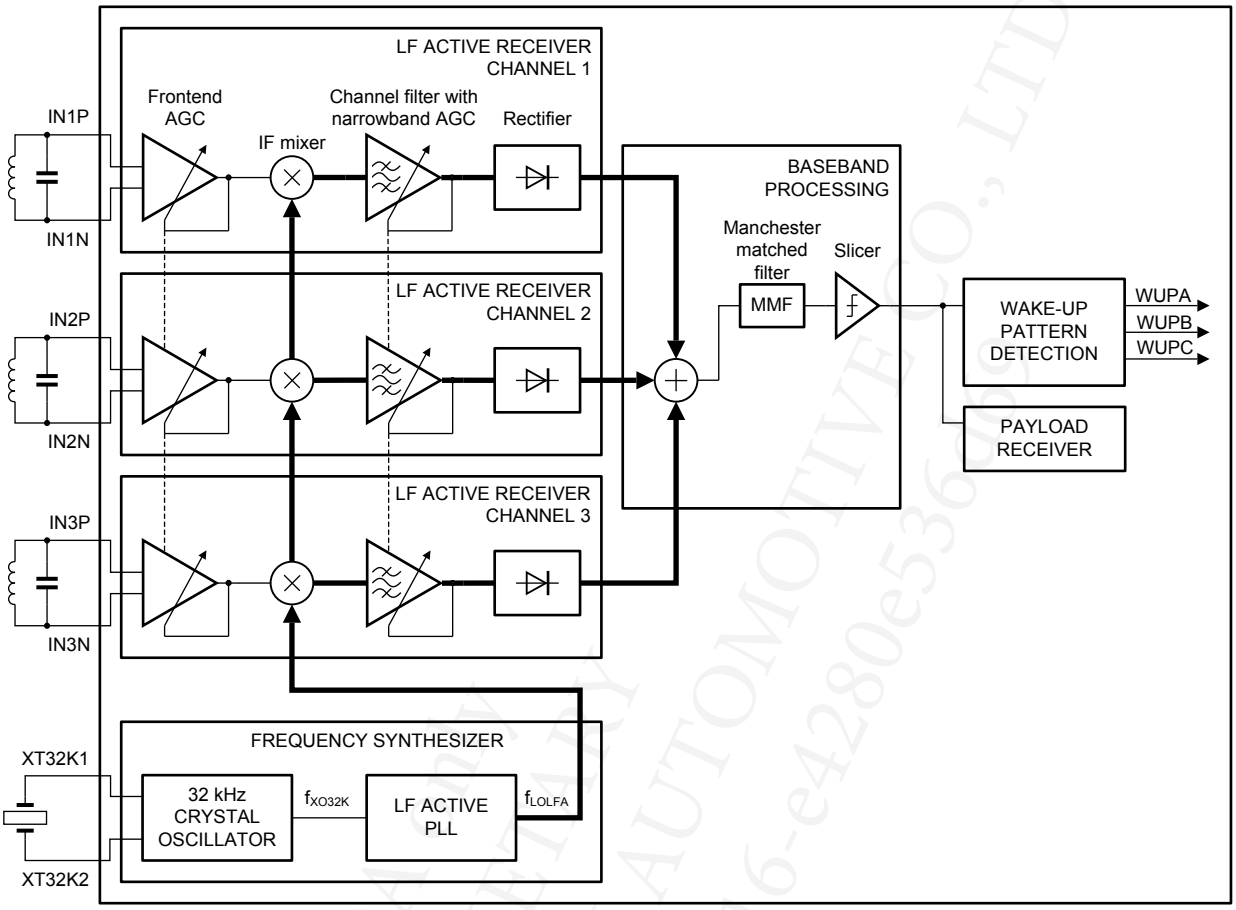


Figure 18. LF active receiver block diagram

2.5.2 LF telegram definition

The LF active interface supports LF telegrams with the following properties:

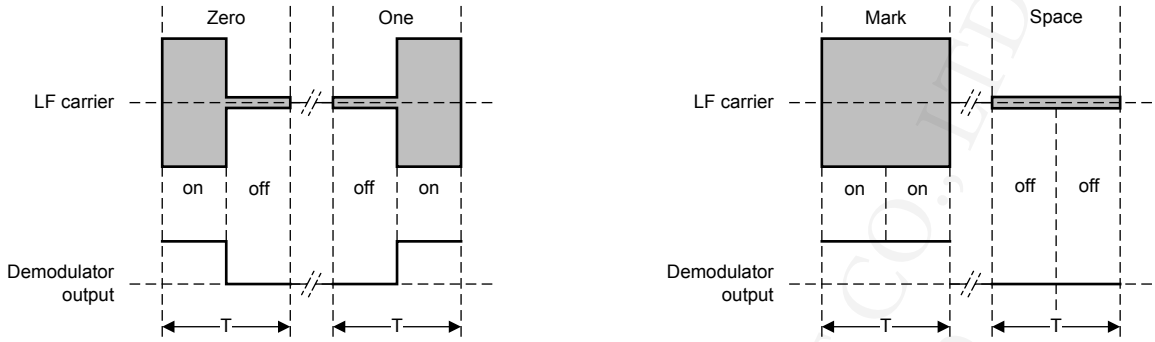
- LF carrier signal with carrier frequency f_{CARR}:

$$f_{\mathrm{CARR}} = f_{\mathrm{CARR,nom}} + \Delta f_{\mathrm{CARR}} \tag{2}$$

- On-off keying (OOK) of the LF carrier signal
  - Signal shaping caused by the bandwidth limitation due to the transmitter and receiver coils' quality factor may apply.
- Manchester encoding according to Figure 19(a) with a bit period T:

$$T = T_{\mathrm{nom}} + \Delta T \tag{3}$$

- The code violation section contains Manchester code violations according to Figure 19(b).



a. Regular Manchester codes

b. Manchester code violations

1. The waveforms shown here are for demonstration purpose only. The actual waveforms may deviate.

Figure 19. Regular Manchester code and Manchester code violations

The LF telegram structure consists of the run-in pattern, the wake-up pattern, and optional payload (see Figure 20):

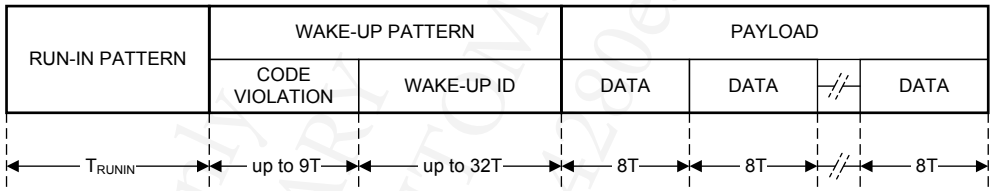


Figure 20. LF telegram structure

- **Run-in pattern**
  The run-in pattern is required for receiver settling and it shall preferably consist of Manchester zeros. The content of the run-in pattern is not evaluated. The run-in pattern shall have a minimum length T_{RUNIN}:

$$T_{RUNIN} = n_{RUNIN} \cdot T \quad (4)$$

- **Wake-up pattern**
  The whole wake-up pattern is used for the wake-up pattern detection. The wake-up pattern consists of the code violation pattern and the wake-up ID.
  The bits in the code violation pattern can be configured as regular Manchester code (zero or one) or as Manchester code violation (mark or space). The length of the code violation pattern is configurable and may contain up to 9 bits.
  The length of the wake-up ID is configurable and it may contain up to 32 bits of regular Manchester code (zero or one).
  Code violations in the wake-up pattern help to support telegram synchronization and to avoid that a wake-up pattern is found erroneously in a regular Manchester encoded data stream.
- **Payload data**
  The LF telegram may include payload data after the wake-up pattern. The payload is optional and may be omitted. Payload data is Manchester encoded (zeros and ones) and it is only supported in byte granularity (8T). The recommended maximum payload length shall not exceed 32 bytes.

NCF215A / NCF215B fully supports the LF telegram used by predecessor devices—e.g. NCF21A1/A2, NCF2157/58—as depicted in Figure 21.

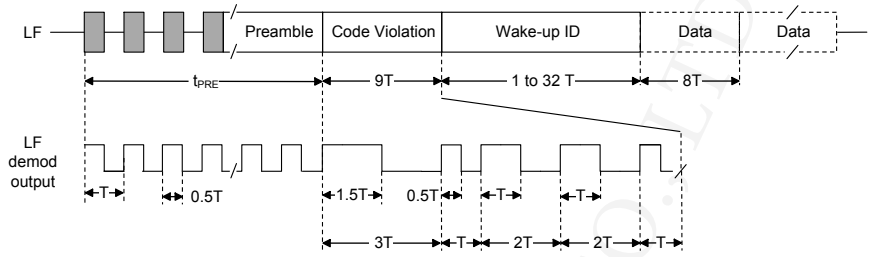


Figure 21. Legacy LF telegram

Please note that NCF215A / NCF215B requires some bits of the legacy code violation as additional run-in bits. Thus, the first few bits of the legacy code violation are not used for wake-up detection as depicted in Figure 22.

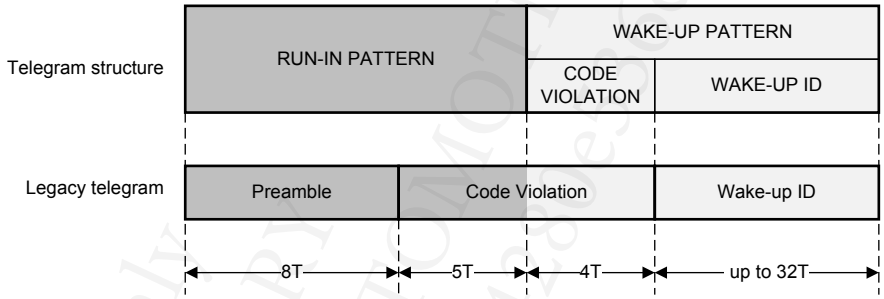


Figure 22. Mapping of legacy LF telegram

2.5.3 Frequency synthesizer

2.5.3.1 32 kHz crystal oscillator

The 32 kHz crystal oscillator can be operated independently of the LF active receiver and requires the supply voltages VBAT and VBATREG. The 32 kHz crystal oscillator uses a Pierce oscillator cell with gain control and features integrated load capacitors for the external crystal. It is intended for the operation with an external crystal with a nominal frequency of $f_{XO32K,nom}$ and a nominal load capacitance of C_{L_XO32K}.

For LF active operation, the crystal oscillator frequency f_{XO32K} must always stay within the following boundaries:

$$f_{XO32K,nom} + \min\left(\Delta f_{XO32K}\right) \leq f_{XO32K} \leq f_{XO32K,nom} + \max\left(\Delta f_{XO32K}\right) \quad (5)$$

The device supports a clock fail detection, which is able to detect any interruption of the 32 kHz crystal clock. This clock fail information can be configured as wake-up condition from the POWER OFF state or as interrupt source. The detection circuit requires a settling time of $t_{XO32KFAIL\_set}$ after it is enabled, during which time its output is invalid. It is recommended that until settled, the clock fail information is masked via bit XO32K_FAIL_MASK in register PRECON2.

It is advised to enable the clock fail detection once the crystal oscillator has settled. The clock fail detection is not intended to monitor the start-up of the crystal oscillator and the application shall always wait the crystal oscillator settling time t_{XO32K_set} before the clock is used.

2.5.3.2 LF active PLL

The device features a fully integrate phase locked loop (PLL) to generate the local oscillator frequency $f_{LOLFA} = 3 \cdot f_{XO32K}$ for the superheterodyne receiver. Furthermore, the PLL provides clock outputs for the DC-DC converter and the timer system (LFAPLLCLK). The LF active PLL requires the supply sources VBAT, VBATREG, VLFA and VLFADIG.

2.5.4 LF active receiver channel and baseband processing

The LF active receiver has three identical receiver channels consisting of a frontend AGC, an IF mixer, a channel filter with narrow band AGC, and a rectifier section. It requires the supplies VBAT, VBATREG, VLFA and VLFADIG.

The frontend AGC is a controllable attenuator operated in a closed loop. It includes a level detector which adjusts the attenuation of the incoming signal in order to create an optimal signal level for the IF mixer.

The IF mixer is implemented as quadrature (IQ) image rejection mixer. By multiplication of the incoming signal with f_{LOLFA}, the IF mixer creates in-phase (I) and quadrature (Q) output signals, which are fed into the subsequent channel filter.

The channel filter is centered around the IF frequency $f_{IFLFA} = f_{CARR,nom} - f_{LOLFA}$. The channel filter is responsible for the selectivity around the wanted signal f_{CARR} and attenuates other unwanted signals outside the wanted band—in particular signals from wireless electrical vehicle chargers located around 85 kHz, which are attenuated with $a_{CF,85k}$. Simultaneously, the channel filter acts as baseband filter for the OOK modulated signal thanks to its narrow filter bandwidth B_{CF}.

The channel filter has an integrated narrowband AGC loop, which supports a constant level at the filter output going to the subsequent rectifiers. The AGC loop influences only the gain of the filter while the actual filter characteristics are maintained over the whole dynamic range.

The narrowband AGC reacts on the channel-filtered signal, i.e. the gain is mainly determined by the wanted signal. This is in contrast to the frontend AGC, which operates on the whole input spectrum and can therefore be driven by a strong unwanted signal. This is an intended behavior, as the frontend AGC must limit the input signal for the IF mixer. As a consequence, the frontend AGC and the narrowband AGC have their own control loop and they operate fully independently of each other.

The AGC supports a fast attack mode to ensure that any wanted signal is acquired quickly. After the end of the protocol, the AGC regulates back to the sensitivity level, which is reached after the AGC recovery time t_{AGC_REC} at the latest.

The rectifiers operate as envelope detectors retrieving the baseband information for further processing. The in-phase and quadrature signals are rectified separately.

The device supports common baseband processing of all three receiver channels by combining all six rectified signals (I and Q of channel 1 to 3, respectively) into one common baseband signal. The common baseband ensures rotation independent LF receiver performance provided that all three LF active inputs use similar LF antennas.

The common baseband signal is processed with a Manchester matched filter (MMF), whose output feeds into the slicer to digitize the signal. The digital slicer outputs are used as input signals for the wake-up pattern detection and the payload receiver.

In order to support common baseband processing, it is mandatory that all three LF active receiver channels operate at the same total gain. This is achieved by a common control

of the frontend AGC and the narrowband AGC, respectively, in all three channels. Hence, the attenuation of the frontend AGC is determined by the strongest input signal of all three channels and the gain of the narrowband AGC by the strongest channel-filtered signal of all three channels. Please note that the frontend AGC and the narrowband AGC are still independent as mentioned above.

The LF active interface supports two different sensitivity modes G1M and G3M plus two desensitization modes D1M and D2M, which can be used to reduce the sensitivity temporarily in the application. The application shall consider a waiting time t_{ACT_set} after changing the receiver sensitivity.

2.5.5 Wake-up pattern detection

The wake-up pattern detection supports three independent wake-up patterns with identical configuration possibilities. Every wake-up pattern can be enabled, disabled, and configured individually. The individual configuration includes the content and the length of the wake-up pattern. Additional configurations are available to improve the pattern detection behavior under specific conditions, e.g. for high data rate offset (segmented correlator) or for very short wake-up patterns (strict correlation modes).

If the LF active receiver is enabled, the wake-up pattern detection searches continuously for all enabled wake-up patterns in parallel. If the incoming signal matches any of the enabled user programmed wake-up patterns, a wake-up event and an interrupt request is generated. If the device is in POWER OFF state, the wake-up brings it into BATTERY state.

The wake-up pattern detection features an optional error tolerance, which, when activated, tolerates between 1 and 7 wrong bits in the received LF signal. The error tolerance can support successful wake-up pattern detection in case single bits are destroyed by pulsed disturbers. Alternatively, it can be used to improve the sensitivity of the wake-up pattern detection. Please note that the activation of the error tolerance introduces ambiguity in the pattern matching process; e.g. if the error tolerance is configured to tolerate 1 wrong bit, a wake-up event is not only triggered when the programmed wake-up pattern is received but also if a pattern is received that differs by 1 bit from the programmed one.

2.5.6 Payload receiver

The payload receiver is only activated after a successful wake-up pattern match. It receives the payload data and buffers it in an 8 bit data register for further processing by the micro-controller. The micro-controller must fetch the received data byte in time before it is overwritten with the next received data byte. It is in the responsibility of the micro-controller to stop the payload receiver once all expected data bytes are received.

The application can configure whether the wake-up pattern detection searches for a wake-up pattern in parallel to the payload reception or not. In the latter case, the wake-up pattern detection becomes active, only after the payload receiver was stopped by the application.

2.5.7 Narrowband received signal strength indication (RSSI)

The narrowband received signal strength indication (RSSI, see Figure 23) supports LF input signal strength measurement over a wide dynamic range, starting below the sensitivity limit of the LF active interface and going up to $V_{RSSI,max}$. The measurement range can be extended on application level for very strong magnetic fields by use of the

channel shorting resistors. The RSSI analog frontend is connected directly to the LF input pins and is arranged in parallel to the LF active interface (PKE receiver) and the LF passive interface (immobilizer). The RSSI analog frontend conditions the input signal for the subsequent Sigma-Delta ADC (SD-ADC) and the RSSI digital part. The steep digital filters allow excellent narrowband performance and suppress unwanted signals outside the wanted band. The selected RSSI architecture excels with outstanding linearity and measurement accuracy.

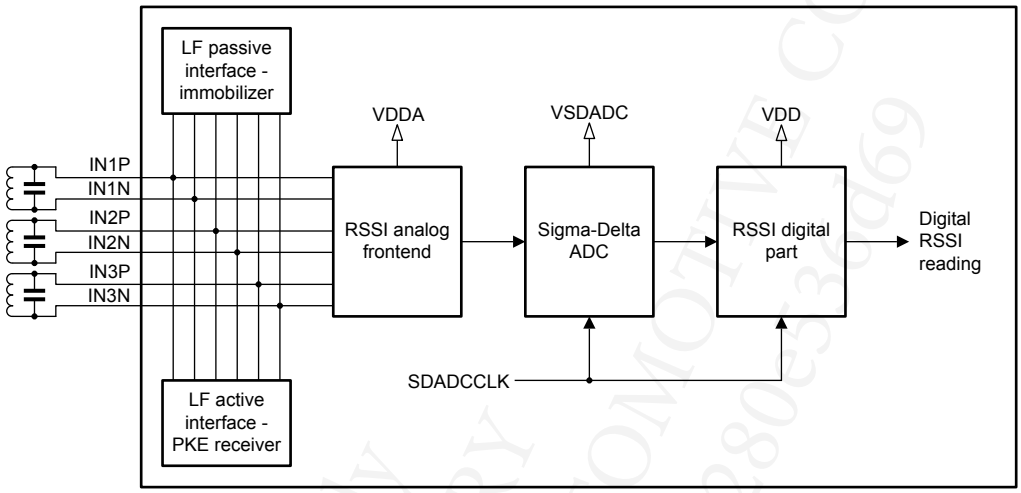


Figure 23. Narrowband RSSI block diagram

Activation of the RSSI analog frontend turns off the frontend AGC of the LF active interface to avoid disturbance. The LF active interface can be kept on, however, reception of LF active protocols is not supported in this case.

2.5.7.1 RSSI analog frontend

The RSSI analog frontend in Figure 24 consists of:

- Channel shorting resistors
- Q factor adjustment
- RSSI attenuator
- Input channel selection and optional summation
- Programmable gain selection
- Range overflow detector

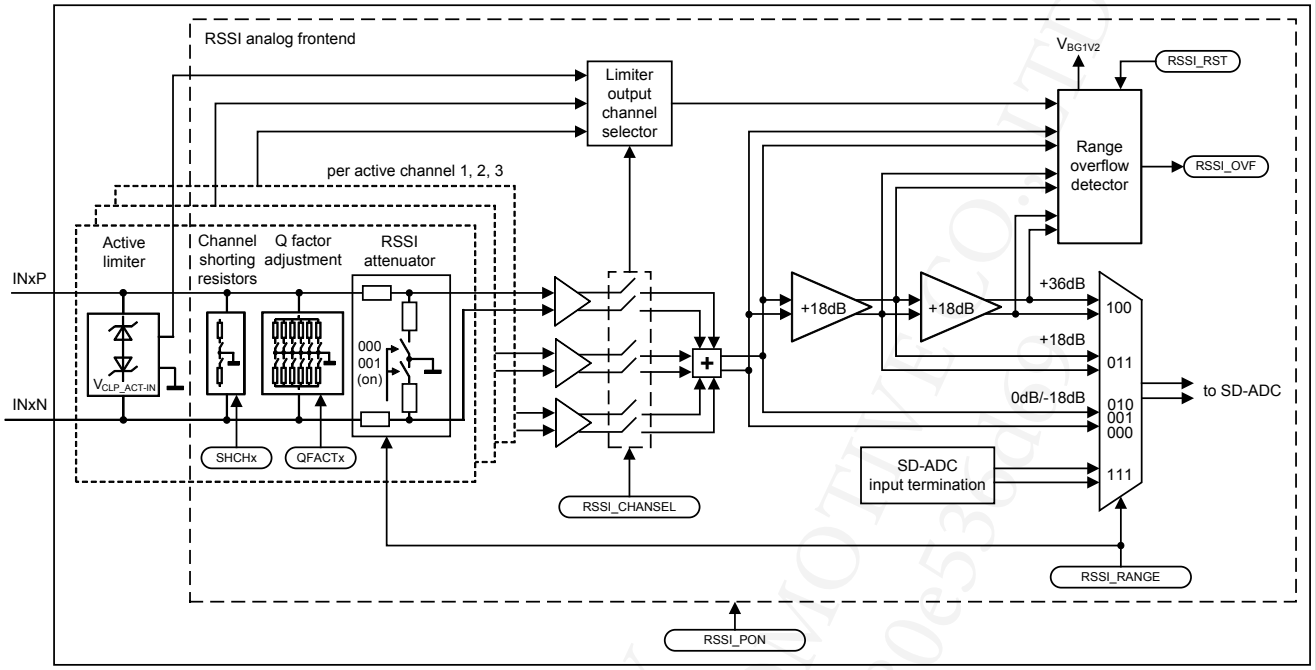
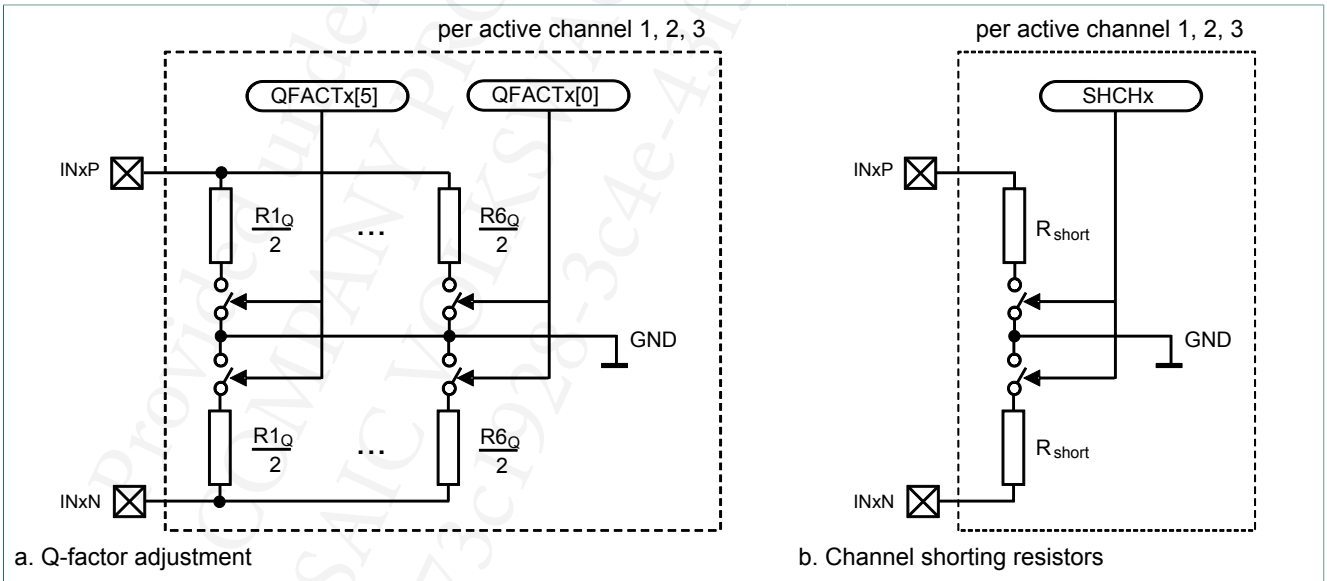


Figure 24. RSSI analog frontend

Channel shorting resistors

The channel shorting resistors R_{short} load the external resonant circuit and they are provided to attenuate the LF signal on individual RSSI channels (Figure 25b). When doing an RSSI measurement on one LF channel it is recommended to activate the channel shorting resistors on the other two LF channels to minimize errors caused by crosstalk between the three external coils. Additionally, the channel shorting resistors can be activated on the measured LF channel to linearize and to extend the measurement range for very strong LF input signals that would otherwise exceed the 0 dB or −18 dB range.



a. Q-factor adjustment

b. Channel shorting resistors

Figure 25. Q-factor adjustment and channel shorting resistors

Q factor adjustment

Q factor adjustment (Figure 25a) is provided to allow control of the Q factor of the external resonant circuit during RSSI measurement. The external resonant circuit is loaded with configurable resistors, which are divided into two equal parts that are connected to ground via switches. By providing six weighted resistors ($R1_Q$ to $R6_Q$) in parallel, meaningful resistor values can be chosen by switching on/off various combinations.

Optionally, the Q factor adjustment may be used for LF active protocol reception as well. In this case it is recommended to select the automatic Q factor adjustment deactivation when an LF passive protocol is detected (set bit PRECON2.RINMODE = 1, see Table 46). This avoids negative influence on the immobilizer performance which might be caused by additional loading of the external resonant circuit.

Input signal selection

The RSSI analog frontend allows the selection of one individual LF channel (IN1P/IN1N, IN2P/IN2N, IN3P/IN3N) or the sum of two or all three LF channels. For normal RSSI measurement only one LF channel shall be selected at a time. The summation of multiple LF channels can be used to assess the phase relationship between different LF channels.

Gain selection, RSSI attenuator, range overflow detector (indicator)

The device supports different gain ranges—referred to as +36 dB, +18 dB, 0 dB, and -18 dB modes—to cope with the wide dynamic range of the input signal. The appropriate gain setting is identified with the help of fast range overflow detectors (indicators). Once the correct gain setting is found, the amplified signal is switched to the input of the SD-ADC for further processing.

The -18 dB mode is implemented by means of the RSSI attenuator. The application may decide to use the channel shorting resistor instead of the RSSI attenuator as range extension for strong input signals.

The range overflow detection operates on the whole frequency spectrum of the applied input signal, i.e. the wanted signal and potential interferers, and has configurable thresholds. In addition to finding the correct gain setting at the beginning of the measurement, the range overflow detection runs throughout the whole RSSI measurement cycle to check for any overflow condition. An overflow condition can appear, if the input signal increases significantly during the RSSI measurement cycle (e.g. caused by an increase of an interferer).

One part of the range overflow detection (RSSICON0.RSSI_OVF = 000b) reuses the active limiter output signals from the LF active interface (see Figure 24) to signal an overflow condition for very strong input signals.

Every device stores individual RSSI calibration values to correct gain errors of the different gain stages in order to get one continuous measurement range. Software routines for RSSI measurement and calibration are provided as C library functions to be linked to the application program.

2.5.7.2 RSSI digital processing

The digitized output from the SD-ADC is first filtered with a narrow digital bandpass filter centered around $f_{CARR,nom}$ (see Figure 26). Four different filter settings A to D are available to balance the wanted filter bandwidth ($B_{RSSI\_FILT\_A} > B_{RSSI\_FILT\_B} >$

$B_{RSSI\_FILT\_C} > B_{RSSI\_FILT\_D}$) and filter settling time ($t_{RSSI\_FILT\_A} < t_{RSSI\_FILT\_B} < t_{RSSI\_FILT\_C} < t_{RSSI\_FILT\_D}$). All four filter settings are designed to suppress signals from wireless electrical vehicle chargers located around 85 kHz in an optimal way. Narrower filter settings can be selected to suppress other interferers, which are closer to the target frequency.

The digital bandpass filter is followed by an amplitude measurement unit, measuring the peak amplitude, and an averaging unit. The averaging factor is configurable and a higher number gives more accurate and stabler RSSI readings.

The output of the SD-ADC is continuously monitored with an overload detector. If an overload condition is detected, the flag SDADC_OVERLOAD in register RSSICON3 is set and the RSSI output values are not reliable. Please note that the SD-ADC overload detector must always be used together with the analog range overflow detectors (see Section 2.5.7.1) to detect all overload conditions reliably.

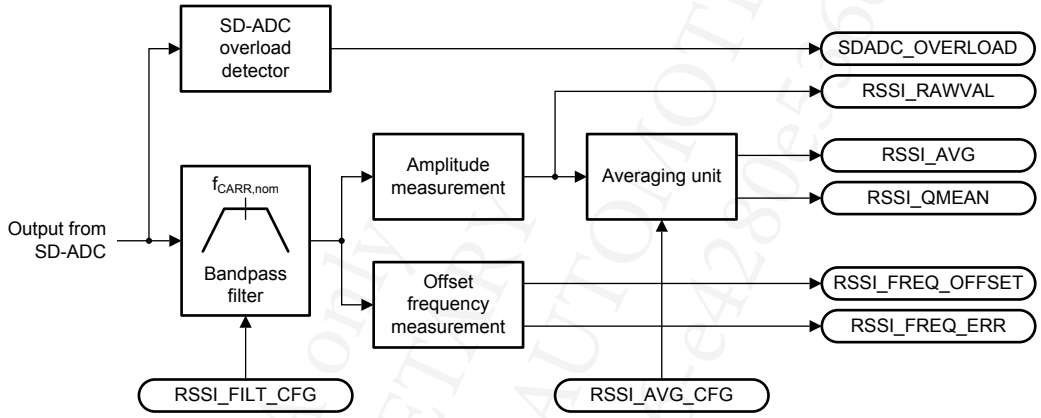


Figure 26. RSSI digital processing

The device supports a unique method for interferer detection within the filter bandwidth. Using different amplitude measurement methods, the device can reliably detected whether one or several signals are present. If only one signal is present, the offset frequency measurement unit distinguishes, if it is a wanted signal around the nominal frequency or an interferer with a different frequency. If an interferer is detected, the application may perform a second RSSI measurement with the wanted signal turned off to measure only the interferer amplitude. The amplitude of the wanted signal can then be calculated from the RSSI readings of the two measurements.

2.5.7.3 RSSI measurement sequence

An RSSI measurement sequence consists in general of an initialization step, followed by three consecutive single channel RSSI measurements. Each single-channel measurement must be preceded by a range selection step, used to set the gain path in the proper state, allowing operation over the entire dynamic range. A precondition for the RSSI measurement is a constant carrier input signal on the selected LF input channel. Modulated input signals will lead to lower RSSI values caused by narrowband filtering and averaging over the measurement time. An example RSSI measurement sequence is depicted in Figure 27.

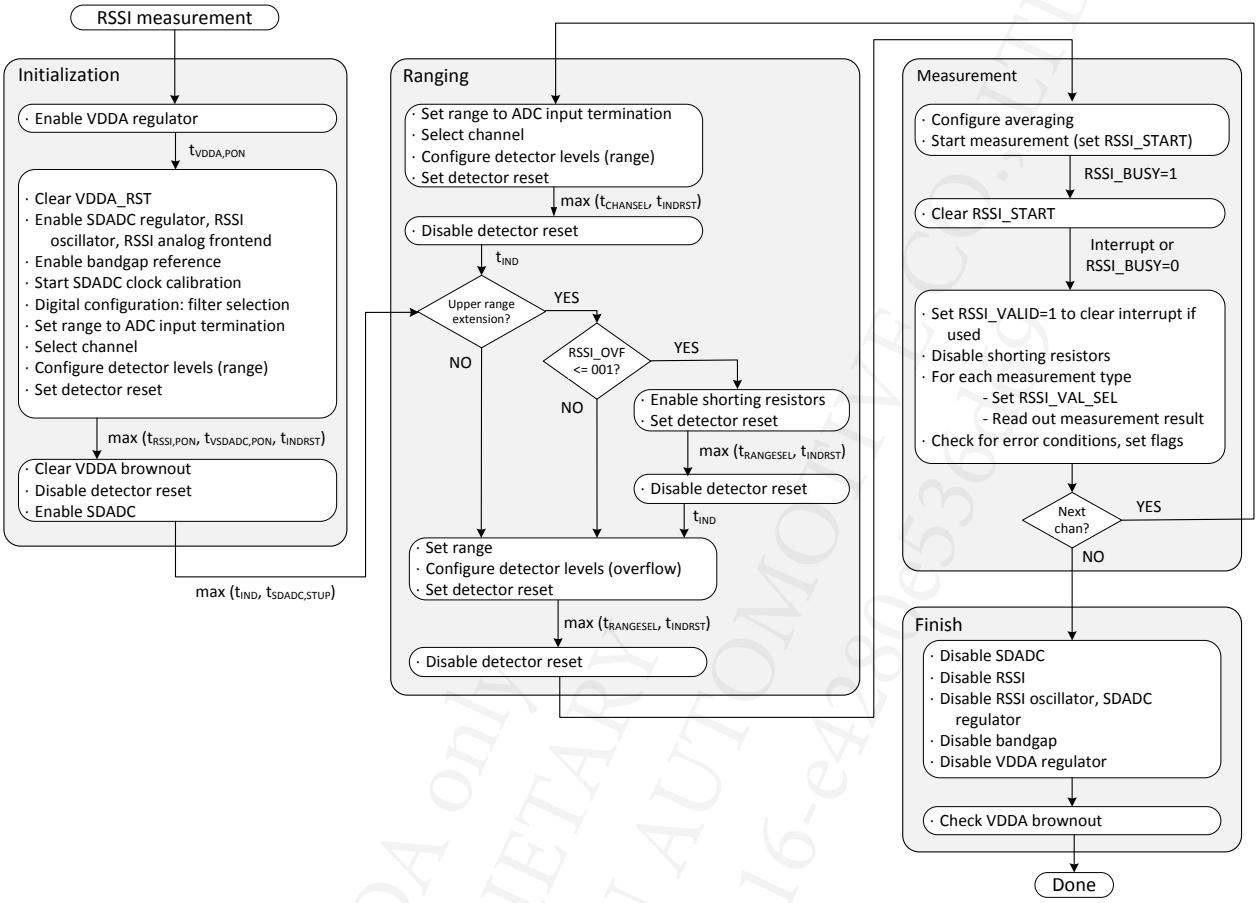


Figure 27. RSSI measurement sequence

Initialization

The RSSI measurement starts with powering up the relevant supply domains and the required circuit blocks. The RSSI analog frontend is accommodated in the VDDA supply domain and the SD-ADC in the VSDADC domain. The application shall turn on VDDA and VSDADC supplies before the RSSI block can be used. A waiting time of $t_{VDDA,PON}$, followed by deassertion of VDDA_RST, is required after turning on the VDDA regulator and before the RSSI analog frontend can be enabled by setting RSSI_PON. At this time, the 16 MHz precision RC oscillator for the SD-ADC and the 1.2 V bandgap reference (bit BG1V2EN in register ADCCON, see Table 156) must also be enabled and the calibration of the SD-ADC oscillator must be triggered, which requires an execution time of $t_{SDADCCLK,CAL}$. Digital settings, such as digital filter selection may also be set at this time.

After RSSI power-on, the application shall wait until the RSSI block has settled ($t_{RSSI,PON}$) before the first measurement can be started. At this time, the SD-ADC must also be enabled, allowing sufficient settling time ($t_{SDADC,STUP}$) before the first conversion.

It is recommended to clear the VDDA brownout flag at this point, so as to guard the subsequent RSSI operation against a potential brownout condition caused by a weak battery.

It is also recommended to power-on the RSSI block with the channel selection set to the first channel to be measured (e.g. RSSI_CHANSEL[2:0] = 001 for channel 1). In this case, the first RSSI measurement can omit the first part, which includes a waiting period of $t_{CHANSEL}$. For this, it is also necessary to set the RSSI range to the SD-ADC input termination setting, load the range/overflow detectors with the range settings, and apply RSSI_RST as described in detail below.

Single channel RSSI ranging and measurement

A single channel RSSI ranging and measurement sequence starts with setting the gain range to the SD-ADC input termination (RSSI_RANGE[2:0] = 111) and selecting the channel to be measured (RSSI_CHANSEL[2:0]), including optional shorting of non-selected channels (SHCHx=1). At the same time the range/overflow detectors must be loaded with the settings for the range detection phase (as defined in Section 2.5.10.13) and detector reset must be applied (RSSI_RST = 1) for at least time t_{INDRST}. This state has to be maintained for the minimum channel selection time $t_{CHANSEL}$.

After releasing the detector reset (RSSI_RST = 0) and waiting for the settling time t_{IND}, the range overflow bits (RSSI_OVF[2:0]) can be evaluated and the gain chain has to be set accordingly. Typically, RSSI_RANGE[2:0] is set to the value returned by the range detectors, RSSI_OVF[2:0]. When using the upper range extension feature, the application must check the range detector results before setting the range. In case the value 000 or 001 was returned (out-of-range condition or 0 dB range overflow respectively), it is recommended that the shorting resistors for the selected channel are activated and range detection is repeated. This is done by resetting again the range detectors for at least t_{INDRST} and allowing a time of $t_{RANGESEL}$ for the gain path to settle and t_{IND} for the detectors to detect the new range. The value returned in RSSI_OVF[2:0] is now the value to use for the range setting, RSSI_RANGE[2:0].

Following, the range/overflow detectors have to be programmed with the settings for overflow detection, to guard against possible overflow during the measurement. A minimum reset time of t_{INDRST} is required, this can overlap with the range settling time $t_{RANGESEL}$, which is needed because of the updated range setting.

For the A/D conversion, the average configuration must be set beforehand. This may be static, or differ from channel to channel due to possible use of the upper range extension for some channels. A/D conversion is be started by setting bit RSSI_START. RSSI_START should be cleared once RSSI_BUSY is set to 1, indicating that processing of the digitized signal has started. The end of conversion is signaled after the time t_{RSSI_DIG} (see Equation 7) by RSSI_BUSY going low and interrupt IF_RSSI, if enabled. The results of the measurement can be fetched from the RSSI_VAL register, by setting RSSI_VAL_SEL appropriately to indicate the desired result type.

The corrected RSSI result $RSSI_{CAL}$ is available after application of the RSSI calibration library function to the average RSSI value RSSI_AVG read out of the RSSI_VAL register.

It is recommended that the channel shorting resistors are disabled as soon as each channel conversion is finished. In addition, in order to minimize the overall measurement time it is recommended to select the next channel (RSSI_CHANSEL[2:0]) at the end of the respective single channel measurement as early as possible, so that settling time $t_{CHANSEL}$ can partly overlap with software execution. It is to be noted however that in case the shorting resistors were switched, the LC tank circuit also needs to settle again since the Q factor has changed; this is an application-dependent delay between the shorting resistors release and the end of channel settling ($t_{CHANSEL}$ delay), that needs to be considered in addition to the timing constraints imposed by the operation of the IC.

If the total measurement time of the RSSI measurement sequence is exceeding 2 ms, flag R2MSDET should be set regularly to reset the 2 ms detection.

Assessment of measurement results

A number of checks should be used to assess the validity and expected accuracy of the measurement results:

- After an A/D conversion, it should be checked that SDADC_OVERLOAD=0. If not, an ADC overload condition has occurred and the measurement result is invalid. This may happen for example in case a pulsed disturber started between the range detection and the measurement.
- An overflow condition of the analog gain path is indicated by the condition RSSI_OVF ≤ RSSI_RANGE (in case the -18dB range was set for the measurement) or RSSI_OVF < RSSI_RANGE (in case any other range was set). In the event of an analog overflow the accuracy of the result is not guaranteed.
- In case VDDABRNREG=1, a low VDDA level has occurred during the measurement, for example due to end-of-life battery. In this case the measurement results are not reliable.
- If the values RSSI_QMEAN and RSSI_AVG differ by more than a threshold RSSI_DIFF, this indicates the presence of multitone signal, such as the wanted CW RSSI burst plus an in-band disturber. For averaging factors ≥ 16, the recommended value of RSSI_DIFF is 3 LSB.
- Otherwise, if RSSI_FREQ_ERR=1, the input signal may still be a multitone or a pure in-band jammer. In this case the value of RSSI_FREQ_OFFSET is immaterial.
- Otherwise, if RSSI_FREQ_OFFSET is larger than the threshold RSSI_FO, the signal is most likely a pure in-band jammer, at a frequency indicated by RSSI_FREQ_OFFSET. However, in the presence of weak signals, this condition can also happen with a combination of weak wanted and jammer signals. A recommended value for RSSI_FO is 15 LSB if averaging ≥ 32 is used, or 22 LSB for averaging ≥16, plus the expected carrier frequency offset between base-station transmitter and key fob. For averaging less than 16, RSSI_FREQ_OFFSET is not valid and shall not be evaluated.
- Otherwise, the input signal is the wanted RSSI burst at a level of RSSI_AVG.

In cases above where the measurement might indicate a multitone signal, the application may report an error or it may repeat the measurement at a time when the RSSI burst is not present, and calculate the wanted signal strength as $\sqrt{\text{RSSI\_QMEAN}_1^2 - \text{RSSI\_QMEAN}_2^2}$ (see Figure 28).

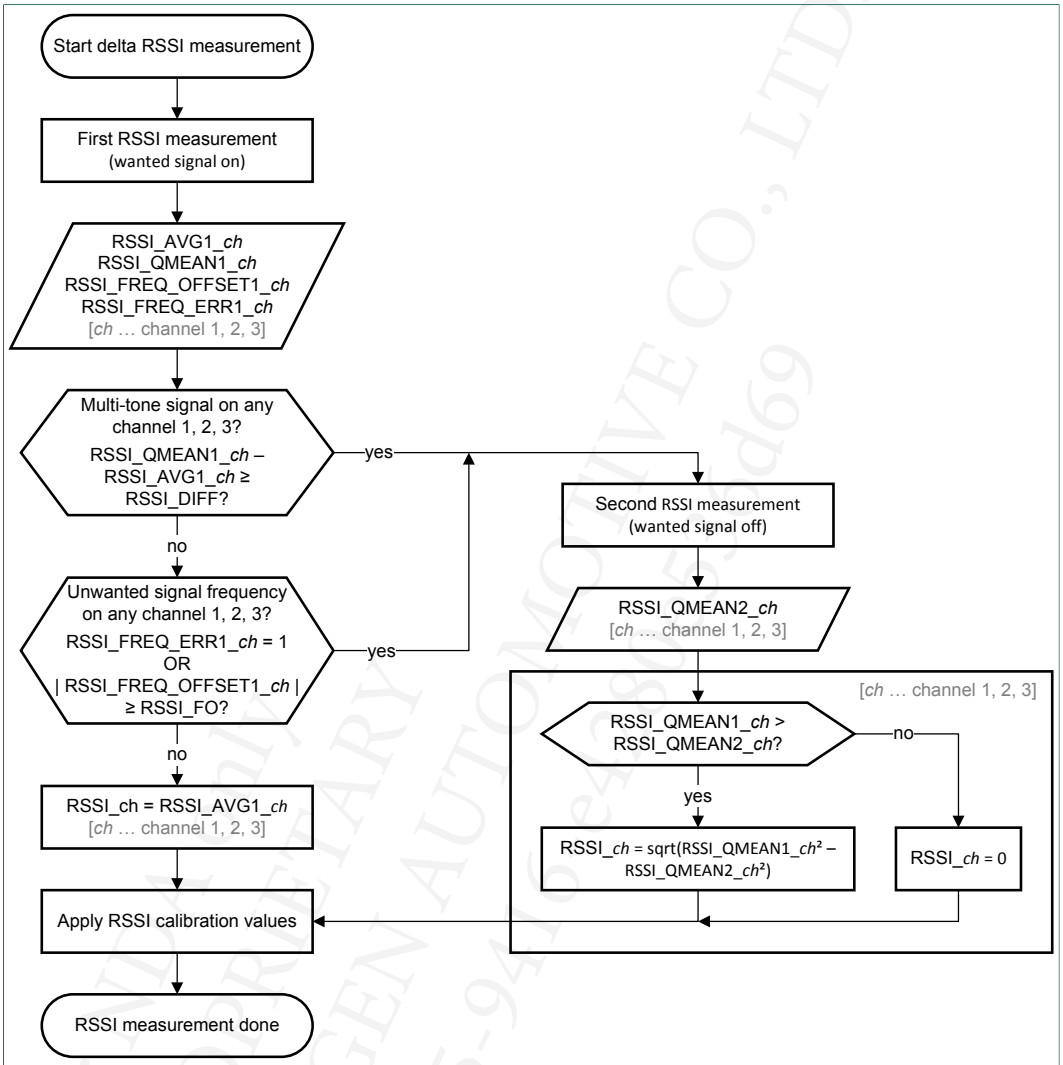


Figure 28. Delta RSSI measurement flow with in-band jammer detection

The RSSI peak-to-peak input voltage $V_{RSSI,pp}$ is calculated according to Equation 6 from the calibrated RSSI reading $RSSI_{CAL}$ (derived from RSSI_AVG or RSSI_QMEAN). The gain value G_{RSSI_dB} depends on the used gain setting and must be replaced by G_{RSSI_54dB}, G_{RSSI_36dB}, G_{RSSI_18dB}, G_{RSSI_0dB}, and G_{RSSI_-18dB}, respectively.

$$V_{RSSI,pp} = RSSI_{CAL} \cdot \frac{K_{SDADC}}{G_{RSSI\_dB}} \quad (6)$$

2.5.8 Interval timer and real-time clock

The interval timer can generate periodical events in order to wake-up the device from POWER OFF state. The wake-up time is configurable.

The real-time clock features a 16 bit register holding minutes, seconds, and fractions of seconds with a resolution of nominal 1/16th of a second. The register content can be used as a time stamp in protocols or to display the time. The application can extend the

time stamp interval with additional software counters stored in battery supplied registers. The real-time clock supports wake-up events independently from the interval timer.

The interval timer and the real-time clock use the same counter chain, which is operated with the 32 kHz crystal clock (XO32KCLK). Due to the continuous operation in the regulated battery supply domain VBATREG, both timers operate independently of the supply state.

When the interval timer is running it provides a divided clock (LPDIVCLK) with 2 kHz nominal clock speed.

The status bits RTC_WUP, RTC_WUP_OVF and IT_WUP are located in register PRESTAT. The real-time clock data is stored in the register RTCDAT.

2.5.9 LF active post-wake-up timer

The LF active post-wake-up timer is intended to support protocol timings which use the incoming LF protocol as timing reference. Typical reference time points are the detection of the wake-up pattern or the end of the LF protocol.

The LF active post-wake-up timer is an incrementing timer with a compare register. Most of the time the timer is off and held in reset. The timer starts counting automatically, when a valid LF active wake-up pattern is recognized. If the timer value reaches the value stored in the compare register, an interrupt is raised and the timer is reset again. The timer supports a single shot and a multi shot mode. In single shot mode, the timer is stopped after the compare match, whereas the timer starts incrementing again in multi shot mode to support the generation of back-to-back timing intervals. The application can modify the compare register or stop the timer at any time.

Optionally, it is possible to select the reception of a new data byte by the LF active receiver as an additional reset source. This is required, if the end of the protocol is requested as reference time point. The LF active post-wake-up timer is then reset with the reception of every single data byte and it starts incrementing again immediately thereafter.

The LF active post-wake-up timer is clocked with the accurate 32 kHz crystal clock (XO32KCLK) and it is supplied by the regulated battery supply domain VBATREG.

2.5.10 Registers

2.5.10.1 DC-DC converter control registers 0, 1, 3, 4, 6, 7, 8, DCDCCONx

The DC-DC converter is controlled by several control bits in the registers DCDCCON0 (Table 25), DCDCCON1 (Table 26), DCDCCON3 (Table 27), DCDCCON4 (Table 28), DCDCCON6 (Table 29), DCDCCON7 (Table 30), and DCDCCON8 (Table 31).

Table 25. DC-DC converter control register 0, DCDCCON0 (reset value xx00_0100b)

Bit	Symbol	Access	Value	Description
7	DCDC_RAMP_DONE	R/W0		DC-DC converter ramp-up status
			0	Initial ramp-up not finished, DC-DC converter is not ready to use
			1	Initial ramp-up finished, VLFA is within functional range [1]
6	DCDC_STUP_DONE	R/W0		DC-DC converter start-up sequence status

Bit	Symbol	Access	Value	Description
			0	DC-DC converter start-up not finished
			1	DC-DC converter start-up finished [1]
5 to 3	RDT	R/W0		Reserved for device test—must be set to 000 in the application
2 to 1	DCDC_CKSEL[1:0]	R/W		DC-DC converter clock source selection
			00	Reserved for device test
			01	Reserved for device test
			10	Uses the clock from the internal start-up oscillator, internal start-up oscillator is on
			11	Uses the clock from the LF active PLL, internal start-up oscillator is off
0	DCDC_EN	R/W		DC-DC converter enable
			0	DC-DC converter disabled, VLFA is not driven by the DC-DC converter
			1	DC-DC converter enabled

[1] Writing a 1 is not allowed.

Table 26. DC-DC converter control register 1, DCDCCON1 (reset value 40h)

Bit	Symbol	Access	Value	Description
7 to 0	DCDCCON1[7:0]	R/W		DC-DC converter control register 1
			40h	Required setting for DC-DC converter operation
			all others	Reserved for device test

Table 27. DC-DC converter control register 3, DCDCCON3 (reset value 3Ch)

Bit	Symbol	Access	Value	Description
7 to 0	DCDCCON3[7:0]	R/W		DC-DC converter control register 3
			3Ch	Required setting for DC-DC converter operation
			all others	Reserved for device test

Table 28. DC-DC converter control register 4, DCDCCON4 (reset value 00h)

Bit	Symbol	Access	Value	Description
7 to 0	DCDCCON4[7:0]	R/W		DC-DC converter control register 4
			00h	Required setting for DC-DC converter operation
			all others	Reserved for device test

Table 29. DC-DC converter control register 6, DCDCCON6 (reset value 20h)

Bit	Symbol	Access	Value	Description
7 to 0	DCDCCON6[7:0]	R/W		DC-DC converter control register 6
			20h	Required setting for DC-DC converter operation
			all others	Reserved for device test

Table 30. DC-DC converter control register 7, DCDCCON7 (reset value 000x_xxxxh)

Bit	Symbol	Access	Value	Description
7 to 5	RDT	R/W0		Reserved for device test—must be set to 000 in the application
4 to 0	RDT	-/W0		Reserved for device test—must be set to 000 in the application

Table 31. DC-DC converter control register 8, DCDCCON8 (reset value 0xxx_xxxxh)

Bit	Symbol	Access	Value	Description
7	BG_EN	R/W		DC-DC converter bandgap voltage reference enable
			0	Bandgap voltage reference disabled
			1	Bandgap voltage reference enabled
6	BG_OK	R/W0		DC-DC converter bandgap voltage reference status
			0	Bandgap voltage invalid
			1	Bandgap voltage valid [1]
5 to 0	RDT	-/-		Reserved for device test

[1] Writing a 1 is not allowed.

DCDC_RAMP_DONE

Indicates that the initial ramp-up of the DC-DC converter output is finished and VLFA reached the necessary range for operation of the LF active interface, while the DC-DC converter is still operating on its internal clock. The LF active interface can be enabled at this time, but power efficiency will not be optimal as long as the DC-DC converter is not switched to the LF active PLL clock.

The flag will be automatically cleared when the DC-DC converter is disabled (DCDC_EN = 0). Note that any external disturbance of the voltage level at pin VLFA will not affect the value of this flag.

DCDC_STUP_DONE

Indicates that the start-up procedure of the DC-DC converter is completed after its clock selection was switched to the LF active PLL (DCDC_CKSEL = 11).

The flag will be automatically cleared when the DC-DC converter is disabled (DCDC_EN = 0). A high-to-low transition of DCDC_STUP_DONE while the DC-DC converter is enabled might indicate a general failure and sets bit LFA_DCDC_FAILREG (see Table 43), which is one source of the LF active monitors interrupt flag IF_LFAMON, see Table 104.

DCDC_CKSEL

Selection of clock source for the DC-DC converter. After power-up or reset, DCDC_CKSEL = 10 selects the internal start-up oscillator. After the LF active PLL is enabled and settled, DCDC_CKSEL shall be set to 11 to select the clock from the LF active PLL and power down the internal start-up oscillator. A settling time of t_{DCDC_set} is required after selection of the PLL clock.

BG_EN, BG_OK, DC-DC converter bandgap reference voltage

BG_EN enables the bandgap voltage reference of the DC-DC converter. The bandgap reference requires a settling time of t_{DCDCBG_set}. It is allowed to enable the DC-DC converter (DCDC_EN = 1) immediately after enabling the reference, since the status of the bandgap reference is checked internally and the bit DCDC_RAMP_DONE is only asserted, if the bandgap reference voltage is settled.

BG_OK indicates the status of the bandgap reference. A high-to-low transition of BG_OK might indicate a general failure. When the start-up of the DC-DC converter was done and the bit DCDC_STUP_DONE is 1, any high-to-low transition of BG_OK causes a high-to-low transition of DCDC_STUP_DONE which eventually sets bit LFA_DCDC_FAILREG (see Table 43).

2.5.10.2 LF active enable registers 0 to 4, LFAEN0 to LFAEN4

The function blocks of the LF active receiver, the 32 kHz crystal oscillator, and the LF active PLL can be enabled and disabled by several control bits in the registers LFAEN0 (Table 32), LFAEN1 (Table 33), LFAEN2, LFAEN3 and LFAEN4 (Table 34).

Table 32. LF active enable register 0, LFAEN0 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	LFA_EN_DEMOD_MMF	R/W		Enable the Manchester matched filter in the demodulator
			0	Manchester matched filter disabled
			1	Manchester matched filter enabled
6	LFA_EN_DEMOD_MMF_SLICER	R/W		Enable the slicer in the MMF path
			0	MMF slicer disabled
			1	MMF slicer enabled
5	RFU	-/W0		Reserved for future use
4	LFA_EN_IFFILT_CAL	R/W		Enable the IF filter calibration unit
			0	IF filter calibration disabled
			1	IF filter calibration enabled
3	LFA_EN_XTAL_32K_OK_FLAG	R/W		Enable the monitoring circuit for the clock fail detection of the 32 kHz crystal oscillator
			0	Monitoring circuit disabled
			1	Monitoring circuit enabled
2	LFA_EN_XTAL_32K	R/W		Enable the 32 kHz crystal oscillator
			0	Crystal oscillator disabled
			1	Crystal oscillator enabled
1	RDT	R/W0		Reserved for device test—must be set to 0 in the application

Bit	Symbol	Access	Value	Description
0	LFA_EN_LDO	R/W		Enable the VLFADIG supply regulator
			0	Regulator disabled
			1	Regulator enabled

Table 33. LF active enable register 1, LFAEN1 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	LFA_EN_XTAL_CLK_DEMOD	R/W		Enable the 32 kHz crystal clock for the demodulator
			0	Clock disabled
			1	Clock enabled
6	LFA_EN_PLL_CLK_TIMER	R/W		Enable LFAPLLCLK for the timer system
			0	LFAPLLCLK disabled
			1	LFAPLLCLK enabled
5	LFA_EN_PLL_CLK_DCDC	R/W		Enable the LF active PLL clock for the DC-DC converter
			0	Clock disabled
			1	Clock disabled
4	LFA_EN_PLL_CLK_IFFILT_CAL	R/W		Enable the LF active PLL clock for the IF filter calibration unit
			0	Clock disabled
			1	Clock enabled
3	LFA_EN_PLL_LO	R/W		Enable the local oscillator clock for the mixer
			0	Clock disabled
			1	Clock disabled
2	LFA_EN_PLL_NDIV	R/W		Enable the LF active PLL feedback divider block
			0	PLL feedback divider disabled
			1	PLL feedback divider enabled
1	LFA_EN_PLL_VCO	R/W		Enable the LF active PLL VCO block
			0	VCO disabled
			1	VCO enabled
0	LFA_EN_PLL_PFD	R/W		Enable the LF active PLL phase frequency detector block
			0	Phase frequency detector disabled
			1	Phase frequency detector enabled

Table 34. LF active enable register 2, 3, 4, LFAEN2, LFAEN3, LFAEN4 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	RFU	-/W0		Reserved for future use
6	LFA_CHx_EN_RECT_Q	R/W		Enable the quadrature path (Q) rectifier of channel x (x = 1,2,3)
			0	Rectifier disabled

Bit	Symbol	Access	Value	Description
			1	Rectifier enabled
5	LFA_CHx_EN_RECT_I	R/W		Enable the in-phase path (I) rectifier of channel x (x = 1,2,3)
			0	Rectifier disabled
			1	Rectifier enabled
4	LFA_CHx_EN_AGC2_IF	R/W		Enable the 2nd narrowband AGC stage of channel x (x = 1,2,3)
			0	AGC disabled
			1	AGC enabled
3	LFA_CHx_EN_AGC1_IF	R/W		Enable the 1st narrowband AGC stage of channel x (x = 1,2,3)
			0	AGC disabled
			1	AGC enabled
2	LFA_CHx_EN_IFFILT	R/W		Enable the IF filter sections of channel x (x = 1,2,3)
			0	IF filter sections disabled
			1	IF filter sections enabled
1	LFA_CHx_EN_IF_MIXER	R/W		Enable the mixer in the receiver chain of channel x (x = 1,2,3)
			0	Mixer disabled
			1	Mixer enabled
0	LFA_CHx_EN_AGC_RF	R/W		Enable the frontend AGC of channel x (x = 1,2,3)
			0	AGC disabled
			1	AGC enabled

LFA_EN_IFFILT_CAL, IF filter calibration enable

Enables the IF filter calibration unit. Preconditions: 32 kHz crystal oscillator clock settled, LF active PLL settled, VLFADIG supply settled. The clock input must be enabled by setting LFA_EN_PLL_CLK_IFFILT_CAL = 1. The filter calibration requires a settling time of $t_{IFFILTCAL\_set}$.

LFA_EN_LDO0, VLFADIG regulator enable

Preconditions for the activation of the VLFADIG regulator are: 32 kHz crystal oscillator clock settled, VLFA supply settled, DC-DC converter reference voltage settled. The regulator requires a startup time of $t_{VLFADIG,PON}$.

LF active PLL activation

The LF active PLL consists of the voltage controlled oscillator (VCO), the feedback divider and the phase frequency detector for proper operation, all of which must be enabled together by setting LFA_EN_PLL_VCO = 1, LFA_EN_PLL_NDIV = 1, and LFA_EN_PLL_PFD = 1.

Preconditions for the activation of the LF active PLL are: 32 kHz crystal oscillator clock settled, VLFA and VLFADIG supplies settled. The LF active PLL supports a lock detector, which is enabled automatically together with the LF active PLL. The lock detector can be used to determine when the PLL is settled (bit LFA_PLL_LD in register LFASTATUS, see Table 43). The LF active PLL requires a settling time of t_{LFAPLL_set}.

2.5.10.3 LF active control registers 0 to 2 and 4 to 8, LFACONx

The registers LFACON0 (Table 35), LFACON1 (Table 36), LFACON2 (Table 37), LFACON4 (Table 38), LFACON5 (Table 39), LFACON6 (Table 40), LFACON7 (Table 41), and LFACON8 (Table 42) allow the configuration of the LF active receiver.

Table 35. LF active control register 0, LFACON0 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	RDT	R/W0		Reserved for device test—must be set to 0 in the application
6	LFA_RF_AGC_RESET	R/W		Reset of the frontend AGC stage; effects all three channels 1, 2, 3
			0	No reset, normal AGC function
			1	AGC reset to maximum gain (minimum attenuation), AGC function inhibited
5	RDT	R/W0		Reserved for device test—must be set to 0 in the application
4	LFA_BRNREG	R/W1->0		VLFA brownout wake-up and interrupt request register [1]
			0	No VLFA brownout—no wake-up event, no interrupt request
			1	VLFA brownout event detected—wake-up event and interrupt request active
3	LFA_BRNFLAG	R/-		VLFA brownout flag
			0	VLFA above brownout threshold $V_{BO,VLFA}$
			1	VLFA below brownout threshold $V_{BO,VLFA}$
2	LFA_BRNEN	R/W		VLFA brownout monitor enable
			0	VLFA brownout monitor disabled, no wake-up or interrupt request is generated
			1	VLFA brownout monitor enabled
1	LFA_IF_AGC2_RESET	R/W		Reset of the 2nd narrowband AGC stage; effects all three channels 1, 2, 3
			0	No reset, normal AGC function
			1	AGC reset to maximum gain (minimum attenuation), AGC function inhibited
0	LFA_IF_AGC1_RESET	R/W		Reset of the 1st narrowband AGC stage; effects all three channels 1, 2, 3
			0	No reset, normal AGC function
			1	AGC reset to maximum gain (minimum attenuation), AGC function inhibited

[1] LFA_BRNREG is one source of the LF active monitors interrupt flag IF_LFAMON, see Table 104.

Table 36. LF active control register 1, LFACON1 (reset value 2Bh)

Bit	Symbol	Access	Value	Description
7 to 0	LFACON1[7:0]	R/W		LFA active configuration register 1
			2Bh	Required setting for LF active operation

Bit	Symbol	Access	Value	Description
			all others	Reserved for device test

Table 37. LF active control register 2, LFACON2 (reset value A6h)

Bit	Symbol	Access	Value	Description
7 to 0	LFACON2[7:0]	R/W		LFA active configuration register 2
			A6h	Required setting for LF active operation
			all others	Reserved for device test

Table 38. LF active control register 4, LFACON4 (reset value A6h)

Bit	Symbol	Access	Value	Description
7 to 0	LFACON4[7:0]	R/W		LFA active configuration register 4
			A6h	Required setting for LF active operation
			all others	Reserved for device test

Table 39. LF active control register 5, LFACON5 (reset value AAh)

Bit	Symbol	Access	Value	Description
7 to 0	LFACON5[7:0]	R/W		LFA active configuration register 5
			AAh	Required setting for LF active operation
			all others	Reserved for device test

Table 40. LF active control register 6, LFACON6 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	LFA_EN_AGC_FASTDECAY	R/W		Enable the fast decay function for all AGCs
			0	Fast decay function disabled
			1	Fast decay function enabled—required setting for LF active operation
6	LFA_ISO_RELEASE	R/W		Set signal Isolation between VLFADIG and VBATREG supply domains
			0	Signal isolation active (signals blocked) - required setting, if VLFADIG supply is off or not yet settled
			1	Signal isolation released (signals propagated)
5	RDT	R/W0		Reserved for device test—must be set to 0 in the application
4	RDT	R/W0		Reserved for device test—must be set to 0 in the application
3 to 2	LFA_SET_XTAL_GM[1:0]	R/W		Set bias current for the 32 kHz crystal oscillator
			00	Standard bias current - recommended setting
			01	Doubled bias current

Bit	Symbol	Access	Value	Description
			10	Reserved for future use
			11	Reserved for future use
1	RDT	R/W0		Reserved for device test—must be set to 0 in the application
0	RDT	R/W0		Reserved for device test—must be set to 0 in the application

Table 41. LF active control register 7, LFACON7 (reset value xxxx_xx1xb)

Bit	Symbol	Access	Value	Description
7 to 5	RFU	-/W0		Reserved for future use
4 to 2	RDT	-/-		Reserved for device test
1	RDT	R/W1		Reserved for device test—must be set to 1 in the application
0	RDT	-/-		Reserved for device test

Table 42. LF active control register 8, LFACON8 (reset value 000x_xxxxb)

Bit	Symbol	Access	Value	Description
7 to 5	RDT	R/W		Reserved for device test—must be set to 100 in the application
4 to 3	RFU	-/W0		Reserved for future use
2 to 0	RDT	-/-		Reserved for device test

AGC reset

The frontend AGC and the two stages of the narrowband AGC can be reset manually by setting the bits LFA_RF_AGC_RESET, LFA_IF_AGC1_RESET and LFA_IF_AGC2_RESET to 1 for at least $t_{AGC\_SENSRST}$. After execution of the AGC reset, the receiver starts with the highest gain, i.e. at the sensitivity limit.

VLFA brownout monitor

When the VLFA brownout monitor is turned on, it monitors the supply voltage VLFA continuously and signals it status by bit LFA_BRNFLAG. When the supply VLFA drops below the threshold voltage $V_{BO,VLFA}$, the register bit LFA_BRNREG is set to 1 and acts as static device wake-up event from the POWER OFF state and as interrupt source for the LF active monitors interrupt. It is recommended that in case of VLFA brownout condition the application restarts the DC-DC converter and the LF-Active receiver. The bit LFA_BRNREG may be cleared by the application manually by writing a '1' to the respective bit position when the brownout condition is resolved, or automatically when the brownout detector is disabled.

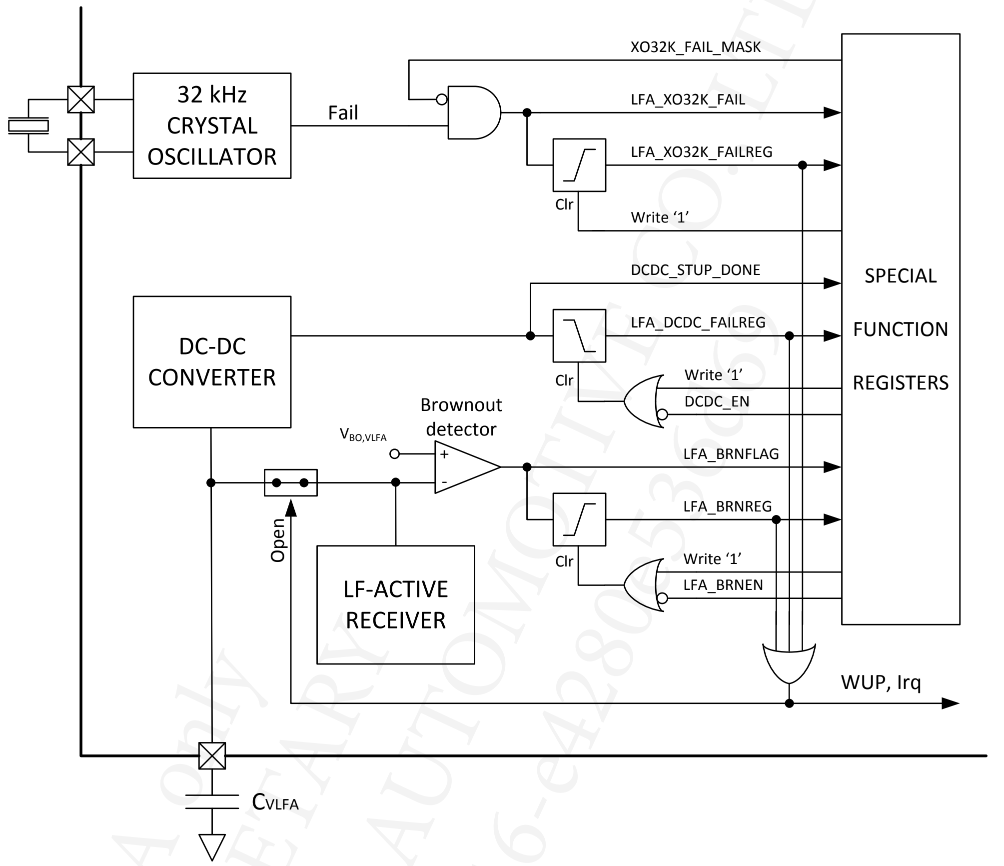


Figure 29. LF-Active monitors wake-up and interrupt generation logic

It is advised to enable the VLFA brownout monitor once the supply VLFA has settled (i.e. DCDC_STUP_DONE = 1, see Table 25). The brownout monitor is not intended to indicate the end of the VLFA start-up phase.

2.5.10.4 LF active status registers, LFASTATUS

The register LFASTATUS (Table 43) contains status information and interrupt registers of the LF active receiver infrastructure.

Table 43. LF active status register, LFASTATUS (reset value 0Xh)

Bit	Symbol	Access	Value	Description
7	LFA_DCDC_ FAILREG	R/W1->0		DC-DC converter fail wake-up and interrupt request register [1]
			0	No DC-DC converter fail detected—no wake-up event, no interrupt request
			1	DC-DC converter fail detected—wake-up event and interrupt request active
6	LFA_XO32K_ FAILREG	R/W1->0		32 kHz clock fail detector wake-up and interrupt request register [1]
			0	No 32 kHz clock fail detected—no wake-up event, no interrupt request

Bit	Symbol	Access	Value	Description
			1	32 kHz clock fail detected—wake-up event and interrupt request active
5	LFA_PLL_LD	R/-		Status of the LF active PLL lock detector
			0	LF active PLL not in lock
			1	LF active PLL locked
4	LFA_XO32K_FAIL	R/-		Status of the 32 kHz clock fail detector
			0	32 kHz clock is available
			1	32 kHz clock is not available
3 to 0	RFU	-/W0		Reserved for future use

[1] LFA_DCDC_FAILREG and LFA_XO32K_FAILREG are sources of the LF active monitors interrupt flag IF_LFAMON, see Table 104.

LFA_DCDC_FAILREG

Provided that the device is operated within specification, the operation of the DC-DC converter is guaranteed. However, improper programming could lead to DC-DC converter failure. Such a situation is when the internal oscillator of the DC-DC converter is selected (DCDC_CKSEL=10b) after the DC-DC converter has settled and entered steady-state operation (DCDC_STUP_DONE=1), in which case DCDC_STUP_DONE is cleared and regulation stops. A high to low transition of DCDC_STUP_DONE while the DC-DC converter is enabled sets bit LFA_DCDC_FAILREG, which in turn triggers the LFAMON interrupt / wake-up condition. In this case the application should restart the DC-DC converter and LF-Active receiver. LFA_DCDC_FAILREG will be cleared automatically when the DC-DC converter is disabled. Alternatively, application software can clear the bit by writing a '1' to the respective bit position.

LFA_XO32K_FAIL, LFA_XO32K_FAILREG

The 32 kHz crystal oscillator monitoring circuit is controlled via SFR bits LFA_EN_XTAL_32K_OK_FLAG and XO32K_FAIL_MASK, in registers LFAEN0 and PRECON2 respectively. Bit LFA_XO32K_FAIL, when not masked, reflects the current status of the crystal oscillator circuit. A low-to-high transition of this bit sets the persistent bit LFA_XO32K_FAILREG, which in turn triggers the LFAMON interrupt / wake-up condition. It is recommended that in this case the application restarts the entire LF-Active interface, including oscillator circuit, DC-DC converter and LF-Active receiver. Once the condition is resolved, LFA_XO32K_FAILREG is cleared by writing a '1' to the respective bit position.

It is advised that once the oscillator monitoring circuit is enabled, its output is masked for time $t_{XO32KFAIL\_set}$, in order to avoid spurious interrupts during its settling.

It is possible that in some cases a crystal oscillator or DC-DC converter failure might lead to overvoltage at VLFA. For this reason, once an LFA monitor condition is detected, the LF-Active receiver supply is isolated from the DC-DC converter output and the VLFA pin. VLFA will be actively discharged when the DC-DC converter is disabled, during the restart procedure.

2.5.10.5 LF active sensitivity register, LFASENSE

The register LFASENSE (Table 44) is required to set the LF active receiver gain and sensitivity.

Table 44. LF active sensitivity register, LFASENSE (reset value 00h)

Bit	Symbol	Access	Value	Description
7	LFA_SET_SENSE_ MODE[7:0]	R/W		LF active receiver gain mode setting
			01h	Desensitization setting D2C
			03h	Desensitization setting D1C
			29h	Gain mode setting G0C
			4Fh	Gain mode setting G1M
			9Bh	Gain mode setting G2C
			BFh	Gain mode setting G3M
			all other	Reserved for future use

2.5.10.6 Preprocessor data register PREDAT

The preprocessor data register provides access to a data byte received via the active interface, Table 45.

Table 45. Preprocessor data register PREDAT (reset value xxh)

Bit	Symbol	Access	Value	Description
7 to 0	PREDATA[7:0]	R/-		Preprocessor data byte

2.5.10.7 Preprocessor control register PRECON2

The preprocessor control register PRECON2 is shown in Table 46.

Table 46. Preprocessor control register PRECON2 (reset value x1xx_xx01b)

Bit	Symbol	Access	Value	Description
7	RFU	-/W0		Reserved for future use
6	PRERST	R/W		Preprocessor reset
			0	No reset
			1	The preprocessor is reset and disabled; all status bits in register PRESTAT are reset
5 to 2	RFU	-/W0		Reserved for future use
1	RINMODE	R/W		Automated disable of the LF Active circuit in IMMO mode
			0	LF Active connected to INxP/INxN pins in IMMO mode
			1	LF Active automatically disconnected in IMMO mode
0	XO32K_FAIL_MASK	R/W		Mask the output of the 32 kHz clock fail detector
			0	Do not mask the output of the 32 kHz clock fail detector
			1	Mask the output of the 32 kHz clock fail detector: LFA_XO32K_FAIL = 0

RINMODE, LF Active loading LF pins control bits

The device is equipped with an optional feature of automated LF Active circuit disconnection during IMMO mode. By means of RINMODE, it is defined whether this feature is enabled or not. When the bit is set to 1, the frontend AGC of the LF Active circuit is turned off and the Q factor adjustment is disconnected from the LF pins actively,

which allows for more efficient LF field energy consumption by minimized leakage current flowing into the LF Active circuit when LF passive circuit is to be supplied.

2.5.10.8 Preprocessor control registers PRECON3 to 5

The preprocessor control registers PRECON3, PRECON4 and PRECON5, which are related to channel 1, 2 and 3, respectively, are shown in Table 47

Table 47. Preprocessor control register PRECON3, 4 and 5 (reset value 0x00_0000b)

Bit	Symbol	Access	Value	Description
7 to 6	RFU	-/W0		Reserved for future use
5	QFACTx[5]	R/W		Q-factor adjustment of channel x receiver coil via resistor R6Qx
			0	Disable R6Qx
			1	Activate R6Qx
4	QFACTx[4]	R/W		Q-factor adjustment of channel x receiver coil via resistor R5Qx
			0	Disable R5Qx
			1	Activate R5Qx
3	QFACTx[3]	R/W		Q-factor adjustment of channel x receiver coil via resistor R4Qx
			0	Disable R4Qx
			1	Activate R4Qx
2	QFACTx[2]	R/W		Q-factor adjustment of channel x receiver coil via resistor R3Qx
			0	Disable R3Qx
			1	Activate R3Qx
1	QFACTx[1]	R/W		Q-factor adjustment of channel x receiver coil via resistor R2Qx
			0	Disable R2Qx
			1	Activate R2Qx
0	QFACTx[0]	R/W		Q-factor adjustment of channel x receiver coil via resistor R1Qx
			0	Disable R1Qx
			1	Activate R1Qx

QFACTx[5:0], Q-factor adjustment of receiver coil in channel x

With QFACTx[5:0] the Q-factor of the receiver coil in channel x is adjusted by loading the coil with different resistances. For this, six resistors are provided in parallel (R1Qx to R6Qx) which can be activated each on demand. This allows to use different coils for the respective 3D LF channel.

2.5.10.9 Wake-up receiver control register WUPCON

The wake-up receiver control register WUPCON is shown in Table 48.

Table 48. Wake-up receiver control register WUPCON (reset value X000h)

Bit	Symbol	Access	Value	Description
15 to 12	RFU	-/W0		Reserved for future use
11 to 8	SCM_CFG[3:0]	R/W		Strict correlation mode configuration

Bit	Symbol	Access	Value	Description
			9h	Highest false wake-up rate reduction
			Ah	High false wake-up rate reduction
			5h	Moderate false wake-up rate reduction
			0h	Strict correlation mode disabled
			all others	Reserved for future use
7 to 6	WUPPAT_SEL[1:0]	R/W		Wake-up pattern selector
			00	Select wake-up pattern A
			01	Select wake-up pattern B
			10	Select wake-up pattern C
			11	Reserved for future use
5	WUPRX_EN_PAYLOAD	R/W		Enables the data flow between the wake-up receiver and the payload receiver.
			0	Payload receiver input muted
			1	Payload receiver input enabled
4	EN_CORR	R/W		Enable the wake-up receiver
			0	Wake-up receiver disabled
			1	Wake-up receiver enabled
3	EN_WUPC	R/W		Enable wake-up pattern C detection
			0	Pattern C detection disabled
			1	Pattern C detection enabled
2	EN_WUPB	R/W		Enable wake-up pattern B detection
			0	Pattern B detection disabled
			1	Pattern B detection enabled
1	EN_WUPA	R/W		Enable wake-up pattern A detection
			0	Pattern A detection disabled
			1	Pattern A detection enabled
0	RDT	R/W0		Reserved for device test—must be set to 0 in the application

SCM_CFG[3:0]

The strict correlation mode can be used to reduce the false wake-up rate when a short wake-up pattern is selected. The bit field SCM_CFG adjusts the trade-off between false wake-up rate and sensitivity of the strict correlation mode. With setting 9h, maximum false wake-up rate reduction can be achieved, at the cost of a modest sensitivity loss. With settings Ah and 5h, progressively more moderate false wake-up rate reduction is achieved, with respectively smaller sensitivity loss. Other values are invalid. This configuration applies to those wake-up patterns for which strict correlation mode is enabled with EN_STRICT_CORR = 1. If strict correlation mode is not enabled for any pattern, the value of SCM_CFG is ignored.

WUPPAT_SEL[1:0]

Pattern-specific configuration for wake-up patterns A, B and C is overlaid onto the same memory addresses (registers WUPPATEVNx, WUPPATODDx and WUPPATCON, which are shared by all patterns). On a shared register write, WUPPAT_SEL demultiplexes the byte(s) written to the appropriate pattern-specific physical register. On a shared register read, WUPPAT_SEL multiplexes the byte(s) read from the appropriate pattern-specific physical register.

WUPRX_EN_PAYLOAD

Gates the data flow between the wake-up receiver and the payload receiver, in order to save current when the payload receiver is not in use. Set this bit to '1' as part of the standard LF active startup procedure.

EN_CORR, EN_WUPA, EN_WUPB, EN_WUPC

The bit EN_CORR enables the wake-up pattern detection. When set to 1, all wake-up patterns enabled via the bits are EN_WUPA, EN_WUPB and EN_WUPC are correlated in parallel with the incoming signal.

2.5.10.10 Wake-up pattern configuration registers WUPPATEVENx, WUPPATODDx, WUPPATCON

The registers WUPPATEVN0 (Table 49), WUPPATEVN1 (Table 50), WUPPATEVN2 (Table 51), WUPPATODD0 (Table 52), WUPPATODD1 (Table 53), WUPPATODD2 (Table 54) and WUPPATCON (Table 55) store the individual configuration of the wake-up patterns A, B and C. These registers have a common address for all three wake-up patterns and bit field WUPPAT_SEL (see Table 48) must be used to select the read/write access to/from the wanted wake-up pattern.

Table 49. Wake-up pattern even-chip configuration register WUPPATEVN0 (reset value: XXXXh)

Bit	Symbol	Access	Value	Description
15 to 0	WUPPATEVN0[15:0]	R/W		Wake-up reference pattern bits 15 to 0 (even chips)

Table 50. Wake-up pattern even-chip configuration register WUPPATEVN1 (reset value: XXXXh)

Bit	Symbol	Access	Value	Description
15 to 0	WUPPATEVN1[15:0]	R/W		Wake-up reference pattern bits 31 to 16 (even chips)

Table 51. Wake-up pattern even-chip configuration register WUPPATEVN2 (reset value: XXXXh)

Bit	Symbol	Access	Value	Description
15 to 9	RFU	-/W0		Reserved for future use
8 to 0	WUPPATEVN2[8:0]	R/W		Wake-up reference pattern bits 40 to 32 (even chips)

Table 52. Wake-up pattern odd-chip configuration register WUPPATODD0 (reset value: XXXXh)

Bit	Symbol	Access	Value	Description
15 to 0	WUPPATODD0[15:0]	R/W		Wake-up reference pattern bits 15 to 0 (odd chips)

Table 53. Wake-up pattern odd-chip configuration register WUPPATODD1 (reset value: XXXXh)

Bit	Symbol	Access	Value	Description
15 to 0	WUPPATODD1[15:0]	R/W		Wake-up reference pattern bits 31 to 16 (odd chips)

Table 54. Wake-up pattern odd-chip configuration register WUPPATODD2 (reset value: XXXXh)

Bit	Symbol	Access	Value	Description
15 to 9	RFU	-/W0		Reserved for future use
8 to 0	WUPPATODD2[8:0]	R/W		Wake-up reference pattern bits 40 to 32 (odd chips)

Table 55. Wake-up pattern control register WUPPATCON (reset value 0000h)

Bit	Symbol	Access	Value	Description
15 to 12	CV2LEN[3:0]	R/W		Length of CV2 sequence (part of the code violation sequence used for matching), in bits
			0d - 9d	CV2 length in number of bits
			10d - 15d	Reserved for future use
11	MMF	R/W		Select the matched filter setting
			0	Reserved for future use
			1	Manchester matched filter is used
10 to 8	ERRTOL[2:0]	R/W		Error tolerance level
			0d	Error tolerance disabled
			1d - 7d	Error tolerance enabled for up to ERRTOL bit-match errors
7	EN_STRICT_CORR	R/W		Enable strict correlation mode
			0	Strict correlation mode not enabled, normal correlation applied, SCM_CFG is ignored
			1	Strict correlation mode enabled
6	EN_SEG_CORR	R/W		Enable segmented correlation
			0	Non-segmented correlation applied
			1	Segmented correlation applied
5 to 0	WUPLEN[5:0]	R/W		Length of the Manchester-coded wake-up pattern, in bits
			0d - 32d	Wake-up pattern length in number of bits
			33d - 63d	Reserved for future use

CV2LEN[3:0]

The code violation (CV) pattern in the input signal may be divided in two parts: CV1, the first part, which is not used for pattern matching but together with the run-in bits for the receiver settling (see Figure 22), and CV2, the second part, used for pattern matching. CV2LEN specifies the length of the second part, in bit periods.

ERRTOL[2:0], error tolerance

Specifies the maximum number of bit-match errors that will still flag a pattern match and will trigger a wake-up event. When ERRTOL = 0, no errors are accepted and full correlation is used instead. Increasing level of error tolerance improves sensitivity at the expense of increased false wake-up rate and sensitivity to wake-up patterns that deviate by the specified number of tolerated bits.

EN_STRICT_CORR

Enables the strict correlation mode for wake-up pattern A, B, or C. The common parameter SCM_CFG (see Table 48) applies to all wake-up patterns for which EN_STRICT_CORR is set. Note that strict correlation mode should not be enabled at the same time as error tolerance or segmented correlation for the same wake-up pattern.

EN_SEG_CORR

Enables segmented correlation for wake-up pattern A, B, or C. This option achieves better sensitivity in the presence of large date rate offsets ΔT, at the expense of increased false wake-up rate.

WUPLEN[5:0]

This bit field specifies the number of Manchester-coded bits in the wake-up pattern. The maximum allowable value is limited by the 41 bits total processed by the wake-up receiver and the programmed value of CV2 length. There is no hard limit on the minimum valid value, even though in practice a minimum number of Manchester-coded bits will be necessary, based on code-space and false-wake-up rate considerations.

Wake-up pattern programming

The wake-up correlator and the respective registers allow up to 41 bits (82 chips) of combined Manchester bits and code violation (CV) pattern. Both CV and Manchester chips must be programmed into the WUPPAT{EVN,ODD}{2,1,0} registers, as described below. The CV pattern must be the legacy code violation sequence— M0S0MSMS0 in Manchester notation—according to Figure 21.

Patterns are right-aligned within the WUP pattern registers, meaning that if in total fewer than 82 chips are programmed, the upper part of WUPPAT{EVN,ODD}2 (and possibly WUPPAT{EVN,ODD}1) remains unused.

With all data transmitted from the base-station side in big-endian order (most significant bit first), the CV pattern corresponds to the most significant used positions of the pattern registers WUPPAT{EVN,ODD}{2,1,0}, while the last transmitted bit of the Manchester-coded pattern corresponds to the least significant bits of WUPPAT{EVN,ODD}0. For an N-bit (2*N-chip) combined CV+Manchester wake-up pattern, individual chips may be numbered 2*N-1 to 0, meaning that the first CV chip falls into an odd register and the last Manchester chip into an even register (specifically, bit WUPPATEVN0[0]).

The following example illustrates pattern programming in case of a 24-bit Manchester pattern and 4 CV bits used in correlation (CV = CV1+CV2 = 5+4):

- The Manchester-coded pattern, b_{23} to b_0, is programmed into registers {WUPPATEVN1[7:0], WUPPATEVN0[15:0]}. The respective bits of the ODD registers do not need to be programmed.

- The CV pattern spelled out in chips is 11-10-00-10-11-00-11-00-10. Of these, the last 4 bit periods, 00-11-00-10 are significant for the correlation and must be programmed into the pattern registers. Separating even from odd chips, we program:
  - Chips 0100 into register WUPPATEVN1[11:8]
  - Chips 0101 into register WUPPATODD1[11:8]
- In this example, registers WUPPAT{EVN,ODD}2, as well as register bits WUPPAT{EVN,ODD}1[15:12] are not used and are left unprogrammed.

Figure 30 illustrates this programming example, where the 24-bit Manchester wake-up pattern is CF00F0h.

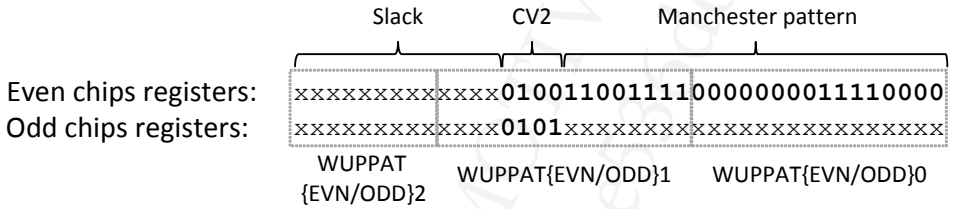


Figure 30. Wake-up pattern programming example

2.5.10.11 Payload receiver control register PAYRXCON

The preprocessor status register contains status information of the preprocessor block in order to detect e.g. matching wake-up patterns. After a battery insertion and when the CPU resets the preprocessor (by setting PRERST and ITRST) the status bits are cleared.

Table 56. Payload receiver control register PAYRXCON (reset value xxxx_xx00_1001_1111b)

Bit	Symbol	Access	Value	Description
15 to 10	RDT	-/-		Reserved for device test
9	RDT	R/W0		Reserved for device test—must be set to 0 in the application
8	RESTARTONWUP	R/W		Enable the restart-on-WUP function
			0	Function disabled, a wake-up pattern detected during payload reception will be ignored
			1	Function enabled, a wake-up pattern (including CV) detected during payload reception will abort the current payload reception and restart data reception immediately after the end of the wake-up pattern.
7 to 5	RDT	R/W		Reserved for device test—must be set to 100 in the application
4	WUPRXSELC	R/W		Enable payload reception for wake-up pattern C
			0	No payload reception will be performed for pattern C
			1	Payload reception will be performed for pattern C
3	WUPRXSELB	R/W		Enable payload reception for wake-up pattern B
			0	No payload reception will be performed for pattern B
			1	Payload reception will be performed for pattern B

Bit	Symbol	Access	Value	Description
2	WUPRXSELA	R/W		Enable payload reception for wake-up pattern A
			0	No payload reception will be performed for pattern A
			1	Payload reception will be performed for pattern A
1 to o	RDT	R/W		Reserved for device test—must be set to 11 in the application

WUPRXSELC, WUPRXSELB, WUPRXSELA

Enable payload reception for each wake-up pattern individually.

When the LF protocol ensures that a certain wake-up pattern is not followed by a payload, it is beneficial to clear the corresponding enable bit for the payload receiver. In this way, unnecessary activity is avoided and the application software does not need to act, in order to stop the payload receiver from receiving data that is anyway not valid.

2.5.10.12 Preprocessor status register PRESTAT

The preprocessor status register contains status information of the preprocessor block in order to detect e.g. matching wake-up patterns. After a battery insertion and when the CPU resets the preprocessor (by setting PRERST and ITRST) the status bits are cleared.

The preprocessor status register provides byte and word access.

Table 57. Word and byte access to the status register PRESTAT

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
PRESTAT	PRESTATH	PRESTATL

The specific status bits are cleared by writing a ‘1’, while writing a ‘0’ leaves the corresponding bit unchanged. For example, writing data = 01h, bit 0 of the status register is cleared.

Table 58. Preprocessor status register PRESTAT (reset value X0X0h)

Bit	Symbol	Access	Value	Description
15	STOPRX	R/W		Stop the payload receiver
			0	Do not change the status of the payload receiver
			1	Stop the payload receiver
14	MODE	R/-		Get payload receiver status
			0	Payload receiver is idle
			1	Payload receiver is detecting data bytes
13	RTC_WUP_OVF	R/-		Real-time clock wake-up overflow flag
			0	No real-time clock wake-up detected while RTC_WUP was set
			1	New real-time clock wake-up detected when RTC_WUP was set
12	RFU	-/W0		Reserved for future use
11	NEWBYTE_OVF	R/W1		New byte overflow
			0	No new byte received while NEWBYTE was set

Bit	Symbol	Access	Value	Description
			1	New byte received while preprocessor data buffer is full
10	WUPCMH	R/-		Wake-up pattern C matching history flag
			0	Wake-up pattern did not match reference pattern C before
			1	Wake-up pattern did match reference pattern C before
9	WUPBMH	R/-		Wake-up pattern B matching history flag
			0	Wake-up pattern did not match reference pattern B before
			1	Wake-up pattern did match reference pattern B before
8	WUPAMH	R/-		Wake-up pattern A matching history flag
			0	Wake-up pattern did not match reference pattern A before
			1	Wake-up pattern did match reference pattern A before
7	RFU	-/W0		Reserved for future use
6	IT_WUP	R/W1->0		Interval timer wake-up
			0	No wake-up event
			1	Wake-up event
5	RTC_WUP	R/W1->0		Real-time clock timer wake-up
			0	No wake-up event
			1	Wake-up event
4	RFU	-/-		Reserved for future use
3	NEWBYTE	R/W1->0		New data byte received
			0	No new data byte received
			1	New data byte received
2	WUPCM	R/W1->0		Wake-up pattern C matching flag
			0	Wake-up pattern does not match reference pattern C
			1	Wake-up pattern matches reference pattern C
1	WUPBM	R/W1->0		Wake-up pattern B matching flag
			0	Wake-up pattern does not match reference pattern B
			1	Wake-up pattern matches reference pattern B
0	WUPAM	R/W1->0		Wake-up pattern A matching flag
			0	Wake-up pattern does not match reference pattern A
			1	Wake-up pattern matches reference pattern A

Remark: Register bits RTC_WUP_OVF, IT_WUP and RTC_WUP are sources for the CPU interrupt controller’s interval timer and real-time clock interrupt, flag IF_IT. Register bits NEWBYTE_OVF, WUPxMH, NEWBYTE, WUPxM are sources for the CPU interrupt controller’s LF active preprocessor interrupt, flag IF_PP. Only register bits RTC_WUP_OVF, WUPxMH, IT_WUP, RTC_WUP and WUPxM are wake-up sources for the power management block.

STOPRX, stop the payload receiver

STOPRX is used by the application software to signal to the payload receiver that sufficient data bytes have been received. Setting this bit to 1 causes the payload receiver to return to idle state (MODE = 0), at which time the bit STOPRX is auto-cleared.

A minimum duration of one cycle of the 32 kHz crystal oscillator is required between the CPU wake-up event and the STOPRX command.

RTC_WUP_OVF, real-time clock timer wake-up overflow flag

The real-time clock wake-up overflow flag is cleared automatically when bit RTC_WUP is cleared. Separate clearing of RTC_WUP_OVF is not supported. Entering POWER OFF state is only possible when this bit is cleared.

NEWBYTE_OVF, new byte overflow flag

When a new byte is received, NEWBYTE is set and an interrupt is generated. NEWBYTE_OVF is set whenever a new byte is received and NEWBYTE was already set, a condition indicating an overflow.

The two flags are cleared when the CPU writes a 1 to the respective bit position. (Note that this is unlike the WUPxM/MH flags). A wake-up event clears both bits automatically.

WUPxM, WUPxMH, wake-up pattern x matching (history) flag

The wake-up pattern matching flags WUPxM represent the status of the last detected wake-up pattern. The corresponding history flags WUPxMH accumulate the status of all detected wake-up patterns, which were not yet processed. The following conditions cause an update of the wake-up and wake-up history flags.

1. A new wake-up pattern match is detected:
   If a wake-up pattern match is detected while the payload receiver is active and RESTARTONWUP = 0, the event is ignored and no flag update takes place. If RESTARTONWUP = 1, the corresponding wake-up flag WUPxM is set. All other wake-up flags are cleared. If more than one wake-up pattern matches at the same time all corresponding wake-up flags WUPxM are set.
   At the same time, if the payload receiver was idle, a pending 1 in a wake-up flag WUPxM is transferred into the corresponding wake-up history flag WUPxMH. A pending 0 in a wake-up flag does not influence the state of the history flag, i.e. once a history flag is 1 it maintains its state. In case the payload receiver was active when the WUP pattern was detected, WUPxMH flags remain unaffected.
2. A positive edge of the power-on reset of the micro-controller (VDDPOR) is detected:
   Any pending wake-up pattern match event is transferred into the corresponding history flag and all wake-up pattern match flags are cleared; i.e. if WUPxM = 1, the corresponding wake-up pattern history flag WUPxMH will be set. This event does not clear any wake-up pattern history flag WUPxMH
   This mechanism is intended for applications, which cannot be interrupted by a pattern matching event. If this application finishes with a reset of the micro controller the device boots again. The application can then decide whether to process or discard any old wake-up matching events.
3. The wake-up flags and their corresponding history flags can be cleared by writing a 1 to the wake-up flag WUPxM. The different wake-up flags (WUPAM, WUPBM, WUPCM) can be cleared separately. Clearing WUPxM automatically clears WUPxMH as well. Disjoint clearing of the wake-up flag and the corresponding wake-up history flag is not supported.

If any of the flags WUPxM or WUPxMH is ‘1’, an interrupt and a wake-up request for the power management is generated. Entering POWER OFF state is only possible when these bits are cleared.

IT_WUP, interval timer wake-up

An interrupt request is generated when a periodical wake-up occurs. The period of the wake-up signal is defined by IT_SEL[2:0]. Once this bit is set, it remains ‘1’ until it is cleared by the application. Entering POWER OFF state is only possible when this bit is cleared.

RTC_WUP, real-time clock wake-up

An interrupt request is generated when there is a wake-up caused by the real-time clock. The period of the wake-up is selected by RTC_SEL[1:0]. Once this bit is set, it remains ‘1’ until it is cleared by the application. Entering POWER OFF state is only possible when this bit is cleared.

NEWBYTE, new data byte received

This bit is set and an interrupt request is generated when a new data byte is received. Once this bit is set, it remains ‘1’ until it is cleared by the application. Moreover, this bit is cleared automatically by any subsequent wake-up match.

2.5.10.13 RSSI control register 0 to 2, RSSICON0, RSSICON1, RSSICON2

The analog frontend of the RSSI block is controlled via the RSSI control registers RSSICON0 (see Table 59), RSSICON1 (see Table 60) and RSSICON2 (see Table 61).

Table 59. RSSI control register 0 RSSICON0 (reset value 0000h)

Bit	Symbol	Access	Value	Description
15 to 13	RSSI_CHANSEL	R/W		RSSI channel selection
			000	No channel selected
			001	Channel 1 selected
			010	Channel 2 selected
			011	Summation of channel 1 and channel 2 selected
			100	Channel 3 selected
			101	Summation of channel 1 and channel 3 selected
			110	Summation of channel 2 and channel 3 selected
			111	Summation of channel 1, channel 2 and channel 3 selected
12	RFU	-/-		Reserved for future use
11 to 9	RSSI_RANGE[2:0]	R/W		RSSI range selection
			000	Range -18 dB
			001	Range -18 dB
			010	Range 0 dB
			011	Range +18 dB
			100	Range +36 dB
			101	Reserved for future use

Bit	Symbol	Access	Value	Description
			110	Reserved for future use
			111	SD-ADC input termination
8	RDT	R/W0		Reserved for device test – must be set to 0 in the application
7	RSSI_PON	R/W		RSSI power on
			0	RSSI block turned off
			1	RSSI block turned on
6 to 4	RFU	-/W0		Reserved for future use
3 to 1	RSSI_OVF[2:0]	R/W		RSSI range overflow
			000	Input signal out of measurement range
			001	Range 0 dB overflow, if RSSI_RANGE ≥ 010 Range -18 dB overflow, if RSSI_RANGE ≤ 001
			010	Range 18 dB overflow
			011	Range 36 dB overflow
			100	No overflow
			101 - 111	Reserved for future use
0	RSSI_RST	R/W		RSSI range / overflow detector reset
			0	No effect
			1	Reset range indication / overflow detection signal information

Table 60. RSSI control register 1 RSSICON1 (reset value 77h)

Bit	Symbol	Access	Value	Description
7 to 4	RSSI_OVF18DB_LVL	R/W		Select level for the +18 dB range overflow detector
			3d	Optional setting for the range detection phase, if a 62.5 kHz interferer is expected; more dynamic range for the range detection phase, but reduced dynamic range during the measurement
			8d	Standard setting for the range detection phase; optimum dynamic range during the measurement
			12d	Standard setting for range overflow detection during the measurement
			all others	Reserved
3 to 0	RSSI_OVF0DB_LVL	R/W		Select level for the +0 dB range overflow detector
			3d	Optional setting for the range detection phase, if a 62.5 kHz interferer is expected; more dynamic range for the range detection phase, but reduced dynamic range during the measurement
			8d	Standard setting for the range detection phase; optimum dynamic range during the measurement
			12d	Standard setting for range overflow detection during the measurement

Bit	Symbol	Access	Value	Description
			all others	Reserved

Table 61. RSSI control register 2 RSSICON2 (reset value 07h)

Bit	Symbol	Access	Value	Description
7	RSSI_RVV_INTEN	R/W		Enable interrupt on RSSI raw value valid condition
			0	No interrupt generated if RSSI_RAWVAL_VALID is set
			1	Interrupt is generated if RSSI_RAWVAL_VALID
6 to 4	RDT	-/-		Reserved for device test
3 to 0	RSSI_OVF36DB_LVL	R/W		Select level for the +36 dB range overflow detector
			3d	Optional setting for the range detection phase, if a 62.5 kHz interferer is expected; more dynamic range for the range detection phase, but reduced dynamic range during the measurement
			8d	Standard setting for the range detection phase; optimum dynamic range during the measurement
			12d	Standard setting for range overflow detection during the measurement
			all others	Reserved

RSSI_OVF[2:0], RSSI range overflow

An RSSI range overflow is encoded in the RSSI_OVF[2:0] register. The bits represent overflows in the respective RSSI measurement ranges. A value of '000' indicates an input signal that is higher than the dynamic range of the RSSI amplifier chain.

RSSI_RVV_INTEN

Setting this bit to 1 enables generation of the RSSI interrupt IF_RSSI (see Table 103), every time a raw RSSI measurement is available, as indicated by bit RSSI_RAWVAL_VALID in register RSSICON7. Note that for the interrupt to propagate to the CPU, bit IE_RSSI (see Table 98) must also be set. When RSSI_RVV_INTEN is cleared, no interrupt is generated but RSSI_RAWVAL_VALID still indicates availability of a raw measurement.

2.5.10.14 RSSI control register 3 to 5, RSSICON3, RSSICON4, RSSICON5

The digital part of the RSSI block and the SD-ADC is controlled via the RSSI control registers RSSICON3 (see Table 62), RSSICON4 (see Table 63), and RSSICON5 (see Table 64). Registers RSSICON3 and RSSICON4 shall not be altered when the digital RSSI processing is running.

Table 62. RSSI control register 3 RSSICON3 (reset value 0011_x001b)

Bit	Symbol	Access	Value	Description
7	RDT	-/W0		Reserved for device test—must be set to 0 in the application
6 to 4	RSSI_FILT_CFG[2:0]	R/W		Digital RSSI filter selection
			0d	Filter setting A, $B_{RSSI\_FILT\_A}$

Bit	Symbol	Access	Value	Description
			4d	Filter setting B, $B_{RSSI\_FILT\_B}$
			3d	Filter setting C, $B_{RSSI\_FILT\_C}$
			7d	Filter setting D, $B_{RSSI\_FILT\_D}$
			all others	Reserved for future use
3	SDADC_OVERLOAD	R/-		SD-ADC overload flag
			0	No SD-ADC overload condition
			1	SD-ADC overload condition detected
2 to 0	SDADC_OVL_ CFG[2:0]	R/W		Configuration of the SD-ADC overload detector
			001	Recommended setting for the application
			all others	Reserved for device test

Table 63. RSSI control register 4 RSSICON4 (reset value 1Fh)

Bit	Symbol	Access	Value	Description
7 to 0	RSSI_AVG_CFG[7:0]	R/W		RSSI average configuration
			0d - 255d	RSSI_AVG_CFG + 1 raw values are averaged per result

Table 64. RSSI control register 5 RSSICON5 (reset value 08h)

Bit	Symbol	Access	Value	Description
7 to 6	RFU	-/W0		Reserved for future use
5	RSSI_OSC_ CALDONE	R/W1->0		SD-ADC precision oscillator calibration done flag
			0	Calibration not finished
			1	Calibration finished
4	RSSI_OSC_ CALSTART	R/W		Start of the SD-ADC precision oscillator calibration sequence
			0	W: Stop the calibration sequence; R: Calibration sequence not running
			1	W: Start the calibration sequence; R: Calibration sequence is running
3	RDT	R/W1		Reserved for device test—must be set to 1 in the application
2	RSSI_OSC_EN	R/W		SD-ADC precision oscillator enable
			0	Precision oscillator off, SDADCCLK not available
			1	Precision oscillator on, SDADCCLK available
1	RFU	-/W0		Reserved for future use
0	RSSI_LDO_EN	R/W		Regulator enable for the VSDADC supply
			0	Regulator disabled, VSDADC off
			1	Regulator enabled, VSDADC on

RSSI filter and averaging selection

RSSI_AVG_CFG determines how many raw values are averaged in order to generate one complete RSSI measurement. The number of raw values used is equal to RSSI_AVG_CFG + 1, so a range from 1 to 256 raw values can be specified. Higher values give more stable RSSI readings.

The digital processing time t_{RSSI_DIG} determines the time for one RSSI measurement sequence (RSSI_START = 1, see Table 65). This time depends on the digital filter setting time $t_{RSSI\_FILT\_x}$ (i.e. $t_{RSSI\_FILT\_A}$, $t_{RSSI\_FILT\_B}$, $t_{RSSI\_FILT\_C}$ or $t_{RSSI\_FILT\_D}$) and the number of averages and is calculated according to Equation 7.

$$t_{RSSI\_DIG} = t_{RSSI\_FILT\_x} + \text{RSSI\_AVG\_CFG} \cdot t_{RSSI\_DIGPROC} \quad (7)$$

2.5.10.15 RSSI control register 7 and RSSI value register, RSSICON7, RSSIVAL

Register RSSICON7 (see Table 65) controls the execution of the RSSI measurement. Every RSSI measurement delivers different results, which can be read via register RSSIVAL (see Table 66).

Table 65. RSSI control register 7 RSSICON7 (reset value 00h)

Bit	Symbol	Access	Value	Description
7 to 5	RSSI_VAL_SEL[2:0]	R/W		Select which value can be read from register RSSIVAL
			000	RSSI_AVG—average of raw measurements
			001	RSSI_QMEAN—quadratic mean of raw measurements
			010	RSSI_MIN—minimum raw measurement
			011	RSSI_MAX—maximum raw measurement
			100	RSSI_RAW—raw measurement result
			101	RSSI_FREQ_OFFSET—estimate for carrier frequency offset
			110	Reserved for device test
			111	Reserved for future use
4	RSSI_VALID	R/W1->0		New RSSI measurement result available [1]
			0	No new result available
			1	New result is available
3	RSSI_RAW_VALID	R/W1->0		New raw RSSI value available [1]
			0	No new raw value available
			1	New raw value is available
2	RSSI_BUSY	R/-		RSSI busy indicator
			0	No RSSI measurement running
			1	RSSI measurement running
1	SDADC_ENABLE	R/W		SD-ADC enable
			0	SD-ADC is powered down
			1	SD-ADC is enabled
0	RSSI_START	R/W		Start RSSI measurement sequence

Bit	Symbol	Access	Value	Description
			0	No RSSI measurement requested
			1	RSSI measurement sequence started

[1] This flag is one source of the RSSI interrupt flag IF_RSSI, see Table 103.

Table 66. RSSI value register RSSIVAL (reset value XXXXh)

Bit	Symbol	Access	Value	Description
RSSI_VAL_SEL = 000				
15 to 0	RSSI_AVG[15:0]	R/-		RSSI_AVG—average of raw measurements
RSSI_VAL_SEL = 001				
15 to 0	RSSI_QMEAN[15:0]	R/-		RSSI_QMEAN—quadratic mean of raw measurements
RSSI_VAL_SEL = 010				
15 to 0	RSSI_MIN[15:0]	R/-		RSSI_MIN—minimum raw measurement
RSSI_VAL_SEL = 011				
15 to 0	RSSI_MAX[15:0]	R/-		RSSI_MAX—maximum raw measurement
RSSI_VAL_SEL = 100				
15 to 0	RSSI_RAW[15:0]	R/-		RSSI_RAW—raw measurement result
RSSI_VAL_SEL = 101				
15 to 9	RFU	-/-		Reserved for future use
8	RSSI_FREQ_ERR	R/-		RSSI offset frequency estimation error flag
			0	RSSI_FREQ_OFFSET is valid
			1	RSSI_FREQ_OFFSET in not valid and must be discarded
7 to 0	RSSI_FREQ_OFFSET[7:0]	R/-		RSSI_FREQ_OFFSET—estimate for carrier frequency offset from nominal carrier frequency $f_{CARR,nom}$ Signed value in two's complement notation, 1 LSB equals approximately 122 Hz

RSSI_VAL_SEL[2:0]

This bit field selects between the different results after every RSSI measurement (or during RSSI measurement, in case of raw values). RSSI_VAL_SEL can be changed after a measurement sequence is finished, so all different results relating to a single measurement sequence can be retrieved.

RSSI_VALID

Indicates that an RSSI measurement sequence has completed and the values RSSI_AVG, RSSI_QMEAN, RSSI_MIN, RSSI_MAX, RSSI_FREQ_OFFSET and RSSI_FREQ_ERR are available. RSSI_VALID is one static source of the RSSI interrupt flag IF_RSSI (see Table 103).The application software is responsible for clearing RSSI_VALID by writing a 1 to the respective bit position.

RSSI_RAWVAL_VALID

Indicates that a raw RSSI measurement is available to be retrieved via register RSSIVAL (RSSI_VAL_SEL = 100). The application software is responsible for clearing RSSI_RAWVAL_VALID by writing a 1 to the respective bit position.

Given that a raw measurement is completed after every $t_{RSSI\_DIGPROC}$, the application software has a limited amount of time to read out each raw measurement. If a raw measurement result is not read in time, it is overwritten by the next one and bit RSSI_RAWVAL_VALID remains set. There is no overflow indication to software.

RSSI_RAWVAL_VALID is one static source of the RSSI interrupt flag IF_RSSI (see Table 103), provided this interrupt source is enabled via bit RSSI_RVV_INTEN in register RSSICON2 (see Table 61).

RSSI_BUSY

When set, this bit indicates that the RSSI block is currently executing an RSSI measurement. RSSI_BUSY is set when a new measurement is requested via RSSI_START, and cleared when all configured raw measurements have been performed and a complete set of RSSI results is available.

SDADC_ENABLE

This bit enables the SD-ADC in order to execute RSSI measurements. The SD-ADC requires a start-up time of $t_{SDADC,STUP}$ before it can be used.

RSSI_START

This bit starts the digital processing of the SD-ADC output, after all analog setup is completed. For a single RSSI measurement (including averaging), the bit RSSI_START shall be cleared after RSSI_BUSY is asserted and before the result is generated, hence, before RSSI_VALID is asserted. Keeping RSSI_START asserted throughout a whole RSSI measurement sequence activates the continuous measurement mode, where consecutive results (including averaging) are generated in a row until RSSI_START is set back to 0.

2.5.10.16 LF channel-shorting control register LFSHCON

The LF pins feature active switches for attenuating the LF signals on the unused RSSI channels. Hence, while RSSI measurement is taking place on one LF channel, the other two can be attenuated by means of SHCHx bits in register (Table 67).

Table 67. LF channel-shorting control register LFSHCON (reset value 00h)

Bit	Symbol	Access	Value	Description
7 to 4	RFU	-/W0		Reserved for future use
3	SHCH3	R/W		Channel 3 short-switch control
			0	No attenuation, switch open
			1	Channel 3 input attenuated, switch closed
2	SHCH2	R/W		Channel 2 short-switch control
			0	No attenuation, switch open
			1	Channel 2 input attenuated, switch closed
1	SHCH1	R/W		Channel 1 short-switch control

Bit	Symbol	Access	Value	Description
			0	No attenuation, switch open
			1	Channel 1 input attenuated, switch closed
0	STDIS	R/W		Safety timer disable
			0	Safety timer enabled
			1	Safety timer disabled

SHCHx, Channel x short-switch control

The LF signal attenuation on given channel (INxP/N pair) pins, can be applied when the internal active switch is closed by means of SHCHx control bit set 1. No attenuation is applied when SHCHx control bit set 0. If the short switch control is enabled then the RSSI R_{short} resistance applies at the selected channel between INxN and ground and INxP and ground, respectively.

The SHCHx bits are automatically cleared and cannot be set to 1 when the device is supplied from the LF field, i.e. when device is in the LF FIELD state (PMODE = 0). The SHCHx bits are also cleared automatically on transition to the POWER OFF state.

STDIS, Safety timer disable control

To ensure the shorting switches are released after RSSI measurements are finished, a safety mechanism is included by means of a fixed interval timer. The safety timer uses the same clock as the watchdog timer and has a time-out interval of 32.0 ms (nominal). Where longer times are needed, the application can disable the safety timer and rely on the watchdog. The safety timer is active whenever any of the SHCHx bits is set to 1 and the STDIS bit set to 0, hence in default configuration. The time-out period will be restarted whenever any of the SHCHx bits is set to 1, unless STDIS is set to 1. The SHCHx bits are automatically cleared whenever the safety time-out limit is reached. The safety timer stops automatically in debug mode.

When STDIS is set 1, no safety timer will be triggered nor running regardless on SHCHx settings. In this case, user software has to assure the channel switches are driven open after the RSSI measurement.

2.5.10.17 Real-time clock control register RTCCON

The interval timer and real-time clock control register RTCCON is shown in Table 68.

Table 68. Preprocessor control register RTCCON (reset value 80h)

Bit	Symbol	Access	Value	Description
7	ITRST	R/W		Interval timer reset
			0	No reset
			1	Reset and disable interval timer and real-time clock
6 to 5	RTC_SEL[1:0]	R/W		real-time clock event period
			00	No wake-up
			01	1 sec
			10	1 min
			11	60 min

Bit	Symbol	Access	Value	Description
4 to 2	IT_SEL[2:0]	R/W		Interval timer event period
			000	No wake-up
			001	500 us
			010	100 ms
			011	500 ms
			100	1 sec
			101	2 sec
			110	1 min
			111	2 min
1 to 0	IT_MODE[1:0]	R/W		Interval timer operation modes
			00	Interval timer and real-time clock are stopped. FSEC, SEC and MIN registers can be written. Any write access to these registers re-initializes the interval timer, thus all bits are cleared. LPDIVCLK output (for details, see CLKCON3.TMUX0C) is stopped.
			01	Reserved for future use
			10	Interval timer is running and real-time clock is stopped. FSEC, SEC and MIN registers can be written. If IT_SEL = 001 or 010, the interval timer generates a periodical wake-up. All other settings of IT_SEL do not generate a wake-up. LPDIVCLK output is running.
			11	Interval timer and real-time clock are running. Periodical wake-ups are generated according to the settings IT_SEL and RTC_SEL. LPDIVCLK output is running.

ITRST, interval timer reset

Setting ITRST stops the counter chain for both the interval timer and the real-time clock and clears FSEC, SEC, MIN, IT_WUP, RTC_WUP and RTC_WUP_OVF. ITRST is used if the interval timer and real-time clock are not needed or if they shall be stopped and configured again.

ITRST can be set when the interval timer and real-time clock are running. Setting ITRST permanently resets the interval timer and the values of MIN, SEC and FSEC can not be modified.

IT_SEL[2:0], interval timer wake-up period

If an application changes IT_SEL while the interval timer is running, the first wake-up for this new value may occur earlier than expected. If the application does not use the real-time clock, it can avoid this by clearing the interval timer first (IT_MODE[1:0] = 00b – real-time clock is cleared as well) and then changing IT_SEL.

IT_MODE[1:0], interval timer operation modes

The interval timer and the real-time clock are controlled via IT_MODE[1:0]. It is recommended to check the bits after writing in order to consider a possible synchronization delay between the CPU and the interval timer clock sources.

Stopping the interval timer via IT_MODE[1:0] is recommended before IT_SEL or RTC_SEL are modified in order to generate even the first wake-up in the expected time.

2.5.10.18 Real-time clock data register RTCDAT

The RTCDAT register allows word and byte access of the real-time clock data (Table 69).

Table 69. Word and byte access to the real-time clock data register RTCDAT

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
RTCDAT	RTCDATH	RTCDATL

The content of the real-time clock data register is shown in Table 70. The contents of MIN, SEC and FSEC can be read or updated via write access. The content of RTCDAT is not buffered or synchronized to the CPU clock. When the real-time clock is running, reading of RTCDAT can generate unstable and wrong values as the real-time clock value is not necessarily settled when reading takes place. During write access, dependent on IT_MODE, the remaining bits of the RTCDAT register may change as well.

Table 70. real-time clock data register RTCDAT (reset value 0000h)

Bit	Symbol	Access	Value	Description
15 to 10	MIN[5:0]	R/W		Minutes
9 to 4	SEC[5:0]	R/W		Seconds
3 to 0	FSEC[3:0]	R/W		Fractions of seconds (1/16th seconds)

MIN, minutes

MIN holds the number of passed minutes and increments every minute. After reaching the upper limit value of 59d, MIN is cleared with the next increment signal. In case an invalid value (> 59d) is written to MIN, this value will be kept until the next increment signal sets MIN to 0 again.

SEC, seconds

SEC holds the number of passed seconds and increments every second. After reaching the upper limit value of 59d, SEC is cleared with the next increment signal. In case an invalid value (> 59d) is written to SEC, this value will be kept until the next increment signal sets SEC to 0 again.

FSEC, fractions of seconds

FSEC holds the number of passed 1/16th seconds. Any write access to register RTCCON clears these bits.

2.5.10.19 Post-wake-up timer control register, POSTWUPCON

Post-wake-up timer is a hardware counter provided to aid the key-fob in an accurate timing response in the LF active protocol. Following configuration in the POSTWUPCON register, the post-wake-up timer will generate counter-match pulses as time stamps

related to either, the wake-up pattern matching-, the NewByte-, or both mentioned events. Same counter can be configured to trigger on any target-time-write action into the POSTWUPCOMP register, or by a dedicated run-bit set, hence is suitable for general purpose time measurement by a user application. Post-wake-up timer events can optionally source the compare-and-match interrupt.

The post-wake-up timer control POSTWUPCON is shown in Table 71.

Table 71. Post-wake-up timer control register POSTWUPCON (reset value 00h)

Bit	Symbol	Access	Value	Description
7	RFU	-/W0		Reserved for future use
6	MULTISHOT	R/W		Multi-shot enable bit
			0	Multi-shot disabled
			1	Multi-shot enabled
5	CMPWRPENDING	R/-		Timer Compare value pending update to counter
			0	Counter timer Compare updated
			1	Counter timer Compare pending update
4	WUPRESTART	R/W		Timer counting enable on WUP
			0	No effects
			1	Activate timer counting on WUPs
3	NBRESTART	R/W		Timer counting enable on NewByte event
			0	No effects
			1	Activate timer counting on NewByte event
2	RUN	R/W		Post wake-up timer run status and control bit
			0	Counter stopped (R); stop counter (W)
			1	Counter running (R); leave running (W)
1	CMPINTEN	R/W		Compare and match interrupt enable bit
			0	No effects, interrupt disabled
			1	Interrupt enabled
0	CMPMATCH	R/W		Interrupt Flag / Clear match interrupt bit
			0	Compare event not reached (R); No effects (W)
			1	Compare event reached (R); Clear the interrupt flag (W)

MULTISHOT, Multi-shot counter mode enable

If MULTISHOT set to 0 then whenever the compare value is reached, the post-wake-up counter will automatically stop. If MULTISHOT is set to 1 then, whenever the compare value is reached, the post-wake-up counter will reset to 0000h and will restart counting, which allows that multiple events can be triggered. Any new wake-up match or NewByte detected (if enabled via WUPRESTART and NBRESTART) will also restart counting.

CMPWRPENDING, Timer Compare value pending update to counter

When the CMPWRPENDING is read 1, it indicates that a new value set in POSTWUPCMP[15:0] is still pending an update into the internal register of the post-

wake-up timer. When the CMPWRPENDING is read 0, it indicates that the value stored in POSTWUPCMP[15:0] and the value of the internal post-wake-up timer register are equal.

WUPRESTART, WUP counter mode enable

When the WUPRESTART bit is set 1, any new wake-up pattern match resets and restarts the post-wake-up timer. If WUPRESTART bit is set 0, any new wake-up pattern match does not influence the post-wake-up timer.

NBRESTART, NewByte counter mode enable

When the NBRESTART bit is set 1, any subsequent NewByte event resets and restarts the post-wake-up timer. If NBRESTART bit is set 0, any subsequent NewByte event does not influence the post-wake-up timer.

RUN, post-wake-up timer run status and control bit

With the RUN status bit, application has additional information whether timer is running or not. When RUN is read 0, it indicates the post-wake-up timer is stopped. Read 1 will indicate the counter is running. Application writes 0 into RUN when post-wake-up timer is to be stopped. Writing 1 into this bit has no effects on timer behaviour. Hardware will restart counter depending on configured RESTART event.

CMPINTEN, post-wake-up timer interrupt enable bit

With the CMPINTEN bit set 1, it enables the preprocessor interrupt, IF_PP (see Table 104), to fire when the post-wake-up count is equal to or exceeds PWUPCMP[15:0]. Note, in addition to CMPINTEN bit, IE_PP (see Table 99) needs to be set before the interrupt propagates to the CPU. The timer compare match will create only an interrupt but no wake-up event.

CMPMATCH, post-wake-up timer compare match flag

CMPMATCH=0 indicates that the post-wake-up timer has not yet reached the compare value in PWUPCMP[15:0]. When CMPMATCH=1, the compare value has been reached. Note that the bit does not indicate the current state of the comparison: in case of multi-shot mode the timer automatically wraps around to zero and restarts counting, while the bit is persistent. Application software is responsible to clear CMPMATCH by writing a '1' to the respective bit position. Writing a '0' has no effect.

2.5.10.20 Post-wake-up timer compare register, POSTWUPCOMP

The post-wake-up timer compare register POSTWUPCOMP offers word and byte access as shown in Table 72, and bit-fields as shown in Table 73.

Table 72. Word and byte access to the post-wake-up compare register, POSTWUPCOMP

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
POSTWUPCOMP	POSTWUPCOMPH	POSTWUPCOMPL

Table 73. Post WUP timer control register POSTWUPCOMP (reset value 0000h)

Bit	Symbol	Access	Value	Description
15 to 0	PWUPCMP[15:0]	R/W		Compare value for the post-wake-up timer event

POSTWUPCMP[15:0], Compare value settings

The PWUPCMP[15:0] holds the value the post-wake-up timer value is compared against, to generate a match-event. When post-wake-up timer reaches the programmed PWUPCMP[15:0] value, a CPU interrupt is generated.

2.6 LF tuning capacitors

The LF tuning function provides a facility for adjusting the input capacitance seen at the LF input pins, INxP and INxN. This allows fine tuning of the resonant frequency of the external antenna circuit to optimize the reception of an incoming LF signal.

The tuning capacitance is implemented as a configurable array of capacitors connected between the LF input pins INxP, INxN, and ground as depicted in Figure 31. The tuning capacitors support a resolution of C_{STEP} and they can be set for each LF input individually in 32 steps from 0 to $31 \cdot C_{STEP}$.

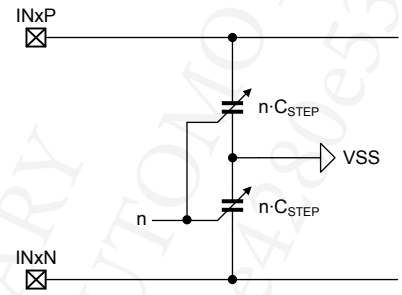


Figure 31. LF tuning capacitors

The effect of the LF tuning capacitors depends on the input signal strength. For weak input signals—typical for LF Active operation—the LF front-end rectifier has no influence. The tuning capacitors operate in series to the LF input, thus, their effective capacitance seen at the LF input pins is halved. The effective input capacitance C_{IN} for this case is given in Equation 8:

$$C_{IN} = C_{IN\_ACT} + (n \cdot C_{STEP}) / 2 \quad (8)$$

For strong input signals—like for LF Passive (immobilizer) operation—the LF front-end rectifier connects one LF input to ground during every half-wave. This means that one side of the LF tuning capacitor is grounded as well and, thus, does not contribute. The effective input capacitance C_{IN} seen between the pins INxP/INxN for this case is given in Equation 9:

$$C_{IN} = C_{IN\_PAS} + n \cdot C_{STEP} \quad (9)$$

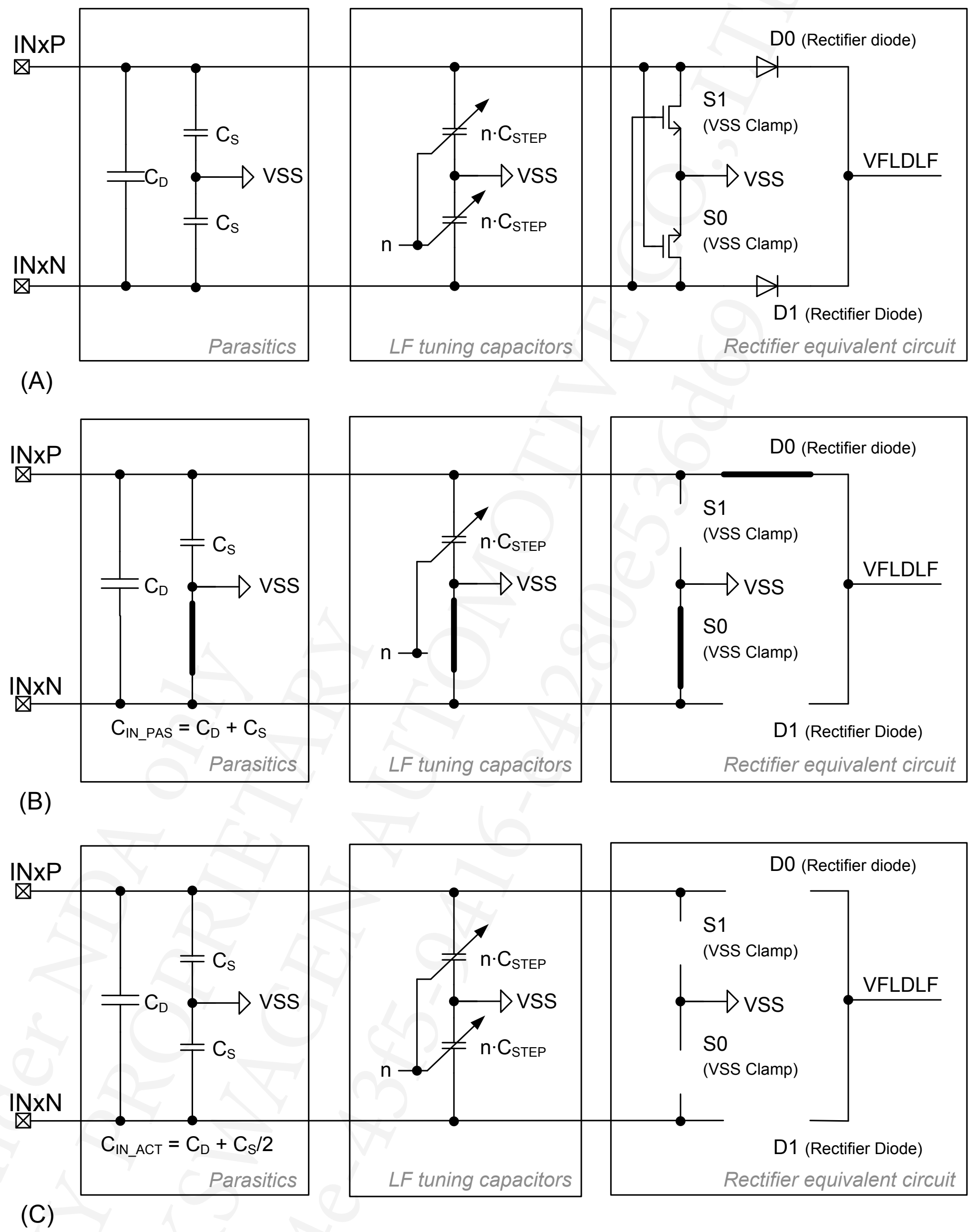
To account for this behavior, the device supports two different user configurable sets of tuning values, which are optimized for LF Active operation with weak input signals and LF Passive (immobilizer) operation with strong input signals. The selection between these two settings is done automatically dependent on the battery supply level and the recognition of an LF Passive protocol.

Each channel pair, IN1P/IN1N, IN2P/IN2N and IN3P/IN3N can be controlled independently by writing the contents of the LFTUNECHxACT and LFTUNECHxIMMO

SFRs, one register per channel (x=1, 2, 3). Capacitor selection can be controlled from either the VBAT domain registers, LFTUNECHxACT, or the VDD domain registers, LFTUNECHxIMMO, depending on the supply state and whether the LF front-end is in passive immobilizer mode or not. Further details are described in Section 2.6.2.

For weakly-coupled input signals, the LF front-end rectifier has no effect and the voltages on INxP and INxN are differential with a common-mode voltage around ground. In this case, the LF tuning capacitors on INxP and INxN are in series resulting in an effective tuning value of half the single-ended value. For strongly-coupled signals, the LF front-end rectifier creates half-wave rectified voltage signals on INxP and INxN. In this case the capacitance to ground on each pin is in circuit for each half-wave. The effective tuning capacitance is the single-ended value.

Strongly-coupled and weakly-coupled signals influence the equivalent resonance capacitance as can be seen in Figure 32, with the help of the LF-front-end rectifier AC-model (A). The LF front-end rectifier for strongly-coupled signals is AC-grounding the INxN side through-out the VSS-clamp S0 in (B), while for the weakly-coupled signals, the complete model of the rectifier can be replaced by "opens" (C).



1. This figure shows a simplified model of the rectifier, wherein the limiter, the active demodulator and the passive (de)modulator are omitted.

Figure 32. LF input capacitance, (A) AC-model, (B) Strongly-coupled signals, and (C) Weakly-coupled signals

2.6.1 Tuning capacitance

Table 74 and Table 75 show details on LF tune decoding and indicate how much capacitance is added to each pin (single-ended) for each code independent on which supply domain the selection is active. C_{STEP} represents the unit capacitor in the LF tuning array.

LF tuning function is disabled by the tuning capacitance settings 0. When LF_CAPI_CHx[4:0] and LF_CAPB_CHx[4:0] are set to 0, there is no added capacitance. The input capacitance at each pin is as specified by parameters C_{IN_PAS} (strongly-coupled signal) and C_{IN_ACT} (weakly-coupled signal) in the Static Characteristics section.

2.6.2 Use cases

Each use case begins with the device in the POWER OFF state. In this state VDD is below the POR threshold. Each use case assumes that an LF signal is received on one or more of the INxP/N input channels.

2.6.2.1 LF Active with battery supply

When the LF signal is received, the state of the LF tuning capacitance will remain unchanged as long as the device does not change to immobilizer mode.

As stated before, for very small signals, the effective LF tuning capacitance is half that for larger (rectified) signals. The code stored in LFTUNECHxACT should be chosen to optimize small-signal operation, even though for stronger signals, the tuning is not optimal. However, with such large signal levels, the resulting small de-tuning will usually not reduce the LF Active reception performance noticeably. For RSSI, other non-linear effects are present as well.

2.6.2.2 Passive immobilizer without battery supply

The battery supply voltage is absent or below the internal BATPOR threshold. The device has no power supply.

In this case, with no battery, the LF Active receiver is not functional. Only LF Passive (immobilizer) communication is possible.

When an LF signal is first received, LF tune selection defaults to a state equivalent to the reset state of LFTUNECHxIMMO. This state is internally defined, independent of the contents of LFTUNECHxIMMO and cannot be altered.

If the LF input signal is strong enough to exceed the field-flag threshold, VTHR,FD_ATIC_VIN, and is unmodulated for more than 2ms, the device enters passive immobilizer mode and the internal VDD supply is powered from the LF signal. After this time, the device boot routine executes, during which, LFTUNECHxIMMO is loaded with values stored in the configuration EEPROM. This value is user-definable and may be different from the default (reset) value. A system call can be used by the application software to overwrite the value for LFTUNECHxIMMO in the configuration EEPROM.

2.6.2.3 Passive immobilizer with battery supplied

The battery supply voltage exceeds the internal BATPOR threshold.

Prior to reception of the LF signal, LF tune selection is taken from LFTUNECHxACT special function registers. When an LF signal is received, the LF tune state is maintained until passive immobilizer mode is started and VDD exceeds the internal POR threshold. At this point, LF tune selection switches to the contents of LFTUNECHxIMMO, which at this point is the reset state 00011b.

After this time, the device boot routine is executed and is loading the LFTUNECHxIMMO with a value stored in the configuration EEPROM. This value is user-definable and may be different from the default (reset) value.

2.6.2.4 LF tune for passive immobilizer - timing diagram

The diagram below shows the sequence of events for use cases described in Section 2.6.2.2 and Section 2.6.2.3 and how LF tune selection changes when the LF input is applied.

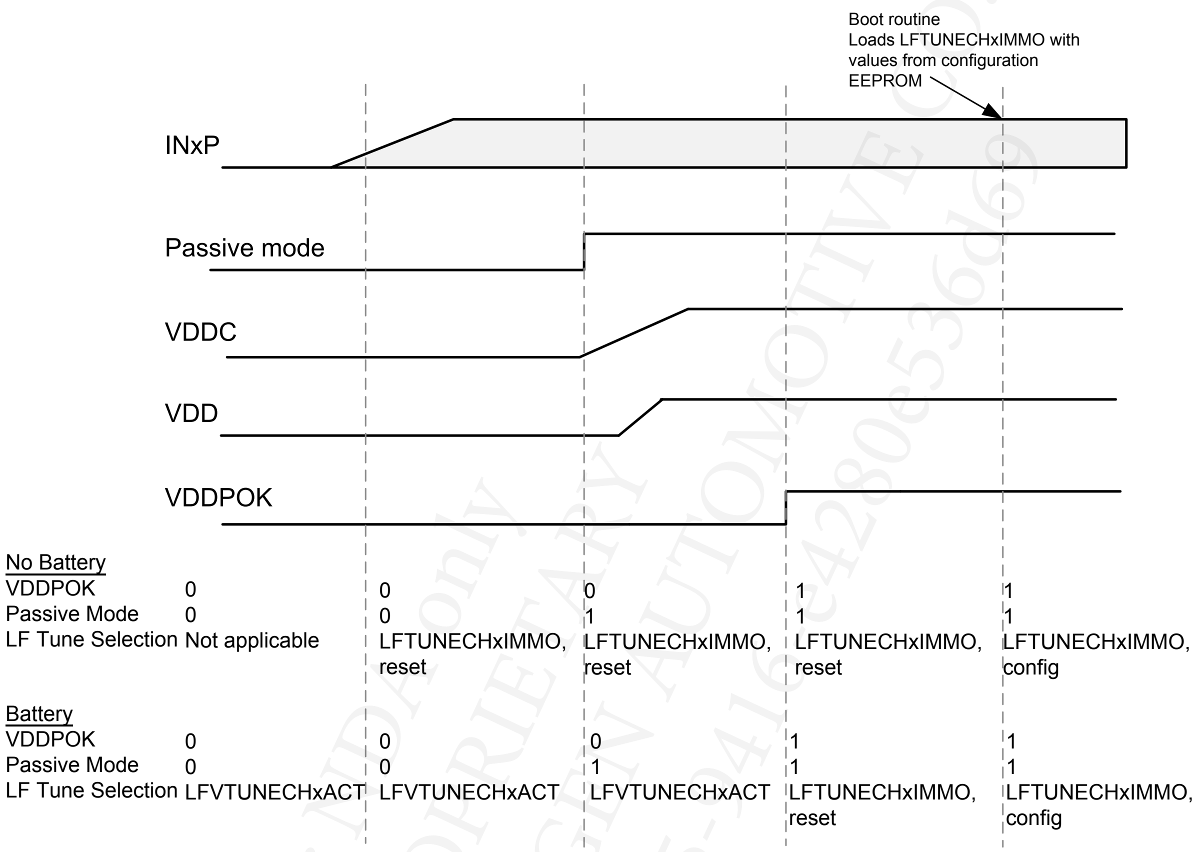


Figure 33. LF tune for passive immobilizer - timing diagram

2.6.3 Suggested settings

When designing the external antenna circuit, the capacitor chosen should take account of the device input capacitance and the state of LF tune. Any stray capacitance from the PCB should also be considered. This would require that the off-chip tuning capacitor is reduced compared to the value calculated for optimal tuning.

As discussed in Section 2.6.2.2, values stored in LFTUNECHxIMMO are updated during the boot routine when LF passive mode has been detected by loading values from the Device Configuration Page DCFG E (see Table 90) located in the ULP EEPROM. In the first instance it is suggested that these values are the same as the LFTUNECHxIMMO reset state (00011b) to avoid a change in the LF tune capacitance during boot. If it is necessary to optimize tuning to account for external component spreads, then the values stored in the configuration EEPROM can be modified with the knowledge that prior to loading these values, the antenna circuit will not be optimally tuned.

If the off-chip tuning capacitor is designed to give optimal tuning for passive immobilizer operation, the values stored in LFTUNECHxACT can be adjusted after battery insertion to optimize tuning for small-signal LF Active operation.

This approach would lead to optimized tuning for use cases described in Section 2.6.2.2 and Section 2.6.2.3.

The use case in Section 2.6.2.3 can also be applied for applications in which LF Active is not used. In such circumstances it would be advisable to load LFTUNECHxACT with the same value as stored in LFTUNECHxIMMO to have the optimum tuning already during the passive immobilizer start-up phase. Please note that there is still a temporary change of the tuning value during the boot routine, unless the LFTUNECHxIMMO reset state (00011b) is used.

2.6.4 Registers for tuning capacitors settings

Tuning capacitor settings are defined as 5-bit fields organized in two sets of consecutive user-mode byte-registers, one set maintained in VBAT domain and the other maintained in VDD domain. Each set contains three registers - one for each LF channel, as specified in the following sub-sections.

2.6.4.1 Tuning configuration control registers, LFTUNECHxIMMO

The register LFTUNECHxIMMO is described in Table 74.

Table 74. Tuning configuration registers LFTUNECHxIMMO (reset value 0000_0011b)

Bit	Symbol	Access	Value	Description
7 to 5	RFU	-/W0		Reserved for future use
4 to 0	LF_CAPI_CHx[4:0]	R/W		Applied INxP/N tuning capacitance
			00000	No capacitance switched; C_{tune}= 0 * C_{STEP}
			00001 - 11111	Switched capacitance to each pin: C_{tune}= Value * C_{STEP}

VDD domain tuning capacitor settings, LF_CAPI_CHx[4:0]

When the device boots into immobilizer mode, the LF tune selection switches automatically to the content of the registers LFTUNECHxIMMO, which at this point hold the reset value 00011b. Later the boot routine loads the values stored in the device configuration page DCFG E in the ULP EEPROM into the register bits LF_CAPI_CHx.

2.6.4.2 Tuning configuration control registers, LFTUNECHxACT

The register LFTUNECHxACT is described in Table 75.

Table 75. Tuning configuration registers LFTUNECHxACT (reset value 0001_0011b)

Bit	Symbol	Access	Value	Description
7 to 5	RFU	-/W0		Reserved for future use
4 to 0	LF_CAPB_CHx[4:0]	R/W		Applied INxP/N tuning capacitance
			00000	No capacitance switched; C_{tune}= 0 * C_{STEP}
			00001 - 11111	Switched capacitance to each pin: C_{tune}= Value * C_{STEP}

VBAT domain tuning capacitor settings, LF_CAPB_CHx[4:0]

These registers control the LF tuning capacitors while battery is present (above BATPOR threshold) and immobilizer mode is not active. Unlike the LFTUNECHxIMMO registers, they are not written by the boot routine, instead, the application software is responsible for their contents.

2.7 RISC controller

The NCF215A / NCF215B is powered by NXP's 3rd generation low power 16 bit extended Micro RISC Kernel (MRK III) with enhanced instruction set (MRK III-e), which controls device operation in LF FIELD and BATTERY state.

The MRK III utilizes a Harvard architecture featuring a 16 bit ALU and supports hardware extended MUL and DIV operations. The instruction set supports 8 bit and 16 bit operations and is optimized for C programming. Due to the efficient 2-stage pipeline (fetch/execute), most instructions execute in a single machine cycle (two clock cycles), resulting in ultra-low power consumption.

The MRK III provides 64 kByte linear data address range and 128 kByte linear code address range, powerful addressing modes and high code density. Besides, the MRK III supports a power saving mode and code/data protection mechanisms (privilege modes).

2.7.1 Power saving modes

2.7.1.1 RUN mode

In RUN mode the MRK III is regularly clocked and processes the program instructions.

2.7.1.2 IDLE mode

The IDLE mode is a power saving mode and invoked via the command IDLE. In IDLE mode the MRK III CPU is halted by gating the internal clock signal for the MRK III CPU.

IDLE mode can only be entered, if the level sensitive wake-up signal of the MRK III controller is not active. As soon as the wake-up signal becomes active, the MRK III resumes operation and switches to RUN mode.

2.7.2 Privilege modes

2.7.2.1 SYSTEM mode

In SYSTEM mode, the NXP implemented firmware (system code, e.g. transponder emulation) is processed. SYSTEM mode is entered by a software interrupt via the SYS command or by serving a system interrupt request. SYSTEM mode is also used while executing the BOOT routine and during MDI operation.

After completing the system routines, the MRK III switches back to USER mode and control is given back to the application program.

2.7.2.2 USER mode

The application program is executed in USER mode. In USER mode, all MRK III instructions can be processed. If the MRK III is in SYSTEM mode, USER mode is entered via the USR command or by serving a user interrupt request.

2.7.3 Memory organization

The memory management unit (MMU) provides access to the different memories for code and data storage. It supports strict separation between memory areas assigned to SYSTEM or USER mode.

2.7.3.1 System code memory

The NXP implemented system ROM functions contain (see Section 2.24)

- Boot routine
- Transponder emulation functions
- In-circuit Monitor and Download Interface

The system code memory is not visible for the application.

2.7.3.2 System data memory

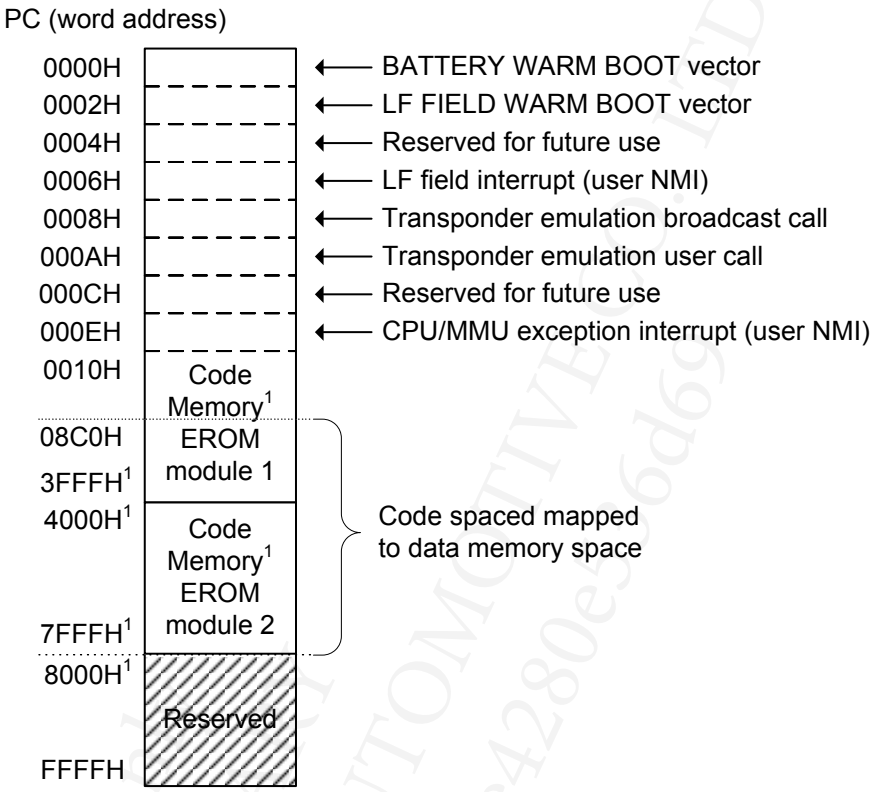
The NCF215A / NCF215B has a dedicated data memory area including system RAM for device execution in SYSTEM mode. The system data memory area is not visible for the application. All system calls, the built-in transponder emulations and the in-circuit debugging functions use the system RAM.

2.7.3.3 Application code memory

Application code and read-only data reside in EROM memory. Each application code instruction is either 16 or 32 bit long and thus occupies two or four bytes of EROM memory, respectively (see Figure 34).

For a battery wake-up event or in a case EROM execution of the immobilizer is selected, the application code is started at the corresponding BATTERY or LF FIELD WARM BOOT vector after the BOOT routine.

The EROM has a size of 64 kBytes and consists of two identical memory modules, 1 and 2, with a size of 32 kBytes each. EROM module 1 is unconditionally available upon each entry to EROM application code. EROM module 2 is conditionally enabled depending on an EEPROM device configuration (see DCFG D, Table 89). In addition, the application can make use of a provided system call to enable or disable EROM module 2, based on the application needs. As EROM module 2 requires a static bias current of ΔI_{DD_EROM2} when powered up, it is strongly advised to keep EROM module 2 disabled if not needed, which is e.g. recommended for a custom EROM immobilizer implementation.



1. The NCF215A / NCF215B can support up to 64 kByte of application code memory. The actual amount of available application code memory and the end address of the code memory space may vary depending on an orderable type number. For details contact your local NXP sales representative.

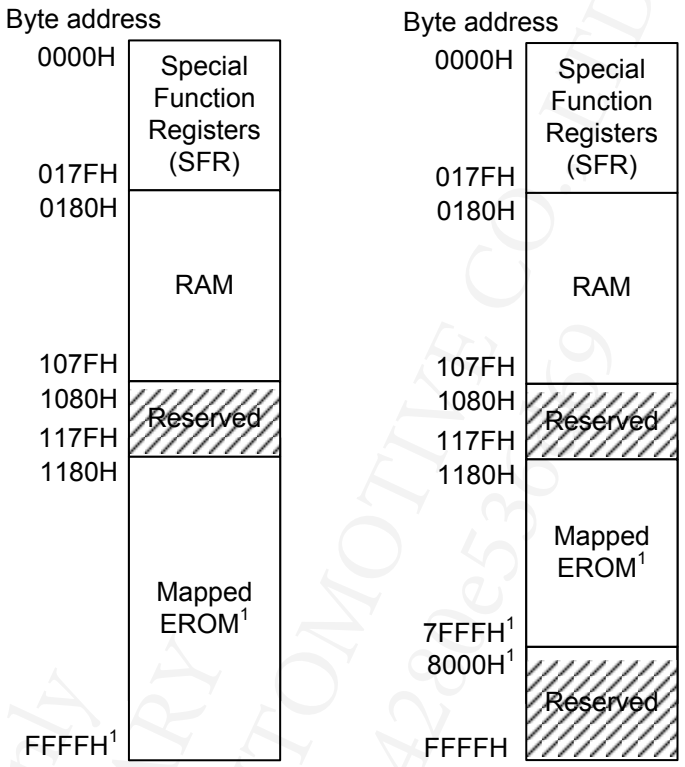
Figure 34. Application code memory

2.7.3.4 Application data memory

The data memory address space is split to cover the Special Function Registers (SFR) and the User RAM (Figure 35). The SFR enable full read/write access to the peripherals. The User RAM provides memory for volatile application data and stack storage and is available for the application program without any limitations, because device execution in SYSTEM mode uses system RAM only. The stack starts at the end of the User RAM and grows with decreasing addresses.

In order to give access to constant data stored in the EROM (like look-up tables, constants, etc.) the unoccupied data address range is mapped to the code memory with the same logical address. Since the lower addresses of the application data memory are already used by the SFR and RAM, the EROM mapping starts at addresses after the RAM section. Thus, the EROM code memory content at addresses corresponding to the SFR and RAM sections in the data memory cannot be accessed via data mapping. Although the instructions in the code memory have word granularity, read-only data can also be accessed with byte granularity (byte address = 2 × word address).

The memory mapping scheme supports the standard ANSI-C memory model and avoids performance losses caused by generic pointer types, which are able to address different memory types dynamically.



1. The NCF215A / NCF215B can support up to 64 kByte of application code memory. The actual amount of available application code memory and the end address of the code memory space may vary depending on an orderable type number. For details contact your local NXP sales representative. The left figure shows 64 kByte and the right one 32 kbyte of application code memory as examples.

Figure 35. Application data memory

The NCF215A / NCF215B provides ultra-low power (ULP) serial EEPROM for persistent application data storage. The ULP EEPROM is intended for the immobilizer and remote keyless entry applications.

The ULP EEPROM is not mapped into the application data memory. It is only accessible via the ULP EEPROM interface.

2.7.4 CPU/MMU exceptions

The CPU and the MMU provide means to detect forbidden execution attempts. This function can be enabled and disabled by means of an EEPROM configuration. If it is enabled, either a device reset or the CPU/MMU exception NMI is generated if one of the following conditions is detected:

- Attempt to execute an illegal command code
- Attempt to make a stack access with the stack pointer unequal to a word address
- Attempt to access an unassigned memory range
- Attempt to access EROM module 2 when it is powered down

This feature is enabled and disabled via device configuration DCFG A in ULP EEPROM module 15 with setting CXDIS (see Table 87). The selection between reset and NMI is configured with bit CXNMIEN in register INTEN0 (see Table 97).

2.7.5 CPU Machine Cycle Counter, CPUMCC

For measuring the time of a code segment execution, NCF215A / NCF215B is equipped with a 32-bit machine cycle counter, CPUMCC. When enabled, the counter is incremented by a CPU clock as selected in the CLKCON0 register. Following to the clock configuration bit, CLKSELCNT, the CPUMCC can optionally count the Idle instruction clock cycles. In Monitor and Debug mode, the CPUMCC counting is suspended.

2.7.6 Register description

The CPU/MMU exceptions can be monitored, the RISC Machine Cycle Counter can be operated an the status of EROM module 2 can be interrogated as described in the following sections.

2.7.6.1 Register, CXSW

This register reports the CPU/MMU exception status.

Table 76. MMU exception status word register, CXSW (reset value 00h)

Bit	Symbol	Access	Value	Description
7	SYSMODE	R/-		System mode flag when the exception occurred
			0	USER mode when the exception occurred
			1	SYSTEM mode when the exception occurred
6 to 3	I[3:0]	R/-		Interrupt request level when the exception occurred during interrupt routine
			0000 - 1111	For details, see interrupt request level assignment in Table 94
2	XPMEM	R/-		MMU program memory exception flag
			0	No exception in accessing program memory
			1	Addressed program memory out of range or attempt to access EROM module 2 when powered down
1	XSTACK	R/-		Misaligned CPU stack flag
			0	No exception in CPU stack, even value in the CPU stack
			1	CPU stack misaligned, odd value in CPU stack
0	XINSTR	R/-		Unknown instruction exception flag
			0	No exception in detecting instructions
			1	Unknown instruction detected

2.7.6.2 Register, CXPC

This register contains the registered program counter value when the exception occurred. The register is read-only and provides byte and word access.

Table 77. Word and byte access to the status register CXPC

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
CXPC	CXPCH	CXPCL

Table 78. Register, CXPC (reset value 0000h)

Bit	Symbol	Access	Value	Description
15 to 0	PC[15:0]	R/-		Program counter value when MMU exception occurred

2.7.6.3 Register CPUMCCCNT0

This register contains the registered machine cycle counter value, the lower two bytes. Value represents the exact number of machine cycles between the counter start and counter stop instructions. Register is read-only and provides byte and word access.

Table 79. Word and byte access to the status register, CPUMCCCNT0

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
CPUMCCCNT0	CPUMCCCNT0H	CPUMCCCNT0L

Table 80. Register, CPUMCCCNT0 (reset value 0000h)

Bit	Symbol	Access	Value	Description
15 to 0	MCCCNT[15:0]	R/-		Machine cycle counter value, the lower two bytes

2.7.6.4 Register CPUMCCCNT1

This register contains the registered machine cycle counter value, the upper two bytes. Value represents the exact number of machine cycles between the counter start and counter stop instructions. Register is read-only and provides byte and word access.

Table 81. Word and byte access to the status register, CPUMCCCNT1

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
CPUMCCCNT1	CPUMCCCNT1H	CPUMCCCNT1L

Table 82. Register, CPUMCCCNT1 (reset value 0000h)

Bit	Symbol	Access	Value	Description
15 to 0	MCCCNT[31:16]	R/-		Machine cycle counter value, the upper two bytes

2.7.6.5 Machine Cycle Counter Control Register, CPUMCCCON

The CPUMCCCON register holds control bits of the CPU Machine Cycles Counter for clock selection, counting start and stop, and counter reset.

Table 83. CPU Machine Cycle Counter Control Register, CPUMCCCON (reset value xxxx_x000b)

Bit	Symbol	Access	Value	Description
7 to 3	RFU	-/W0		Reserved for future use
2	CLKSELCNT	R/W		Instruction/Machine Cycle Counter mode selection
			0	System clock (CPUCLK) counter - does not stop during IDLE instructions
			1	CPU Instruction Cycle counter - stops during IDLE instructions
1	ENCNT	R/W		Machine Cycle Counter enable
			0	Stop and freeze the counter

Bit	Symbol	Access	Value	Description
			1	Start (enable or resume) the counter
0	RSTCNT	R0/W		Machine Cycle Counter reset request one-shot. Writing a 1 resets the counter. Always read as 0
			0	No Action
			1	Reset the Machine Cycle Counter

2.7.6.6 Register PFCON3

This register reports the status of EROM module 2. EROM module 2 can be enabled and disabled by a system call (for details refer to [2]).

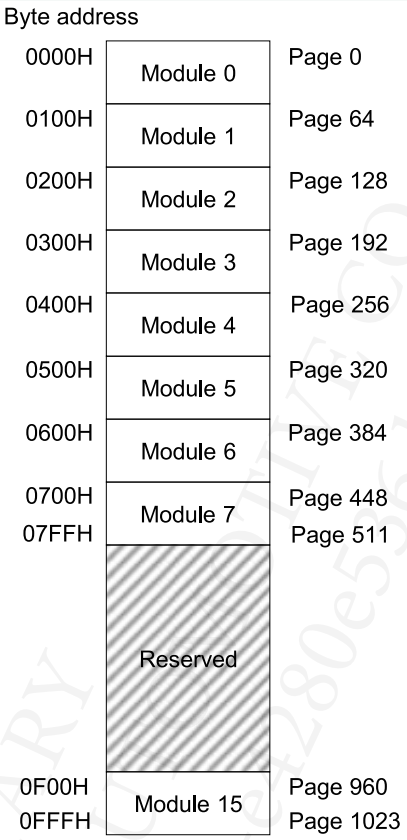
Table 84. EROM control register, PFCON3 (reset value xxh)

Bit	Symbol	Access USER mode	Value	Description
7 to 2	RDT	-/-		Reserved for device test
1	PF2_EN	R/-		EROM module 2 control
			0	off
			1	on
0	RDT	-/-		Reserved for device test

2.8 ULP EEPROM

The ultra-low power (ULP) serial EEPROM is intended for persistent data storage for the immobilizer, boot routine and system functions in ROM and the application software. The ULP EEPROM consists of up to 9 modules (module 0 to 7 and module 15). In Figure 36 the ULP EEPROM data memory map is given in case 2048 Byte EEPROM (module 0 to 7) plus 256 Bytes for module 15 is actually available. In this case the application has full read/write/program access to modules 0 to 7. The only exception is pages 0 to 7, which are specially protected and do not allow direct read access or alteration. Module 15 holds trim and configuration data and can only be read but not written or programmed by the application (note: some specific locations may be programmed with a dedicated system call).

Each ULP module consists of 64 pages containing 4 byte (32 bit) each. The ULP modules are optimized in terms of power consumption for read access and programming by having a separate power-on bit for each module.



1. The NCF215A / NCF215B can support up to 2048 Byte of ULP EEPROM (excluding module 15). The actual amount of available ULP EEPROM and the available modules may vary depending on the type number. Here the ULP EEPROM data memory map is given in case the actual available EEPROM is 2048 Bytes. For details contact your local NXP sales representative.

Figure 36. ULP EEPROM data memory map (2048 Byte EEPROM configuration)

2.8.1 Available ULP EEPROM modules

The NCF215A / NCF215B supports up to 2048 Byte ULP Serial EEPROM (excluding module 15). The actual amount of available ULP Serial EEPROM and thus the number of available EEPROM pages may vary depending on the type number. For details contact your local NXP sales representative. The actual ULP EEPROM data memory map is dependent on the actual amount of available ULP Serial EEPROM.

2.8.2 ULP module 15

Independent from the actual amount of available ULP Serial EEPROM supported, ULP module 15 is always available and contains the 64 bit chip information consisting of the 32 bit serial number (SN) and the 32 bit chip information (CINF). Further, ULP module 15 locates the device configuration pages. Module 15 contains trim and configuration data in the reserved areas (see Figure 37).

All pages except 1004 to 1007 are readable by the MRK III CPU core. The pages 960 to 975 and 992 to 1023 contain factory programmed data which can not be altered. The pages 976 to 991 locate the device configuration data (DCFG) which can only be modified in INIT mode (see Section 2.23) via the Monitor and Download Interface (MDI).

To enable compatibility to future devices, it is not recommended to store any other data into the DCFG area.

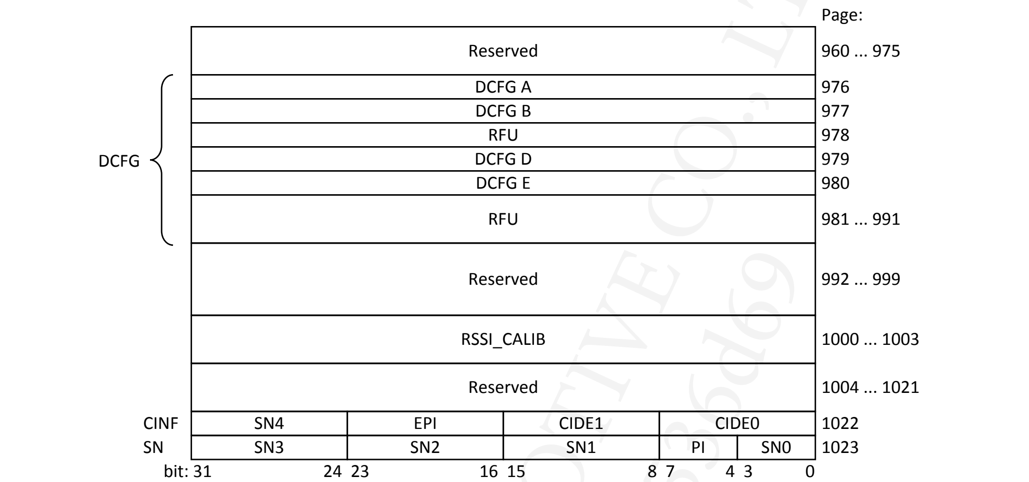


Figure 37. ULP EEPROM memory module 15

2.8.2.1 Serial Number (SN)

The SN represents the 32 bits of the unique device serial number.

The SN is located in ULP memory page 1023. SN bits 4 to 7 represent the product type identifier (PI). The SN is typically employed in the process of device authentication in transponder mode as well as during rolling code or challenge response generation for keyless entry applications.

Table 85. Device serial number SN (content upon delivery see Table 91)

Bit	Symbol	Access	Value	Description
31 to 24	SN3[7:0]	R/-		Device serial number bit 24 to 31
23 to 16	SN2[7:0]	R/-		Device serial number bit 16 to 23
15 to 8	SN1[7:0]	R/-		Device serial number bit 8 to 15
7 to 4	PI[3:0]	R/-	1011b	Device product identifier (Bh)
3 to 0	SN0[3:0]	R/-	0000b	Device serial number bit 0 to 3 (NXP identifier)

2.8.2.2 Chip Information (CINF)

The enhanced chip information CINF, is located in ULP memory page 1022 and serves to enlarge the unique device serial number by 8 bits (SN4). Further, the CINF contains the NXP enhanced product identifier (EPI) and the customer identifier (CIDE).

Table 86. Enhanced chip information CINF (content upon delivery see Table 91)

Bit	Symbol	Access	Value	Description
31 to 24	SN4[7:0]	R/-	0000_0000b	Device serial number bit 32 to 39
23 to 16	EPI[7:0]	R/-		Device enhanced product identifier
			0001_1010b	NCF215A
			0001_1011b	NCF215B
15 to 8	CIDE1[7:0]	R/-	0000_0000b	Customer identifier bit 8 to 15

Bit	Symbol	Access	Value	Description
7 to 0	CIDE0[7:0]	R/-	0011_0110b	Customer identifier bit 0 to 6 (36h)

2.8.2.3 RSSI_CALIB

RSSI_CALIB includes four pages with calibration coefficients for each gain range and for every channel as well as calibration data for the RSSI channel shorting resistor values. This calibration data is used by the RSSI measurement and calibration routines provided as C library functions.

2.8.2.4 Device configuration (DCFG)

The device configuration DCFG pages contain device configuration information, which is locked against overwriting. The DCFG bits can be initialized via the Monitor and Download Interface (MDI) only and are evaluated after each device reset within the boot routine.

Table 87. Device configuration page DCFG A (content upon delivery see Table 91)

Bit	Symbol	Access via MDI in INIT mode	Access by User Software	Value	Description
31 to 30	ENWER	R/W	R/-		Enable system call to write EROM (phcaiKEyLLGenFunc_CS_EROM_write)
				10	Enabled
				others	Disabled
29 to 16	RFU	-/W0	-/-		Reserved for future use
15 to 12	CXDIS[3:0]	R/W	R/-		CPU/MMU exceptions
				1001	Disabled
				others	Enabled
11 to 4	RFU	-/W0	-/-		Reserved for future use
3 to 0	LFFLDDIS[3:0]	R/W	R/-		LF field reset and non-maskable interrupt
				1001	Disabled
				others	Enabled

Table 88. Device configuration page DCFG B (content upon delivery see Table 91)

Bit	Symbol	Access via MDI in INIT mode	Access by User Software	Value	Description
31 to 8	RFU	-/W0	-/-		Reserved for future use
7 to 6	CHAN_SEL[1:0]	R/W	R/-		Channel for clock recovery in transponder emulation
				00	Reserved for future use
				01	Channel 1
				10	Channel 2

Bit	Symbol	Access via MDI in INIT mode	Access by User Software	Value	Description
				11	Channel 3
5	RFU	-/W0	-/-		Reserved for future use
4	STRONGMOD	R/W	R/-		Strong LF modulator in transponder emulation
				0	Enable standard LF modulator
				1	Enable strong LF modulator
3 to 1	RFU	-/W0	-/-		Reserved for future use
0	LFTEN	R/W	R/-		LF transponder emulation enable
				0	Use LF warm boot vector
				1	Enable emulation in system ROM

CHAN_SEL[1:0], Channel for clock recovery

Channel clock selection of the 1D-device that is effective after an LF field wake-up is defined by the user-area EEPROM configuration bits CHAN_SEL[1:0]. For NCF215A, the CHAN_SEL[1:0] is not used. For NCF215B, the CHAN_SEL[1:0] holds the pre-configured 1D-device channel configuration. Value of CHAN_SEL[1:0] will be read from DCFG and written into the LFCLKSEL[1:0] in I3DCON as the default value.

STRONGMOD, Strong LF-field modulator in transponder emulation

If set, after each device reset the transponder emulation will use additional load across the coil inputs for strong field modulation. If cleared, the field modulation will be performed with the standard load.

LFTEN, LF transponder emulation enable

If set, after each device reset the monolithic transponder emulation is enabled. If cleared, the boot sequence does not invoke the transponder emulation. Instead control is passed to the application program, starting at the LF (immobilizer) WARM BOOT vector.

Table 89. Device configuration page DCFG D (content upon delivery see Table 91)

Bit	Symbol	Access via MDI in INIT mode	Access by User Software	Value	Description
31 to 8	RFU	-/W0	-/-		Reserved for future use
7	PF2_A	R/W	R/-		EROM module 2 configuration, if device starts with battery supply
				0	EROM module 2 is disabled
				1	EROM module 2 in enabled
6	PF2_B	R/W	R/-		EROM module 2 configuration, if device starts with LF supply (immobilizer)
				0	EROM module 2 is disabled
				1	EROM module 2 in enabled

Bit	Symbol	Access via MDI in INIT mode	Access by User Software	Value	Description
5 to 0	RFU	-/W0	-/-		Reserved for future use

Table 90. Device configuration page DCFG E (content upon delivery see Table 91)

Bit	Symbol	Access via MDI in INIT mode	Access by User Software	Value	Description
31	RFU	-/W0	-/-		Reserved for future use
30 to 29	LF_CAPB_CH3M[4:3]	R/W	R/-	10	Tuning capacitors configuration for LF active mode - channel 3, higher two bits
28 to 24	LF_CAPB_CH2M[4:0]	R/W	R/-	10011	Tuning capacitors configuration for LF active mode - channel 2
23 to 21	LF_CAPB_CH3M[2:0]	R/W	R/-	011	Tuning capacitors configuration for LF active mode - channel 3, lower three bits
20 to 16	LF_CAPB_CH1M[4:0]	R/W	R/-	10011	Tuning capacitors configuration for LF active mode - channel 1
15	RFU	-/W0	-/-		Reserved for future use
14 to 13	LF_CAPI_CH3M[4:3]	R/W	R/-	00	Tuning capacitors configuration for Immobilizer mode - channel 3, higher two bits
12 to 8	LF_CAPI_CH2M[4:0]	R/W	R/-	00011	Tuning capacitors configuration for Immobilizer mode - channel 2
7 to 5	LF_CAPI_CH3M[2:0]	R/W	R/-	011	Tuning capacitors configuration for Immobilizer mode - channel 3, lower three bits
4 to 0	LF_CAPI_CH1M[4:0]	R/W	R/-	00011	Tuning capacitors configuration for Immobilizer mode - channel 1

LF tuning capacitors

Internal tuning capacitors configuration of 5-bits for each channel is provided twice, as LF_CAPB_CHxM[4:0] and LF_CAPI_CHxM[4:0], and stored into the page 3D4h. Bits 15 to 0 contain the passive LF capacitors configuration for the immobilizer mode, hence, will be loaded into the SFRs LFTUNECHxIMMO by the boot-routine when LF passive mode has been detected after a LF-field detection wake-up event. Bits 30 to 16 contain the LF active mode configuration and must be loaded into the SFRs LFTUNECHxACT by the application program.

2.8.3 ULP EEPROM interface

The access to the NCF215A / NCF215B memory modules is restricted to system call functions only. Please refer for detailed description of these application software calls to the WFS-5c_MRKIII-ROM-LIB documentation ([2]).

The memory modules consist of 256 bytes each and are essentially bit oriented (Figure 38). The ULP EEPROM interface provides byte oriented read access via an 8 bit data register to minimize the CPU load. Programming of the ULP serial EEPROM is supported on 32 bit pages only. An internal state machine handles the low level access to the module. The interface performs the read/write and programming operations autonomously and indicates the status via busy flag and optional wake-up from idle mode.

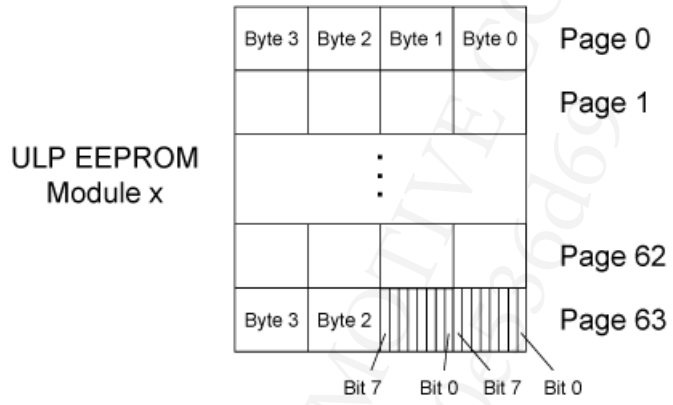


Figure 38. ULP EEPROM module

The internal ULP EEPROM interface contains an address register with bit addressing capabilities and auto-increment feature (modulo 32 bit for write access). The auto increment function allows reading of consecutive bytes/bits without additional access to the address register.

2.9 EEPROM content at delivery

The ULP EEPROM content is initialized with default values during device manufacturing (Table 91).

Table 91. ULP EEPROM content upon delivery

Content (hex) [1]	ULP Module	Page
xx xx xx xx	0	0 to 3 (SKC1)
00 00 00 00		4 to 7 (SKC3)
xx xx xx xx	0	8 to 63
xx xx xx xx	1	64 to 127
xx xx xx xx	2	128 to 191
xx xx xx xx	3	192 to 255
xx xx xx xx	4	256 to 319
xx xx xx xx	5	320 to 383
xx xx xx xx	6	384 to 447
xx xx xx xx	7	448 to 487, 489, 491, 493, 495
00 00 00 00		496, 498, 500, 502 (Trip Counter value)
00 00 55 00		497, 499, 501, 503 (Trip Counter date, attack)
01 00 00 00		504 (SEG0_SZ = 1)

Content (hex) [1]	ULP Module	Page
00 00 00 00		505
8A 00 00 00		506 (SEG0_AM ciphered R/W access only)
00 00 00 00		507
xx xx xx xx		508
xx xx xx A5		509 (BLANK)
xx xx xx xx		510, 511
xx xx xx xx	15	960 to 975, 992 to 1021
00 00 90 00		976
00 00 00 01		977
00 00 00 00		978
07 E7 40 86		979
53 73 03 63		980
00 00 00 00		981 to 991
xx 1A 00 36 [2]		1022
xx xx xx B0		1023

[1] Locations marked 'x' are undefined and may hold any pattern.
[2] Setting valid for NCF215A

The EEPROM content may be changed as desired by the application, except for the pages 960 to 975 and 992 to 1023.

Bit 7 to 4 of page 1023 serve the function of a product type identifier (PI) and are set to '1011b' (see Section 2.8.2.1).

Bit 16 to 23 of page 1022 serve the function of an enhanced product type identifier (EPI) and are set to '0001 1010b' for NCF215A (see Section 2.8.2.2).

2.10 Interrupt system

The NCF215A / NCF215B contains an interrupt controller featuring 15 hardware interrupt priority levels. If more than one hardware interrupt request is pending at the same time the source with the highest request level is selected, independent of the RISC controller privilege mode (SYSTEM or USER mode).

The priority levels for LF field detection, CPU/MMU exception and user hardware interrupts are fixed. All user hardware interrupts use one common interrupt vector, which address is defined by the application via a dedicated SFR. This allows flexible software controlled handling of interrupt priorities, dynamic assignment of different interrupt service routines and the definition of distinct interrupt service routines for different applications.

The application can switch dynamically between single or nested interrupt execution and it can decide whether a selected event causes an interrupt or a wake-up event. If an interrupt is enabled, it causes the RISC controller to perform a CALL operation to the configured location, where execution of the Interrupt Service Routine (ISR) starts.

User interrupts (maskable and non-maskable) are usually disabled during the execution of system code (SYS instructions). In this case any interrupt request is latched and

execution is delayed until control is returned to the application code. Please note that the system is basically able to allow user interrupts also during execution of system code. Any system call using this feature will describe this behavior explicitly.

2.10.1 Interrupt sources

The interrupt sources are summarized in Table 92. Every interrupt source has a dedicated interrupt request flag. Maskable interrupts have additionally an interrupt enable bit. If an interrupt source is used as user and system interrupt two different interrupt enable bits are provided to allow separate control in every mode.

The supported interrupt types are maskable system interrupts (System), maskable user interrupts (User) and non-maskable user interrupts (User NMI). Interrupt sources can be level sensitive or edge sensitive.

Table 92. Interrupt sources

Interrupt Description	Interrupt type	Sensitivity
LF field interrupt	User NMI, System	Edge
CPU/MMU exception interrupt	User NMI, System	Edge
Port interrupt	User	Edge
Timer 0 interrupt	User, System	Edge
Timer 1 compare interrupt	User, System	Edge
Timer 1 capture interrupt	User, System	Edge
Alternative port interrupt	User	Edge
System timer 0 interrupt	System	Level
Immobilizer interface unit interrupt	User, System	Level
ULP EEPROM interrupt	User, System	Edge
ADC interrupt	User, System	Edge
AES calculation unit interrupt	User, System	Edge
Random number generator interrupt	User, System	Edge
RSSI interrupt	User	Level
Interval timer and real time clock interrupt	User	Level
LF active preprocessor interrupt	User	Level
SPI 0 interrupt	User	Level
SPI 1 interrupt	User	Level
Timer 2 interrupt	User	Edge
LF active monitors interrupt	User	Level
Motion sensor interface interrupt	User	Level
VBAT brownout monitor interrupt	User	Level [1]

[1] The source of this interrupt is the registered VBAT brownout monitor flag, bit VBATBRNREG in PCON2, which implies a special treatment for reading or clearing the interrupt flag

A level sensitive interrupt has a transparent interrupt request flag, which is set as long as the request remains active (Figure 39). A level sensitive interrupt cannot be cleared

directly since the interrupt request flag is transparent. Thus, a level sensitive interrupt request has to be cleared by acknowledging the event in the corresponding peripheral.

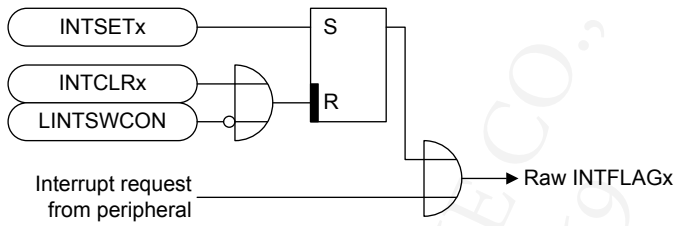


Figure 39. Interrupt request flag for level sensitive interrupts

An edge sensitive interrupt uses an edge detector as interrupt request flag (Figure 40). Edge sensitive interrupts shall be acknowledged by clearing the interrupt request flag via the application program. This is necessary, as several interrupts use a common interrupt vector and the system cannot determine which one is served by the application, if several interrupts occur simultaneously.

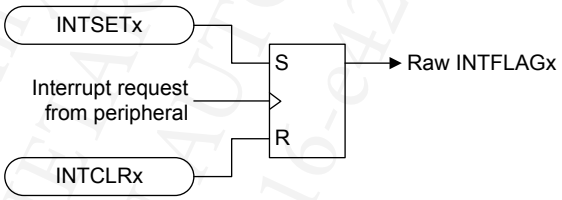


Figure 40. Interrupt request flag for edge sensitive interrupts

Non-maskable user interrupts are a specific form of edge sensitive interrupt sources.

Non-maskable interrupts have dedicated interrupt vectors. The interrupt request flag is cleared automatically when the interrupt is vectored (Figure 41).

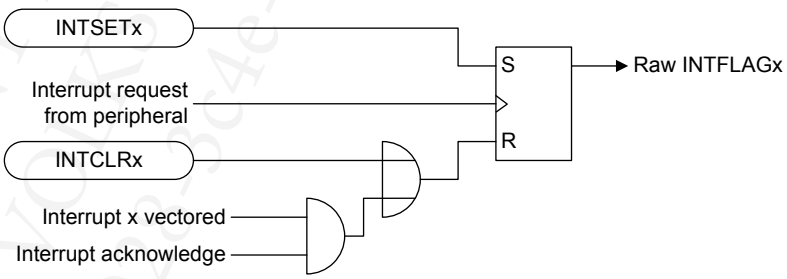


Figure 41. Interrupt request flag for non-maskable user interrupts

2.10.1.1 Interrupt vector addresses

The interrupt vector addresses depend on the interrupt type (Table 93).

Table 93. Interrupt vector addresses

Interrupt source	Address range	Address (word address)
Break interrupt	SYSTEM	0002h
Maskable system interrupt	SYSTEM	0040h
CPU/MMU exception interrupt (user NMI)	SYSTEM	0016h
	USER	000Eh
LF field interrupt (user NMI)	SYSTEM	000Ch
	USER	0006h
Maskable user interrupt	USER	Selectable (INTVEC)

All interrupt sources except the maskable user interrupt are called in SYSTEM mode and have fixed interrupt addresses.

Directly after vectoring a non-maskable user interrupt in SYSTEM mode, a USER call (call-back) is generated to return to USER mode and to proceed the program execution at the corresponding interrupt vector address in the USER address range (0006h or 000Eh for the LF or CPU/MMU exception interrupt, respectively).

The maskable user interrupt features a configurable interrupt vector address by use of the special function register INTVEC. This gives the following possibilities:

- Define different interrupt service routines for different applications
- Define different interrupt service routines with different priority schemes (even in one application)
- Allow dynamic switching of interrupt service routines in an application (e.g. to provide different priority schemes)

2.10.2 Interrupt priorities

2.10.2.1 Interrupt request levels

The interrupt controller processes the events from the peripherals and generates an interrupt request with the interrupt request level for every source. All interrupt sources are synchronized to the CPU clock before they generate an interrupt request (Figure 42).

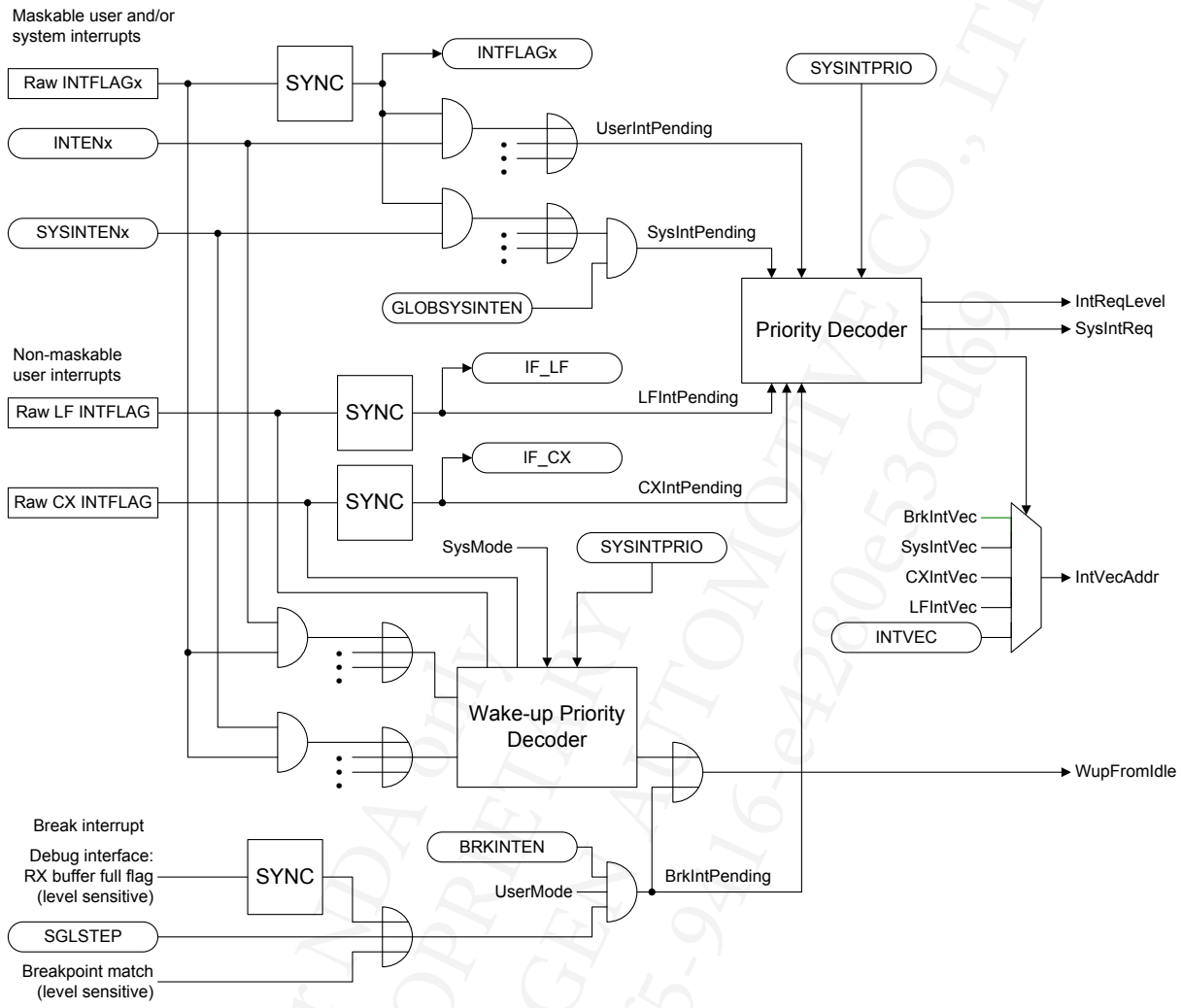


Figure 42. Priority decoding with interrupt controller

Table 94 summarizes the interrupt request levels and their assignment to interrupt events. If more than one interrupt request is pending at the same time the source with the highest request level is selected, independent of the privilege mode (SYSTEM or USER mode).

Table 94. Interrupt request level assignment to interrupt events

Interrupt request level	Source
15	Break interrupt
	Maskable system interrupt (SYSINTPRIO= 11b, GLOBSYSINTEN = 1)
14	CPU/MMU exception interrupt (user NMI)
13	LF field interrupt (user NMI)
12	Reserved for future use
11	Maskable system interrupt (SYSINTPRIO= 10b, GLOBSYSINTEN = 1)

Interrupt request level	Source
10	Maskable system interrupt (SYSINTPRIO= 01b, GLOBSYSINTEN = 1)
9 to 3	Reserved for future use
2	Maskable user interrupt
1	Maskable system interrupt (SYSINTPRIO= 00b, GLOBSYSINTEN = 1)

System interrupts (except the LF field and CPU/MMU exception interrupts) are usually disabled (i.e. GLOBSYSINTEN = 0). It will be stated explicitly, if any system function makes use of system interrupts.

2.10.2.2 Interrupt priority levels

The responsiveness to hardware interrupt requests is controlled by the interrupt priority level. After device reset the CPU starts with interrupt priority level 15 in SYSTEM mode.

The CPU always operates in a certain interrupt priority level ranging from 0 to 15. An interrupt request is granted, if the hardware interrupt request level is greater than the current interrupt priority level of the CPU (exception: break interrupt, see below).

The following actions are executed when an interrupt is served:

- The current interrupt priority level, the privilege mode (SYSTEM or USER mode), the program counter and the flags are pushed on the stack
- The priority level is set to the new interrupt request level (i.e. it is increased)
- If necessary the privilege mode is changed
- The program counter is set to the provided interrupt vector address

The interrupt priority level increases with every acknowledged interrupt, hence all interrupts with the same or lower priority are inhibited. Consequently, once the interrupt priority level reaches the value 15 all further interrupt requests are ignored.

At the end of an interrupt service routine the command RETI triggers the following operations:

- The content stored at the beginning of the interrupt service routine is popped from the stack (including the stored interrupt priority level and privilege mode)
- The interrupt priority level is set to the stored value
- If necessary the privilege mode is changed
- The program counter is set to the stored value where the program was interrupted.

A RETI command decreases the interrupt priority level unless nested interrupts were used (see Section 2.10.2.3).

The interrupt request level 0 means that no hardware interrupt is pending. Level 0 cannot be used as request level as such an interrupt would never be served.

2.10.2.3 Interrupt priority level adjustment

The interrupt priority level can be changed in the allowed range by the application program with the dedicated command SIL, considering following restrictions dependent on the privilege mode:

- In USER mode the interrupt priority levels can be set to values from 0 to 10. Any attempt to set it to a higher value will yield value 10 instead.
- In SYSTEM mode, all values from 0 to 15 can be selected.

If the interrupt priority level is set to 10, all maskable user interrupts are disabled.

The modification of the interrupt priority level can be used to allow and inhibit interrupts (interrupt nesting).

2.10.2.4 Break interrupt

The break interrupt is active only in USER mode and causes the device to switch to SYSTEM mode immediately. The break interrupt has the highest interrupt request level and is executed independently of the current interrupt priority level (i.e. it is executed even though the interrupt priority level is at its maximum value 15).

The following sources can generate a break interrupt:

- A hardware breakpoint is reached
- The single step bit SINGLESTEP is set
- The monitor and download interface received a command that causes an interruption of the application program in USER mode

Acknowledgement of the break interrupt sets the interrupt priority level to 15.

2.10.2.5 LF field and CPU/MMU exception interrupts

The LF field and CPU/MMU exception non-maskable user interrupts have an interrupt request level (13 and 14 respectively) which are higher than the maximum possible interrupt execution level in USER mode (10). These two interrupt sources are not gated with GLOBSYSINTEN, thus the LF field and CPU/MMU exception interrupts are always vectored when the device is in USER mode.

The LF field and CPU/MMU exception interrupts are vectored in SYSTEM mode. Directly afterwards a USER call (call back) is generated to return the execution to the user program. Although the interrupt request level of the LF field and CPU/MMU exception NMIs are higher than 10 the execution of the USER call is executed with interrupt execution level 10.

Consequently, if the user call was caused by an LF field interrupt it is granted that an emerging CPU/MMU exception interrupt is properly recognized later on (and vice versa).

If the device runs in SYSTEM mode the LF field and CPU/MMU exception interrupts are treated as any other interrupt source and they are only vectored, if the interrupt request level exceeds the current interrupt execution level. An application in SYSTEM mode can therefore select whether an LF field or CPU/MMU interrupt shall be vectored or not.

2.10.3 Interrupt request by software

It is possible to trigger an interrupt request for every interrupt source by software. This could be helpful e.g. during software development in order to support convenient and efficient testing of the interrupt service routines. Every interrupt request flag has two assigned control bits to set (INTSETx) and to clear (INTCLRx) the corresponding interrupt request flag.

For edge sensitive interrupt sources there is no difference whether the interrupt was triggered by the peripheral or by the software. In both cases the application program has to acknowledge the interrupt via bit INTCLRx (unless it was a non-maskable user interrupt).

The software trigger for level sensitive interrupt sources is only supported, if this feature is released by setting the global control bit LINTSWCON. As a level sensitive interrupt

does not have a storage element in the interrupt controller a parallel flip-flop is necessary to generate an interrupt request by software. The output of this flip-flop is logically ORed to the genuine level sensitive interrupt source. In contrast to the normal behavior of a level sensitive interrupt the software triggered interrupt request shall be acknowledged via the corresponding bit INTCLRx. Please note that bit INTCLRx does not have any influence on the genuinely generated interrupt request from the peripheral.

2.10.4 Software interrupts

Software interrupts are initiated via a system call (SYS command) or user call (USR command) and are not affected by the current interrupt priority level, thus they are always executed. Software interrupts allow switching the privilege mode (SYSTEM or USER mode).

Software interrupts influence the interrupt priority level dependent on the privilege mode.

USER mode, execution of a system call (SYS):

- The privilege mode changes to SYSTEM mode
- The interrupt priority level is set to 15

USER mode, execution of a user call (USR):

- The privilege mode and the priority level do not change

SYSTEM mode, execution of a system call (SYS):

- The privilege mode and the priority level do not change.

SYSTEM mode, execution of a user call (USR):

- The privilege mode changes to USER mode
- The interrupt priority level is set to 10

User calls in USER mode and system calls in SYSTEM mode are handled like normal call routines with the difference that these routines shall finish with a RETI instead of a normal RET command.

2.10.5 Wake-up from IDLE mode

The wake-up from IDLE mode is controlled by the interrupt controller. Even if the interrupts are globally disabled, it is possible to select the wake-up from IDLE mode function. Once the CPU is in IDLE mode it resumes operation as soon as the wake-up signal becomes active.

The wake-up from IDLE mode is controlled with the interrupt enable and system interrupt enable bits. A wake-up from IDLE mode is generated under the following circumstances:

- The device is in USER mode and a source is pending, which is enabled by its (user) interrupt enable bit
- The device is in USER mode and a non-maskable user interrupt is pending
- The device is in USER mode and a break interrupt is pending
- The device is in SYSTEM mode and a source is pending, which is enabled by its system interrupt enable bit
- A source is pending which generates an interrupt (mode independent, but dependent on the current interrupt priority level and interrupt request level)

The bit GLOBSYSINTEN has no influence on the wake-up from IDLE mode when the device operates in SYSTEM mode. However, it disables all system interrupts also in

USER mode, thus in USER mode a pending system interrupt source will not cause a wake-up from IDLE mode.

If more than one wake-up source is selected or either system interrupts in USER mode or user interrupts in SYSTEM mode can occur, it is recommended to use a safe routine for the invocation of the IDLE mode where the interesting interrupt flag is checked additionally.

Example: The routine uses the IDLE mode in USER mode safely although a system interrupt is enabled. Even if this routine is interrupted, it will work as intended and will not finish the routine prematurely.

```
INTCLR0.val = 0x08;
while ((INTFLAG0.val & 0x08) == 0) go_idle();
```

2.10.6 System and user stack

The NCF215A / NCF215B has a system and a user stack. If the device executes in SYSTEM mode all data is pushed on and popped from the system stack. The same applies for the user stack if the device is in USER mode.

Every interrupt invocation stores 2 words on the stack, the return address and the flags (including the system mode flag and the interrupt priority level).

If an interrupt request causes a change of the privilege mode, the return address is pushed on the current stack and the flags are pushed on the target stack (e.g. if a USR call is executed in SYSTEM mode, the return address is pushed on the system stack and the flags are pushed on the user stack).

If a return from interrupt is executed, the flags are popped from the current stack. Dependent on the popped system mode flag the controller might perform a privilege mode switch and then pops the return address from the target stack (e.g. if the USR call finishes with a RETI and the device branches back to SYSTEM mode, the return address is retrieved from the system stack again).

2.10.7 Registers

The register groups 0 to 2 of the interrupt controller allow either byte or word access (Table 95). For register group 3, only byte access is meaningful.

Table 95. Word and byte access to interrupt controller registers

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
INTENW0	INTEN1	INTEN0
INTENW1	INTEN2	INTEN1
SYSINTENW0	SYSINTEN1	SYSINTEN0
INTFLAGW0	INTFLAG1	INTFLAG0
INTFLAGW1	INTFLAG2	INTFLAG1
INTSETW0	INTSET1	INTSET0
INTSETW1	INTSET2	INTSET1
INTCLRW0	INTCLR1	INTCLR0
INTCLRW1	INTCLR2	INTCLR1

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
INTVEC	INTVECH	INTVECL

2.10.7.1 Interrupt control register INTCON

The INTCON register defines the behavior of the system interrupts and is write accessible in SYSTEM mode only.

Table 96. Interrupt control register INTCON (reset value 00h)

Bit	Symbol	Access SYSTEM mode	Access USER mode	Value	Description
7	LINTSWCON	R/W	R/-		Software control of level sensitive interrupts
				0	Software control of level sensitive interrupts disabled
				1	Interrupt flags controlled by application
6	GLOBSYSINTEN	R/W	R/-		Global system interrupt enable
				0	System interrupts are disabled
				1	System interrupts are enabled
5 to 4	SYSINTPRIO[1:0]	R/W	R/-		System Interrupt Priority
				00	System interrupts have lowest priority. System interrupts can be disabled in USER mode.
				01	System interrupts have higher priority than maskable user interrupts but lower priority than the non-maskable user interrupt. System interrupts can be disabled in USER mode.
				10	System interrupts have higher priority than maskable user interrupts but lower priority than the non-maskable user interrupt. System interrupts cannot be disabled in USER mode.
				11	System interrupts have highest priority. System interrupts cannot be disabled in USER mode.
3 to 0	RFU	-/W0	-/-		Reserved for future use

LINTSWCON, Software control of level sensitive interrupts

If this bit is set to '1', the interrupt flags of level sensitive interrupt sources can be controlled by the application via the corresponding interrupt set and interrupt clear bit.

SYSINTPRIO[1:0], System interrupt priority

If an interrupt source has the user interrupt enable flag and the system interrupt enable flag set to '1' simultaneously, it depends on the settings of GLOBSYSINTEN and SYSINTPRIO whether this interrupt is served as a user or system interrupt.

2.10.7.2 Interrupt enable registers INTENx

The INTENx registers control the selection of user interrupts and sources for wake-up from IDLE mode. These registers are also used to accomplish interrupt masking.

Table 97. User interrupt enable register INTEN0 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	RFU	-/W0		Reserved for future use
6	IE_ALTPORT	R/W		Alternative port interrupt
			0	Interrupt disabled
			1	Interrupt enabled
5	IE_T1CAP	R/W		Timer 1 capture interrupt
			0	Interrupt disabled
			1	Interrupt enabled
4	IE_T1CMP	R/W		Timer 1 compare interrupt
			0	Interrupt disabled
			1	Interrupt enabled
3	IE_T0	R/W		Timer 0 interrupt
			0	Interrupt disabled
			1	Interrupt enabled
2	IE_PORT	R/W		Port interrupt
			0	Interrupt disabled
			1	Interrupt enabled
1	IE_CXNMI	R/W		CPU/MMU exception non-maskable interrupt
			0	Generate device reset
			1	Generate non-maskable user interrupt
0	IE_LFNMI	R/W		LF non-maskable interrupt
			0	Generate device reset
			1	Generate non-maskable user interrupt

IE_PORT and IE_ALTPORT, regular and alternative port interrupt enable

When IE_PORT is set, a regular port interrupt will be enabled following the wake-up configuration settings in the PRESWUPx registers, and the individual port interrupt disable register, PxINTDIS. Unlike the regular port interrupt, when IE_ALTPORT set, the alternative port interrupt will follow only the disable configuration in PxINTDIS and will be generated on both edges - falling and rising, regardless on port resistor and wake-up settings in PRESWUPx.

IE_CXNMI, CPU/MMU exception non-maskable interrupt enable

The bit IE_CXNMI is intended to select whether a CPU/MMU exception generates a device reset or a non-maskable user interrupt request.

IE_LFNMI, LF non-maskable interrupt enable

The bit IE_LFNMI is intended to select whether an emerging LF field generates a device reset or a non-maskable user interrupt request.

Table 98. User interrupt enable register INTEN1 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	IE_RSSI	R/W		RSSI interrupt
			0	Interrupt disabled
			1	Interrupt enabled
6	RFU	-/W0		Reserved for future use
5	IE_RNG	R/W		Random number generator interrupt
			0	Interrupt disabled
			1	Interrupt enabled
4	IE_AES	R/W		AES calculation unit interrupt
			0	Interrupt disabled
			1	Interrupt enabled
3	IE_ADC	R/W		ADC interrupt
			0	Interrupt disabled
			1	Interrupt enabled
2	RFU	-/W0		Reserved for future use
1	IE_ULP	R/W		ULP EEPROM interrupt
			0	Interrupt disabled
			1	Interrupt enabled
0	IE_IIU	R/W		Immobilizer interface unit interrupt
			0	Interrupt disabled
			1	Interrupt enabled

Table 99. User interrupt enable register INTEN2 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	IE_VBATBRN	R/W		VBAT brownout monitor interrupt
			0	Interrupt disabled
			1	Interrupt enabled
6	IE_MSI	R/W		Motion sensor interface interrupt
			0	Interrupt disabled
			1	Interrupt enabled
5	IE_LFAMON	R/W		LF active monitors interrupt
			0	Interrupt disabled
			1	Interrupt enabled
4	IE_T2	R/W		Timer 2 interrupt
			0	Interrupt disabled
			1	Interrupt enabled
3	IE_SP1	R/W		SPI 1 interrupt

Bit	Symbol	Access	Value	Description
			0	Interrupt disabled
			1	Interrupt enabled
2	IE_SP0	R/W		SPI 0 interrupt
			0	Interrupt disabled
			1	Interrupt enabled
1	IE_PP	R/W		LF active preprocessor interrupt
			0	Interrupt disabled
			1	Interrupt enabled
0	IE_IT	R/W		Interval timer and real time clock interrupt
			0	Interrupt disabled
			1	Interrupt enabled

2.10.7.3 System interrupt enable register SYSINTENx

These registers control the selection of system interrupts and sources for wake-up from IDLE mode. Write access is granted only in SYSTEM mode.

Table 100. System interrupt enable register SYSINTEN0 (reset value 00h)

Bit	Symbol	Access SYSTEM mode	Access USER mode	Value	Description
7	SIE_ST0	R/W	R/-		System Timer 0 interrupt
				0	Interrupt disabled
				1	Interrupt enabled
6	RFU	-/W0	-/-		Reserved for future use
5	SIE_T1CAP	R/W	R/-		Timer 1 capture system interrupt
				0	Interrupt disabled
				1	Interrupt enabled
4	SIE_T1CMP	R/W	R/-		Timer 1 compare system interrupt
				0	Interrupt disabled
				1	Interrupt enabled
3	SIE_T0	R/W	R/-		Timer 0 system interrupt
				0	Interrupt disabled
				1	Interrupt enabled
2 to 0	RFU	-/W0	-/-		Reserved for future use

Table 101. System interrupt enable register SYSINTEN1 (reset value 00h)

Bit	Symbol	Access SYSTEM mode	Access USER mode	Value	Description
7 to 6	RFU	-/W0	-/-		Reserved for future use
5	SIE_RNG	R/W	R/-		Random number generator interrupt
				0	Interrupt disabled
				1	Interrupt enabled
4	SIE_AES	R/W	R/-		AES calculation unit interrupt
				0	Interrupt disabled
				1	Interrupt enabled
3	SIE_ADC	R/W	R/-		ADC interrupt
				0	Interrupt disabled
				1	Interrupt enabled
2	RFU	-/W0	-/-		Reserved for future use
1	SIE_ULP	R/W	R/-		ULP EEPROM interrupt
				0	Interrupt disabled
				1	Interrupt enabled
0	SIE_IIU	R/W	R/-		Immobilizer interface unit interrupt
				0	Interrupt disabled
				1	Interrupt enabled

2.10.7.4 Interrupt request flag registers INTFLAGx

The registers INTFLAGx signal interrupt requests pending that were generated by the corresponding peripheral. These registers give read access to the synchronized interrupt request flags. Any write access is ignored.

Table 102. Interrupt request flag register INTFLAG0 (reset value XXh)

Bit	Symbol	Access	Value	Description
7	IF_ST0	R/-		System timer 0 interrupt
			0	No interrupt request
			1	Interrupt request
6	IF_ALTPORT	R/-		Alternative port interrupt
			0	No interrupt request
			1	Interrupt request
5	IF_T1CAP	R/-		Timer 1 capture interrupt
			0	No interrupt request
			1	Interrupt request
4	IF_T1CMP	R/-		Timer 1 compare interrupt
			0	No interrupt request
			1	Interrupt request

Bit	Symbol	Access	Value	Description
3	IF_T0	R/-		Timer 0 interrupt
			0	No interrupt request
			1	Interrupt request
2	IF_PORT	R/-		Port interrupt
			0	No interrupt request
			1	Interrupt request
1	IF_CX	R/-		CPU/MMU exception non-maskable interrupt
			0	No interrupt request
			1	Interrupt request
0	IF_LF	R/-		LF field non-maskable interrupt
			0	No interrupt request
			1	Interrupt request

Table 103. Interrupt request flag register INTFLAG1 (reset value XXh)

Bit	Symbol	Access	Value	Description
7	IF_RSSI	R/-		RSSI interrupt
			0	No interrupt request
			1	Interrupt request
7	RFU	-/-		Reserved for future use
5	IF_RNG	R/-		Random number generator interrupt
			0	No interrupt request
			1	Interrupt request
4	IF_AES	R/-		AES calculation unit interrupt
			0	No interrupt request
			1	Interrupt request
3	IF_ADC	R/-		ADC interrupt
			0	No interrupt request
			1	Interrupt request
2	RFU	R/-		Reserved for future use
1	IF_ULP	R/-		ULP EEPROM interrupt
			0	No interrupt request
			1	Interrupt request
0	IF_IIU	R/-		Immobilizer interface unit interrupt
			0	No interrupt request
			1	Interrupt request

Table 104. Interrupt request flag register INTFLAG2 (reset value XXh)

Bit	Symbol	Access	Value	Description
7	IF_VBATBRN	R/-		VBAT brownout monitor interrupt
			0	No interrupt request
			1	Interrupt request
6	IF_MSI	R/-		Motion sensor interface interrupt
			0	No interrupt request
			1	Interrupt request
5	IF_LFAMON	R/-		LF active monitors interrupt
			0	No interrupt request
			1	Interrupt request
4	IF_T2	R/-		Timer 2 interrupt
			0	No interrupt request
			1	Interrupt request
3	IF_SP1	R/-		SPI 1 interrupt
			0	No interrupt request
			1	Interrupt request
2	IF_SP0	R/-		SPI 0 interrupt
			0	No interrupt request
			1	Interrupt request
1	IF_PP	R/-		LF active preprocessor interrupt
			0	No interrupt request
			1	Interrupt request
0	IF_IT	R/-		Interval timer and real time clock interrupt
			0	No interrupt request
			1	Interrupt request

2.10.7.5 Interrupt set registers INTSETx

The INTSETx registers can be used to trigger a corresponding interrupt request by software. Reading of these registers is not supported and will yield '0'.

Table 105. Interrupt set register INTSET0 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	IS_ST0	R0/W		System Timer 0 interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
6	IS_ALTPORT	R0/W		Alternative port interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
5	IS_T1CAP	R0/W		Timer 1 capture interrupt

Bit	Symbol	Access	Value	Description
			0	Interrupt request unchanged
			1	Set interrupt request
4	IS_T1CMP	R0/W		Timer 1 compare interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
3	IS_T0	R0/W		Timer 0 interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
2	IS_PORT	R0/W		Port interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
1	IS_CX	R0/W		CPU/MMU non-maskable interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
0	IS_LF	R0/W		LF non-maskable interrupt
			0	Interrupt request unchanged
			1	Set interrupt request

Table 106. Interrupt set register INTSET1 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	IS_RSSI	R0/W		RSSI interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
6	RFU	R0/W0		Reserved for future use
5	IS_RNG	R0/W		Random number generator interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
4	IS_AES	R0/W		AES calculation unit interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
3	IS_ADC	R0/W		ADC interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
2	RFU	R0/W0		Reserved for future use
1	IS_ULP	R0/W		ULP EEPROM interrupt
			0	Interrupt request unchanged

Bit	Symbol	Access	Value	Description
			1	Set interrupt request
0	IS_IIU	R0/W		Immobilizer interface unit interrupt
			0	Interrupt request unchanged
			1	Set interrupt request

Table 107. Interrupt set register INTSET2 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	IS_VBATBRN	R0/W		VBAT brownout monitor interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
6	IS_MSI	R0/W		Motion sensor interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
5	IS_LFAMON	R0/W		LF active monitors interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
4	IS_T2	R0/W		Timer 2 interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
3	IS_SP1	R0/W		SPI 1 interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
2	IS_SP0	R0/W		SPI 0 interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
1	IS_PP	R0/W		LF active preprocessor interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
0	IS_IT	R0/W		Interval timer and real time clock interrupt
			0	Interrupt request unchanged
			1	Set interrupt request

2.10.7.6 Interrupt clear registers INTCLRx

The INTCLRx registers can clear a corresponding interrupt request by software. Reading of these registers is not supported and will yield '0'.

Table 108. Interrupt clear register INTCLR0 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	IC_ST0	R0/W		System timer 0 interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
6	IC_ALTPORT	R0/W		Alternative port interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
5	IC_T1CAP	R0/W		Timer 1 capture interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
4	IC_T1CMP	R0/W		Timer 1 compare interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
3	IC_T0	R0/W		Timer 0 interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
2	IC_PORT	R0/W		Port interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
1	IC_CX	R0/W		CPU/MMU exception non-maskable interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
0	IC_LF	R0/W		LF non-maskable interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request

Table 109. Interrupt clear register INTCLR1 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	IC_RSSI	R0/W		RSSI interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
6	RFU	R0/W0		Reserved for future use
5	IC_RNG	R0/W		Random number generator interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
4	IC_AES	R0/W		AES calculation unit interrupt
			0	Interrupt request unchanged

Bit	Symbol	Access	Value	Description
			1	Clear interrupt request
3	IC_ADC	R0/W		ADC interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
2	RFU	R0/W0		Reserved for future use
1	IC_ULP	R0/W		ULP EEPROM interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
0	IC_IIU	R0/W		Immobilizer interface unit interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request

Table 110. Interrupt clear register INTCLR2 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	IC_VBATBRN	R0/W		VBAT brownout monitor interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
6	IC_MSI	R0/W		Motion sensor interface interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
5	IC_LFAMON	R0/W		LF active monitors interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
4	IC_T2	R0/W		Timer 2 interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
3	IC_SP1	R0/W		SPI 1 interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
2	IC_SP0	R0/W		SPI 0 interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
1	IC_PP	R0/W		LF active preprocessor interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
0	IC_IT	R0/W		Interval timer and real time clock interrupt

Bit	Symbol	Access	Value	Description
			0	Interrupt request unchanged
			1	Clear interrupt request

2.10.7.7 User interrupt vector address INTVEC

The INTVEC register features a configurable interrupt vector address for the maskable user interrupt.

Table 111. User interrupt vector address INTVEC (reset value 0040h)

Bit	Symbol	Access	Value	Description
15 to 8	INTVECH [7:0]	R/W		User interrupt vector address High Byte (MSByte)
7 to 0	INTVECL [7:0]	R/W		User interrupt vector address Low Byte (LSByte)

2.11 Timer/Counter 0, 2

Timer/Counter 0 and Timer/Counter 2 are identical.

Timer/Counter 0/2 is a 16 bit timer/counter with 12 bit pre-scaler and can operate as interval and event counter, as digital modulator or as clock divider. Timer 0/2 is also suitable as alternative clock source for the immobilizer interface unit and digital modulator.

Timer 0/2 has two operating modes, auto-reload mode and single shot mode, which are selected by bit TxSGL. For auto-reload mode, a 16 bit reload register is provided (see Figure 43).

Different clock sources can be applied (RCCLK/2, XCLK, TMUX0CLK, TMUX1CLK). The timer can run with the undivided clock to achieve a best possible resolution even with slow clock sources.

If Timer 0/2 reaches the zero value, an interrupt is generated and a control line (TxLINE) can be set, cleared or toggled. This allows the creation of a synchronized digital bit stream or a divided clock output. The output TxLINE of Timer 0/2 is connected to selected I/O ports and it is available as capture input for Timer 1.

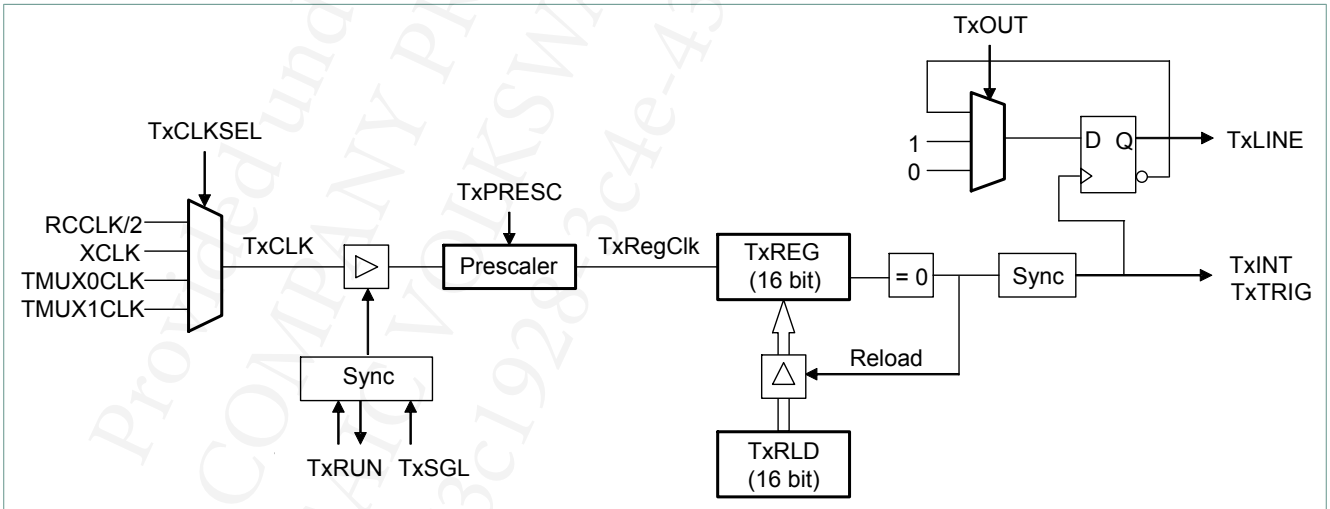


Figure 43. Block diagram of Timer 0/2

The timer starts by loading the reload value from register TxRLD into register TxREG. Afterwards, it counts down automatically. Reaching the zero value, timer register TxREG is reloaded with the value from reload register TxRLD, an interrupt request is generated and other peripheral functions are triggered.

The timer is clocked with the output of the pre-scaler. The clock for the timer register is:

$$TxRegClk = 2^{TxPRESC} \cdot TxCLK \qquad \text{for } TxPRESC < 13 \tag{10}$$

The timer interval becomes:

$$\begin{aligned} TxINTERVAL &= 2 \cdot TxCLK && \text{for } TxPRESC = 0 \text{ and } TxRDL = 0 \\ TxINTERVAL &= (TxRDL + 1) \cdot TxRegClk && \text{for all other settings} \end{aligned} \tag{11}$$

2.11.1 Registers

2.11.1.1 Timer 0/2 register TxREG

Timer 0/2 supports read access to the timer register. The content of the timer register is not buffered or synchronized. Therefore, reading of TxREG is only recommended when the timer is stopped (TxRUN = 0). When the timer is running reading of TxREG can generate unstable and wrong values as the timer value is not necessarily settled when reading takes place.

Write access to timer register TxREG is not supported.

Table 112. Timer 0/2 Register TxREG (reset value xx_xxh)

Bit	Symbol	Access	Value	Description
15 to 8	TxREGH [7:0]	R/-		Timer 0/2 Register High Byte (MSByte)
7 to 0	TxREGL [7:0]	R/-		Timer 0/2 Register Low Byte (LSByte)

2.11.1.2 Timer 0/2 control register TxCON0

Timer 0/2 is operated and controlled by Timer 0/2 Control Registers 0 and 1.

Table 113. Timer 0/2 Control Register TxCON0 (reset value 00h)

Bit	Symbol	Access	Value	Description
7 to 6	TxOUT [1:0]	R/W		Timer 0/2 output line configuration
			00	Value unchanged, output line flip-flop after timer reset 0
			01	Value is set to ‘0’, output line flip-flop after timer reset 0
			10	Value toggles, output line flip-flop after timer reset 0
			11	Value is set to ‘1’, output line flip-flop after timer reset 1
5 to 3	RFU	-/W0		Reserved for future use
2	TxSGL	R/W		Timer 0/2 single shot
			0	Timer 0/2 is configured in auto reload mode
			1	Timer 0/2 is configured in single shot mode

Bit	Symbol	Access	Value	Description
1	TxRST	R0/W		Timer 0/2 reset
			0	No effect
			1	Timer reset
0	TxRUN	R/W		Timer 0/2 run
			0	Timer 0/2 is stopped
			1	Timer 0/2 is running. While reading, a 1 can also indicate the synchronization phase for start or stop

TxOUT[1:0], Timer 0/2 output line configuration

Timer 0/2 has an output line flip-flop driving the signal TxLINE. The behavior of this signal can be configured with the output line configuration bits TxOUT. The content of the output flip-flop is updated every time the timer register reaches zero. The initial value of the output line flip-flop after a reset of Timer 0/2 can also be controlled with TxOUT.

If bit TxOUT[0] is set, it is possible to generate a synchronized bit data stream by writing the desired data to bit TxOUT[1]. The output line is then updated with the new data bit when the timer register reaches the value zero for the next time.

The selection of TxOUT = 10 allows the generation of a divided clock output with 50 % duty cycle.

TxSGL, Timer 0/2 single shot

Timer 0/2 has two different operating modes: an auto-reload mode and a single shot mode. If bit T0SGL is set, Timer 0/2 operates in single shot mode. If the timer is started by setting the bit T0RUN to '1' the counter starts decrementing until the timer register reaches zero. Simultaneously an interrupt is generated and the timer stops automatically. This clears bit TxRUN and reloads the timer register TxREG. The bit TxSGL itself is not influenced and stays '1'.

TxRST, Timer 0/2 reset

The reset bit TxRST can be used to generate an asynchronous reset of Timer 0/2 comprising the prescaler, the synchronization logic and the output line flip-flop. Moreover the current content of the reload register TxRLD is loaded into timer register TxREG. A '1' shall be written to TxRST to execute the reset. Writing a '0' has no effect and reading of TxRST always yields '0'.

Launching a reset when the timer is running causes the timer to stop immediately and TxRUN is cleared. If TxRST and TxRUN are set simultaneously the reset bit has priority and the timer does not start.

TxRUN, Timer 0/2 run

Timer 0/2 can be started and stopped with the control bit TxRUN. Reading TxRUN gives the current status of Timer 0/2. If a '1' is written to TxRUN the timer is enabled and it starts counting with the rising edge of TxCLK. Writing a '0' to TxRUN forces the timer to stop operation. Every change of signal TxRUN is synchronized to TxCLK before it becomes effective. Reading of TxRUN yields '1' if the timer is running and during the synchronization phase to start and stop the timer.

2.11.1.3 Timer 0/2 control register TxCON1

Timer 0/2 control register 1 stores the selection of the prescaler value TxPRESC[3:0] and the used clock source TxCLKSEL[1:0].

The control bits in register TxCON1 are not buffered nor synchronized to the timer clock TxCLK. The content of register TxCON1 shall only be modified, if the timer is stopped (TxRUN = 0). Any alteration of TxCON1 when the timer is running can cause unpredictable behavior.

Table 114. Timer 0/2 Control Register TxCON1 (reset value 00h)

Bit	Symbol	Access	Value	Description
7 to 6	RFU	-/W0		Reserved for future use
5 to 4	TxCLKSEL[1:0]	R/W		Timer 0/2 clock source selection
			00	RCCLK/2 (8 MHz nominal)
			01	External clock, XCLK
			10	Output of timer source multiplexer 0, TMUX0CLK
			11	Output of timer source multiplexer 1, TMUX1CLK
3 to 0	TxPRESC[3:0]	R/W		Timer 0/2 prescaler selection
			0000	TxREGClk = 1 * TxCLK
			0001	TxREGClk = 2 * TxCLK
			0010	TxREGClk = 4 * TxCLK
			0011	TxREGClk = 8 * TxCLK
			0100	TxREGClk = 16 * TxCLK
			0101	TxREGClk = 32 * TxCLK
			0110	TxREGClk = 64 * TxCLK
			0111	TxREGClk = 128 * TxCLK
			1000	TxREGClk = 256 * TxCLK
			1001	TxREGClk = 512 * TxCLK
			1010	TxREGClk = 1024 * TxCLK
			1011	TxREGClk = 2048 * TxCLK
			1100	TxREGClk = 4096 * TxCLK
			1101 to 1111	RFU

TxCLKSEL[1:0], Timer 0/2 clock source selection

The Timer 0/2 clock source selection selects the clock source.

TxPRESC[3:0], Timer 0/2 prescaler selection

The Timer 0/2 prescaler selection selects the clock speed for the timer register according to Equation 10.

2.11.1.4 Timer 0/2 reload register TxRLD

The reload register TxRLD is used to set the time-out interval of Timer 0/2. The behavior of any write access to register TxRLD depends on the current state of Timer 0/2.

If the timer is stopped (TxRUN = 0) any write access to TxRLD updates also the timer register with the new value and clears the prescaler. When the timer is started, the first interval corresponds to the newly selected time-out.

If the timer is running (TxRUN = 1), the reload register itself is not buffered and its value is taken to reload the timer register. Writing to register TxRLD at the same moment when the timer register is reloaded can cause unpredictable behavior. Therefore, when the timer is running the application shall only write the reload register if it is ensured that the write access is finished prior to the next timer underflow.

The reload register shall not be written in the time window from the request to stop the timer (setting TxRUN from '1' to '0') until the timer has stopped. If the timer is stopped by setting the reset bit TxRST, there is no limitation.

Table 115. Timer 0/2 Reload Register TxRLD (reset value xx_xxh)

Bit	Symbol	Access	Value	Description
15 to 8	TxRLDH [7:0]	R/W		Timer 0/2 Compare Register High Byte (MSByte)
7 to 0	TxRLDL [7:0]	R/W		Timer 0/2 Compare Register Low Byte (LSByte)

It is possible to use Timer 0/2 as 8 bit instead of a 16 bit counter in order to optimize the code density of the software. For this, register TxRLDH has to be set to zero once and the time-out interval is determined by setting TxRLDL.

2.12 Timer/Counter 1

Timer 1 is an 8/16 bit timer with 12 bit prescaler and is intended as interval and event counter for general purpose applications, as demodulator or signal generator and modulator. Together with Timer 0 it can be used as versatile clock measurement and/or trimming unit. Timer 1 features four operating modes (see Table 116).

Table 116. Operating Modes

Mode	Mode description
0	16 bit timer register with 16 bit compare and 16 bit capture register
1	16 bit timer register with 16 bit compare and 16 bit capture register in single shot operation
2	8 bit timer register with two 8 bit compare and two 8 bit capture registers
3	8 bit timer register with one 8 bit compare register, two 8 bit capture registers and one 8 bit guard time register for capture event processing

In all modes, an interrupt is generated if a compare event or a capture event is generated. Further, a reset upon capture and/or compare event is selectable. A capture event can be triggered on the signals rising edge, falling edge or on both signal edges, dependent on the configuration.

The input signal which is used as capture source is sampled with the gated timer clock T1CLK. Two samples are necessary to decide whether the input has a rising or falling edge. Thus, the low and the high pulse of this signal shall be longer than 1/T1CLK in order to be properly processed.

When selected, the capture mechanism is only active, if the timer is running. The first sample after start is discarded and the capture logic is initialized instead, i.e. no capture event will be generated, even if the first sample after start is different to the last sample of the previous run.

2.12.1 Operating modes

2.12.1.1 Mode 0

In Mode 0 Timer 1 is a synchronous 16 bit timer / counter with 12 bit prescaler, providing a 16 bit compare and a 16 bit capture register. The timer is operating continuously in auto reload mode, thus allowing generating a divided clock output at an I/O port. On a timer event, a control line or an I/O pin can be set, cleared or toggled (see Figure 44).

The timer register T1REG is implemented as incrementing counter and its content is continuously compared to the buffered compare value T1CMPSync. If both registers match an interrupt request is generated and the peripheral functions are triggered.

T1REG is cleared automatically, if selected. The compare register T1CMP has an internal synchronization stage, ensuring safe operation even if the value of T1CMP is changed when the timer is running.

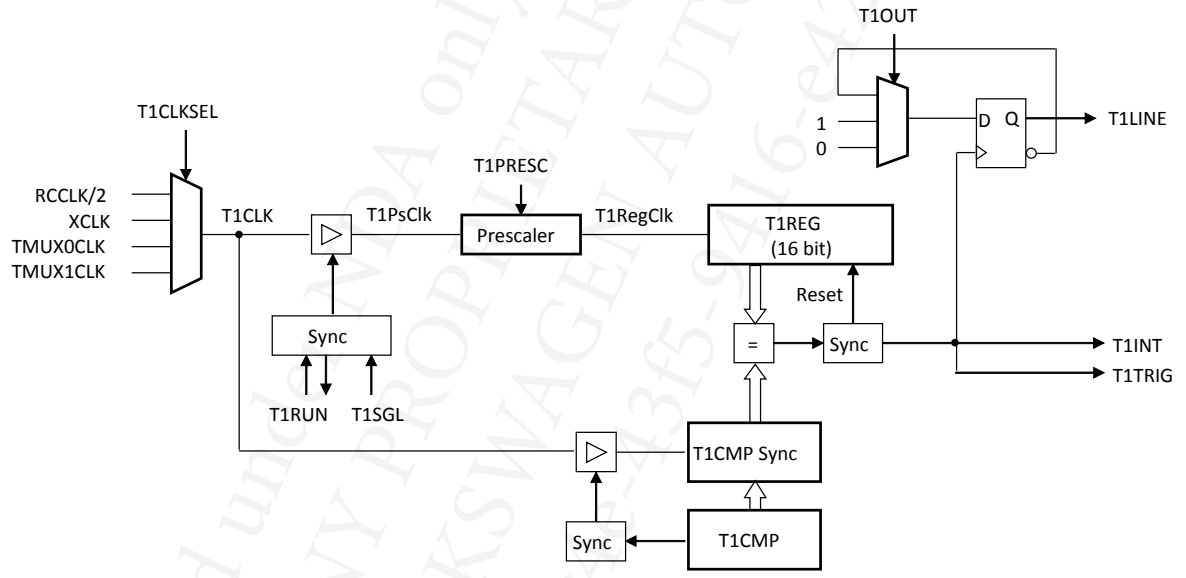


Figure 44. Block diagram of Timer 1 configured in Mode 0 and 1

The timer register is clocked with the output of the prescaler. The clock for the timer register is:

$$T1RegClk = 2^{T1PRESC} \cdot T1CLK \qquad \text{for } T1PRESC < 13 \tag{12}$$

The timer interval depends on the settings of T1RSTCAP and T1RSTCMP. For interval generation the setting T1RSTCAP = 0 and T1RSTCMP = 1 is recommended. In this case the interval yields:

$$T1INTERVAL = (T1CMP + 1) \cdot T1RegClk \quad \text{for } T1PRESC \neq 0$$
$$T1INTERVAL = 2 \cdot T1CLK \quad \text{for } T1PRESC = 0 \text{ and } T1CMP = 0 \tag{13}$$

A capture interrupt is triggered, if T1CAP is loaded due to an external event.

2.12.1.2 Mode 1

Mode 1 has the same properties as Mode 0 with the exception that the timer automatically stops when the first compare match occurs. If bit T1RSTCMP is set, the timer register is cleared when the timer stops.

2.12.1.3 Mode 2

In Mode 2, Timer 1 is operating as 8 bit timer / counter with 12 bit prescaler, providing two 8 bit compare and two 8 bit capture registers.

Mode 2 is intended to generate flexible bit sequences and PWM signals. Both 8 bit timer registers T1REGL and T1REGH run in parallel. It is recommended to clear the timer register prior to start to ensure that both timer registers contain the same value (see Figure 45).

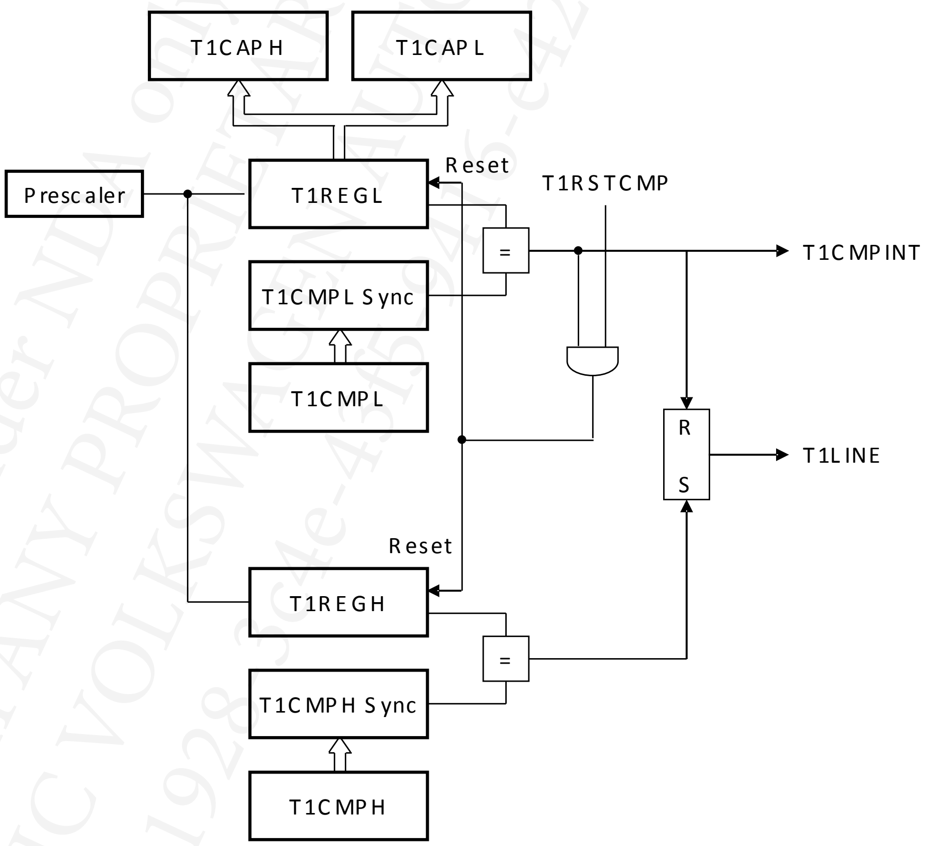


Figure 45. Block diagram of Timer 1 configured in Mode 2

With the two compare registers T1CMPL and T1CMPH it is possible to select two different values. When register T1REGH matches T1CMPH the output line T1LINE is set, whereas it is cleared upon a match between T1REGL and T1CMPL. If bit T1RSTCMP is set, it is possible to generate a PWM signal with variable pulse length and duty cycle.

A match between T1REGL and T1CMPL generates a compare interrupt request.

If both registers T1CMPL and T1CMPH match at the same time T1CMPL has priority. The reset signal upon compare is derived from T1REGL for both timer registers.

The capture interrupt is generated, if T1CAPL is loaded.

It is possible to generate a pulse position like bit sequence by use of the output signal of an additional timer as capture source. If the reset upon capture feature is used this defines the period. With T1CMPL and T1CMPH it is possible to place a single pulse within this interval.

2.12.1.4 Mode 3

As in Mode 2, in Mode 3 Timer 1 is operating as 8 bit timer / counter with 12 bit prescaler, providing two 8 bit compare and two 8 bit capture registers.

The capture event processing with programmable guard time is useful for signal de-spiking and debouncing as well as for convenient signal demodulation.

The timer is running in 8 bit mode with T1REGL as main timer register. Both capture registers T1CAPL and T1CAPH are connected to T1REGL. A match between T1REGL and T1CMPL generates a compare interrupt request. A capture interrupt is generated, if T1CAPL is loaded. With the help of the two capture registers continuous pulse interval, pulse width and duty cycle measurements can be realized, allowing the implementation of an efficient pulse width demodulator with time-out notification (see Figure 46).

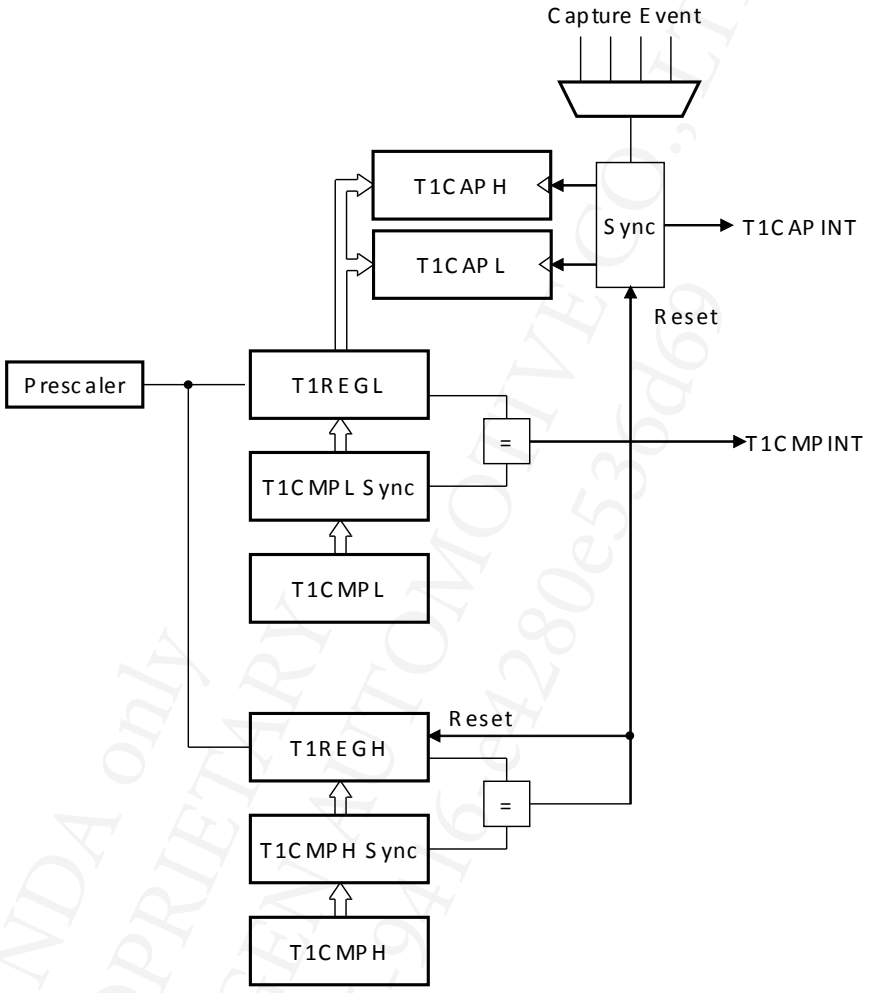


Figure 46. Block diagram of Timer 1 configured in Mode 3

It is possible to specify a guard time after every capture event or signal transition. This is useful if the timer is used to demodulate noisy signals. Only the first transition triggers the capture logic. Any other signal transition is ignored until the guard time elapses.

Register T1REGH is used together with T1CMPH to set the guard time. The timer register shall be cleared manually before start of the timer. If the timer is started and a capture event is detected, T1REGH starts counting. It is stopped and cleared if a match between T1REGH and T1CMPH occurs. The capture logic is blocked as long as T1REGH is running. The guard time is triggered on every selected signal transition no matter whether this generates an interrupt/capture event or not.

The signal level of the selected capture event is evaluated directly after release of the capture logic. If both the rising and the falling edge are selected as capture events it can happen that a new capture event is generated immediately. This would for example be the case if a rising edge was detected first and then the signal becomes statically low again when the guard time has not yet elapsed. In this case a falling edge is detected directly after release of the capture logic.

2.12.2 Registers

2.12.2.1 Timer 1 register T1REG

Timer 1 supports read access to the timer register. The content of the timer register is not buffered or synchronized. Therefore, reading of T1REG is only recommended when the timer is stopped (T1RUN = 0). When the timer is running reading of T1REG can generate unstable and wrong values as the timer value is not necessarily settled when reading takes place. It is recommended to use the manual capture function when the timer is running.

Write access to timer register T1REG is not supported.

Table 117. Timer 1 register T1REG (reset value 00 00h)

Bit	Symbol	Access	Value	Description
15 to 8	T1REGH [7:0]	R/-		Timer 1 Register High Byte (MSByte)
7 to 0	T1REGL [7:0]	R/-		Timer 1 Register Low Byte (LSByte)

2.12.2.2 Timer 1 control register T1CON0

Timer 1 control register 0 holds the control bits to adjust the timer mode and output line. Further, bits to configure the reset and run conditions are provided.

Table 118. Timer 1 control register 0 T1CON0 (reset value 00h)

Bit	Symbol	Access	Value	Description
7 to 6	T1OUT [1:0]	R/W		Timer 1 output line configuration (T1LINE)
			00	No change T1LINE after Timer 1 reset: 0
			01	Mode 0,1,3: Set to ‘0’ Mode 2: Set to ‘1’, if T1REGH = T1CMPH Set to ‘0’, if T1REGL = T1CMPL T1LINE after Timer 1 reset: 0
			10	Mode 0,1,3: Toggles Mode 2: Toggles, if T1REGH = T1CMPH or T1REGL = T1CMPL T1LINE after Timer 1 reset: 0
			11	Mode 0,1,3: Set to ‘1’ Mode 2: Set to ‘0’, if T1REGH = T1CMPH Set to ‘1’, if T1REGL = T1CMPL T1LINE after Timer 1 reset: 1
5	T1RSTCAP	R/W		Timer 1 reset at capture event
			0	No reset
			1	Reset T1REGL, T1REGH and prescaler
4	T1RSTCMP	R/W		Timer 1 reset after compare match
			0	No reset
			1	Mode 0,1: Reset T1REG after T1REG = T1CMP Mode 2,3: Reset T1REGL and T1REGH after T1REGL = T1CMPL

Bit	Symbol	Access	Value	Description
3 to 2	T1MODE[1:0]	R/W		Timer 1 mode selection
			00	Mode 0
			01	Mode 1
			10	Mode 2
			11	Mode 3
1	T1RST [1]	R0/W		Timer 1 reset
			0	No reset
			1	Timer 1 reset
0	T1RUN [1]	R/W		Timer 1 run bit
			0	Timer 1 is stopped
			1	Timer 1 is started/running. While reading, a 1 can also indicate the synchronization phase for start or stop

[1] If T1RST and T1RUN are set simultaneously, T1RST has priority and the timer does not start.

T1OUT[1:0], Timer 1 output line configuration

Timer 1 has an output line flip-flop driving the signal T1LINE. The behavior of this signal depends on the selected timer operating mode and can be configured with the output line configuration bits T1OUT.

The content of the output flip-flop is updated with every compare match. In Mode 0 and 1, T1LINE is updated, if T1REG = T1CMP. In Mode 3, T1LINE is updated, if T1REGL = T1CMPL.

The initial value of the output line flip-flop after a Timer 1 reset is also controlled via T1OUT.

T1RSTCAP, Timer 1 reset upon capture bit

It is possible to reset the timer register in parallel to a capture event. The timer register is reset to zero at the same time when the content is transferred into the capture register. The prescaler is reset to its start value simultaneously. All these events are accomplished with the prescaler clock T1PsClk instead of the timer register clock T1RegClk. Due to the additional reset of the prescaler it is ensured that the result of consecutive interval measurements always yield values independent of the previous interval.

T1RSTCMP, Timer 1 reset after compare match bit

It is possible to reset the timer register after a compare match with the next rising edge of the timer register clock T1RegClk. The prescaler is not influenced.

Example: T1CMP = 4, T1RSTCMP = 1, the timer counts 0, 1, 2, 3, 4, 0, 1, 2, 3, 4, 0, 1, …

T1MODE[1:0], Timer 1 mode selection

Whenever the timer mode is changed the application shall perform a reset of Timer 1 via bit T1RST. It is allowed to set T1RST with the same command that modifies T1MODE.

T1RST, Timer 1 reset bit

The reset bit T1RST can be used to generate an asynchronous reset of Timer 1 comprising the prescaler, the timer register, the synchronization logic, the capture logic and the output line flip-flop. The current content of register T1CMP is loaded into the synchronization register T1CMPSync. A '1' shall be written to T1RST to execute the reset. Writing a '0' has no effect and reading of bit T1RST always yields '0'.

Launching a reset when the timer is running causes the timer to stop immediately and the bit T1RUN is cleared. If T1RST and T1RUN are set simultaneously the reset bit has priority and the timer does not start.

T1RUN, Timer 1 run bit

Timer 1 can be started and stopped with the control bit T1RUN. Reading of T1RUN gives the current status of Timer 1. If a '1' is written to T1RUN the timer is enabled and it starts counting with the rising edge of T1CLK. Writing a '0' to T1RUN forces the timer to stop operation. Every change of signal T1RUN is synchronized to T1CLK before it becomes effective. Reading of T1RUN yields '1' if the timer is running and during the synchronization phase to start and stop the timer.

2.12.2.3 Timer 1 control register T1CON1

The Timer 1 control register 1 stores the selection of the prescaler value T1PRESC[3:0] and the used clock source T1CLKSEL[1:0].

The control bits in register T1CON1 are not buffered nor synchronized to the timer clock T1CLK. The content of register T1CON shall only be modified, if the timer is stopped (T1RUN = 0). Any alteration of T1CON1 when the timer is running can cause unpredictable behavior.

Table 119. Timer 1 control register 1 T1CON1 (reset value 00h)

Bit	Symbol	Access	Value	Description
7 to 6	RFU	-/W0		Reserved for future use
5 to 4	T1CLKSEL[1:0]	R/W		Timer 1 clock source selection
			00	RCCLK/2 (8 MHz nominal)
			01	External clock, XCLK
			10	Output of timer source multiplexer 0, TMUX0CLK
			11	Output of timer source multiplexer 1, TMUX1CLK
3 to 0	T1PRESC[3:0]	R/W		Timer 1 prescaler selection
			0000	T1RegClk = 1 * T1CLK
			0001	T1RegClk = 2 * T1CLK
			0010	T1RegClk = 4 * T1CLK
			0011	T1RegClk = 8 * T1CLK
			0100	T1RegClk = 16 * T1CLK
			0101	T1RegClk = 32 * T1CLK
			0110	T1RegClk = 64 * T1CLK
			0111	T1RegClk = 128 * T1CLK
			1000	T1RegClk = 256 * T1CLK

Bit	Symbol	Access	Value	Description
			1001	T1RegClk = 512 * T1CLK
			1010	T1RegClk = 1024 * T1CLK
			1011	T1RegClk = 2048 * T1CLK
			1100	T1RegClk = 4096 * T1CLK
			1101 - 1111	RFU

T1CLKSEL[1:0], Timer 1 clock source selection

The Timer 1 clock source selection selects the clock source.

T1PRESC[3:0], Timer 1 prescaler selection

The Timer 1 prescaler selection selects the clock speed for the timer register according to Equation 12.

2.12.2.4 Timer 1 control register T1CON2

Timer 1 control register 2 holds the control bits to adjust the capture functionality.

Table 120. Timer 1 control register 2 T1CON2 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	T1MANCAP	R/W		Timer 1 manual capture bit
			0	No manual capture event
			1	Mode 0,1: Content of T1REG is transferred into T1CAP (16 bit) Mode 2,3: Content of T1REGL is transferred into T1CAPL (8 bit)
6 to 4	T1CAPMODE[2:0]	R/W		Timer 1 capture mode selection
			000	No event
			001	Mode 0,1 (event for T1CAP): Rising edge Mode 2,3 (event for T1CAPH): None Mode 2,3 (event for T1CAPL): Rising edge Mode 3 (event to trigger guard time): Rising edge
			010	Mode 0,1 (event for T1CAP): Falling edge Mode 2,3 (event for T1CAPH): None Mode 2,3 (event for T1CAPL): Falling edge Mode 3 (event to trigger guard time): Falling edge
			011	Mode 0,1 (event for T1CAP): Both edges Mode 2,3 (event for T1CAPH): None Mode 2,3 (event for T1CAPL): Both edges Mode 3 (event to trigger guard time): Both edges
			100	Mode 0,1 (event for T1CAP): Falling edge Mode 2,3 (event for T1CAPH): Rising edge Mode 2,3 (event for T1CAPL): Falling edge Mode 3 (event to trigger guard time): Both edges

Bit	Symbol	Access	Value	Description
			101	Mode 0,1 (event for T1CAP): Rising edge Mode 2,3 (event for T1CAPH): None Mode 2,3 (event for T1CAPL): Rising edge Mode 3 (event to trigger guard time): Both edges
			110	Mode 0,1 (event for T1CAP): Falling edge Mode 2,3 (event for T1CAPH): None Mode 2,3 (event for T1CAPL): Falling edge Mode 3 (event to trigger guard time): Both edges
			111	Mode 0,1 (event for T1CAP): Rising edge Mode 2,3 (event for T1CAPH): Falling edge Mode 2,3 (event for T1CAPL): Rising edge Mode 3 (event to trigger guard time): Both edges
3 to 0	T1CAPSRC[3:0]	R/W		Timer 1 capture signal source selection
			0000	Input of port P17
			0001	Input of port P21
			0010	Output signal line of Timer 0
			0011	Output signal line of Timer 2
			0100	Output signal of LF IMMO demodulator
			0101	Reserved for future use
			0110	Reserved for future use
			0111	Input of port P13
			1000	Output signal of timer source multiplexer 0 (TMUX0CLK)
			1001 to 1101	Reserved for future use
			1110	Constant ‘0’
			1111	Constant ‘1’

T1MANCAP, Timer 1 manual capture bit

A capture operation can be requested manually when the timer is running. Thereby it is possible to read a consistent counter value even if the timer is running.

Once the bit T1MANCAP is set by the application, it will stay '1' until the capture request has been executed, causing the control bit to be cleared. Thus, T1MANCAP can be polled by the application to verify, if the capture request has been carried out.

A manual capture event never generates an interrupt request or triggers a reset upon capture or starts the guard time. The manual capture works independently of the selected setting of the capture mode T1CAPMODE. It even works, if T1CAPMODE = 000.

The manual capture event is accomplished with the prescaler clock T1PsClk to minimize the latency.

The manual capture functionality is not supported, if the timer is stopped. If T1MANCAP is set when the timer is stopped, the manual capture event will be accomplished as soon as the timer is started again. If the timer is stopped, the application can instead read the timer register directly.

The bit T1MANCAP cannot be cleared by the application except by executing a timer reset with bit T1RST.

Dependent on the selected timer operating mode the manual capture function transfers different portions of data into different registers.

T1CAPMODE[2:0], Timer 1 capture mode selection

With the timer 1 capture mode selection it is possible to select which event of the capture source signal is used to generate a capture event and to load the respective capture register. In timer operating mode 2 and 3 it is possible to select different actions for the two capture registers T1CAPH and T1CAPL. In timer mode 3 it is also possible to select the behavior of the guard time logic.

If all three bits of T1CAPMODE are zero, the capture function is disabled completely in all timer operating modes.

In timer mode 3 the difference between setting 001 and 101 (and 010 and 110) is the behavior of the guard time. If the settings 101 or 110 are selected, the guard time is activated even if an inactive edge is detected. This avoids false triggers in case there are multiple signal transitions in the vicinity of the unselected event. The settings 001 and 010 are intended for signals with very different behavior of the rising and falling edges. For these signals it can be more appropriate to define a longer guard time after the significant edge that covers also the unselected edge. Thereby it is possible to generate a shorter guard time after the unselected edge if the pulse width is known.

In timer mode 2 and 3 the selection of either value 100 or 111 for T1CAPMODE can be used to distinguish the event that causes the generation of the capture interrupt (only a capture event of T1CAPL generates an interrupt).

T1CAPSRC[3:0], Timer 1 capture signal source selection

With this setting it is possible to select the source signal for the capture event.

The settings 1110b and 1111b are intended for debugging and test purposes. Therewith it is possible to trigger a capture event on either edge by software.

2.12.2.5 Timer 1 compare register T1CMP

The compare register T1CMP is used to set the time-out interval of Timer 1. The compare register has an internal synchronization stage (T1CMPSync) to allow safe operation even when the timer is running. The behavior of any write access to register T1CMP depends on the current state of the timer. If the timer is stopped (T1RUN = 0) any write access to T1CMP updates also the synchronization stage T1CMPSync. The prescaler and the timer register T1REG are not influenced. If the timer is running (T1RUN = 1), a write access to T1CMP triggers the synchronization logic first. The new value of T1CMP is transferred with one of the next rising edges of T1CLK into the synchronization register T1CMPSync. The value of T1CMP shall stay constant for this time period to allow a correct data transfer. Any write access to either T1CMPL or T1CMPH causes a resynchronization of the complete register T1CMP. Therefore, if both values T1CMPL and T1CMPH are intended to be changed a word access to register T1CMP shall be used rather than two consecutive byte accesses to T1CMPL and T1CMPH. Any read access to T1CMP yields the content of the register itself and not the content of the synchronization register T1CMPSync.

Table 121. Timer 1 compare register T1CMP (reset value XX_XXh)

Bit	Symbol	Access	Value	Description
15 to 8	T1CMPH [7:0]	R/W		Timer 1 Compare Register High Byte (MSByte)
7 to 0	T1CMPL [7:0]	R/W		Timer 1 Compare Register Low Byte (LSByte)

2.12.2.6 Timer 1 capture register T1CAP

The Timer 1 Capture Register is loaded automatically with the content of the timer register. Reading shall only be performed if the content is stable. Write access to T1CAP is not supported.

Table 122. Timer 1 capture register T1CAP (reset value XX_XXh)

Bit	Symbol	Access	Value	Description
15 to 8	T1CAPH [7:0]	R/-		Timer 1 Capture Register High Byte (MSByte)
7 to 0	T1CAPL [7:0]	R/-		Timer 1 Capture Register Low Byte (LSByte)

2.12.3 Interaction with I/O port interface

If an I/O pin is selected as capture input the application shall ensure that the corresponding I/O pin is configured as input.

2.13 Watchdog timer

The device incorporates a watchdog timer to recover the system from application program deadlocks. This avoids that the connected battery is unnecessarily discharged.

The watchdog timer is active when the device is supplied from the battery (BATTERY state), while it is disabled when the device is supplied from the LF field (LF FIELD state). The watchdog timer stops automatically in debug mode.

If the watchdog timer is active and not periodically restarted, a time-out event forces the device from the BATTERY state into the LF FIELD state and generates a device reset. If the watchdog time-out event is configured as wake-up source, the device switches back to the BATTERY state, executes the boot routine and continues with the program execution. Please refer to Section 2.2.2.2 to determine the device behavior in case an LF wake-up event is pending after the watchdog time-out reset.

If the watchdog time-out event is not configured as wake-up source, the system behavior after the watchdog time-out reset depends on the field supply condition and the voltage at pin VDDC. The device may continue program execution, starting with the boot routine, as long as the field supply is sufficient.

A battery buffered flag indicates a previous watchdog time-out event and, as a potential device wake-up source, is evaluated by the boot routine.

The clock for the watchdog timer is derived from the auxiliary RC oscillator and runs at a frequency of $1/T_{REF,LF}$. The watchdog timer consists of a 16 bit incrementing main timer with 11 bit prescaler. The timeout is selectable in 16 steps from approximately 16 ms to 537 s. The selected time-out value can be locked.

In single shot mode, the clearing of the watchdog is prevented, thus the application shall finish prior to the selected fixed watchdog time-out. This mode is intended for applications which do not handle the watchdog at all.

2.13.1 Registers

2.13.1.1 Watchdog timer control register WDCON

The watchdog timer is controlled via the watchdog timer control register WDCON.

Table 123. Watchdog timer control register WDCON (reset value 50h)

Bit	Symbol	Access	Value	Description
7 to 4	WDTIM[3:0]	R/W [1]		Watchdog time-out selection
			0000	2^{11} $T_{REF,LF}$ ≈ 16 ms
			0001	2^{12} $T_{REF,LF}$ ≈ 33 ms
			0010	2^{13} $T_{REF,LF}$ ≈ 66 ms
			0011	2^{14} $T_{REF,LF}$ ≈ 131 ms
			0100	2^{15} $T_{REF,LF}$ ≈ 262 ms
			0101	2^{16} $T_{REF,LF}$ ≈ 524 ms
			0110	2^{17} $T_{REF,LF}$ ≈ 1.05 s
			0111	2^{18} $T_{REF,LF}$ ≈ 2.10 s
			1000	2^{19} $T_{REF,LF}$ ≈ 4.19 s
			1001	2^{20} $T_{REF,LF}$ ≈ 8.39 s
			1010	2^{21} $T_{REF,LF}$ ≈ 16.8 s
			1011	2^{22} $T_{REF,LF}$ ≈ 33.6 s
			1100	2^{23} $T_{REF,LF}$ ≈ 67.1 s
			1101	2^{24} $T_{REF,LF}$ ≈ 134 s
			1110	2^{25} $T_{REF,LF}$ ≈ 268 s
			1111	2^{26} $T_{REF,LF}$ ≈ 537 s
3 to 2	WDMODE[1:0]	R/W [1]		Watchdog mode selection
			00	Standard operation, all control bits in register WDCON can be written. Use this mode if the application requires changing the watchdog time-out value.
			01	Fixed time-out selection: The bits WDTIM and WDMODE0 cannot be changed. Use this mode to select a fixed time-out.
			10 or 11	Single shot mode: The bits WDTIM, WDMODE and WDCLR cannot be changed. Use this mode to select a fixed time-out for an application, which does not handle the watchdog at all. The application shall finish prior to the selected watchdog time-out. It is not possible to clear the watchdog.
1	WDTRIG	R0/W		Trigger watchdog time-out
			0	No effect
			1	Trigger watchdog time-out
0	WDCLR	R0/W[1]		Watchdog clear
			0	No effect
			1	Clears watchdog prescaler and main timer

[1] Note: Write access to all control bits except bit 1 depends on the setting of WDMODE

WDTIM[3:0], watchdog time-out selection

The register bits WDTIM select a tap from the watchdog main timer. If the selected tap holds a '1', a watchdog time-out is generated. All other bits of the main timer as well as the prescaler are not considered. After the watchdog has been cleared, the watchdog time-out can be calculated according to Equation 14.

$$WDTIMEOUT = 2^{(11+WDTIM)} \cdot T_{REF,LF} \quad (14)$$

If WDMODE = 00b, WDTIM can be changed at any time without influencing the current state of the watchdog timer. When changing the timeout window, it is recommended to clear the watchdog counter simultaneously.

If WDTIM is changed to a lower value and the watchdog is not cleared simultaneously it depends on the state of the selected tap of the main timer whether a time-out is generated immediately or not. It can happen that no time-out is generated even though the current value of the main timer is greater than WDTIMEOUT.

After a device reset WDTIM is set to 0101b, hence, the watchdog time-out value is set to 2^{16} $T_{REF,LF}$ (approximately 524 ms).

WDMODE[1:0], watchdog mode selection

The watchdog timer supports three different application modes.

Please note that the bits WDMODE have the character of one-time programmable bits. It is not possible to clear one of the WDMODE bits by the application program once they are set. It is possible to set WDMODE from 01b to 11b in order to enter the single shot mode once a fixed time-out has already been selected. Changing WDMODE = 10b to WDMODE = 11b does not change anything as both settings are equivalent.

If the bits WDMODE[1] and WDCLR are set simultaneously the request to clear the watchdog is already ignored and no reset is accomplished.

WDTRIG, trigger watchdog time-out

If a '1' is written to this bit it can be used to trigger a watchdog time-out intentionally. The effect is the same as if a real watchdog time-out has occurred. This functionality can be used to check the behavior of the application program after a watchdog time-out. Writing a '0' to WDTRIG has no effect. Reading of WDTRIG always yields '0'.

WDCLR, watchdog clear

To prevent the watchdog timer from generating a time-out, a '1' has to be written periodically to the control bit WDCLR by the application program. This clears the watchdog prescaler and main timer. Writing a '0' to WDCLR has no effect. Reading of WDCLR always yields '0'.

WDTOF, watchdog time-out flag (in PRESWUP0)

A watchdog time-out event sets the watchdog time-out flag WDTOF in special function register PRESWUP0. This flag is located in the battery supplied domain and keeps its state even in POWER-OFF device state. Bit WDTOF can only be cleared by the user by writing a '1', writing a '0' has no effect.

WDTOFWUPEN, wake-up by the watchdog time-out flag, enable (in PRESWUP0)

A watchdog time-out event, more precisely the WDTOF flag, can be enabled as a device wake-up source by setting the WDTOFWUPEN bit to 1 in the special function register PRESWUP0. This control bit is located in the battery supplied domain and maintains its state until set to 0 by the user software, or at reset condition at battery insertion (BATPOR). The state of the WDTOFWUPEN bit is maintained in POWER-OFF as long as a valid battery is connected.

2.14 I/O ports

2.14.1 I/O port functions

The device incorporates three I/O ports—P1, P2, and P3—with up to 8 independently configurable bidirectional port pins per port. All I/O port pins can be controlled individually.

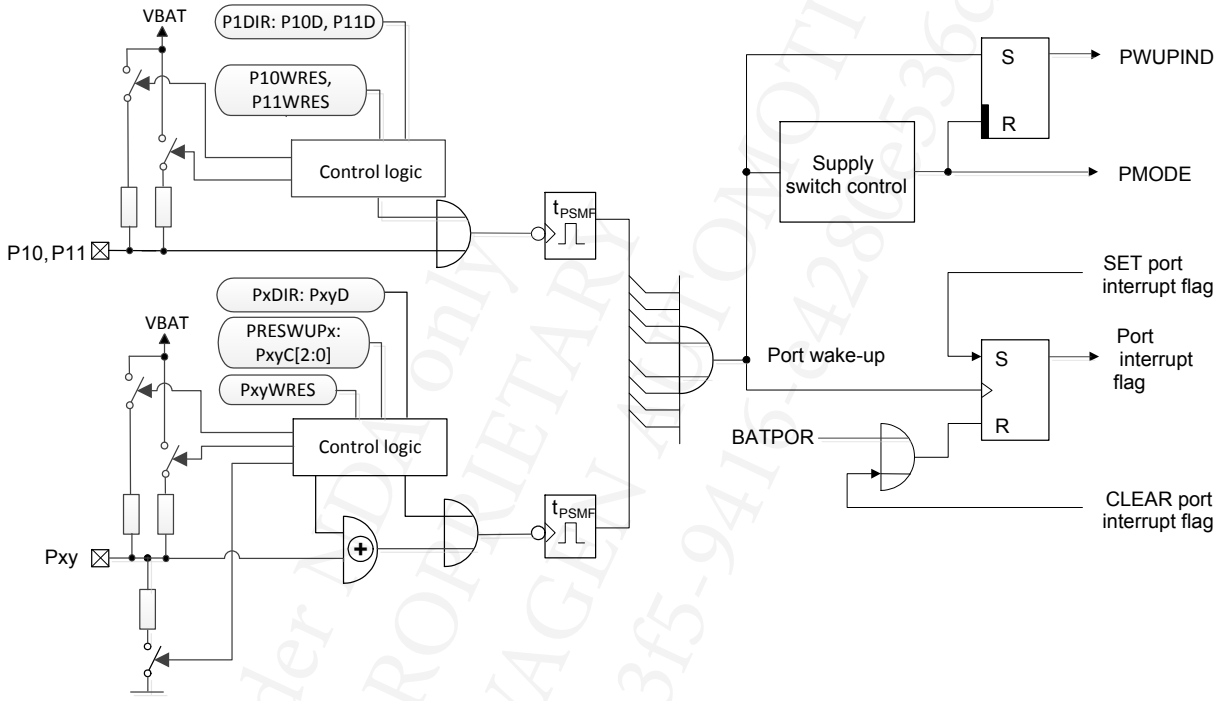
Features:

- User configurable push-pull output or digital input in BATTERY state
- Digital input in POWER OFF state
- All port pins have port wake-up and port interrupt capabilities
- Two fail-safe port wake-up pins P10 and P11
  - Permanent pull-up resistor in input mode
  - Pull-up resistor disabled in output mode
  - Two different pull-up strengths: strong (R_{PU_STR}) and weak (R_{PU_WK})
  - Port wake-up and port interrupt on high to low transition
- Standard port pins (all pins except P10, P11)
  - User configurable pull-up or pull-down resistor in input mode; resistors can be fully disabled
  - Pull-up/pull-down resistor disabled in output mode
  - Two different pull-up strengths: strong (R_{PU_STR}) and weak (R_{PU_WK})
  - User configurable port wake-up and port interrupt on high to low or low to high transition or port wake-up and port interrupt can be disabled
- VBAT buffered pull-up/pull-down resistor settings and port wake-up configuration—port configuration is maintained in POWER OFF state
- Selected port pins are shared with digital and/or analogue alternative port function (see Section 2.14.3.7)
- Very weak pull-up resistors (R_{PU_MD1}, R_{PU_MD2}, R_{PU_MD3}) at pin P21_MD for use with an external motion sensor

2.14.2 Port wake up

The port wake up logic can wake up the device from POWER OFF state or triggers a corresponding interrupt request during program execution. The wake-up feature is supported by all I/O pins. A port wake up from POWER OFF state transits the device to the BATTERY state. If the device is field supplied (LF FIELD state), the port wake-up information is stored and can be used for branch decision in the boot routine. For all wake-up ports, the wake-up mono-flop is triggered for the specified time t_{PSMF} in input mode and disabled if the port operates in output mode. Due to spurious events, the port wake-up mono-flop can be triggered if the direction of a port pin changes.

Example: A device is operating in BATTERY state. A wake-up port is used as output and set to high level. The port is configured to use the internal pull-down and to wake-up on a falling edge. Setting the device to POWER OFF state, the port is set to input and due to the configured internal pull-down set to low level. Consequently, a falling edge is detected which could result in a wake-up event. Similarly, a spurious port wake-up will be triggered if PxINTDIS.PxxINTDIS is set at the time a VDDRST occurs and a port is configured on falling/rising edge while the port state is kept low/high, respectively. To avoid this behavior and ignore possible wake-up event, the power-off routine should first disable port interrupt, clear the port direction (set it as "input"), clear eventual alternative port functions, enable single port interrupts and then wait for t_{PSMF} (plus the time the external circuitry needs to establish static conditions at the port lines) before the effective power-off instruction.



1. Pxy represents all available I/O pins except P10 and P11

Figure 47. Port wake up logic

For P10 and P11, the port wake-up is sensitive at high to low transitions of the port pin. These ports feature permanent pull-up resistors in input mode. The pull-up resistor can be configured between strong and weak for every port pin separately. The wake-up mono-flop is enabled, if the port pin is in input mode. Due to this, P10 and P11 support a fail-safe wake-up from POWER OFF state regardless of the setting of any battery supplied control register. It is strongly recommended that every application uses at least one of these two ports for wake-up generation in order to avoid deadlock situations if the battery supplied registers are not correctly configured.

All other port pins except P10 and P11 feature a selectable pull-up (weak or strong) or pull-down resistor and a user selectable wake-up either on high to low or low to high transition of the port. The wake-up on low to high transition of the port can be used by the application to detect the release of a button. Either the internal pull-up resistor or

an external pull-up device shall be used for correct operation. If a port pin is needed as general purpose pin and not as button input it is possible to disable the wake-up function.

2.14.3 Registers

The port wake-up indicator flag PWUPIND (from Figure 47) is hosted in the power control register PCON1 (see Table 7).

2.14.3.1 Port direction control registers, PxDIR

The I/O port lines can be configured as input or output as defined in the P1DIR register. If the corresponding direction bit is set the port line is configured for output and the corresponding port I/O driver forces the port line high or low, depending on the state of the corresponding data output source selected. If the corresponding direction bit is cleared, the I/O port driver is configured for input and the corresponding push-pull stage is forced into tri-state.

It is important to notice that the port direction control bit can be overruled by the alternative port functions (see also Section 2.14.3.7).

Table 124. Port 1 direction control register P1DIR (reset value 00h)

Bit	Symbol	Access	Value	Description
7	P17D	R/W		Port 1.7 direction
			0	Input
			1	Output
6	P16D	R/W		Port 1.6 direction
			0	Input
			1	Output
5	P15D	R/W		Port 1.5 direction
			0	Input
			1	Output
4	P14D	R/W		Port 1.4 direction
			0	Input
			1	Output
3	P13D	R/W		Port 1.3 direction
			0	Input
			1	Output
2	P12D	R/W		Port 1.2 direction
			0	Input
			1	Output
1	P11D	R/W		Port 1.1 direction
			0	Input
			1	Output
0	P10D	R/W		Port 1.0 direction
			0	Input

Bit	Symbol	Access	Value	Description
			1	Output

Table 125. Port 2 direction control register P2DIR (reset value 0000_0000b)

Bit	Symbol	Access	Value	Description
7	P27D	R/W		Port 2.7 direction
			0	Input
			1	Output
6	P26D	R/W		Port 2.6 direction
			0	Input
			1	Output
5	P25D	R/W		Port 2.5 direction
			0	Input
			1	Output
4	P24D	R/W		Port 2.4 direction
			0	Input
			1	Output
3	P23D	R/W		Port 2.3 direction
			0	Input
			1	Output
2	P22D	R/W		Port 2.2 direction
			0	Input
			1	Output
1	P21D	R/W		Port 2.1 direction
			0	Input
			1	Output
0	P20D	R/W		Port 2.0 direction
			0	Input
			1	Output

Table 126. Port 3 direction control register P3DIR (reset value xx00_0000b)

Bit	Symbol	Access	Value	Description
7 to 6	RFU	-/W0		Reserved for future use
5 to 4	RFU	-/W0		Reserved for future use
3	P33D	R/W		Port 3.3 direction
			0	Input
			1	Output

Bit	Symbol	Access	Value	Description
2	P32D	R/W		Port 3.2 direction
			0	Input
			1	Output
1	RFU	-/W0		Reserved for future use
0	P30D	R/W		Port 3.0 direction
			0	Input
			1	Output

2.14.3.2 Port x Interrupt Disable register PxINTDIS

PxINTDIS disables the corresponding Port x interrupt if the corresponding bit is set. Compared to PRESWUPx the PxINTDIS register allows deactivating also interrupts on the fail safe wake-up ports P10 and P11 and it allows disabling port interrupts when running from field supply.

Table 127. Port 1 Interrupt Disable register P1INTDIS (reset value 00h)

Bit	Symbol	Access	Value	Description
7	P17INTDIS	R/W		Port 1.7 interrupt disable
			0	enabled
			1	disabled
6	P16INTDIS	R/W		Port 1.6 interrupt disable
			0	enabled
			1	disabled
5	P15INTDIS	R/W		Port 1.5 interrupt disable
			0	enabled
			1	disabled
4	P14INTDIS	R/W		Port 1.4 interrupt disable
			0	enabled
			1	disabled
3	P13INTDIS	R/W		Port 1.3 interrupt disable
			0	enabled
			1	disabled
2	P12INTDIS	R/W		Port 1.2 interrupt disable
			0	enabled
			1	disabled
1	P11INTDIS	R/W		Port 1.2 interrupt disable
			0	enabled
			1	disabled
0	P10INTDIS	R/W		Port 1.0 interrupt disable
			0	enabled

Bit	Symbol	Access	Value	Description
			1	disabled

Table 128. Port 2 Interrupt Disable register P2INTDIS (reset value 0000_0000b)

Bit	Symbol	Access	Value	Description
7	P27INTDIS	R/W		Port 2.7 interrupt disable
			0	enabled
			1	disabled
6	P26INTDIS	R/W		Port 2.6 interrupt disable
			0	enabled
			1	disabled
5	P25INTDIS	R/W		Port 2.5 interrupt disable
			0	enabled
			1	disabled
4	P24INTDIS	R/W		Port 2.4 interrupt disable
			0	enabled
			1	disabled
3	P23INTDIS	R/W		Port 2.3 interrupt disable
			0	enabled
			1	disabled
2	P22INTDIS	R/W		Port 2.2 interrupt disable
			0	enabled
			1	disabled
1	P21INTDIS	R/W		Port 2.1 interrupt disable
			0	enabled
			1	disabled
0	P20INTDIS	R/W		Port 2.0 interrupt disable
			0	enabled
			1	disabled

Table 129. Port 3 Interrupt Disable register P3INTDIS (reset value xx00_0000b)

Bit	Symbol	Access	Value	Description
7 to 6	RFU	-/W0		Reserved for future use
5 to 4	RFU	-/W0		Reserved for future use
3	P33INTDIS	R/W		Port 3.3 interrupt disable
			0	enabled
			1	disabled

Bit	Symbol	Access	Value	Description
2	P32INTDIS	R/W		Port 3.2 interrupt disable
			0	enabled
			1	disabled
1	RFU	-/W0		Reserved for future use
0	P30INTDIS	R/W		Port 3.0 interrupt disable
			0	enabled
			1	disabled

2.14.3.3 Port output control registers PxOUT

The port output register controls the respective port output flip-flop in case the port line is used in output mode. Any read operation from the port output control register will return the state of the flip-flop rather than the state of the port line.

Table 130. Port 1 output control register P1OUT (reset value 00h)

Bit	Symbol	Access	Value	Description
7	P17O	R/W		Port 1.7 output
			0	Low (‘0’)
			1	High (‘1’)
6	P16O	R/W		Port 1.6 output
			0	Low (‘0’)
			1	High (‘1’)
5	P15O	R/W		Port 1.5 output
			0	Low (‘0’)
			1	High (‘1’)
4	P14O	R/W		Port 1.4 output
			0	Low (‘0’)
			1	High (‘1’)
3	P13O	R/W		Port 1.3 output
			0	Low (‘0’)
			1	High (‘1’)
2	P12O	R/W		Port 1.2 output
			0	Low (‘0’)
			1	High (‘1’)
1	P11O	R/W		Port 1.0 output
			0	Low (‘0’)
			1	High (‘1’)
0	P10O	R/W		Port 1.0 output
			0	Low (‘0’)
			1	High (‘1’)

Table 131. Port 2 Interrupt Disable register P2OUT (reset value 0000_0000b)

Bit	Symbol	Access	Value	Description
7	P27O	R/W		Port 2.7 output
			0	Low (‘0’)
			1	High (‘1’)
6	P26O	R/W		Port 2.6 output
			0	Low (‘0’)
			1	High (‘1’)
5	P25O	R/W		Port 2.5 output
			0	Low (‘0’)
			1	High (‘1’)
4	P24O	R/W		Port 2.4 output
			0	Low (‘0’)
			1	High (‘1’)
3	P23O	R/W		Port 2.3 output
			0	Low (‘0’)
			1	High (‘1’)
2	P22O	R/W		Port 2.2 output
			0	Low (‘0’)
			1	High (‘1’)
1	P21O	R/W		Port 2.1 output
			0	Low (‘0’)
			1	High (‘1’)
0	P20O	R/W		Port 2.0 output
			0	Low (‘0’)
			1	High (‘1’)

Table 132. Port 3 output control register P3OUT (reset value xx00_0000b)

Bit	Symbol	Access	Value	Description
7 to 6	RFU	-/W0		Reserved for future use
5 to 4	RFU	-/W0		Reserved for future use
3	P33O	R/W		Port 3.3 output
			0	Low (‘0’)
			1	High (‘1’)
2	P32O	R/W		Port 3.2 output
			0	Low (‘0’)
			1	High (‘1’)
1	RFU	-/W0		Reserved for future use

Bit	Symbol	Access	Value	Description
0	P30O	R/W		Port 3.0 output
			0	Low (‘0’)
			1	High (‘1’)

2.14.3.4 Port input sense registers PxINS

Reading from the port lines is accomplished by means of the special function registers port input sense PxINS. Reading these registers directly sense the port pins and returns the corresponding states of the I/O lines. The port input sense logic is disabled for port pins if an analogue port function is active. The corresponding port input sense bits return a '0' in this case.

If no battery supply is available, all port input sense bits return a '1'.

Table 133. Port 1 input sense register P1INS (reset value xxxx_xxxxb)

Bit	Symbol	Access	Value	Description
7	P17S	R/-		Port 1.7 input
			0	Low (‘0’)
			1	High (‘1’)
6	P16S	R/-		Port 1.6 input
			0	Low (‘0’)
			1	High (‘1’)
5	P15S	R/-		Port 1.5 input
			0	Low (‘0’)
			1	High (‘1’)
4	P14S	R/-		Port 1.4 input
			0	Low (‘0’)
			1	High (‘1’)
3	P13S	R/-		Port 1.3 input
			0	Low (‘0’)
			1	High (‘1’)
2	P12S	R/-		Port 1.2 input
			0	Low (‘0’)
			1	High (‘1’)
1	P11S	R/-		Port 1.1 input
			0	Low (‘0’)
			1	High (‘1’)
0	P10S	R/-		Port 1.0 input
			0	Low (‘0’)
			1	High (‘1’)

Table 134. Port 2 input sense register P2INS (reset value xxxx_xxxxb)

Bit	Symbol	Access	Value	Description
7	P27S	R/-		Port 2.7 input
			0	Low (‘0’)
			1	High (‘1’)
6	P26S	R/-		Port 2.6 input
			0	Low (‘0’)
			1	High (‘1’)
5	P25S	R/-		Port 2.5 input
			0	Low (‘0’)
			1	High (‘1’)
4	P24S	R/-		Port 2.4 input
			0	Low (‘0’)
			1	High (‘1’)
3	P23S	R/-		Port 2.3 input
			0	Low (‘0’)
			1	High (‘1’)
2	P22S	R/-		Port 2.2 input
			0	Low (‘0’)
			1	High (‘1’)
1	P21S	R/-		Port 2.1 input
			0	Low (‘0’)
			1	High (‘1’)
0	P20S	R/-		Port 2.0 input
			0	Low (‘0’)
			1	High (‘1’)

Table 135. Port 3 input sense register P3INS (reset value xxxx_xxxxb)

Bit	Symbol	Access	Value	Description
7 to 6	RFU	-/-		Reserved for future use
5 to 4	RFU	-/-		Reserved for future use
3	P33S	R/-		Port 3.3 input
			0	Low (‘0’)
			1	High (‘1’)
2	P32S	R/-		Port 3.2 input
			0	Low (‘0’)
			1	High (‘1’)
1	RFU	-/-		Reserved for future use

Bit	Symbol	Access	Value	Description
0	P30S	R/-		Port 3.0 input
			0	Low (‘0’)
			1	High (‘1’)

2.14.3.5 Port pull up strength control register PxWRES

Port pins feature a pull-up strength control register, stored in VBAT domain. Configuration is kept even when VDD disappears and device is in POWER-OFF mode. All port pins can be configured to strong pull-ups (typ. 100 µA when VBAT = 3 V) or weak pull-ups (typ. 10 µA). Reading PxWRES returns the pull up strength (0 = weak, 1 = strong). The pull-up strength is also latched in POWER OFF state but cannot be guaranteed (e.g. in case of battery bouncing or insertion) and should be refreshed from time to time per software. Strong pull-ups are used as default on battery power-on reset (BATPOR). The pull-up resistor is temporarily disabled if the I/O pin is switched to output. Moreover, the resistors are temporarily disabled for all I/O pins if an alternative function of the corresponding port is active.

Table 136. Port pull up strength control register P1WRES (reset value 1111_1111b)

Bit	Symbol	Access	Value	Description
7	P17WRES	R/W		Port 1.7 pull up strength
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})
6	P16WRES	R/W		Port 1.6 pull up strength
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})
5	P15WRES	R/W		Port 1.5 pull up strength
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})
4	P14WRES	R/W		Port 1.4 pull up strength
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})
3	P13WRES	R/W		Port 1.3 pull up strength
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})
2	P12WRES	R/W		Port 1.2 pull up strength
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})
1	P11WRES	R/W		Port 1.1 pull up strength
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})
0	P10WRES	R/W		Port 1.0 pull up strength
			0	weak (R_{PU_WK})

Bit	Symbol	Access	Value	Description
			1	strong (R_{PU_STR})

Table 137. Port pull up strength control register P2WRES (reset value 1111_1111b)

Bit	Symbol	Access	Value	Description
7	P27WRES	R/W		Port 2.7 pull up strength
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})
6	P26WRES	R/W		Port 2.6 pull up strength
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})
5	P25WRES	R/W		Port 2.5 pull up strength
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})
4	P24WRES	R/W		Port 2.4 pull up strength
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})
3	P23WRES	R/W		Port 2.3 pull up strength
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})
2	P22WRES	R/W		Port 2.2 pull up strength
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})
1	P21WRES	R/W		Port 2.1 pull up strength
			0	weak pull-up according to setting of P21MRES (see Table 140)
			1	strong (R_{PU_STR})
0	P20WRES	R/W		Port 2.0 pull up strength
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})

Table 138. Port pull up strength control register P3WRES (reset value xx11_1111b)

Bit	Symbol	Access	Value	Description
7 to 6	RFU	-/W1		Reserved for future use
5 to 4	RFU	-/W1		Reserved for future use
3	P33WRES	R/W		Port 3.3 pull up strength
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})

Bit	Symbol	Access	Value	Description
2	P32WRES	R/W		Port 3.2 pull up strength
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})
1	RFU	-/W1		Reserved for future use
0	P30WRES	R/W		Port 3.0 pull up strength
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})

2.14.3.6 Port resistor/wake up configuration, PRESWUPx

The port resistor and wake-up configuration registers are used to configure the pull-up or pull-down resistor of the respective I/O port and to configure the port pin wake-up function. For every I/O port featuring a selectable pull-up or pull-down resistor and wake-up function three control bits are available.

It is possible to select a pull-up resistor or a pull-down resistor or to deactivate both, but not to turn on the pull-up and the pull-down resistor simultaneously.

The port resistor and wake-up configuration registers allow either byte or word access (Table 139).

Table 139. Word and byte access to port resistor and wake-up configuration registers PRESWUPx

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
PRESWUP0	PRESWUP0H	PRESWUP0L
PRESWUP1	PRESWUP1H	PRESWUP1L
PRESWUP2	PRESWUP2H	PRESWUP2L
PRESWUP3	PRESWUP3H	PRESWUP3L
PRESWUP4	PRESWUP4H	PRESWUP4L

Table 140. Port resistor and wake-up configuration register PRESWUP0 (reset value 8888h)

Bit	Symbol	Access	Value	Description
15 to 13	P15C[2:0]	R/W		Port 1.5 wake up configuration
			000	Resistors off; Wake-up on falling edge of P15
			001	Resistors off; Wake-up on rising edge of P15
			010	Pull-down resistor activated; Wake-up disabled
			011	Resistors off; Wake-up disabled
			100	Pull-up resistor activated; Wake-up on falling edge of P15
			101	Pull-up resistor activated; Wake-up on rising edge of P15
			110	Pull-up resistor activated; Wake-up disabled
			111	Reserved for future use
12	RFU	-/W0		Reserved for future use

Bit	Symbol	Access	Value	Description
11 to 9	P14C[2:0]	R/W		Port 1.4 wake up configuration
			000	Resistors off; Wake-up on falling edge of P14
			001	Resistors off; Wake-up on rising edge of P14
			010	Pull-down resistor activated; Wake-up disabled
			011	Resistors off; Wake-up disabled
			100	Pull-up resistor activated; Wake-up on falling edge of P14
			101	Pull-up resistor activated; Wake-up on rising edge of P14
			110	Pull-up resistor activated; Wake-up disabled
			111	Reserved for future use
8	RFU	-/W0		Reserved for future use
7 to 5	P13C[2:0]	R/W		Port 1.3 wake up configuration
			000	Resistors off; Wake-up on falling edge of P13
			001	Resistors off; Wake-up on rising edge of P13
			010	Pull-down resistor activated; Wake-up disabled
			011	Resistors off; Wake-up disabled
			100	Pull-up resistor activated; Wake-up on falling edge of P13
			101	Pull-up resistor activated; Wake-up on rising edge of P13
			110	Pull-up resistor activated; Wake-up disabled
			111	Reserved for future use
4	WDTOFWUPEN [1]	R/W		Watchdog overflow as wake-up source configuration
			0	Wake-up on WDTOF disabled
			1	Wake-up on WDTOF enabled
3 to 1	P12C[2:0]	R/W		Port 1.2 wake up configuration
			000	Resistors off; Wake-up on falling edge of P12
			001	Resistors off; Wake-up on rising edge of P12
			010	Pull-down resistor activated; Wake-up disabled
			011	Resistors off; Wake-up disabled
			100	Pull-up resistor activated; Wake-up on falling edge of P12
			101	Pull-up resistor activated; Wake-up on rising edge of P12
			110	Pull-up resistor activated; Wake-up disabled
			111	Reserved for future use
0	WDTOF [2]	R/W1->0		Watchdog time-out flag
			0	Write access: No effect Read access: No watchdog time-out event
			1	Write access: Clear flag Read access: Watchdog time-out event

[1] For the bit description, see related bit-description in section "WDTOFWUPEN, wake-up by the watchdog time-out flag, enable (in PRESWUP0)".
[2] For the bit description, read in related bit-description in section "WDTOF, watchdog time-out flag (in PRESWUP0)".

Table 141. Port resistor and wake-up configuration register PRESWUP1 (reset value 8888h)

Bit	Symbol	Access	Value	Description
15 to 13	P21C[2:0]	R/W		Port 2.1 wake up configuration
			000	Resistors off; Wake-up on falling edge of P21
			001	Resistors off; Wake-up on rising edge of P21
			010	Pull-down resistor activated; Wake-up disabled
			011	Resistors off; Wake-up disabled
			100	Pull-up resistor activated; Wake-up on falling edge of P21
			101	Pull-up resistor activated; Wake-up on rising edge of P21
			110	Pull-up resistor activated; Wake-up disabled
			111	Reserved for future use
12, 8	P21MRES[1:0]	R/W		Port P2.1 weak pull-up configuration for motion sensor interface; only effective if P21WRES=0 (see Table 136)
			00	Standard weak pull-up (R_{PU_WK})
			01	Weak pull-up 1 for motion sensor interface (R_{PU_MD1})
			10	Weak pull-up 2 for motion sensor interface (R_{PU_MD2})
			11	Weak pull-up 3 for motion sensor interface (R_{PU_MD3})
11 to 9	P20C[2:0]	R/W		Port 2.0 wake up configuration
			000	Resistors off; Wake-up on falling edge of P20
			001	Resistors off; Wake-up on rising edge of P20
			010	Pull-down resistor activated; Wake-up disabled
			011	Resistors off; Wake-up disabled
			100	Pull-up resistor activated; Wake-up on falling edge of P20
			101	Pull-up resistor activated; Wake-up on rising edge of P20
			110	Pull-up resistor activated; Wake-up disabled
			111	Reserved for future use
7 to 5	P17C[2:0]	R/W		Port 1.7 wake up configuration
			000	Resistors off; Wake-up on falling edge of P17
			001	Resistors off; Wake-up on rising edge of P17
			010	Pull-down resistor activated; Wake-up disabled
			011	Resistors off; Wake-up disabled
			100	Pull-up resistor activated; Wake-up on falling edge of P17
			101	Pull-up resistor activated; Wake-up on rising edge of P17
			110	Pull-up resistor activated; Wake-up disabled
			111	Reserved for future use
4	RFU	-/W0		Reserved for future use
3 to 1	P16C[2:0]	R/W		Port 1.6 wake up configuration
			000	Resistors off; Wake-up on falling edge of P16

Bit	Symbol	Access	Value	Description
			001	Resistors off; Wake-up on rising edge of P16
			010	Pull-down resistor activated; Wake-up disabled
			011	Resistors off; Wake-up disabled
			100	Pull-up resistor activated; Wake-up on falling edge of P16
			101	Pull-up resistor activated; Wake-up on rising edge of P16
			110	Pull-up resistor activated; Wake-up disabled
			111	Reserved for future use
0	RFU	-/W0		Reserved for future use

Table 142. Port resistor and wake-up configuration register PRESWUP2 (reset value 8888h)

Bit	Symbol	Access	Value	Description
15 to 13	P25C[2:0]	R/W		Port 2.5 wake up configuration
			000	Resistors off; Wake-up on falling edge of P25
			001	Resistors off; Wake-up on rising edge of P25
			010	Pull-down resistor activated; Wake-up disabled
			011	Resistors off; Wake-up disabled
			100	Pull-up resistor activated; Wake-up on falling edge of P25
			101	Pull-up resistor activated; Wake-up on rising edge of P25
			110	Pull-up resistor activated; Wake-up disabled
			111	Pull-up resistor activated; Wake-up disabled
12	RFU	-/W0		Reserved for future use
11 to 9	P24C[2:0]	R/W		Port 2.4 wake up configuration
			000	Resistors off; Wake-up on falling edge of P24
			001	Resistors off; Wake-up on rising edge of P24
			010	Pull-down resistor activated; Wake-up disabled
			011	Resistors off; Wake-up disabled
			100	Pull-up resistor activated; Wake-up on falling edge of P24
			101	Pull-up resistor activated; Wake-up on rising edge of P24
			110	Pull-up resistor activated; Wake-up disabled
			111	Pull-up resistor activated; Wake-up disabled
8	RFU	-/W0		Reserved for future use
7 to 5	P23C[2:0]	R/W		Port 2.3 wake up configuration
			000	Resistors off; Wake-up on falling edge of P23
			001	Resistors off; Wake-up on rising edge of P23
			010	Pull-down resistor activated; Wake-up disabled
			011	Resistors off; Wake-up disabled

Bit	Symbol	Access	Value	Description
			100	Pull-up resistor activated; Wake-up on falling edge of P23
			101	Pull-up resistor activated; Wake-up on rising edge of P23
			110	Pull-up resistor activated; Wake-up disabled
			111	Pull-up resistor activated; Wake-up disabled
4	RFU	-/W0		Reserved for future use
3 to 1	P22C[2:0]	R/W		Port 2.2 wake up configuration
			000	Resistors off; Wake-up on falling edge of P22
			001	Resistors off; Wake-up on rising edge of P22
			010	Pull-down resistor activated; Wake-up disabled
			011	Resistors off; Wake-up disabled
			100	Pull-up resistor activated; Wake-up on falling edge of P22
			101	Pull-up resistor activated; Wake-up on rising edge of P22
			110	Pull-up resistor activated; Wake-up disabled
			111	Pull-up resistor activated; Wake-up disabled
0	RFU	-/W0		Reserved for future use

Table 143. Port resistor and wake-up configuration register PRESWUP3 (reset value 8888h)

Bit	Symbol	Access	Value	Description
15	RFU	-/W1		Reserved for future use
14 to 12	RFU	-/W0		Reserved for future use
11 to 9	P30C[2:0]	R/W		Port 3.0 wake up configuration
			000	Resistors off; Wake-up on falling edge of P30
			001	Resistors off; Wake-up on rising edge of P30
			010	Pull-down resistor activated; Wake-up disabled
			011	Resistors off; Wake-up disabled
			100	Pull-up resistor activated; Wake-up on falling edge of P30
			101	Pull-up resistor activated; Wake-up on rising edge of P30
			110	Pull-up resistor activated; Wake-up disabled
			111	Pull-up resistor activated; Wake-up disabled
8	RFU	-/W0		Reserved for future use
7 to 5	P27C[2:0]	R/W		Port 2.7 wake up configuration
			000	Resistors off; Wake-up on falling edge of P27
			001	Resistors off; Wake-up on rising edge of P27
			010	Pull-down resistor activated; Wake-up disabled
			011	Resistors off; Wake-up disabled
			100	Pull-up resistor activated; Wake-up on falling edge of P27

Bit	Symbol	Access	Value	Description
			101	Pull-up resistor activated; Wake-up on rising edge of P27
			110	Pull-up resistor activated; Wake-up disabled
			111	Pull-up resistor activated; Wake-up disabled
4	RFU	-/W0		Reserved for future use
3 to 1	P26C[2:0]	R/W		Port 2.6 wake up configuration
			000	Resistors off; Wake-up on falling edge of P26
			001	Resistors off; Wake-up on rising edge of P26
			010	Pull-down resistor activated; Wake-up disabled
			011	Resistors off; Wake-up disabled
			100	Pull-up resistor activated; Wake-up on falling edge of P26
			101	Pull-up resistor activated; Wake-up on rising edge of P26
			110	Pull-up resistor activated; Wake-up disabled
			111	Pull-up resistor activated; Wake-up disabled
0	RFU	-/W0		Reserved for future use

Table 144. Port resistor and wake-up configuration register PRESWUP4 (reset value 8888h)

Bit	Symbol	Access	Value	Description
15	RFU	-/W1		Reserved for future use
14 to 12	RFU	-/W0		Reserved for future use
11	RFU	-/W1		Reserved for future use
10 to 8	RFU	-/W0		Reserved for future use
7 to 5	P33C[2:0]	R/W		Port 3.3 wake up configuration
			000	Resistors off; Wake-up on falling edge of P33
			001	Resistors off; Wake-up on rising edge of P33
			010	Pull-down resistor activated; Wake-up disabled
			011	Resistors off; Wake-up disabled
			100	Pull-up resistor activated; Wake-up on falling edge of P33
			101	Pull-up resistor activated; Wake-up on rising edge of P33
			110	Pull-up resistor activated; Wake-up disabled
			111	Pull-up resistor activated; Wake-up disabled
4	RFU	-/W0		Reserved for future use
3 to 1	P32C[2:0]	R/W		Port 3.2 wake up configuration
			000	Resistors off; Wake-up on falling edge of P32
			001	Resistors off; Wake-up on rising edge of P32
			010	Pull-down resistor activated; Wake-up disabled
			011	Resistors off; Wake-up disabled

Bit	Symbol	Access	Value	Description
			100	Pull-up resistor activated; Wake-up on falling edge of P32
			101	Pull-up resistor activated; Wake-up on rising edge of P32
			110	Pull-up resistor activated; Wake-up disabled
			111	Pull-up resistor activated; Wake-up disabled
0	RFU	-/W0		Reserved for future use

2.14.3.7 Port alternative functions register PxALTF

Alternative digital ports functions can be selected for every port pin separately via the port alternative function register PxALTF which allows either byte or word access (Table 145, Table 146, and Table 147).

Table 145. Word and byte access to the status registers PxALTF

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
P1ALTF	P1ALTFH	P1ALTFL
P2ALTF	P2ALTFH	P2ALTFL

If an alternative port function is enabled, it overrules the direction bit (PxyD) and output register (PxyO) for this port.

Table 146. Port 1 alternative digital functions, P1ALTF (reset value 0000h)

Bit	Symbol	Access	Value	Description
15 to 14	P17AF[1:0]	R/W		alternative function port pin P17
			00	no alternative function
			01	LED driver function is enabled driven from P17O
			10	LED driver function is enabled driven from Timer 1 output (T1LINE)
			11	LED driver function is enabled driven from Timer 2 output (T2LINE)
13 to 12	P16AF[1:0]	R/W		alternative function port pin P16
			00	no alternative function, normal operation
			01	Timer 0 output (T0LINE)
			10	SPI0 SDIO
			11	SPI1 SDIO
11 to 10	P15AF[1:0]	R/W		alternative function port pin P15
			00	no alternative function, normal operation
			01	RFU
			10	RFU
			11	SPI1 CK
9 to 8	P14AF[1:0]	R/W		alternative function port pin P14
			00	no alternative function, normal operation
			01	Clock multiplexer output TMUX1

Bit	Symbol	Access	Value	Description
			10	SPI1 SDI
			11	SPI1 SDIO
7 to 6	P13AF[1:0]	R/W		alternative function port pin P13
			00	no alternative function
			01	Clock multiplexer output TMUX0
			10	IIU port modulator output
			11	SPI1 CK
5 to 4	P12AF[1:0]	R/W		alternative function port pin P12
			00	no alternative function
			01	Timer 2 output (T2LINE)
			10	Clock multiplexer output TMUX0
			11	SPI1 SDI
3 to 2	P11AF[1:0]	R/W		alternative function port pin P11
			00	no alternative function
			01	Timer 1 output (T1LINE)
			10	RFU
			11	SPI0 SDIO
1 to 0	P10AF[1:0]	R/W		alternative function port pin P10
			00	no alternative function
			01	Timer 0 output (T0LINE)
			10	IIU port modulator output
			11	SPI0 CK

Table 147. Port 2 alternative digital functions, P2ALTF (reset value 0000h)

Bit	Symbol	Access	Value	Description
15 to 14	P27AF[1:0]	R/W		alternative function port pin P27
			00	no alternative function, normal operation
			01	reserved for future use
			10	reserved for future use
			11	SPI0 SDIO
13 to 12	P26AF[1:0]	R/W		alternative function port pin P26
			00	no alternative function, normal operation
			01	reserved for future use
			10	SPI0 CK
			11	SPI0 SDIO
11 to 10	P25AF[1:0]	R/W		alternative function port pin P25

Bit	Symbol	Access	Value	Description
			00	no alternative function, normal operation
			01	reserved for future use
			10	reserved for future use
			11	SPI0 SDI
9 to 8	P24AF[1:0]	R/W		alternative function port pin P24
			00	no alternative function, normal operation
			01	Timer 2 output (T2LINE)
			10	SPI0 SDI
			11	SPI1 SDI
7 to 6	P23AF[1:0]	R/W		alternative function port pin P23
			00	no alternative function
			01	Timer 1 output (T1LINE)
			10	SPI0 SDIO
			11	SPI1 SDIO
5 to 4	P22AF[1:0]	R/W		alternative function port pin P22
			00	no alternative function
			01	Timer 0 output (T0LINE)
			10	SPI0 CK
			11	SPI1 CK
3 to 2	P21AF[1:0]	R/W		alternative function port pin P21
			00	no alternative function
			01	Timer 2 output (T2LINE)
			10	Reserved for future use
			11	SPI0 SDI
1 to 0	P20AF[1:0]	R/W		alternative function port pin P20
			00	no alternative function
			01	Timer 1 output (T1LINE)
			10	SPI0 CK
			11	SPI0 SDI

2.15 LED driver

The NCF215A / NCF215B features an integrated LED driver to directly drive an external LED connected to VBAT. Port P17_LED can be configured as a current sink to drive an LED without the need for external current limitation or pull-up resistors.

The LED driver supports 12 different current settings in two different ranges - low and high. The low range supports 8 steps with an LED drive current ranging from 1 × $I_{LED\_STEP\_L}$ to 8 × $I_{LED\_STEP\_L}$ and the high range 4 steps ranging from 5 × $I_{LED\_STEP\_H}$ to 8 × $I_{LED\_STEP\_H}$.

The LED driver is enabled by setting P17AF in Port 1 alternative digital functions register P1ALTFH (see Table 146). The P17_LED driver can also be controlled by the Timer 1 or 0. The LED current is switched with bit P17O in Port output control registers P1OUT (see Figure 48 and Table 148).

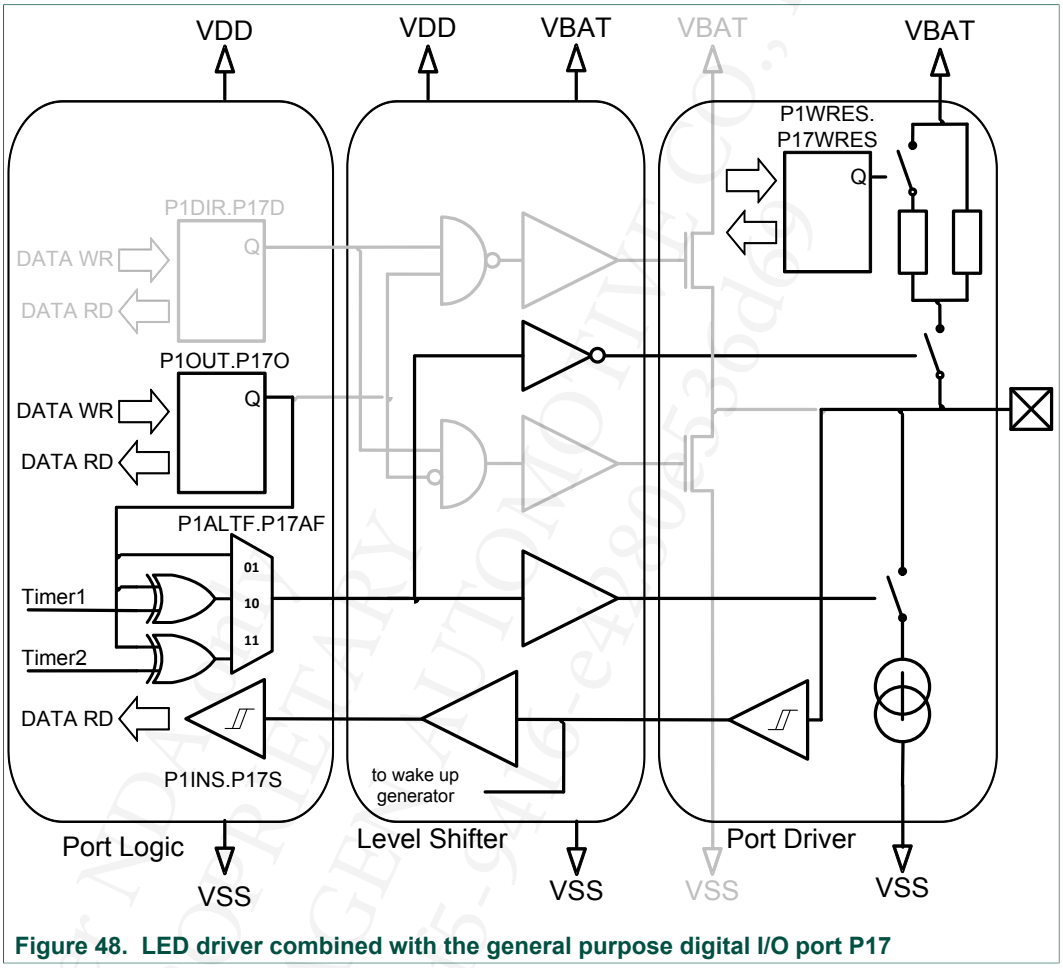


Figure 48. LED driver combined with the general purpose digital I/O port P17

In LED driver mode, the GPI/O input sense and output function are deactivated and the port direction bit has no influence on the port behavior (see grey circuitry in Figure 48). The maximum driving capability is limited to prevent damage of a connected LED and excessive battery drain. In POWER_OFF mode P17_LED is configured as GPIO input and the LED current driver is off. An internal pull-up is connected in parallel to the external diode to avoid any parasitic current when the driver is not enabled. P17WRES determines the internal pull-up resistor strength. The internal pull-up is deactivated as soon as the LED driver is activated in LED driver mode or when the port alternative function is configured.

2.15.1 Registers for LED driver control

In LED driver mode activated by setting P17AF = 01 (Table 146), the GPI/O output function is deactivated and the port direction bit has no influence on the port behavior (see grey circuitry in Figure 48). To enable LED driver on port P17_LED, the P17O control bit in P1OUT is used. When P17O is set to 1 the P17 input sense is disabled and the read value of P1INS.P17S is 0, LED driver is implemented as a current sink to VSS, which is enabled when P17O is set to 1. The maximum driving capability is limited to

prevent damage of a connected LED. In POWER_OFF mode P17_LED is configured as GPIO input and the LED current driver is off. An internal pull-up is connected in parallel to the external diode to avoid any parasitic current when the driver is not enabled. P17WRES determines the internal pull-up resistor strength. The internal pull-up is deactivated as soon as the LED driver is activated in LED driver mode or when the port alternative function is configured by P1ALTF.P17AF[1:0].

Table 148. P17O port output control bit in port output control registers P1OUT (LED driver is enabled)

Bit	Symbol	Access	Value	Description
7	P17O	R/W		P17 current sink to VSS enable
			0	P17 pull-up enabled to prevent P17 / LED cathode connection from floating P17 current sink to VSS disabled, LED is OFF.
			1	P17 pull-up disabled P17 current sink to VSS enabled, LED is ON.

2.15.1.1 LED driver control register, LEDCON

LEDCON register is provided to configure current range of the LED driver, The register LEDCON is described in Table 149.

Table 149. Tuning configuration registers LEDCON (reset value x000_0001b)

Bit	Symbol	Access	Value	Description
7	RFU	-/W0		Reserved for future use
6 to 4	RDT	-/W0		Reserved for device test
3 to 0	LEDRANGE[3:0]	R/W		Current range configuration
			0000	Low range: $I_{LED} = 1 \times I_{LED\_STEP\_L}$
			0001	Low range: $I_{LED} = 2 \times I_{LED\_STEP\_L}$
			0010	Low range: $I_{LED} = 3 \times I_{LED\_STEP\_L}$
			0011	Low range: $I_{LED} = 4 \times I_{LED\_STEP\_L}$
			0100	Low range: $I_{LED} = 5 \times I_{LED\_STEP\_L}$
			0101	Low range: $I_{LED} = 6 \times I_{LED\_STEP\_L}$
			0110	Low range: $I_{LED} = 7 \times I_{LED\_STEP\_L}$
			0111	Low range: $I_{LED} = 8\times I_{LED\_STEP\_L}$
			1000	Reserved for future use
			1001	Reserved for future use
			1010	Reserved for future use
			1011	Reserved for future use
			1100	High range: $I_{LED} = 5 \times I_{LED\_STEP\_H}$
			1101	High range: $I_{LED} = 6 \times I_{LED\_STEP\_H}$
			1110	High range: $I_{LED} = 7 \times I_{LED\_STEP\_H}$
			1111	High range: $I_{LED} = 8 \times I_{LED\_STEP\_H}$

LED driver current range settings, LEDRANGE[3:0]

One out of twelve LED driver current settings can be configured by LEDRANGE[3:0]. Default value 0001 indicates $I_{LED} = 2 \times I_{LED\_STEP\_L}$.

2.16 SPI 0 and 1

The NCF215A / NCF215B provides two identical synchronous, full duplex or half duplex serial peripheral interfaces SPI 0 and SPI 1 (SPI 0/1) with a baud rate selectable between 125 kHz and 4 MHz (with 8 MHz clock). The SPI 0/1 interfaces can be used to connect the PCx7900 (FraNTIC), PQx7980/81 (LoPSTer) or NCK2984 (MantraF). In full duplex mode, each interface uses three port pins, SCKx (serial clock), SDOx (serial data output master) and SDIx (serial data input master). Configuring the SPI 0/1 interfaces in half duplex mode, each interface requires two port pins SCKx and SD(I)Ox by sharing the data line for serial data input and output.

The SPI 0/1 interfaces allow 1 to 8 bit data transfer and provide double buffered operation with separate receive and transmit registers. The clock polarity, clock phase and shift direction (left or right) is configurable. The SPI 0/1 data transfer can be controlled via interrupt processing.

The SPI 0/1 controller supports a master mode, where the master provides the serial clock SCKx. An SPI 0/1 slave mode is not provided. It is possible to connect different slaves to the single bus, but only one slave at the time can communicate with the master. Hence, different slaves shall be enabled with separate slave select signals. The slave select signals must be implemented with general purpose I/O pins and must be controlled by the application program.

The controller supports also a modified SPI 0/1 communication in a pseudo slave mode or externally clocked master mode. In this mode the clock is derived from the slave, while the NCF215A / NCF215B communication control is still in the responsibility of the master device. The pseudo slave mode supports either full duplex or half duplex mode. This mode can be used to implement a software controlled SPI 0/1 slave mode and is optimized for interfacing with PCx7900 (FraNTIC) and PQx7980/81 (LoPSTer).

2.16.1 Modes

In all modes described below only the flag SPxBUSY should be used during transmit or receive, instead of using the transmit or receive buffer flags. Flag SPxBUSY should be checked to be 0 before starting a new data transfer.

2.16.1.1 Master mode, full duplex

The following sequence describes the processing of an SPI 0/1 data transfer when configured to be the master in full duplex mode. This process assumes that any prior data transfer has already been completed and that the receive buffer is empty.

Single byte transfer (see Figure 49):

1. Reset the SPI block and set the SPI 0/1 control registers
2. Write the data to be transmitted to the SPI 0/1 data register. This write access transfers the content of the transmit buffer into the shift register and starts the data transfer. The SPI 0/1 busy flag SPIxBUSY is set.
3. Wait until the SPIxBUSY is cleared. This indicates that the current data transfer has been completed.

4. Optional: Read the received data from the SPI 0/1 data register.

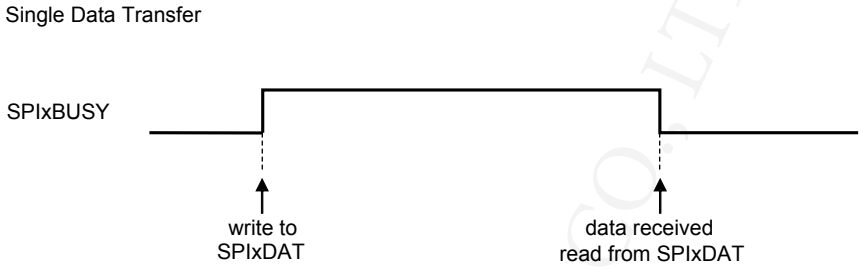


Figure 49. SPI 0/1 single data transfer

Multiple byte transfer (see Figure 50):

1. Reset the SPI block and set the SPI 0/1 control registers
2. Write the first data to be transmitted to the SPI 0/1 data register. This write access transfers the content of the transmit buffer into the shift register and starts the data transfer. The SPI 0/1 busy flag SPIxBUSY is set.
3. Wait until the SPI 0/1 busy flag SPIxBUSY is cleared. This indicates that the current data transfer has been completed.
4. Optional: Read the received data from the SPI 0/1 data register.
5. Write the next data to be transmitted to the SPI 0/1 data register. This write access transfers the content of the transmit buffer into the shift register and starts the data transfer. The SPI 0/1 busy flag SPIxBUSY is set.
6. Go to step 3 if more data shall be transmitted.
7. Wait until the last transfer is completed. The SPI 0/1 busy flag SPIxBUSY is cleared after completion.
8. Optional: Read the last received data from the SPI 0/1 data register.

Please note that the application can skip reading the SPI 0/1 data register, if received data is not desired.

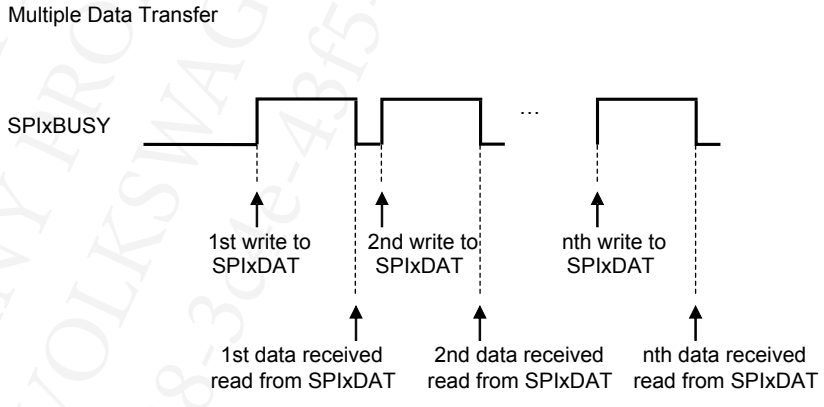


Figure 50. SPI 0/1 multiple data transfer

Dependent on the application, variations of the SPI data transfer sequence might be advantageous.

2.16.1.2 Master mode, half duplex

In half duplex mode the application shall select whether a transmit or receive transfer shall be accomplished.

The transmit mode behaves in the same way as the full duplex mode except that the received data is equal to the transmitted data.

In the receive mode every data transfer is requested by writing dummy data to the SPI 0/1 data register. If several bytes are requested the SPI 0/1 data register shall be written once for every byte.

2.16.1.3 Pseudo slave mode

In pseudo slave mode the clock is generated by the slave while the master has full control. In full duplex as well as in half duplex mode the master determines the number of transfers to be accomplished by the number of successive write accesses to the SPI 0/1 data register. Even in half duplex receive mode the master shall request every byte separately.

The transfer is synchronized according to the selected SPIxCLKPOL and SPIxCLKPHA settings with regard to the provided clock at SCKx. All clock edges before the start or after transfer completion will be ignored.

The application shall assure that the clock at SCKx is at the right state when starting a new data transfer. If the slave provides a continuous clock, the application can check the state of SCKx by reading the corresponding port pin input flag.

If the slave stops the SCKx generation during data transmission the application can trigger the bit SPIxSTOP to stop data reception. This request transfers the current content of the shift register into the receive buffer, while the status register holds the number of received bits.

The pseudo slave mode can be used to implement a software controlled SPI 0/1 slave mode. The software shall check the I/O port pin assigned as slave select input and shall control the SPI 0/1 block accordingly.

2.16.1.4 Pseudo slave initiation mode

The SPI 0/1 block supports a dedicated mode allowing a seamless hand-over of the clock from the master mode to the pseudo slave mode. If data transfer is started in this mode, SCKx is driven for half a clock period by the master and switches to slave mode thereafter. The further communication employs the clock from the slave. This mode supports PCx7900 (FraNTIC) TRANSMIT command and PQx7980/81 (LoPSTer) TRANSMIT and RECEIVE commands. These devices exploit the ninth clock pulse to enable the UHF transmitter/receiver.

The master generates only the first clock edge of the clock signal (rising/falling edge for SPIxCLKPOL = 0/1). Thereafter the port is configured for input and, if selected, the internal pull-up/pull-down resistor becomes active. In order to prevent that a false edge is detected on port SCKx until the slave drives the line, it is recommended to program the internal resistors correspondingly to the last driven state of SCKx. If PQx7980/81 (LoPSTer) is used, it is recommended to select a proper delay time (CLK2SCLK_DELAY) to avoid bus conflicts.

2.16.1.5 Shift register operation

The SPI 0/1 block has an 8 bit internal shift register, which is not directly accessible. Transmit data is transferred from the register TXBUFx into the shift register prior to the transfer and the content of the shift register is copied to RXBUFx upon completion of the transfer. The shift register holds transmit and receive data. For every bit shifted out of the shift register one received bit is shifted in. The most recent output bit is held in a separate

output flip-flop. The content of this output flip-flop defines the state of the SDOx line after transfer completion. This behavior is advantageous, if SPI 0/1 is used to generate a TRANSMIT command for FraNTIC or LoPSTer. In some modes the data value on SDOx is latched in FraNTIC or LoPSTer, if the slave is deselected (see Figure 51). After a reset of the SPI 0/1 block the output flip-flop holds the value '0'.

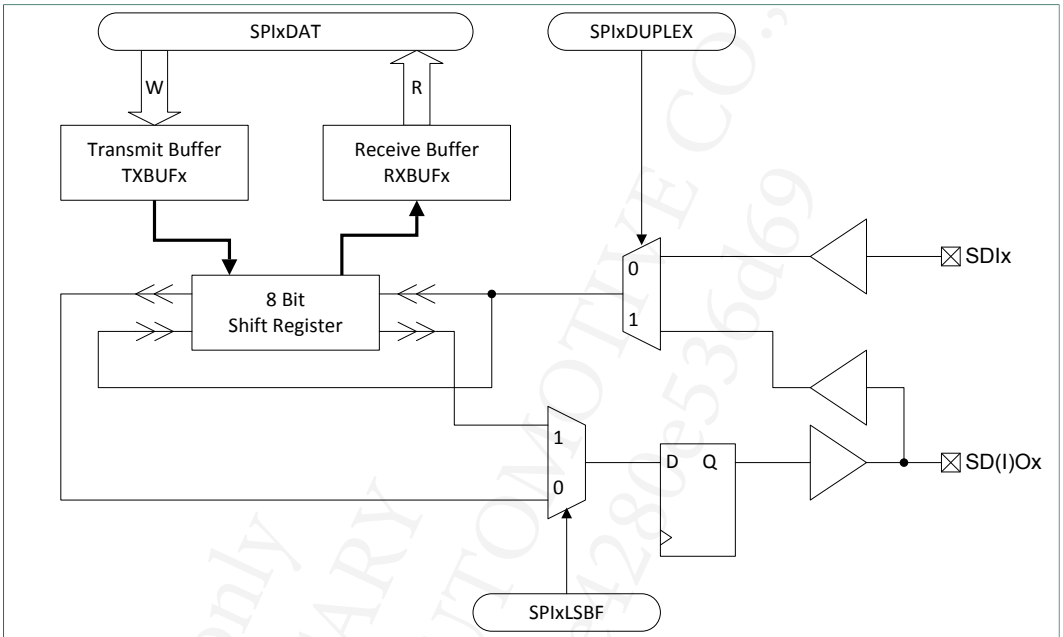


Figure 51. SPI 0/1 shift register organization

The internal shift register can work either in left shift or right shift mode dependent on whether data shall be transferred MSB first or LSB first. The common SPI 0/1 transfer mode is MSB first. Transmit data is shifted out to the left and received data is fed in on the right side of the shift register. Alternatively the SPI 0/1 block supports also transfers with LSB first. In this case transmit data is shifted out to the right and receive data is shifted in on the left side of the shift register.

Usually the SPI 0/1 transfer is byte oriented, thus all transfers are organized as 8 bit transfers. For the use as synchronous serial port controller also other bit granularities are supported (e.g. for FraNTIC and LoPSTer). For this, the SPI 0/1 block supports a selectable number of bits per transfer from 1 to 8. If less than 8 bits are selected for a single transfer the application has to consider the behavior of the shift register when writing to or reading from the SPI 0/1 data register.

During transfer with MSB first, transmit data shall always be left aligned as the leftmost bit is shifted out first. Transmit data shall be properly preprocessed by left shifts before it is written to the SPI 0/1 data register. Receive data is always right aligned with the LSB at the rightmost position.

Table 150. SPI data transfer example with 3 bits in full duplex mode, alignment of transmit and receive data

Transfer bit order	Transfer direction	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MSB first	Transmit data	T2	T1	T0	X	X	X	X	X
	Receive data	X	X	X	X	X	R2	R1	R0
LSB first	Transmit data	X	X	X	X	X	T2	T1	T0
	Receive data	R2	R1	R0	X	X	X	X	X

During transfer with LSB first, transmit data shall be always right aligned with the LSB at the rightmost position. Receive data is left aligned with the MSB at the leftmost position. The application has to perform proper right shifts after reading data from the SPI 0/1 data register.

2.16.2 Interaction with I/O port interface

The SPI 0/1 block interacts with 2 (half duplex mode) or 3 (full duplex mode) I/O pins, when enabled.

2.16.2.1 SDIx

In full duplex mode, the SDIx port is configured as input. If an internal pull-up/pull-down resistor is selected, it is active.

In half duplex mode, the SDIx port is not controlled by the SPI 0/1 block and can be used as standard I/O.

2.16.2.2 SDOx or SD(I)Ox

In both full duplex mode and half duplex transmit mode, the SDOx or SD(I)Ox port is configured as output. The values of the corresponding port output and direction flags are ignored. If no transfer is active the port drives the value stored in the output flip-flop, which in general corresponds to the last transmitted bit.

In half duplex receive mode, the SD(I)Ox port is configured as input. If an internal pull-up/pull-down resistor is selected, it is active. If the application switches between half duplex transmit mode and receive mode the port direction is changed automatically.

2.16.2.3 SCKx

In master mode, the SCKx port is configured as output. The values of the corresponding port output and direction flags are ignored. If no transfer is active the port drives the value selected with the clock polarity bit SPIxCLKPOL.

In pseudo slave mode, the SCKx port is configured as input. If an internal pull-up/pull-down resistor is selected, it is active.

In pseudo slave initiation mode, the SCKx port is configured as output prior to the first data transfer. At this stage the behavior is the same as in master mode configuration. With start of the first data transmission the port drives one clock edge. The port is driven for one internal SPI 0/1 clock cycle to the opposite state of SPIxCLKPOL before it is switched to input. Once the port is switched to input it behaves like the pseudo slave mode even if a new data transfer is started. The SPI 0/1 shall be switched to master mode to re-trigger the SCKx switching behavior. It is sufficient to change the mode, thus a data transfer in master mode is not needed.

2.16.3 Registers

2.16.3.1 SPI 0/1 data register SPIxDAT

The SPI 0/1 data register gives write access to the transmit buffer and read access to the receive buffer. Read access to the transmit buffer and write access to the receive buffer is not supported.

Table 151. SPI 0/1 data register SPIxDAT (reset value xxh)

Bit	Symbol	Access	Value	Description
7 to 0	SPIxDATA[7:0]	R/W		SPI 0/1 data

Transmitted and received data is buffered. Writing data to the SPI data register transfers them into the transmit buffer, while reading the SPI data register returns the value of the read data buffer, where it is transferred to when a transfer is complete. An internal shift register is used for the transmission and reception of the serial data.

2.16.3.2 SPI 0/1 control register SPIxCON0

SPI 0/1 control register 0 provide means to select the desired SPI operating mode. It is recommended to change these settings prior to activation of the SPI 0/1 block by setting SPIxEN. The settings in SPIxCON0 shall not be changed when a SPI 0/1 transfer is active. Otherwise this can result in unpredictable behavior.

Table 152. SPI 0/1 control register SPIxCON0 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	RFU	-/W0		Reserved for future use
6	SPIxLSBF	R/W		SPI 0/1 shift direction
			0	Left shift, MSB (bit 7) first
			1	Right shift, LSB (bit 0) first
5 to 4	SPIxCLKPOL SPIxCLKPHA	R/W		SPI 0/1 clock polarity (bit 5), SPI 0/1 clock phase (bit 4)
			00	First data driven prior to first SCKx rising edge Other data driven at SCKx falling edge Data sampled at SCKx rising edge
			01	First data driven at first SCKx rising edge Other data driven at SCKx rising edge Data sampled at SCKx falling edge
			10	First data driven prior to first SCKx falling edge Other data driven at SCKx rising edge Data sampled at SCKx falling edge
			11	First data driven at first SCKx falling edge Other data driven at SCKx falling edge Data sampled at SCKx rising edge
3 to 2	SPIxMODE[1:0]	R/W		SPI 0/1 operating mode
			00	Master mode
			01	Reserved for future use
			10	Pseudo slave mode
			11	Pseudo slave initiation mode
1 to 0	SPIxDUPLEX[1:0]	R/W		SPI 0/1 duplex mode
			00	Full duplex mode (affecting SCKx, SDOx, SDIx)
			01	Reserved for future use
			10	Half duplex mode – transmission (affecting SCKx, SD(I)Ox)
			11	Half duplex mode – reception (affecting SCKx, SD(I)Ox)

SPIxLSBF, SPI 0/1 shift direction:

This bit selects the shift direction of the internal shift register and hence whether data is transferred LSB or MSB first.

SPIxCLKPOL, SPIxCLKPHA, SPI 0/1 clock polarity and clock phase:

The polarity and phase of port SCKx is selected with the bits SPIxCLKPOL and SPIxCLKPHA. The setting of SPIxCLKPOL defines the logic level of SCKx, if the master mode is selected and no transfer is active. The pin SCKx is then driven to the same value as SPIxCLKPOL.

Figure 52 shows the timing diagram for the four SPI 0/1 data transfer formats available at the example of a single 8 bit data transfer. SSELx denotes an active low slave select signal that has to be generated by the application, e.g. with the help of a standard I/O port.

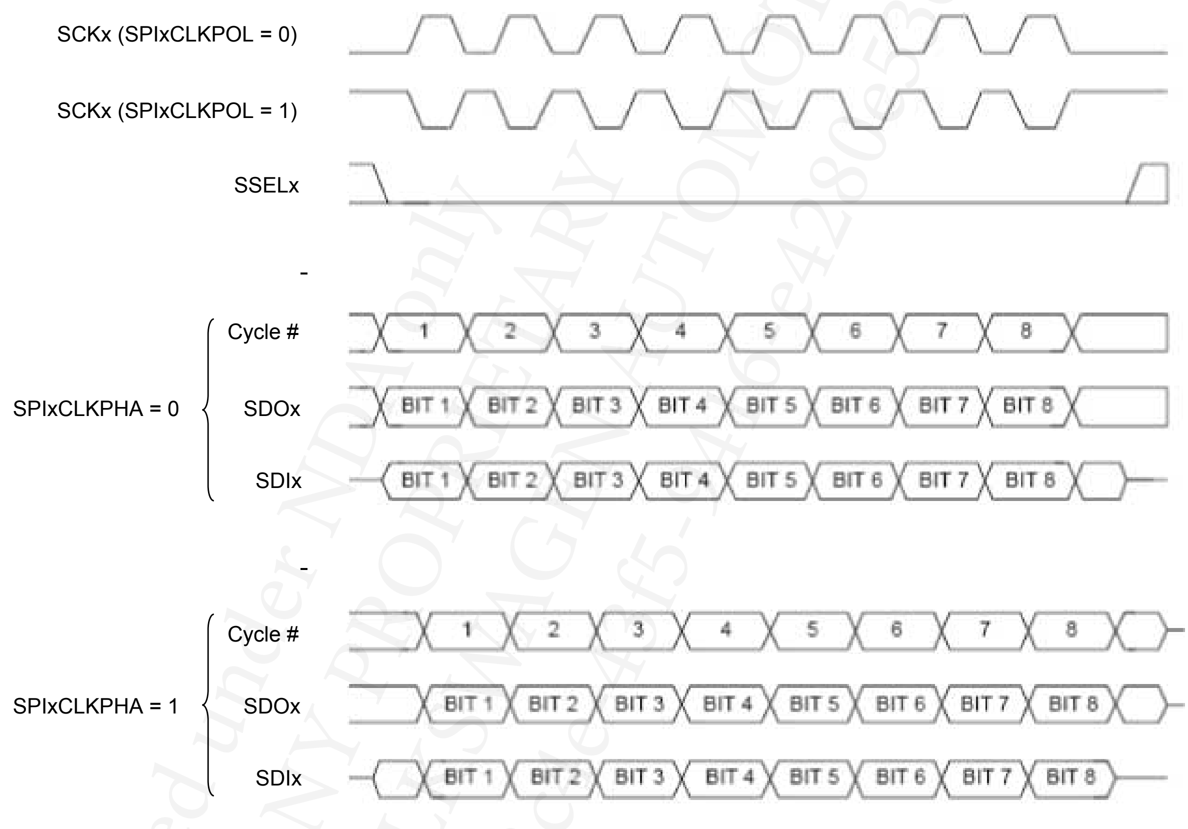


Figure 52. SPI 0/1 data transfer in full duplex mode

SPIxDUPLEX[1:0], SPI 0/1 duplex mode

The SPI 0/1 duplex mode selection configures the SPI 0/1 block either for full or half duplex mode. In full duplex mode the three port pins SCKx, SDOx and SDIx are assigned with special functions. In half duplex mode the two port pins SCKx and SD(I)Ox are assigned, while the application has to select whether transmission or reception is activated.

2.16.3.3 SPI 0/1 control register SPIxCON1

SPI 0/1 control register 1 provide means to select the SPI 0/1 baudrate, the SPI 0/1 interrupt source and bits to enable, reset and stop the SPI 0/1 block.

Table 153. SPI 0/1 control register SPIxCON1 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	RFU	-/W0		Reserved for future use
6 to 4	SPIxCLK[2:0]	R/W		SPI 0/1 clock
			000	Internal SPI 0/1 clock rate: PCLK Transfer baudrate (master mode): PCLK/2 Max. transfer baudrate (pseudo slave mode): PCLK/8
			001	Internal SPI 0/1 clock rate: PCLK/2 Transfer baudrate (master mode): PCLK/4 Max. transfer baudrate (pseudo slave mode): PCLK/16
			010	Internal SPI 0/1 clock rate: PCLK/4 Transfer baudrate (master mode): PCLK/8 Max. transfer baudrate (pseudo slave mode): PCLK/32
			011	Internal SPI 0/1 clock rate: PCLK/8 Transfer baudrate (master mode): PCLK/16 Max. transfer baudrate (pseudo slave mode): PCLK/64
			100	Internal SPI 0/1 clock rate: PCLK Transfer baudrate (master mode): PCLK/8 Max. transfer baudrate (pseudo slave mode): PCLK/8
			101	Internal SPI 0/1 clock rate: PCLK/2 Transfer baudrate (master mode): PCLK/16 Max. transfer baudrate (pseudo slave mode): PCLK/16
			110	Internal SPI 0/1 clock rate: PCLK/4 Transfer baudrate (master mode): PCLK/32 Max. transfer baudrate (pseudo slave mode): PCLK/32
			111	Internal SPI 0/1 clock rate: PCLK/8 Transfer baudrate (master mode): PCLK/64 Max. transfer baudrate (pseudo slave mode): PCLK/64
3	SPIxINTSS	R/W		SPI 0/1 interrupt source
			0	Transmit buffer empty flag SPIxTXBE
			1	Receive buffer full flag SPIxRXBF
2	SPIxSTOP	R0/W		Stop SPI 0/1 communication
			0	No effect
			1	Stop SPI 0/1 transfer
1	SPIxRST	R0/W		SPI 0/1 reset
			0	No effect
			1	Reset SPI 0/1 block
0	SPIxEN	R/W		SPI 0/1 enable
			0	SPI 0/1 block disabled

Bit	Symbol	Access	Value	Description
			1	SPI 0/1 block enabled

SPIxCLK[2:0], SPI 0/1 clock:

The SPI 0/1 clock selection bits SPIxCLK allow setting of the internal clock rate and the transfer baudrate. The timings shall be set prior to a transfer taking place.

In master mode the transfer baudrate can be set either to 1/2 or 1/8 of the internal clock rate. The first setting is intended for maximum communication speed. The second setting can be used in an environment where the baudrate in the master mode and the pseudo slave mode should be aligned.

In pseudo slave mode the clock at SCKx is sampled with the internal SPI 0/1 clock rate, which shall be selected at least 8 times higher than the expected SPI 0/1 baudrate. Hence, the baudrate in the pseudo slave mode shall not exceed 1/8 of the internal clock rate.

The clock for the SPI 0/1 block is derived from the peripheral clock PCLK.

The setting of SPIxCLK shall not be changed when a SPI 0/1 transfer is active. Otherwise this can result in unpredictable behavior.

SPIxINTSS, SPI 0/1 interrupt source:

The application can select the source of the SPI 0/1 interrupt with the interrupt source selection bit SPIxINTSS. The interrupt request signal is statically disabled, if the SPI 0/1 block is disabled (Figure 53). The interrupt request is cleared if SPIxBUSY has changed to ‘0’.

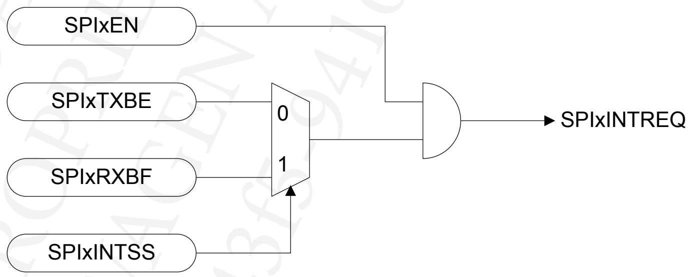


Figure 53. SPI 0/1 interrupt request generation

SPIxSTOP, stop SPI 0/1 communication:

A running SPI 0/1 transfer can be interrupted by setting the bit SPIxSTOP to '1'. This stops the internal state machine and transfers the current content of the shift register into the receive buffer. The SPI 0/1 status flags are updated accordingly. The number of received bits can be retrieved by reading the value SPIxBIT in the SPI 0/1 status register.

Bit SPIxSTOP can be used to finish a SPI 0/1 transfer in pseudo slave mode without losing the last received bits.

After stopping a communication with SPIxSTOP, the SPI 0/1 shall be reset with bit SPIxRST.

Reading of bit SPIxSTOP always yields '0'.

SPIxRST, SPI 0/1 reset:

The SPI 0/1 reset bit can be used to reset the internal state machine. The reset is accomplished, if a '1' is written to bit SPIxRST. Reading of bit SPIxRST always yields '0'.

The reset bit influences the internal state machine, the bit counter, the output flip-flop, the status flags and some other control flip-flops. The configuration of the port pins is not influenced. The only exception is the pseudo slave initiation mode. After a reset it is configured to its initial state, hence the port pin SCKx is configured as output.

If the reset is accomplished when a transfer is ongoing the current transfer is interrupted immediately.

SPIxEN, SPI 0/1 enable:

The SPI 0/1 enable bit enables the entire SPI 0/1 block. If the SPI 0/1 is disabled all blocks except the control registers are reset to their initial state and the internal clock generation is stopped. When the SPI 0/1 block is enabled the assigned I/O port pins are reconfigured.

2.16.3.4 SPI 0/1 status register SPIxSTAT

The SPI 0/1 status register holds mainly status information of the SPI 0/1 block in order to detect e.g. completion of a data transfer. The status bits are read-only.

Any write access to these bits is ignored and does not alter the state of a status bit. It has to be noted that the status register also contains some control bits.

Table 154. SPI 0/1 status register SPIxSTAT (reset value 00h)

Bit	Symbol	Access	Value	Description
7	SPIxBUSY	R/-		SPI 0/1 busy flag
			0	SPI 0/1 block does not transfer data
			1	SPI 0/1 transfer is currently active
6	SPIxTXBE	R/W1->0		SPI 0/1 transmit buffer empty, the next data may be written to SPIxDAT after SPIxBUSY has changed from 1 to 0. Writing a "1" to this bit resets the flag.
			0	Buffer full
			1	Buffer empty
5	SPIxRXBF	R/-		SPI 0/1 receive buffer full, the data may be read from SPIxDAT after SPIxBUSY has changed from 1 to 0.
			0	Buffer empty
			1	Buffer full
4	SPIxRXBOVF	R/-		SPI 0/1 receive buffer overflow
			0	No overflow
			1	Receive buffer is overwritten and previous data is lost
3	RFU	-/W0		Reserved for future use
2 to 0	SPIxBIT[2:0]	R/W		Number of bits per SPI 0/1 transfer and transfer bit counter

Bit	Symbol	Access	Value	Description
			000	Write access: 8 bit transfer Read access (after stop with SPIxSTOP): 0 bit received (SPIxRXBF = 0) or 8 bit received (SPIxRXBF = 1)
			001	Write access: 1 bit transfer Read access (after stop with SPIxSTOP): 1 bit received
			010	Write access: 2 bit transfer Read access (after stop with SPIxSTOP): 2 bit received
			011	Write access: 3 bit transfer Read access (after stop with SPIxSTOP): 3 bit received
			100	Write access: 4 bit transfer Read access (after stop with SPIxSTOP): 4 bit received
			101	Write access: 5 bit transfer Read access (after stop with SPIxSTOP): 5 bit received
			110	Write access: 6 bit transfer Read access (after stop with SPIxSTOP): 6 bit received
			111	Write access: 7 bit transfer Read access (after stop with SPIxSTOP): 7 bit received

SPIxTXBE, SPI 0/1 transmit buffer empty:

SPIxTXBE = '1' signals that the transmit buffer is empty. This bit is automatically cleared by any write access to the SPI 0/1 data register. Also, writing a "1" to this bit resets the flag. The next data may be written to SPIxDAT after SPIxBUSY has changed from 1 to 0.

Note: The behavior of this flag does not depend on the settings of SPIxMODE and SPIxDUPLEX.

SPIxRXBF, SPI 0/1 receive buffer full:

SPIxRXBF = '1' signals that the receive buffer is full. This bit is automatically cleared by any read access to the SPI 0/1 data register. The data may be read from SPIxDAT after SPIxBUSY has changed from 1 to 0.

This bit is always '0' after a reset of the SPI 0/1 block.

Note: The behavior of this flag does not depend on the settings of SPIxMODE and SPIxDUPLEX.

SPIxRXBOVF, SPI 0/1 receive buffer overflow:

If the SPI 0/1 data register has not been read by the application when the next data transfer completes, the receive buffer is overwritten with the new data byte and the previous data is lost. This buffer overflow is signaled by setting the receive buffer overflow flag SPIxRXBOVF to '1'.

The bit SPIxRXBOVF is automatically cleared by any read access to the SPI 0/1 data register.

SPIxBIT[2:0], number of bits per SPI 0/1 transfer and transfer bit counter:

The sub-register SPIxBIT has two different meanings dependent on whether it is written or read.

For write access, the sub-register SPIxBIT determines the number of bits per SPI 0/1 transfer. The values 1 to 7 correspond directly to the requested number of transmitted/ received bits. The value 0 shall be selected for an 8 bit transfer. The sub-register SPIxBIT is double buffered. If a transfer is active and the content of SPIxBIT is changed, the new value becomes effective at the beginning of the next transfer, hence it is loaded at the same time when data is transferred from the transmit buffer into the internal shift register.

During read access, the sub-register SPIxBIT gives access to the internal SPI 0/1 bit counter. If a transfer is stopped with bit SPIxSTOP, the application can retrieve the number of received bits. The value SPIxBIT = 0 can have two different meanings: If the flag SPIxRXBF is '0', no bit was received whereas SPIxRXBF = '1' indicates that 8 bits were received (provided that SPIxRXBOVF = '0'). No decision can be taken in case of a receive buffer overflow.

2.17 General purpose A/D converter

The NCF215A / NCF215B has a Successive Approximation Analog to Digital Converter (ADC) which can be used to measure voltage levels (battery voltage or external voltage levels) and temperature. The ADC is optimized regarding conversion time and overall power consumption. It supports automatic averaging over a configurable number of consecutive measurements.

Note that the VBAT brownout monitor (see VBATBRNREG bit in Section 2.2.4.5) shall be used to monitor the supply voltage level at VBAT to verify whether the supply voltage at VBAT was sufficient for the complete duration of the ADC conversion.

2.17.1 Battery voltage measurement

The NCF215A / NCF215B features battery voltage measurement to analyze and track the condition and life cycle status of the battery.

The voltage at pin VBAT is internally scaled to match with the internal reference voltage for the A-D conversion.

The measurement setup with battery voltage scaling, supply and the voltage source are shown in Figure 54.

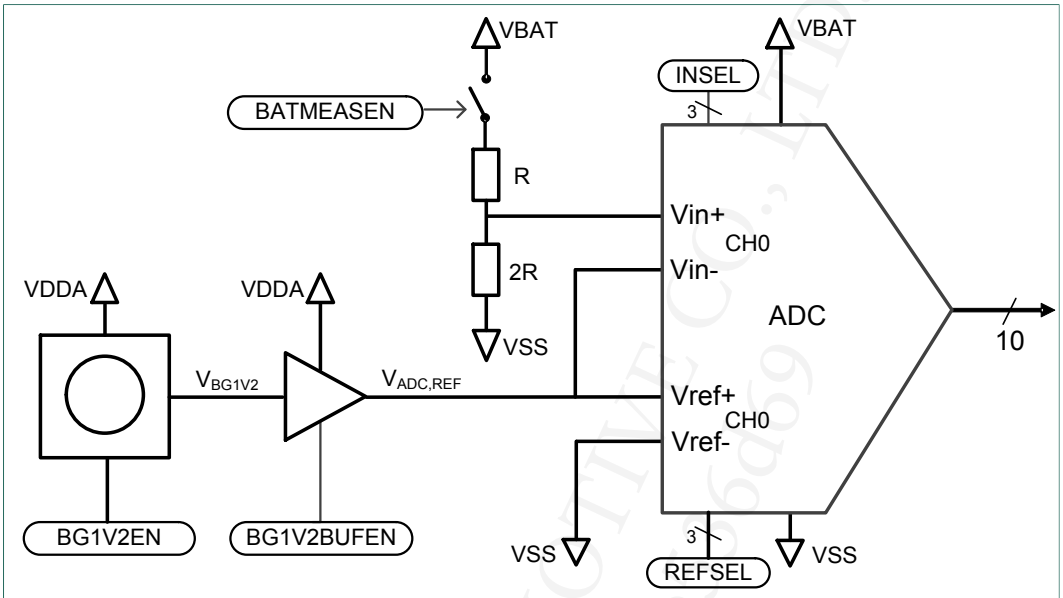


Figure 54. Battery supply voltage measurement

Similar to the default ADC input selection (INSEL = 000b), the default ADC reference selection (REFSEL = 000b) must be used for battery voltage measurements.

The reference block is accommodated in the VDDA supply domain. The application software must turn on the VDDA supply (PCON0.VDDARGLEN = 1) before the supply voltage measurement unit can be used, considering the VDDA regulator start-up time $t_{VDDA,PON}$. A buffered band-gap provides the reference voltage for the ADC, $V_{ADC,REF}$. It must be switched on by setting BG1V2EN = 1 and BG1V2BUFEN = 1 in the register. The buffered reference voltage, $V_{ADC,REF}$ is assumed settled after $t_{BG,PON}$.

The battery voltage is scaled down via a switched resistive divider and is measured against the reference voltage for the best resolution. The measurement output is given by:

$$VBATmeas = ADCDATA \cdot \frac{2 \cdot V_{ADC,REF}}{1024} \cdot \frac{3}{2} \quad (15)$$

Excluding VDDA supply, band-gap and band-gap buffer power-up times, the time for a single conversion is:

$$t_{ADC,CONV} = t_{PON} + t_{SAMPLE} + t_{CONV} + t_{ADC,PDWN} \quad (16)$$

Before triggering A-D conversion for the battery voltage input, the battery voltage sensor (a voltage divider) has to be enabled by means of BATMEASEN bit set 1. When default sampling time used, SAMTIM=00b, SAMTIMEXT=0, and the Main RC oscillator selected as ADC clock source, CLKCON2.ADCCLKSEL=0, the ADC clock frequency will be $f_{ADC,CLK}$ = 4 MHz. As typical battery measurement time is defined by 8 clock cycles for t_{PON} (2 µs), 4 cycles for t_{SAMPLE} (1 µs), 21 cycles for t_{CONV}, and one cycle for the power down, $t_{ADC,PDWN}$, of the ADC, the $t_{ADC,CONV}$ will be equal to 34 clock cycles duration, or 8.5 µs.

For achieving an optimal sampling rate, in software, it is recommended to poll the ADCCON.CONVSTART flag, or the ADC end-of-conversion interrupt flag IF_ADC. User interrupt from ADC testing the IF_ADC flag can also be used.

2.17.2 Temperature measurement

The NCF215A / NCF215B contains a built-in temperature measurement unit to get feedback of the environmental conditions of the device.

The internal reference voltage is scaled to match with the output voltage of the temperature sensor.

The temperature sensor is powered on in case the temperature sensor is enabled by means of ADCCON.TSENSEN bit set 1.

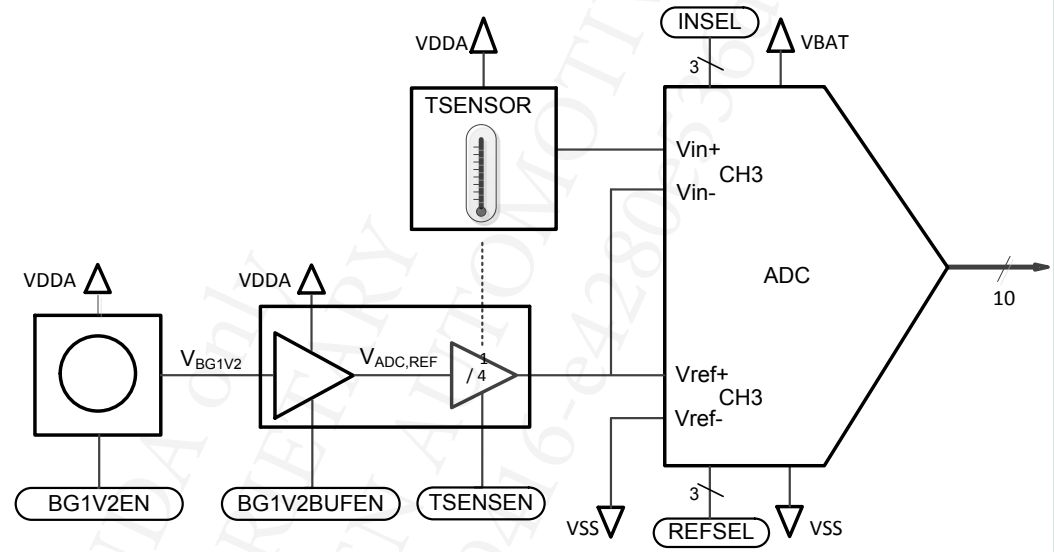


Figure 55. Temperature measurement

Before triggering AD-conversion, the ADC input (INSEL =011b) from temperature sensor has to be selected. Also, an optimized voltage reference must be chosen (REFSEL =011b) for measuring the temperature sensor differential output more accurately.

The measured differential voltage of the temperature sensor is in range between V_{TEMP_min} = -287 mV and V_{TEMP_max} = +278 mV, for the obtained ADCDATA it can be calculated as:

$$VTEMPmeas = (ADCDATA - 512) \cdot \frac{2 \cdot V_{ADC,REF}}{4 \cdot 1024} \quad (17)$$

The Temperature Sensor (TSENSOR) and reference block are accommodated in the VDDA supply domain. As for any ADC measurement using the internal band-gap circuit, the application software must switch-on the VDDA supply (PCON0.VDDARGLEN = 1) before the temperature measurement unit and the ADC can be used, considering the VDDA regulator start-up time $t_{VDDA,PON}$. The buffered band-gap must be switched on via BG1V2EN = 1 and BG1V2BUFEN = 1 to provide the optimized voltage reference after $t_{BG,PON}$. Due to limited drive capability of the temperature sensor output, an increased ADC sampling time of at least 16 µs has to be chosen (SAMTIM[1:0] = 10b).

$$Temp[\,°C\,] = 25 + \frac{ADCDATA - OFF_{TADC}}{G_{TADC}} \quad (18)$$

The output of the A-D converter, ADCDATA, is proportional to the temperature. The typical gain of the temperature sensor is G_{TADC}. Nominal temperature measurement offset at 25 °C is specified as OFF_{TADC}. Best accuracy can be achieved by an application calibration measurement and compensation of the offset.

2.17.3 External voltage measurement

The NCF215A / NCF215B in package HVQFN40 features an external voltage measurement for voltage levels applied between P16 (positive input) and P11, P15, or P32 (negative input).

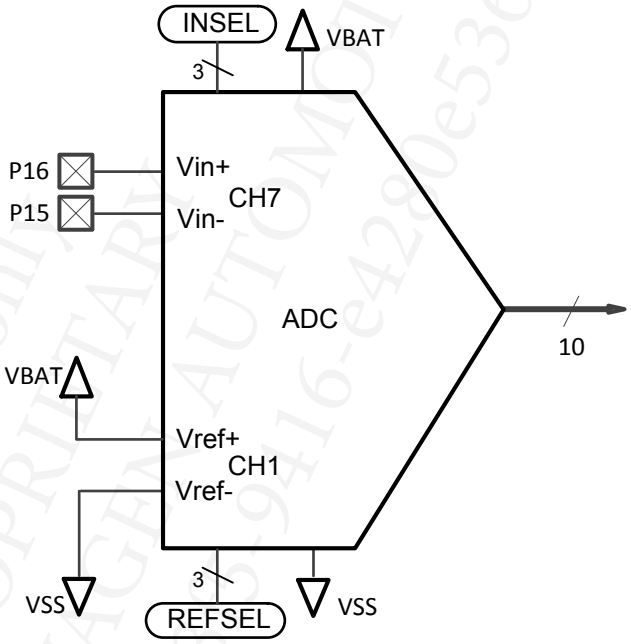


Figure 56. External voltage measurement - CH7

The external input configuration with pins P16 and P15 is connected by INSEL=7, i.e. to the input (Vin+, Vin-) channel CH7. To enable the external input measurements as shown in Figure 56, pins P16 and P15 have to be connected to the ADC as external voltage inputs on the input channel CH7.

Input channel CH6 (INSEL = 6) selects the external input pins P16 and P32.

Only when using CH1, the application software is requested to use dedicated system-call to change the pin configuration. After the measurement on CH1 is done, the application software is requested to revert the P16 and P11 pin configuration by using dedicated system-call. Thereby, the buffered reference is used and the application is requested to do both, to enable the VDDA supply, the band-gap circuit with the output buffer, and to set the INSEL=001b and REFSEL (optionally, the SAMTIM) according to Table 156.

Three reference selections and thereby three dynamic ranges, are possible for the external voltage measurements. The ADC reference settings REFSEL = 010b select two external pins P17_LED and P12 on the reference input (Vref+,Vref-) levels. REFSEL =

001b offers dynamic range Vin_diff = (-V_{BAT}, +V_{BAT}) while selecting REFSEL=000b will enable for dynamic range Vin_diff = (-$V_{ADC,REF}$, +$V_{ADC,REF}$). The REFSEL=000b requires the reference block enabled as explained in Section 2.17.1 and Section 2.17.2.

The external voltage is directly measured against the selected reference voltage, Vref = Vref_ext, Vref = $V_{ADC,REF}$, or Vref = V_{BAT}, allowing for 10-bit resolution.

$$VEXTmeas = (ADCDATA - 512) \cdot \frac{2 \cdot V_{ref}}{1024} \quad (19)$$

According to the limiting values, it is not allowed to apply negative voltages lower than -0.3V to any I/O pin, hence to P16, P11, P15, P32, P17_LED, and P12.

For achieving an optimal sampling rate by software, it is recommended to use the ADC end-of-conversion interrupt flag, IF_ADC, and optionally, a user interrupt servicing routine.

2.17.4 ADC registers

ADC access to configure the ADC and trigger measurements is done via ADCCON. The converted data is stored in ADCDAT, and in case of multiple conversions (SUMCNT greater than 0), also in the ADCSUM register. ADCCON, ADCDAT and ADCSUM are described in Table 156 to Table 160.

2.17.4.1 ADC control register, ADCCON

The register ADCCON provides byte and word access.

Table 155. Word and byte access to the ADC control register ADCCON

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
ADCCON	ADCCONH	ADCCONL

Table 156. ADC control register ADCCON (reset value 00000000_0000xx00b)

Bit	Symbol	Access	Value	Description
15 to 13	INSEL[2:0]	R/W		ADC input selection
			000	Battery voltage measurement
			001	External input measurement, voltage applied on P16 and P11; P11 and P16 are configured in analog mode and the settings P1DIR.1 and P1DIR.6 are ignored
			010	RFU
			011	Temperature sensor measurement
			100	RFU
			101	RFU
			110	External input measurement, voltage applied on P16 and P32; P16 and P32 are automatically configured in analog mode and the settings P1DIR.6 and P3DIR.2 are ignored

Bit	Symbol	Access	Value	Description
			111	External input measurement, voltage applied on P16 and P15; P15 and P16 are automatically configured in analog mode and the settings P1DIR.5 and P1DIR.6 are ignored
12 to 10	REFSEL[2:0]	R/W		Reference selection
			000	Buffered band-gap reference voltage, $V_{ref} = V_{ADC,ref}$ (for battery voltage measurement)
			001	VBAT and VSS
			010	External reference, applied on P17_LED and P12; P12 and P17 are automatically configured in analog mode and the settings P1DIR.2 and P1DIR.7 are ignored
			011	Optimized reference selection for temperature measurement
			100	RFU
			101	RFU
			110	RFU
			111	RFU
9 to 8	SAMTIM[1:0]	R/W		ADC sampling time selection, t_{SAMPLE} (in conjunction with SAMTIMEXT)
			00	SAMTIMEXT=0: 4 / $f_{ADC,CLK}$ [1], SAMTIMEXT=1: 8 / $f_{ADC,CLK}$
			01	SAMTIMEXT=0: 32 / $f_{ADC,CLK}$, SAMTIMEXT=1: 16 / $f_{ADC,CLK}$
			10	SAMTIMEXT=0: 64 / $f_{ADC,CLK}$, SAMTIMEXT=1: 48 / $f_{ADC,CLK}$
			11	SAMTIMEXT=0: 256 / $f_{ADC,CLK}$, SAMTIMEXT=1: 128 / $f_{ADC,CLK}$
7	TSENSEN	R/W		Temperature sensor enable
			0	Temperature sensor disabled
			1	temperature sensor enabled
6	BATMEASEN	R/W		Battery voltage sensor enable
			0	Battery voltage sensor disabled
			1	Battery voltage sensor enabled
5	BG1V2BUFEN	R/W		Band-gap reference buffer enable
			0	Band-gap reference buffer off
			1	Band-gap reference buffer on (VDDA supply needed)
4	BG1V2EN	R/W		Band-gap reference enable
			0	Band-gap reference off
			1	Band-gap reference on (VDDA supply needed)
3	SAMTIMEXT	R/W		ADC sampling time selection, extension of SAMTIM[1:0]
			0	primary settings: (4, 32, 64, 256) * 1/$f_{ADC,CLK}$ [1]
			1	extended settings: (8, 16, 48, 128) * 1/$f_{ADC,CLK}$
2	ADCPOWERON	R/W		ADC power-on enable
			0	ADC powered off
			1	ADC powered on

Bit	Symbol	Access	Value	Description
1	CONVRESET	R0/W		ADC Conversion Reset
			0	no effect
			1	Reset conversion; aborts a running conversion
0	CONVSTART	R/W		ADC Conversion Run/Start
			0	Write access: no effect Read access: no conversion running
			1	Write access: Start Conversion, triggers automatic power-on of ADC Read access: Conversion running

[1] For the ADC clock source selection, see CLKCON2, ADCCLKSEL

2.17.4.2 ADC data register, ADCDAT

The register ADCDAT provides byte and word access to the converted data or to the summed multiple conversion results.

Table 157. Word and byte access to the ADC data register ADCDAT

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
ADCDAT	ADCDATH	ADCDATL

Table 158. ADC data (sum) register ADCDAT (reset value 0000h)

Bit	Symbol	Access	Value	Description
15 to 10	ADCSUM[15:10]	R/-		Bits 15 to 10 of the multiple conversion sum
9 to 8	ADC(SUM)[9:8]	R/-		Bit 9 and 8 of single ADC result or the multiple conversion sum
7 to 0	ADC(SUM)[7:0]	R/-		Bit 7 to 0 of single ADC result or the multiple conversion sum

2.17.4.3 ADC multiple conversion count and sum register, ADCSUM

The register ADCSUM provides byte and word access to the multiple conversion count settings or to the highest two bits of the summed multiple conversion results. Note, during single conversion, the highest two ADCSUM bits will be 0.

Table 159. Word and byte access to the ADC data count and sum register ADCSUM

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
ADCSUM	ADCSUMH	ADCSUML

Table 160. ADC data (sum) register, ADCSUM (reset value 0000_0000_xxxx_xx00b)

Bit	Symbol	Access	Value	Description
15 to 8	SUMCNT[7:0]	R/W	0d - 255d	0 - single conversion, or Value+1 conversions in the sum
7 to 2	RFU	R/-		Reserved for future use
1 to 0	ADCSUM[17:16]	R/-		Bit 17 and 16 of the multiple conversion sum

2.17.4.4 ADC external input control register, BISTCON

The register BISTCON provides byte and word access to the external input channel enable. BISTCON is fully accessible in SYSTEM mode only. An application executed in USER mode shall use a system call to change the register.

Table 161. Word and byte access to the ADC external control register, BISTCON

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
BISTCON	BISTCONH	BISTCONL

Table 162. ADC external input control, BISTCON (reset value 0000h)

Bit	Symbol	Access SYSTEM mode	Access USER mode	Value	Description
15 to 8	RDT	-/W0	-/-		Reserved for device test
7	DCBUSEN	R/W	R/-		DC-bus control bit
				0	Disabled
				1	Enabled
6 to 0	RDT	-/W0	-/-		Reserved for device test

2.18 AES calculation unit

The devices which support built-in WFS-5d based transponder emulations employ the AES co-processor unit for hardware accelerated device authentication, message encryption and rolling code generation.

The hardwired AES co-processor provides encryption with a fixed secret key length of 128 bits and forward encryption.

The co-processor operates with two internal 128 bit registers (AESKEYREG and AESDATAREG) for storage of the secret key and plain/enciphered data, respectively (Figure 57). Both registers have to be loaded prior to an AES calculation. Enciphered data supersedes initial plain data and can be retrieved from register AESDATAREG after the calculation. The content of AESKEYREG is not altered.

A reset function allows clearing of all registers and the internal state of the AES co-processor on request.

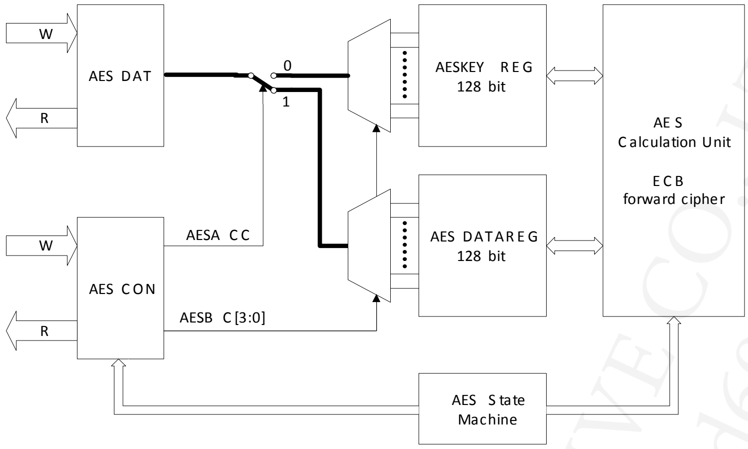


Figure 57. Block diagram of AES calculation unit

2.18.1 Modes

2.18.1.1 Electronic codebook mode (ECB)

The following steps have to be performed for a single AES calculation in Electronic Codebook Mode (ECB):

1. Load 16 bytes secret key into the internal AES register AESKEYREG
2. Load 16 bytes plain data into the internal AES register AESDATAREG
3. Start AES calculation
4. Retrieve enciphered data from AESDATAREG
5. If another calculation is desired with the same secret key, proceed with point 2

If consecutive calculations use the same secret key, it can be re-used without reloading.

2.18.1.2 Output feedback mode (OFB)

The following steps have to be performed for AES calculations in Output Feedback Mode (OFB):

1. Load 16 bytes secret key into the internal AES register AESKEYREG
2. Load 16 bytes initialization vector into the internal AES register AESDATAREG
3. Start AES calculation
4. Retrieve enciphered data from AESDATAREG and XOR it with plain text
5. Proceed with 3)

It is not necessary to reload AESDATAREG between several AES calculations as data stored in AESDATAREG at the end of one calculation is automatically used as input data for the next calculation.

2.18.2 Registers

2.18.2.1 AES data register AESDAT

This register provides the access to both the AESKEYREG and the AESDATAREG. It allows for reading these registers or for writing the registers with an initial value, dependent on the settings.

The AES data register provides byte and word access (Table 163). Any read access to AESDAT while an active AES calculation is ongoing yields an undefined result.

Table 163. Word and byte access to the AES data register AESDAT

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
AESDAT	AESDATH	AESDATL

Table 164. AES data register AESDAT (reset value xxxxh)

Bit	Symbol	Access	Value	Description
15 to 0	AESDATA[15:0]	R/W		AES data

2.18.2.2 AES control register AESCON

The AES calculation unit is controlled via the AES Control Register AESCON.

Table 165. AES control register AESCON (reset value 00h)

Bit	Symbol	Access	Value	Description
7	AESRUN	R/W		AES run
			0	Read: AES calculation finished Write: No effect
			1	Read: AES calculation in operation Write: Start AES calculation
6	AESRST	R0/W		AES reset
			0	No effect
			1	Reset
5	RFU	-/W0		Reserved for future use
4	AESACC	R/W		AES register access
			0	Select AESKEYREG, write only
			1	Select AESDATAREG, read and write
3 to 0	AESBC[3:0]	R/W		AES register byte counter
			0000	Addressed via AESDL: Byte 0 Addressed via AESD: Word 0
			0001	Addressed via AESDL: Byte 1 Addressed via AESD: Word 0
			0010	Addressed via AESDL: Byte 2 Addressed via AESD: Word 1
			0011	Addressed via AESDL: Byte 3 Addressed via AESD: Word 1
			0100	Addressed via AESDL: Byte 4 Addressed via AESD: Word 2
			0101	Addressed via AESDL: Byte 5 Addressed via AESD: Word 2

Bit	Symbol	Access	Value	Description
			0110	Addressed via AESDL: Byte 6 Addressed via AESD: Word 3
			0111	Addressed via AESDL: Byte 7 Addressed via AESD: Word 3
			1000	Addressed via AESDL: Byte 8 Addressed via AESD: Word 4
			1001	Addressed via AESDL: Byte 9 Addressed via AESD: Word 4
			1010	Addressed via AESDL: Byte 10 Addressed via AESD: Word 5
			1011	Addressed via AESDL: Byte 11 Addressed via AESD: Word 5
			1100	Addressed via AESDL: Byte 12 Addressed via AESD: Word 6
			1101	Addressed via AESDL: Byte 13 Addressed via AESD: Word 6
			1110	Addressed via AESDL: Byte 14 Addressed via AESD: Word 7
			1111	Addressed via AESDL: Byte 15 Addressed via AESD: Word 7

AESRUN, AES run

AESRUN is used to start the AES calculation and to monitor its execution status. The internal AES registers (AESKEYREG and AESDATAREG) shall be loaded prior to the start of calculation. The bit AESRUN stays 1 as long as the AES calculation continues. The bit is automatically cleared when the calculation is finished. Writing a zero to bit AESRUN does not have any effect.

Once AESRUN is set any write access to register AESDAT and AESCON is inhibited. The only exception is bit AESRST, which can be used to interrupt the current calculation. Any read access to AESDAT while an active AES calculation is ongoing yields an undefined result.

AESRST, AES reset

AESRST is intended to clear the internal AES registers AESKEYREG and AESDATAREG. This can be used to clear the content of the internal AES registers after a calculation in order to prevent that a program that is executed thereafter has any unintended access to secret information used before.

Setting bit AESRST while an AES calculation is ongoing causes an immediate interruption of the calculation. If bit AESRUN and AESRST are set at the same time, bit AESRST has priority and the AES calculation is not started.

AESACC, AES register access

AESACC selects which internal register is accessed through the special function register AESD and AESDL. Any read or write access to AESD operates directly on the internal AES registers.

The internal register AESKEYREG does not support read access, the secret key can only be written. AESDATAREG has full read and write access and supports read-modify-write operations.

Once the AES calculation has started any read access of bit AESACC yields '0'. After completion of the AES calculation AESACC is undefined.

AESBC[3:0], AES register byte counter

AESBC[3:0] controls which of the 16 bytes of the internal AES register is addressed by a read or write access through register AESDAT.

A byte access to AESDATL uses AESBC[3:0] to select a byte whereas a word access to AESDAT ignores bit AESBC[0] and uses AESBC[3:1] as a pointer to the respective word. Bit AESBC[0] is treated as zero in this case regardless of the current value. Hence, a word access at an odd byte address of the internal AES registers is not supported.

The AES register byte counter features an auto-increment after every read or write access to register AESDAT. A byte access causes an increment by 1 and a word access an increment by 2 (independent of AESBC is even or odd).

Once the AES calculation has started any read access of the bits AESACC and AESBC yields 0. After completion of the AES calculation these bits are undefined.

2.19 Random number generator

The device features a random number generator for seed generation of AES calculations.

The random number generator can be used as non-deterministic random number generator (NRNG) as well as pseudo random number generator (PRNG). All generated random numbers have a size of 16 bits.

The NRNG is also suitable to generate a seed for the PRNG for fast generation of subsequent random numbers.

The block diagram is depicted in Figure 58.

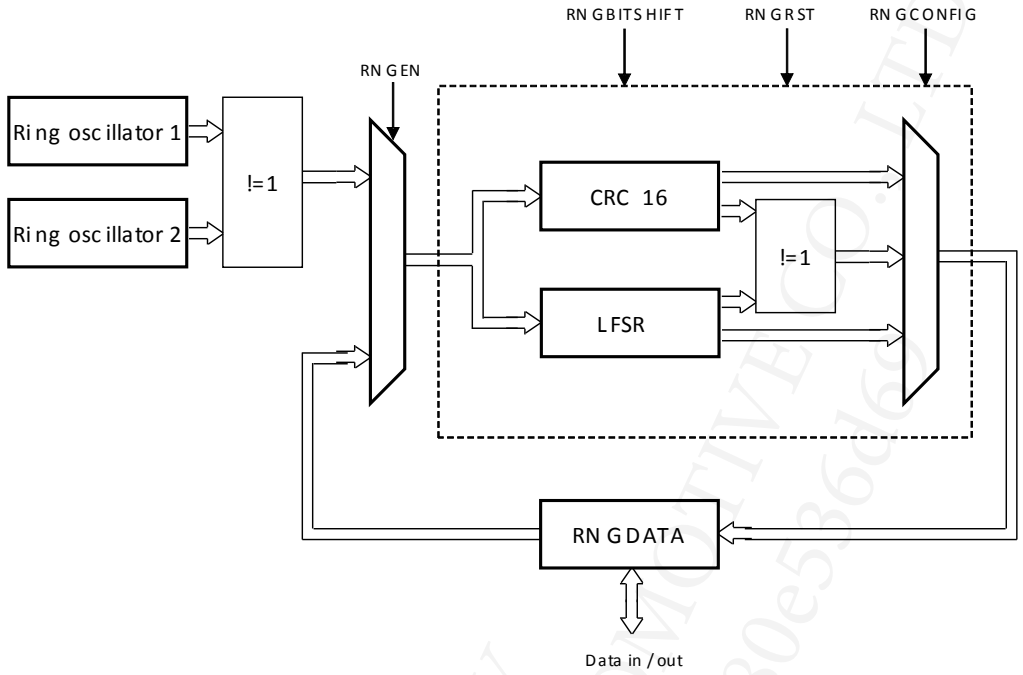


Figure 58. Random number generator block diagram

2.19.1 Ring oscillators

Two free running ring oscillators serve as entropy source. Performing an XOR operation on these two signals, a random bit stream is generated, from which a configured number of bits are sampled. These bits are shifted in a 16 bit cyclic redundancy check (CRC) register or in a 16 bit linear feedback shift register (LFSR), where they are post-processed.

2.19.2 Post-processing

The oscillating entropy signal coming from the ring oscillators is post-processed to increase the amount of random numbers that can be generated. Three post-processing approaches are available (selected via RNGCONFIG).

- 16 bit cyclic redundancy check register (CRC16)
- 16 bit linear feedback shift register (LFSR)
- both the CRC16 and the LFSR register (hybrid mode)

In the first two cases the 16 bit random number is read out directly from the registers, while in the last scenario the random number is generated by an XOR operation on the values of both registers.

2.19.2.1 Cyclic redundancy check register

The 16 bit cyclic redundancy check (CRC16) implements the polynomial

$x^{16} + x^{12} + x^5 + 1$

The register can be supplied with random bits from the ring oscillators or can be used as linear feedback shift register with length 2^{15}-1 in PRNG mode. Since the polynomial is not irreducible the CRC used as LFSR has not a period of maximum length.

Before the PRNG can be used the CRC16 register shall hold an initial value. The initial values 0000h and F80Fh have to be avoided since they cause the CRC16 to stuck at the corresponding value. After power-on reset the CRC16 holds the value AAAAh.

When the CRC16 is used as NRNG all initial values are allowed.

When the CRC16 is used as PRNG two different sets of random numbers can be generated dependent on the initial value. Both sets have a period of 2^{15}-1 and the two sets do not have any random numbers in common. Example initial values for the first set are all powers of 2 (2^1 … 2^{15}) and for the second set AAAAh.

2.19.2.2 Linear feedback shift register

The linear feedback shift register (LFSR) implements the polynomial

$$x^{16} + x^{14} + x^{13} + x^{11} + 1$$

The register can be supplied with random bits from the ring oscillators (RNGEN = '1') or can be used as linear feedback shift register with length 2^{16}-1 in PRNG mode (maximum length LFSR).

When used as PRNG the initial value 0000h has to be avoided since otherwise the LFSR cannot produce any other values. The application shall not use the setting RNGBITSHIFT = 01b (17 bit shift), otherwise the RNG cannot generate all 2^{16}-1 different random numbers.

When used for NRNG post-processing all initial values are allowed.

2.19.2.3 Hybrid mode

The hybrid mode performs an XOR operation on the outputs of the CRC16 and the LFSR and combines thus both methods described in the previous sections.

All restrictions mentioned for CRC16 and LSFR have to be considered also in hybrid mode.

When used as PRNG the period of the random numbers is $(2^{15}-1)*(2^{16}-1)$.

2.19.2.4 Random number generation

In order to generate a non-deterministic random number (NRNG), the following steps have to be executed:

1. Activate the ring oscillators (RNGEN = 1)
2. Wait $t_{RNG,Sett}$ until the ring oscillators have settled.
3. If desired write an initial value to the CRC16 and/or LSFR (optional step)
4. Start the RNG (RNGRUN = '1'). When the operation is finished a new 16 bit random number can be fetched from RNGDAT. The quality of the random number increases when starting the RNG several times. It is recommended to start the RNG nine times for generating a NRNG.
5. If no further random number is required, deactivate the ring oscillators (RNGEN = '0')

In order to generate a pseudo random number (PRNG), the following steps have to be executed:

1. Write a valid initial value to the CRC16 and/or LSFR. In case the initial value was generated with the NRNG the application has to check that the CRC16 or the LSFR does contain valid seed values. When the hybrid mode is selected this shall be checked for the CRC16 and LSFR separately.

2. Start the RNG (RNGRUN = '1'). When the operation is finished a new 16 bit random number can be fetched from RNGDAT.

The following operation modes are recommended:

- NRNG: Hybrid mode, 17 bit shifts
- PRNG: LSFR mode, 16 bit shifts, if little dependency between consecutive random numbers is required
- PRNG: LSFR mode, 1 bit shift, if dependency between consecutive numbers is of less importance (fastest operation mode)

2.19.3 Registers

2.19.3.1 RNG data register RNGDAT

This register provides access to both the CRC register and the LFSR register. It allows for reading 16 bit random numbers or for seeding the RNG with an initial value.

The random number generator data register RNGDAT provides byte and word access (Table 166).

Table 166. Word and byte access to the random number generator data register RNGDAT

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
RNGDAT	RNGDATH	RNGDATL

Table 167. Random number generator data register RNGDAT (reset value XXXXh)

Bit	Symbol	Access	Value	Description
15 to 0	RNGDATA[15:0]	R/W		Random number generator data

RNGDATA[15:0], Random number generator data

RNGDATA is read either from the CRC16 register or from the LFSR register, depending on the setting of RNGCONFIG. When writing seed data to RNGDATA, the value is assigned to either one or both the CRC16 register and the LFSR register, depending on the setting of RNGCONFIG. Reading and writing RNGDATA is only allowed when the random number generator is not running.

2.19.3.2 RNG control register RNGCON

The random number generator control register RNGCON is used to configure and operate the random number generator.

Table 168. Random number generator control register RNGCON (reset value 26h)

Bit	Symbol	Access	Value	Description
7	RNGRUN	R/W		Random number generator run
			0	Read: Random number generation finished Write: No effect
			1	Read: Random number generation in operation Write: Start random number generation
6 to 5	RNGBITSHIFT[1:0]	R/W		Number of bit shifts

Bit	Symbol	Access	Value	Description
			00	16
			01	17
			10	19
			11	1
4 to 3	RNGCONFIG[1:0]	R/W		Random number generator configuration
			00	Initialization mode
			01	Cyclic redundancy check (CRC16)
			10	Linear feedback shift register (LFSR)
			11	Hybrid (CRC16 xor LFSR)
2	RNGTRIMOSC	R/W		Oscillator trim setting
			0	Main setting
			1	Alternative setting
1	RNGEN	R/W		Random number generator enable
			0	PRNG mode Ring oscillators disabled RNG is running with PCLK
			1	NRNG mode Ring oscillators enabled RNG is running with REFCLK
0	RNGRST	R0/W		Random number generator reset
			0	No effect
			1	Reset

RNGRUN, Random number generator run

RNGRUN is used to start generating a new 16 bit random number. During calculations RNGRUN is set indicating that the RNG is busy. As long as RNGRUN is set, any write access to registers RNGDAT and RNGCON is inhibited. The only exception is bit RNG_RST, which can be used to stop a running operation.

RNGRUN is cleared automatically and the RNG interrupt flag IF_RNG is set when a new random number is available.

RNGCONFIG, Random number generator configuration

RNGCONFIG is used to select the type of RNG for generating random numbers. Additionally, RNGCONFIG is used to select the internal register(s) for read and write access via RNGDAT.

Setting the random number generator in initialization mode (RNGCONFIG = 00) and enabling the ring oscillators (RNGEN = 1) initializes the RNG automatically. During this initialization, the RNG starts nine times in hybrid mode for generating a non-deterministic random number (NRNG) with 17 bit shifts. The setting of RNGBITSHIFT[1:0] is ignored. The RNG oscillators keep activated (RNGEN = 1) after finishing the automatic initialization.

Each time the device wakes-up the BOOT routine starts the automatic initialization to generate a seed. The seed becomes valid after RNGRUN is set to 0. The random number generator can be reset after booting, thus refusing the seed calculation.

RNGBITSHIFT[1:0], Number of bit shifts

RNGBITSHIFT selects the number of bit shifts that are applied to generate a new 16 bit random number. The setting is used in both NRNG and PRNG mode.

RNGTRIMOSC, Oscillator trim settings

Two oscillator trim settings are provided, which give two different pairs of RNG oscillator frequencies.

RNGEN, Random number generator enable

RNGEN is used to enable the ring oscillators and to switch the RNG from PRNG to NRNG mode.

In case RNGEN is not set, the ring oscillators are turned off and the RNG is used as PRNG, generating new 16 bit random numbers by shifting the value of the registers according to the number of shifts configured in the control register.

RNGRST, random number generator reset

RNGRST resets the CRC16 register and the LFSR register, independent of the RNGCONFIG settings.

Setting bit RNGRST while the RNG operation is ongoing causes an immediate interruption. If bit RNGRUN and RNGRST are set at the same time, bit RNGRST has priority and the RNG is not started.

2.20 Registers for mathematical/logical operations

2.20.1 Bit swap register BITSWAP

The bit swap register BITSWAP is provided to change the bit order of a byte. A byte is written to register BITSWAP first. After writing, it is swapped. If it is read again from the same location, the bit order is reversed.

The application shall not use read-modify-write instructions with this register.

Table 169. Bit swap register BITSWAP (reset value xxh)

Bit	Access	Bit order write access	Bit order read access
7	R/W	BITSWP[7]	BITSWP[0]
6	R/W	BITSWP[6]	BITSWP[1]
5	R/W	BITSWP[5]	BITSWP[2]
4	R/W	BITSWP[4]	BITSWP[3]
3	R/W	BITSWP[3]	BITSWP[4]
2	R/W	BITSWP[2]	BITSWP[5]
1	R/W	BITSWP[1]	BITSWP[6]
0	R/W	BITSWP[0]	BITSWP[7]

2.20.2 Bit count register (parity generator) BITCNT

The bit count register BITCNT counts the number of bits being '1' in an input byte or input word.

The bit count register BITCNT provides byte and word access. In case of byte access, the unused input byte is set to 0. The application shall not use read-modify-write instructions with this register.

Table 170. Word and byte access to bit count register BITCNT

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
BITCNT	BITCNTH	BITCNTL

If a byte/word is written to BITCNT it is evaluated immediately and the number of bits with content '1' can be read back from BITCNTL, independent of whether BITCNT, BITCNTH or BITCNTL was used as data input.

Table 171. Bit count register BITCNT (reset value 0000_0000_000x_xxxxb)

Bit	Symbol	Access	Value	Description
15 to 5	BITCNT[15:5]	R0/W		Write: Input value, bits 15 to 5 Read: Always 0
4 to 0	BITCNT[4:0]	R/W		Write: Input value, bits 4 to 0 Read: Bit count value

The 11 most significant bits BITCNT[15:5] always read '0', while BITCNT[4] always reads '0' if a byte calculation was performed. Therefore, the application does not need to mask the read value before further processing.

The list below provides examples for tasks that can be accomplished with this register:

- Determine the parity of a byte/word
  - If the bit BITCNT[0] reads a '1', the input byte/word has an odd number of '1's.
- Check a data byte/word versus a known bit mask
  - XOR the data byte/word with the mask and write the result into register BITCNT. The result is the number of bits unequal to the expected value or bit mask.
- Determine whether a byte is fully set
  - The bit BITCNT[3] is only '1', if the value of the provided input byte is FFh.
- Determine whether a word is fully set
  - The bit BITCNT[4] is only '1', if the value of the provided input byte is FFFFh.

2.20.3 Generic CRC register

The NCF215A / NCF215B supports a generic, fully configurable CRC register with the following features:

- Configurable CRC length from 1 to 16 bits (CRC1 to CRC16)
- Configurable CRC polynomial
- Configurable CRC start value
- Configurable input data bit width between 1 and 8 bits
- Support for LSBit/MSBit first and right/left aligned input data

The CRC register is intended for CRC generation and CRC checking tasks. The CRC calculation is executed in one instruction cycle regardless of the selected input data bit width.

The CRC register consists of a 16 bit CRC data register GCRCDAT and a configurable CRC polynomial, which can be set via register GCRCPOLY. A principle of the CRC operation is depicted in Figure 59.

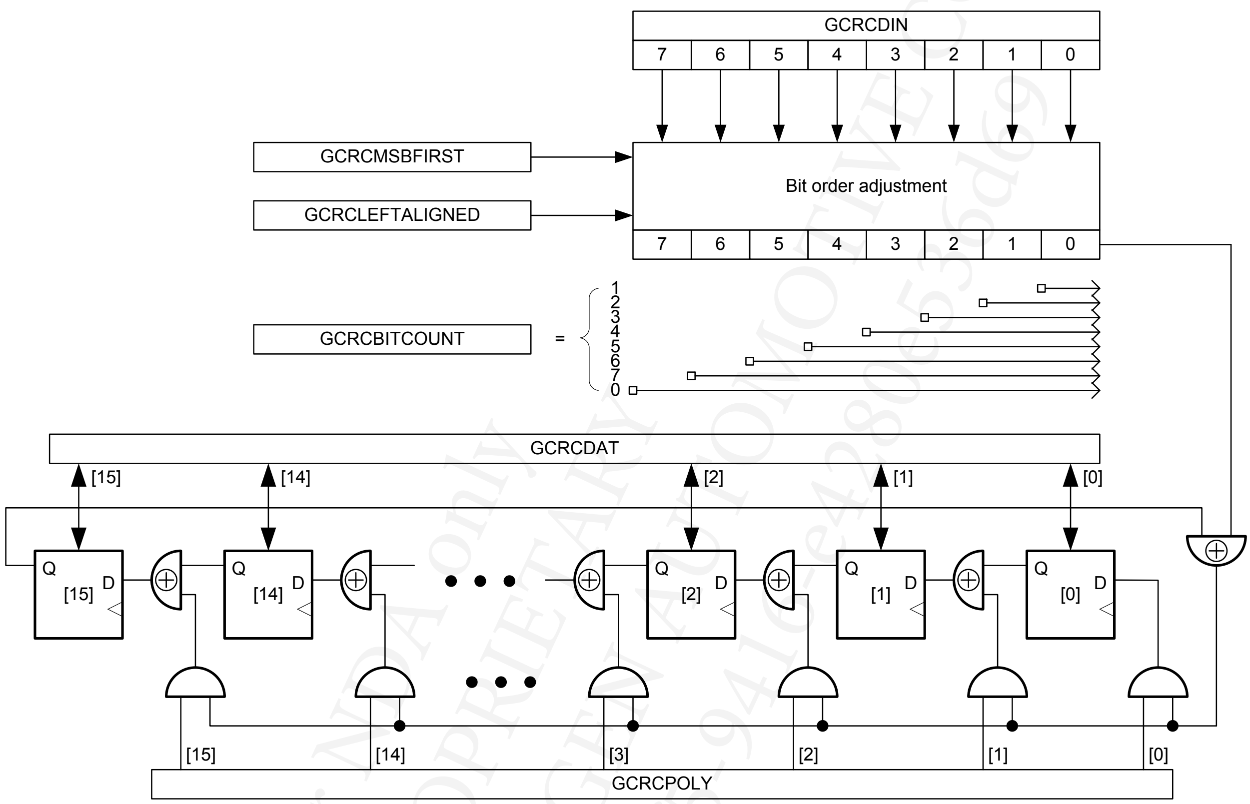


Figure 59. Principle operation of the generic CRC register, configuration of the CRC polynomial

The length of the CRC polynomial is configurable from CRC1 to CRC16. If a CRC with a length of less than 16 bits is desired, the polynomial and data in GCRCDAT must always be left aligned. The unused lower bits must be set to 0 in GCRCPOLY. Moreover, the initial value of GCRCDAT must also be 0 for the unused lower bits to avoid that any unwanted data is shifted from the unused part of GCRCDAT into the wanted CRC value.

The CRC register supports parallel calculation of input data with 1 to 8 bits. Data must be written to register GCRCDIN. Every write access to GCRCDIN starts the CRC calculation automatically and updates register GCRCDAT.

The interpretation of the input data written to GCRCDIN can be selected as LSBit or MSBit first. If less than 8 input data bits are selected via register GCRCBITCNT, only the specified number of bits is considered for the calculation. It is selectable whether the leftmost or the rightmost bits of GCRCDIN are processed in this case. This selection is independent of the logical representation LSBit or MSBit first. The bits are shifted automatically to the correct position.

2.20.3.1 Generic CRC register description

Table 172. Word and byte access to the generic CRC registers

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
GCRCDAT	GCRCDATH	GCRCDATL
GCRCPOLY	GCRCPOLYH	GCRCPOLYL

Table 173. Generic CRC data register GCRCDAT (reset value 0000h)

Bit	Symbol	Access	Value	Description
15 to 0	GCRCDATA[15:0]	R/W		Generic CRC data register

Table 174. Generic CRC polynomial register GCRCPOLY (reset value 0000h)

Bit	Symbol	Access	Value	Description
15 to 0	GCRCPOLY[15:0]	R/W		Generic CRC polynomial register

Table 175. Generic CRC input data register GCRCDIN (reset value xxh)

Bit	Symbol	Access	Value	Description
7 to 0	GCRCDIN[7:0]	R0/W		Generic CRC input data register

Table 176. Generic CRC control register GCRCCON0 (reset value 00h)

Bit	Symbol	Access	Value	Description
7 to 6	RFU	-/W0		Reserved for future use
5	GCRCLEFTALIGNED	R/W		Select whether the leftmost or righmost bits in GCRCDIN are processed in case GCRCBITCNT is set to a value unequal to 0 (see Table 177 for an example). This setting has no effect for GCRCBITCNT = 0.
			0	Data in GCRCDIN is interpreted right aligned; i.e. the rightmost number of bits defined by GCRCBITCNT is processed
			1	Data in GCRCDIN is interpreted left aligned; i.e. the leftmost number of bits defined by GCRCBITCNT is processed
4	GCRCMSBFIRST	R/W		Select the shift direction of the data in GCRCDIN (see Table 177 for an example)
			0	Data in GCRCDIN is processed LSBit first starting with the rightmost significant bit
			1	Data in GCRCDIN is processed MSBit first starting with the leftmost significant bit
3	RFU	-/W0		Reserved for future use
2 to 0	GCRCBITCNT[2:0]	R/W		Number of bits in GCRCDIN that are processed per write access to GCRCDIN. The order of processing is determined by the settings GCRCMSBFIRST and GCRCLEFTALIGNED.
			0d	8 bits

Bit	Symbol	Access	Value	Description
			1d	1 bit
			2d	2 bits
			3d	3 bits
			4d	4 bits
			5d	5 bits
			6d	6 bits
			7d	7 bits

Table 177. Example for selection of bit order for CRC calculation

GCRCMSBFIRST	GCRCLEFTALIGNED	Processing order of bits in GCRCDIN for GCRCBITCNT = 3 (leftmost bit is processed first)
0	0	$0 \rightarrow 1 \rightarrow 2$
0	1	$5 \rightarrow 6 \rightarrow 7$
1	0	$2 \rightarrow 1 \rightarrow 0$
1	1	$7 \rightarrow 6 \rightarrow 5$

2.20.4 CRC8 register

The NCF215A / NCF215B supports an 8 bit CRC generator for backward compatibility with WFS-5d transponder applications and user defined RKE frames. The generator is based on the polynomial $x^8 + x^2 + x + 1$ and it processes a complete input data byte in one instruction cycle.

The CRC value is stored in a CRC data register. The CRC data register can be initialized and read by directly accessing the data register CRCDAT.

An update of the CRC data register with new data according to the CRC polynomial takes place by writing to the data input register CRC8DIN. The CRC calculation is performed byte-wise. The calculation is equivalent to the bit serial calculation using the CRC8DIN data in MSB to LSB bit order.

2.20.4.1 CRC data register CRCDAT

CRCDAT stores the CRC value and can be read or written for CRC initialization.

According to the HT-Pro2 protocol, CRCDAT shall be loaded with the initial value 00h before data is exchanged.

Table 178. CRC data register CRCDAT (reset value 00h)

Bit	Symbol	Access	Value	Description
7 to 0	CRCDATA[7:0]	R/W		CRC result register

2.20.4.2 CRC8 data input register CRC8DIN

CRC8DIN is provided to add data to the CRC calculation. Any write access to CRC8DIN updates CRCDAT with the newly calculated CRC value considering CRC8DIN according to the 8 bit CRC polynomial.

Table 179. CRC8 data input register CRC8DIN (reset value xxh)

Bit	Symbol	Access	Value	Description
7 to 0	CRC8DIN[7:0]	-/W		CRC 8 data input value

2.21 Motion sensor interface

The device provides the capability to operate with an external MEMS type motion sensor (e.g. FXLS8962AF) or an external mechanical motion sensor component (rolling ball movement sensor) via the dedicated GPIO pin P21_MD. The main anticipated use of this feature is to deactivate the LF active interface if the key has not been moved for a specific period of time. The primary benefits of this feature are:

- Reduction in standby current when the key is known to be inactive, leading to increased battery life and/or smaller batteries
- Increased resistance against relay station attacks

2.21.1 Operation with a MEMS sensor

The motion sensor interface is optimized for operation with NXP's MEMS sensor FXLS8962AF. The MEMS sensor can be connected with the one-wire interface or, if wanted, with an additional SPI interface to support extended configuration possibilities of the MEMS sensor.

The motion sensor interface supports the following functions in conjunction with the MEMS sensor:

- Autonomous operation in the VBATREG supply domain
- Detection of interrupt pulses from the MEMS sensor at pin P21_MD
- Automatic pulse length evaluation to distinguish between motion detect and boot pulses
- Configurable length of motion absent detection
- Configurable device wake-up and interrupt control for motion absence detection and boot pulse detection

After motion absence detection, the motion sensor interface can be deactivated to save power. A new motion detection pulse from the MEMS sensor is then handled via the standard port wake-up function of P21_MD.

2.21.2 Operation with a mechanical sensor

It is assumed that the external mechanical motion sensor behaves like a digital switch and the rest position may be either open or closed.

The motion sensor interface supports the following functions in conjunction with the mechanical sensor:

- Autonomous operation in the VBATREG supply domain
- Internal switchable pull-up resistor and pull-down resistor at P21_MD
- Optional operation with an external pull-up resistor
- Detection of rising and falling edges on P21_MD
- Configurable length of motion absent detection (i.e. no edge detected at P21_MD)
- Configurable device wake-up and interrupt control for motion detection (Motion event) and motion absence detection (No-motion event)

2.21.3 Registers

The Motion Sensor Interface is controlled and monitored by 4 SFRs powered in the VBATREG domain as described in the following section.

2.21.3.1 MSI Timer Control Register, MSICON0

This register controls the Idle Timer Counter limit value and the clearing of this counter.

Table 180. MSI Timer Control Register, MSICON0 (reset value 1Eh)

Bit	Symbol	Access	Value	Description
7	RFU	-/W0		Reserved for future use
6	MSI_TCLR	R0/W		Idle timer restart request one-shot. Writing a 1 resets the idle timer. Always read as 0
			0	No Action
			1	Reset the Idle Timer
5 to 0	MSI_TLIM[5:0]	R/W		Idle Timer Overflow Limit - The un-interrupted length of time (in units of T_{MSI_CNT}, see MSI_RANGE in Table 184) for which there must be no motion detected by the sensor for the counter to flag that motion has ceased.
			00_0000	Setting not permitted, do not use
			00_0001 to 11_1111	No motion timeout = MSI_TLIM × T_{MSI_CNT}

2.21.3.2 MSI Enable Control Register, MSICON1

This register controls the enable for the Motion Sensor Interface module, mode of operation (Motion Sensor or Auxiliary Timer), and Wake-up and Interrupt enables for the "Motion Detected" and "Motion Ceased" events.

Table 181. MSI Enable Control Register, MSICON1 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	MSI_EN	R/W		Motion sensor interface / auxiliary interval timer enable.
			0	Module Disabled
			1	Module Enabled
6	MSI_MODE	R/W		Motion sensor interface / auxiliary interval timer mode selection
			0	Motion sensor interface mode - monitor P21_MD.
			1	Auxiliary interval timer mode - ignore P21_MD.
5 to 4	RFU	-/W0		Reserved for future use
3	MSI_MOT_WUP_EN	R/W		"Motion detected" wake-up enable. This setting is only effective, if MSI_MOT_INT_EN = 1. If MSI_MOT_INT_EN = 0, this wake-up is suppressed.
			0	Wake-up disabled for "Motion Detected" event
			1	Wake-up enabled for "Motion Detected" event

Bit	Symbol	Access	Value	Description
2	MSI_OVF_WUP_EN	R/W		"Motion ceased" wake-up enable. This setting is only effective, if MSI_OVF_INT_EN = 1. If MSI_OVF_INT_EN = 0, this wake-up is suppressed.
			0	Wake-up disabled for "Motion Ceased" event
			1	Wake-up enabled for "Motion Ceased" event
1	MSI_MOT_INT_EN	R/W		Motion detected interrupt enable.
			0	Interrupt disabled for "Motion Detected" event
			1	Interrupt enabled for "Motion Detected" event
0	MSI_OVF_INT_EN	R/W		Motion ceased interrupt enable.
			0	Interrupt disabled for "Motion Ceased" event
			1	Interrupt enabled for "Motion Ceased" event

2.21.3.3 MSI Idle Timer Count Register, MSISTAT0

Table 182. MSI Idle Timer Count Register, MSISTAT0 (reset value 00h)

Bit	Symbol	Access	Value	Description
7 to 6	RFU	-/W0		Reserved for future use
5 to 0	MSI_TREG[5:0]	R/-		Idle timer value

MSI_TREG[5:0], Idle timer value

The MSI_TREG[5:0] holds the read-only binary value indicating the time since timer (re)start or last motion event in multiples of T_{MSI_CNT}. MSI_TREG[5:0] is clocked with the 32 kHz crystal oscillator (XO32KCLK) and it is not buffered or synchronized to the CPU clock. While accessing MSI_TREG[5:0] by the CPU, it has to be ensured by multiple reading that the register content is stable, otherwise, invalid data may be read.

2.21.3.4 MSI Flag and Interrupt Register, MSISTAT1

This register enables the CPU to read the status of the Motion Interrupt, Overflow Interrupt and Counter Overflow flags.

Table 183. MSI Flag and Interrupt Register, MSISTAT1 (reset value 00h)

Bit	Symbol	Access	Value	Description
7 to 5	RFU	-/W0		Reserved for future use
4	MSI_MEMSBOOT_OVF	R/-		MEMS boot pulse timer overflow flag
			0	No overflow while evaluating pulse length, or if a valid motion or boot pulse detected
			1	Maximum boot pulse length of 12.5 ms exceeded
3	MSI_MEMSBOOT_INT	R/W1->0		MEMS boot interrupt flag
			0	No interrupt; Also, when interrupt disabled
			1	MEMS boot interrupt fired
2	MSI_OVF	R/-		Idle Timer Overflow status flag
			0	The Idle timer counter has not reached its maximum value

Bit	Symbol	Access	Value	Description
			1	The idle timer counter has reached its maximum value
1	MSI_MOT_INT	R/W1->0		Motion Detected Interrupt status flag
			0	Motion has not been detected since last reset
			1	Motion has been detected since last reset
0	MSI_OVF_INT	R/W1->0		Idle Timer Overflow Interrupt status flag
			0	The Idle timer counter has not reached its maximum value since last reset
			1	The Idle timer counter has reached its maximum value since last reset

MSI_MEMSBOOT_OVF, Pulse validation timer overflow

A hardware pulse length detection validates the length of low pulses on P21_MD driven by MEMS.Valid motion pulse or a valid MEMS boot pulse are detected by means of three thresholds. When the highest threshold of 12.5ms is crossed by the timer while P21_MD is kept "low", this case would be associated to a "too long boot pulse". In this case, MSI will not generate a wake-up nor an interrupt will be sourced. The timer is stalled when the threshold cross detected and flag set. The pulse validating timer is reset and the MSI_MEMSBOOT_OVF flag is cleared by the start of the next MEMS sensor pulse (i.e. the next falling edge of the MEMS sensor input, P21_MD.)

MSI_MEMSBOOT_INT, Pulse validation timer interrupt

Two MEMS interrupt sources share the same interrupt request and the interrupt flag IF_MSI. To distinguish between a motion pulse or a boot pulse that sourced the interrupt, the MSI_MEMSBOOT_INT flag is provided. This flag is set and the interrupt is raised as soon as the low time of a pulse reaches the minimum boot pulse length of 7.5 ms. This is done to give application maximum time to respond to the interrupt. In this situation and following configuration bits in MSICON2, the MSI will generate a wake-up or interrupt signal for the CPU. The MSI_MEMSBOOT_INT interrupt flag is cleared when MSI_MEMSBOOT_INT value 1 is written by application.

MSI_OVF, Idle Timer Overflow status flag

MSI_OVF is active high whenever the Idle timer is in its terminal count state - i.e. whenever count = TLIM.

MSI_MOT_INT, Motion Detected Interrupt status flag

MSI_MOT_INT is active high when motion has been detected since the interrupt was last reset. Writing a "1" to this bit resets the interrupt.

MSI_OVF_INT, Idle Timer Overflow Interrupt status flag

MSI_OVF is active high whenever the Idle timer counter has reached its maximum value since the interrupt was last reset. Writing a "1" to this bit resets the interrupt.

2.21.3.5 MSI MEMS Control Register, MSICON2

The MSICON2 register controls the enable for the MEMS functions of the Motion Sensor Interface module. More precisely, the MEMS pulse validation enable bit as well as the

configuration bits for spike pulses tolerance and wake-up and interrupt enable at a boot pulse detected are all maintained in this register.

Furthermore, this register selects the idle timer clock period T_{MSI_CNT}.

Table 184. MSI MEMS Control Register, MSICON2 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	MSI_MEMS_MODE	R/W		MEMS pulse validation enable
			0	Pulse length validation disabled, every edge resets the timer
			1	Pulse length validation enabled
6 to 4	MSI_RANGE	R/W		Selection of idle timer clock period T_{MSI_CNT}
			000	T_{MSI_CNT} = 2 × 32768 / f_{XO32K} (typ. 2 s)
			001	T_{MSI_CNT} = 8 × 32768 / f_{XO32K} (typ. 8 s)
			010	T_{MSI_CNT} = 32 × 32768 / f_{XO32K} (typ. 32 s)
			011	T_{MSI_CNT} = 128 × 32768 / f_{XO32K} (typ. 128 s)
			100	T_{MSI_CNT} = 512 × 32768 / f_{XO32K} (typ. 512 s)
			101	T_{MSI_CNT} = 2048 × 32768 / f_{XO32K} (typ. 2048 s)
			110	Reserved for future use
			111	Reserved for future use
3	RFU	-/W0		Reserved for future use
2	MSI_SPIKEREJECT	R/W		Enable rejecting short pulses, shorter than 2.5 ms
			0	Disabled, pulse timer reset after each edge
			1	Enabled, pulse timer reset by low pulses longer than 2.5 ms
1	MSI_MEMSBOOT_WUP_EN	R/W		Enable wake-up when valid boot pulse detected. This setting is only effective, if MSI_MEMSBOOT_INT_EN = 1. If MSI_MEMSBOOT_INT_EN = 0, this wake-up is suppressed.
			0	No effects, wake-up disabled
			1	Wake-up enabled when a low pulse longer than 7.5 ms detected
0	MSI_MEMSBOOT_INT_EN	R/W		Enable interrupt when valid boot pulse detected
			0	No effects, interrupt disabled
			1	Interrupt enabled when a low pulse longer than 7.5 ms detected

MSI_MEMS_MODE, Pulse validation enable

The hardware pulse validation timer is reset at any edge on P21_MD if MSI_MEMS_MODE is set to 0. When MSI_MEMS_MODE is set to 1, the timer starts validating low pulses on P21_MD against critical thresholds that validate pulses as "short" spikes, "motion" pulses, "boot" pulses or "too long" pulses. With the same bit set to 0, pulses validation is disabled, but not the timer itself.

MSI_SPIKEREJECT, Enable tolerance of short pulses

The hardware pulse length timer starts counting when MSI_MEMS_MODE = 1 at a falling edge on P21_MD is sensed. P21_MD is sampled at nominal 1ms interval rate

that allows classification of the observed "low" pulses as "short", "motion", "boot" or "too long". When MSI_SPIKEREJECT is set 1, all short pulse indications are ignored. When MSI_SPIKEREJECT is set 0, the "short" pulses are treated the same as the "motion" pulses.

MSI_MEMSBOOT_WUP_EN, Wake-up enable bit at boot pulse

When the P21_MD line is held "low" over the lower threshold of 2.5 ms, any rising edge on P21_MD appearing before the timer reaches next threshold of 7.5 ms will be interpreted as a "motion" pulse. The MSI will nevertheless generate a wake-up signal for the device's CPU core. This wake up signal will be maintained high until cleared by the CPU writing a "1" to MSI_MOT_INT.

When the P21_MD line is held "low" over the higher threshold of 7.5 ms, any rising edge on P21_MD that appears before the timer reaches next threshold of 12.5ms will be interpreted as a "boot" pulse. When "boot" pulse confirmed, the MSI will generate a wake-up signal for CPU if MSI_MEMSBOOT_WUP_EN is set to 1, otherwise, if MSI_MEMSBOOT_WUP_EN is set to 0, there will be no wake-up generated.

MSI_MEMSBOOT_INT_EN, Interrupt enable bit at boot pulse

When "boot" pulse confirmed, the MSI will generate an interrupt signal for CPU if MSI_MEMSBOOT_INT_EN is set to 1. Flag MSI_MEMSBOOT_INT will be set 1 as well. Otherwise, if MSI_MEMSBOOT_INT_EN is set to 0, there will be no interrupt nor flag set.

As described for the status bit, any low pulse on P21_MD longer than the highest threshold of 12.5ms counted by the pulse timer would set MSI_MEMSBOOT_OVF flag to 1.

2.22 User data registers

The NCF215A / NCF215B provides 16 user registers, 8 of which are supplied by the unregulated battery supply VBAT and the other 8 by the regulated battery supply VBATREG. Each user register has a length of one byte.

These user registers keep their content during RISC power-down mode and can be accessed for customer applications.

2.22.1 Register description

Table 185. User registers USRBATx (reset values 00h)

Bit	Symbol	Access	Value	Description
7 to 0	USRB0[7:0]	R/W		User data register 0 in unregulated battery domain
7 to 0	USRB1[7:0]	R/W		User data register 1 in unregulated battery domain
7 to 0	USRB2[7:0]	R/W		User data register 2 in unregulated battery domain
7 to 0	USRB3[7:0]	R/W		User data register 3 in unregulated battery domain
7 to 0	USRB4[7:0]	R/W		User data register 4 in unregulated battery domain
7 to 0	USRB5[7:0]	R/W		User data register 5 in unregulated battery domain
7 to 0	USRB6[7:0]	R/W		User data register 6 in unregulated battery domain
7 to 0	USRB7[7:0]	R/W		User data register 7 in unregulated battery domain

Table 186. User registers USRBATRGLx (reset values xxh)

Bit	Symbol	Access	Value	Description
7 to 0	USRBRGL0[7:0]	R/W		User data register 0 in regulated battery domain
7 to 0	USRBRGL1[7:0]	R/W		User data register 1 in regulated battery domain
7 to 0	USRBRGL2[7:0]	R/W		User data register 2 in regulated battery domain
7 to 0	USRBRGL3[7:0]	R/W		User data register 3 in regulated battery domain
7 to 0	USRBRGL4[7:0]	R/W		User data register 4 in regulated battery domain
7 to 0	USRBRGL5[7:0]	R/W		User data register 5 in regulated battery domain
7 to 0	USRBRGL6[7:0]	R/W		User data register 6 in regulated battery domain
7 to 0	USRBRGL7[7:0]	R/W		User data register 7 in regulated battery domain

2.23 Device modes

The NCF215A / NCF215B features the Device Modes

- VIRGIN
- INIT
- PROTECTED
- TAMPERED

The Device Modes affect the overall device behavior, the Monitor and Download Interface operation and the user ability to access the EEPROM and EROM. A Device Mode is controlled by a set of configuration bytes, which are located in the EEPROM.

The configuration bytes may not be altered by the user directly, instead the corresponding Monitor and Download Interface command has to be used.

2.23.1 VIRGIN

After manufacturing, the device operates in VIRGIN mode, enabling extended device test and device configuration. Finally, NXP forces the device into INIT mode and the VIRGIN mode is irreversibly locked in order to ensure it cannot be activated again.

2.23.2 INIT

When the device is supplied from NXP, it is configured in INIT mode by default.

The INIT mode shall be used during software development only. The Monitor and Download Interface is fully operational, enabling the customer to initialize the EEPROM and EROM as desired for the application.

To protect the EEPROM and EROM from readout and to disable the debug features, the device shall be forced into PROTECTED mode.

Leaving the device in INIT mode may cause the device to execute a software break, in case a stop command is detected at pin MSDA (for details see [1]). Such a command would terminate execution of the application program and would call the built-in debug program. In this case, execution of the application program is interrupted until a proper debug command is issued or a device reset is applied.

2.23.3 PROTECTED

In the moment the device is set into PROTECTED mode, the EEPROM and EROM are protected against altering and readout via the Monitor and Download Interface, and the debug features are disabled. The PROTECTED mode has to be used during system testing and in the final application.

The device may be forced into INIT mode again by issuing a corresponding command via the Monitor and Download Interface. This command sets the EEPROM and the EROM to a predefined state before the INIT mode is resumed. Hence, all application related EEPROM data and the EROM based application program are discarded. In case this sequence does not complete successfully, the device enters TAMPERED mode.

2.23.4 TAMPERED

The TAMPERED mode is entered temporarily during the sequence that forces the device from PROTECTED mode back into INIT mode. If this sequence does not complete successfully, the TAMPERED mode is entered.

The device may be forced into INIT mode by again issuing a corresponding command via the Monitor and Download Interface. This command sets the EEPROM and the EROM to a predefined state first, before the INIT mode is resumed. Hence, all application related EEPROM data and the EROM based application program are discarded. In case this sequence does not complete successfully, the device remains in TAMPERED mode until a new attempt is made.

2.23.5 Device identification

Device supports special function register IDENT for easy identification of device's family type.

2.23.5.1 IDENT register

This register contains the identifier value.

Table 187. Word and byte access to register IDENT

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
IDENT	IDENTH	IDENTL

Table 188. IDENT value register (reset value 8107h)

Bit	Symbol	Access	Value	Description
15 to 8	IDENTH[7:0]	R/-	81h	Device identifier, high byte
7 to 0	IDENTL[7:0]	R/-	07h	Device identifier, low byte

2.24 System routines

2.24.1 Boot routine

The ROM based boot routine (see Figure 60) is called immediately after a device reset. A device reset can be forced either by a Port Wake-Up condition or a LF Field Reset or can be interrogated by the application program.

The boot routine executes a sequence of instructions to evaluate the device mode and configures the device, e.g. determines the supply condition, evaluates device protection flags, calls transponder emulation modes according to the EEPROM configuration and passes control to the application code accordingly.

The boot routine has to process information about the presence of LF field and battery supply. Further, the boot routine evaluates wake-up events initiated by pressed buttons or the interval timer.

The boot routine checks the setting for LFFLDDIS and handles the bit IE_LFNMI. The NMI is always handled in the application.

In case the field supply is available, but no LF field detect signal is active (weak supply field), a part of the boot routine is executed again because the source of the wake-up event cannot be determined. If the LF field supply is available but operation with corresponding field supply is disabled in the settings (LFFLDDIS), the boot routine polls for new wake-up events.

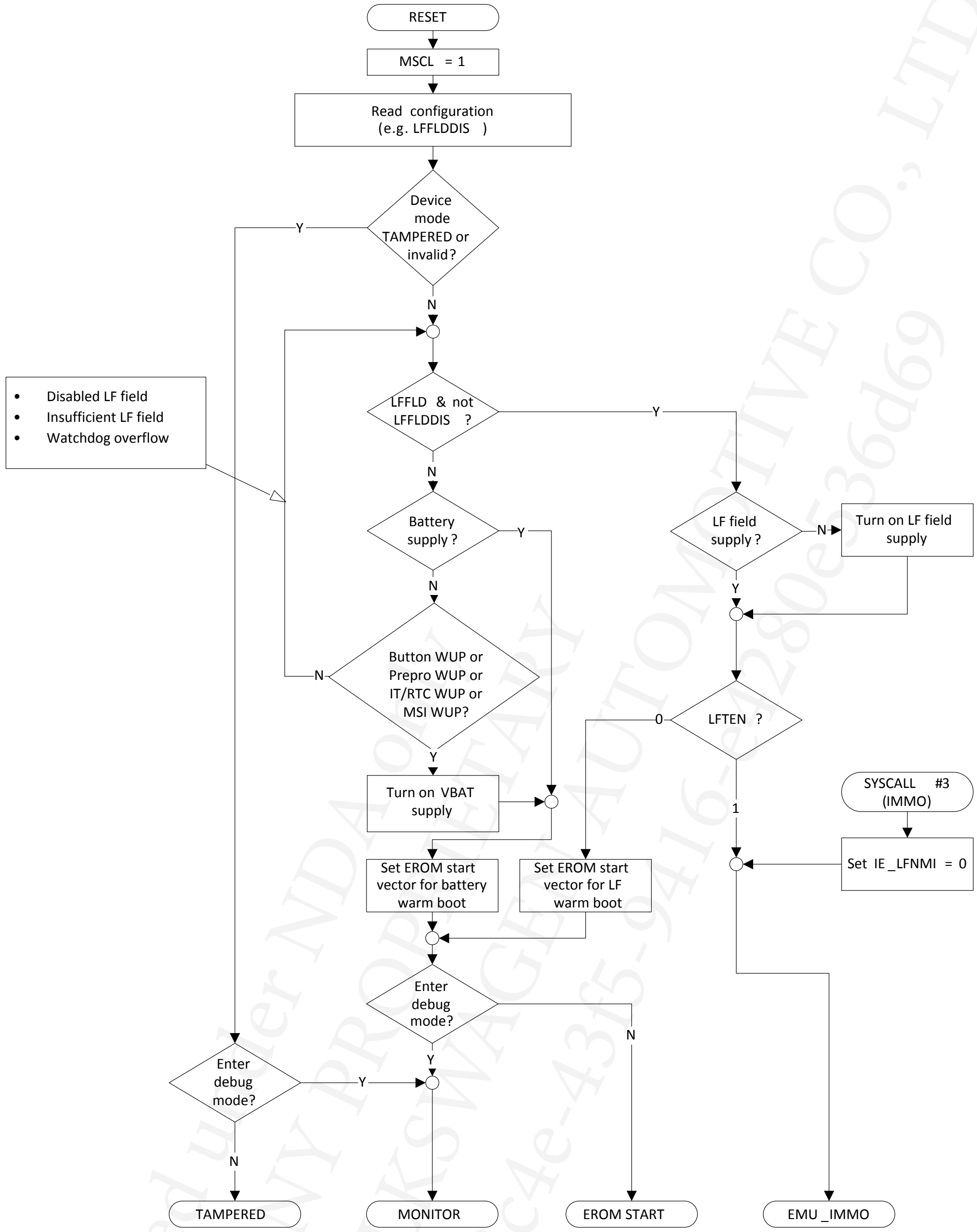


Figure 60. Boot routine flow chart

2.24.2 Transponder emulation

The NCF215A / NCF215B features a set of functions to emulate the WFS-5d transponder protocol. The transponder emulation is called directly from the boot routine or it can be called from the application program with a system call (SYS instruction, [2]).

2.24.3 Monitor and download interface

The in-circuit Monitor and Download Interface is intended for non-intrusive debugging during application program development. The interface allows manipulating the embedded peripherals and provides means to initialize the EEPROM and EROM. It is implemented as two-wire serial interface using the dedicated pins MSDA and MSCL.

The Monitor and Download Interface contains a 16 Bit Real Time Monitor containing Watches. Besides several HW/SW Break Points and single step operation, the interface contains an HW accelerator and allows autonomous operation.

The majority of the features provided by the Monitor and Download Interface are available only, if the device is set into INIT mode, which is the factory default setting. When performing system tests and field trials, the device shall be set to PROTECTED mode. Latter one locks the EEPROM and EROM content, protecting it against alteration and read out, as well as disables the debug features. The device may be forced back into INIT mode by a dedicated monitor command, which will set the EEPROM and EROM to a predefined state.

A detailed description about the operation and the command set of the Monitor and Download interface is given in [1].

3 Glossary

AC

Alternating Current

ADC

Analogue to Digital Converter

AES

Advanced Encryption Standard

AGC

Automatic Gain Control

ASK

Amplitude Shift Keying

BPLM

Binary Pulse Length Modulation

CDM

Charged Device Model

CDP encoding

Conditional DiPhase encoding, also called differential Manchester encoding. It is a line code in which data and clock signals are combined to form a single 2-level self-synchronizing data stream. It is a differential encoding, using the presence or absence of transitions to indicate logical values.

CPU

Central Processing Unit

CRC

Cyclic Redundancy Check

CW

Continuous Wave

DC

Direct Current

DNL

Differential NonLinearity

EEPROM

Electrically Erasable Programmable Read-Only Memory

EMC

ElectroMagnetic Compatibility

EROM

Execution Read-Only Memory (based on EEPROM technology)

ESD

ElectroStatic Discharge

FSM

Finite State Machine

HBM

Human Body Model

INL

Integral NonLinearity

ISM

Industrial, Scientific and Medical

IQ

In-phase/Quadrature phase

LDO

Low Drop-Out regulator

LED

Light Emitting Diode

LF

Low Frequency

LSB

Least Significant Bit

MEMS

Micro-Electro-Mechanical System

MMF

Manchester Matched Filter

MMU

Memory Management Unit

MSB

Most Significant Bit

NC

Not Connected

NRNG

Non-deterministic Random Number Generator

NRZ encoding

Non-Return to Zero encoding

OOK

On-Off Keying

PKE

Passive Keyless Entry

PLL

Phase Locked Loop

POR

Power-On-Reset

POK

Power OK

PRC OSC

Precision RC OSCillator

PRNG

Pseudo-Random Number Generator

RDT

Reserved for Device Test

RF

Radio Frequency

RFU

Reserved for Future Use

RISC

Reduced Instruction Set Computer

RKE

Remote Keyless Entry

ROM

Read-Only Memory

RSSI

Received Signal Strength Indicator

SD-ADC

Sigma-Delta Analog to Digital Converter

SFR

Special Function Register

SPI

Serial Peripheral Interface

TBD

To Be Defined

TX

Transmitter

UHF

Ultra High Frequency

ULP

Ultra Low Power

WUP

Wake-UP

4 References

[1] **WFS-5c_MRKIII-MDI**
MRK III Monitor and Download Interface WFS-5c

[2] **WFS-5c_MRKIII-ROM-LIB**
MRK III ROM Library for the WFS-5c Device Family

5 Revision history

Revision	Release date	Document status	Change notice	Supersedes
1.0	10 December 2018	Product user manual	—	0.1
Modifications:	• Section 2.5 – Reworked and extended the entire section – Removed support for CMF – Added RSSI measurement sequence • Editorial changes in all sections			

6 Contact information

For more information, please visit: http://www.nxp.com

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