



Anticipate EMC with LTSPICE

**more
than you
expect**



Sylvain Le Bras

Field Application Engineer

Sylvain.LeBras@we-online.com

Anticipate EMC with LTSpice

Using LTSPICE and Redexpert to check power supply designs

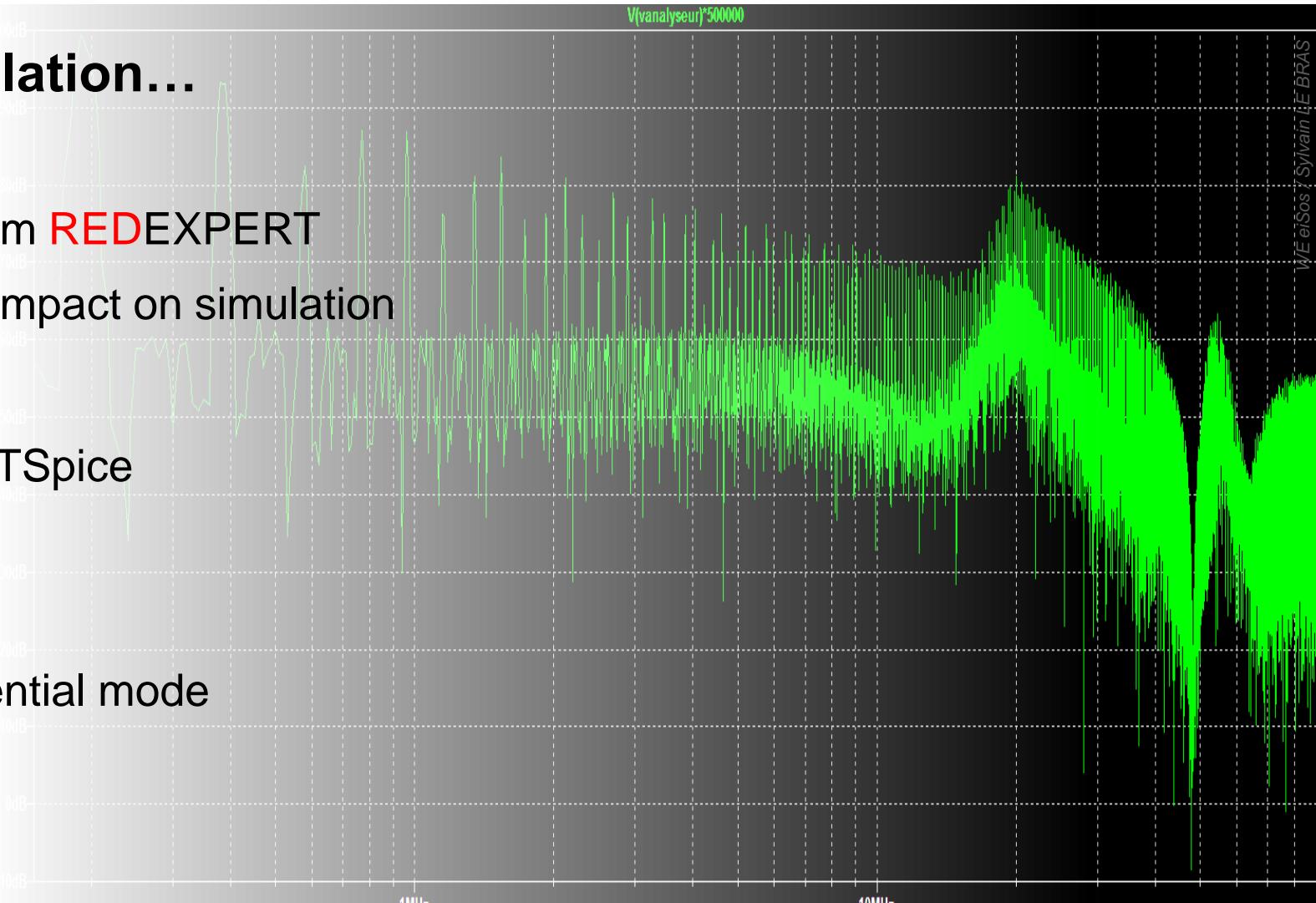


- Intro : From functional simulation...

- Output ripple of a Buck
- Extracting EMC accurate data from REDEXPERT
- Example of (non) EMC accurate impact on simulation

- ...To EMC simulation

- Enabling EMC measurement in LTSpice
- Getting Seriously Accurate ?
- Going further with simulation
 - Splitting Common and Differential mode
 - Making simulation look real
- Examples



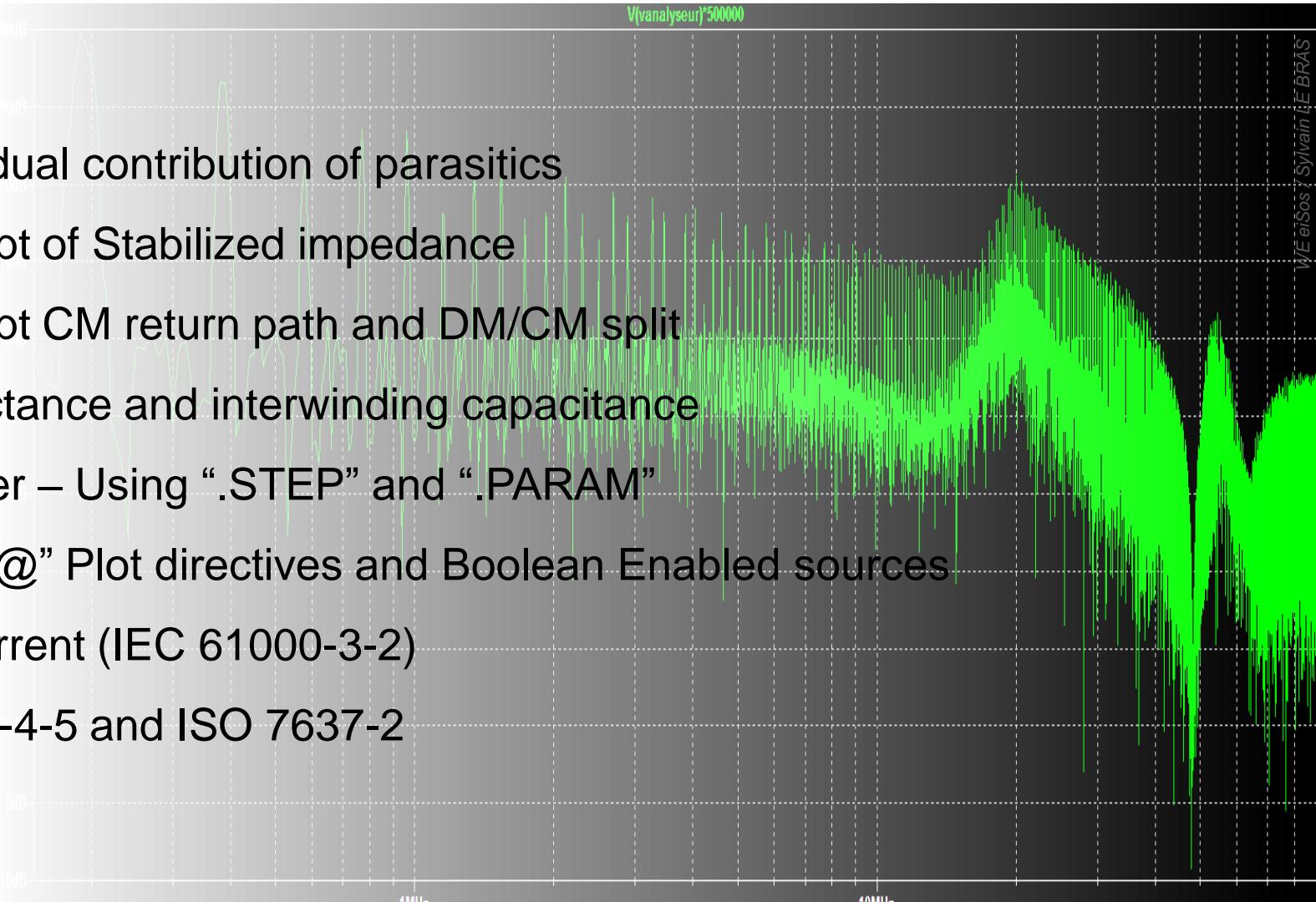
Anticipate EMC with LTSpice

Using LTSPICE and Redexpert to check power supply designs



■ Available examples

1. Output ripple of a Buck – Individual contribution of parasitics
2. Noise at Input of Buck – Concept of Stabilized impedance
3. Noise at Input of Buck – Concept CM return path and DM/CM split
4. Flyback converter – Stray inductance and interwinding capacitance
5. Brushless DC motor and inverter – Using “.STEP” and “.PARAM”
6. Evaluation of filter response – “@” Plot directives and Boolean Enabled sources
7. Power Factor and Harmonic current (IEC 61000-3-2)
8. Surges according to IEC 61000-4-5 and ISO 7637-2



Setup

Getting the tools ready



NOW PART OF



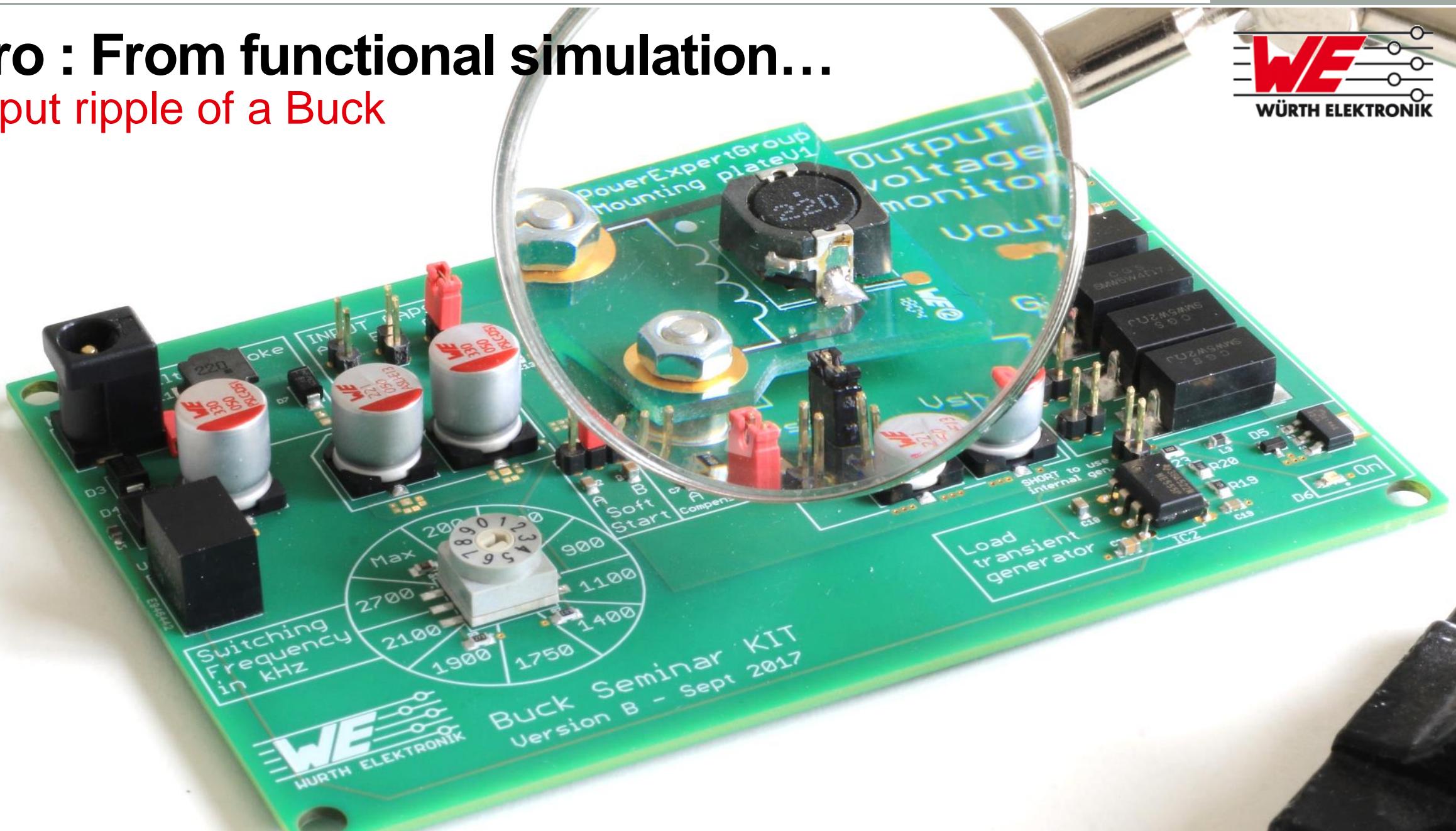
<https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html>

RED EXPERT

<https://www.we-online.com/redexpert>

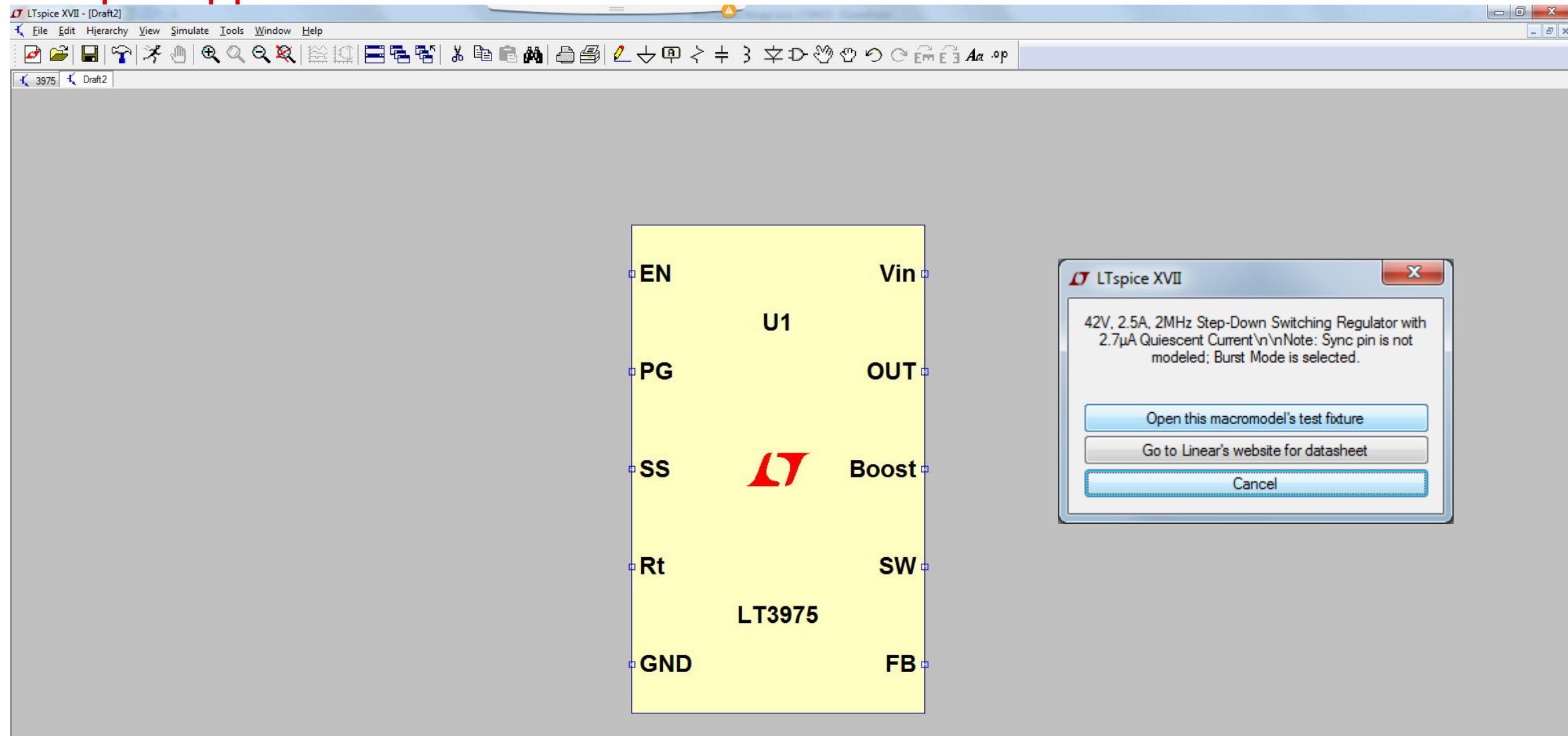
Intro : From functional simulation...

Output ripple of a Buck



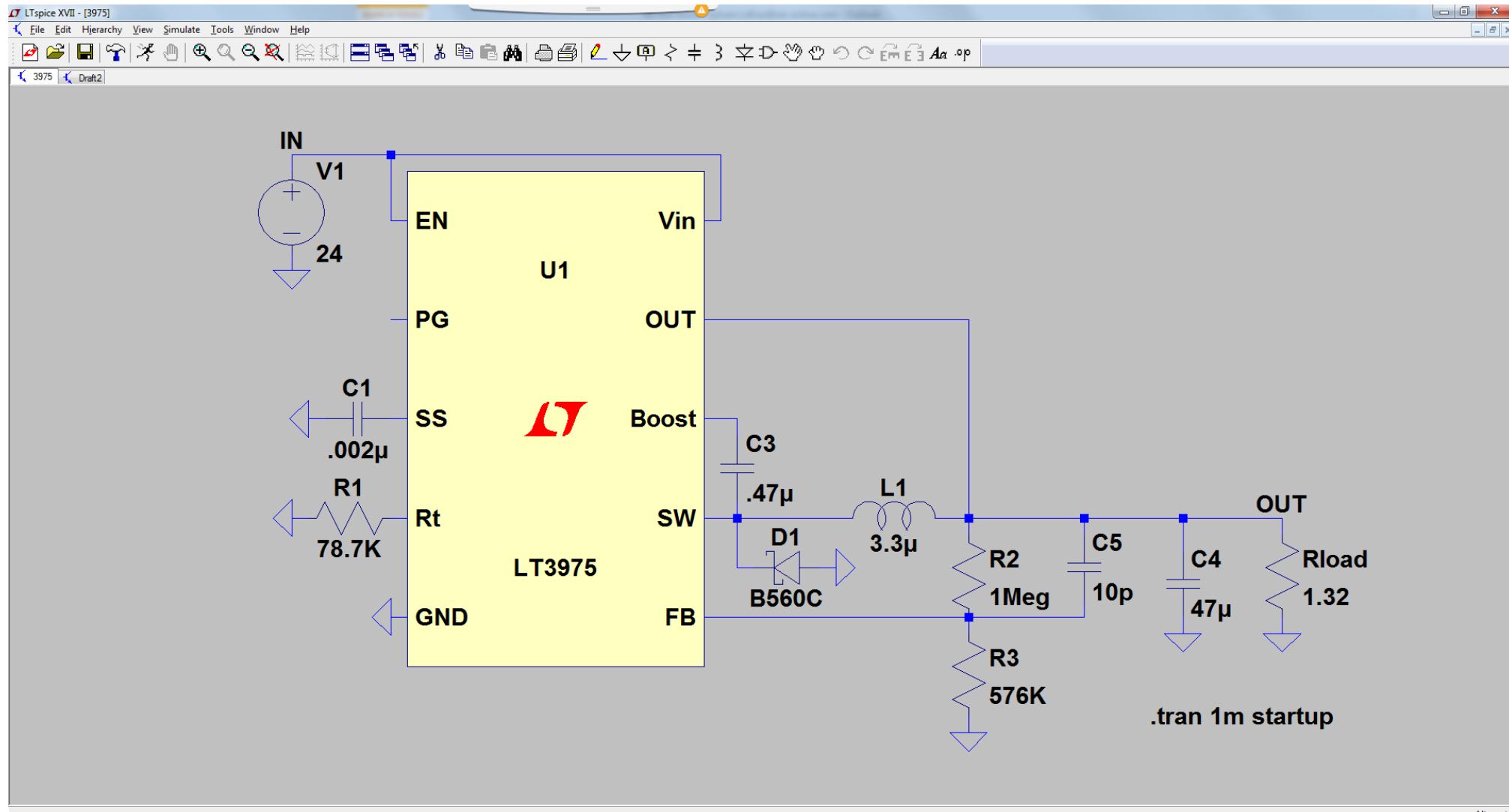
Intro : From functional simulation...

Output ripple of a Buck



Intro : From functional simulation...

Output ripple of a Buck (without the “hardcore mathematics”)

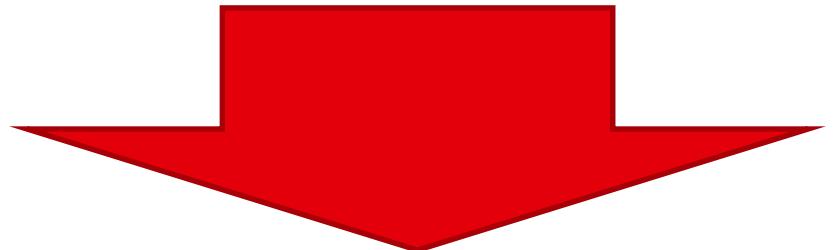


Output ripple of a Buck

Hardcore maths ?



$$V = R \cdot I$$



$$\Delta V = Z_C \cdot \Delta I_L$$

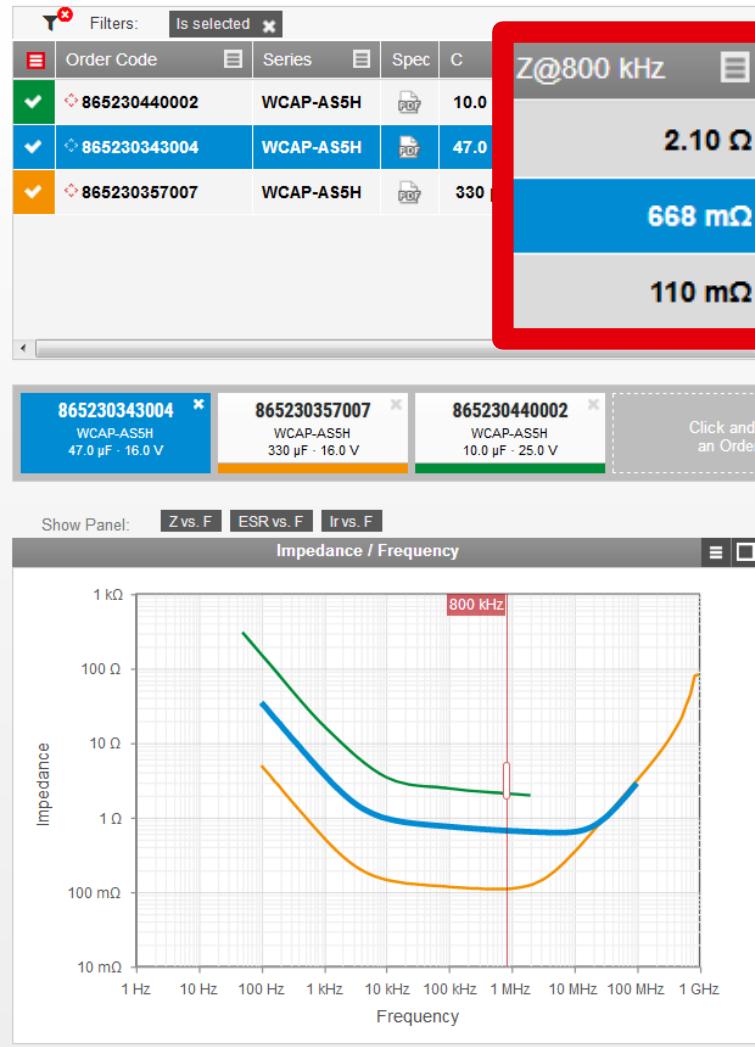
Output ripple of a Buck

Redexpert : an ode to laziness



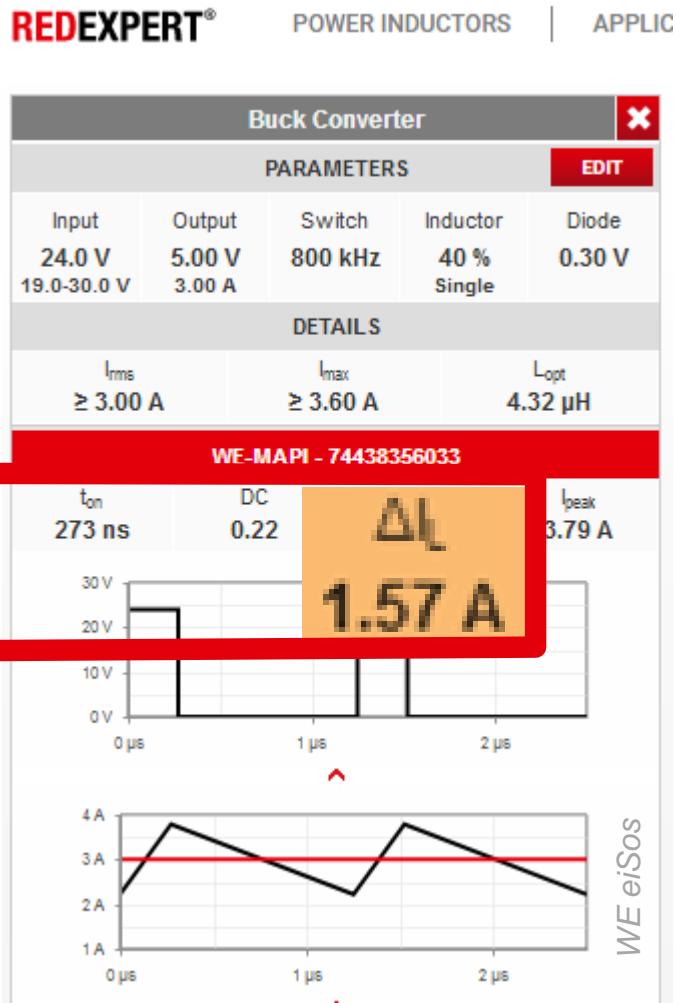
REDEXPERT® ALUMINIUM ELECTROLYTIC CAPACITORS

APPLICATIONS



ZC

ΔIL



Output ripple of a Buck

Redexpert : an ode to laziness



REDEXPERT® ALUMINIUM ELECTROLYTIC CAPACITORS | APPLICATIONS | HOW TO | SHARE

ITEMS LE BRAS

Order Code	Series	C	V _R	Z@800 kHz	DF	Z _{max} @ 100kHz	I _{ripple} @ T _{max} 120Hz	I _{ripple} @ T _{max} 100kHz	Description	I _{leak}
865230440002	WCAP-AS5H	10.0 μ F	25.0 V	2.10 Ω	< 16 %		23.0 mA		ASDB055100M025DVCTAE000	3.00
865230343004	WCAP-AS5H	47.0 μ F	16.0 V	668 m Ω	< 22 %		50.0 mA		ASDD055470M016DVCTBE000	7.52
865230357007	WCAP-AS5H	330 μ F	16.0 V	110 m Ω	< 22 %		300 mA		ASDF105331M016DVCTEE000	52.8

Filters: Is selected

Click and type or drop an Order Code here Add to Cart

Show Panel: Z vs. F ESR vs. F Ir vs. F

Impedance / Frequency

ESR / Frequency

Ripple Current / Frequency

WE eiSos

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[Link](#)

Output ripple of a Buck

Redexpert : an ode to laziness



REDEXPERT®

POWER INDUCTORS

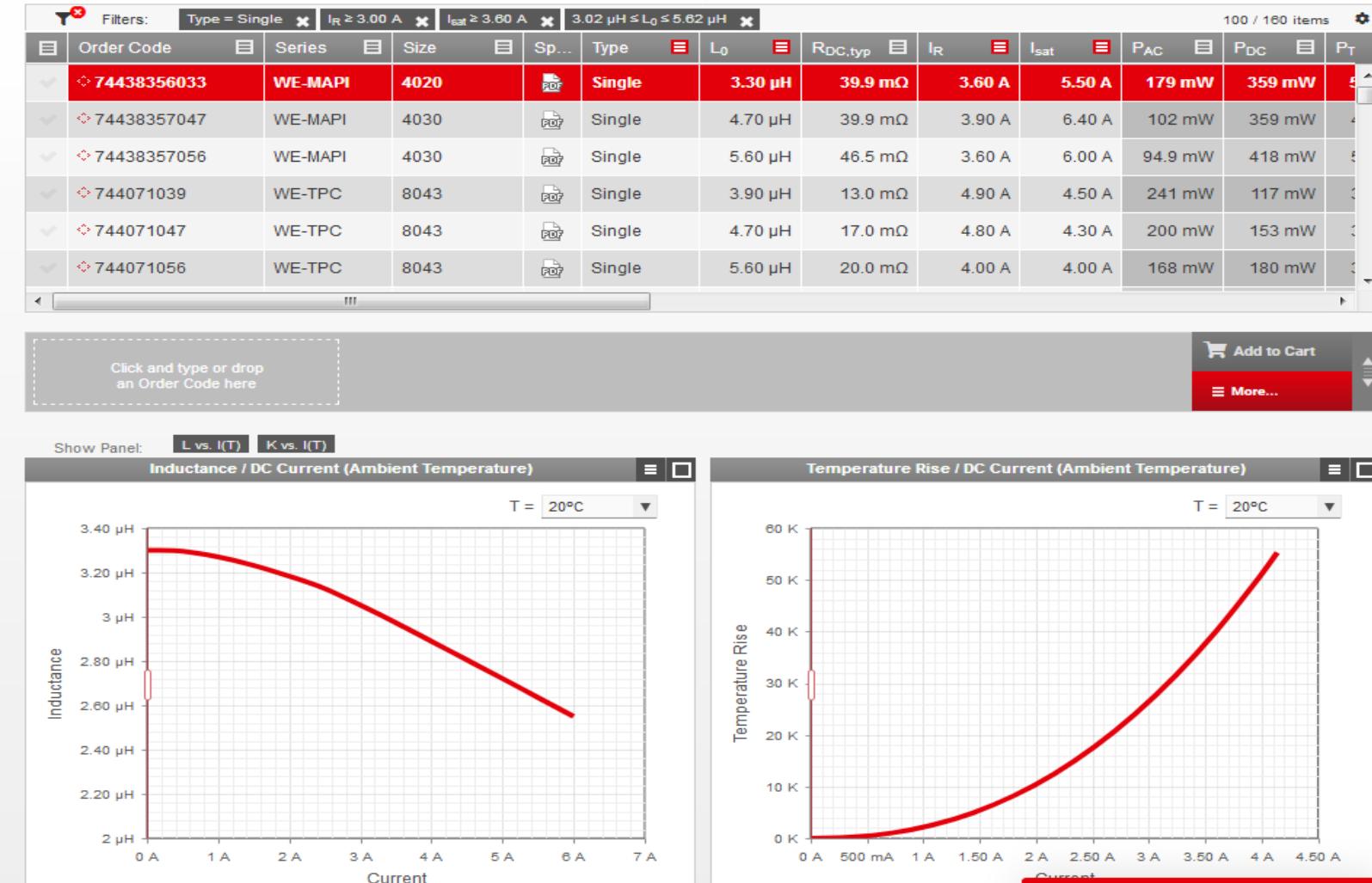
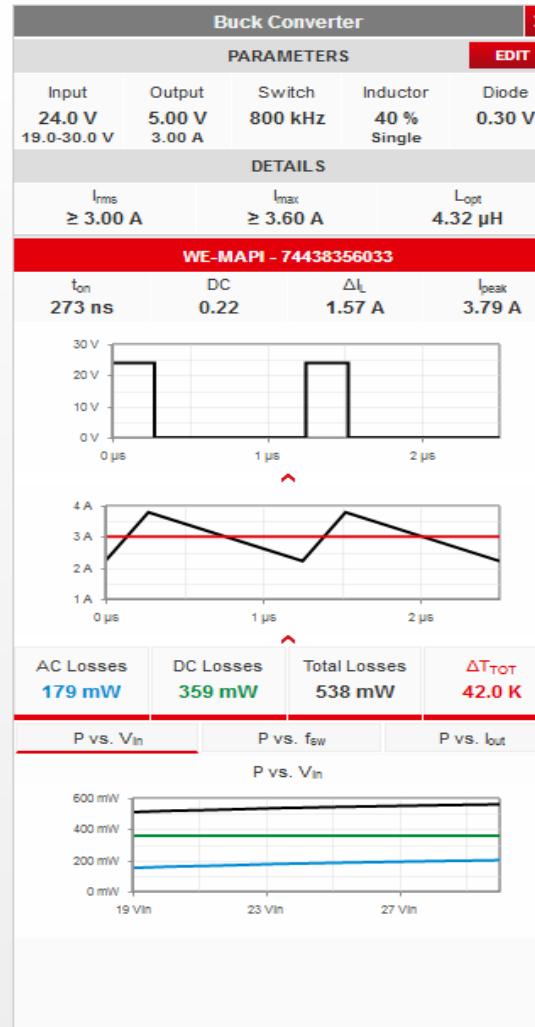
APPLICATIONS

HOW TO

SHARE

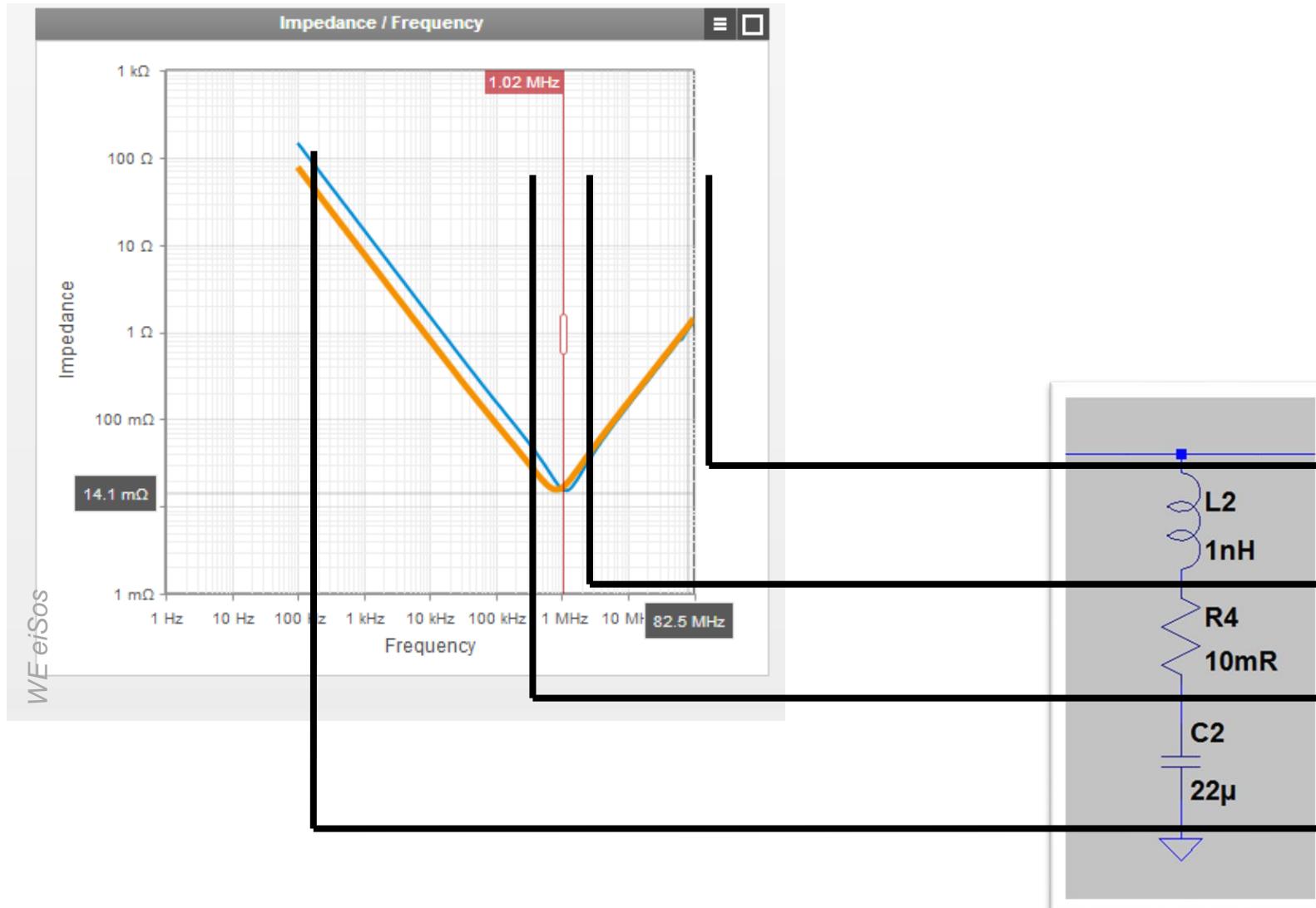
ITEMS

LE BRAS



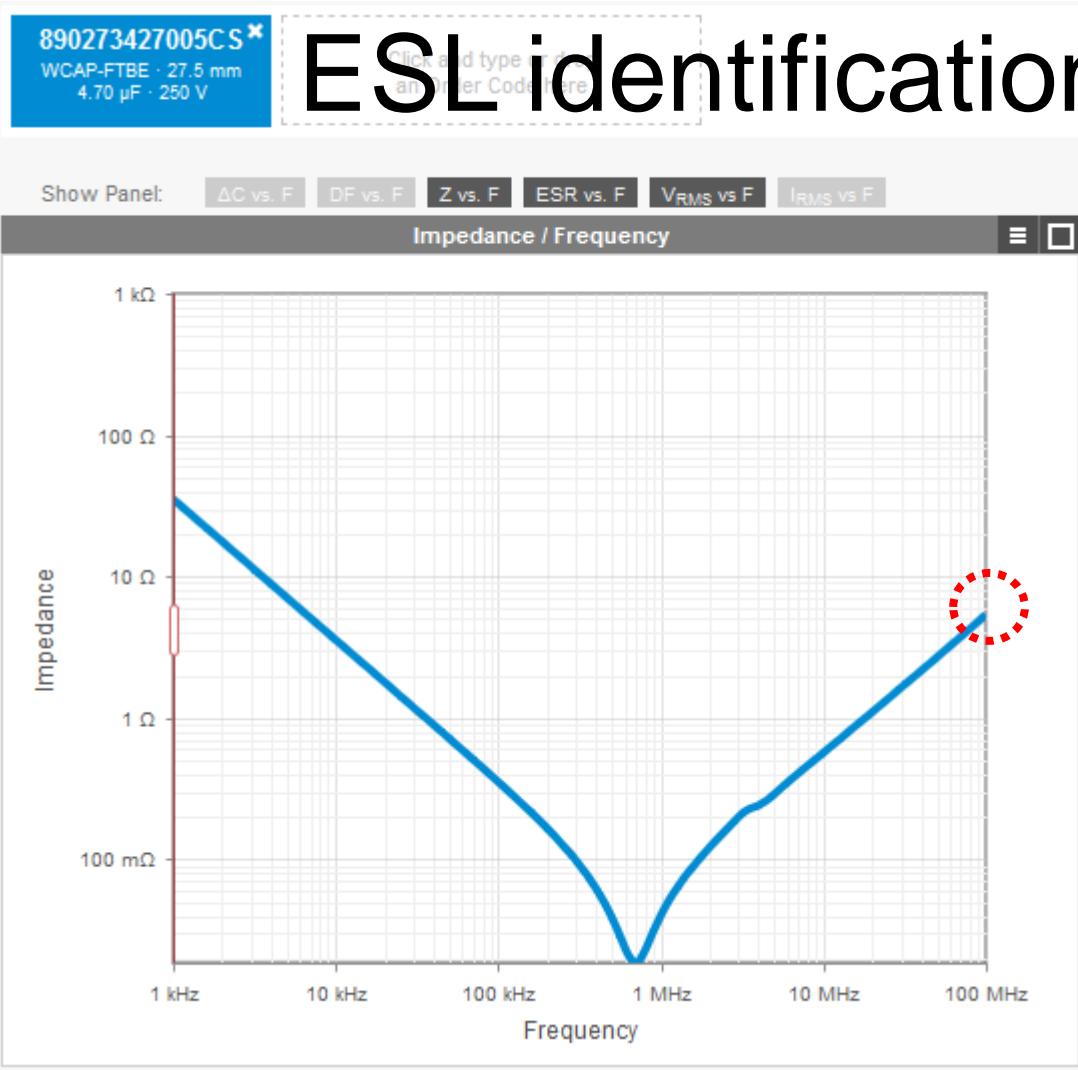
Output ripple of a Buck

Extracting EMC accurate data from REDEXPERT



Output ripple of a Buck

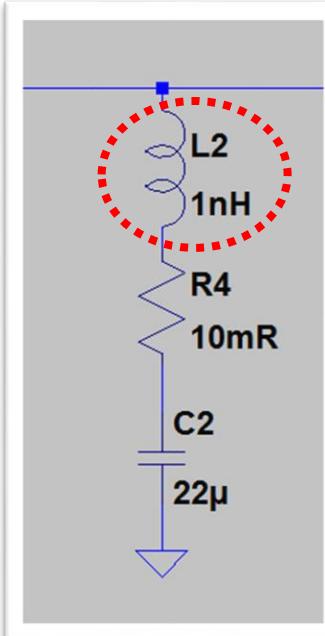
Extracting EMC accurate data from REDEXPERT



$$|Z_L| = L\omega$$

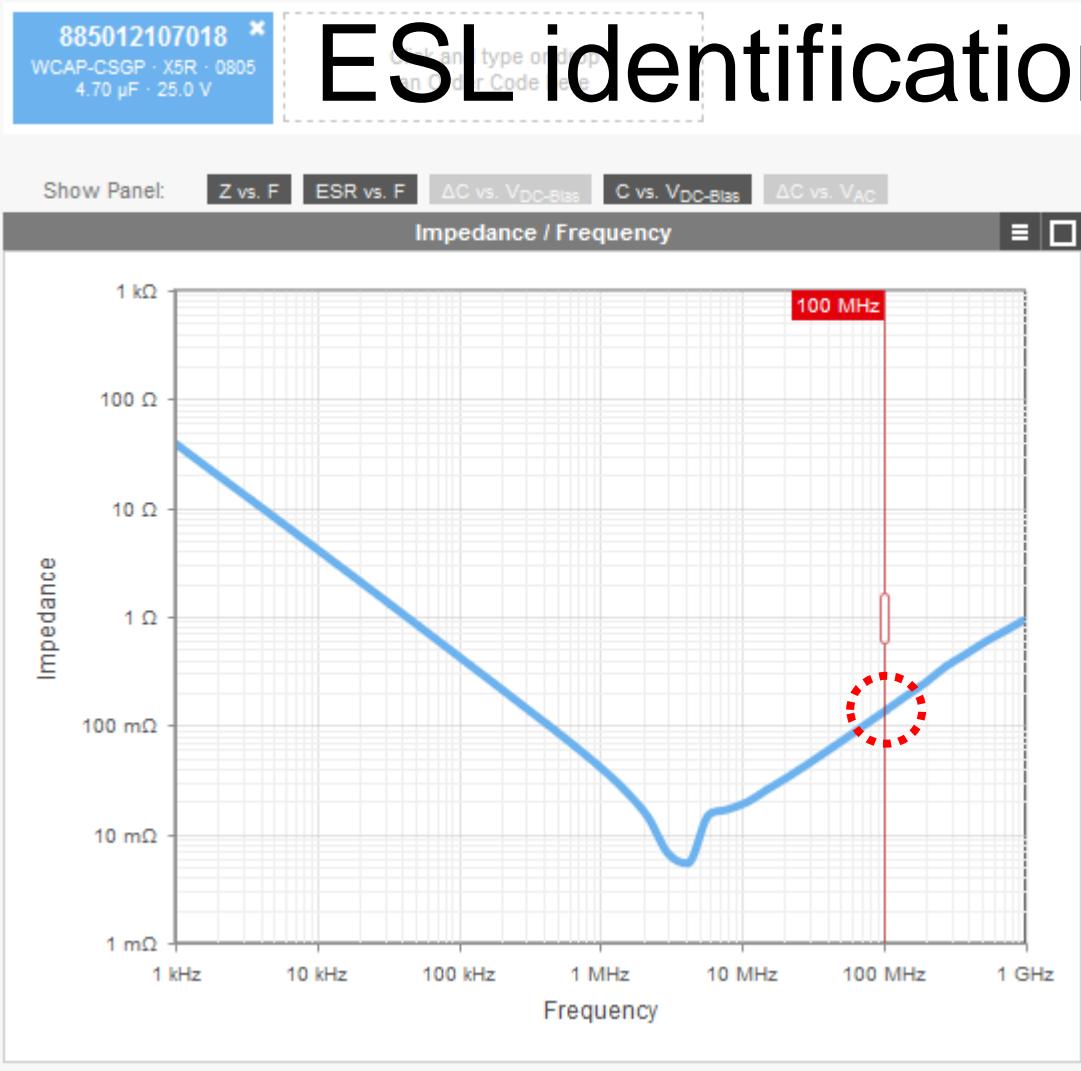
$$\frac{Z_L}{\omega} = L$$

$$L = \frac{|Z_L|}{2\pi F} = \frac{5}{100 \times 10^6 \times 2\pi} \cong 8 \text{ nH}$$



Output ripple of a Buck

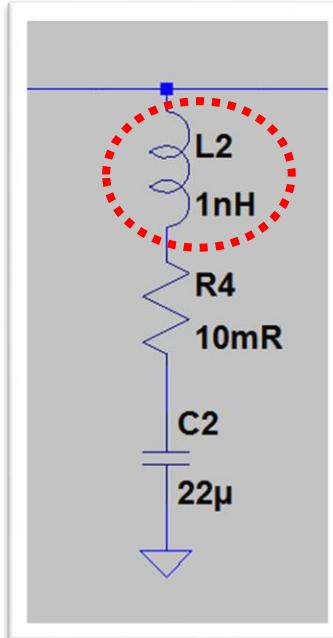
Extracting EMC accurate data from REDEXPERT



$$|Z_L| = L\omega$$

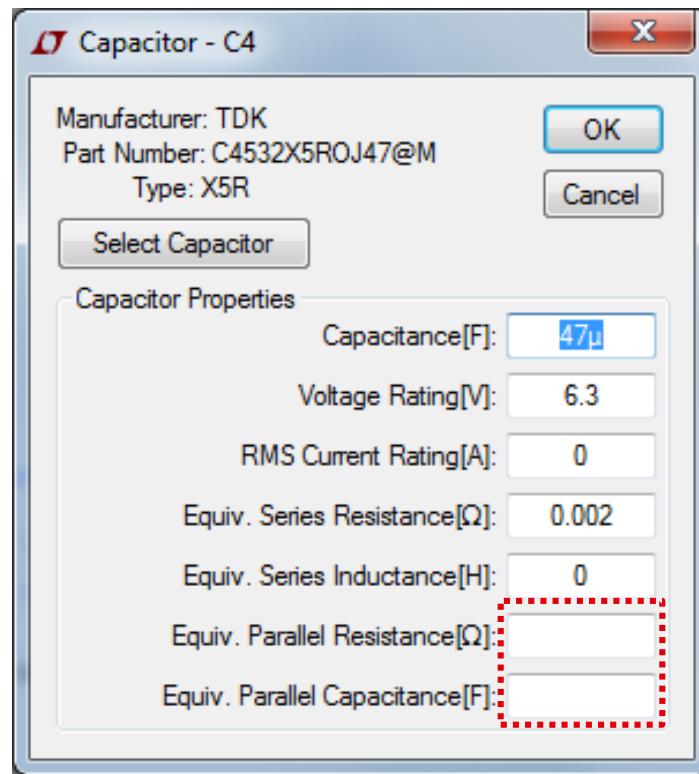
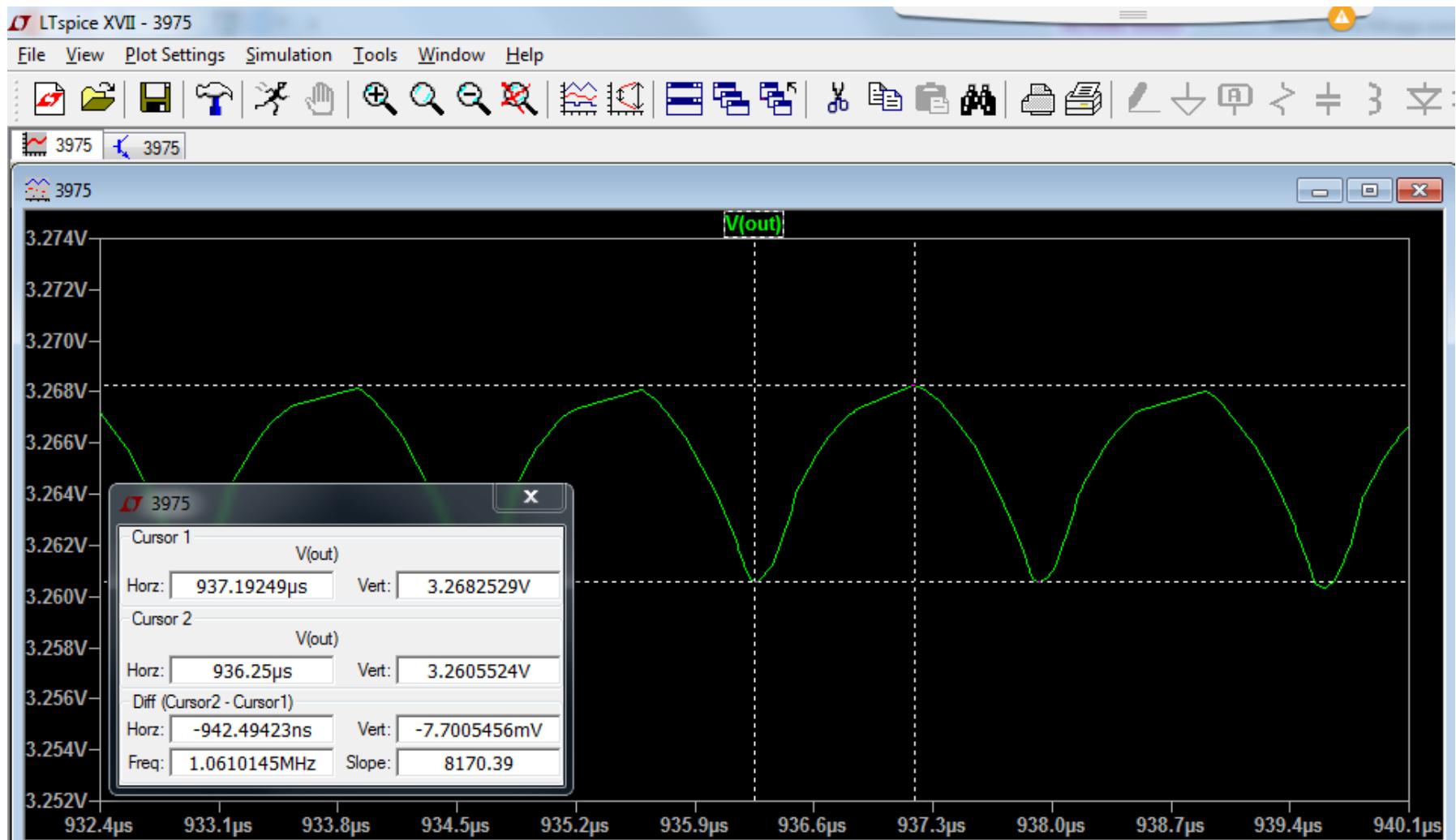
$$\frac{Z_L}{\omega} = L$$

$$L = \frac{|Z_L|}{2\pi F} = \frac{0,132}{100 \times 10^6 \times 2\pi} \cong 0.2 \text{ nH}$$



Output ripple of a Buck

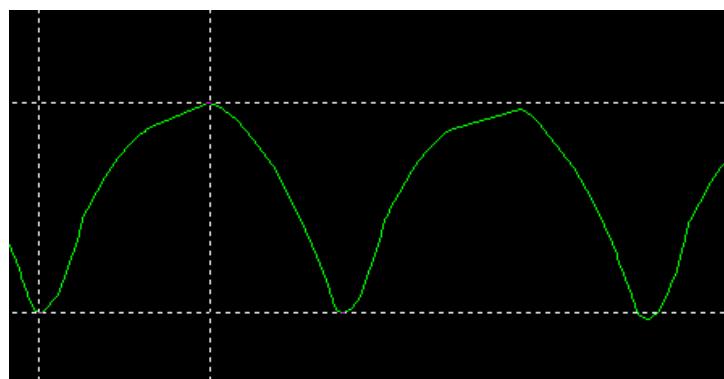
Example of (non) EMC accurate impact on simulation



- ESR = 2 mOhms
- ESL = 0 nH
- DC bias
(DC ? Like don't care ?)

Output ripple of a Buck

Example of (non) EMC accurate impact on simulation



Output ripple of a Buck

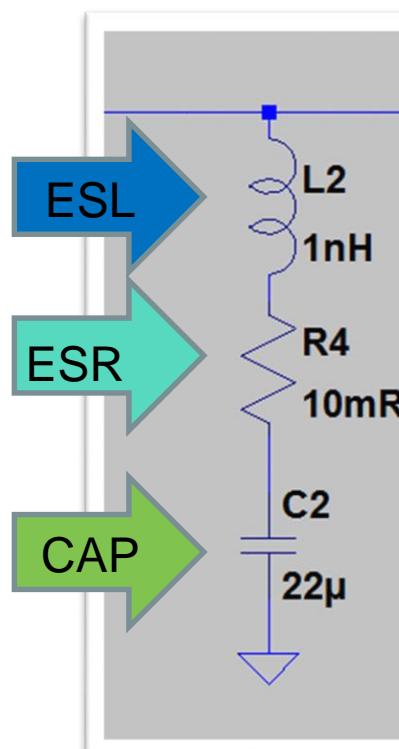
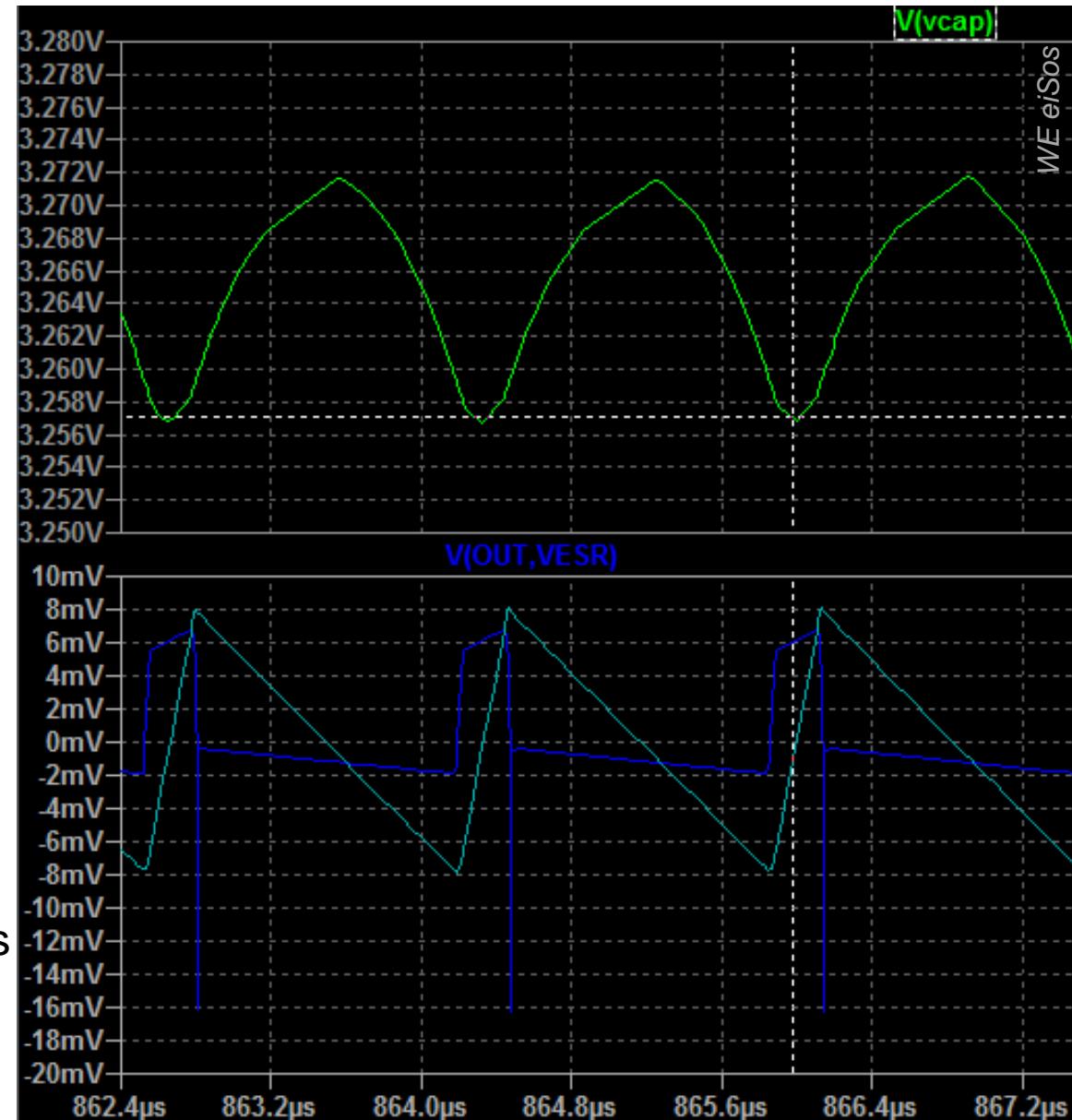
Example of EMC accurate simulation

Charge and discharge of cap

CAP → 14 mV_{p-p}

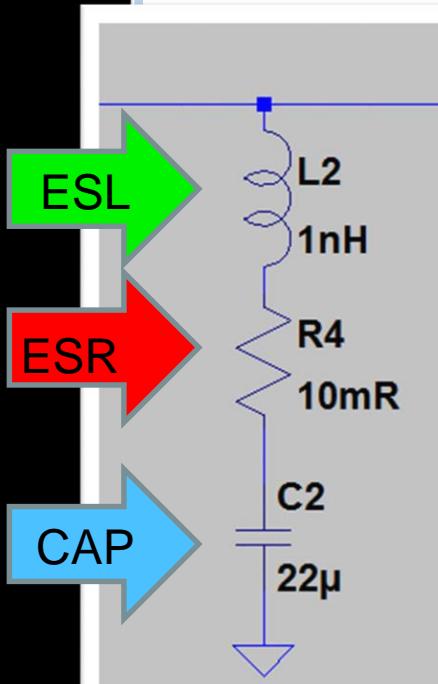
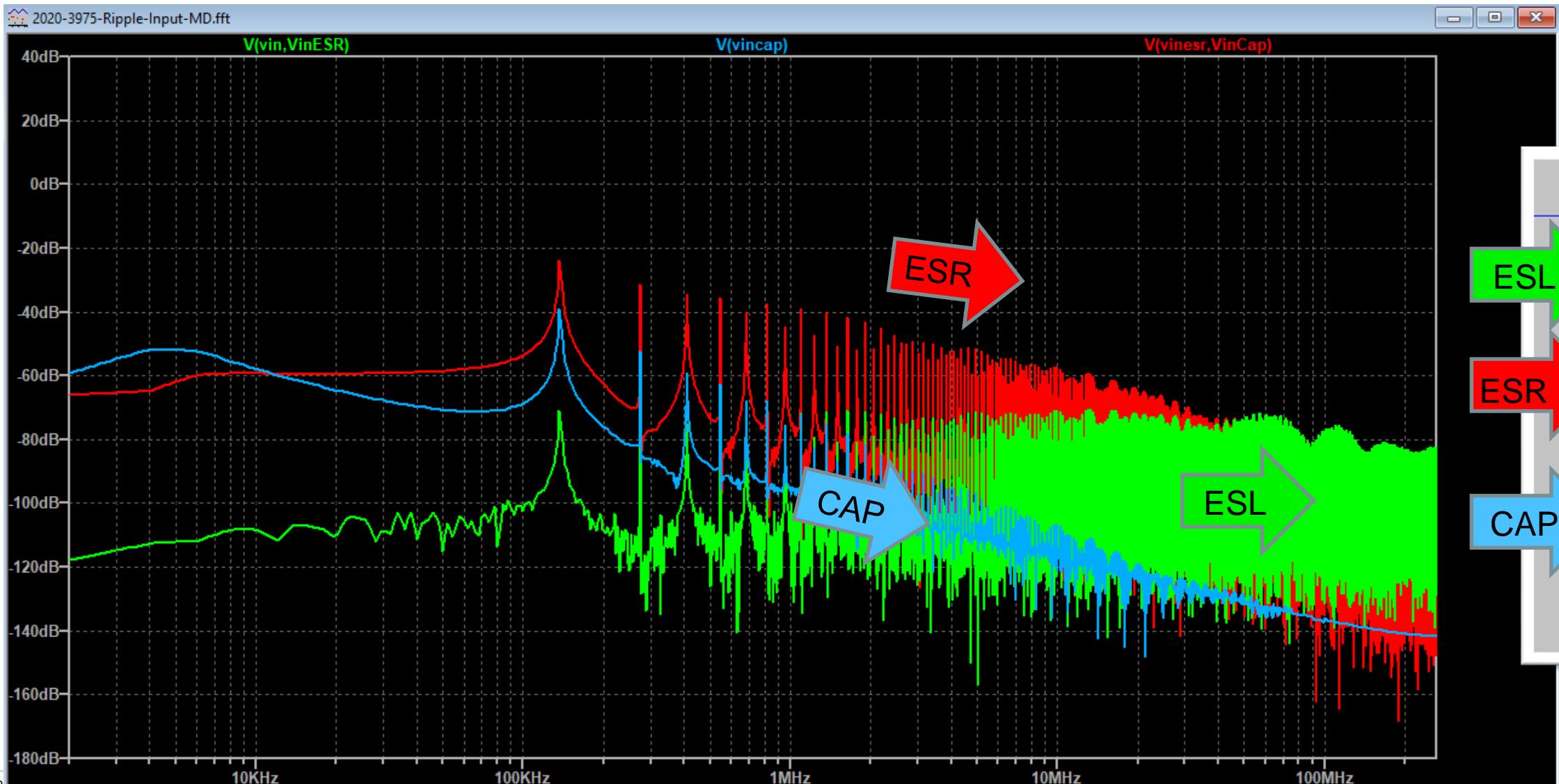
ESR → 16 mV_{p-p}

ESL → 10 mV_{p-p} at low frequencies
 25 mV_{p-p} at high frequencies



Capacitor ripple voltage example

ESR / ESL / CAP breakdown in frequency

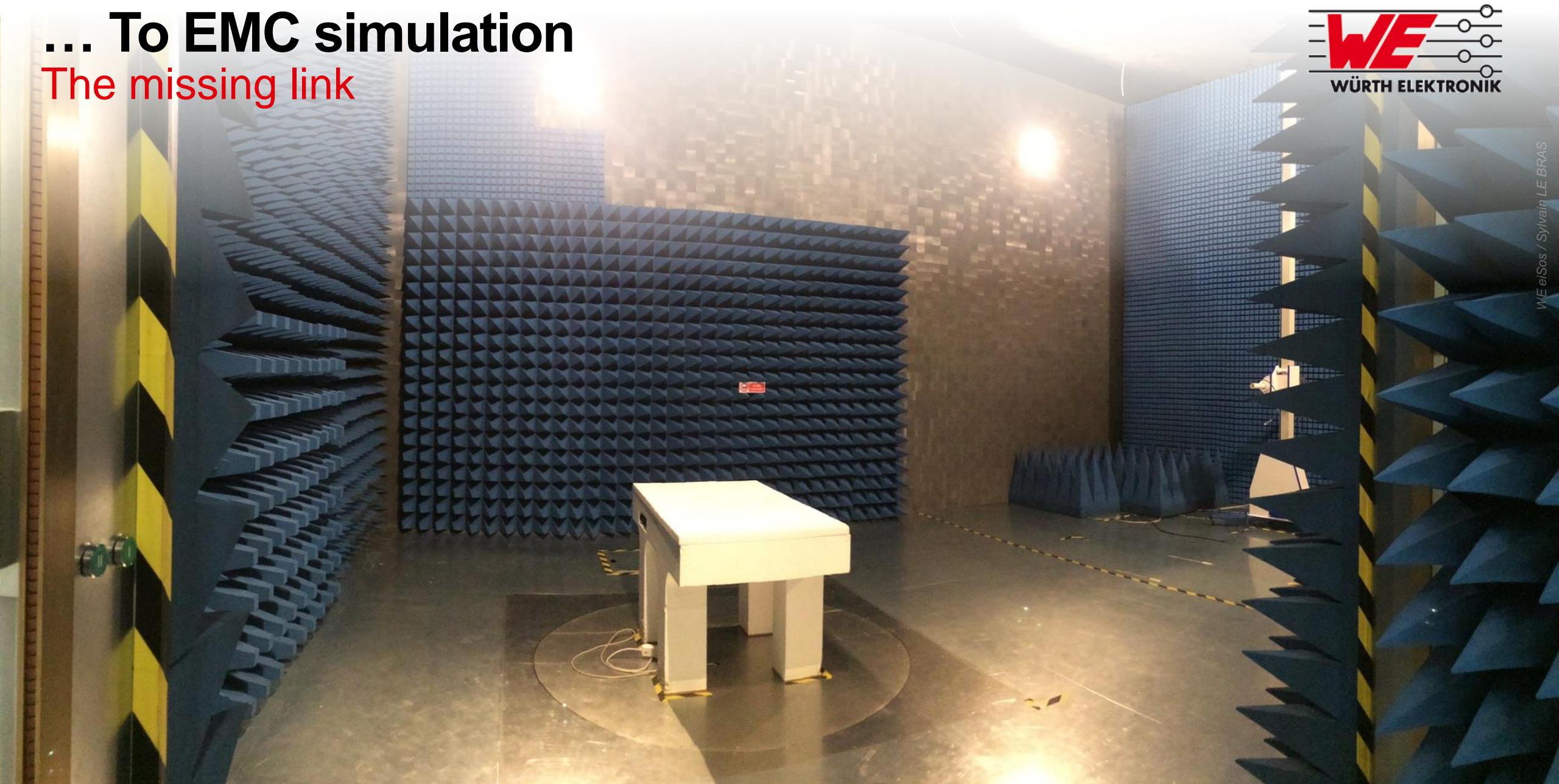


... To EMC simulation

The missing link



WE eiSos / Sylvain LE BRAS



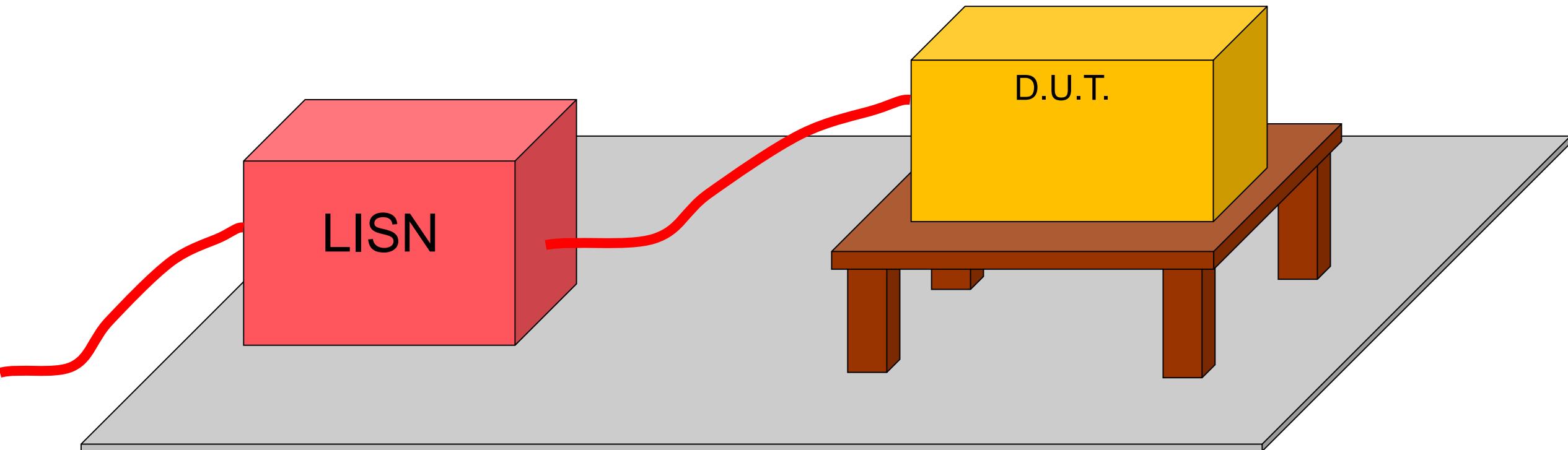
Enabling EMC accurate measurement in LTSpice

What is the keystone of conducted emissions ?



Enabling EMC accurate measurement in LTSpice

What is the keystone of conducted emissions ?

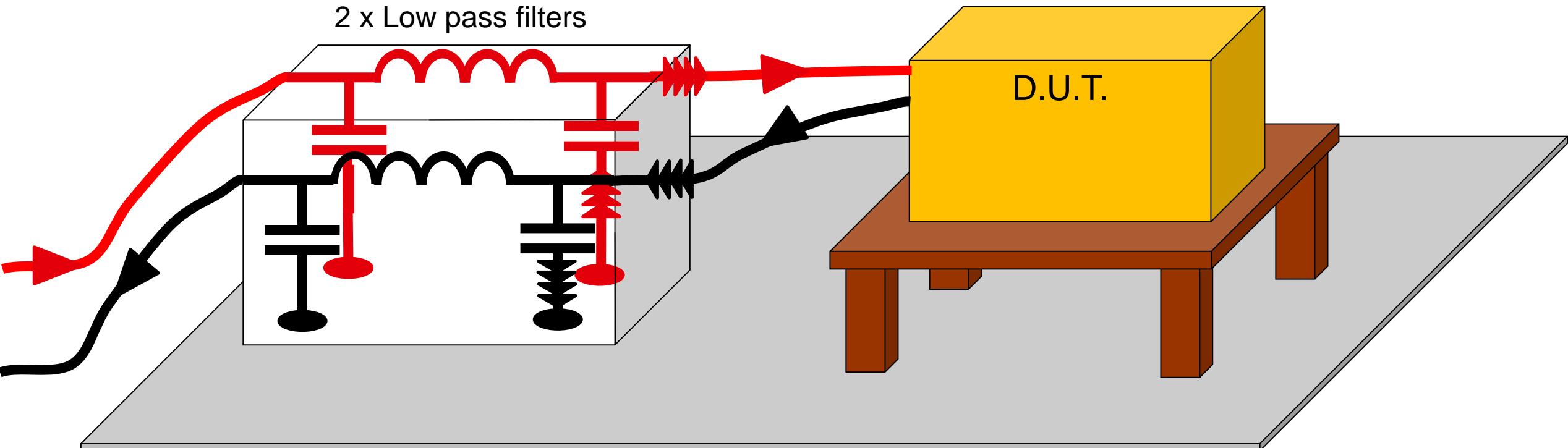


Enabling EMC accurate measurement in LTSpice

What is the keystone of conducted emissions ?



- ▶ Low Frequency
- ▶ High Frequency

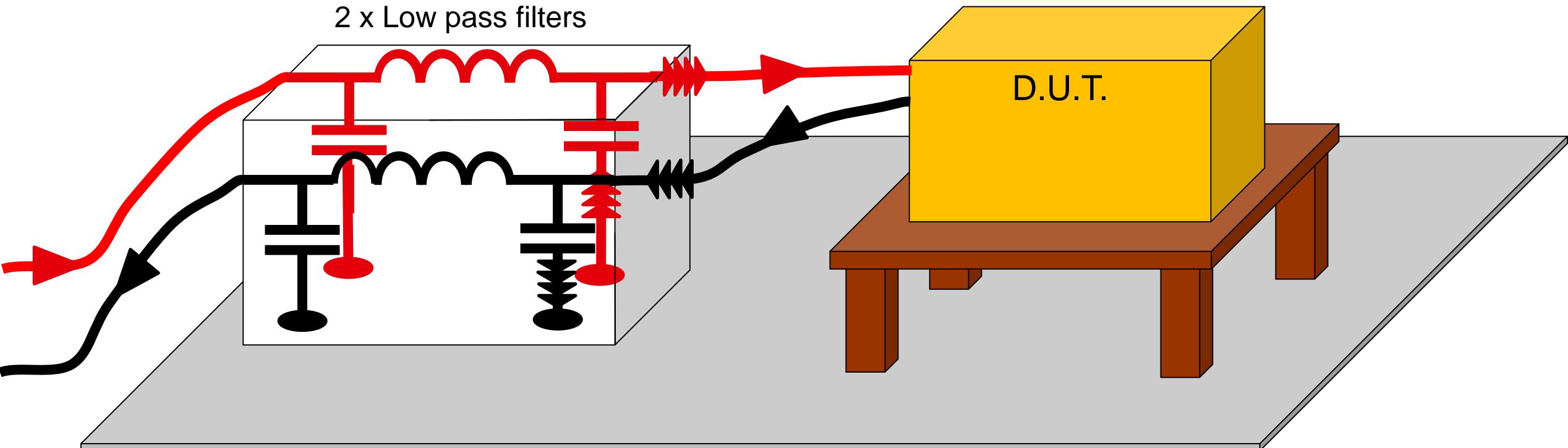


Enabling EMC accurate measurement in LTSpice

What is the keystone of conducted emissions ?

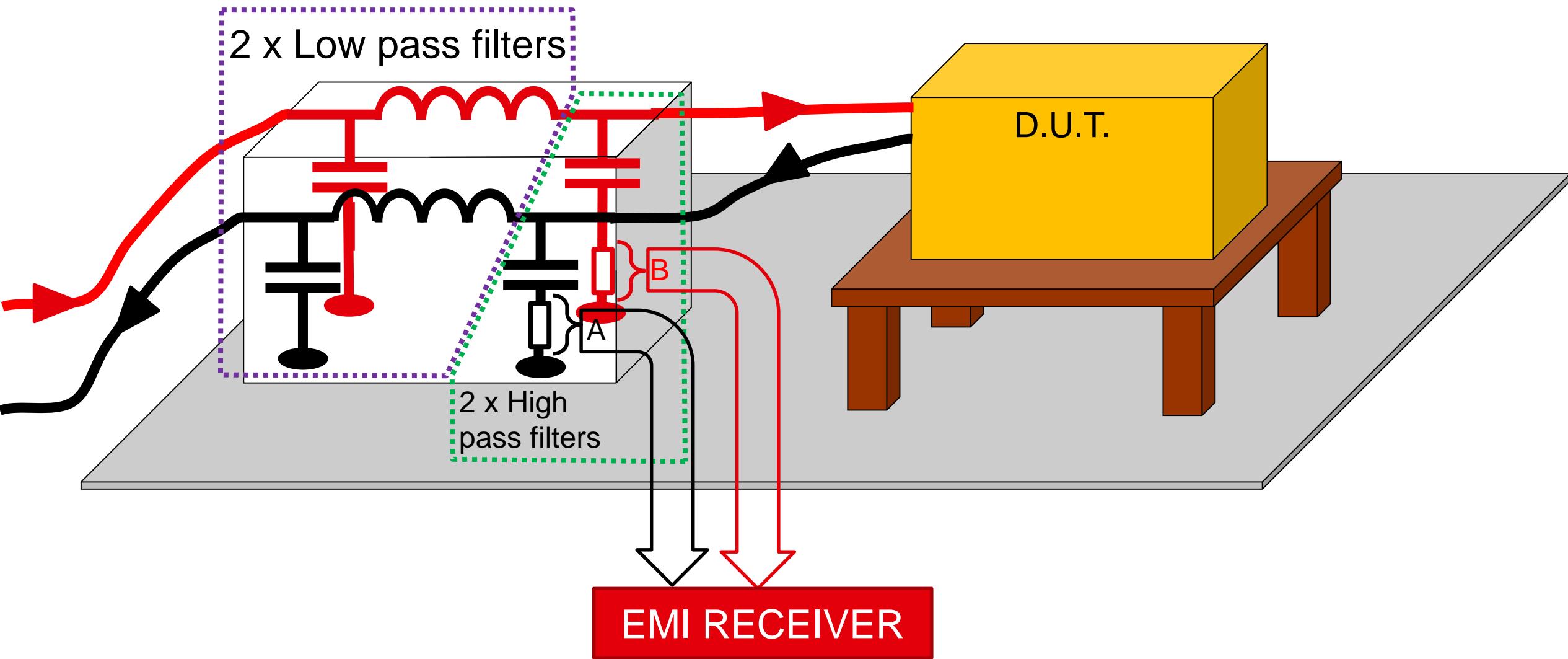


- ▶ Low Frequency
- ▶ High Frequency



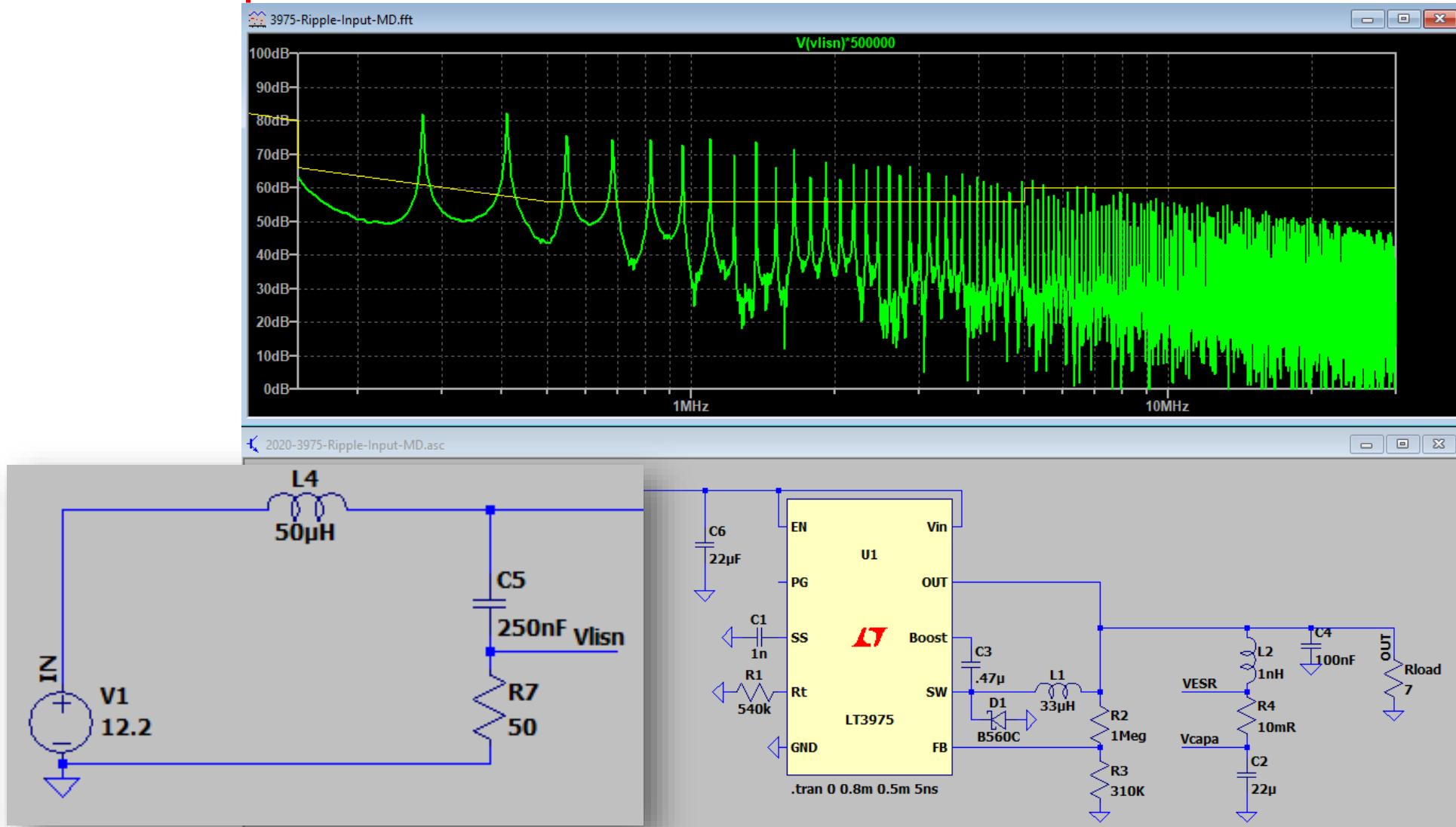
Enabling EMC accurate measurement in LTSpice

What is the keystone of conducted emissions ?



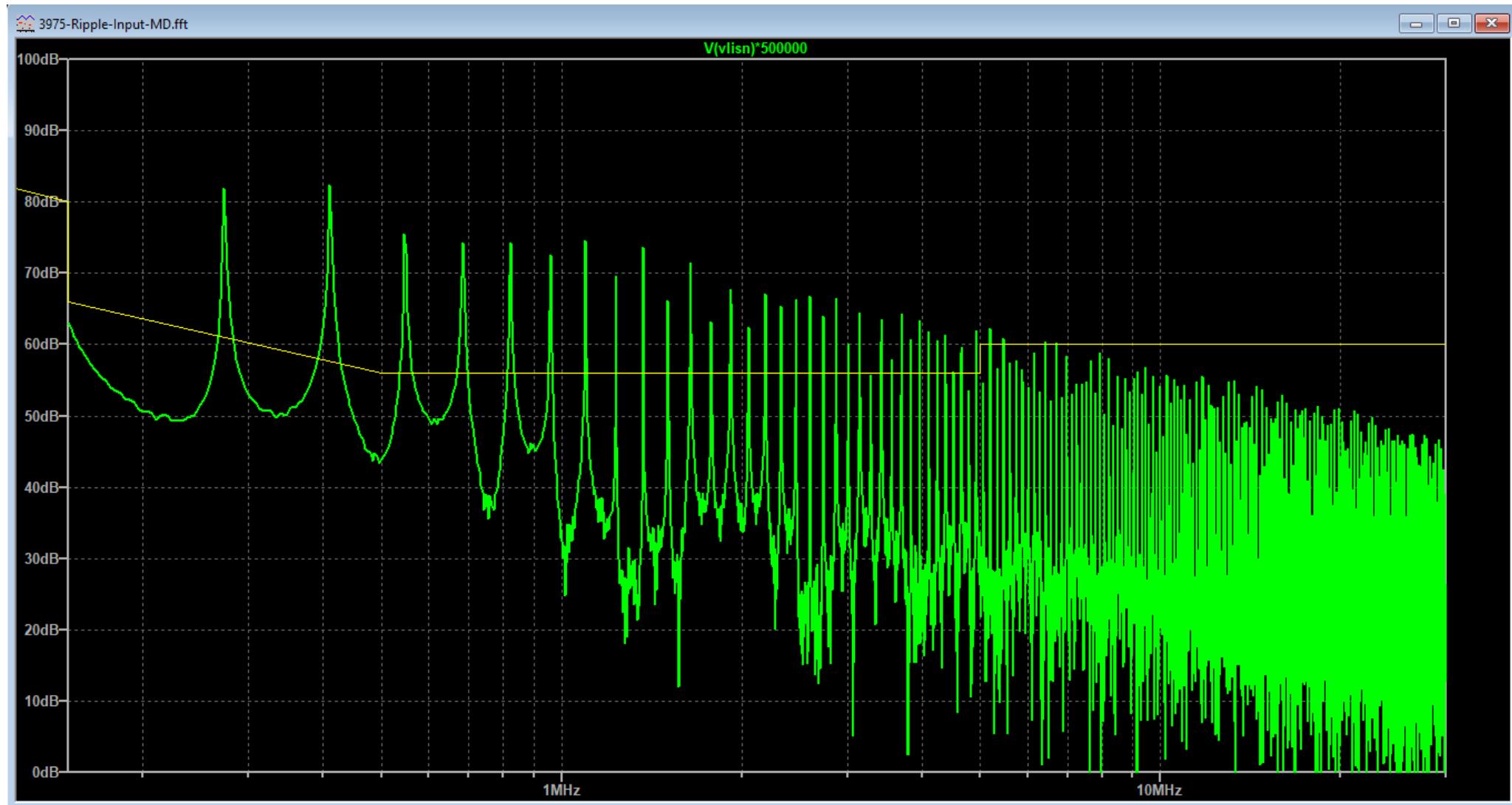
Enabling EMC accurate measurement in LTSpice

FFT with simplified LISN



Reality VS Simulation

FFT with simplified LISN



Reality VS Simulation

Conducted Emissions measurement



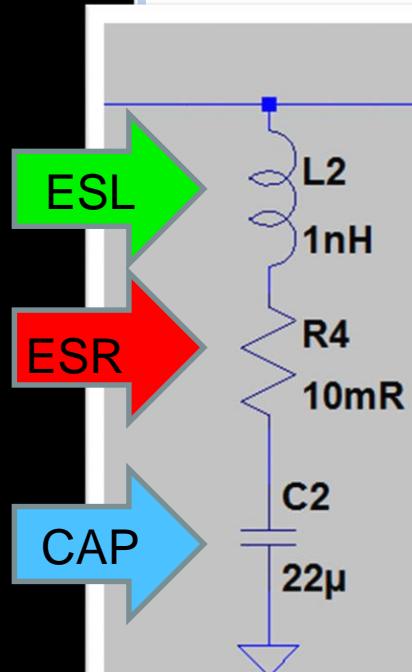
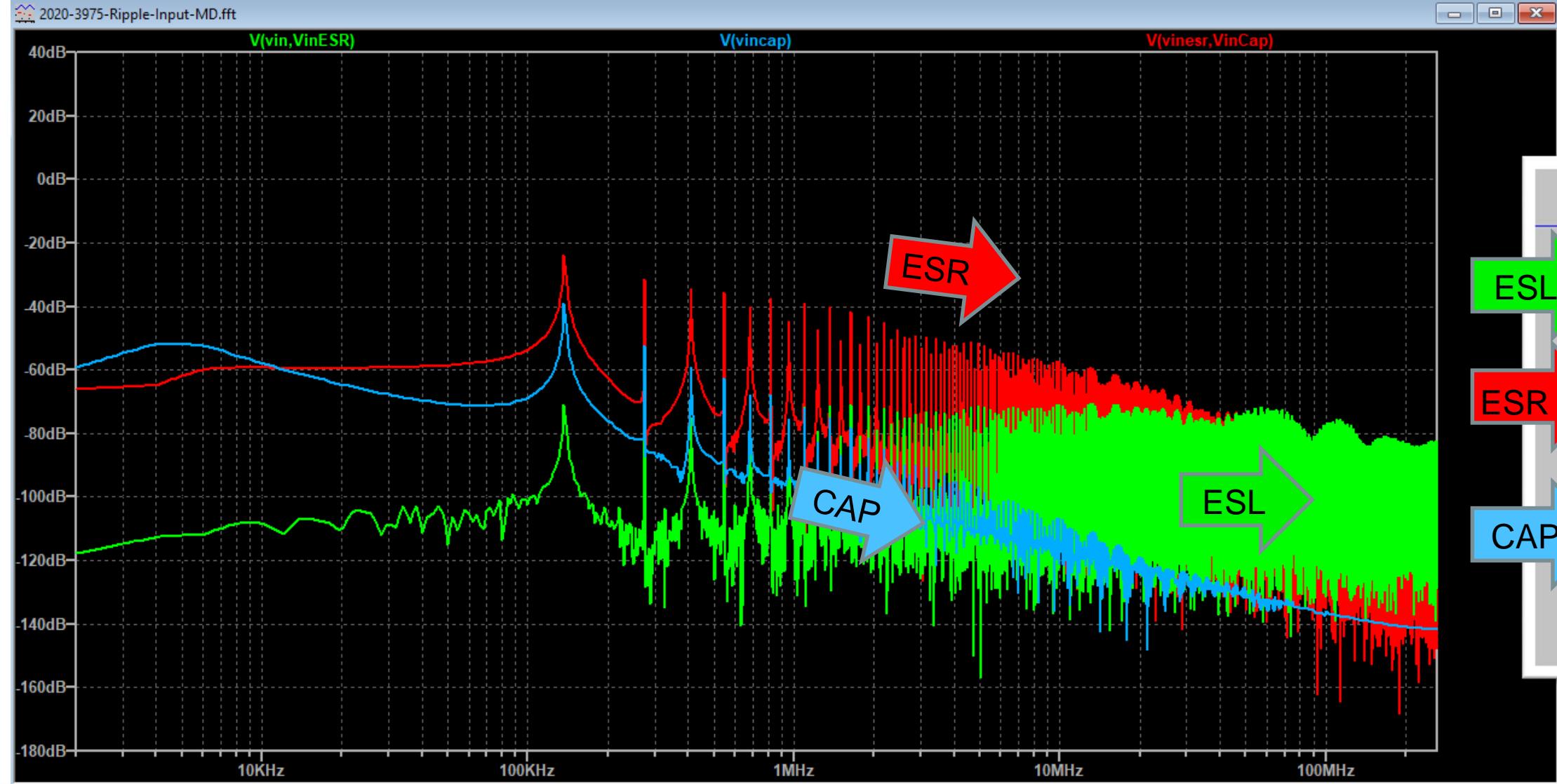
Reality VS Simulation

Conducted Emissions measurement



Reality VS Simulation

ESR / ESL / CAP breakdown in frequency



Reality VS Simulation

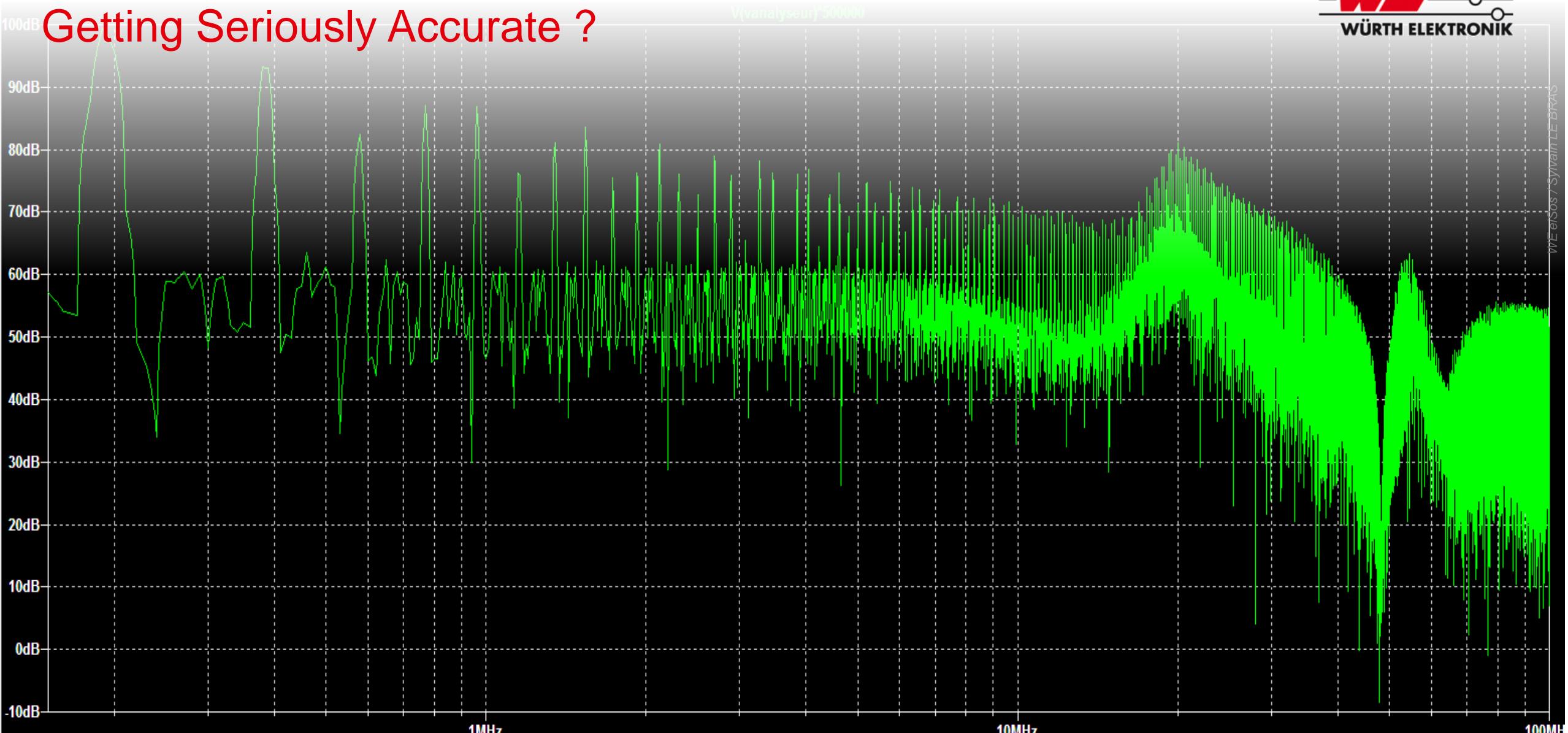


EMI measurement = Σ (Common Mode + Differential Mode)



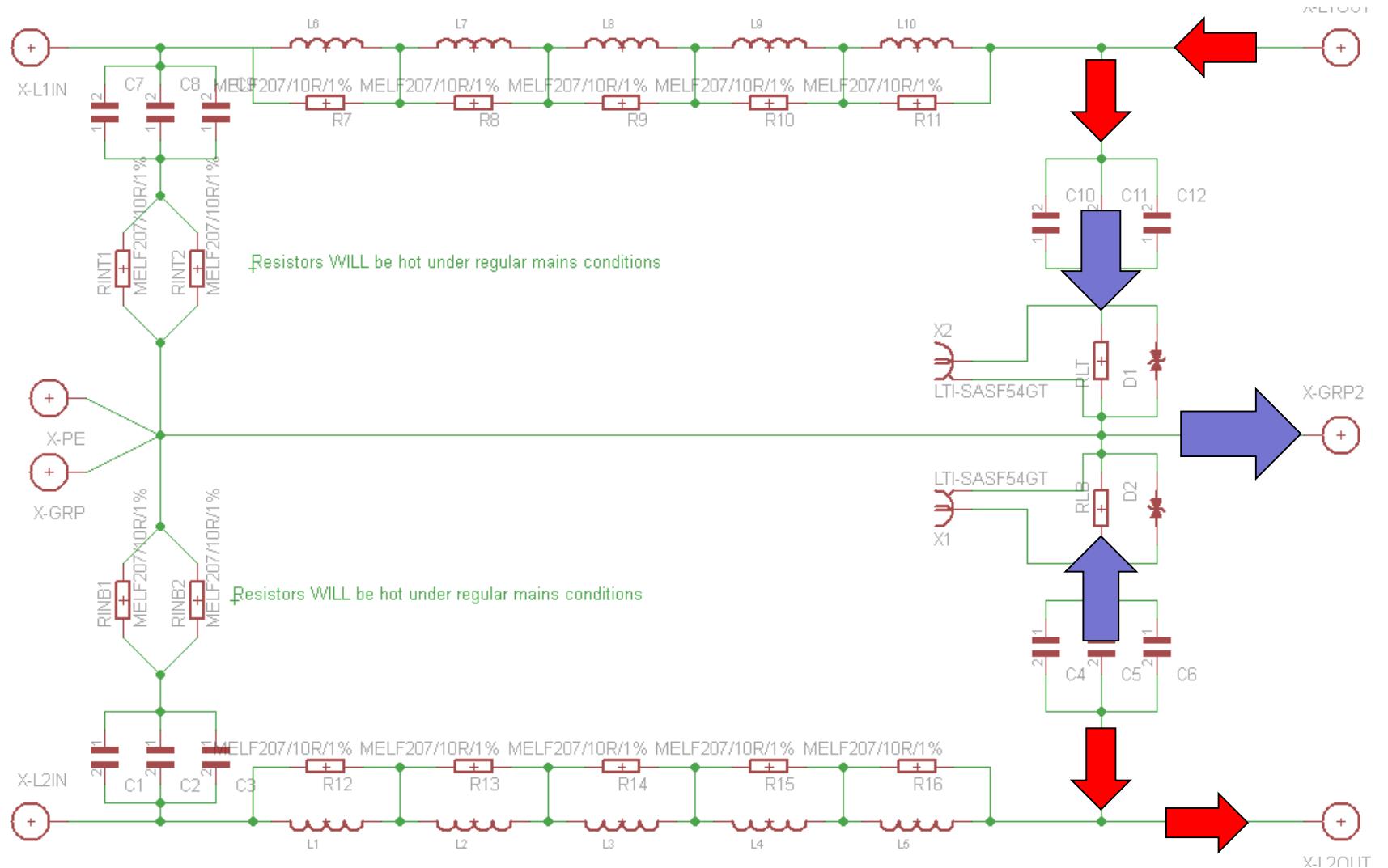
... To EMC simulation

Getting Seriously Accurate ?



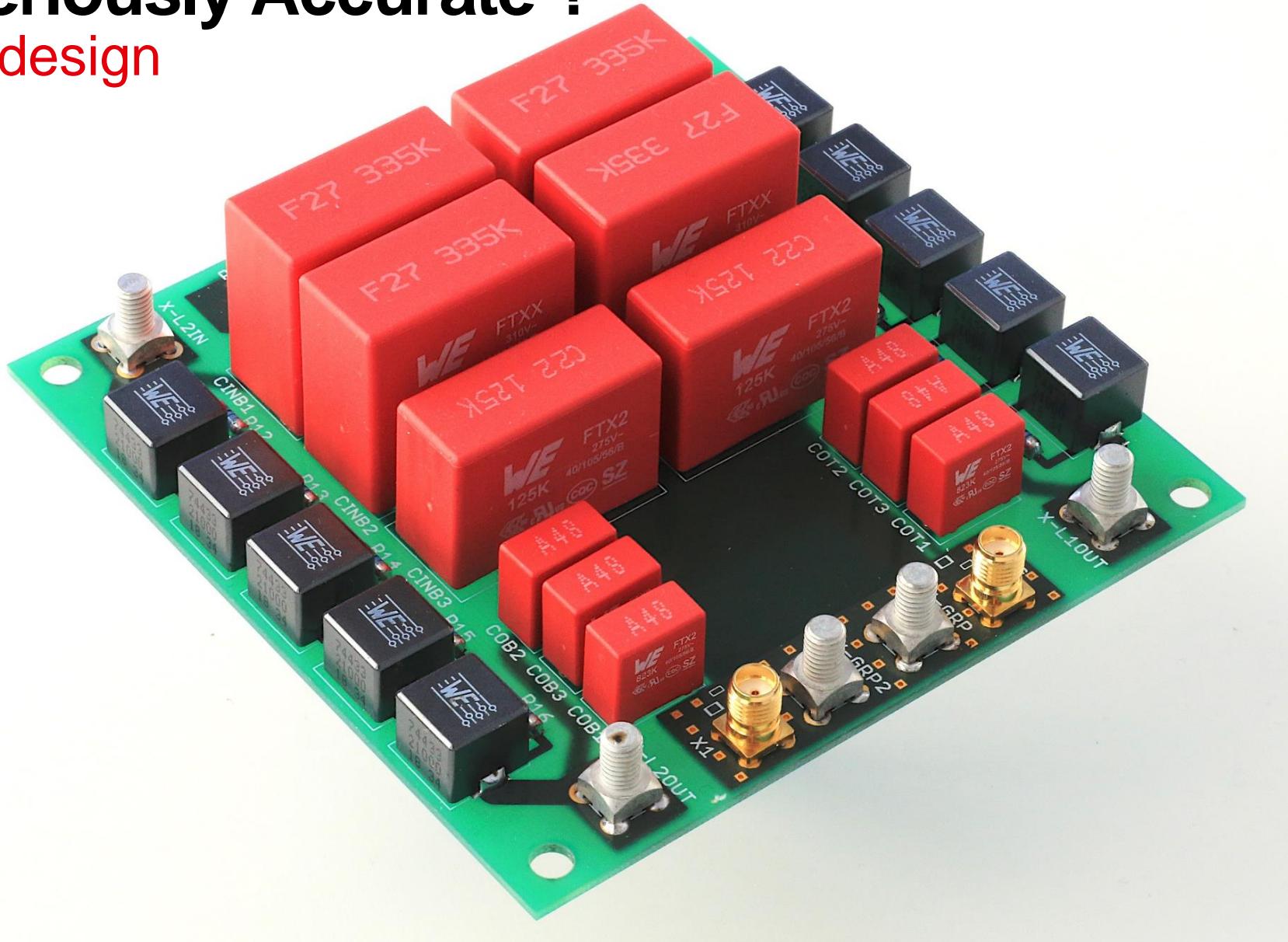
Getting Seriously Accurate ?

Actual LISN design



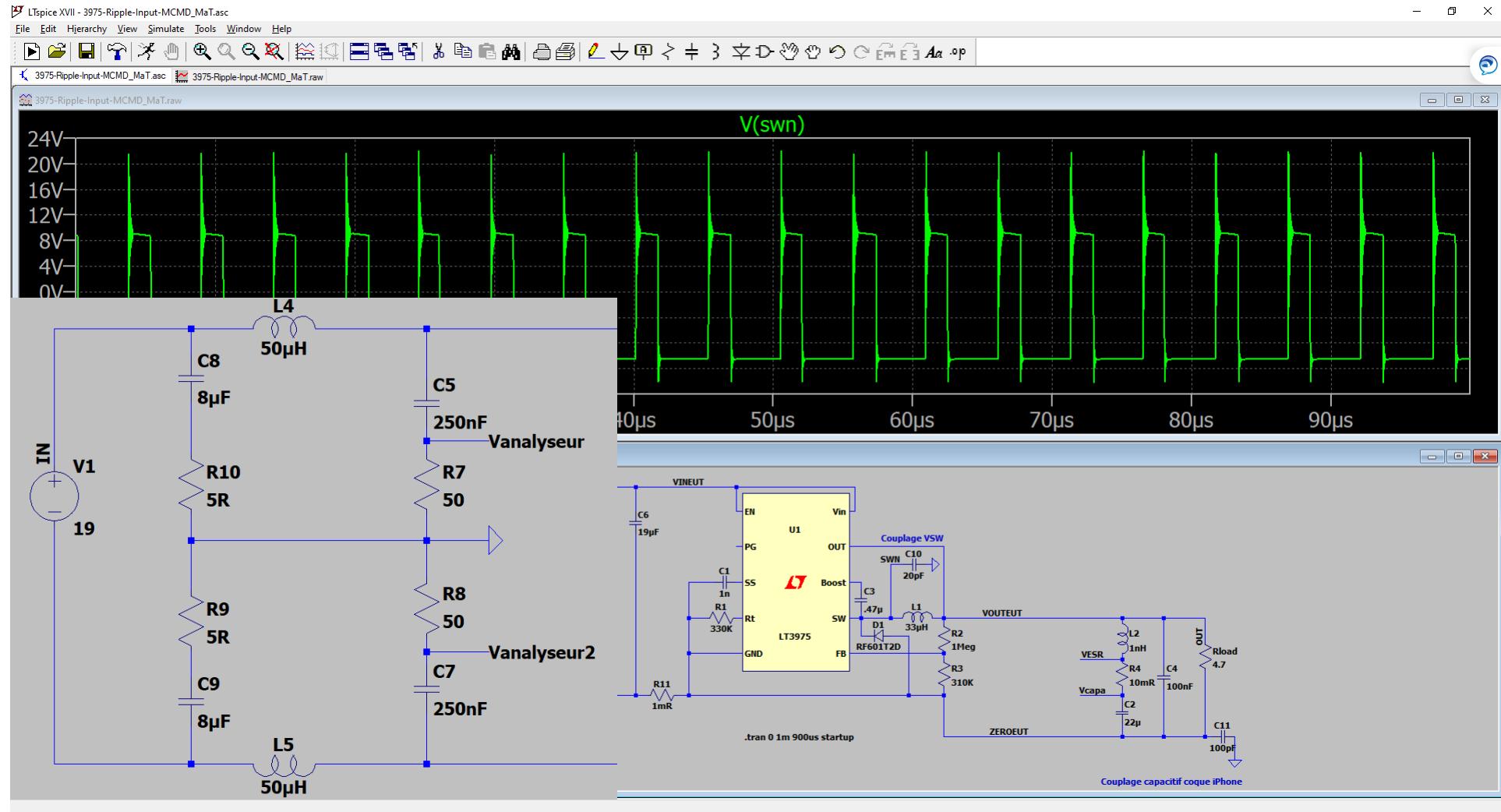
Getting Seriously Accurate ?

Actual LISN design



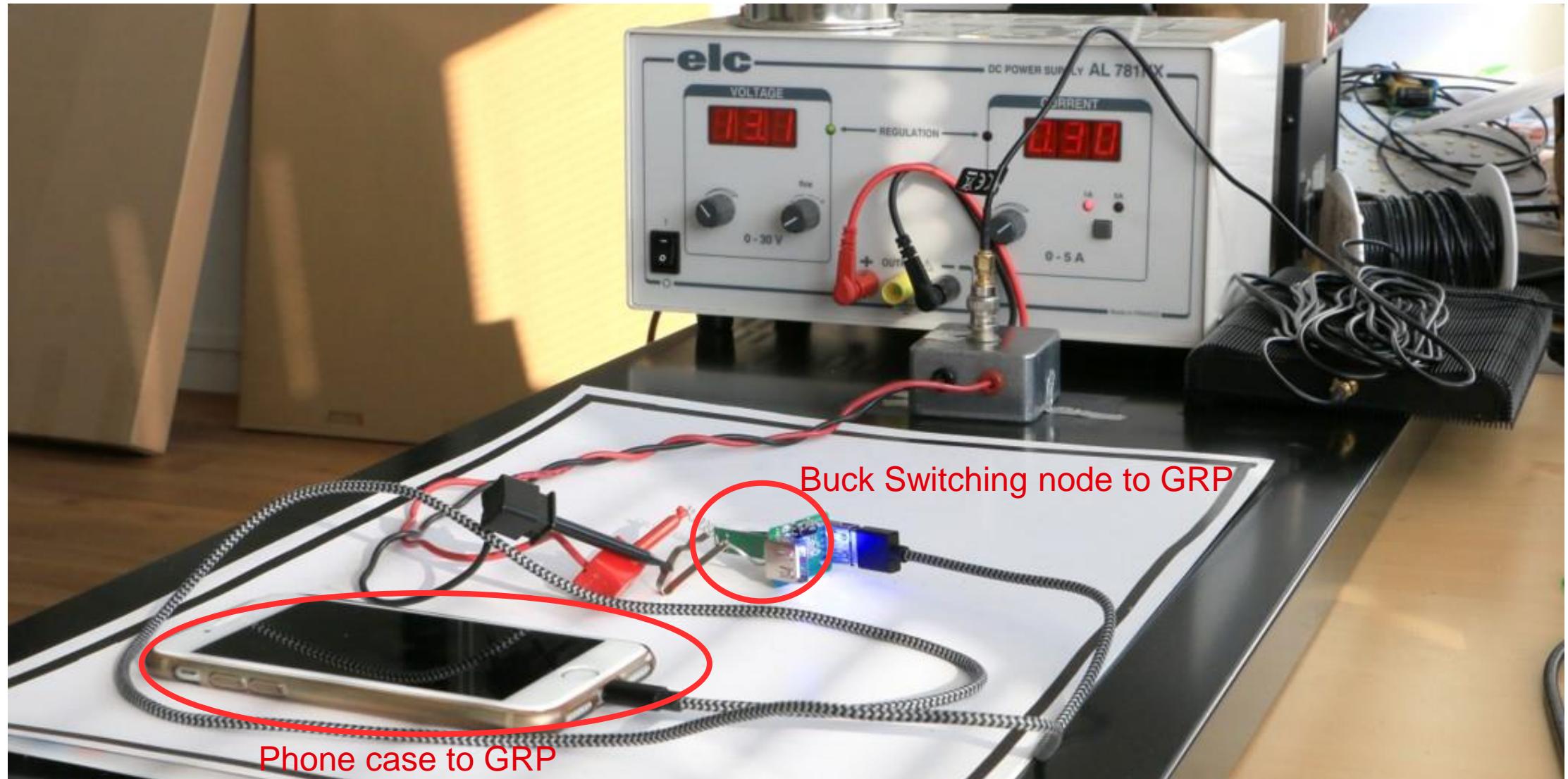
Getting Seriously Accurate ?

Simulation Ready LISN design



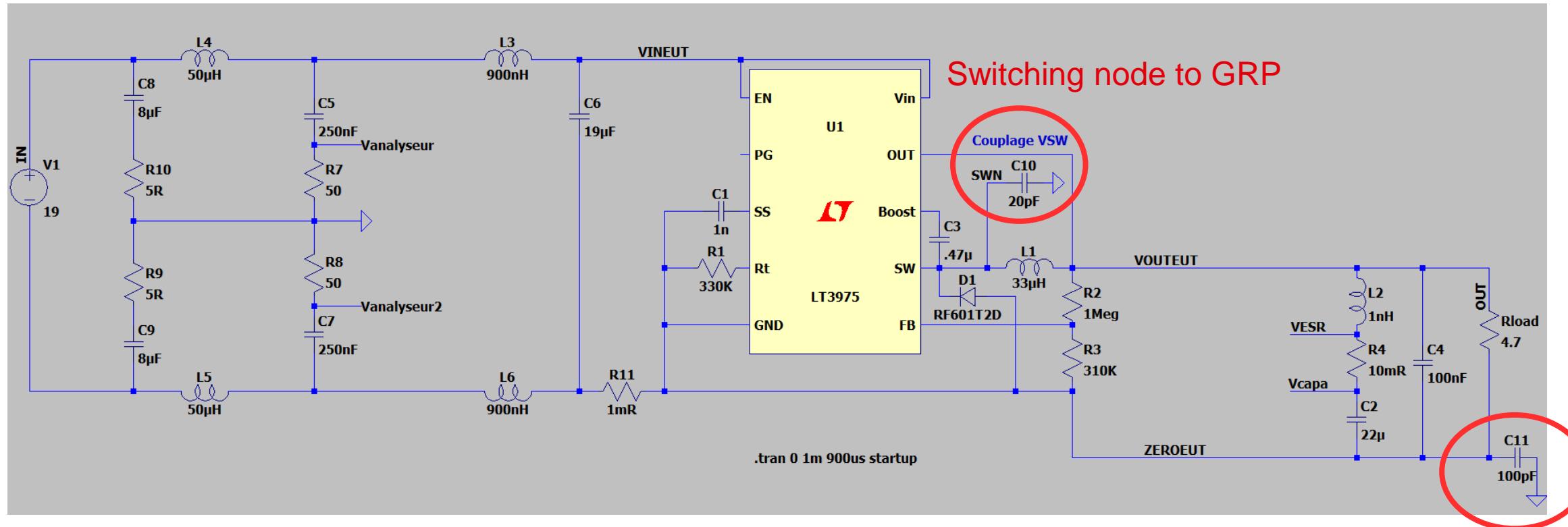
Getting Seriously Accurate ?

Adding E-Field parasitic coupling



Getting Seriously Accurate ?

Adding E-Field parasitic coupling



Phone case to GRP

Getting Seriously Accurate ?

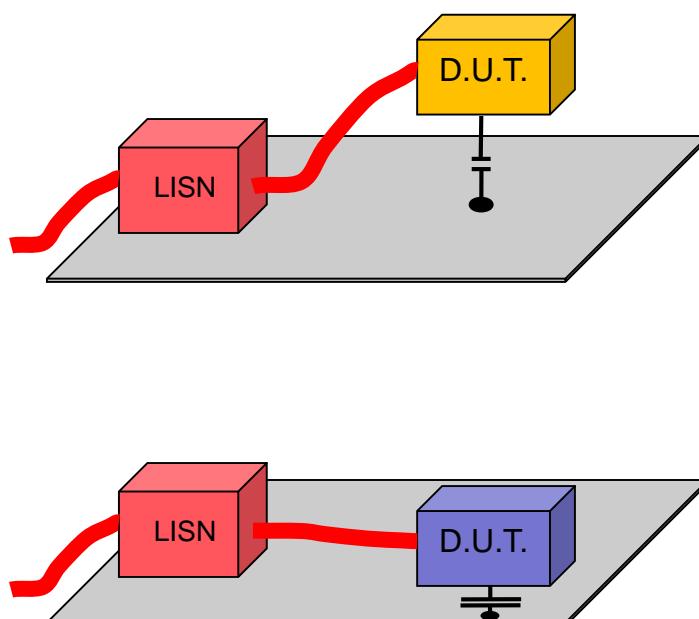
Reality VS Simulation



Frequency Scan

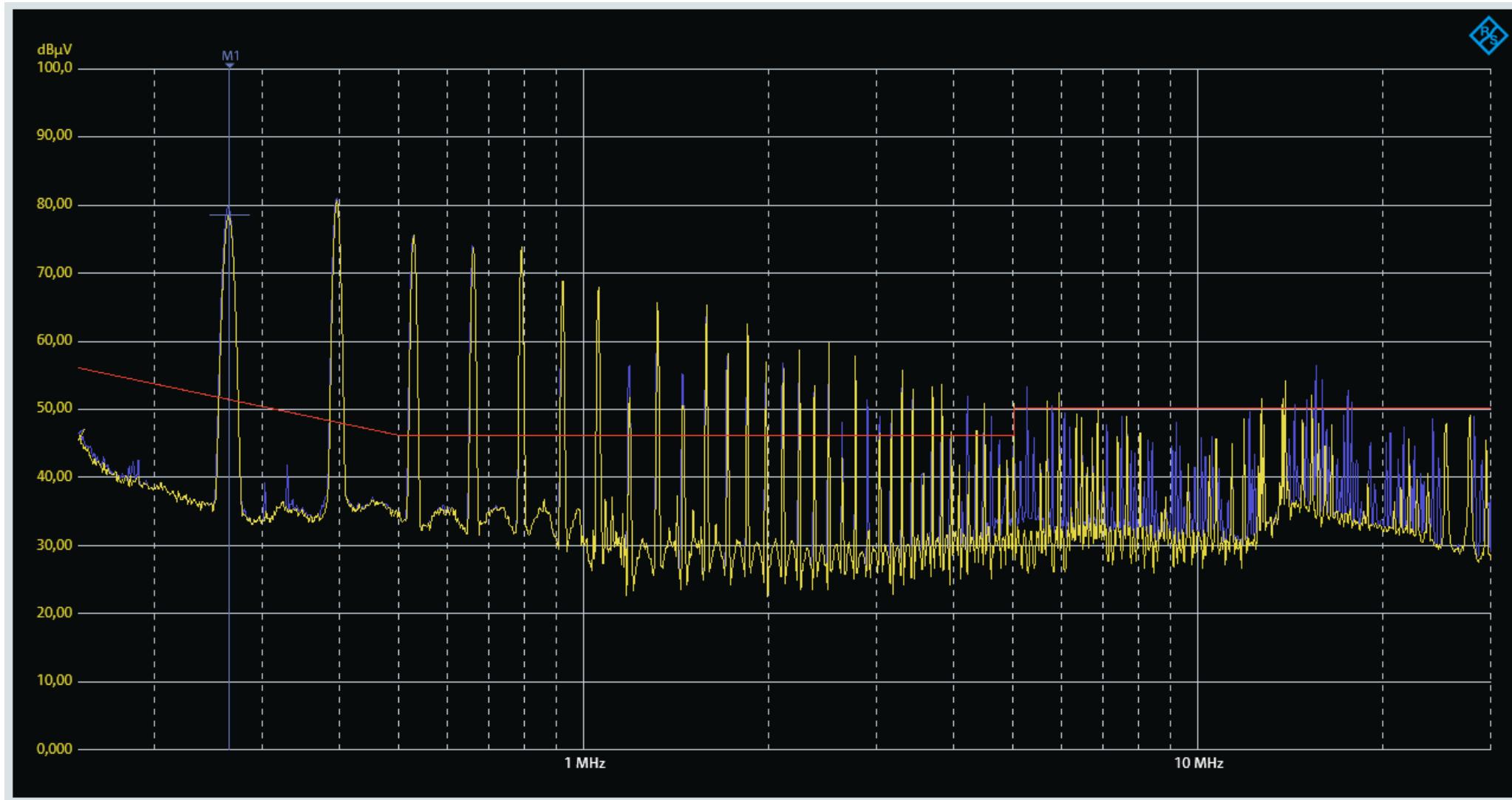
Ref Level 80 dB μ V
 □ RF Attenuator 10 dB
 RBW 100 kHz
 Start Frequency 150 kHz
 Stop Frequency 30 MHz

Measurement Time 10 ms
 Trace Mode Clear / Write
 Trigger Mode Free Run
 Trace Detector Average
 Scan step 0,5 %



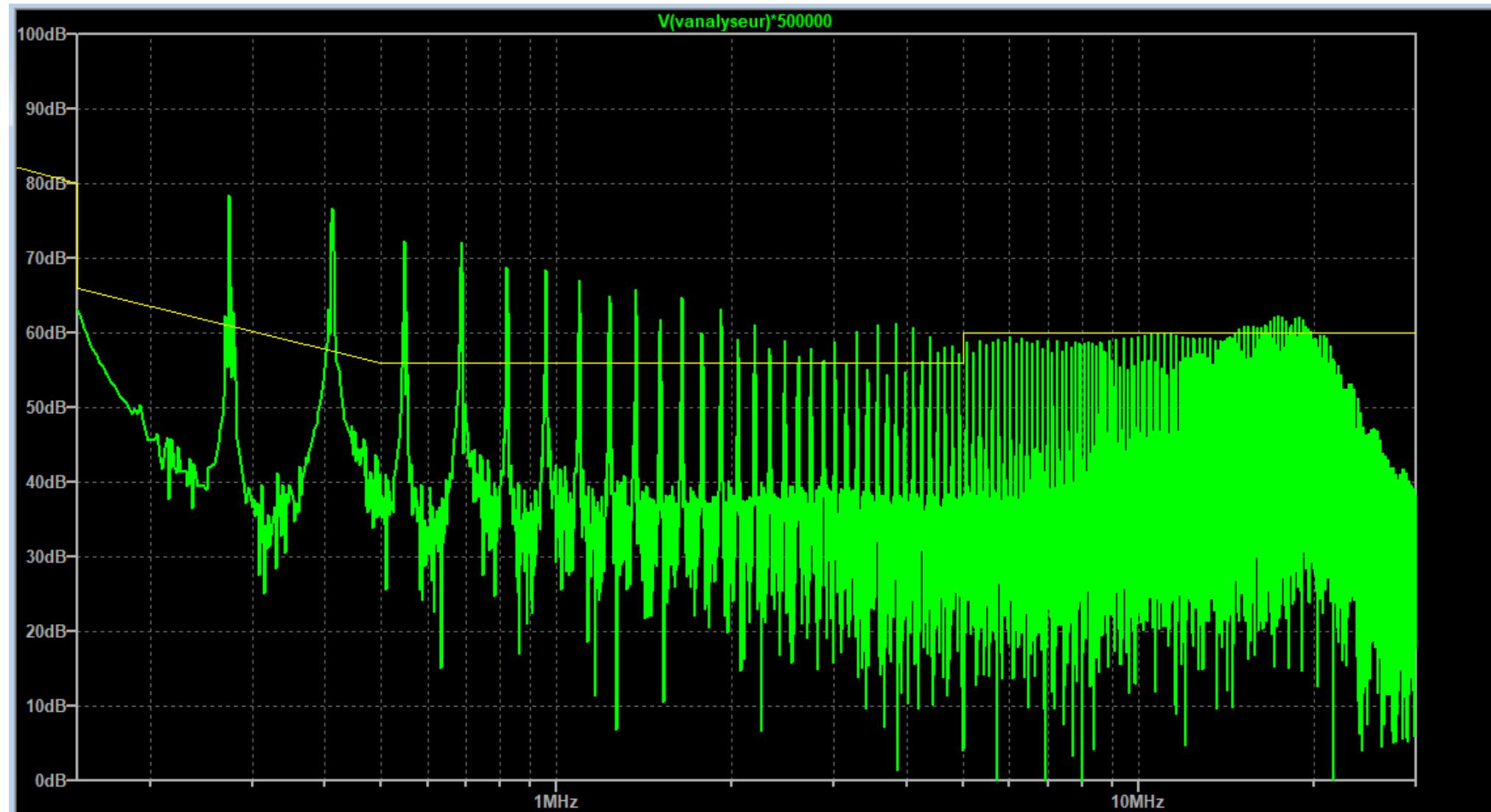
Getting Seriously Accurate ?

Reality VS Simulation



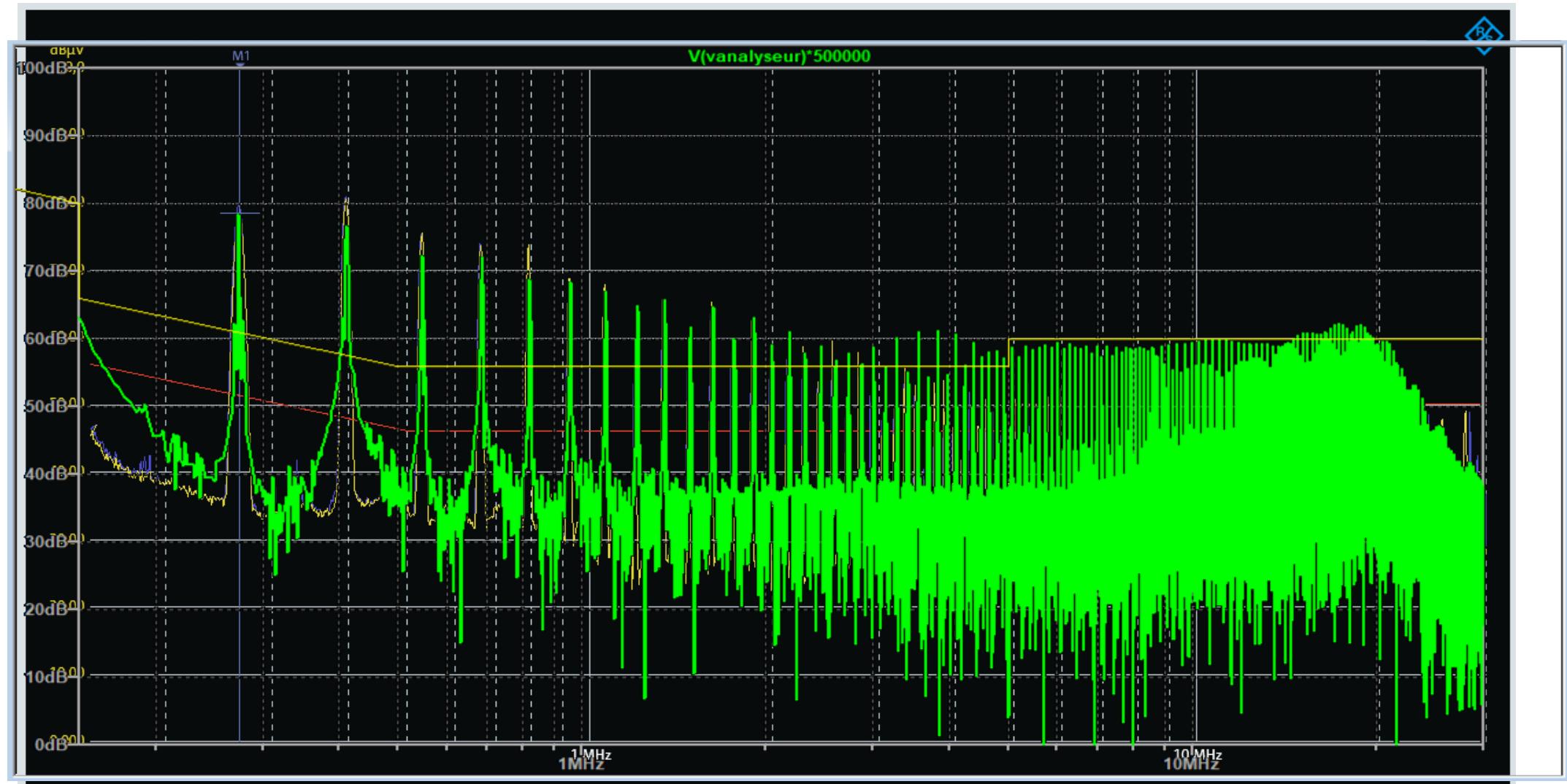
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Reality VS Simulation



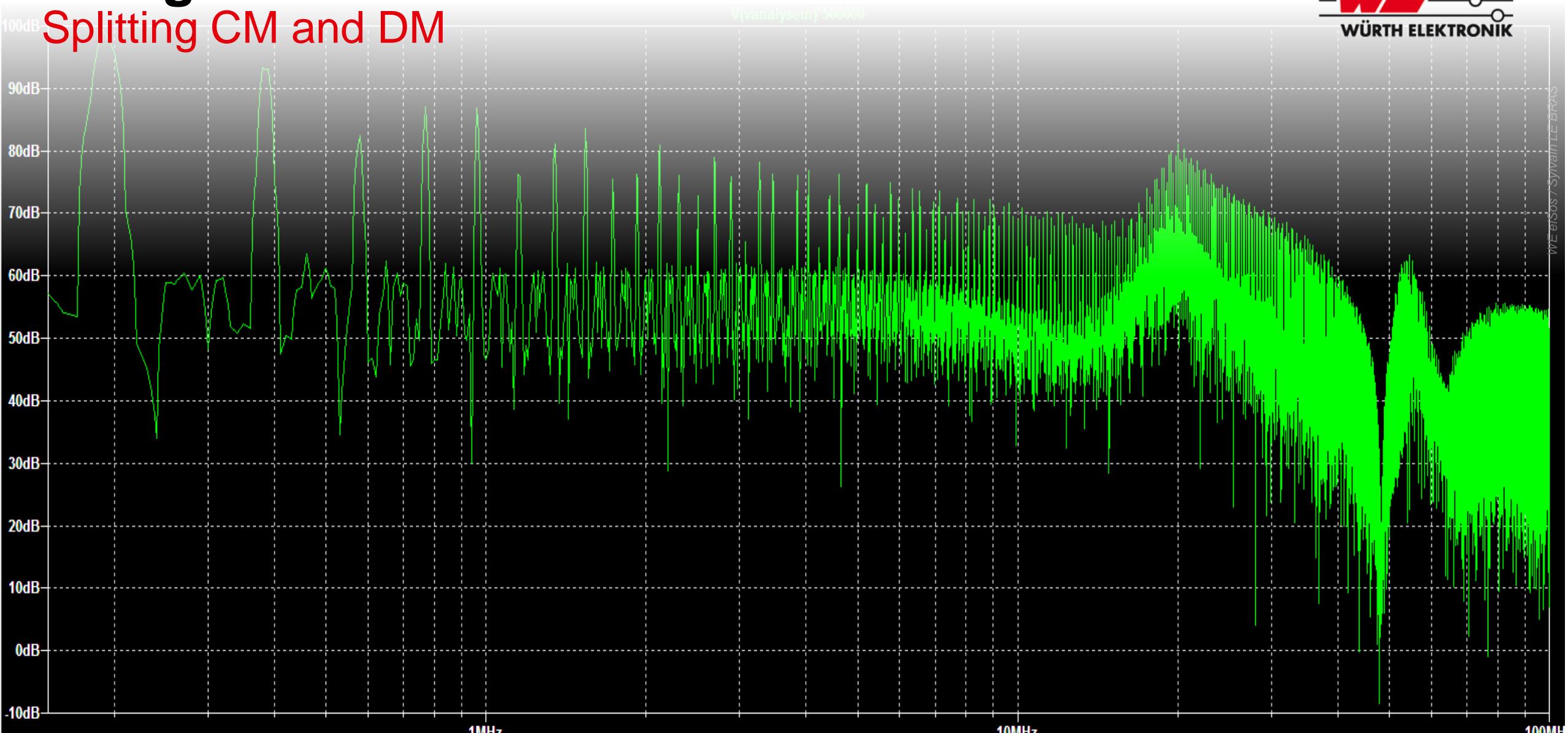
Getting Seriously Accurate ?

Reality VS Simulation



Going further with simulation

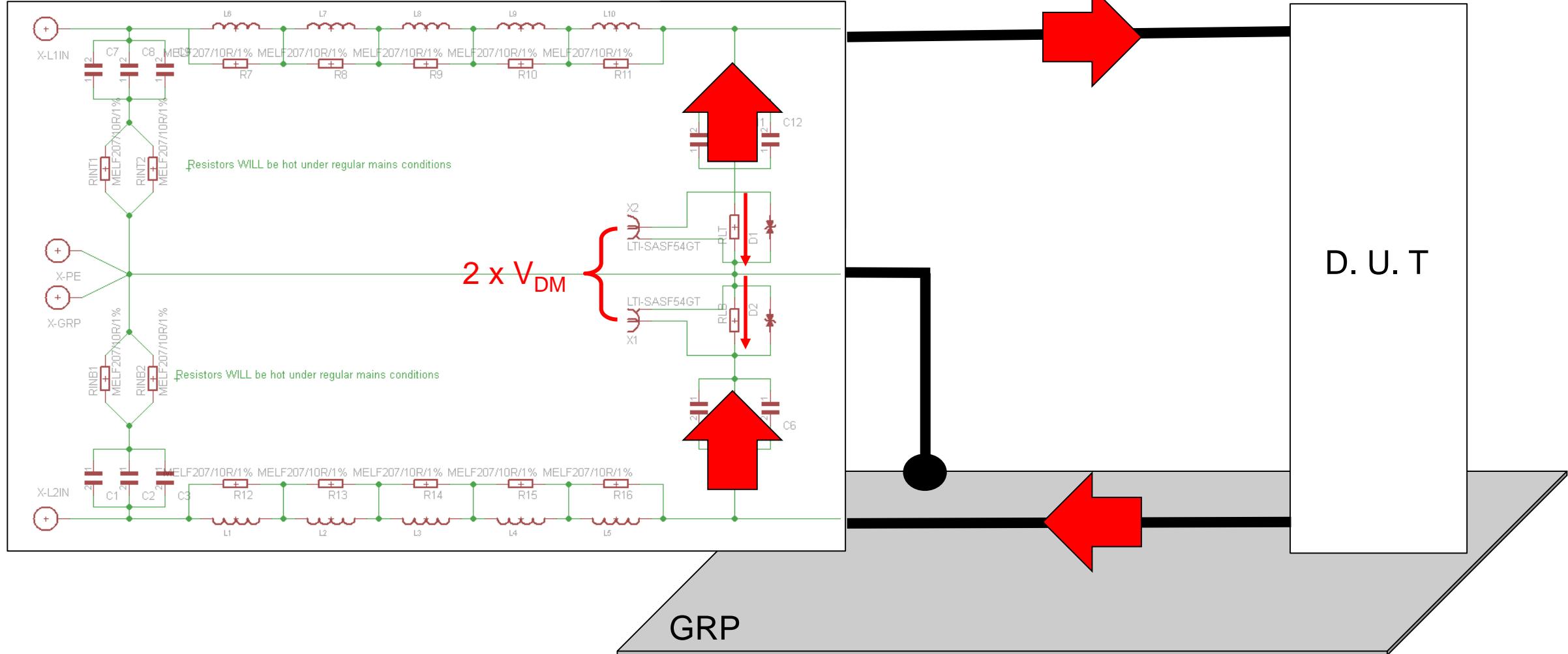
Splitting CM and DM



Going further with simulation

Splitting CM and DM

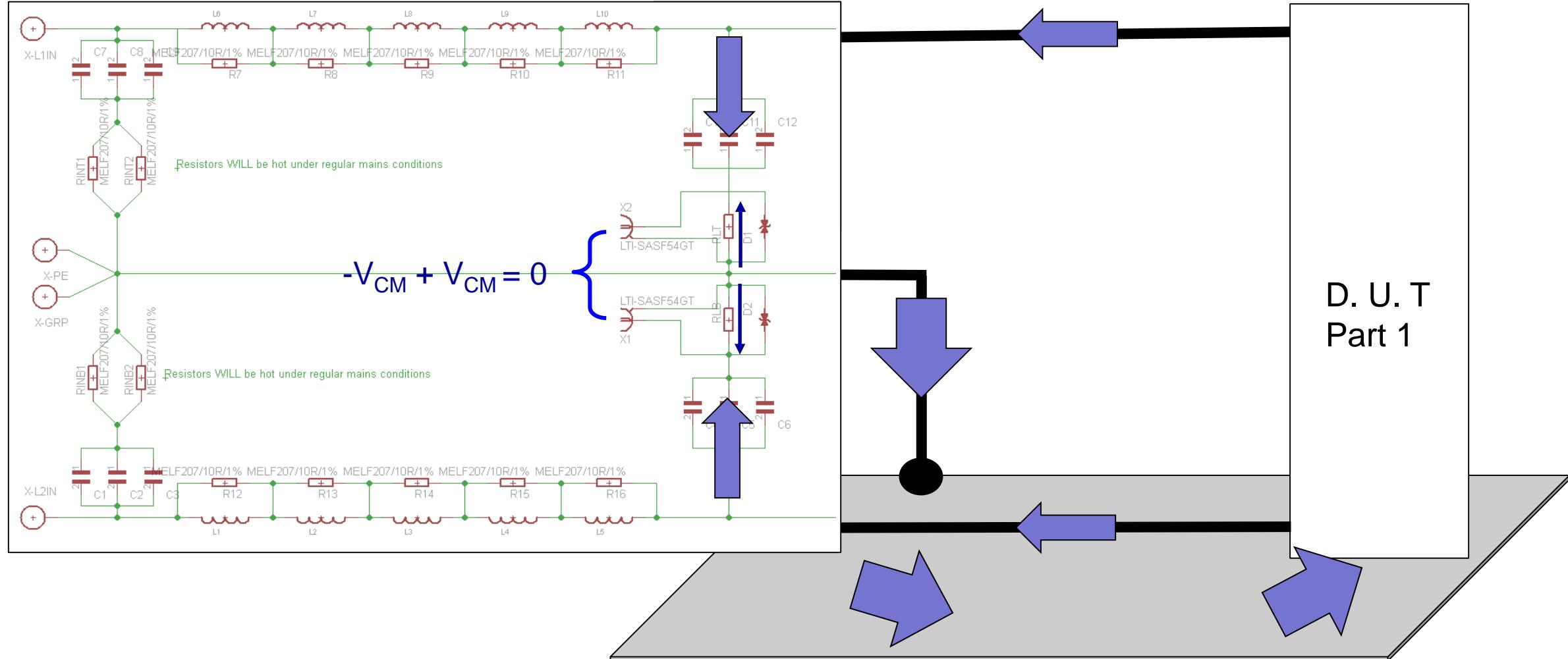
- Symetrical interference ?



Going further with simulation

Splitting CM and DM

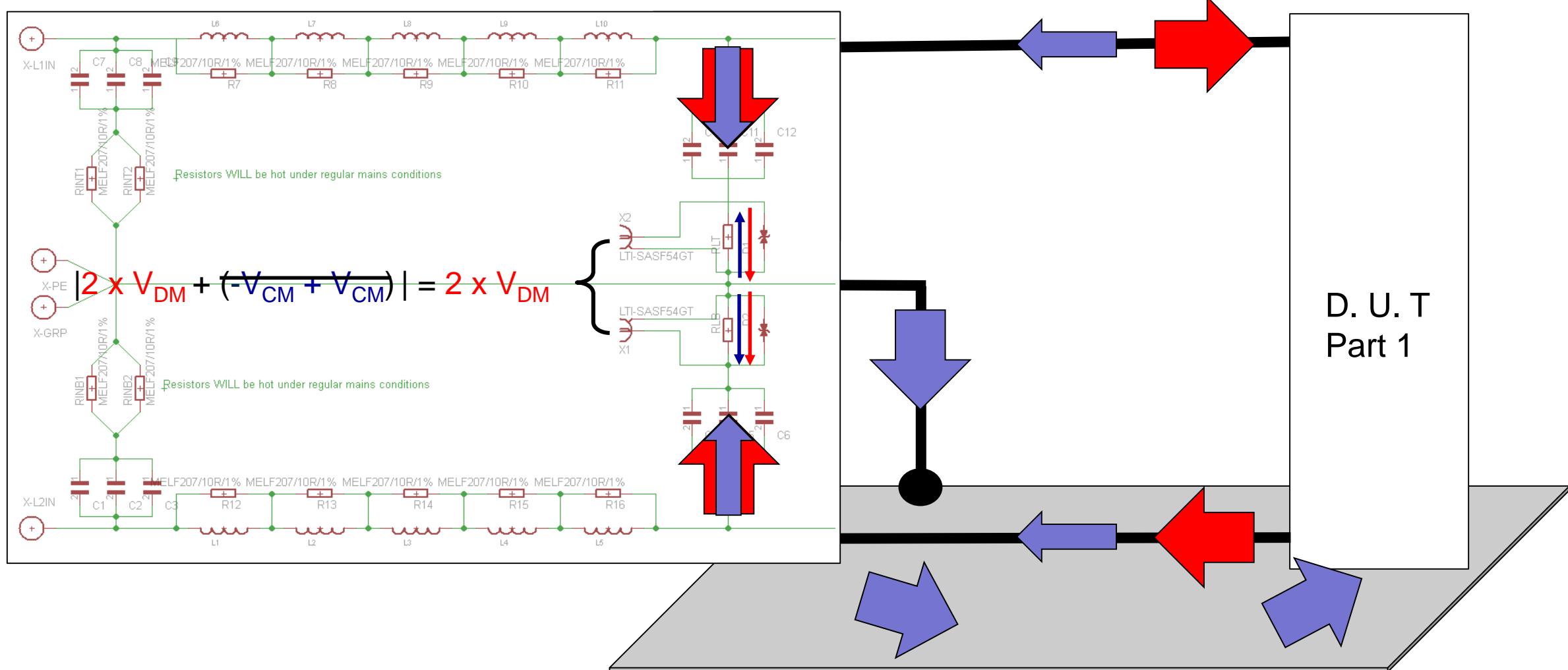
- Asymmetrical interference ?



Going further with simulation

Splitting CM and DM

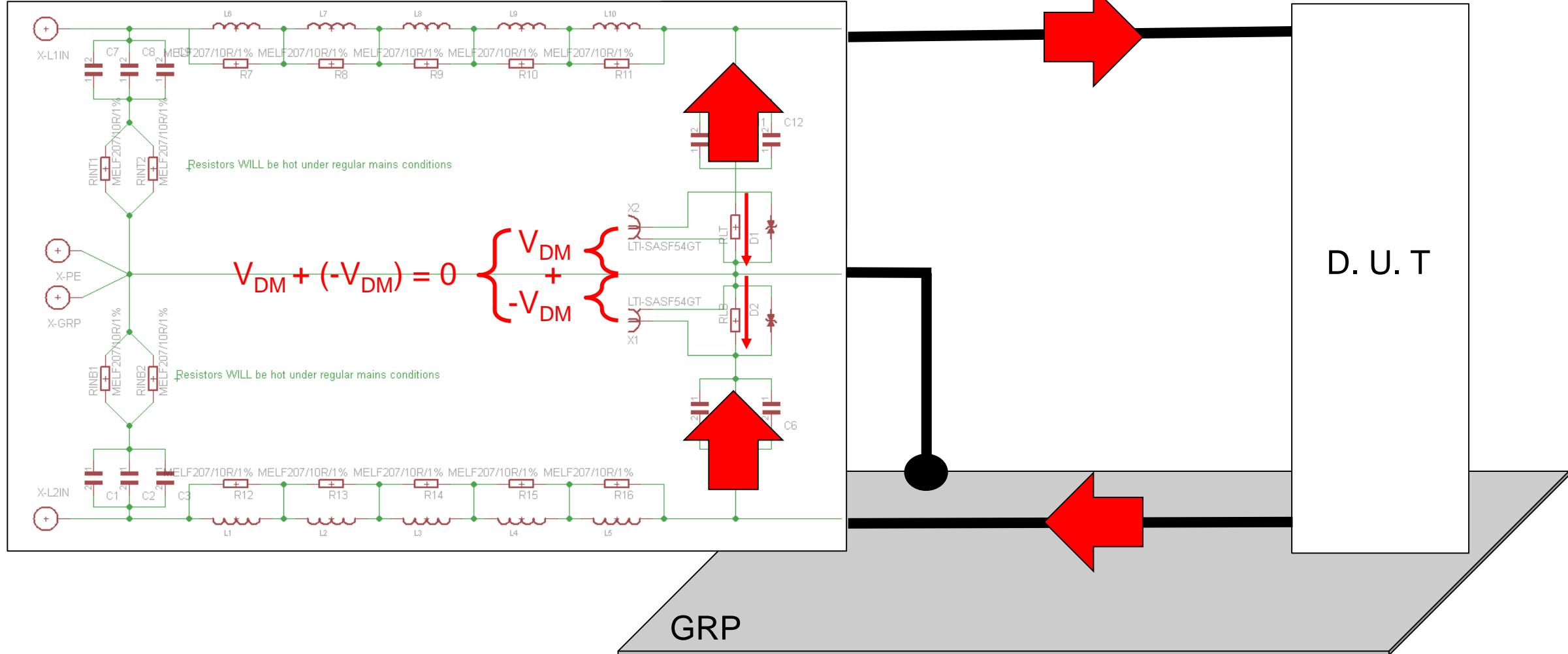
- Asymmetrical interference ?



Going further with simulation

Splitting CM and DM

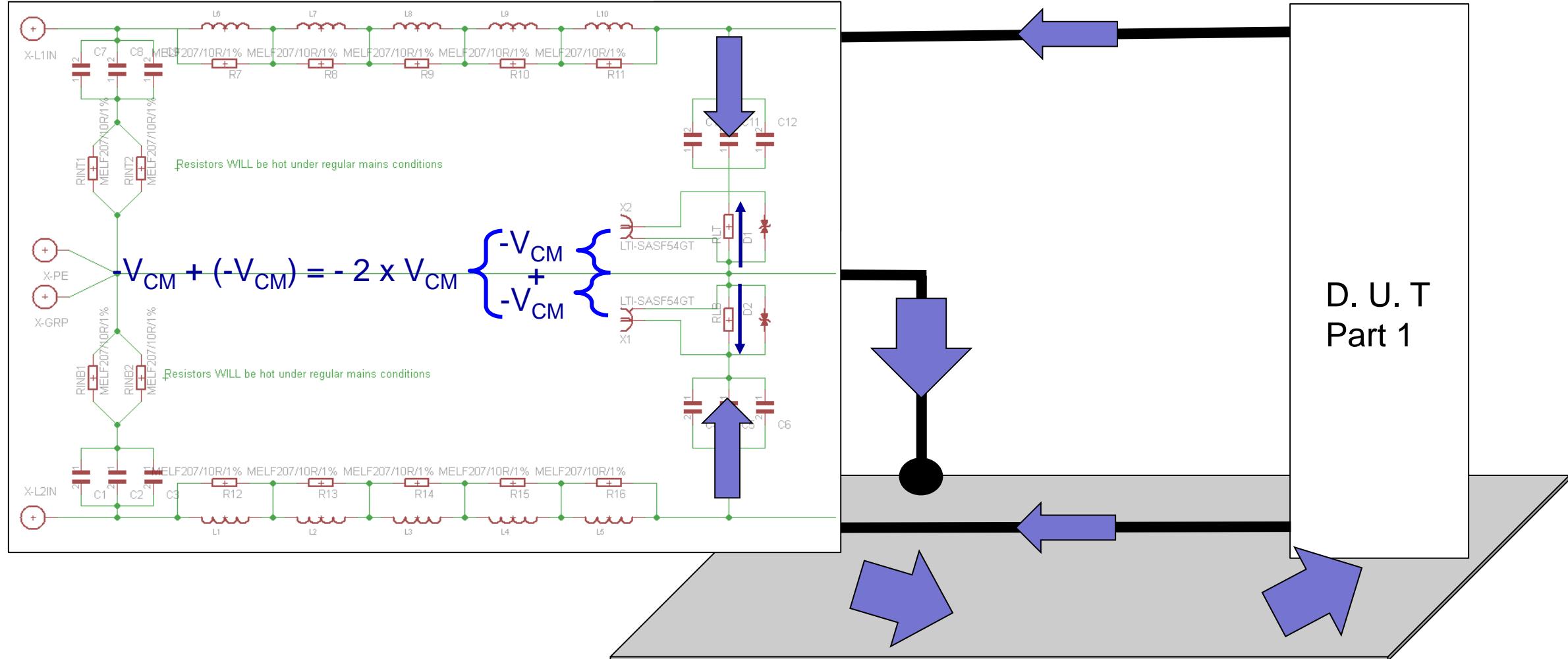
■ Symetrical interference ?



Going further with simulation

Splitting CM and DM

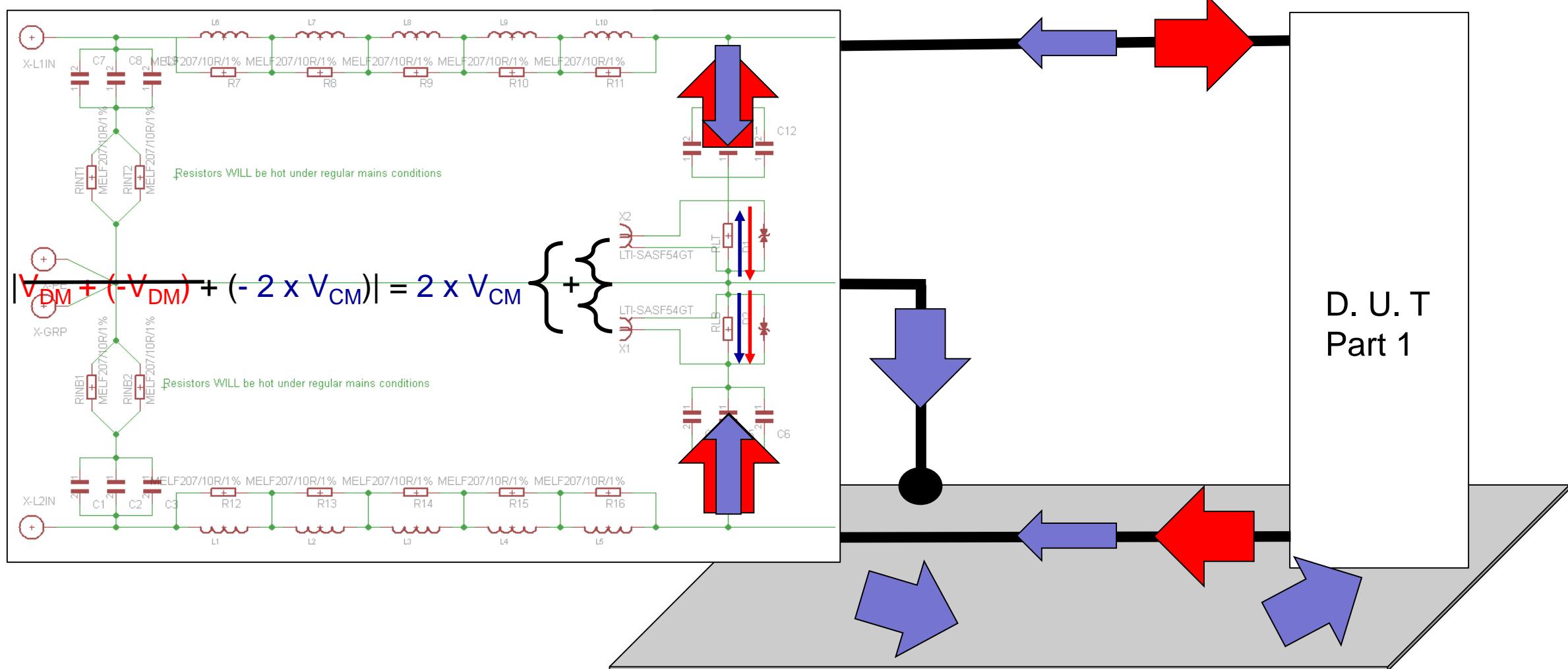
- Asymetrical interference ?



Going further with simulation

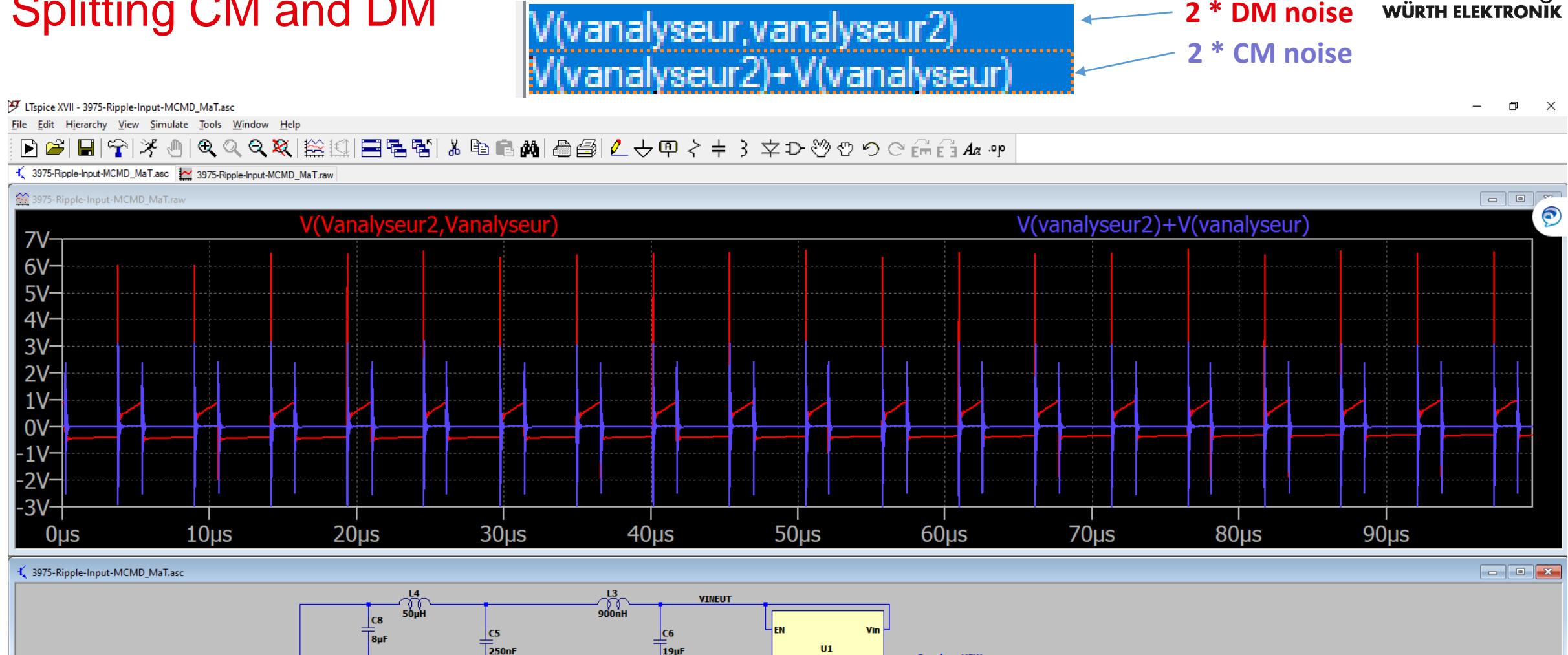
Splitting CM and DM

- Asymetrical interference ?



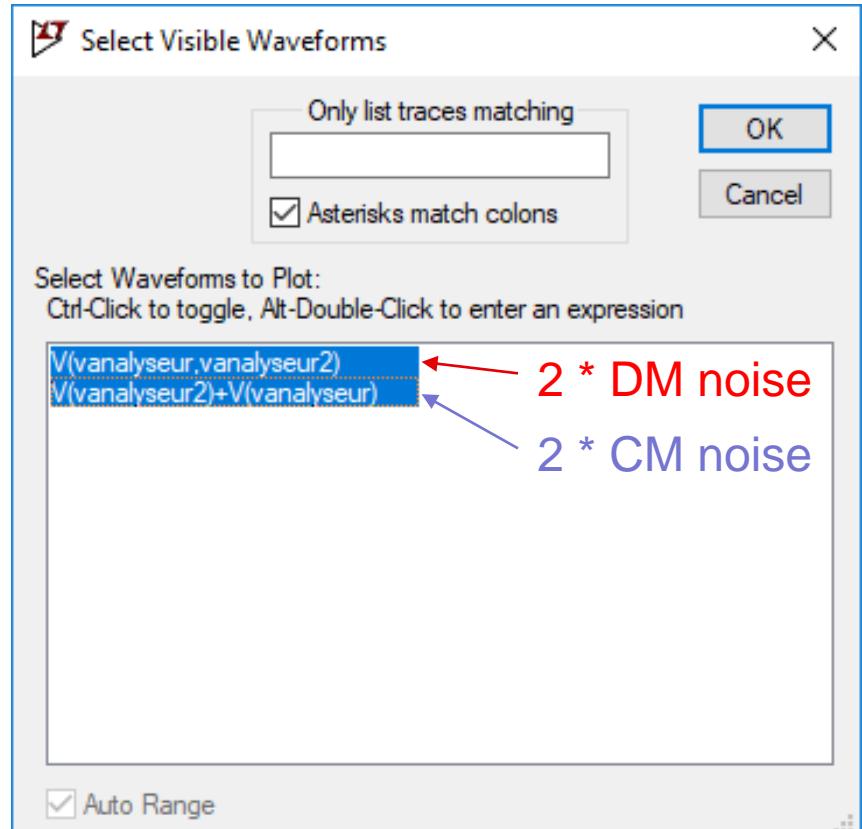
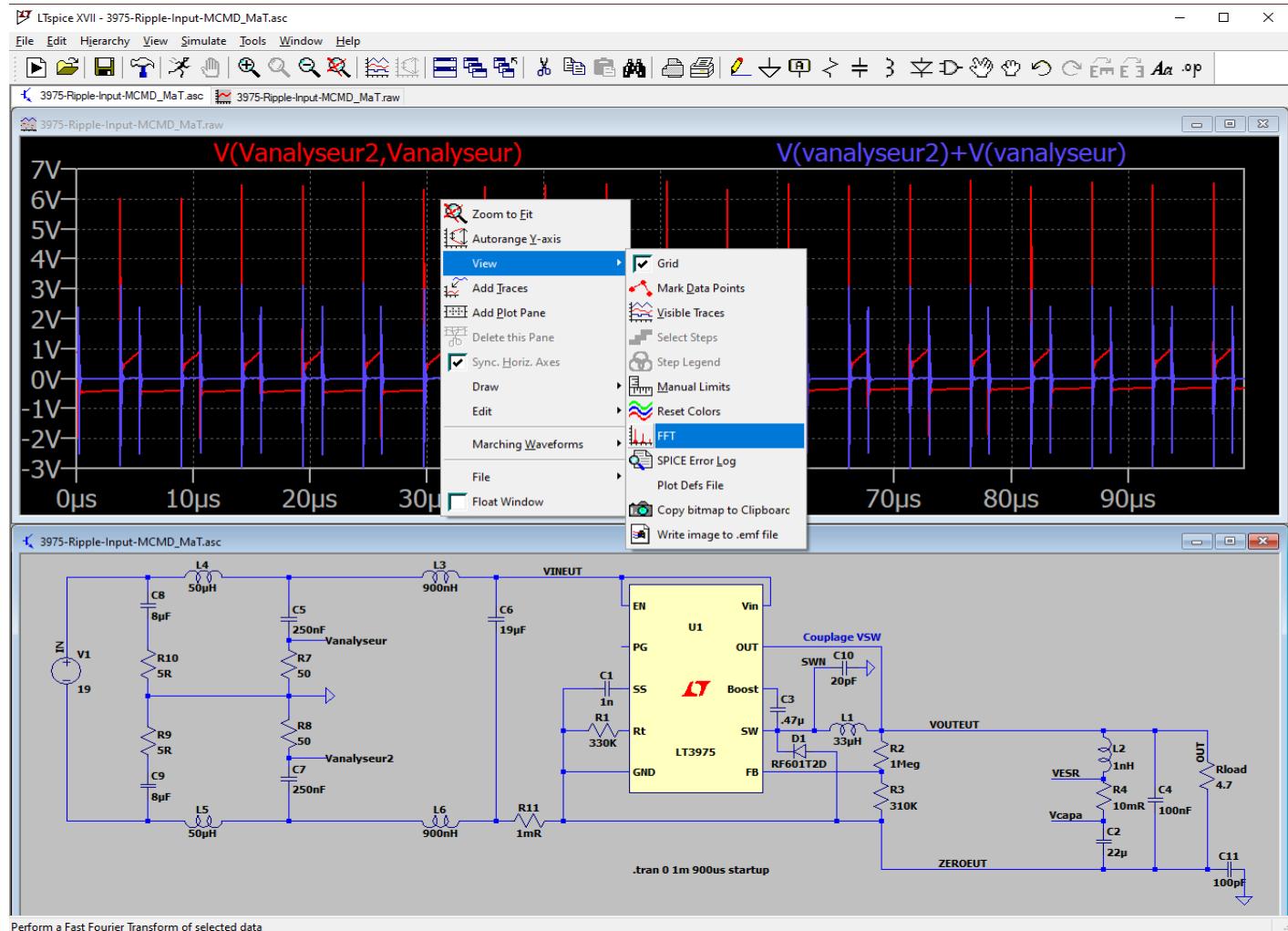
Going further with simulation

Splitting CM and DM



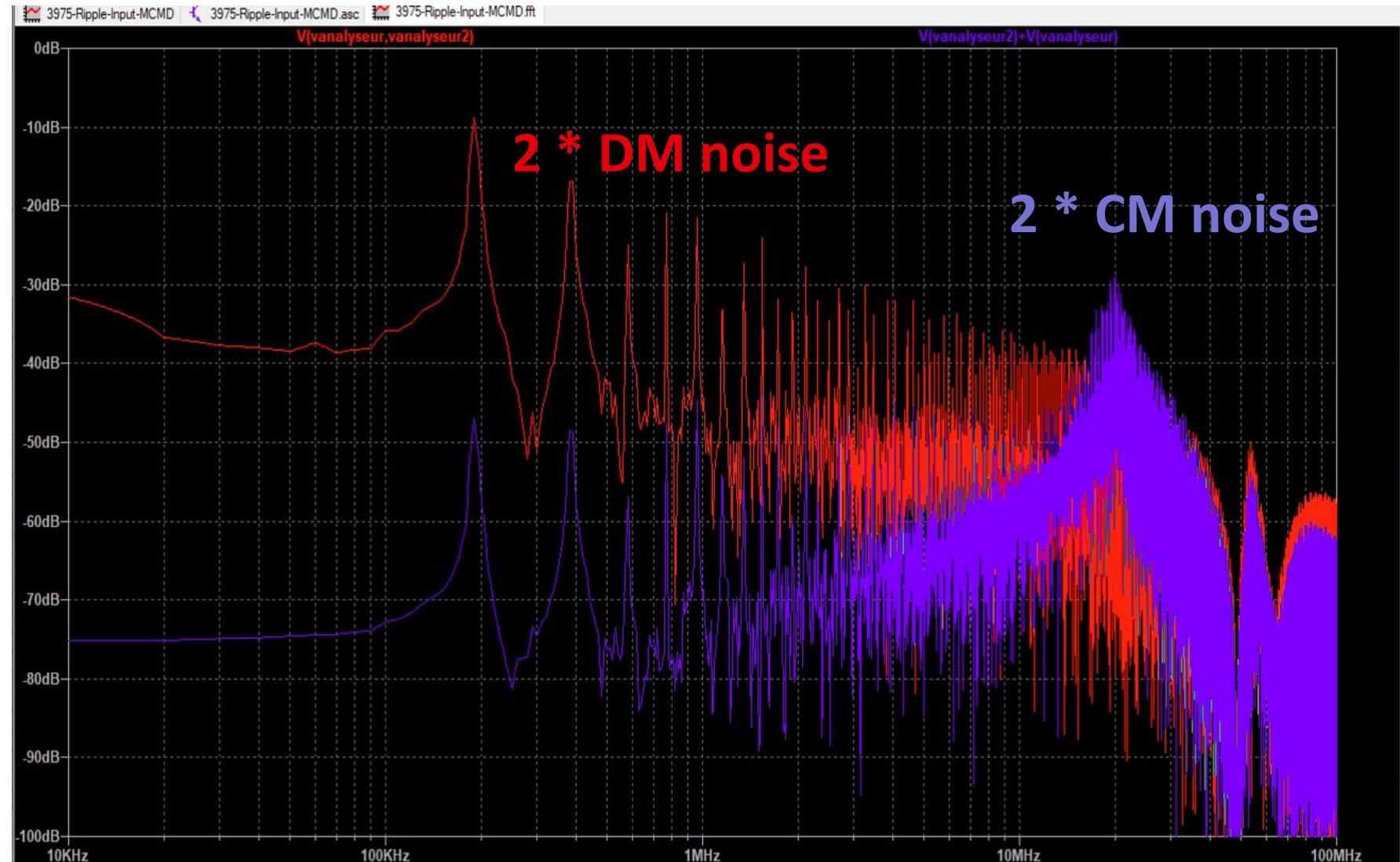
Going further with simulation

Splitting CM and DM



Going further with simulation

Splitting CM and DM

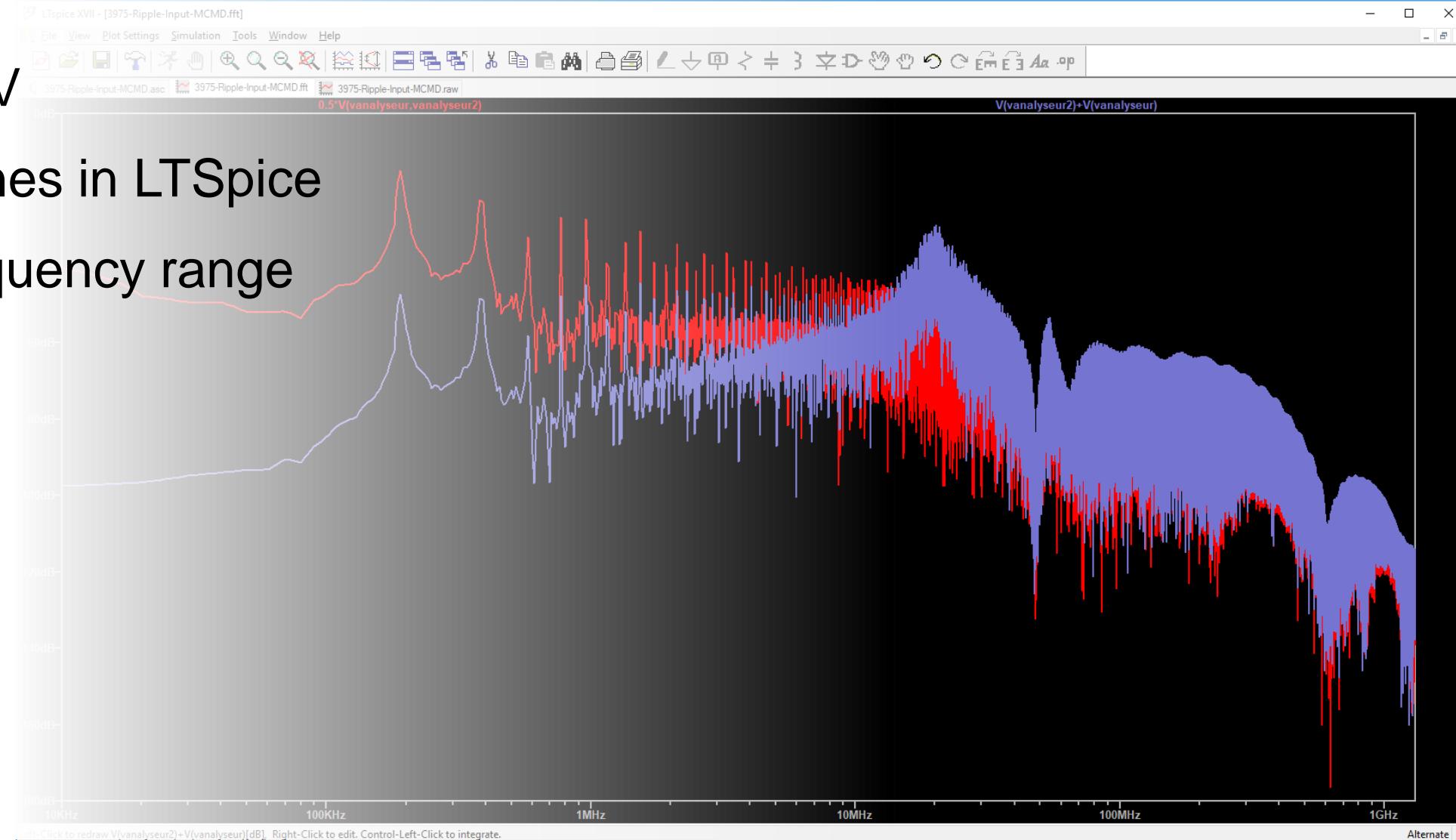


Going further with simulation

Making simulation look real

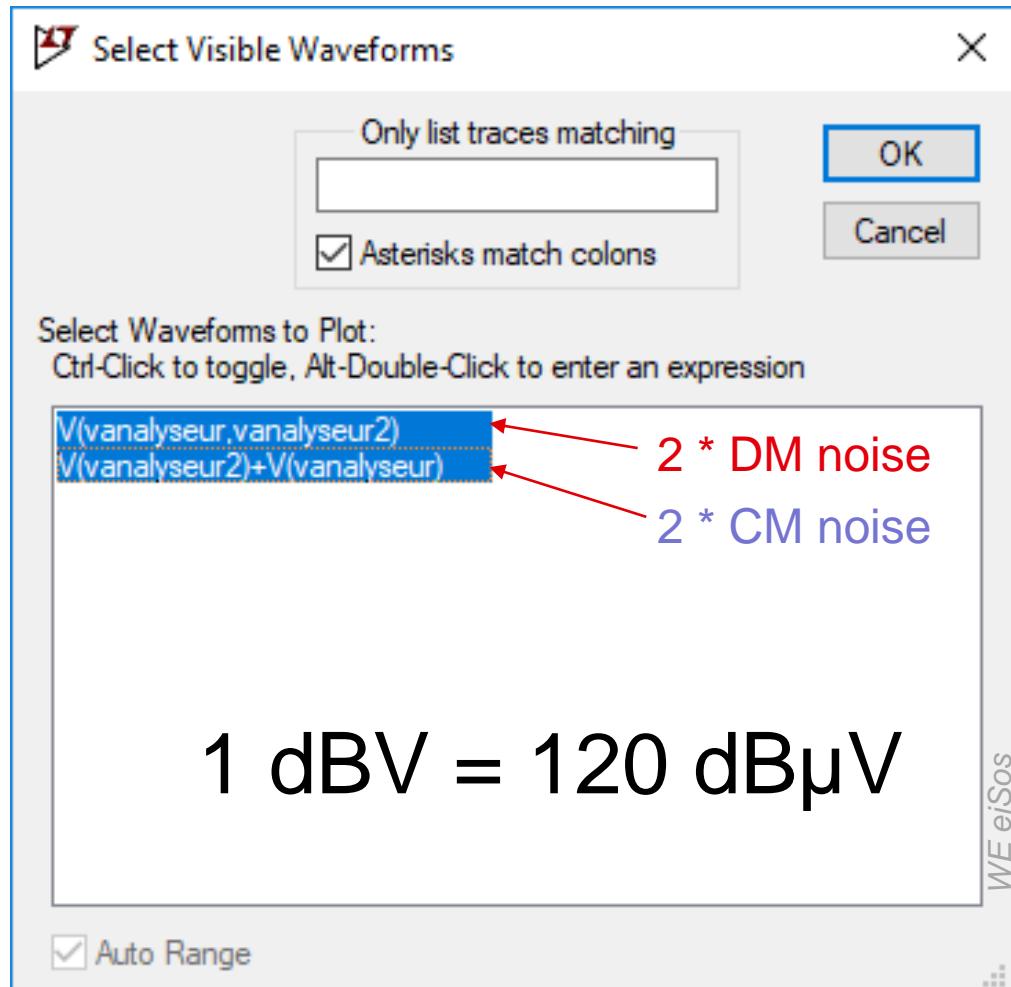


- Scaling to dB μ V
- Loading limit lines in LTSpice
- Defining a Frequency range



Going further with simulation

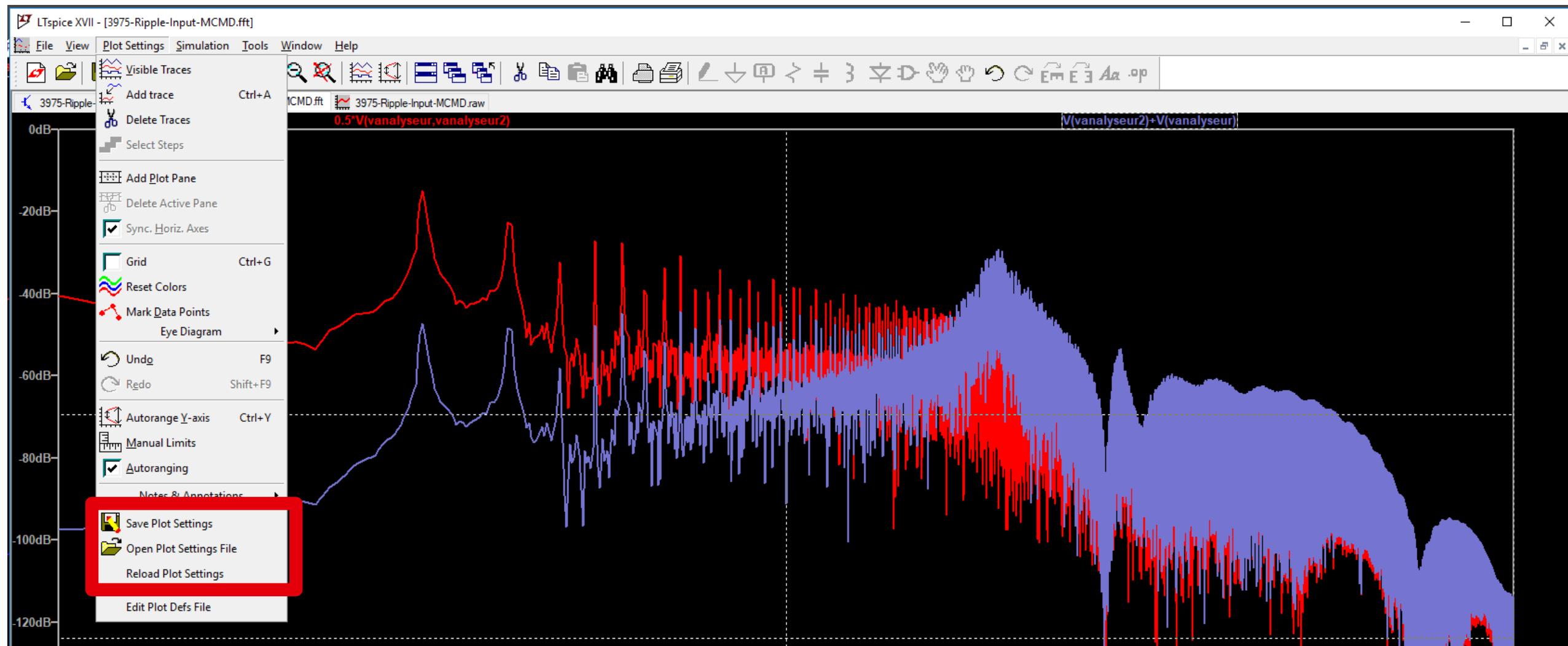
Making simulation look real



$$1 \text{ dBV} = 120 \text{ dB}\mu\text{V}$$

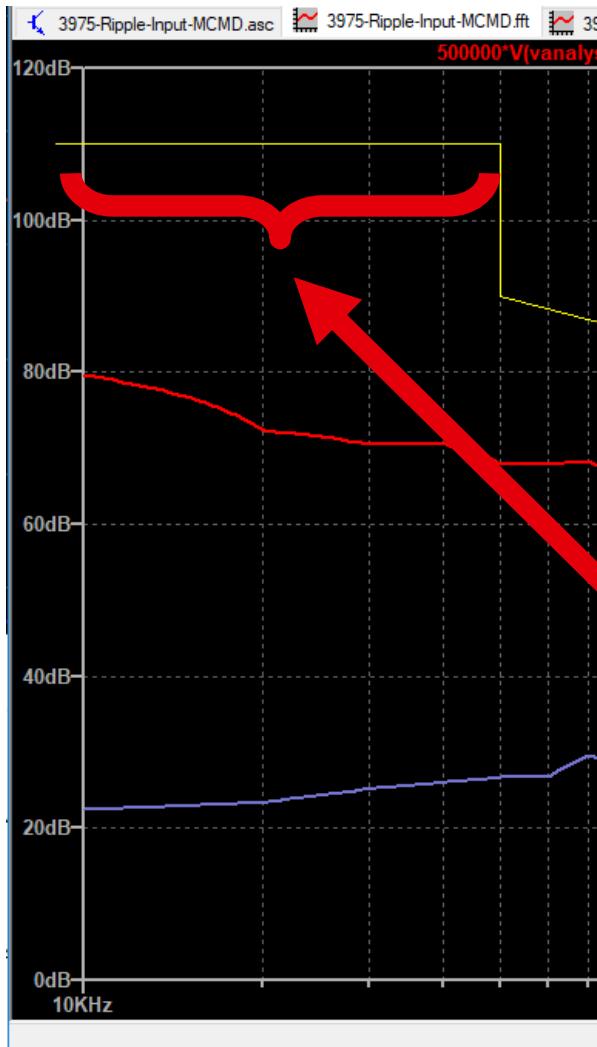
Going further with simulation

Making simulation look real



Going further with simulation

Making simulation look real – Adding limit lines



Line	Start	End	Amp dB μ V start	Amp dB μ V stop	Line def for LTSPICE
Line 1	1	9000	50000	110	110 (9000,0.316227766016838) (50000,0.316227766016838)
Line 2	2	50000	150000	90	80 (50000,0.0316227766016838) (150000,0.01)
Line 3	3	150000	500000	66	56 (150000,0.00199526231496888) (500000,0.000630957344480192)
Line 4	4	500000	5000000	56	56 (500000,0.000630957344480192) (5000000,0.000630957344480192)
Line 5	5	5000000	30000000	60	60 (5000000,0.001) (30000000,0.001)

Fill according to
EMC standards

Copy the result

Paste it here

```
Flyback-example-2-base - Bloc-notes
Fichier Édition Format Affichage Aide
[FFT of time domain data]
{
  Npanes: 1
  {
    traces: 1 {2,0,"V(vanalyseur2)+V(vanalyseur)"}
    X: ('M',0,9000,0,30000000)
    Y[0]: (' ',0,1e-006,10,1)
    Y[1]: (' ',0,-200,40,200)
    Log: 1 2 0
    PltMag: 1
    Line: "dB" 4 0 (9000,0.3162277660168) (50000,0.316227766)
    Line: "dB" 4 0 (50049.8435712172,0.0317065818612387) (150407.110289202,0.0100397786508485)
    Line: "dB" 4 0 (150000,0.00199526231496888) (500000,0.000630957344480192)
    Line: "dB" 4 0 (500000,0.000630957344480192) (5000000,0.000630957344480192)
    Line: "dB" 4 0 (5000000,0.001) (30000000,0.001)
  }
}
```

Windows (CRLF) Ln 10, Col 16 100%

Going further with simulation

Making simulation look real – Defining a range

10kHz to 30 MHz

0 to 120dB μ V

3975-Ripple-Input-MCMD-dbuv.plt - Bloc-notes

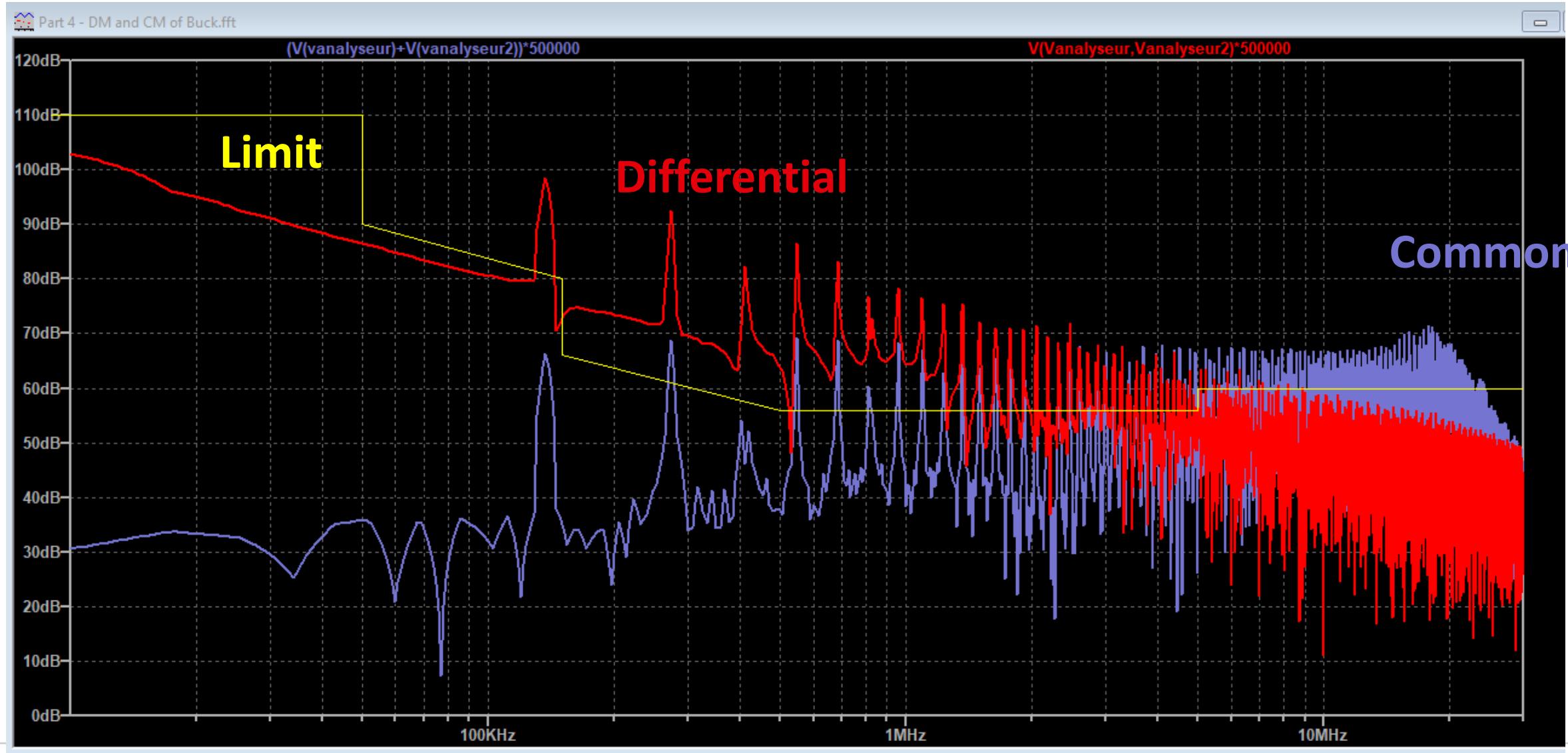
Fichier Edition Format Affichage ?

[FFT of time domain data]

```
{
    Npanes: 1
    {
        traces: 2 {65540,0,"500000*V(vanalyseur,vanalyseur2)"} {65547,0,"1000000*(V(vanalyseur2)+V(vanalyseur))"}
        X: ('M',0,10000,0,3e+007)
        Y[0]: (' ',0,1,20,1e+006)
        Log: 1 2 0
        GridStyle: 1
        PltMag: 1
        Line: "dB" 13 0 (8983.92329505352,319040.747263751) (49889.5367382049,319040.747263751)
        Line: "dB" 13 0 (50000,316227.766016838) (50000,31622.7766016838)
        Line: "dB" 13 0 (50000,31622.7766016838) (150000,10000)
        Line: "dB" 13 0 (150000,10000) (150000,1995.26231496888)
        Line: "dB" 13 0 (150000,1995.26231496888) (500000,630.957344480193)
        Line: "dB" 13 0 (500000,630.957344480193) (5000000,630.957344480193)
        Line: "dB" 13 0 (5000000,630.957344480193) (5000000,1000)
        Line: "dB" 13 0 (5000000,1000) (30000000,1000)
    }
}
```

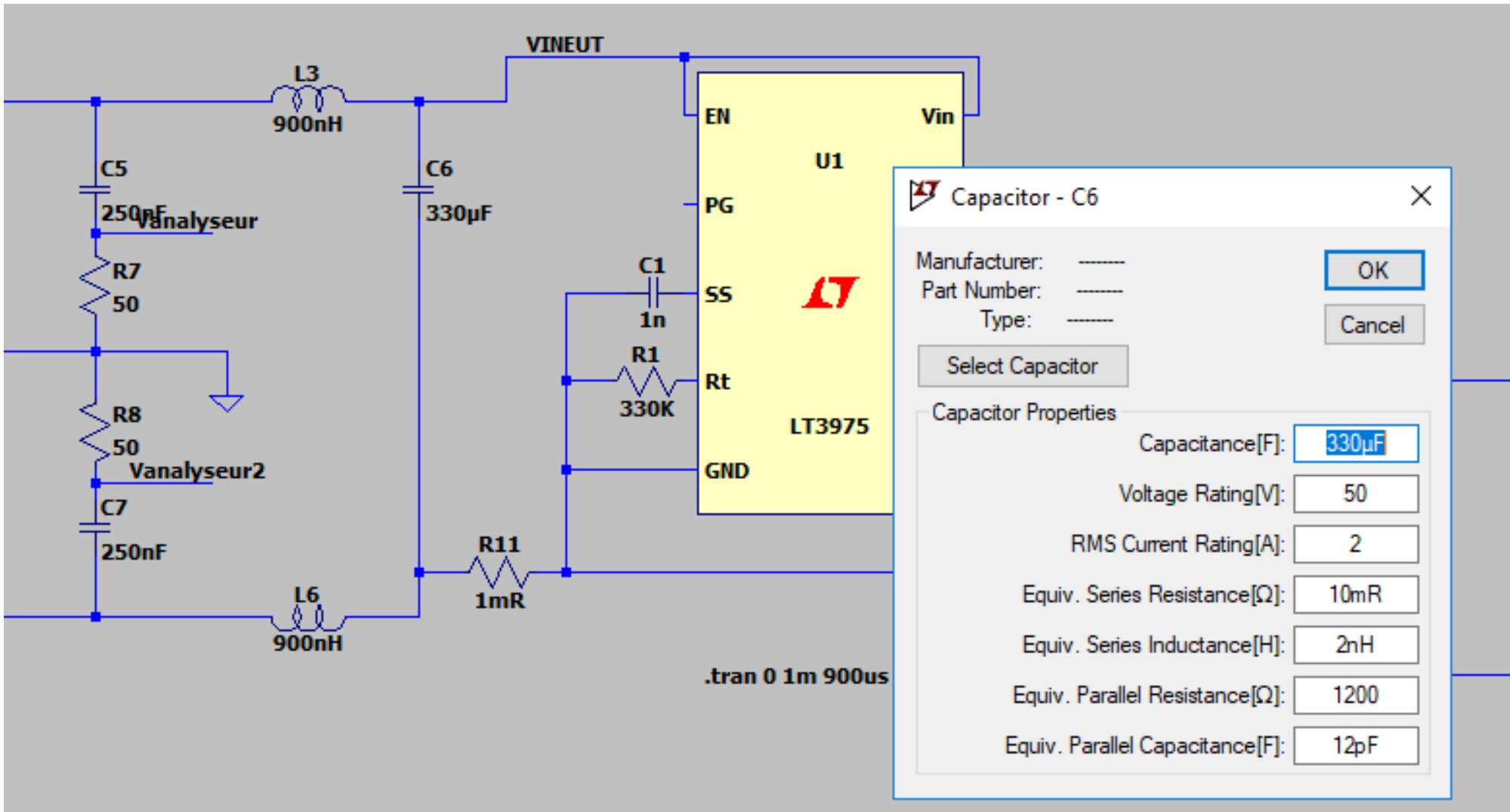
Going further with simulation

Making simulation look real – Result ☺



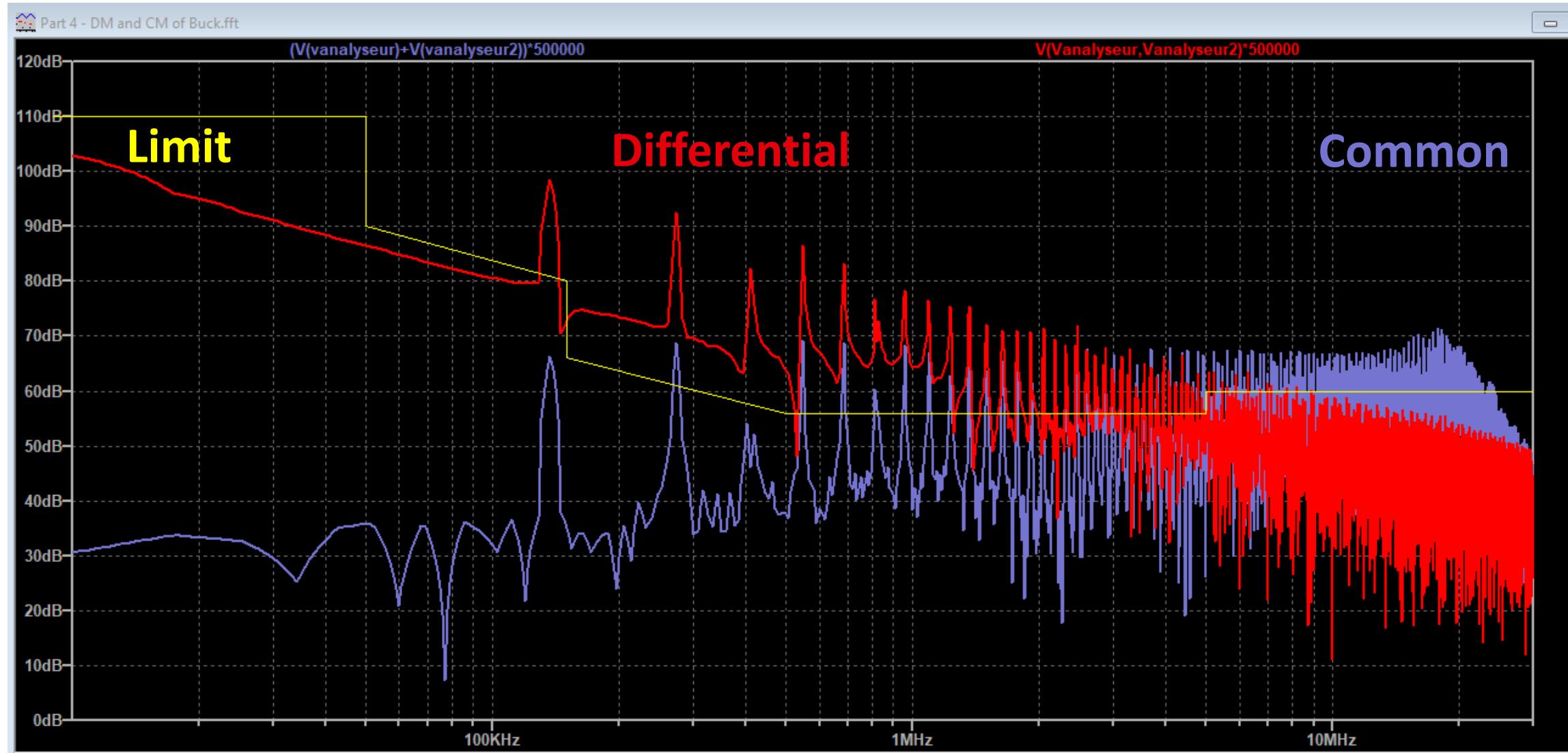
Going further with simulation

Fixing that buck in the simulation – Polymer input cap



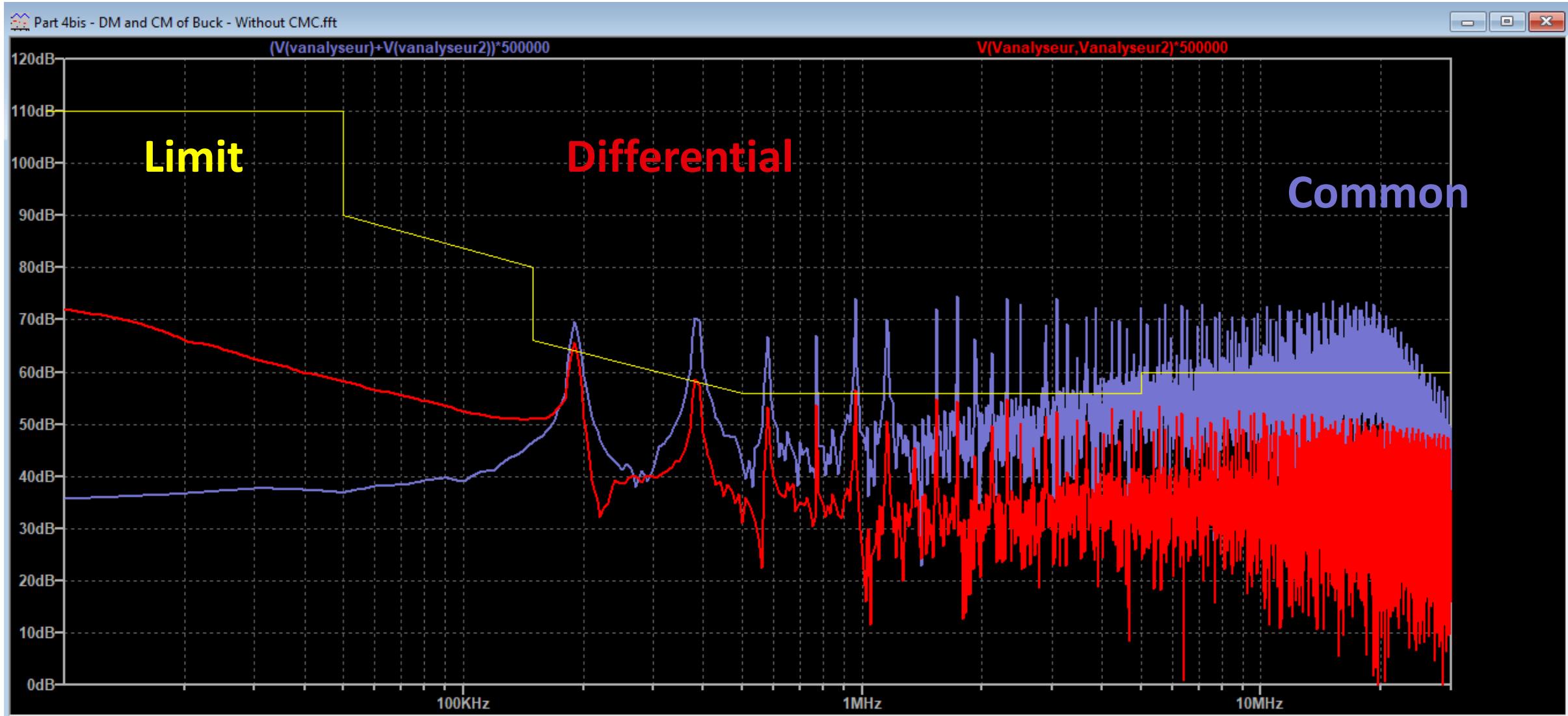
Going further with simulation

Fixing that buck in the simulation – Before Polymer Cap



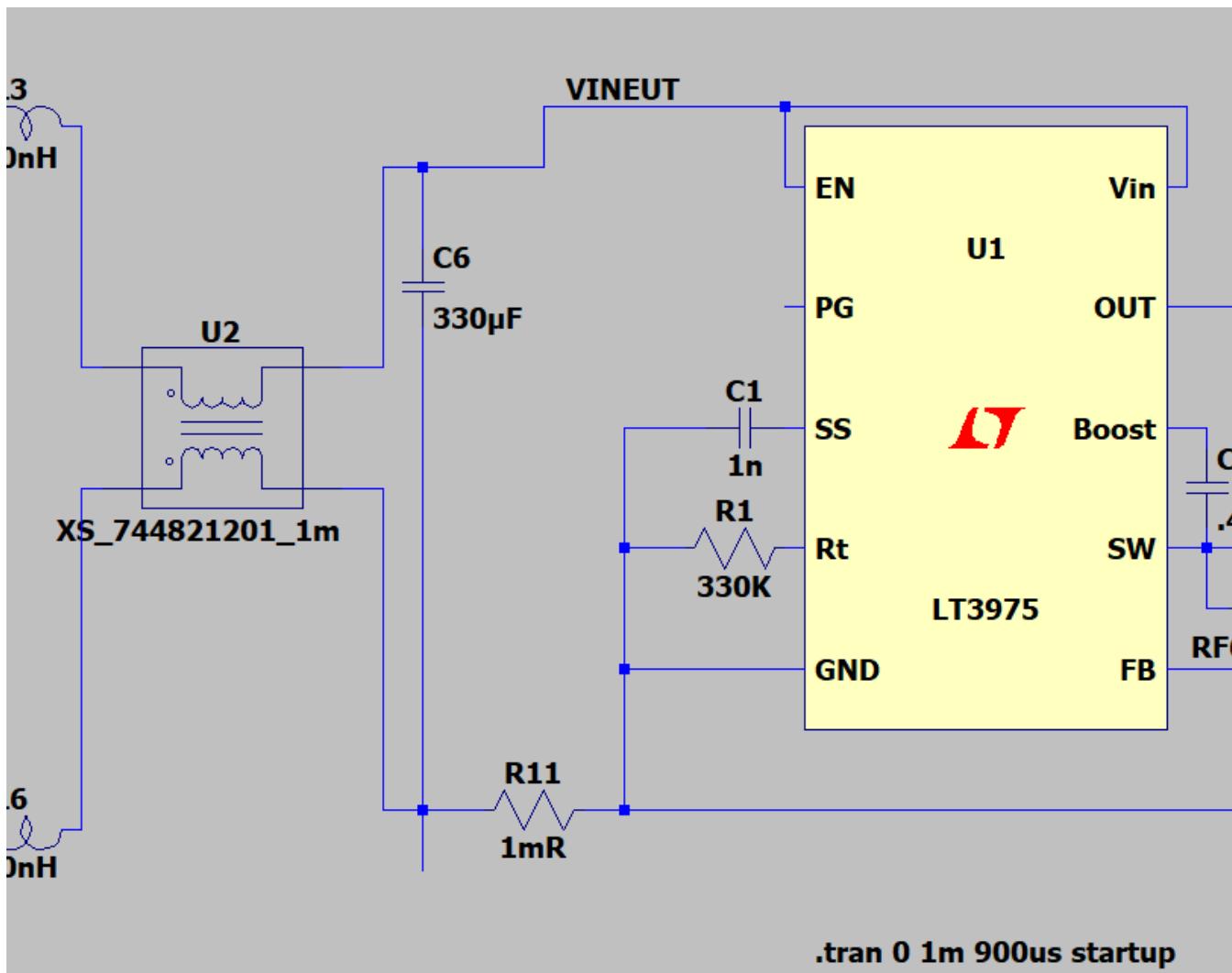
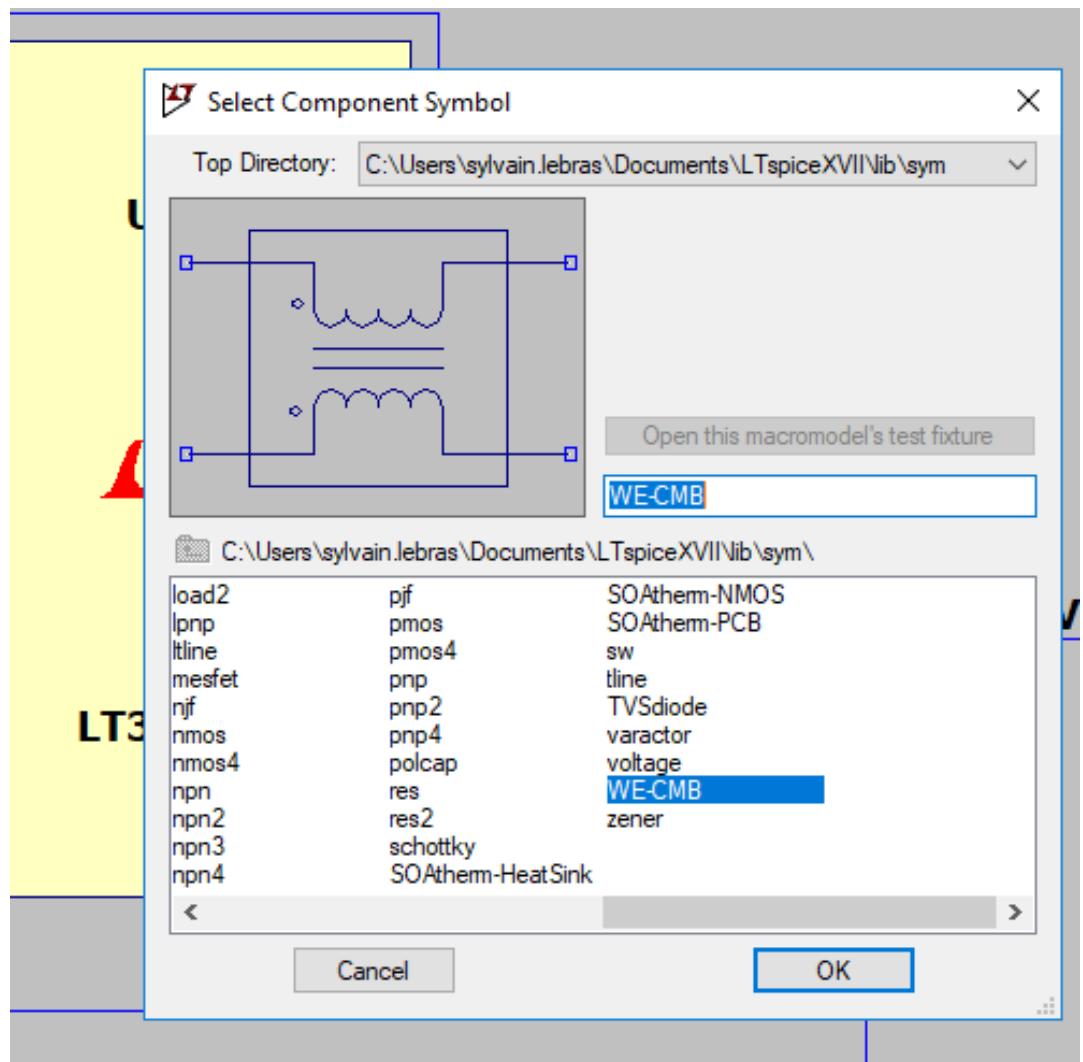
Going further with simulation

Fixing that buck in the simulation – After Polymer Cap



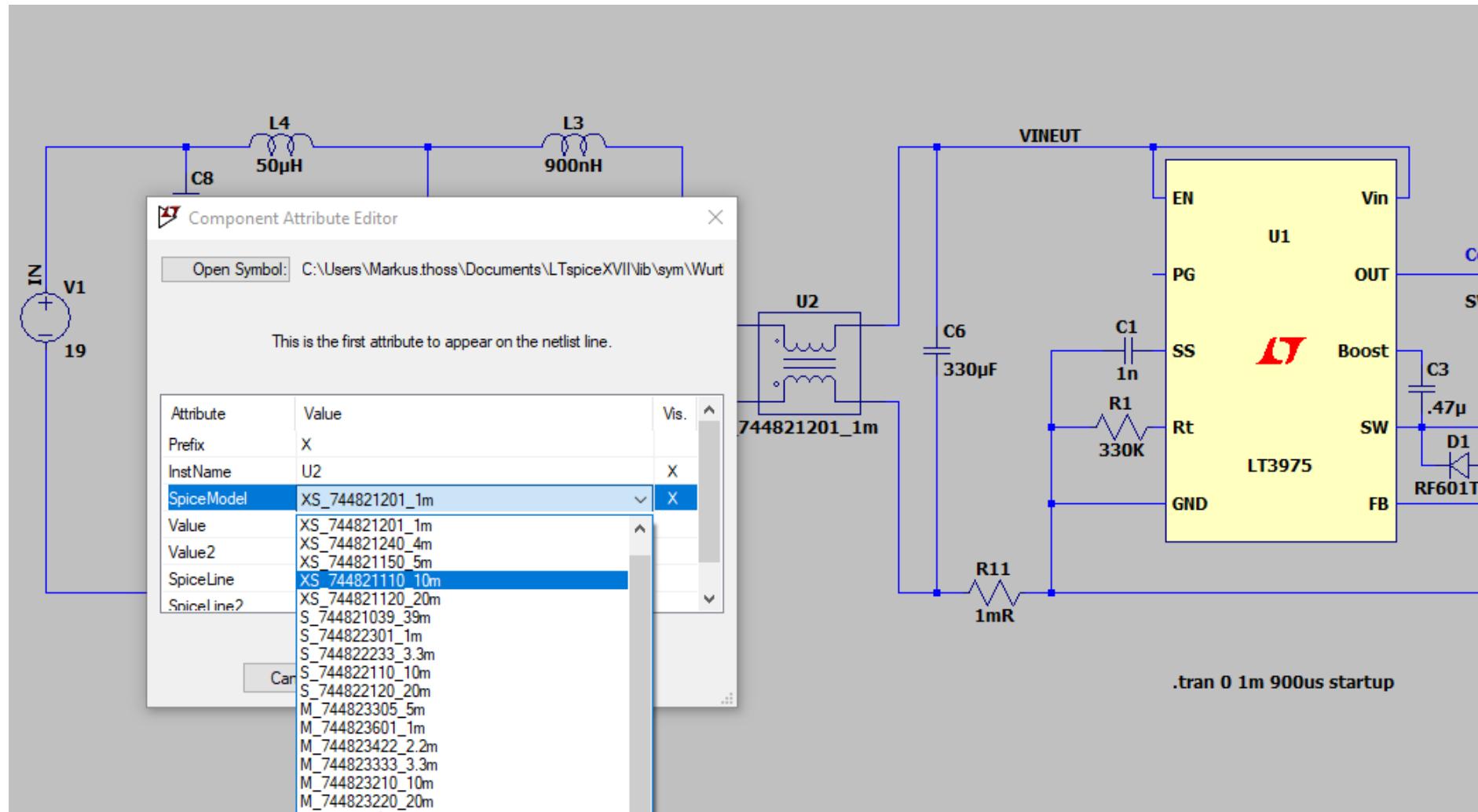
Going further with simulation

Fixing that buck in the simulation – Common mode choke



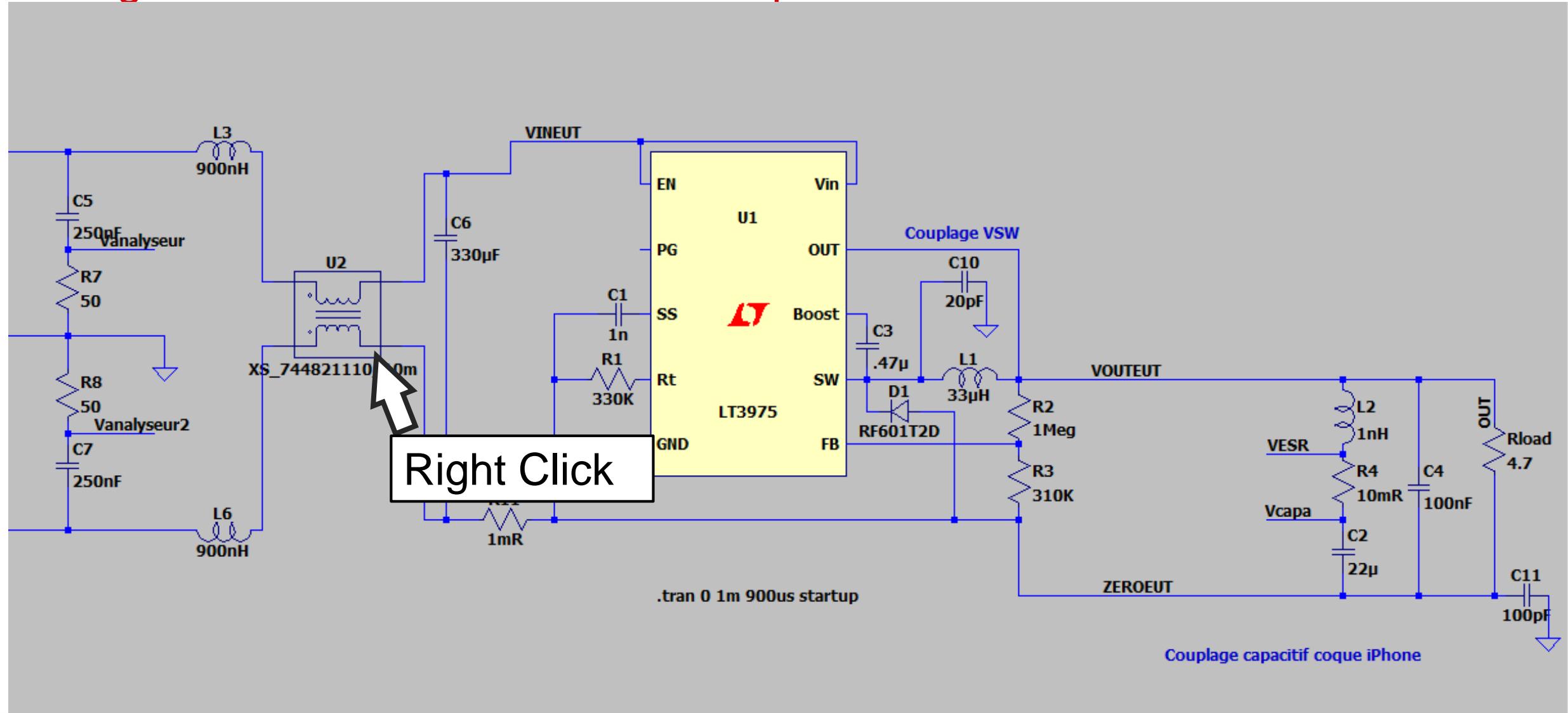
Going further with simulation

Fixing that buck in the simulation – Input Common mode choke



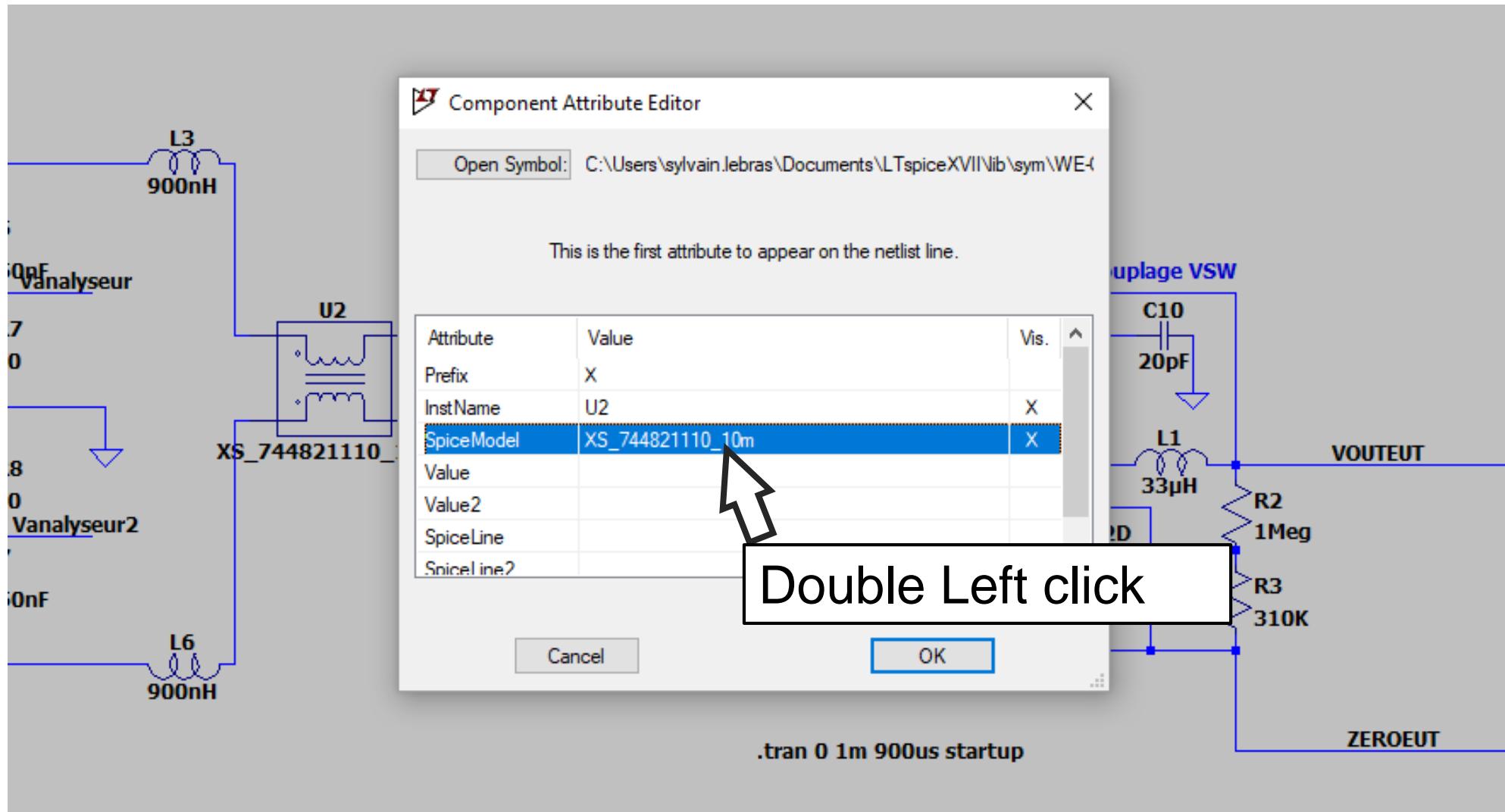
Going further with simulation

Fixing that buck in the simulation – Input Common mode choke



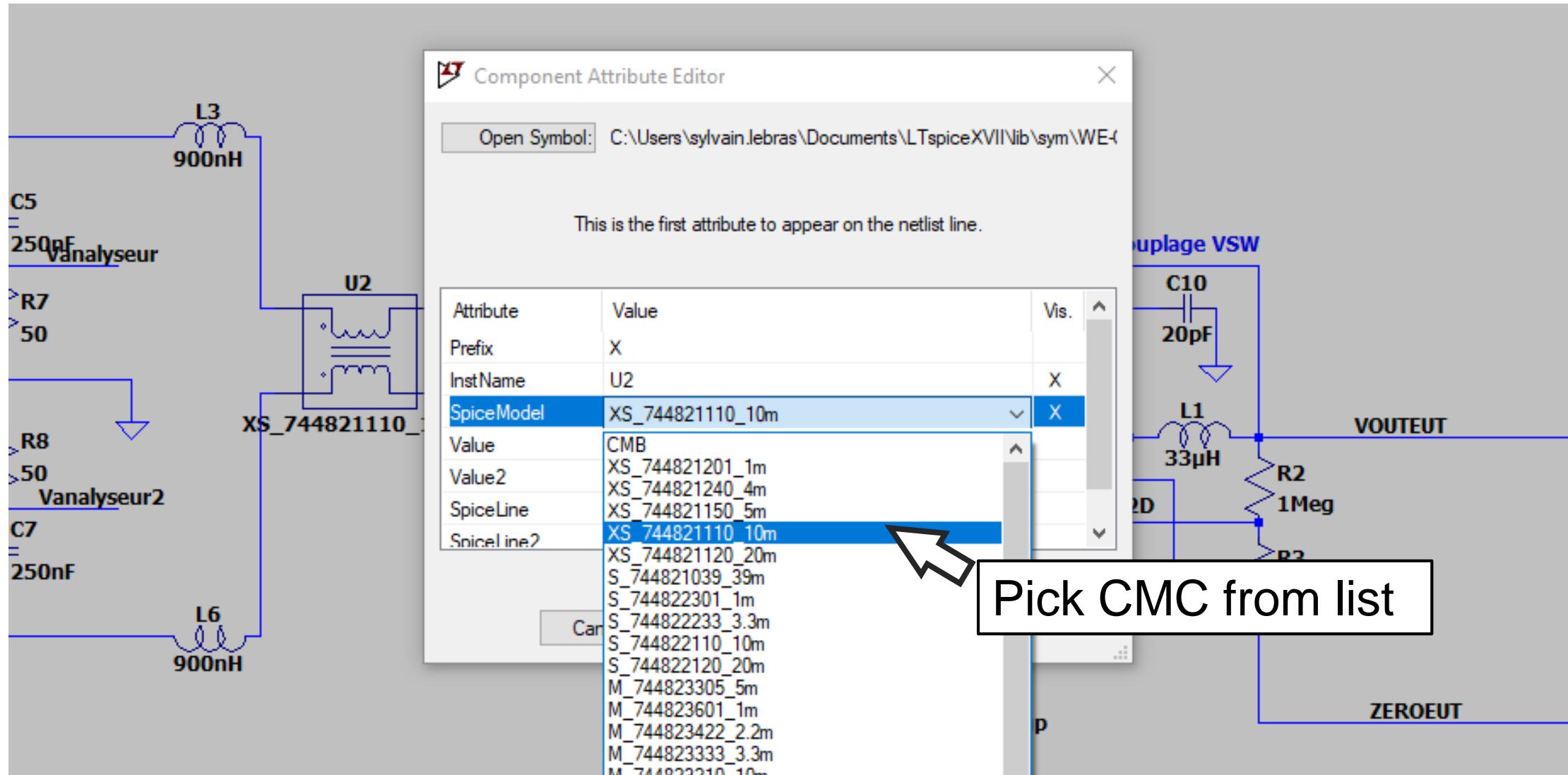
Going further with simulation

Fixing that buck in the simulation – Input Common mode choke



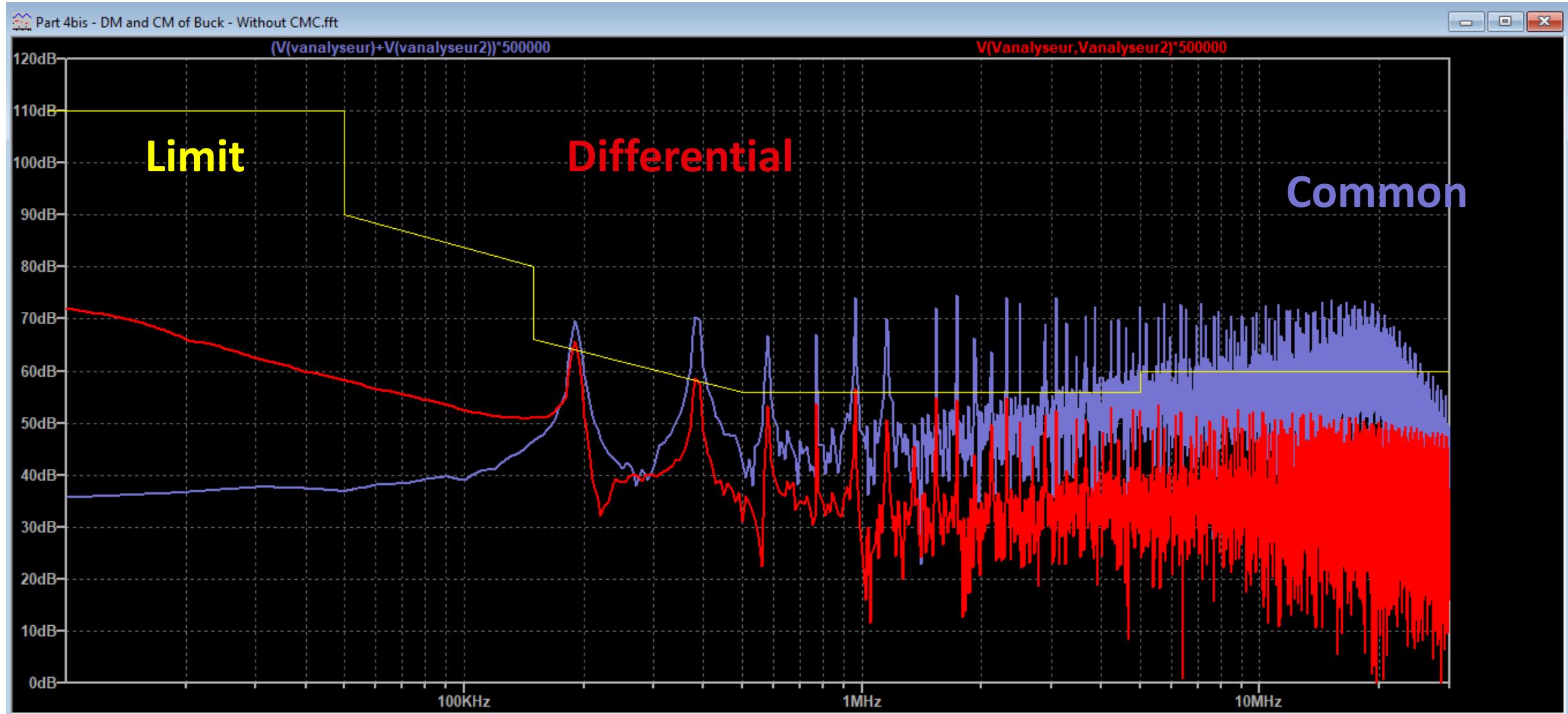
Going further with simulation

Fixing that buck in the simulation – Input Common mode choke



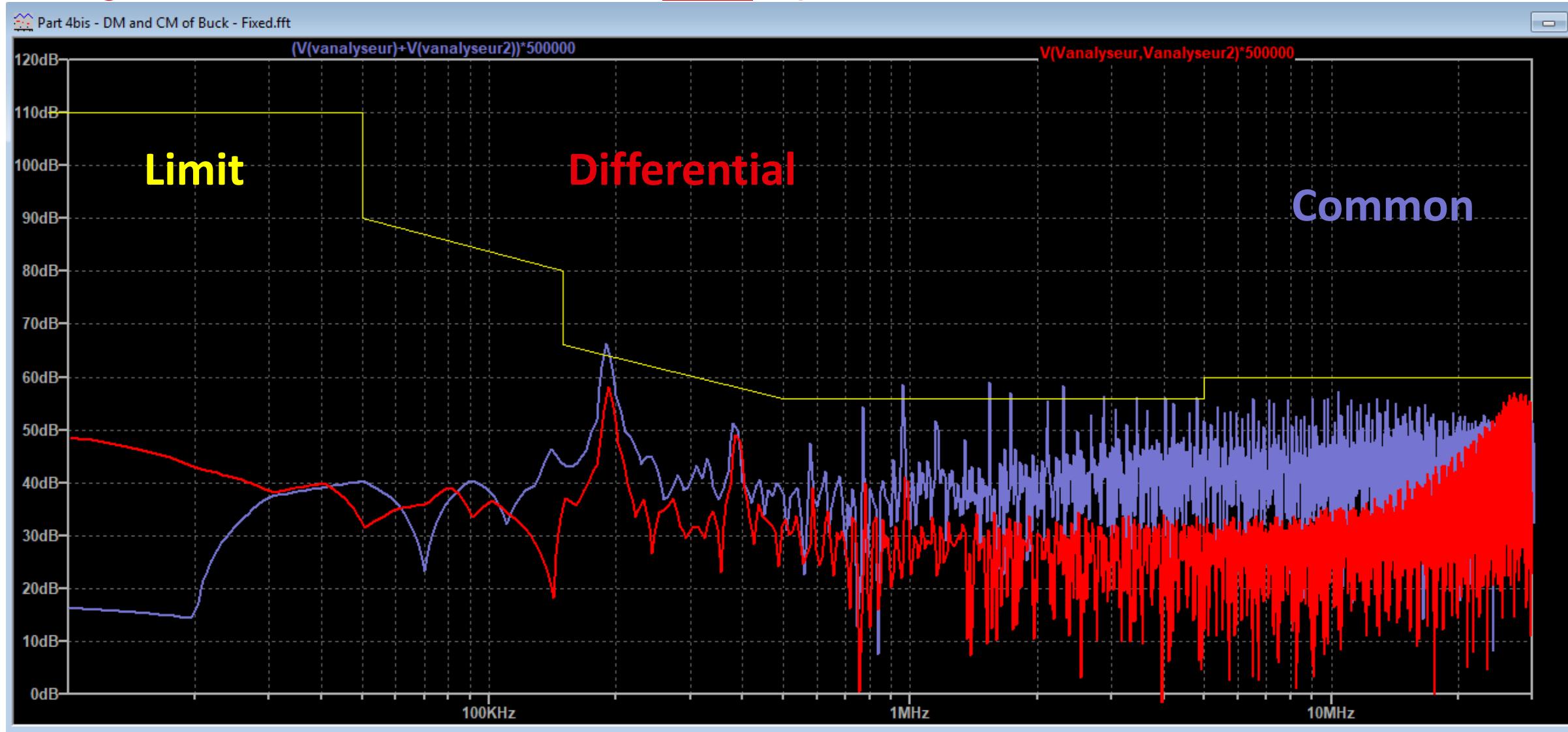
Going further with simulation

Fixing that buck in the simulation – Without Common mode choke



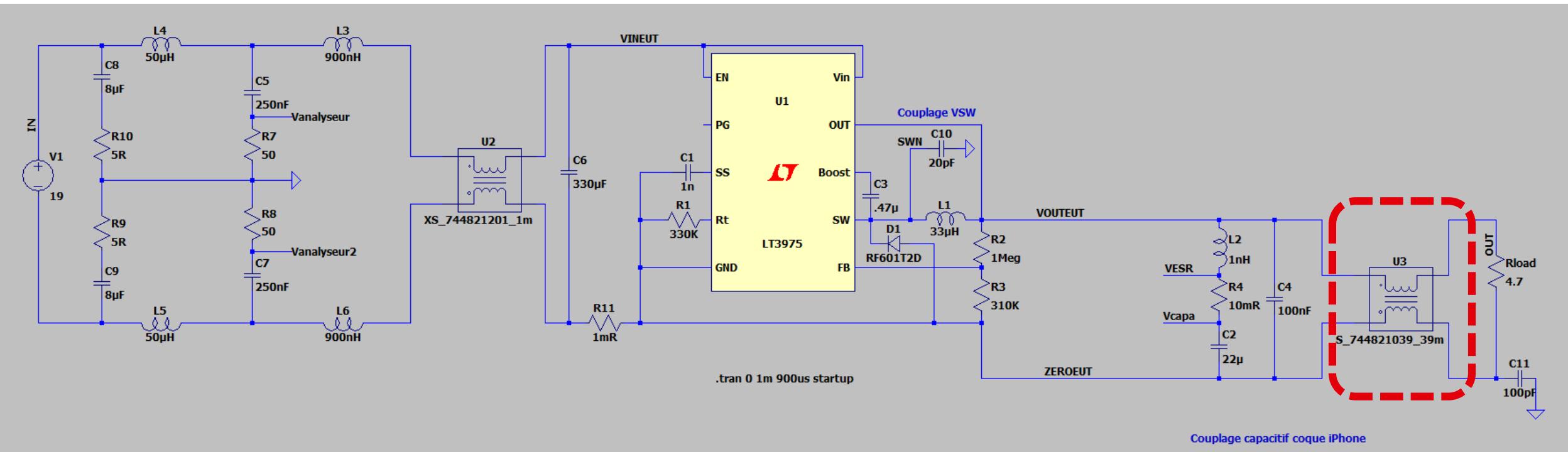
Going further with simulation

Fixing that buck in the simulation – With input Common mode choke



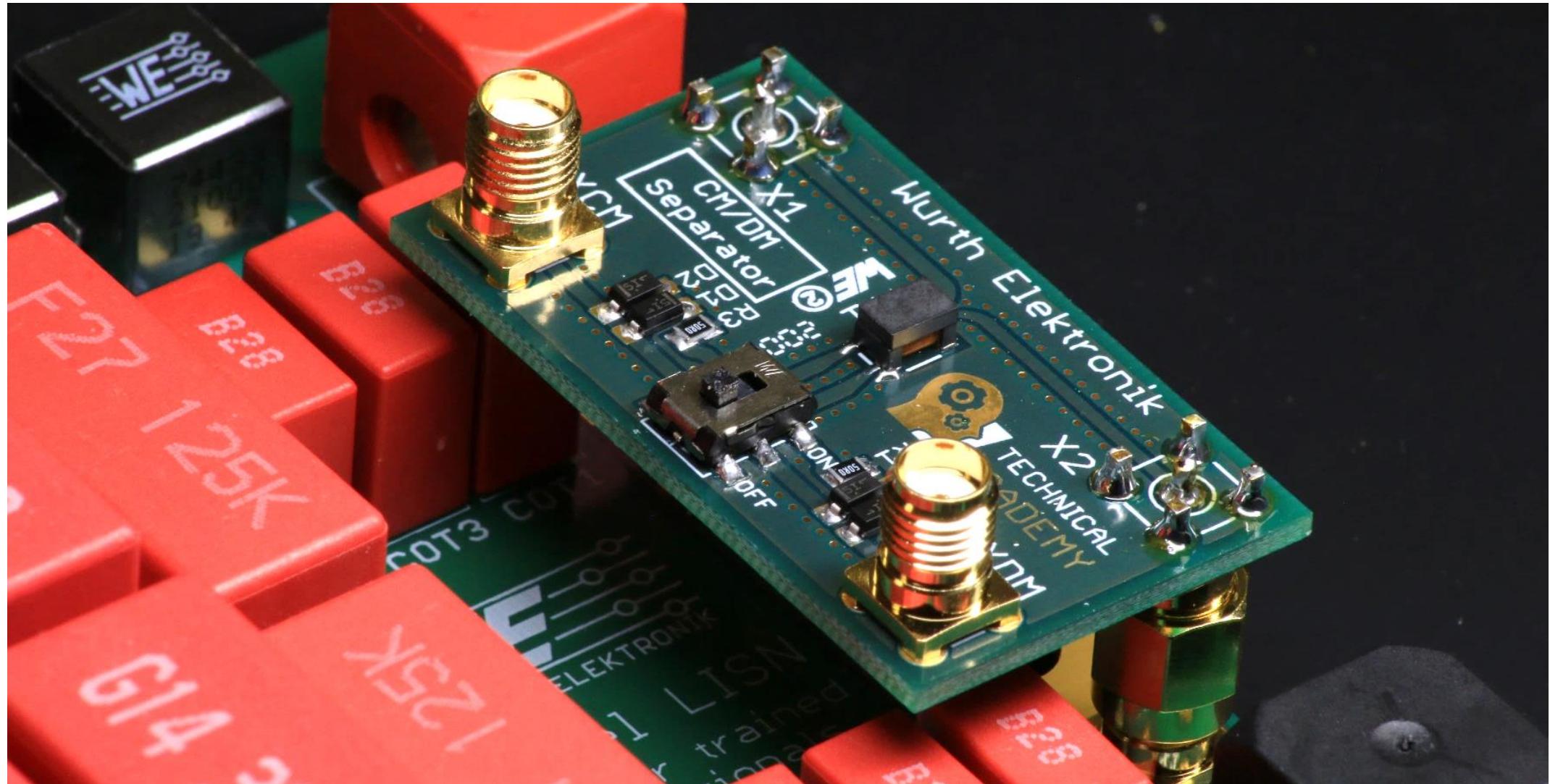
Going further with simulation

Fixing that buck in the simulation – With output CMC



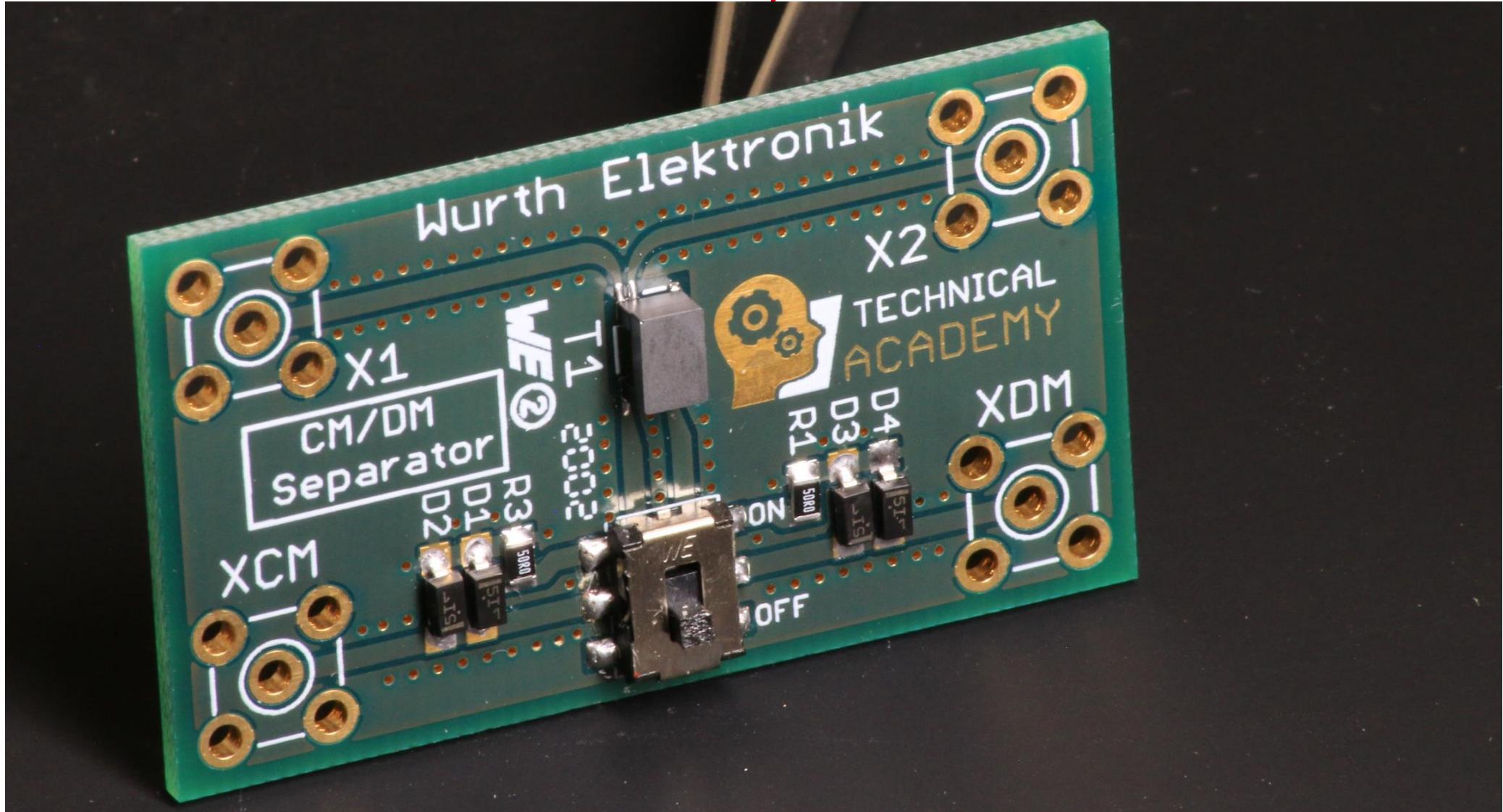
Going further ?

Common mode / Differential Mode separator in real life



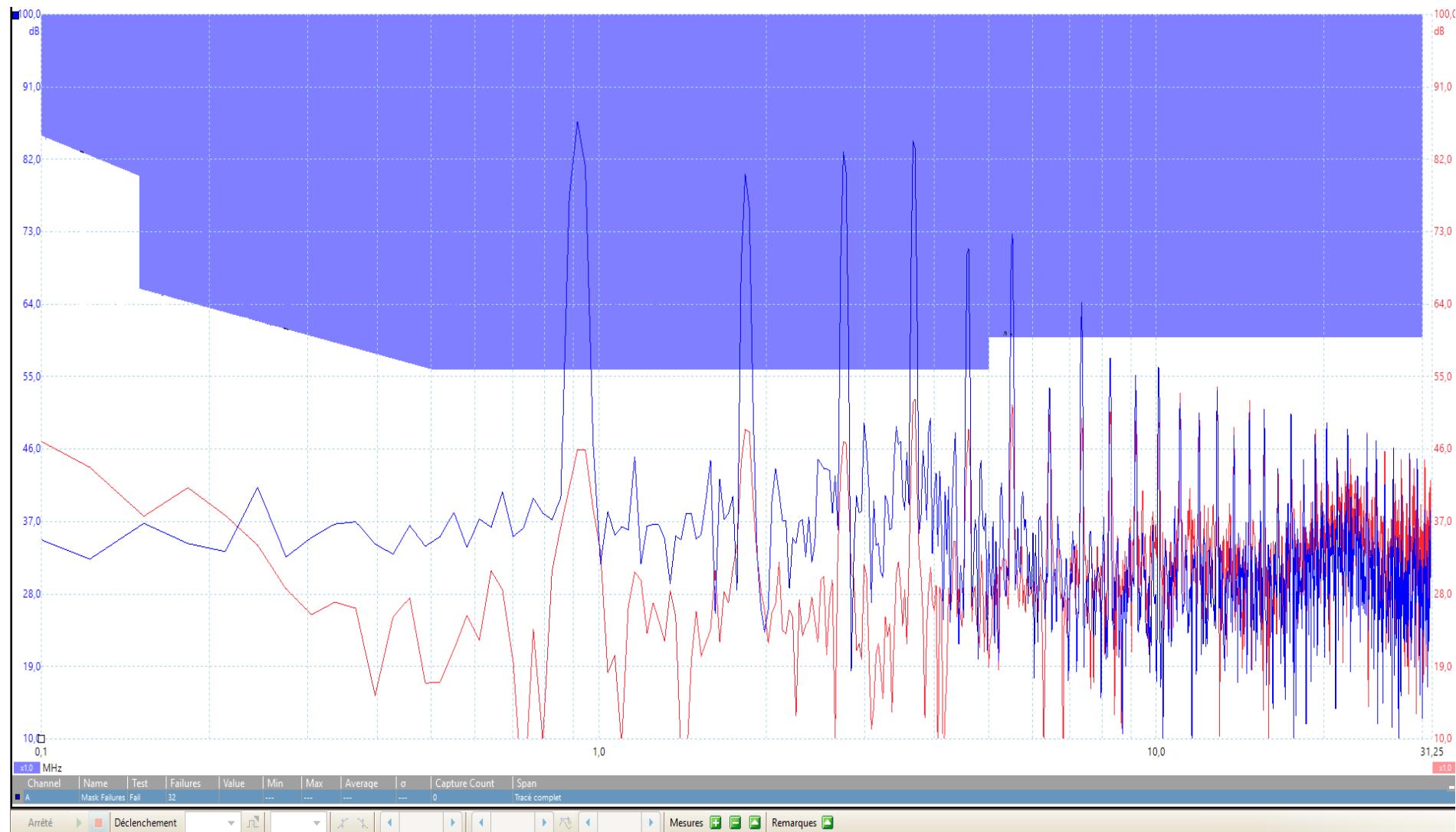
Going further ?

Common mode / Differential Mode separator in real life



Going further ?

Common mode / Differential Mode separator in real life



Modeling Real life examples

Flyback converter for lighting applications



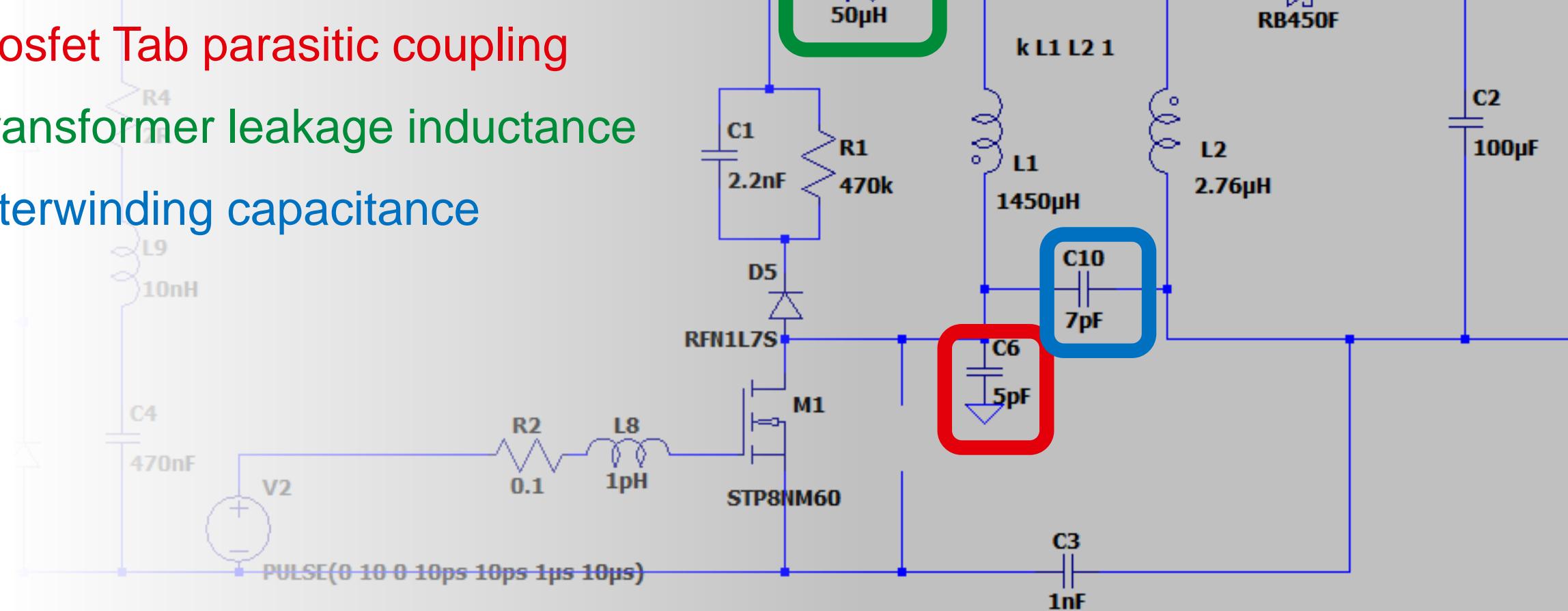
Modeling Real life examples

Flyback converter for lighting applications



- Parasitics :

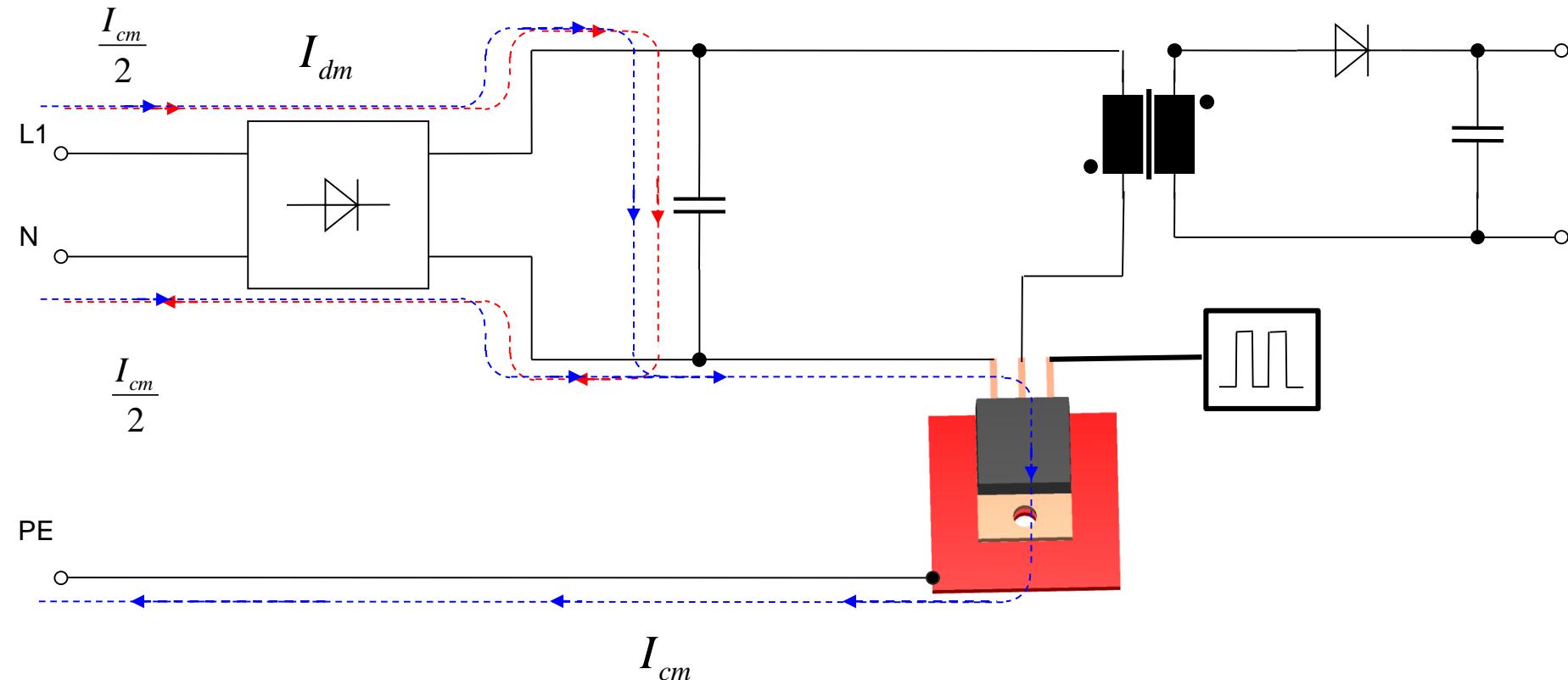
- Mosfet Tab parasitic coupling
- Transformer leakage inductance
- Interwinding capacitance



Real life examples

Flyback converter for lighting applications

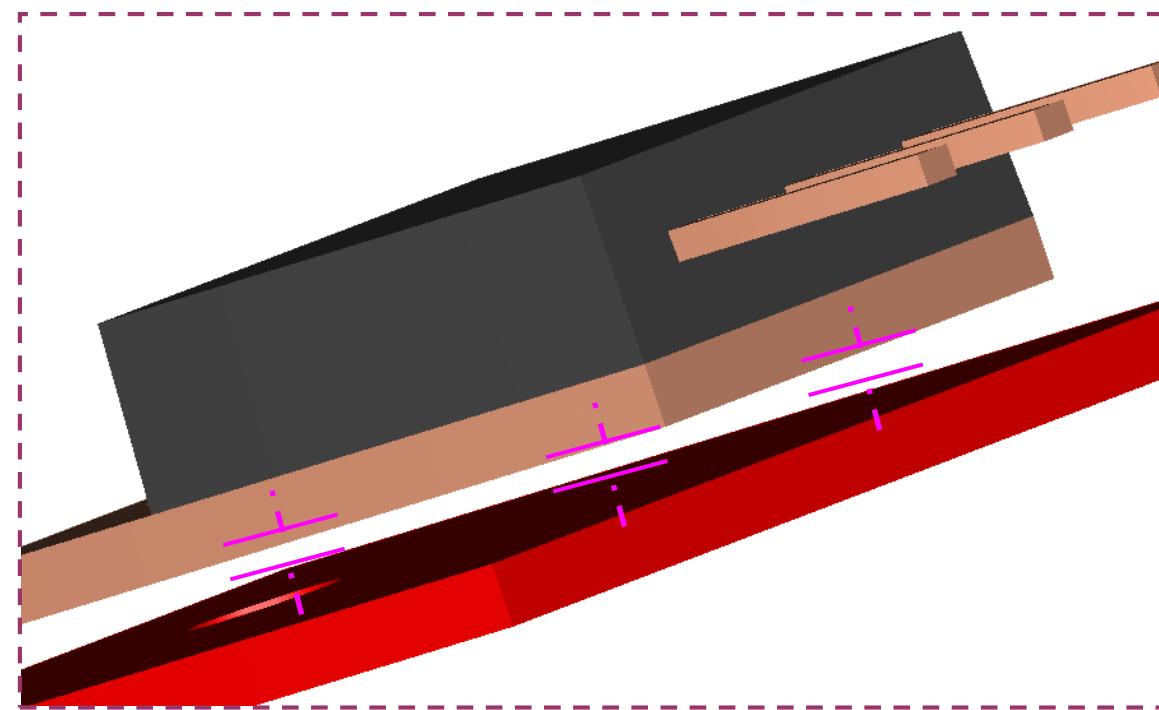
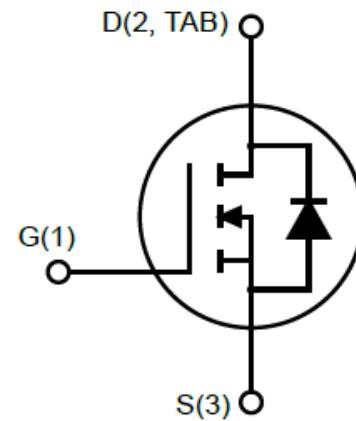
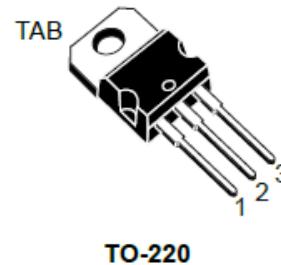
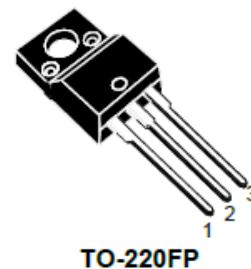
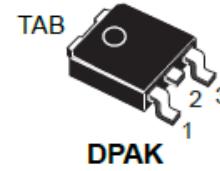
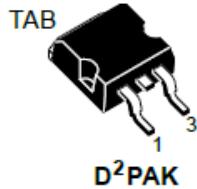
Mosfet Tab parasitic coupling



Real life examples

Flyback converter for lighting applications

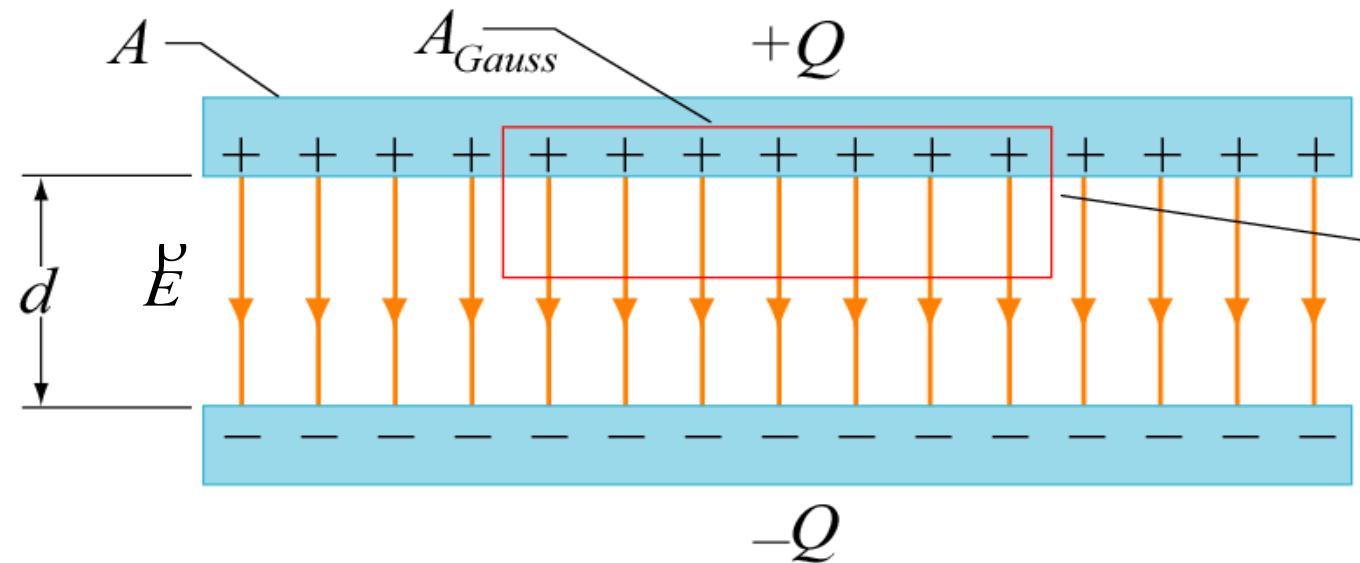
Mosfet Tab parasitic coupling



Real life examples

Flyback converter for lighting applications

Mosfet Tab parasitic coupling



$$C = \frac{\epsilon_0 A}{d}$$

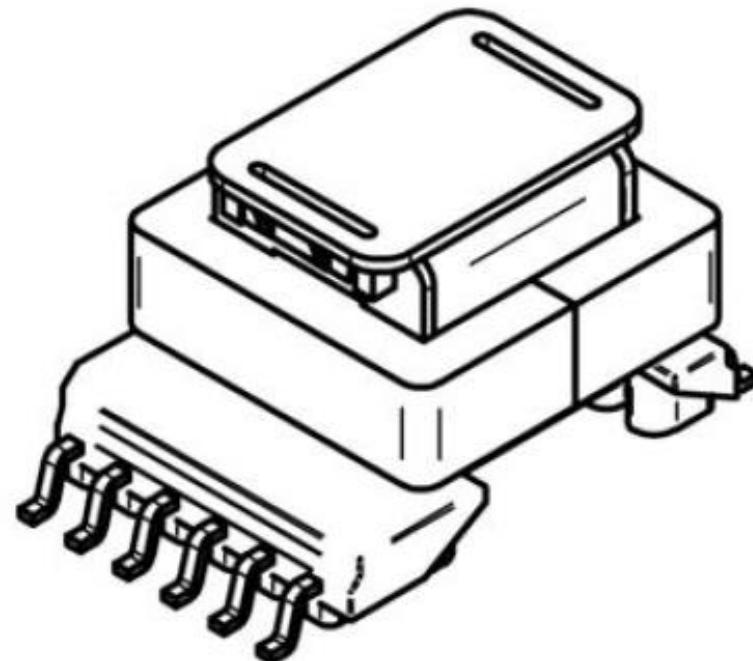
Real life examples

Flyback converter for lighting applications

Primary leakage inductance

D Electrical Properties:

Properties	Test conditions		Value	Unit	Tol.
Inductance	100 kHz/ 100 mV	L	1310	µH	±10%
Turns ratio		n	140 : 6 : 6 : 16		±3%
Saturation current	$ \Delta L / L < 20\%$	I_{sat}	0.8	A	typ.
DC Resistance 1	@ 20°C	R_{DC1}	3000.0	mΩ	max.
DC Resistance 2	@ 20°C	R_{DC2}	25.0	mΩ	max.
DC Resistance 3	@ 20°C	R_{DC3}	25.0	mΩ	max.
DC Resistance 4	@ 20°C	R_{DC4}	450.0	mΩ	max.
Leakage inductance	100 kHz/ 100 mV	L_S	40.0	µH	max.
Insulation test voltage	$W1,4 \Rightarrow W2,3$	U_T	4000	V (AC)	



WE-UOST

Real life examples

Turn ratio to inductance ?



Transformers : from datasheet to LTSpice model

Primary inductance

1310 μH

Lp

Leakage inductance

50 μH

L1

Primary	Secondary	Aux
130	6	16

Ratio

2.79 μH

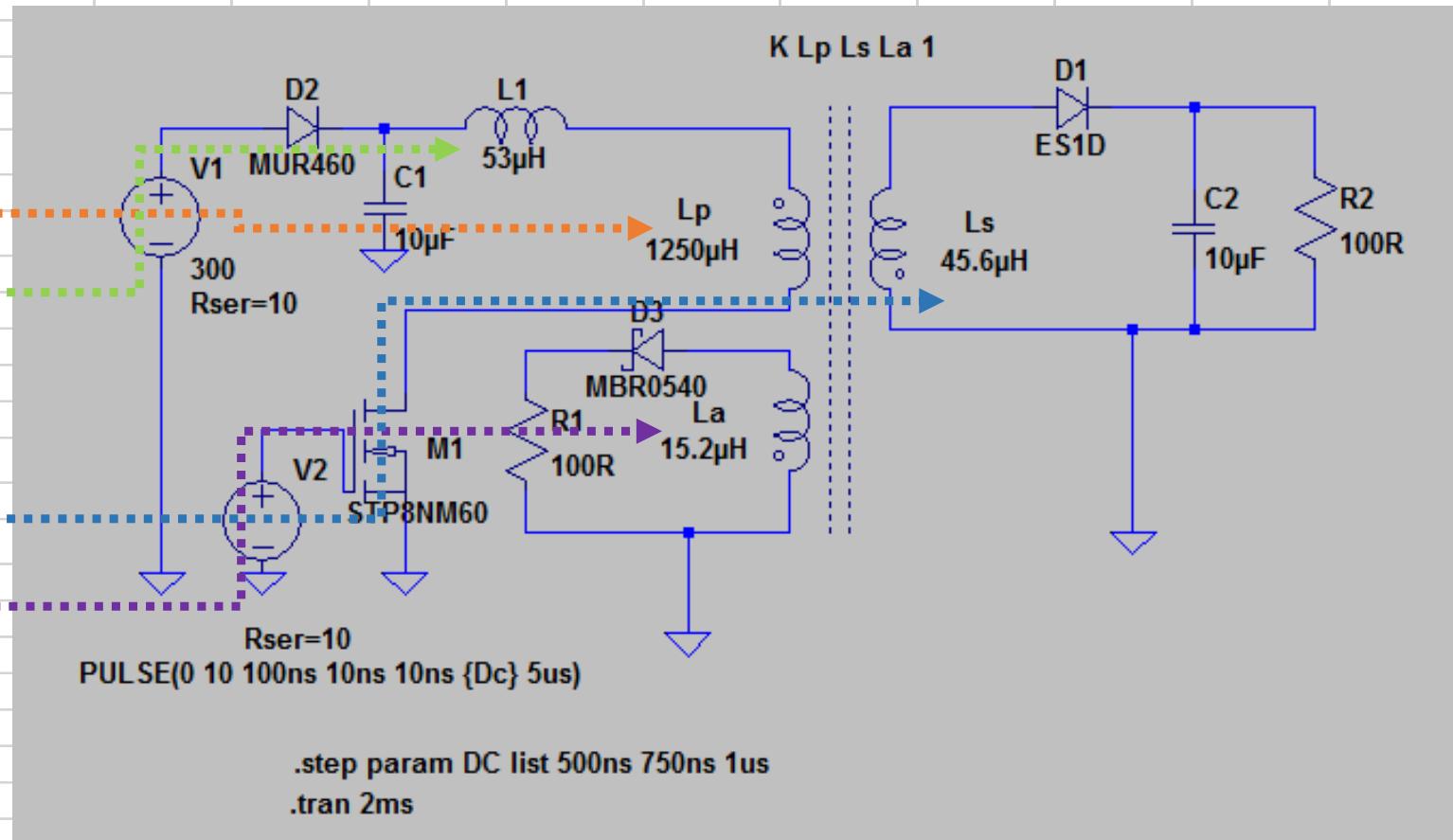
Ls

Secondary inductance

19.84 μH

La

Auxiliary inductance

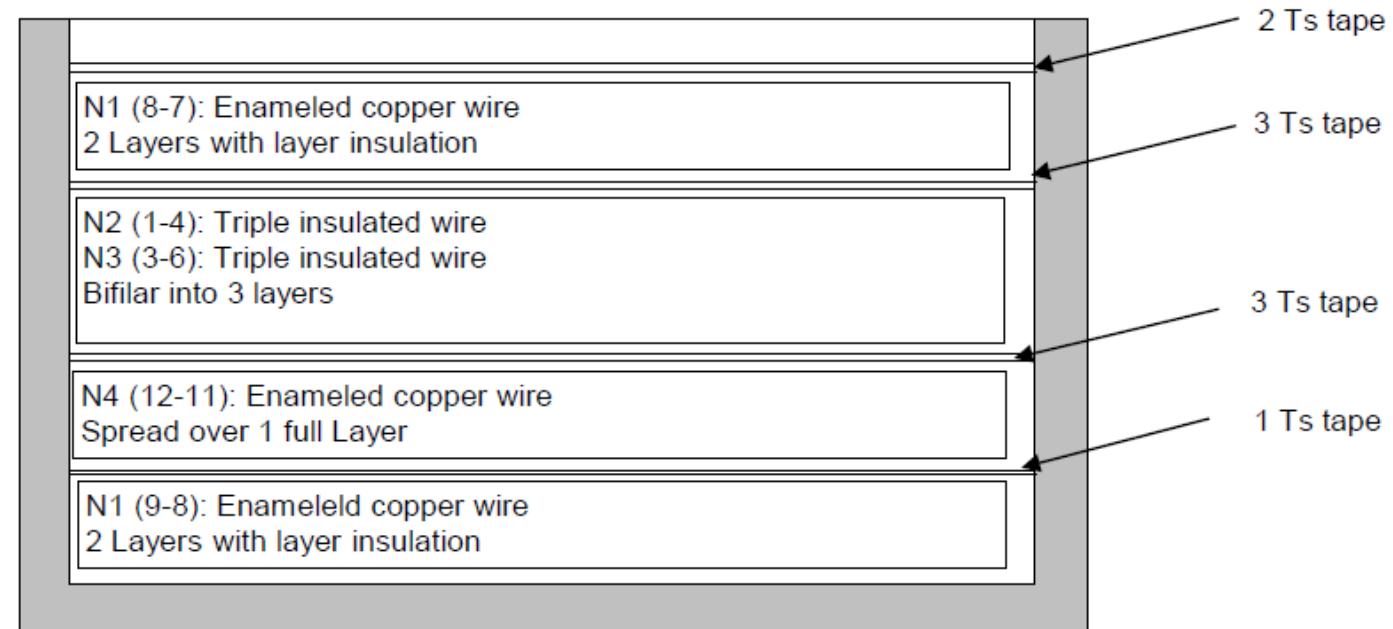
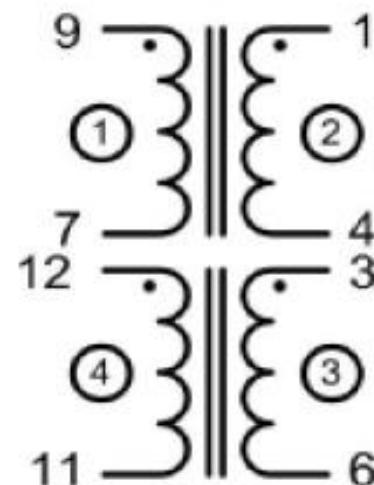


Real life examples

Flyback converter for lighting applications

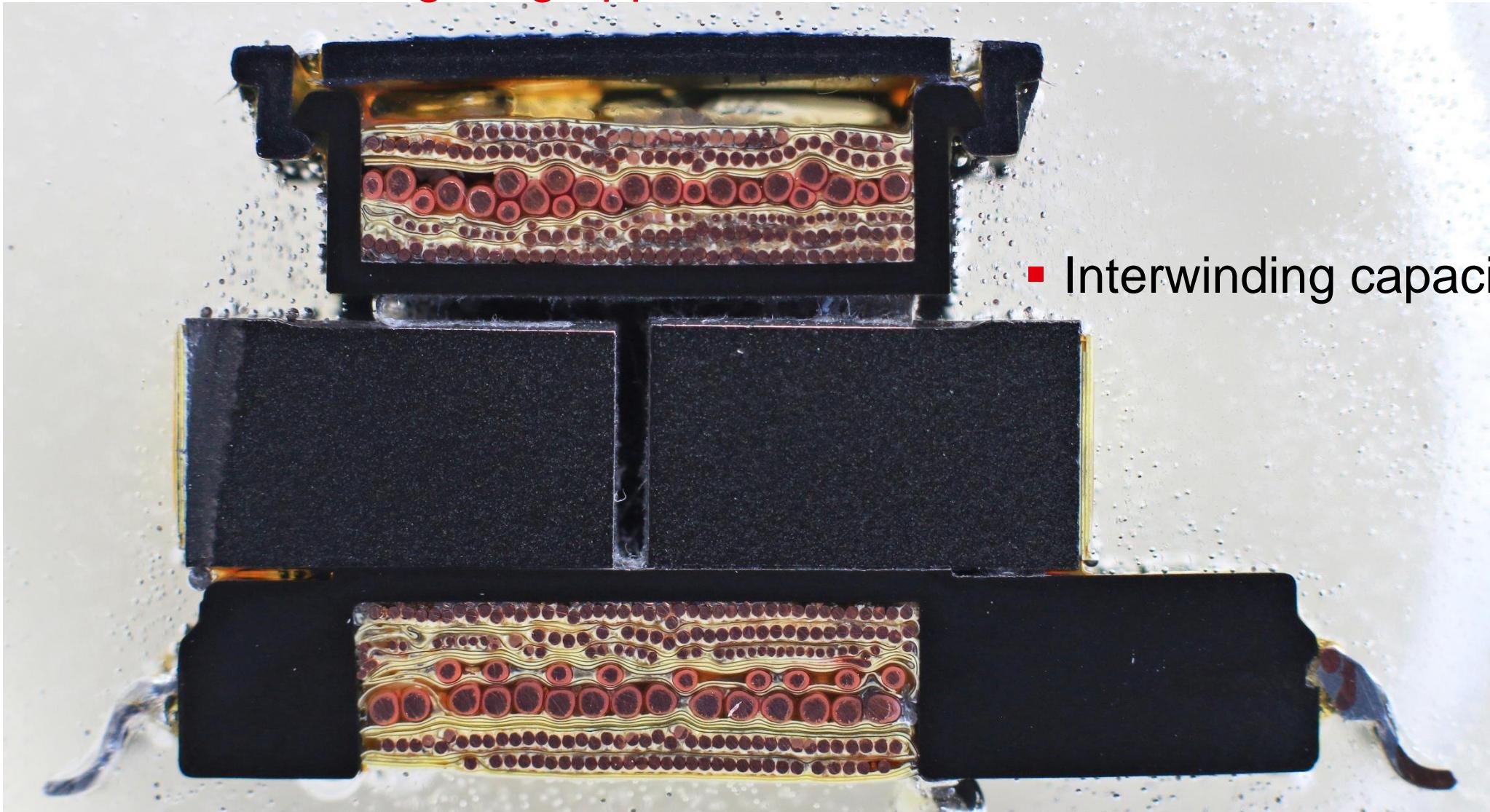


■ Interwinding capacitance ?



Real life examples

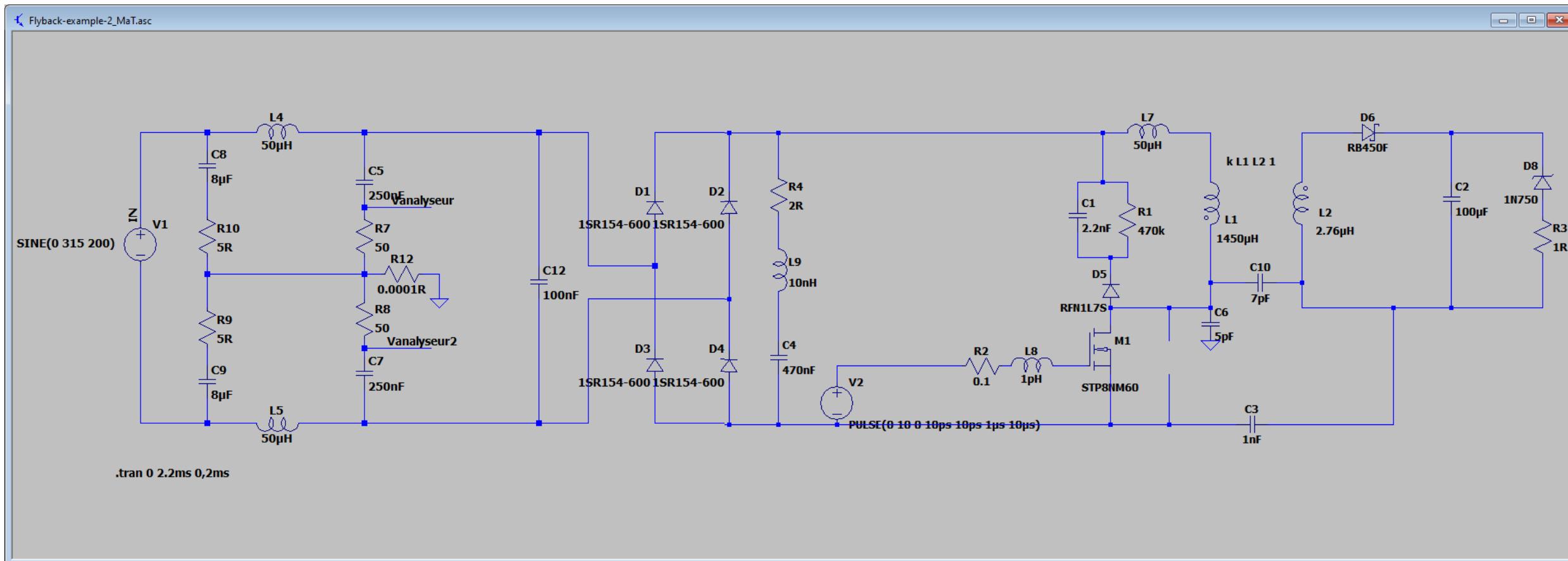
Flyback converter for lighting applications



- Interwinding capacitance ?

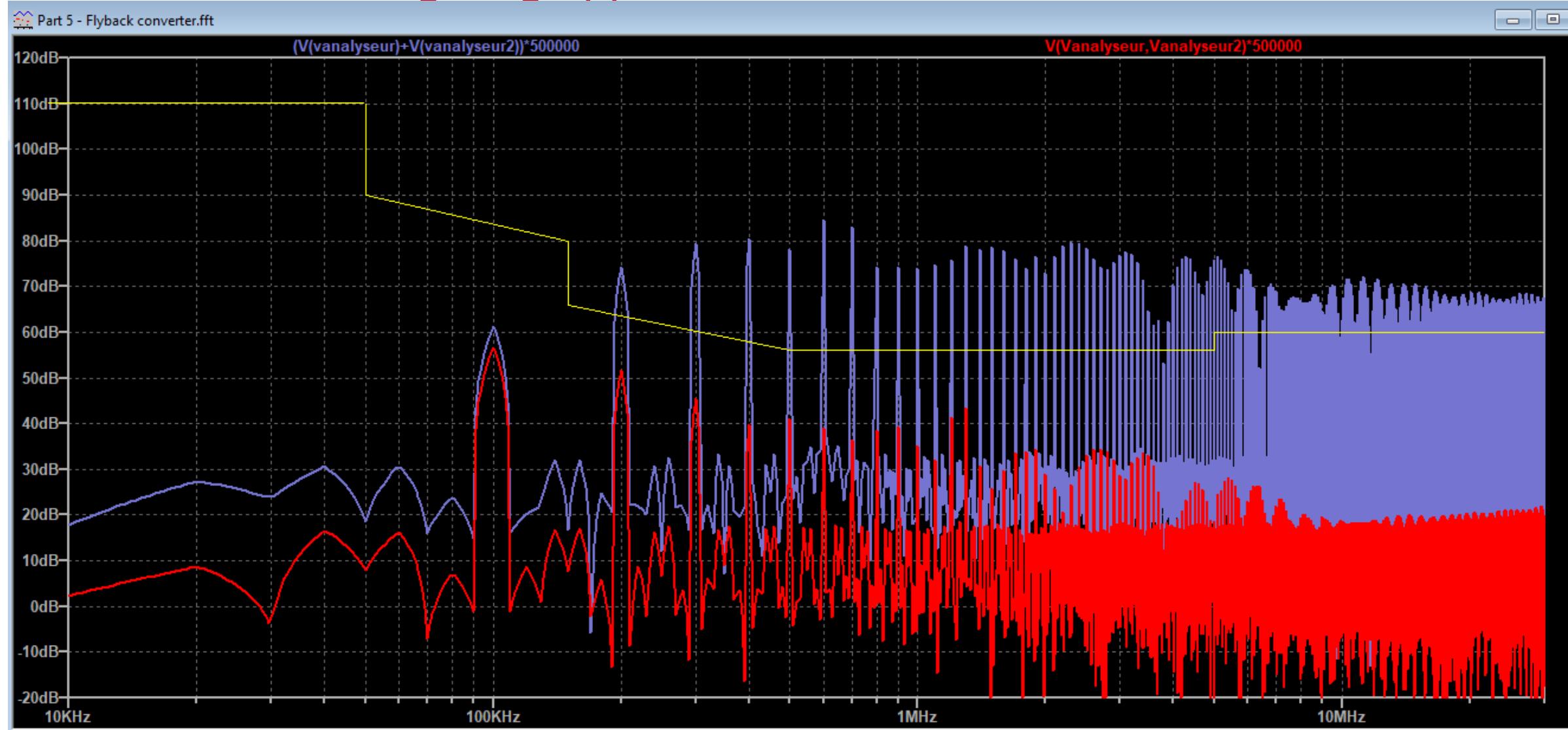
Real life examples

Flyback converter for lighting applications



Real life examples

Flyback converter for lighting applications

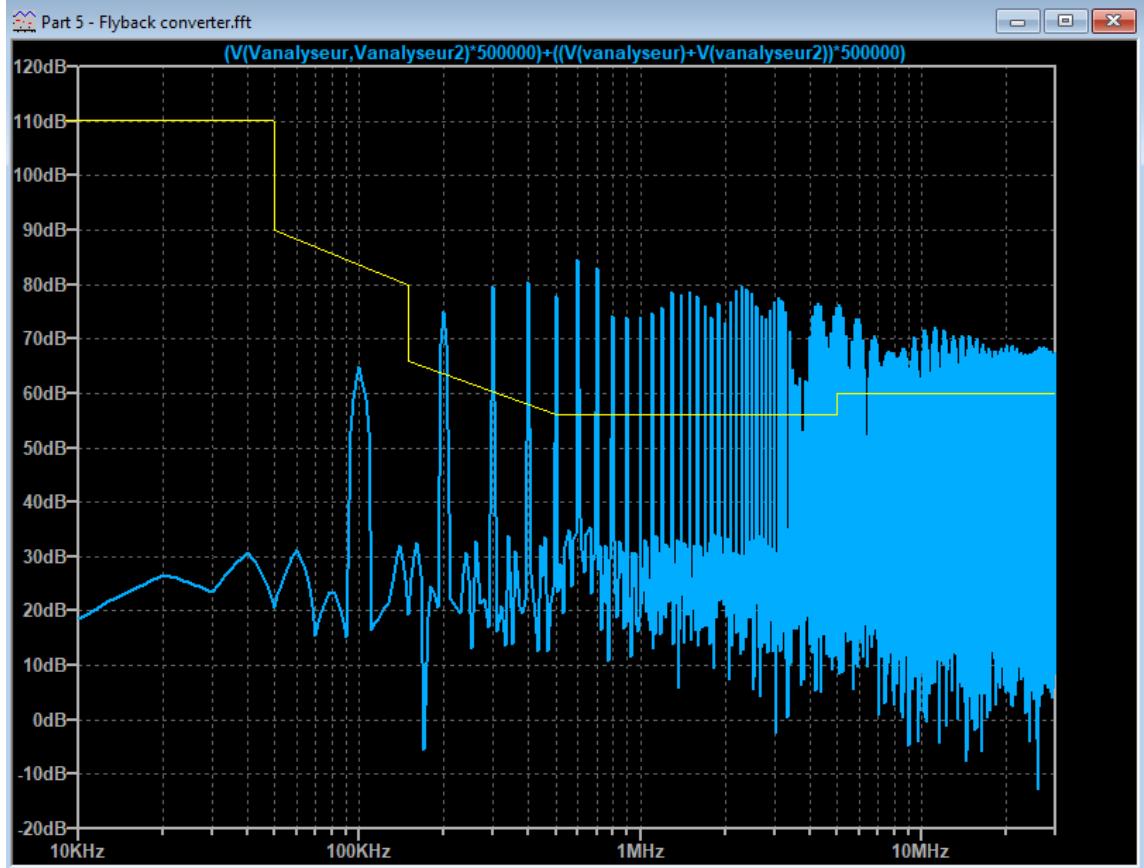


Real life examples

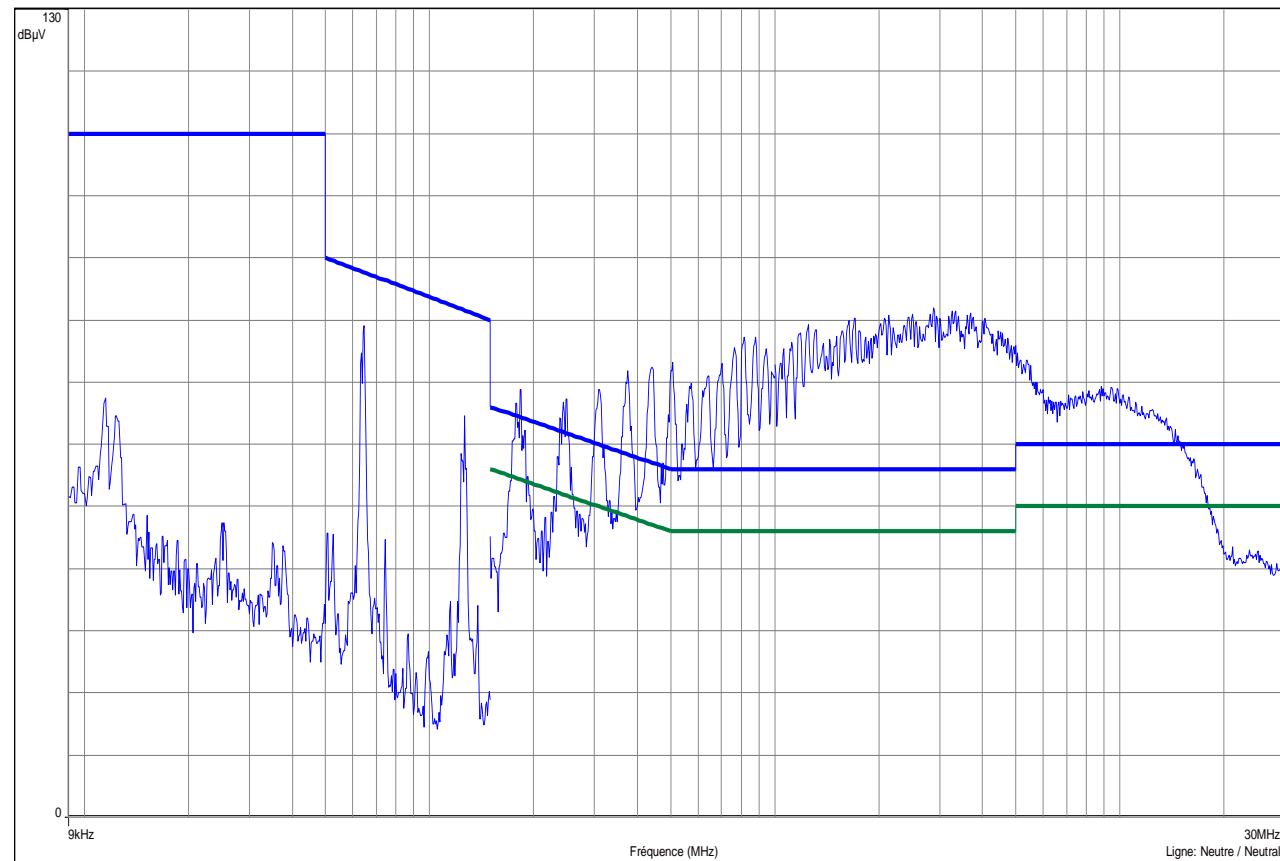
Flyback converter for lighting applications



Simulation



Example of actual measurement



Real life examples

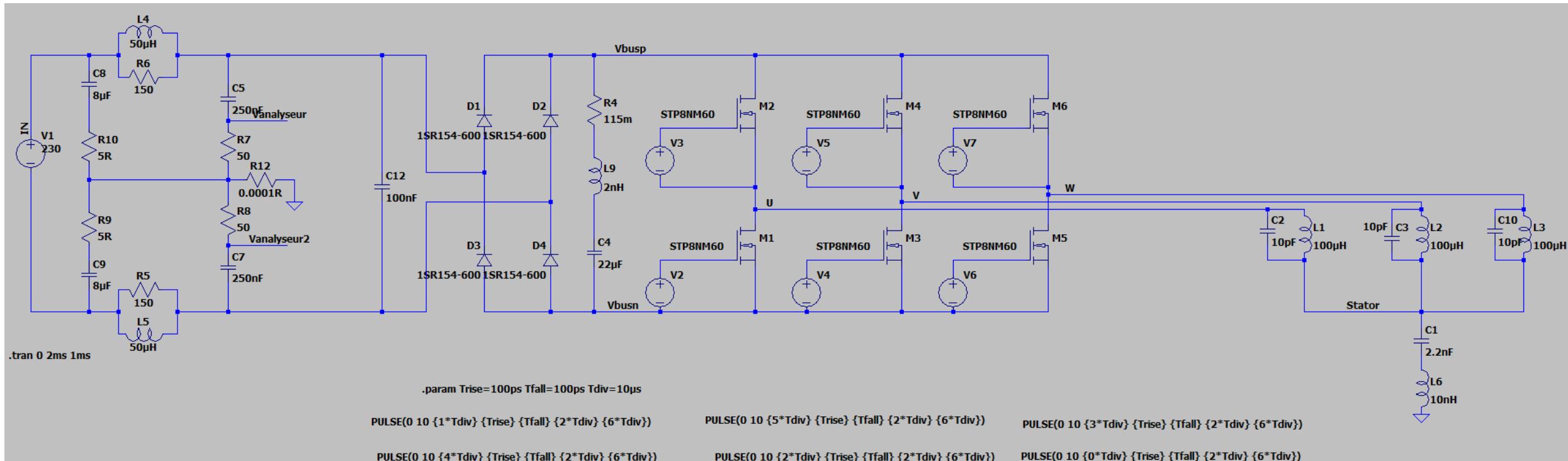
Mains voltage BLDC driver + motor



Real life examples

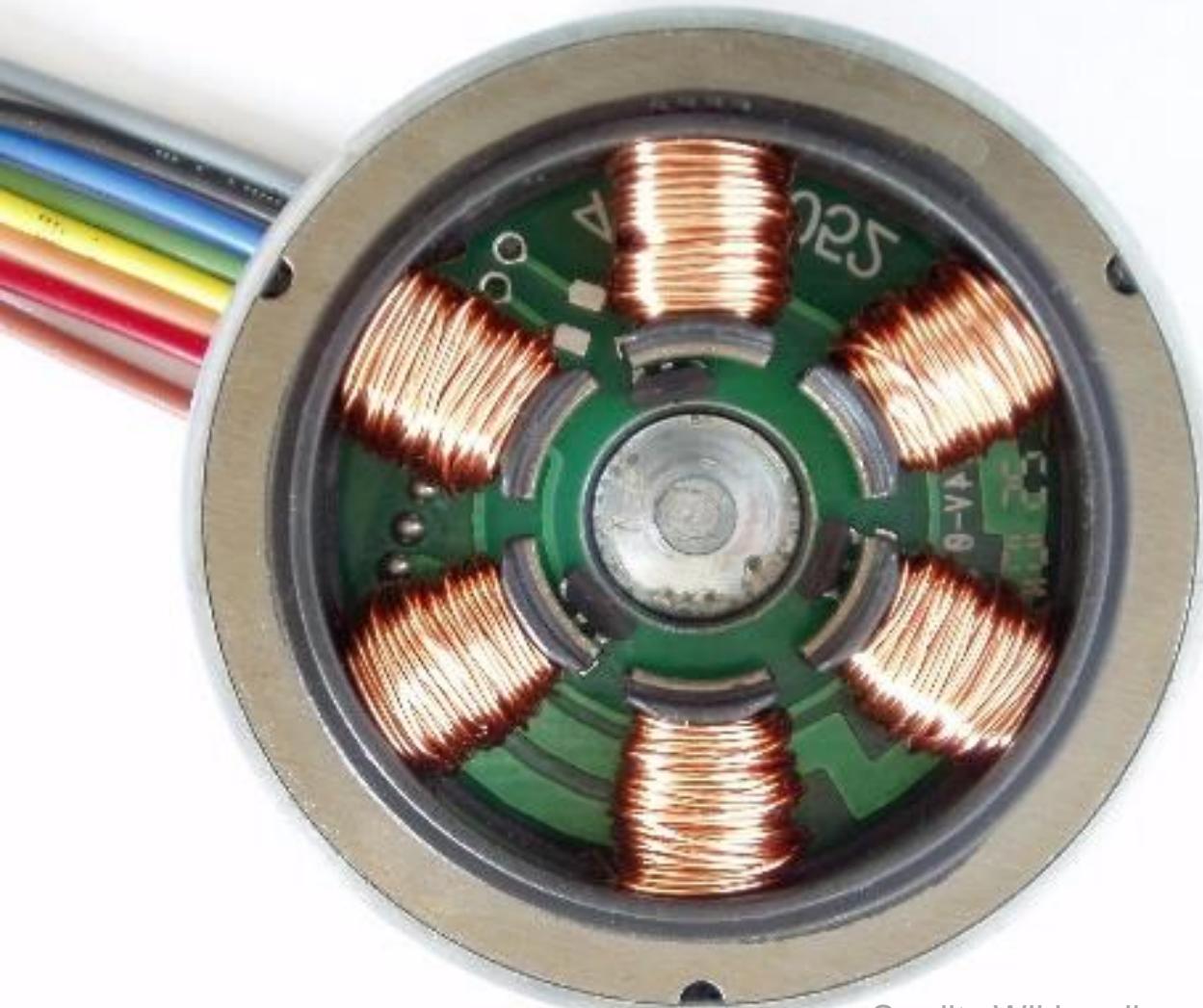
Mains voltage BLDC driver + motor

- Parasitic coupling to and through stator
- Influence of grounding
- Slew rate of driver
- Dead time impact



Real life examples

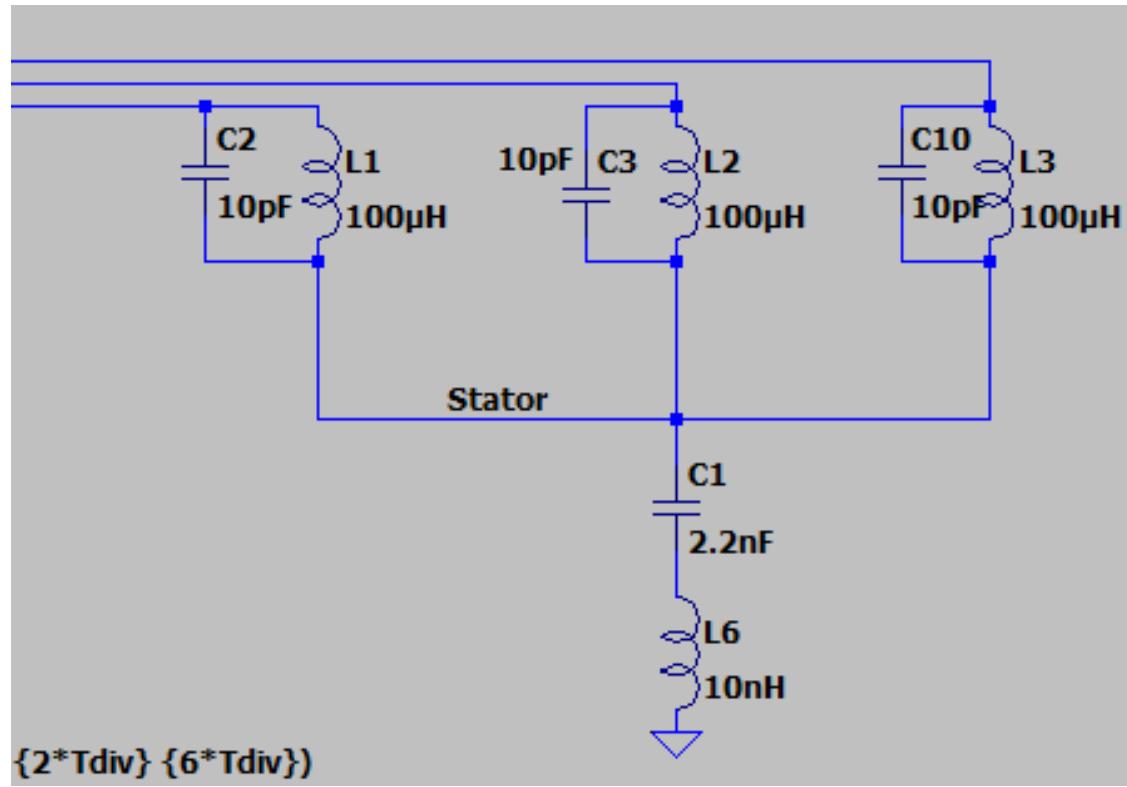
Mains voltage BLDC driver + motor



Credits Wikimedia commons

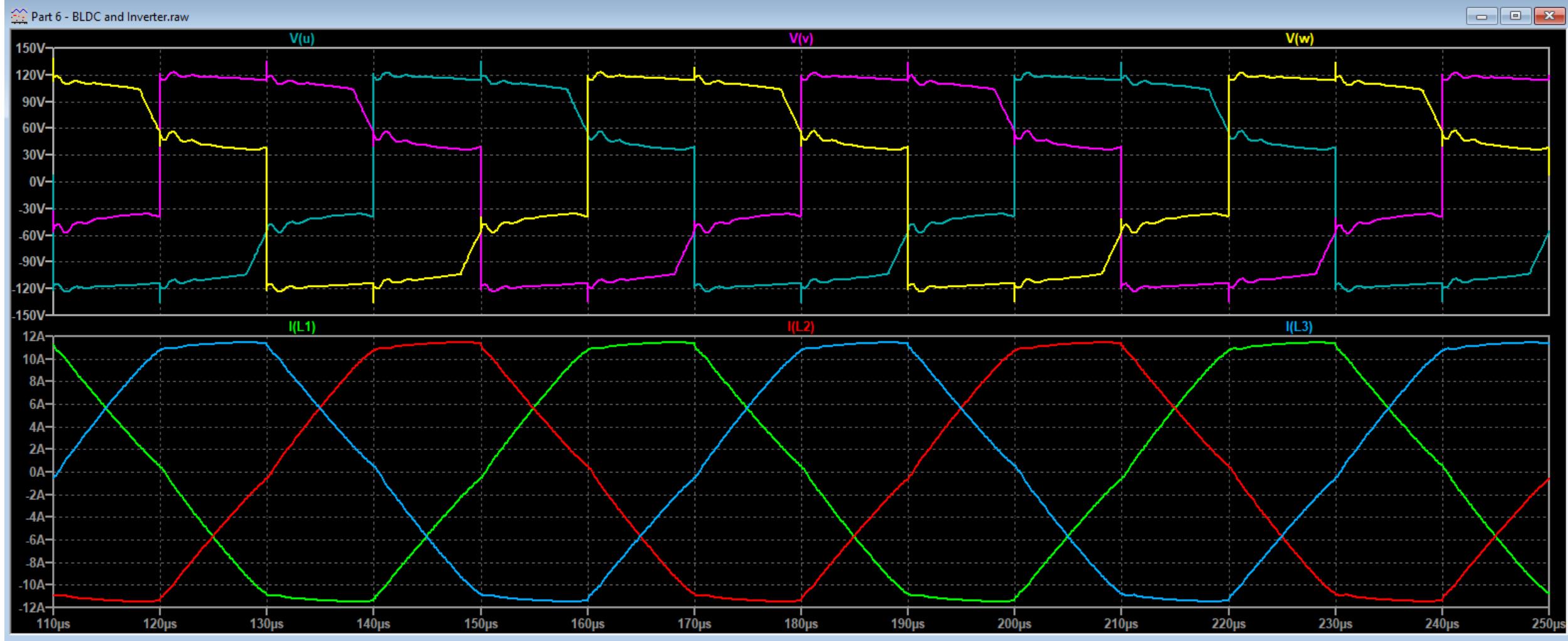


- Parasitic coupling to and through stator
- Influence of grounding (of stator)



Real life examples

Mains voltage BLDC driver + motor



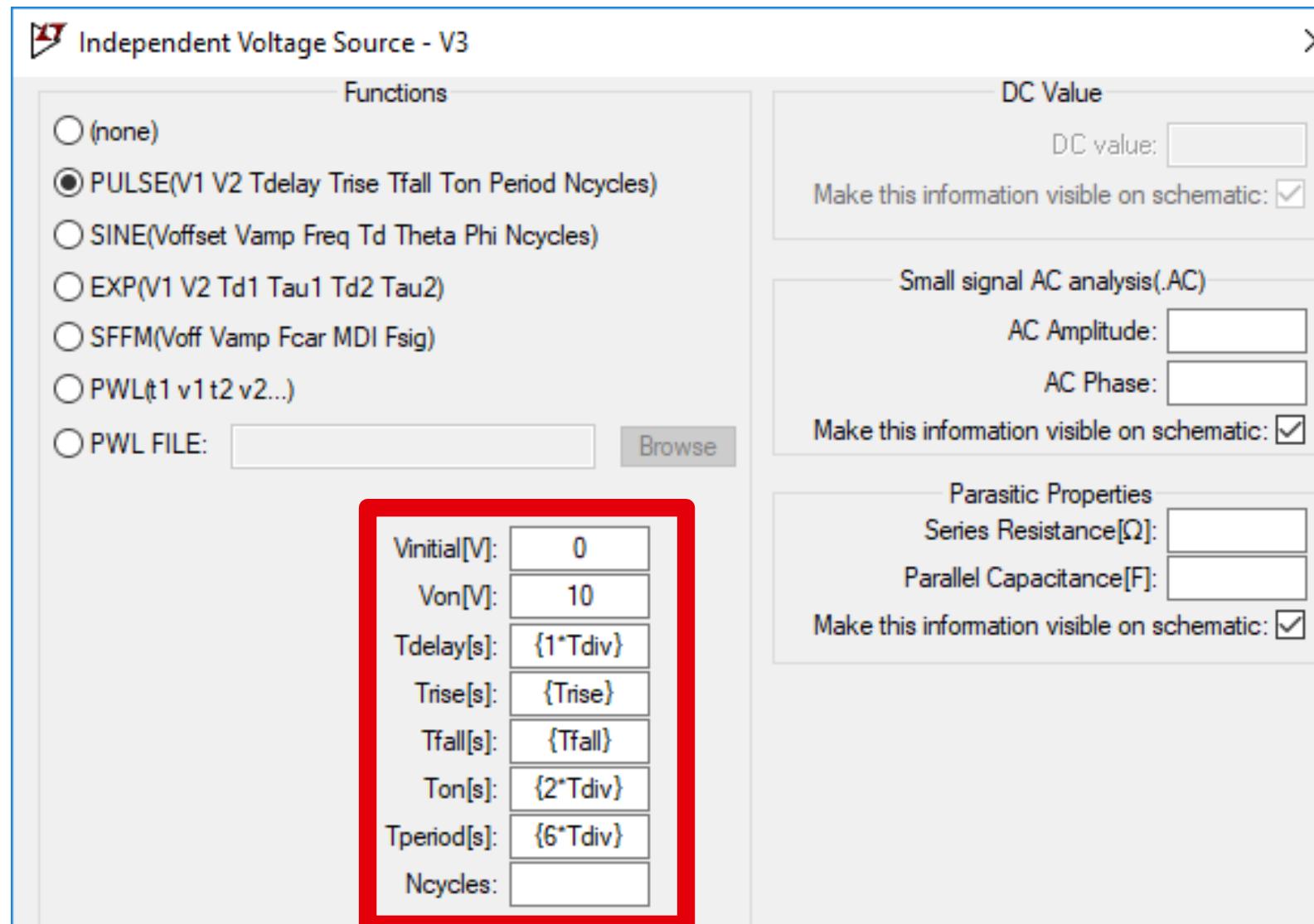
Real life examples

Mains voltage BLDC driver + motor

- Parametric simulation

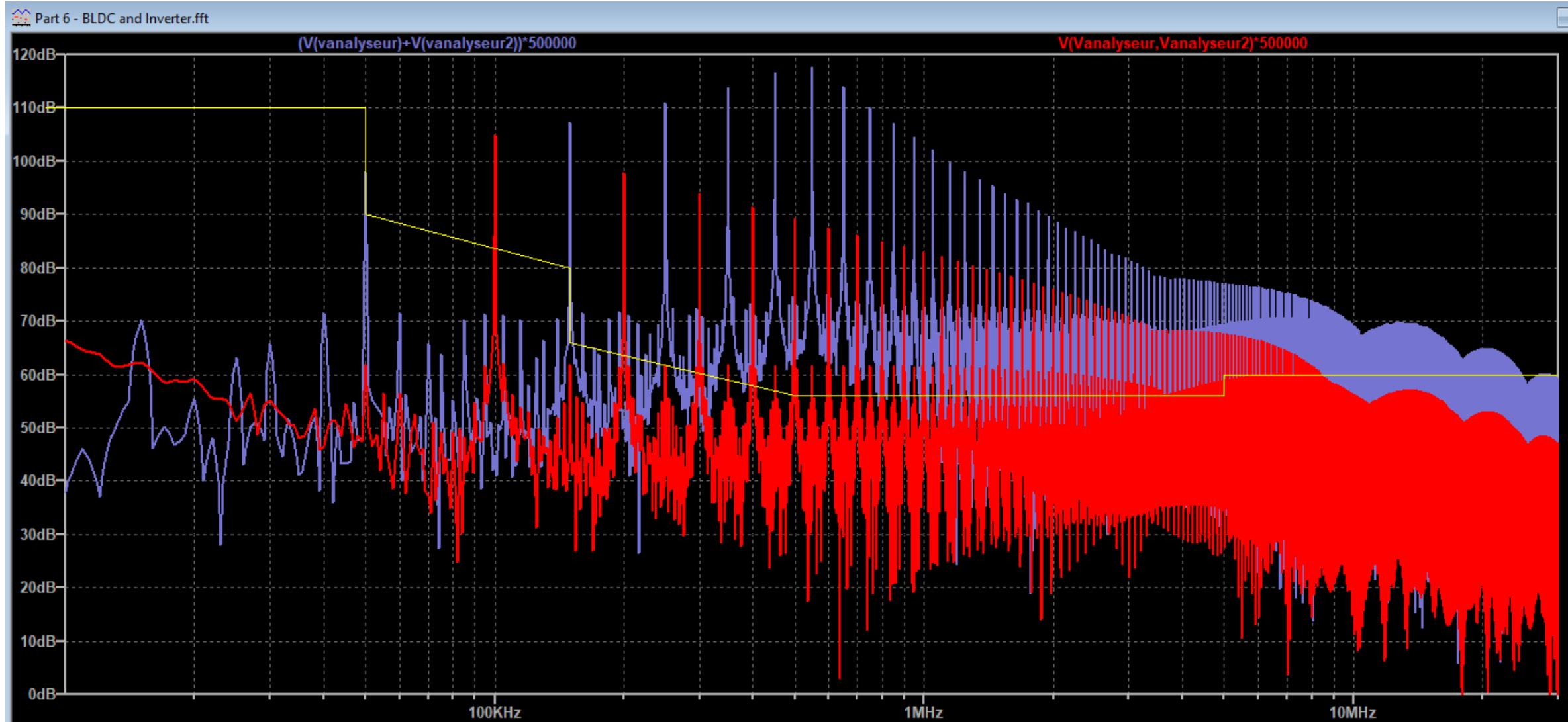
```
.param Trise=100ps Tfall=100ps Tdiv=10μs
```

- .STEP is possible to see impact of slew rate and dead time on EMC signature



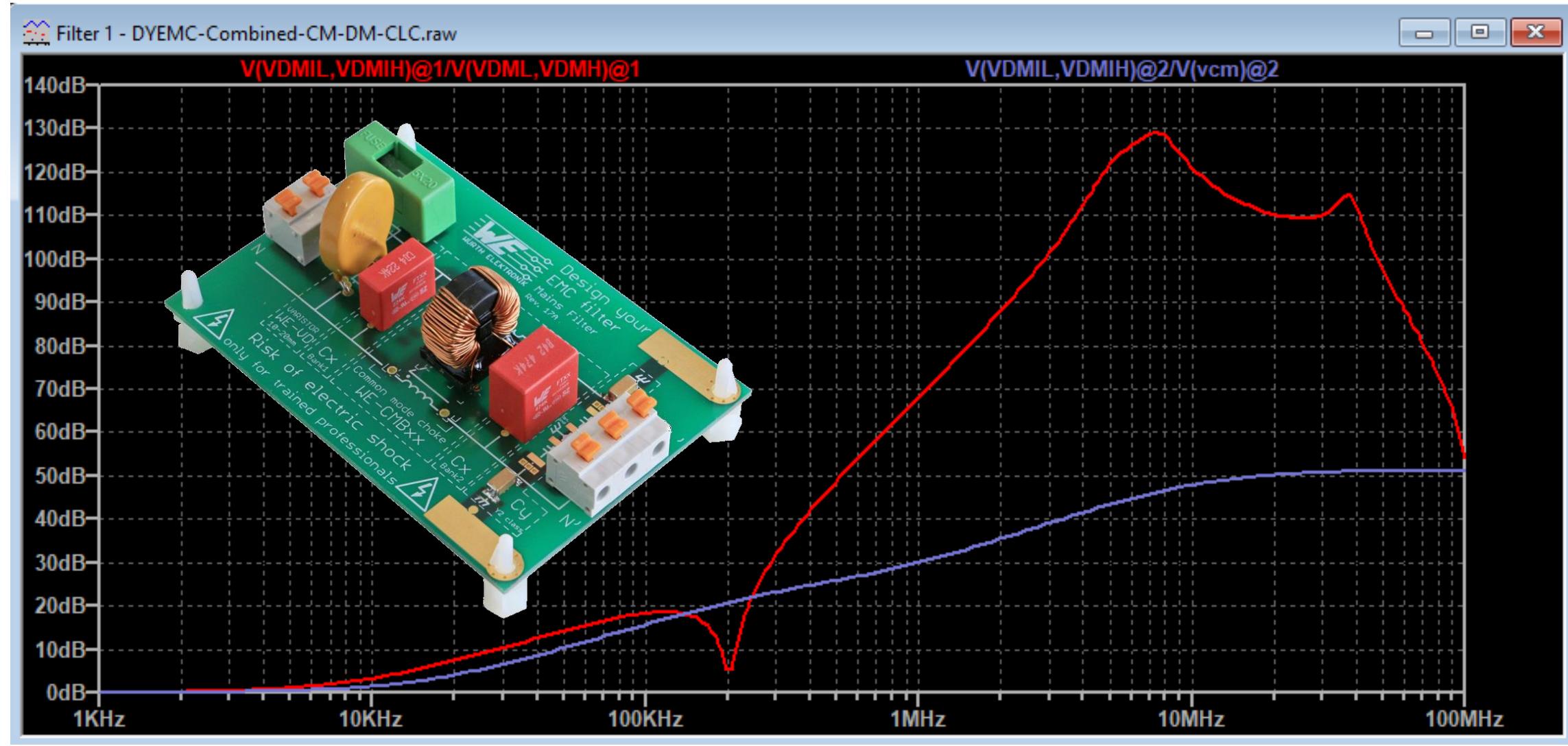
Real life examples

Mains voltage BLDC driver + motor



Evaluation of Filter Insertion losses

Design your EMC filter in LTspice



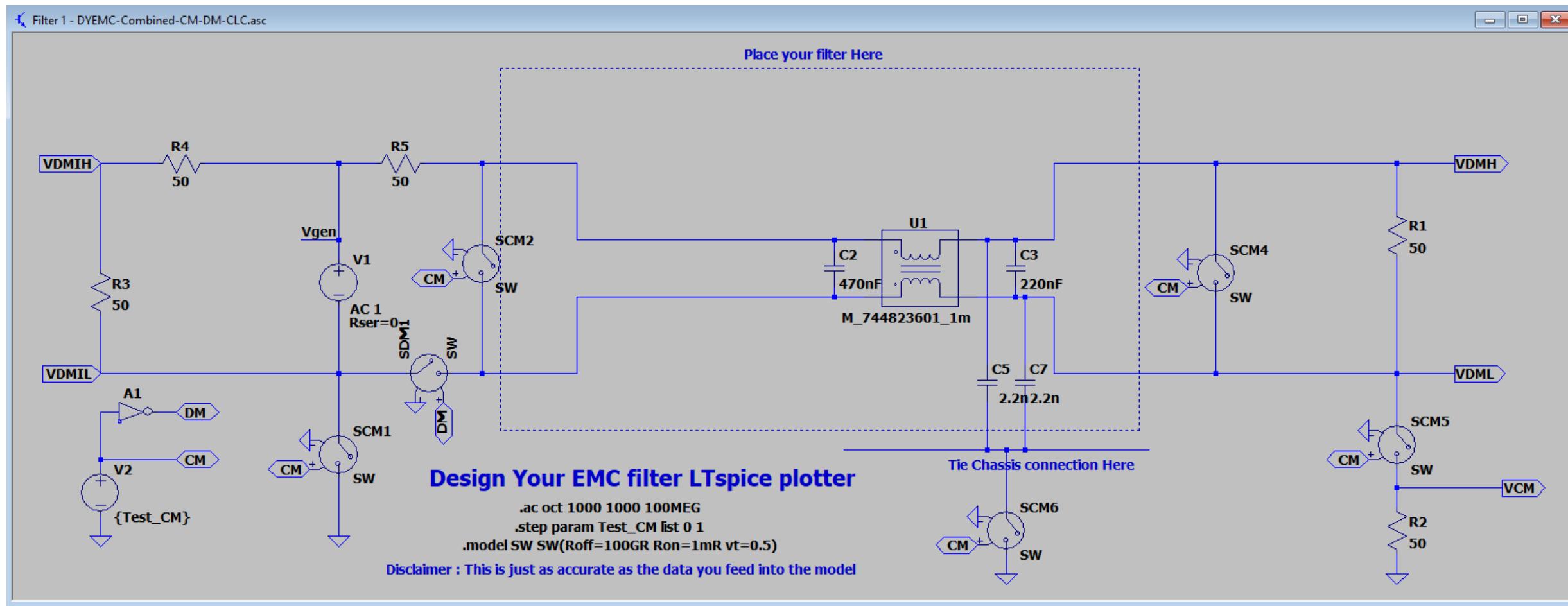
Evaluation of Filter Insertion losses

Design your EMC filter in LTspice



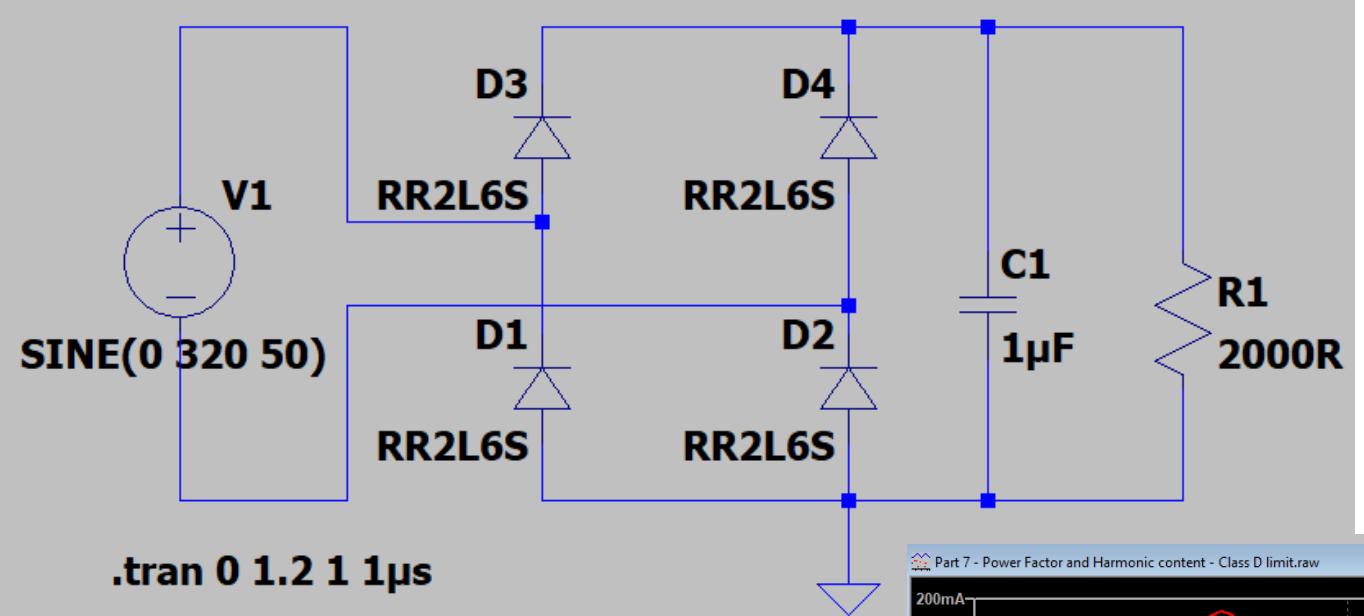
V(VDMIL,VDMIH)@1/V(VDML,VDMH)@1

V(VDMIL,VDMIH)@2/V(vcm)@2

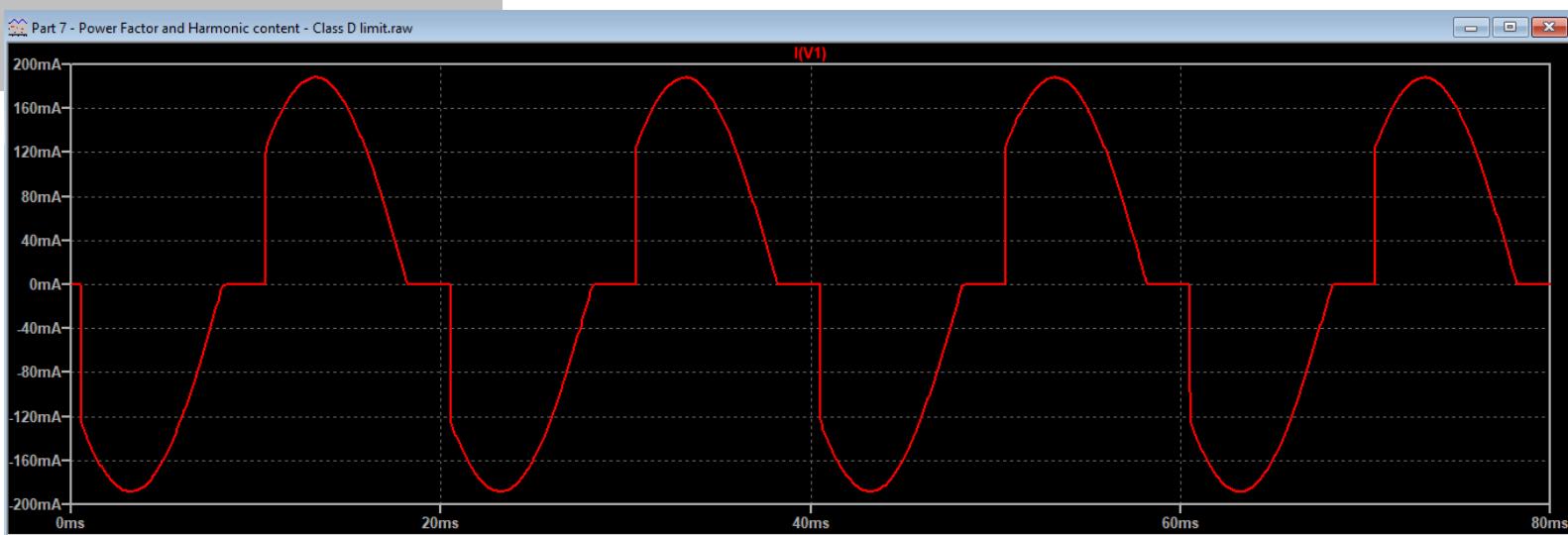


Power Factor and Harmonic current

Anticipate IEC 61000-3-2

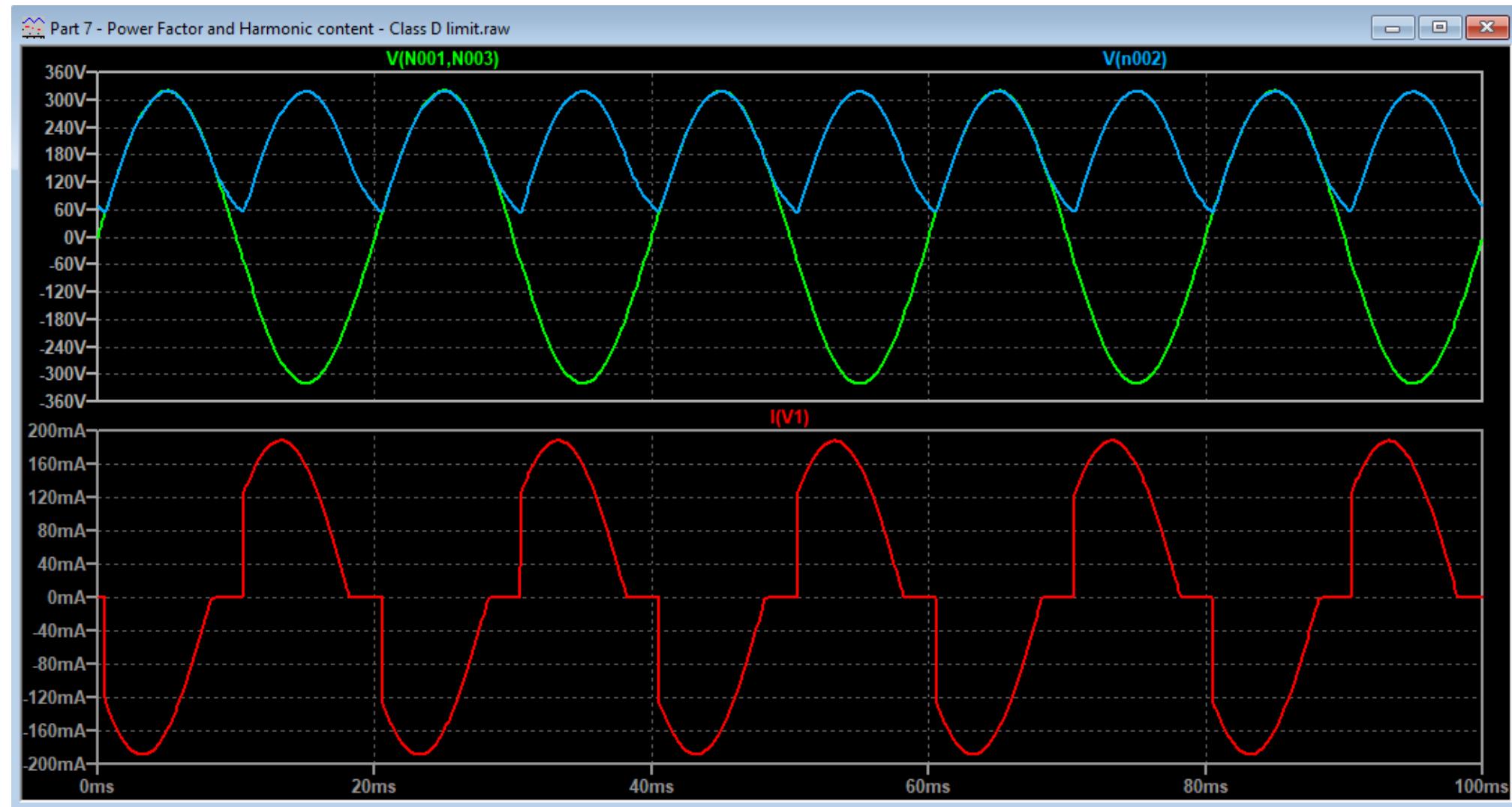


Harmonic order (n)	Maximum permissible harmonic current per watt (mA/W)
3	3.4
5	1.9
7	1.0
9	0.5
11	0.35
13	0.3
$15 \leq n \leq 39$ (odd harmonics only)	$3.85/n$



Power Factor and Harmonic current

Anticipate IEC 61000-3-2



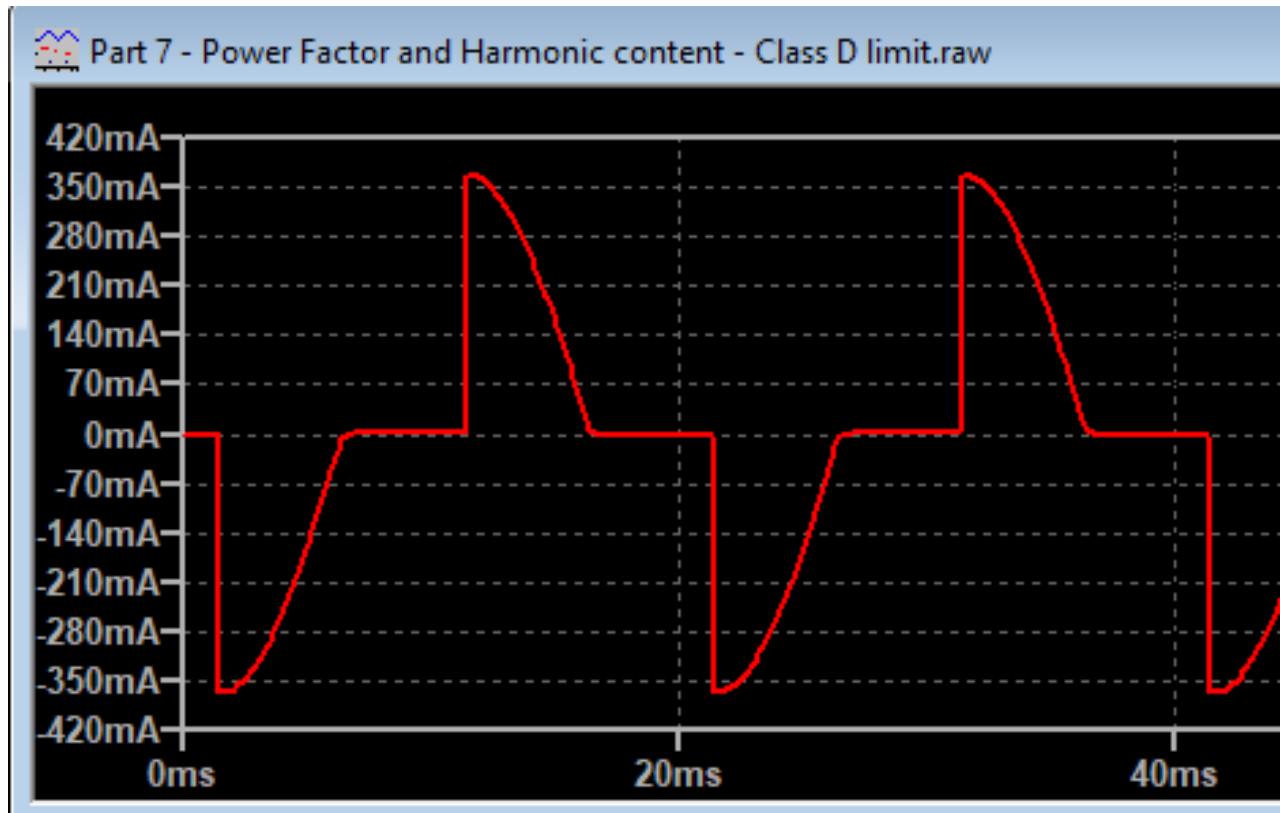
Power Factor and Harmonic current

Anticipate IEC 61000-3-2



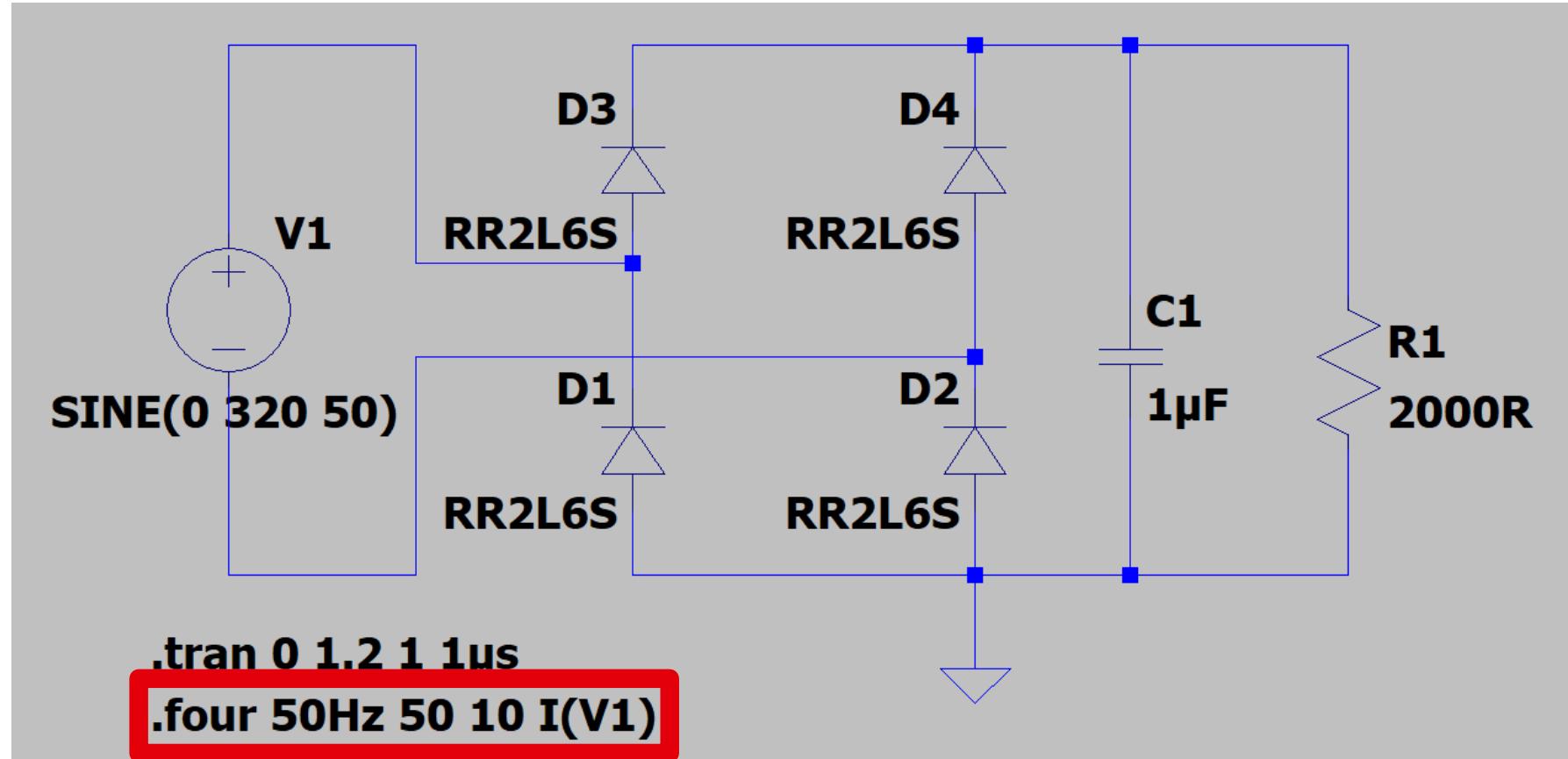
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13	0.3
$15 \leq n \leq 39$ (odd harmonics only)	$3.85/n$

?



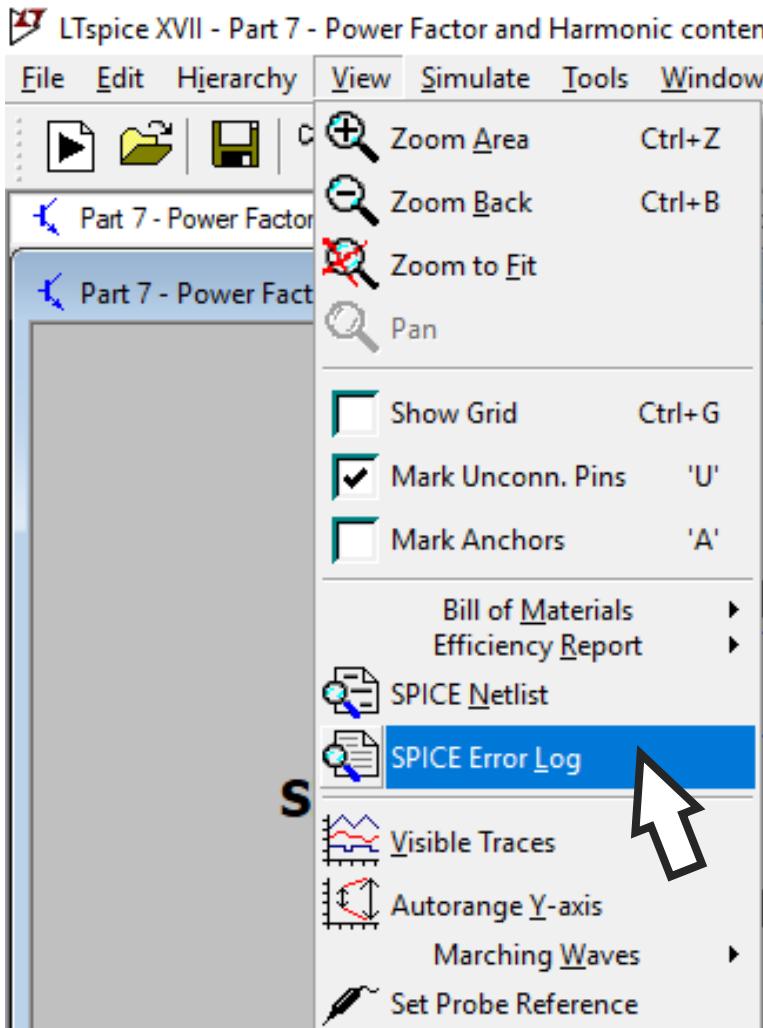
Power Factor and Harmonic current

.FOUR directive to Anticipate IEC 61000-3-2



Power Factor and Harmonic current

.FOUR directive to Anticipate IEC 61000-3-2



Fourier components of I(v1)			
Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component
1	5.000e+01	1.760e-01	1.000e+00
2	1.000e+02	3.265e-07	1.855e-06
3	1.500e+02	2.687e-02	1.526e-01
4	2.000e+02	1.123e-06	6.379e-06
5	2.500e+02	2.074e-02	1.178e-01
6	3.000e+02	2.040e-07	1.159e-06
7	3.500e+02	1.391e-02	7.904e-02
8	4.000e+02	9.960e-07	5.658e-06
9	4.500e+02	8.532e-03	4.847e-02
10	5.000e+02	9.480e-07	5.386e-06
11	5.500e+02	6.452e-03	3.665e-02
12	6.000e+02	7.110e-07	4.039e-06
13	6.500e+02	6.362e-03	3.614e-02
14	7.000e+02	1.526e-06	8.671e-06
15	7.500e+02	5.865e-03	3.332e-02
16	8.000e+02	4.225e-07	2.401e-06
17	8.500e+02	4.761e-03	2.705e-02
18	9.000e+02	1.168e-06	6.634e-06
19	9.500e+02	3.923e-03	2.229e-02
20	1.000e+03	8.830e-07	5.016e-06
21	1.050e+03	3.752e-03	2.131e-02
...
45	2.250e+03	1.732e-03	9.838e-03
46	2.300e+03	7.944e-07	4.513e-06
47	2.350e+03	1.685e-03	9.573e-03
48	2.400e+03	1.657e-07	9.416e-07
49	2.450e+03	1.657e-03	9.412e-03
50	2.500e+03	7.697e-07	4.373e-06
Total Harmonic Distortion: 23.211629% (23.614123%) PF=0.893698 (0.8929)			

Fraction of fundamental Ampera

Phase [degree]	Normalized Phase [deg]
-156.56°	0.00°
57.75°	214.31°
102.46°	259.01°
2.94°	159.50°
108.42°	264.98°
-164.89°	-8.33°
108.04°	264.59°
-63.52°	93.04°
93.80°	250.36°
125.74°	282.30°
64.05°	220.61°
-101.44°	55.12°
41.96°	198.52°
51.93°	208.48°
29.38°	185.94°
-89.14°	67.42°
14.64°	171.20°
-50.15°	106.41°
-8.40°	148.16°
-105.51°	51.05°
-31.96°	124.60°
120.51°	25.00°
98.91°	255.46°
-44.86°	111.70°
77.95°	234.51°
-81.86°	74.69°
59.24°	215.79°
-107.70°	48.86°

Power Factor and Harmonic current

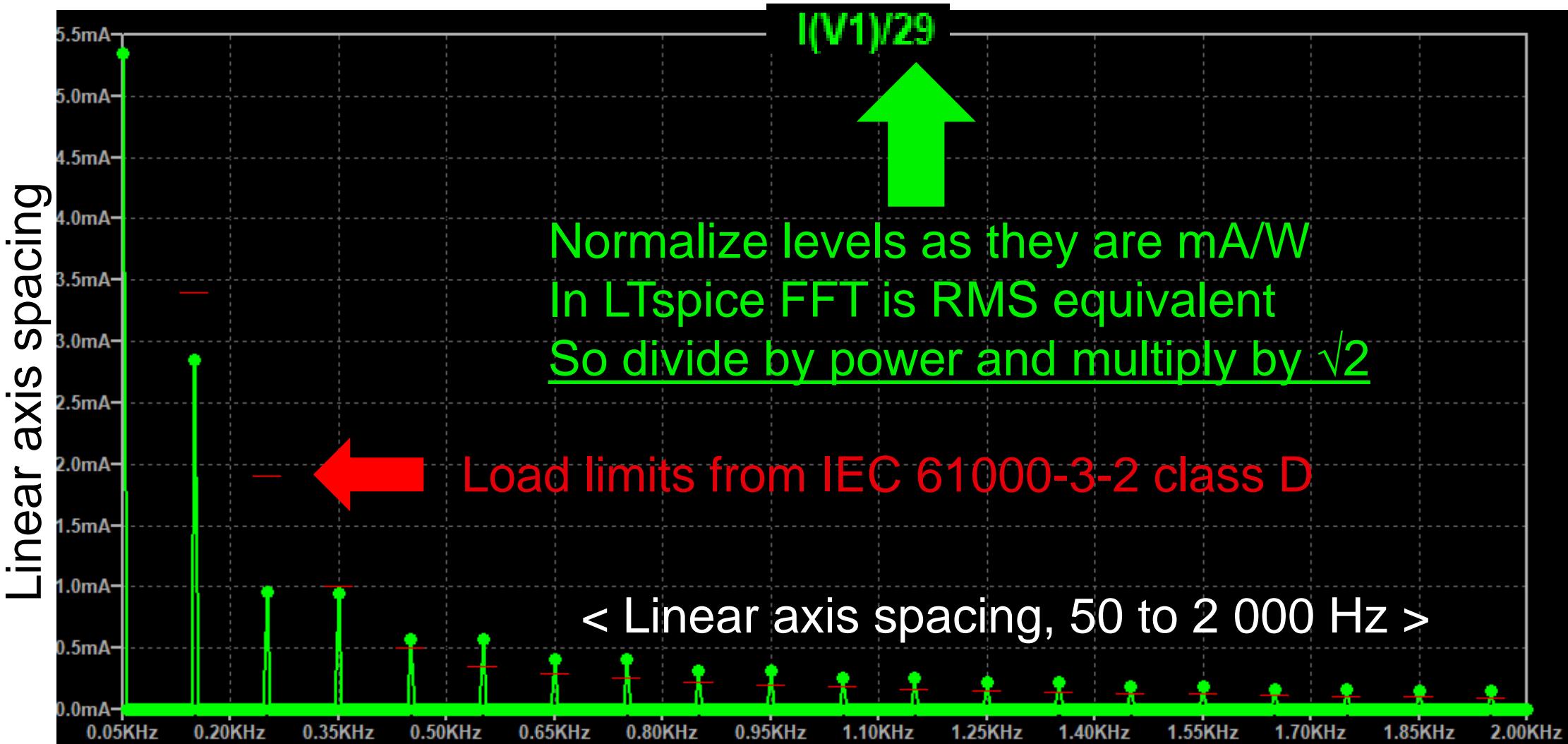
Graphical method to anticipate IEC 61000-3-2



IEC 61000-3-2 Class D - LTSpice limit line calculator					
in 50Hz base	Start Freq	End Freq	mA/W start	Line def for LTSPICE plot settings file	
Line 3	130	170	3.4	Line: "A" 40	(130,0.0034) (170,0.0034)
Line 5	230	270	1.9	Line: "A" 40	(230,0.0019) (270,0.0019)
Line 7	330	370	1	Line: "A" 40	(330,0.001) (370,0.001)
Line 9	430	470	0.5	Line: "A" 40	(430,0.0005) (470,0.0005)
Line 11	530	570	0.35	Line: "A" 40	(530,0.00035) (570,0.00035)
Line 13	630	670	0.296153846	Line: "A" 40	(630,0.000296153846153846) (670,0.000296153846153846)
Line 15	730	770	0.2566666667	Line: "A" 40	(730,0.00025666666666666667) (770,0.00025666666666666667)
Line 17	830	870	0.226470588	Line: "A" 40	(830,0.000226470588235294) (870,0.000226470588235294)
Line 19	930	970	0.202631579	Line: "A" 40	(930,0.000202631578947368) (970,0.000202631578947368)
Line 21	1030	1070	0.1833333333	Line: "A" 40	(1030,0.0001833333333333) (1070,0.0001833333333333)
Line 23	1130	1170	0.167391304	Line: "A" 40	(1130,0.000167391304347826) (1170,0.000167391304347826)
Line 25	1230	1270	0.154	Line: "A" 40	(1230,0.000154) (1270,0.000154)
Line 27	1330	1370	0.142592593	Line: "A" 40	(1330,0.000142592592592593) (1370,0.000142592592592593)
Line 29	1430	1470	0.132758621	Line: "A" 40	(1430,0.000132758620689655) (1470,0.000132758620689655)
Line 31	1530	1570	0.124193548	Line: "A" 40	(1530,0.000124193548387097) (1570,0.000124193548387097)
Line 33	1630	1670	0.1166666667	Line: "A" 40	(1630,0.000116666666666667) (1670,0.000116666666666667)
Line 35	1730	1770	0.11	Line: "A" 40	(1730,0.00011) (1770,0.00011)
Line 37	1830	1870	0.104054054	Line: "A" 40	(1830,0.000104054054054054) (1870,0.000104054054054054)
Line 39	1930	1970	0.098717949	Line: "A" 40	(1930,9.87179487179487E-05) (1970,9.87179487179487E-05)

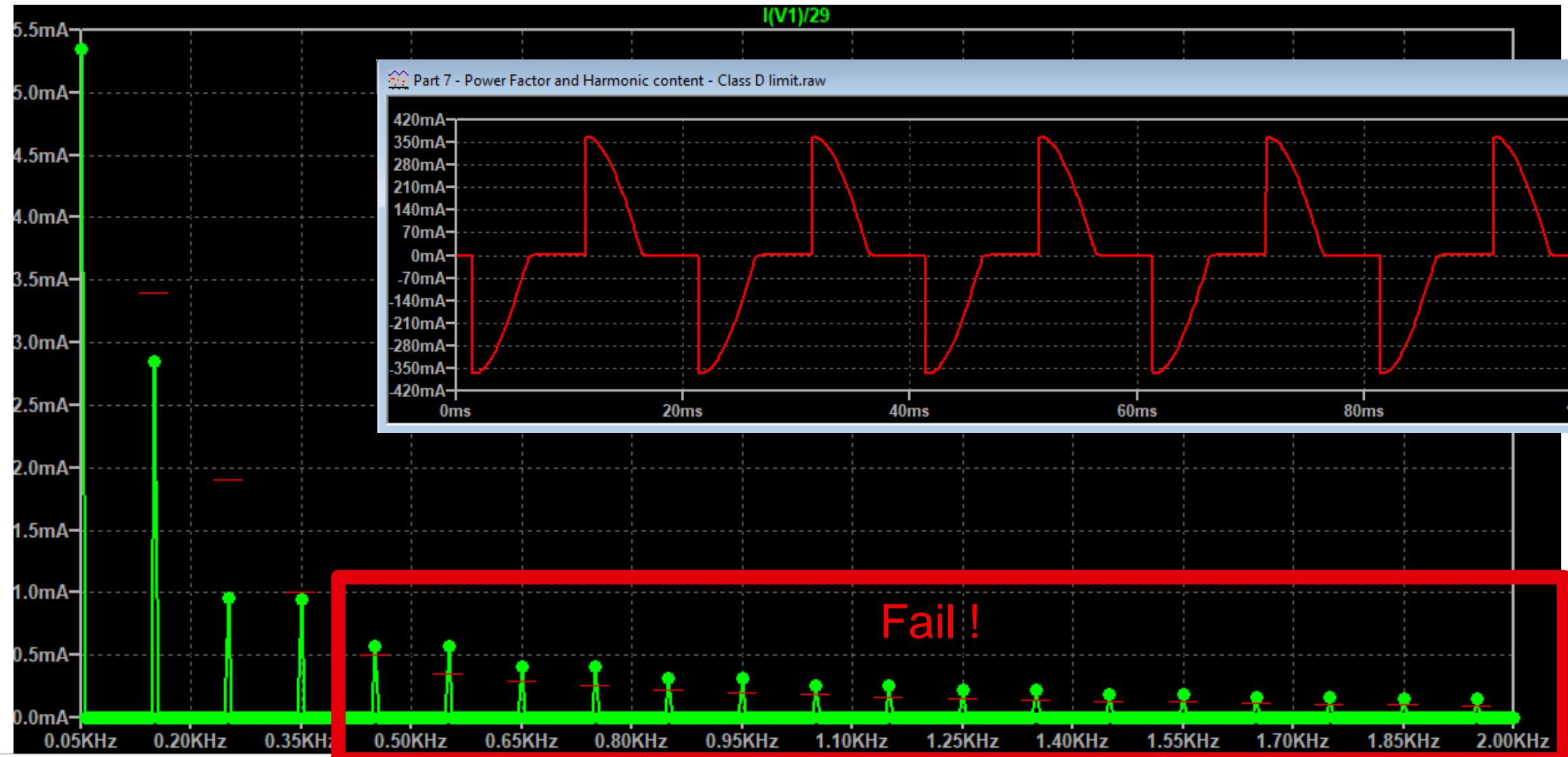
Power Factor and Harmonic current

Graphical method to anticipate IEC 61000-3-2



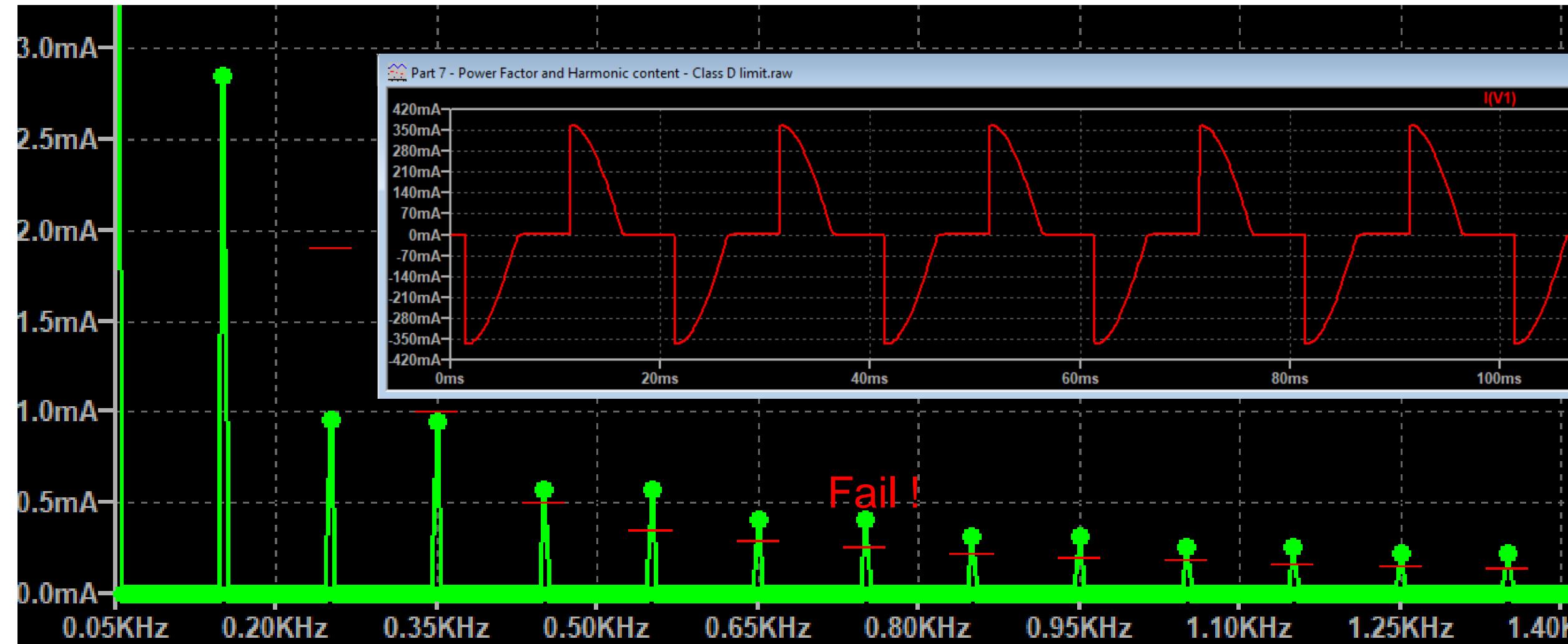
Power Factor and Harmonic current

Graphical method to anticipate IEC 61000-3-2



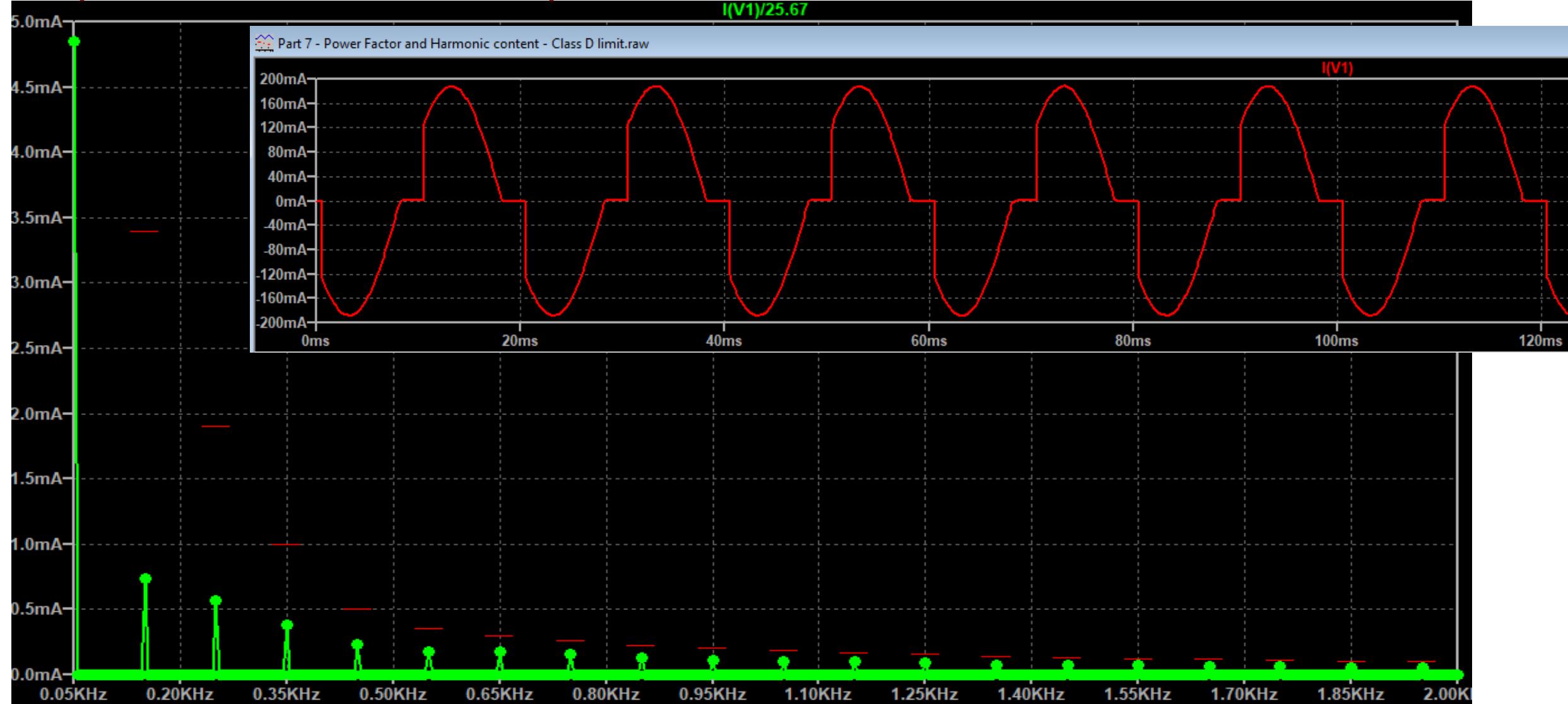
Power Factor and Harmonic current

Graphical method to anticipate IEC 61000-3-2



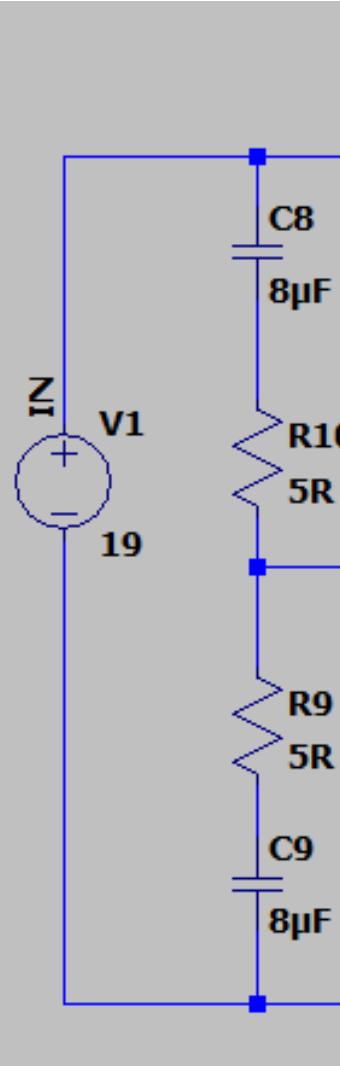
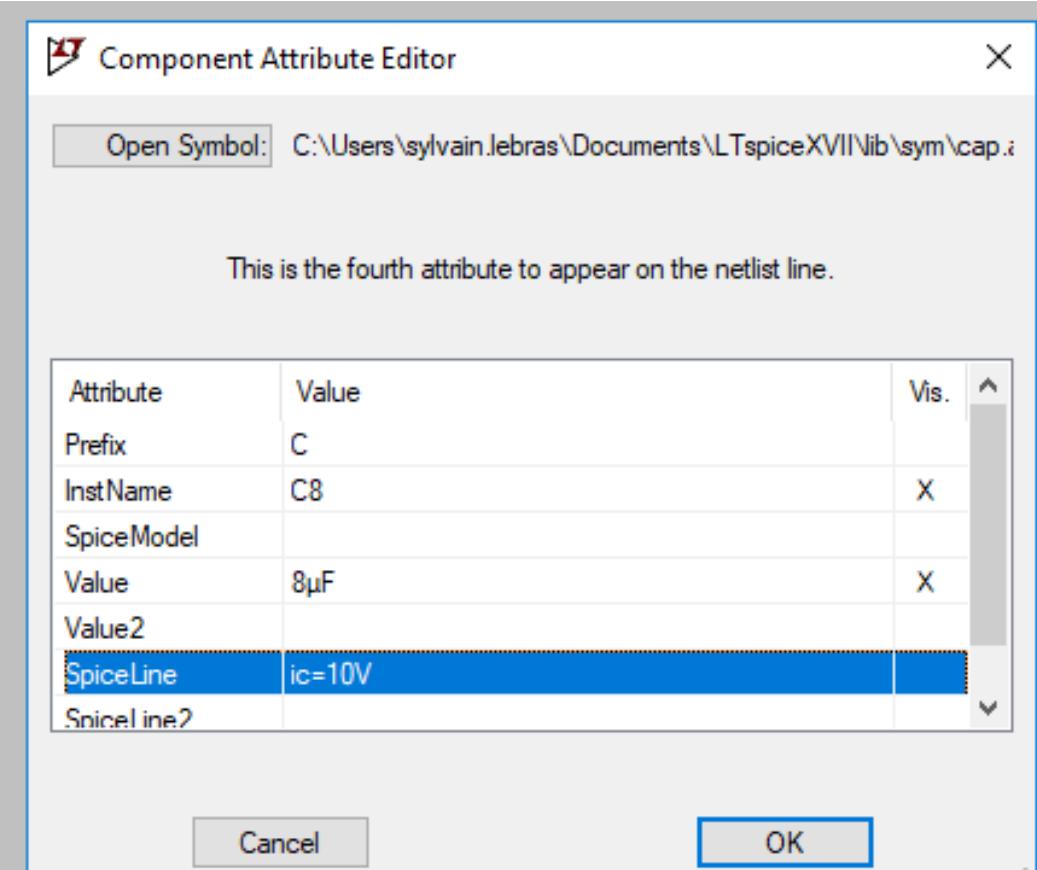
Power Factor and Harmonic current

Graphical method to anticipate IEC 61000-3-2



Good to know

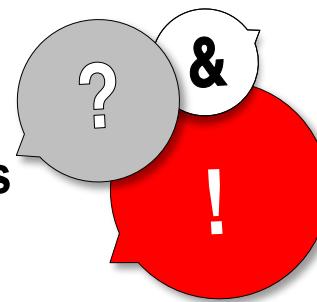
Speed up simulations



Setting initial condition

- Ctrl + Right Click
- SpiceLine
 - $ic=10V$

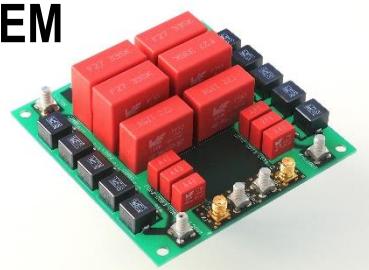
Questions & Réponses



Si vous souhaitez approfondir un des sujets ou avoir la modélisation d'un cas non traité aujourd'hui faites nous un retour nous organiserons une session de formation

Avec plus de 200 inscrits il y aura beaucoup de questions, les réponses peuvent prendre un peu de temps

Les schémas, BOM, Gerbers du matériel CEM seront rendus disponibles sur GitHub



Sylvain.LeBras@we-online.com



Vous recevezz un lien avec les fichiers utilisés pendant cette présentation

- Part 1 - Testfixture.asc
- Part 1 - Testfixture.plt
- Part 2 - Modified Testfixture - 1 output voltage.plt
- Part 2 - Modified Testfixture - 2 Breakdown.plt
- Part 2 - Modified Testfixture.asc
- Part 2 - Modified Testfixture.plt
- Part 3 - Ripple-Input-MD.asc
- Part 3 - Ripple-Input-MD-1 Time based display.plt
- Part 3 - Ripple-Input-MD-2 Frequency based display.plt
- Part 3 - Ripple-Input-MD-4 Frequency based display Breakdown.plt
- Part 4 - DM and CM of Buck - 1 FFT analysis.plt
- Part 4 - DM and CM of Buck - 2 Time based CMDM split.plt
- Part 4 - DM and CM of Buck - 3 FFT display of CMDM split.plt
- Part 4 - DM and CM of Buck.asc
- Part 4bis - DM and CM of Buck - Fixed.asc
- Part 5 - Flyback converter - 1 FFT split analysis.plt
- Part 5 - Flyback converter.asc
- Part 6 - BLDC and Inverter.asc
- Part 6 - BLDC and Inverter.log
- Part 6 - BLDC and Inverter.op.raw
- Part 7 - Power Factor and Harmonic content - Class D limit.asc
- Part 7 - Power Factor and Harmonic content - Class D limit.log
- Part 7 - Power factor and Harmonic content.plt
- Part 8 - DYEMC-Combined-CM-DM-CLC.asc
- Part 8 - DYEMC-Combined-CM-DM-CLC.plt