



Anticipate EMC with LTSPICE

Today's speakers:



Sylvain Le Bras

Field Application Engineer
Sylvain.LeBras@we-online.de
www.we-online.de



Markus Eberle

Marketing
Markus.Eberle@we-online.de
www.we-online.de



Listeners are muted



You are muted during the webinar.
However, you can ask us questions
using the chat function

Information about the Webinar



Duration of the presentation : **30 Min**
Qs & As: **10 - 15 Min**



Any questions?
No problem! Email us: **eiSos-webinar@we-online.com**



Please help us to optimize our webinars!
We are looking forward to your feedback.



On our channel
And on

Würth Elektronik Group
www.we-online.com/webinars

Anticipate EMC with LTSpice

Using LTSPICE and Redexpert to check power supply designs

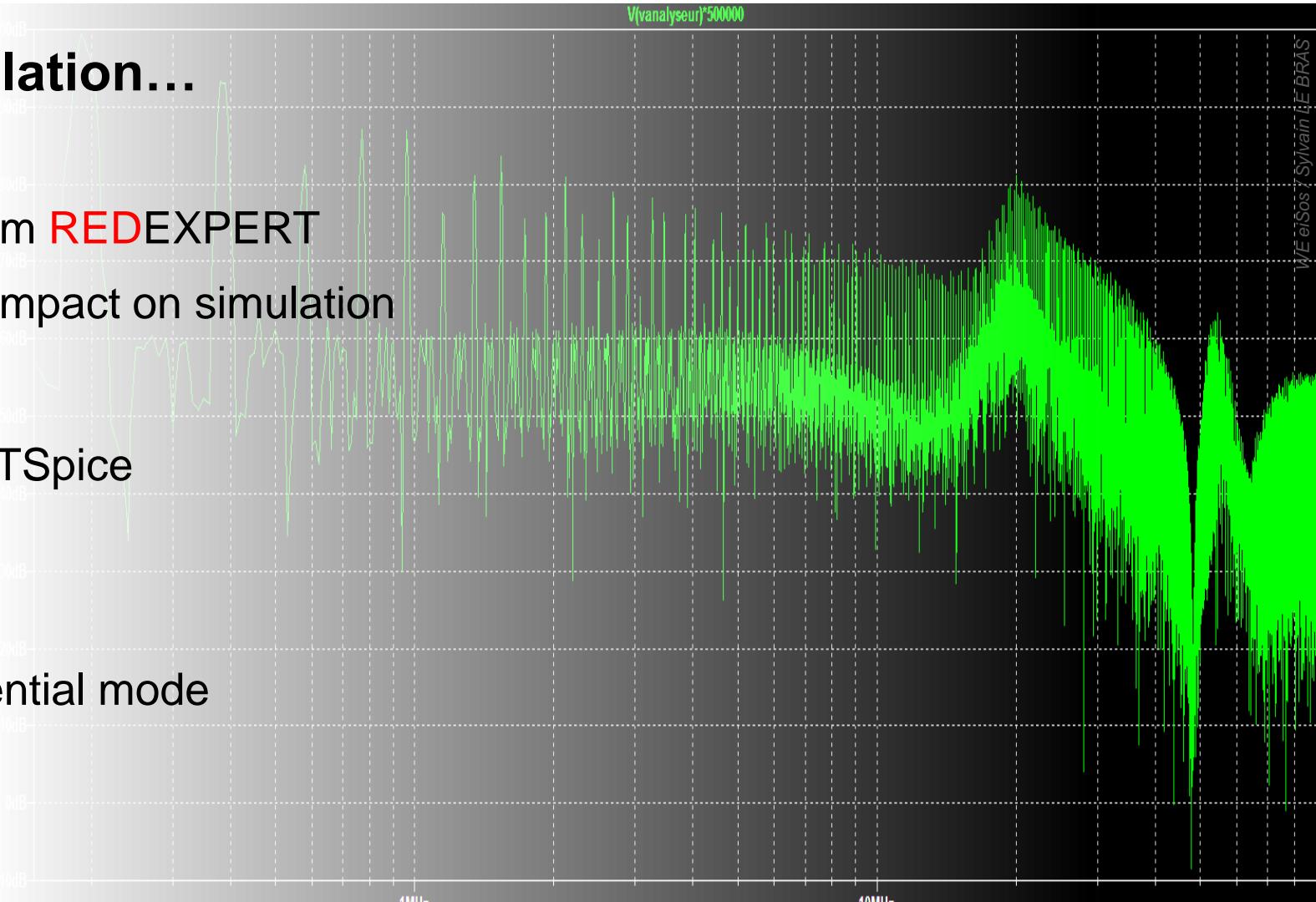


- Intro : From functional simulation...

- Output ripple of a Buck
- Extracting EMC accurate data from REDEXPERT
- Example of (non) EMC accurate impact on simulation

- ...To EMC simulation

- Enabling EMC measurement in LTSpice
- Getting Seriously Accurate ?
- Going further with simulation
 - Splitting Common and Differential mode
 - Making simulation look real
- Examples



Setup

Getting the tools ready



NOW PART OF



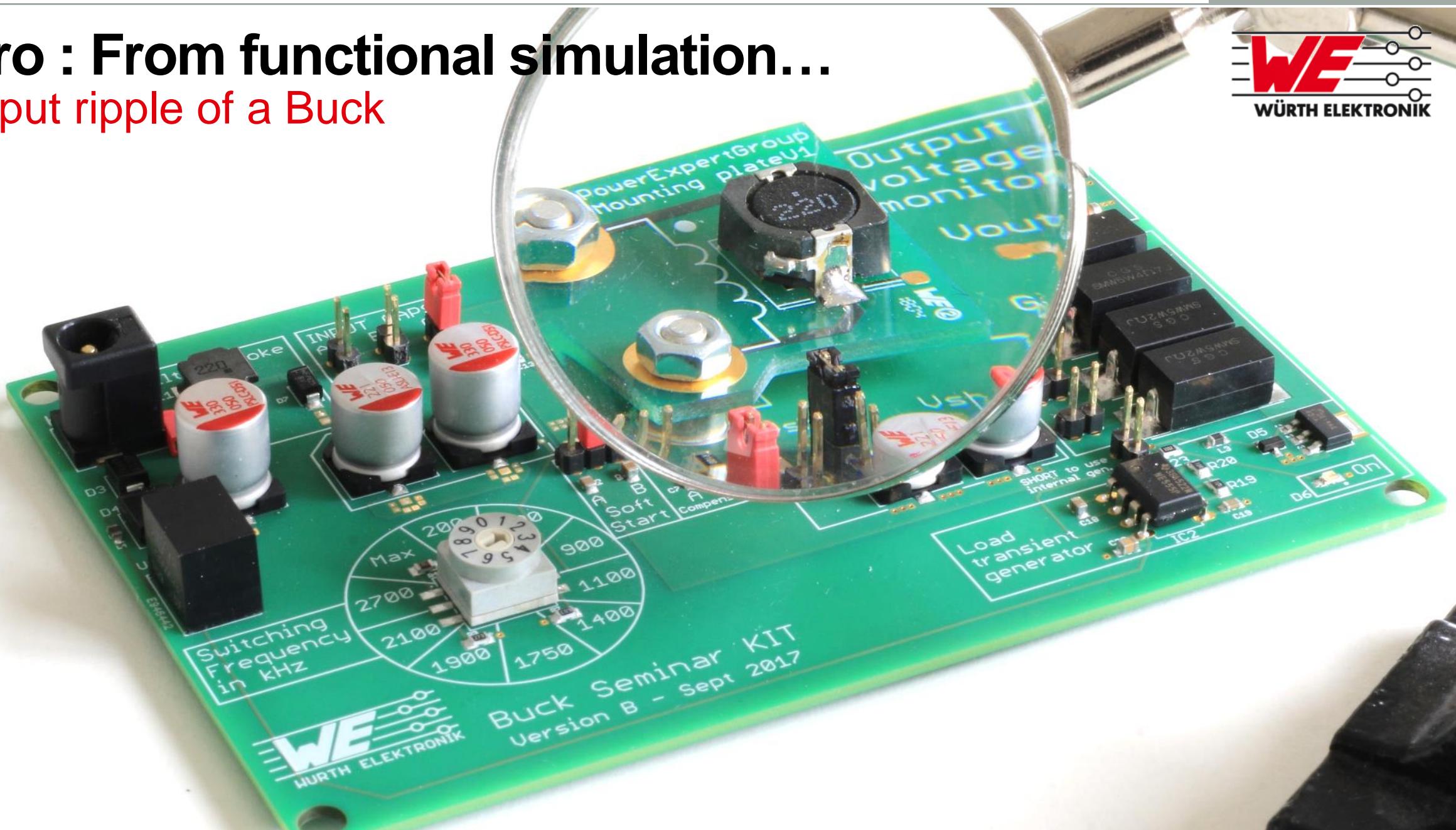
<https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html>

RED EXPERT

<https://www.we-online.com/redexpert>

Intro : From functional simulation...

Output ripple of a Buck



Intro : From functional simulation...

Output ripple of a Buck



The image shows the LTspice XVII software interface. On the left, a schematic diagram of a buck converter circuit is visible, featuring a yellow LT3975 component model. The LT3975 component has the following pin connections:

- EN (Pin 1) to GND
- Vin (Pin 2) to Power Source
- OUT (Pin 3)
- PG (Pin 4) to GND
- SS (Pin 5) to GND
- Boost (Pin 6)
- Rt (Pin 7) to GND
- SW (Pin 8)
- FB (Pin 9) to GND

A small red "LT" logo is located near the center of the LT3975 component. To the right of the schematic, a modal dialog box from LTspice XVII provides detailed information about the component:

LTspice XVII

42V, 2.5A, 2MHz Step-Down Switching Regulator with
2.7 μ A Quiescent Current
Note: Sync pin is not modeled; Burst Mode is selected.

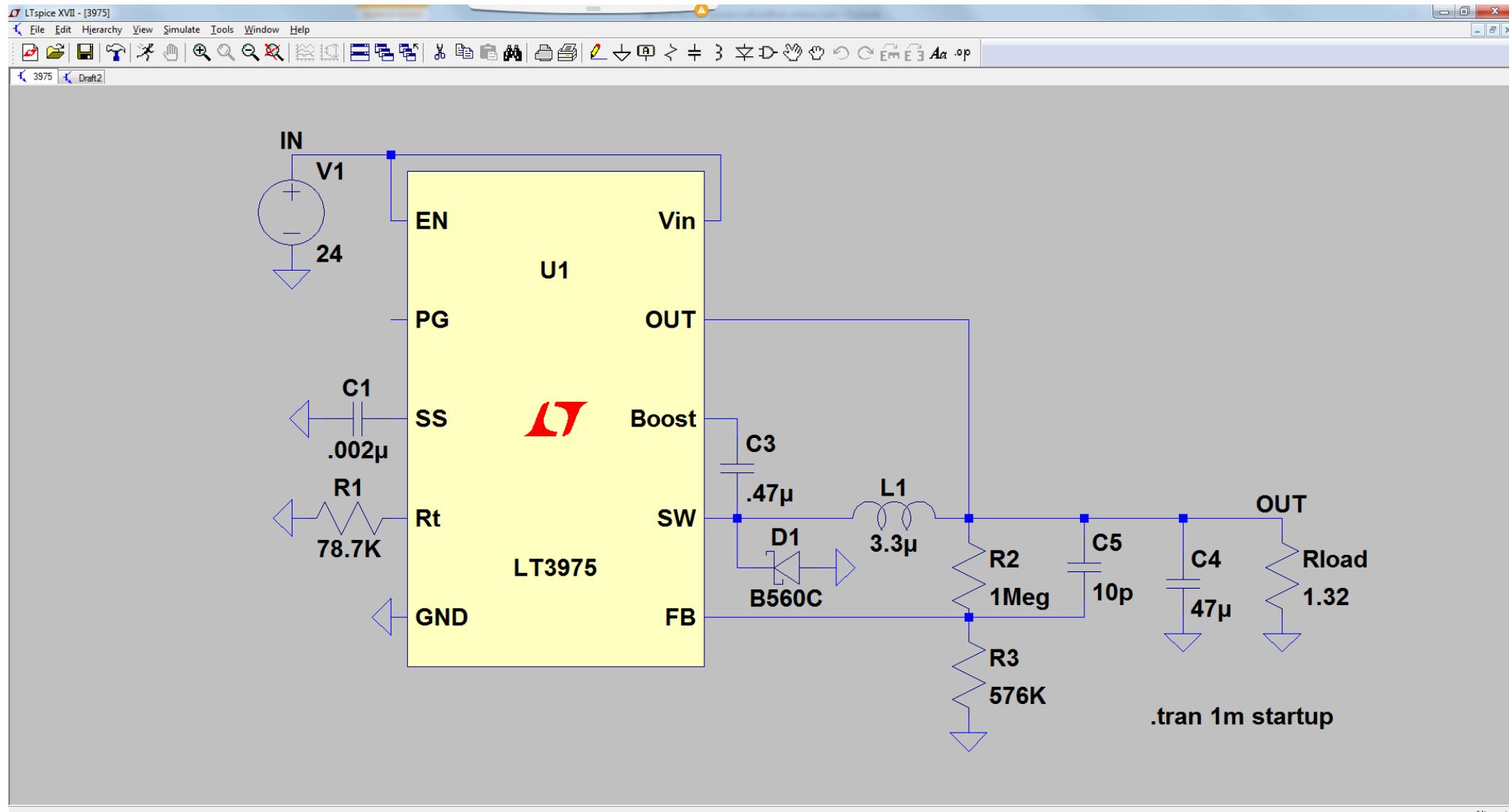
[Open this macromodel's test fixture](#)

[Go to Linear's website for datasheet](#)

[Cancel](#)

Intro : From functional simulation...

Output ripple of a Buck

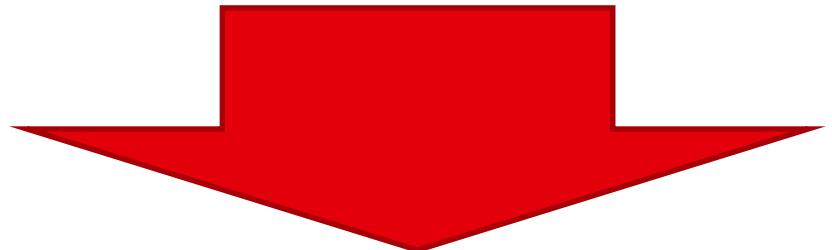


Output ripple of a Buck

Hardcore maths ?



$$V = R \cdot I$$



$$\Delta V = Z_C \cdot \Delta I_L$$

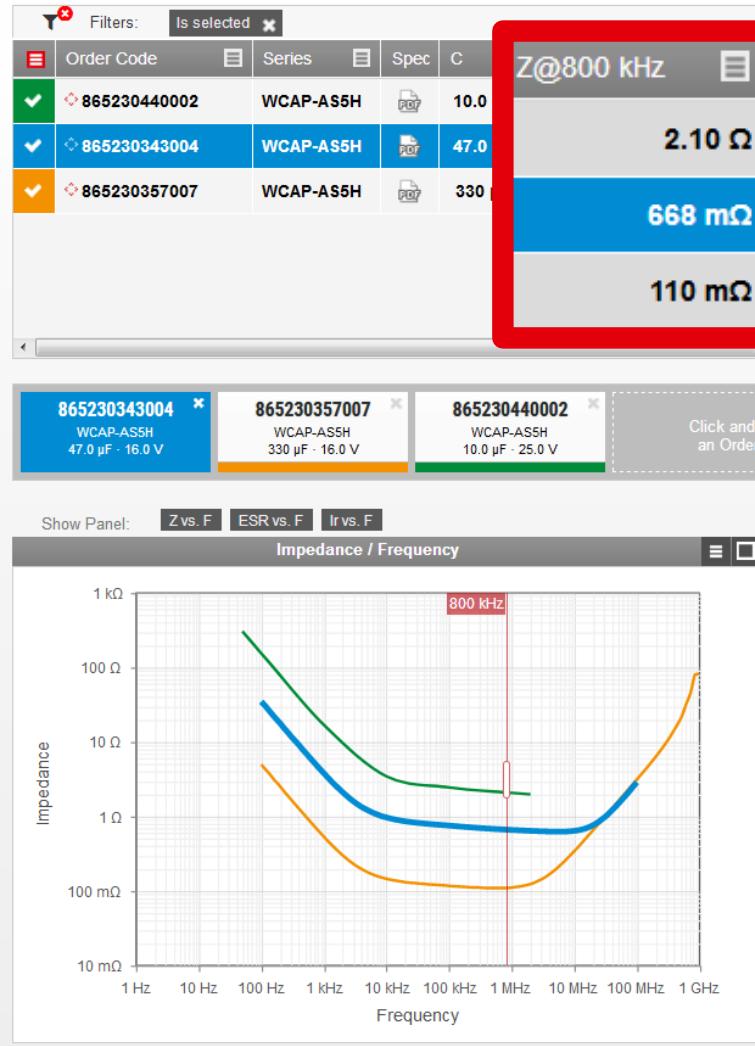
Output ripple of a Buck

Redexpert : an ode to laziness



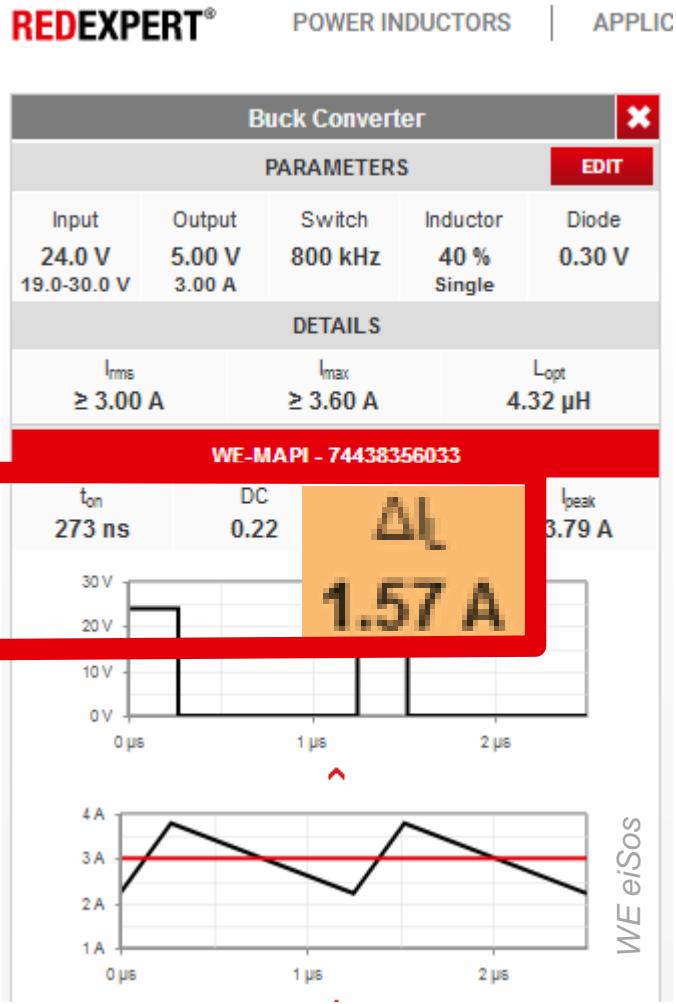
REDEXPERT® ALUMINIUM ELECTROLYTIC CAPACITORS

APPLICATIONS



ZC

ΔIL



Output ripple of a Buck

Redexpert : an ode to laziness

REDEXPERT® ALUMINIUM ELECTROLYTIC CAPACITORS | APPLICATIONS | HOW TO |  SHARE

 ITEMS  LE BRAS

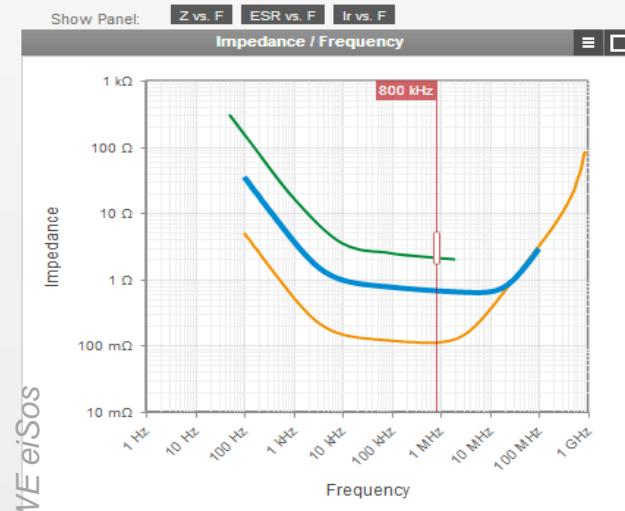
Order Code	Series	C	V _R	Z@800 kHz	DF	Z _{max} @ 100kHz	I _{ripple} @ T _{max} 120Hz	I _{ripple} @ T _{max} 100kHz	Description	I _{leak}
865230440002	WCAP-AS5H	10.0 μ F	25.0 V	2.10 Ω	< 16 %		23.0 mA		ASDB055100M025DVCTAE000	3.00
865230343004	WCAP-AS5H	47.0 μ F	16.0 V	668 m Ω	< 22 %		50.0 mA		ASDD055470M016DVCTBE000	7.52
865230357007	WCAP-AS5H	330 μ F	16.0 V	110 m Ω	< 22 %		300 mA		ASDF105331M016DVCTEE000	52.8

Filters: Is selected 

Click and type or drop an Order Code here  Add to Cart 

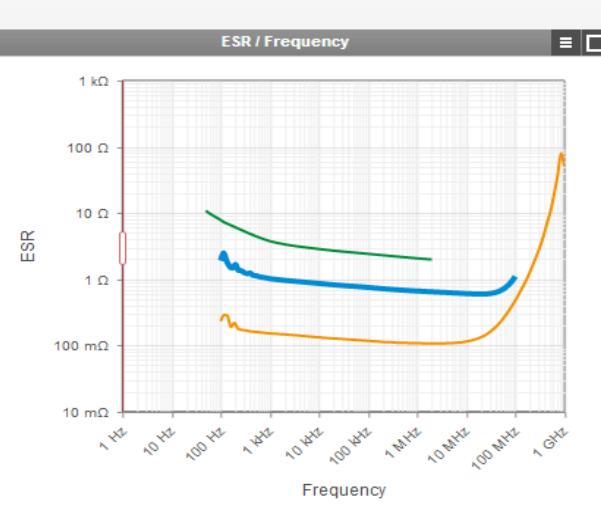
Show Panel: Z vs. F ESR vs. F Ir vs. F

Impedance / Frequency

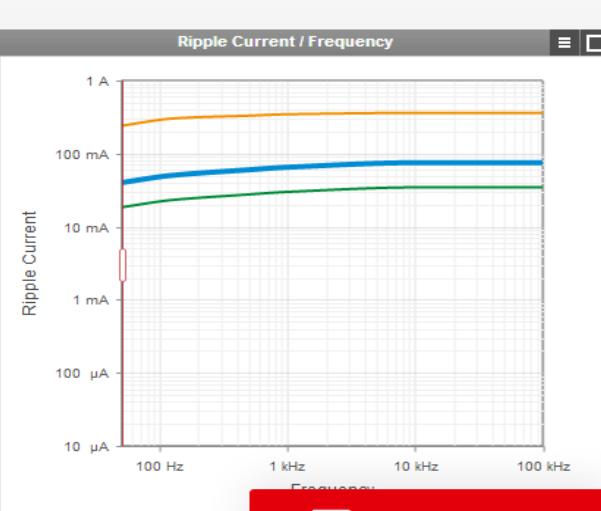


WE eiSos

ESR / Frequency



Ripple Current / Frequency



 Schreiben Sie uns

ABOUT WÜRTH ELEKTRONIK SITEMAP CONTACT IMPRINT COPYRIGHT © 2018 WÜRTH ELEKTRONIK GMBH. ALL RIGHTS RESERVED.

[Link](#)

Output ripple of a Buck

Redexpert : an ode to laziness



REDEXPERT®

POWER INDUCTORS

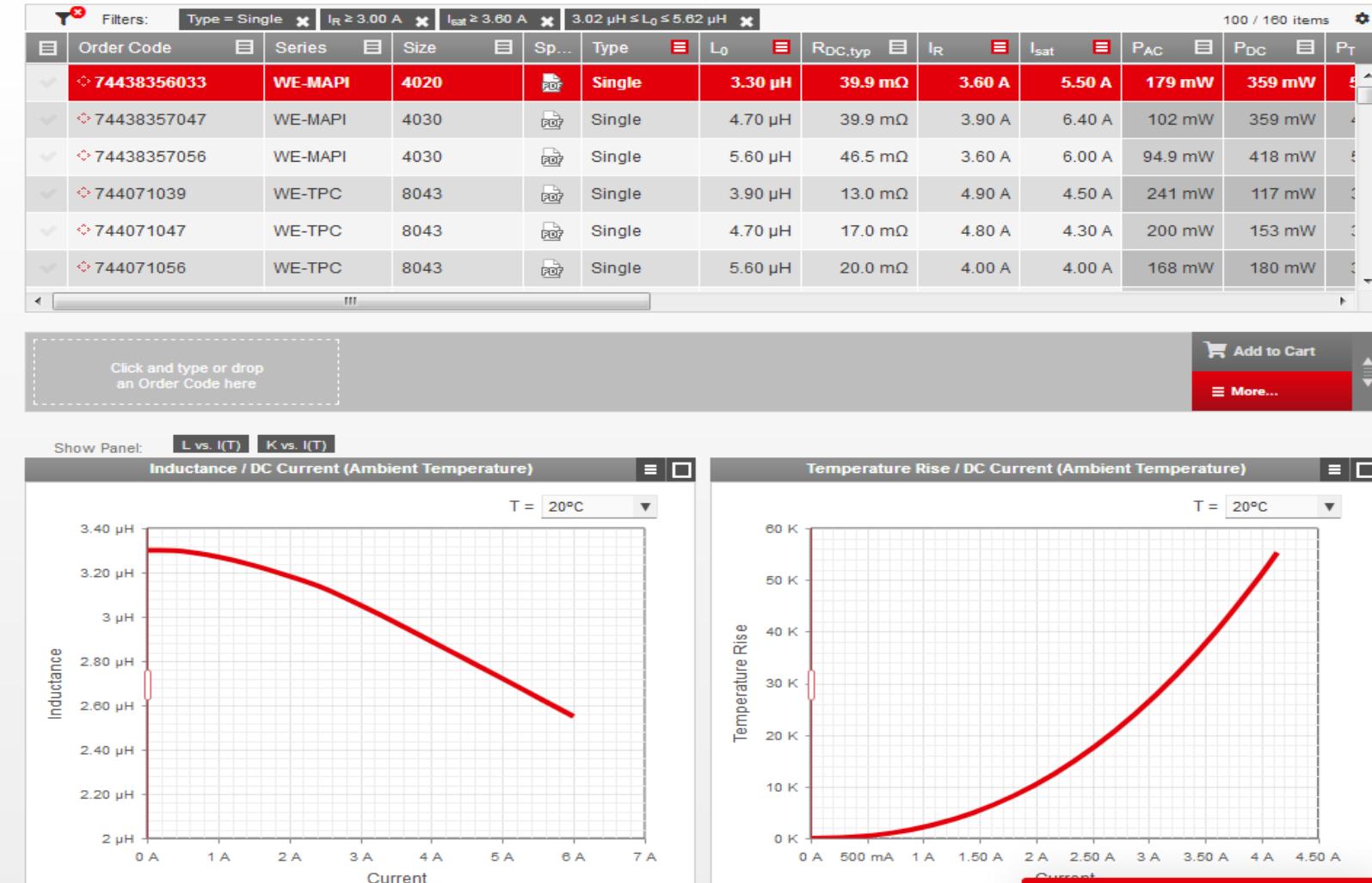
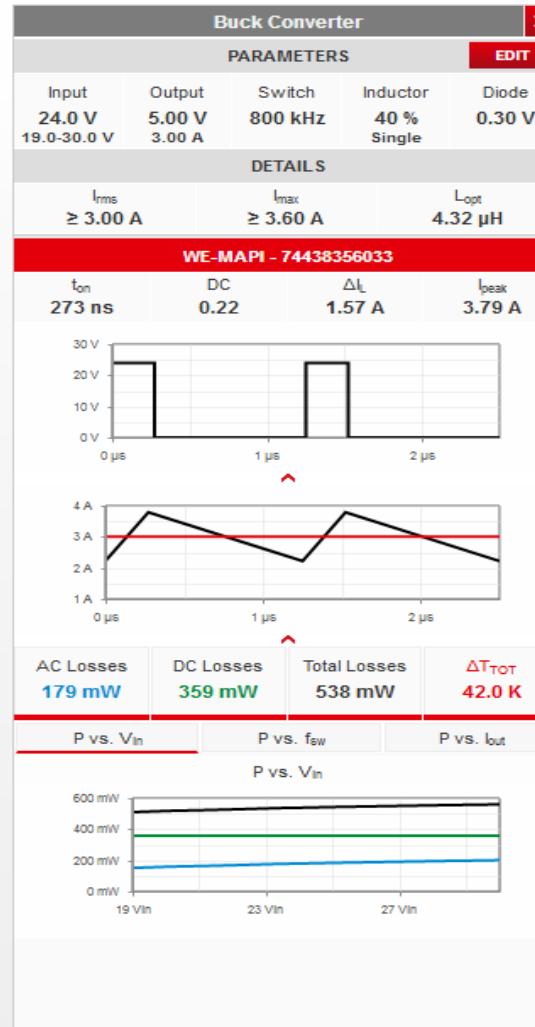
APPLICATIONS

HOW TO

SHARE

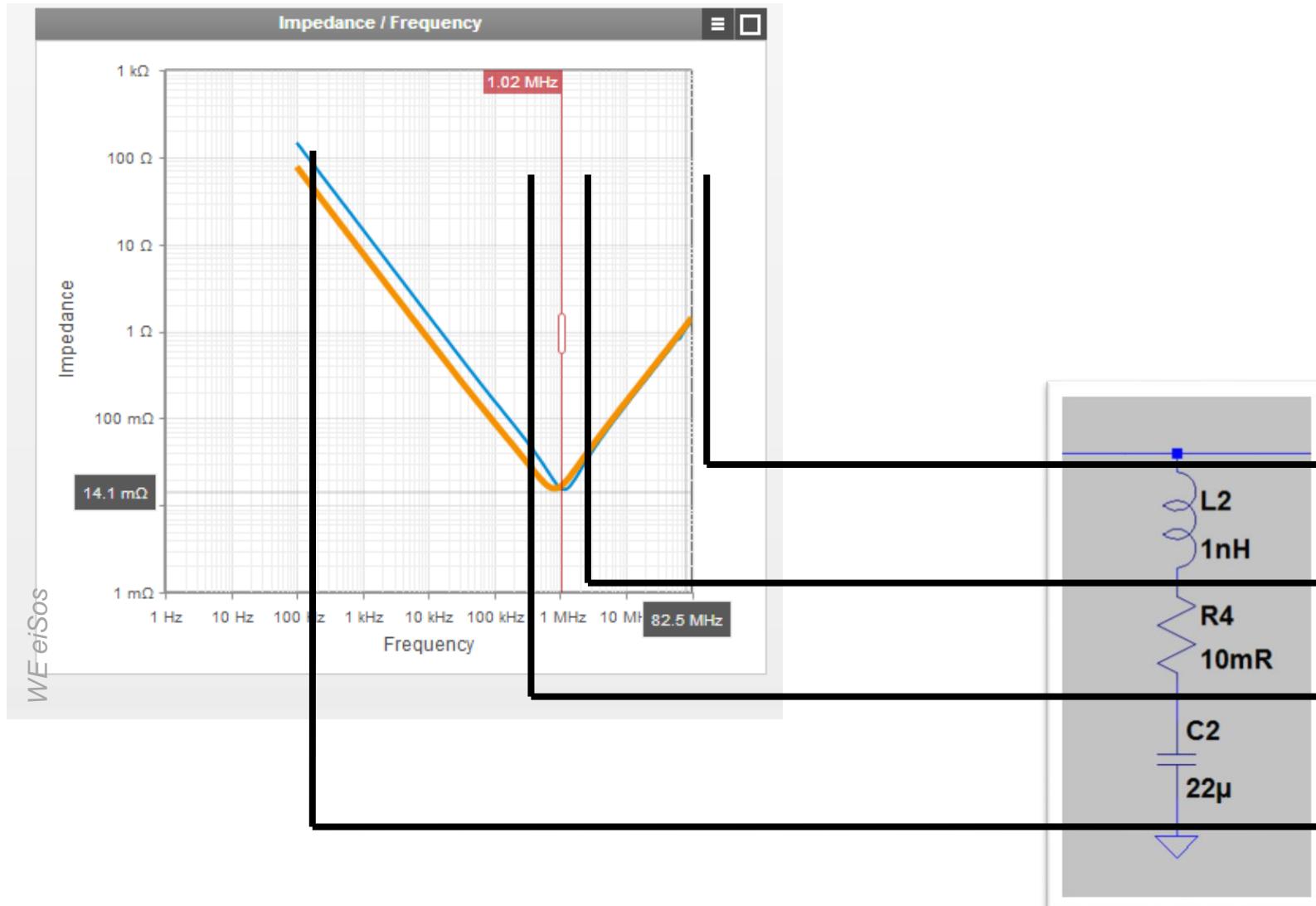
ITEMS

LE BRAS



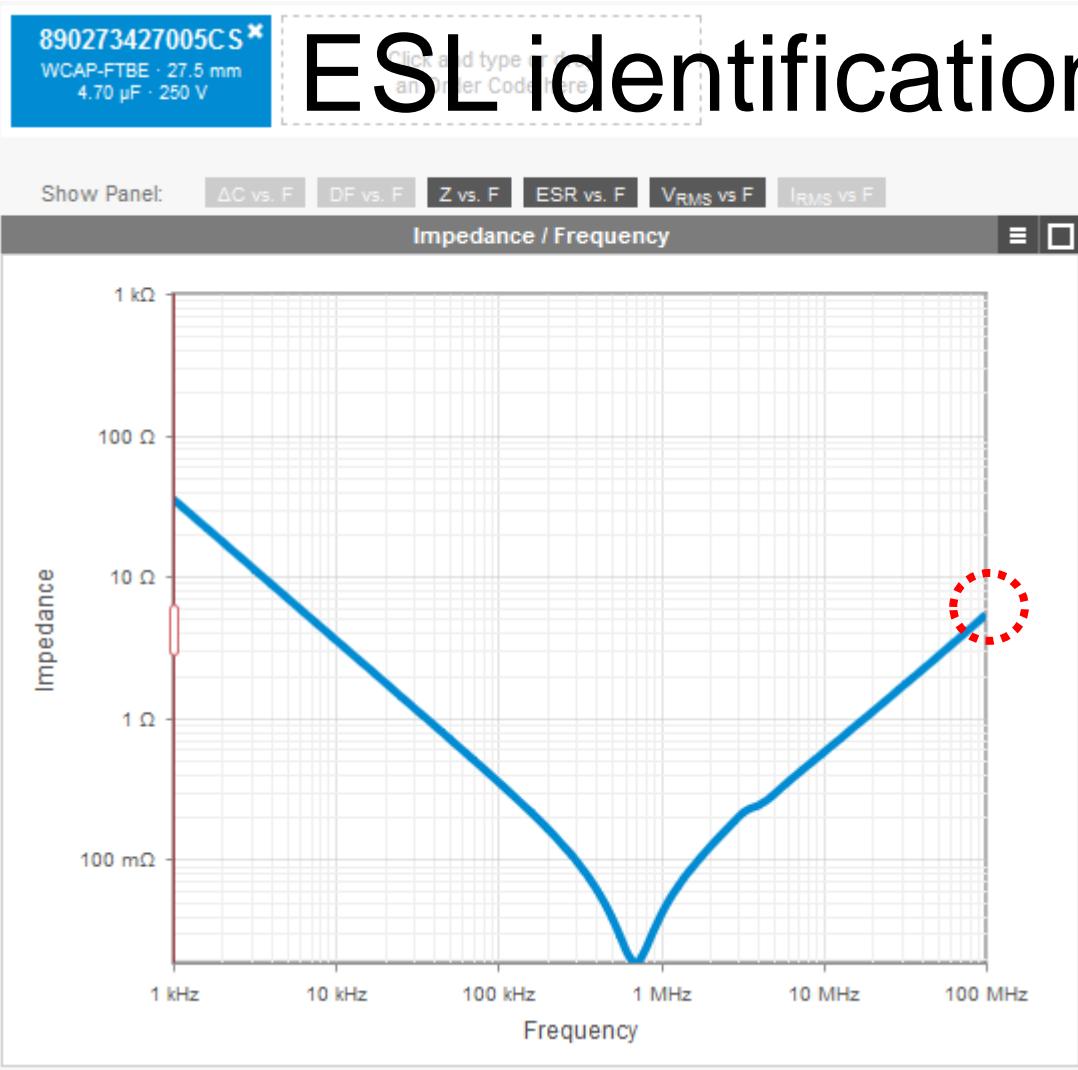
Output ripple of a Buck

Extracting EMC accurate data from REDEXPERT



Output ripple of a Buck

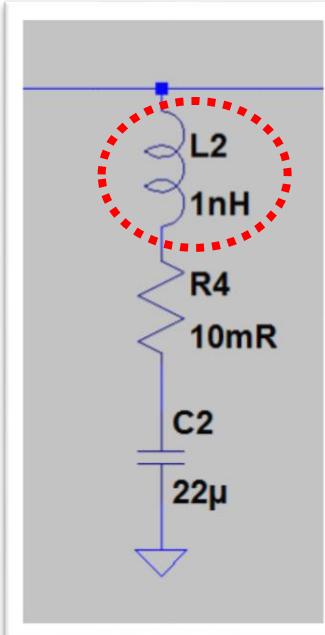
Extracting EMC accurate data from REDEXPERT



$$|Z_L| = L\omega$$

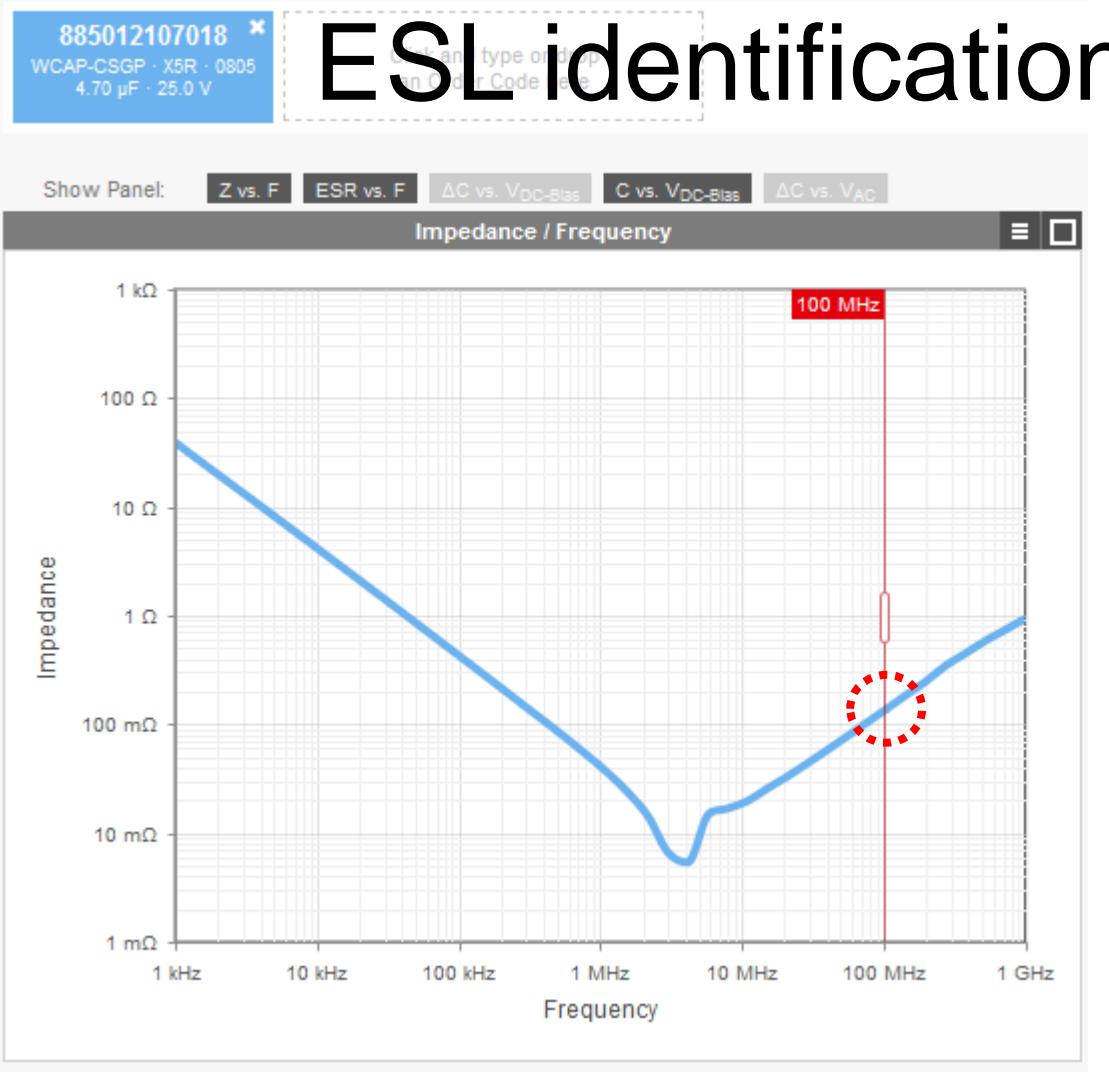
$$\frac{Z_L}{\omega} = L$$

$$L = \frac{|Z_L|}{2\pi F} = \frac{5}{100 \times 10^6 \times 2\pi} \cong 8 \text{ nH}$$



Output ripple of a Buck

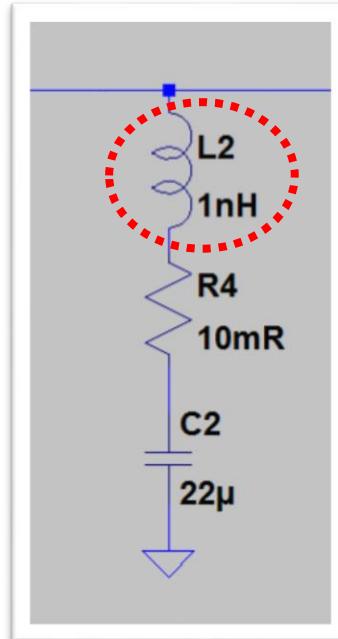
Extracting EMC accurate data from REDEXPERT



$$|Z_L| = L\omega$$

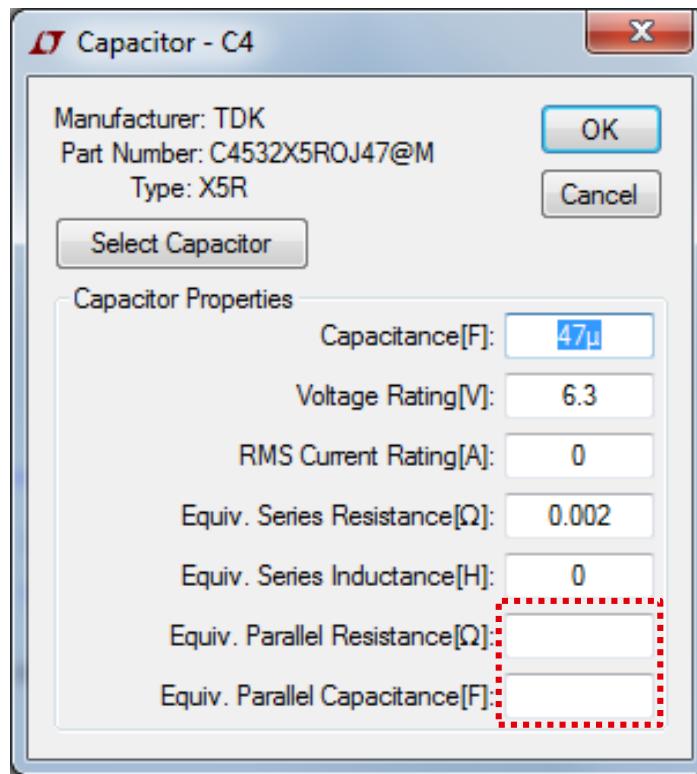
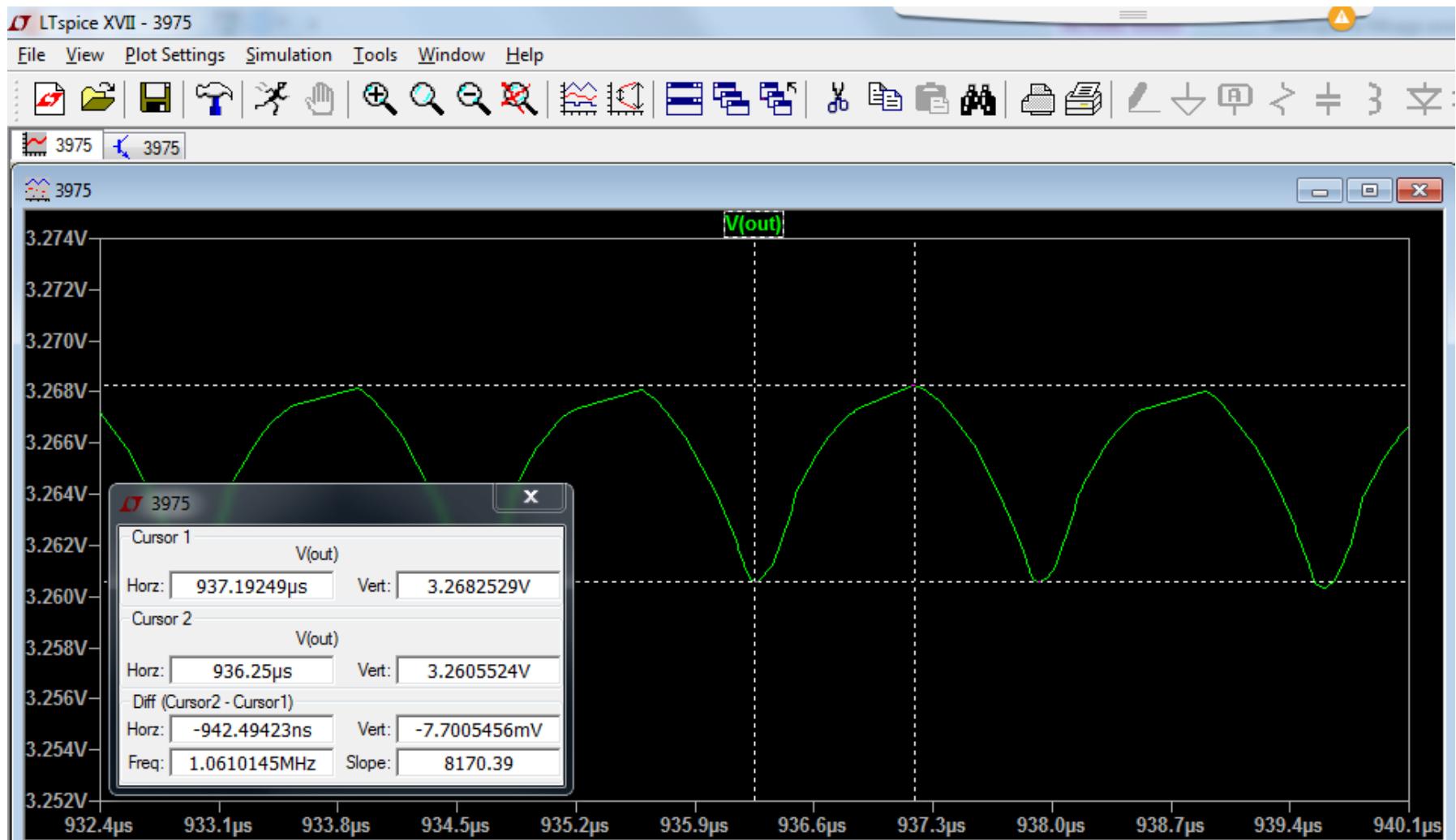
$$\frac{Z_L}{\omega} = L$$

$$L = \frac{|Z_L|}{2\pi F} = \frac{0,132}{100 \times 10^6 \times 2\pi} \cong 0.2 \text{ nH}$$



Output ripple of a Buck

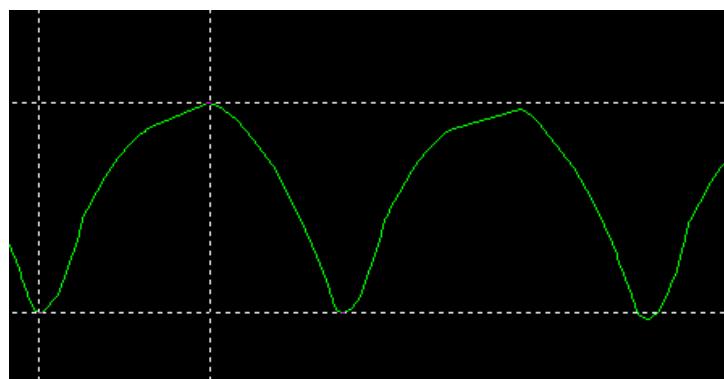
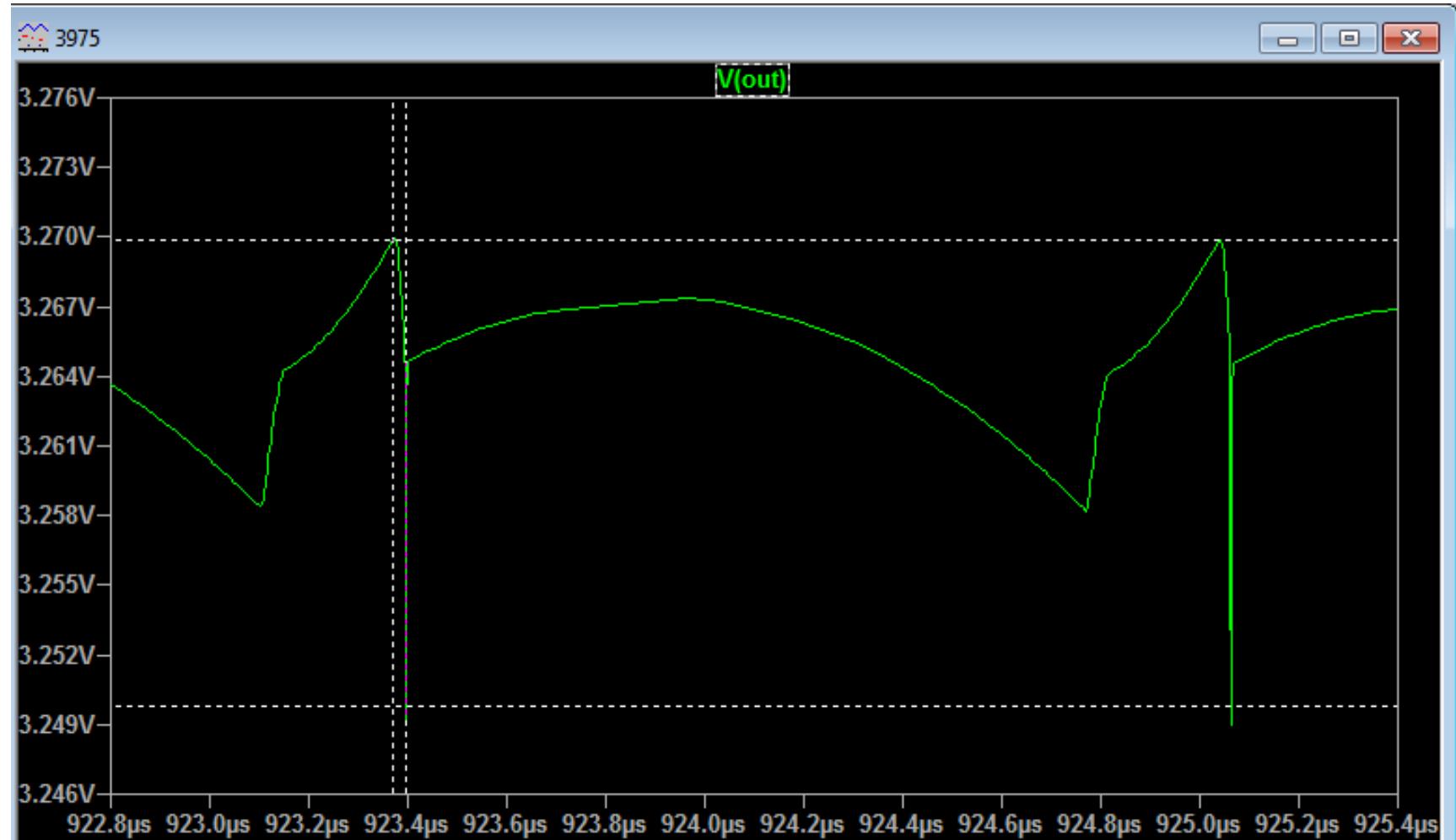
Example of (non) EMC accurate impact on simulation



- ESR = 2 mOhms
- ESL = 0 nH
- DC bias
(DC ? Like don't care ?)

Output ripple of a Buck

Example of (non) EMC accurate impact on simulation



Output ripple of a Buck

Example of EMC accurate simulation

Charge and discharge of cap



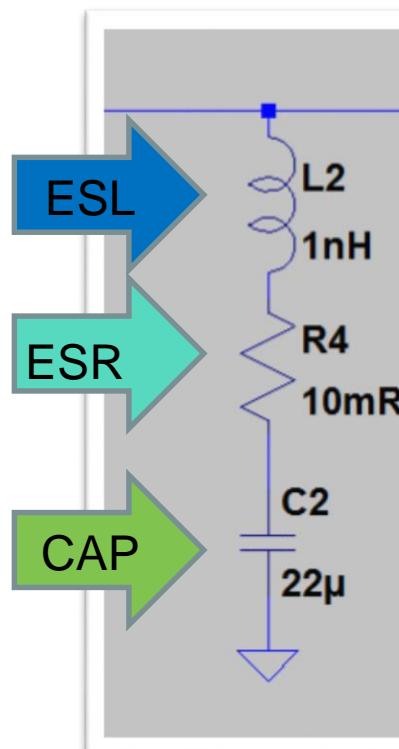
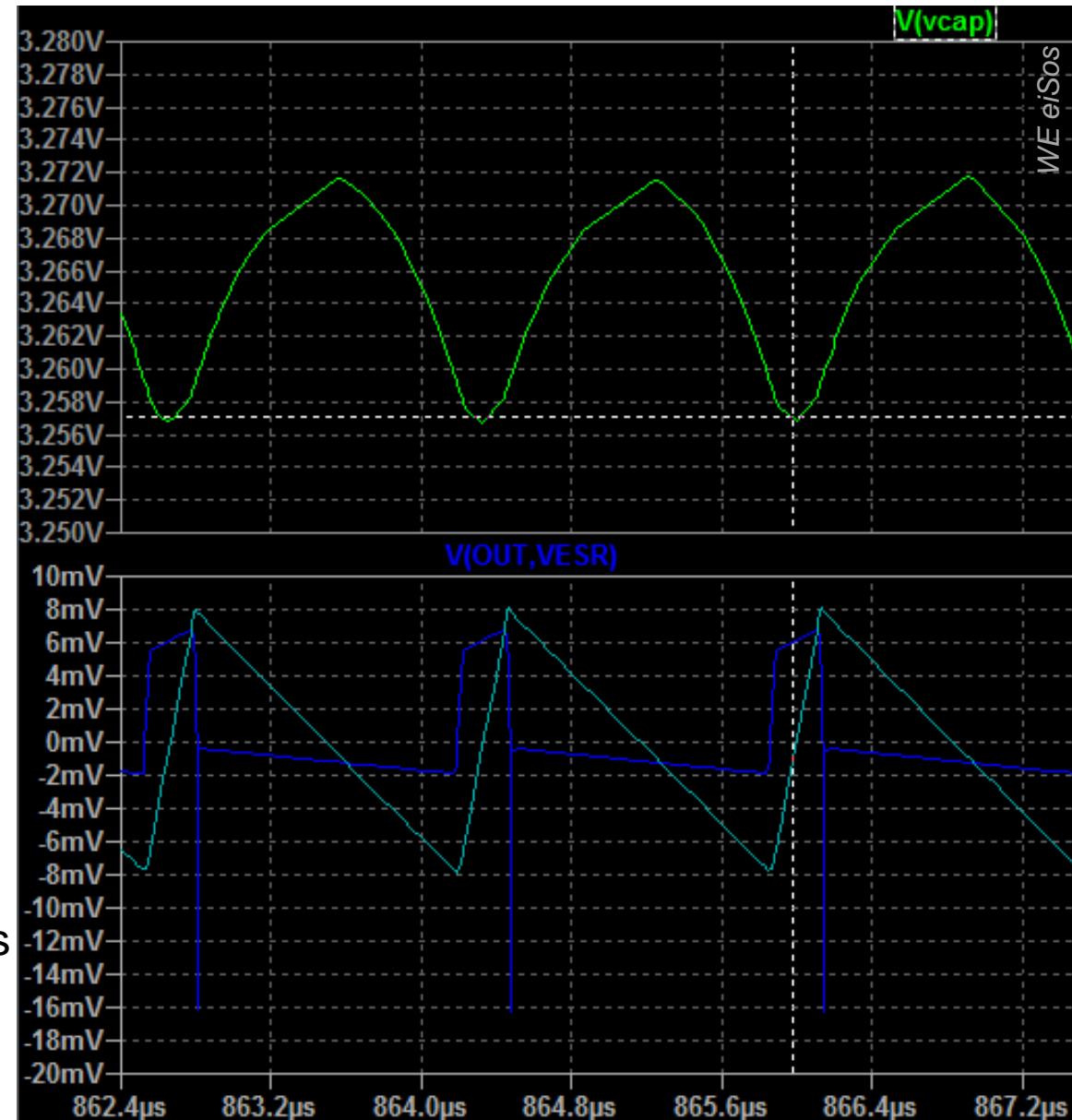
14 mV_{p-p}



16 mV_{p-p}

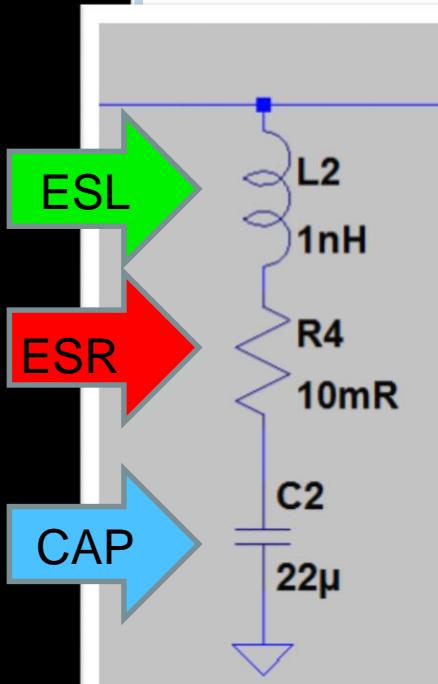
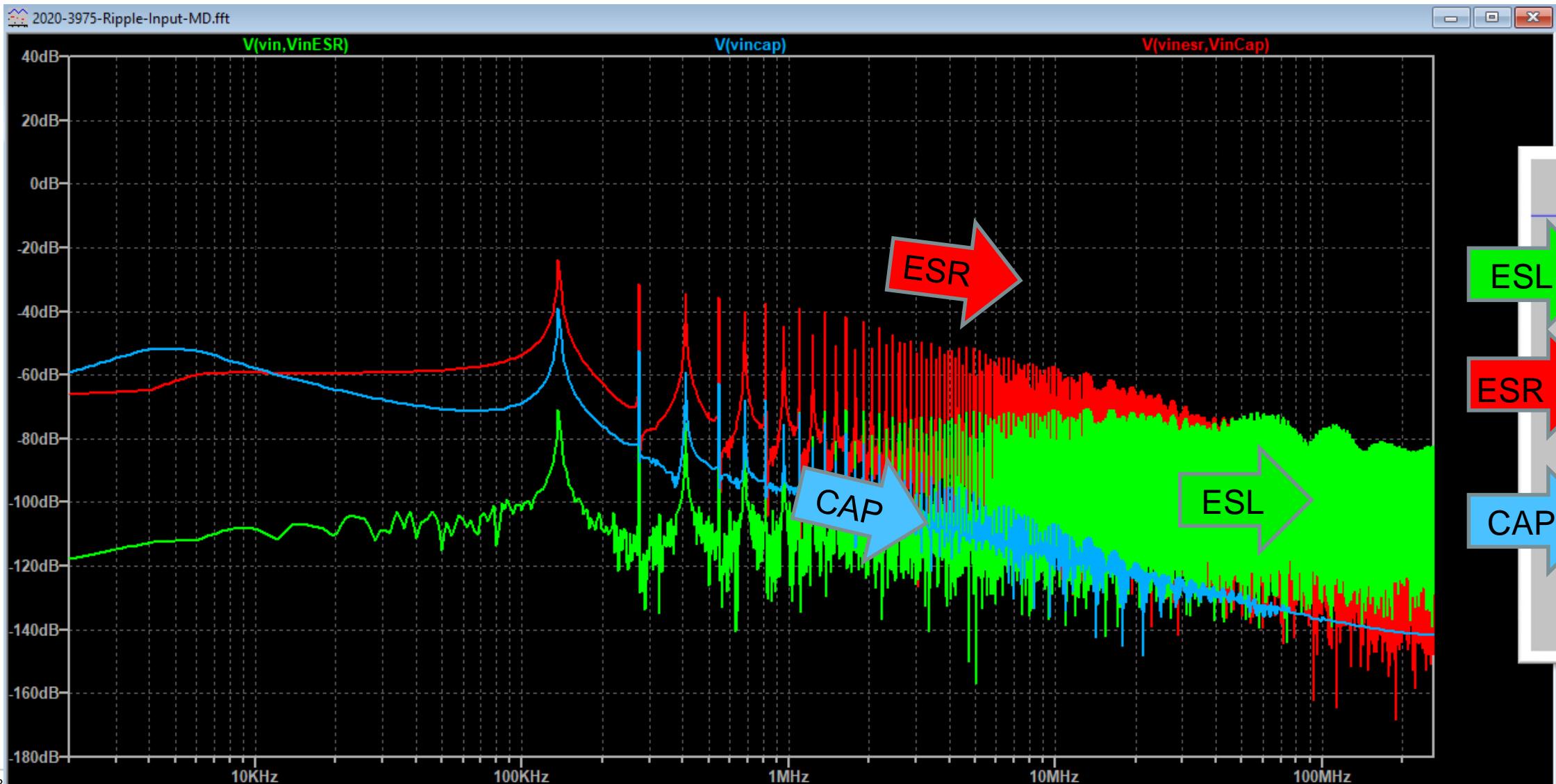


10 mV_{p-p} at low frequencies
 25 mV_{p-p} at high frequencies



Capacitor ripple voltage example

ESR / ESL / CAP breakdown in frequency

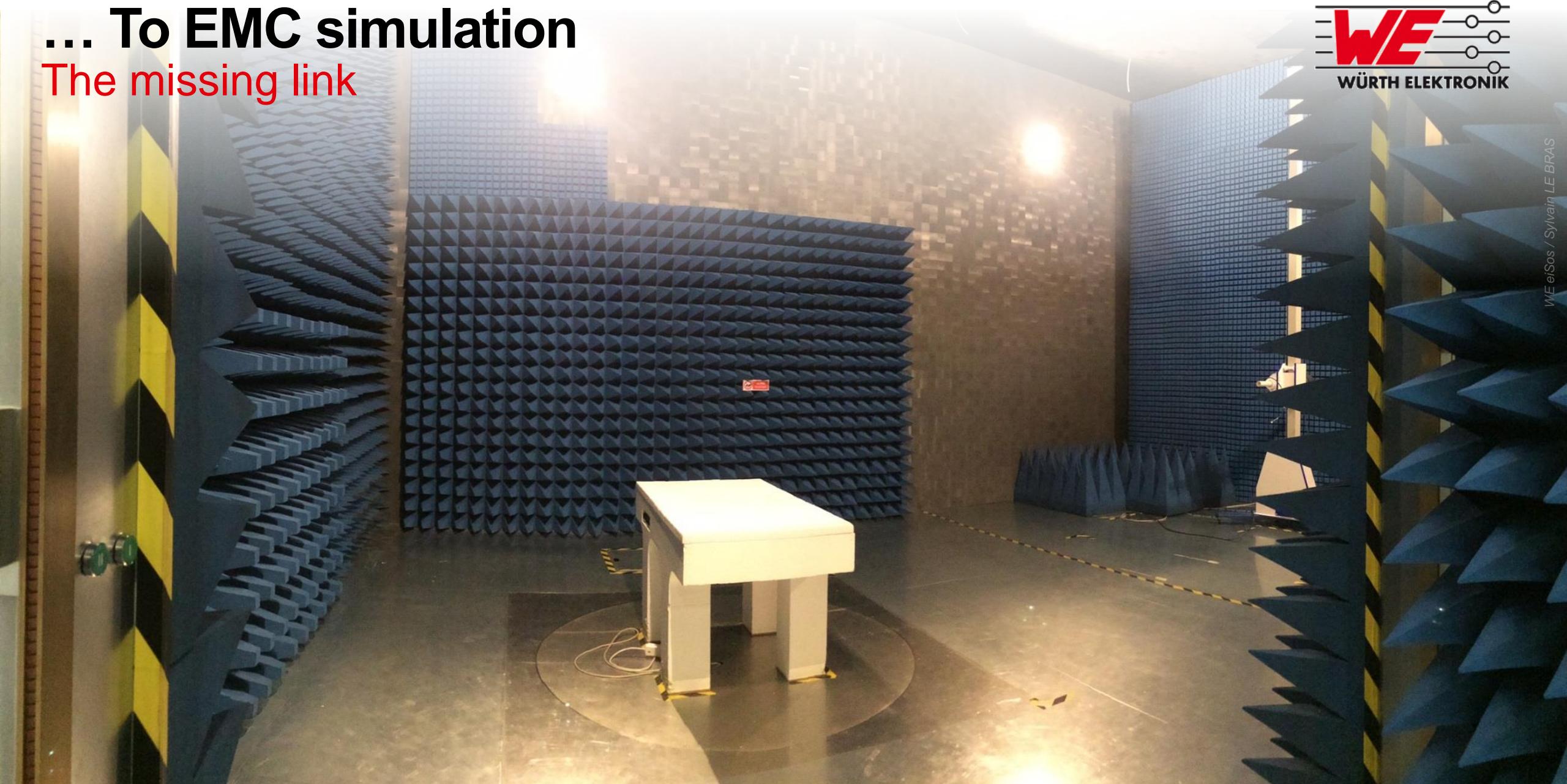


... To EMC simulation

The missing link

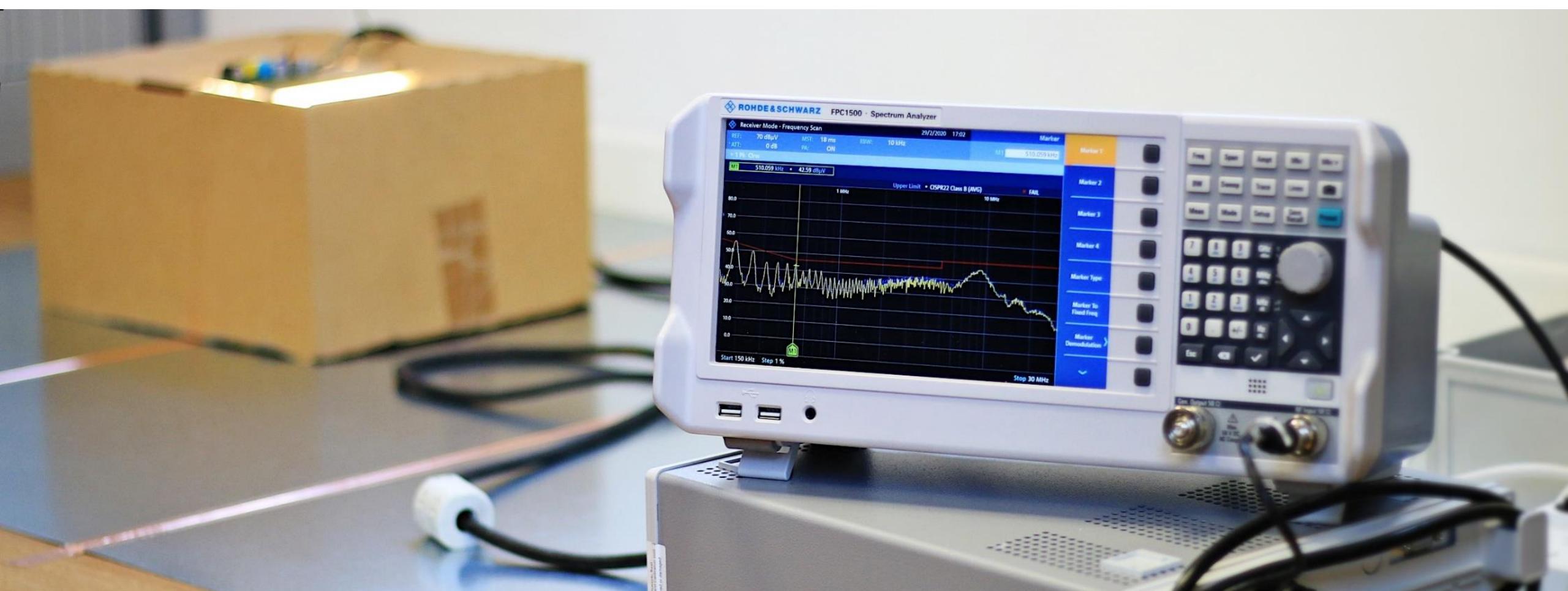


WE eiSos / Sylvain LE BRAS



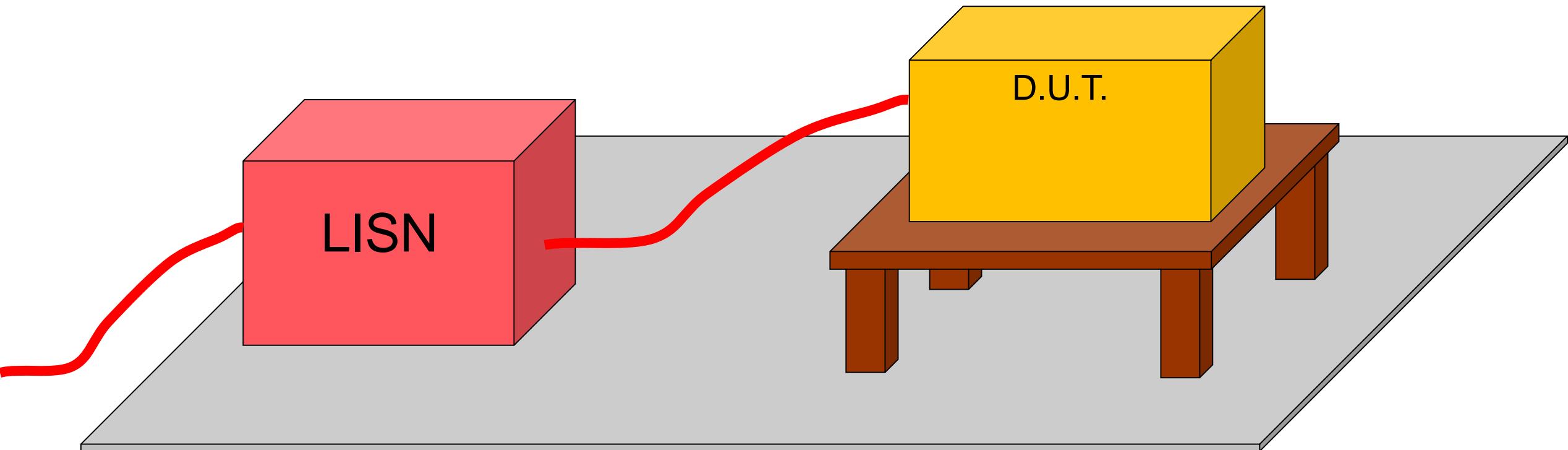
Enabling EMC accurate measurement in LTSpice

What is the keystone of conducted emissions ?



Enabling EMC accurate measurement in LTSpice

What is the keystone of conducted emissions ?

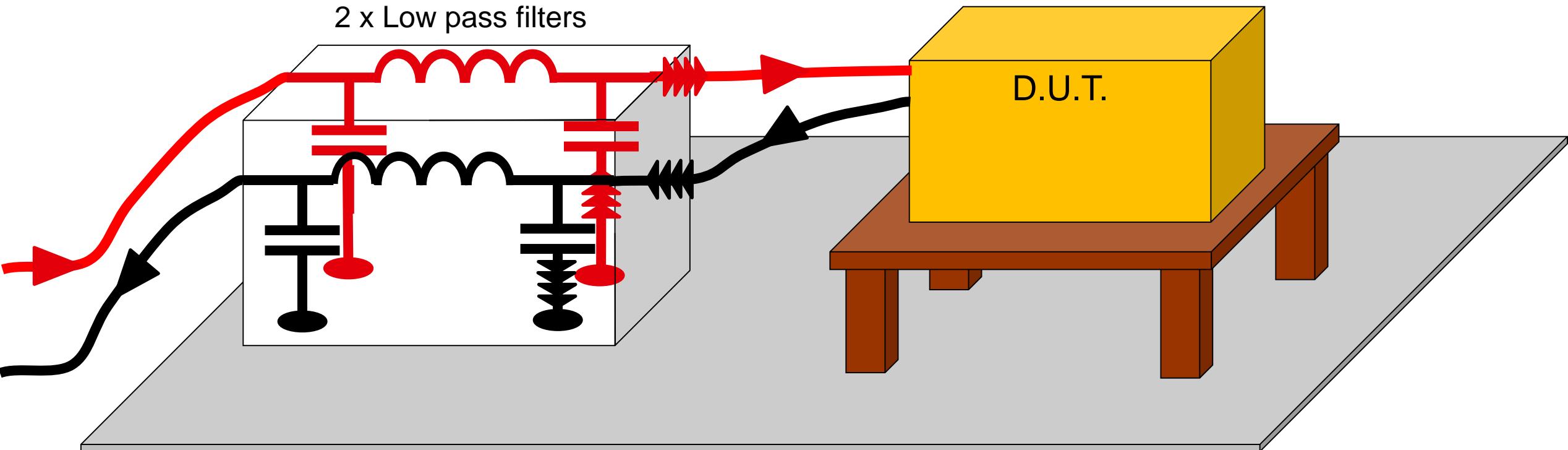


Enabling EMC accurate measurement in LTSpice

What is the keystone of conducted emissions ?



- ▶ Low Frequency
- ▶ High Frequency

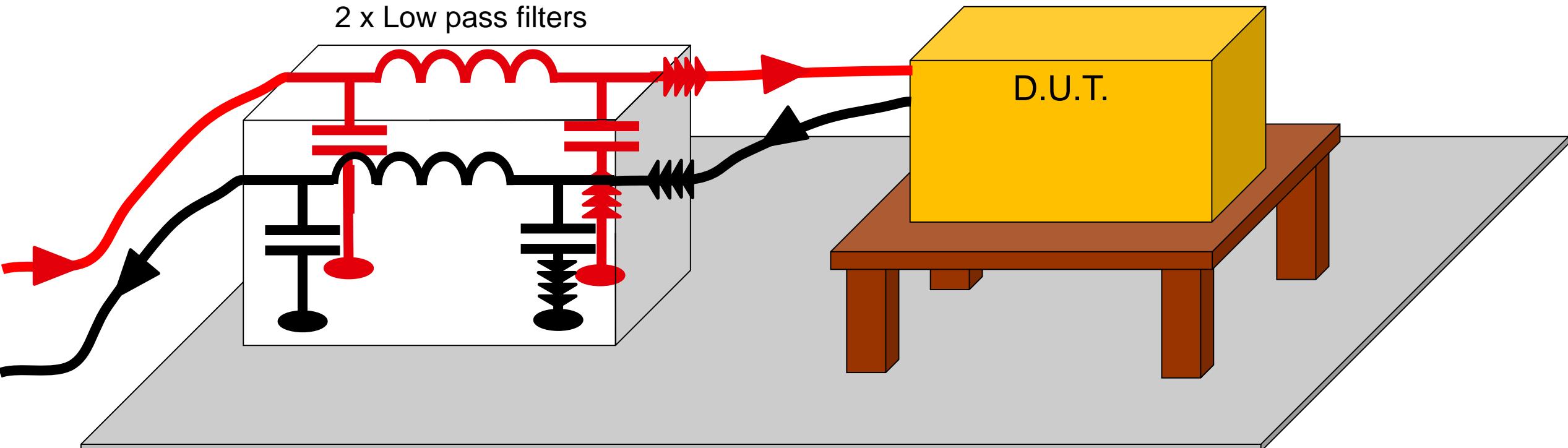


Enabling EMC accurate measurement in LTSpice

What is the keystone of conducted emissions ?

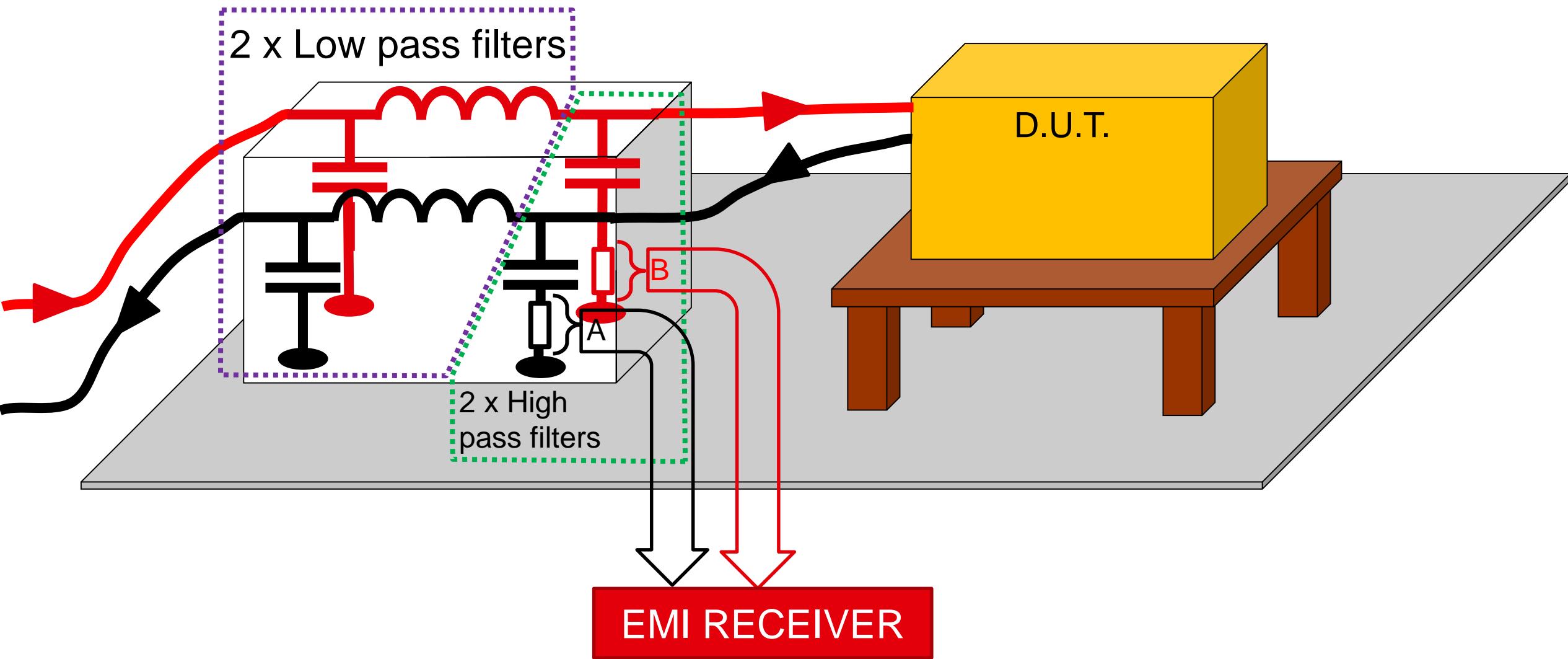


- ▶ Low Frequency
- ▶ High Frequency



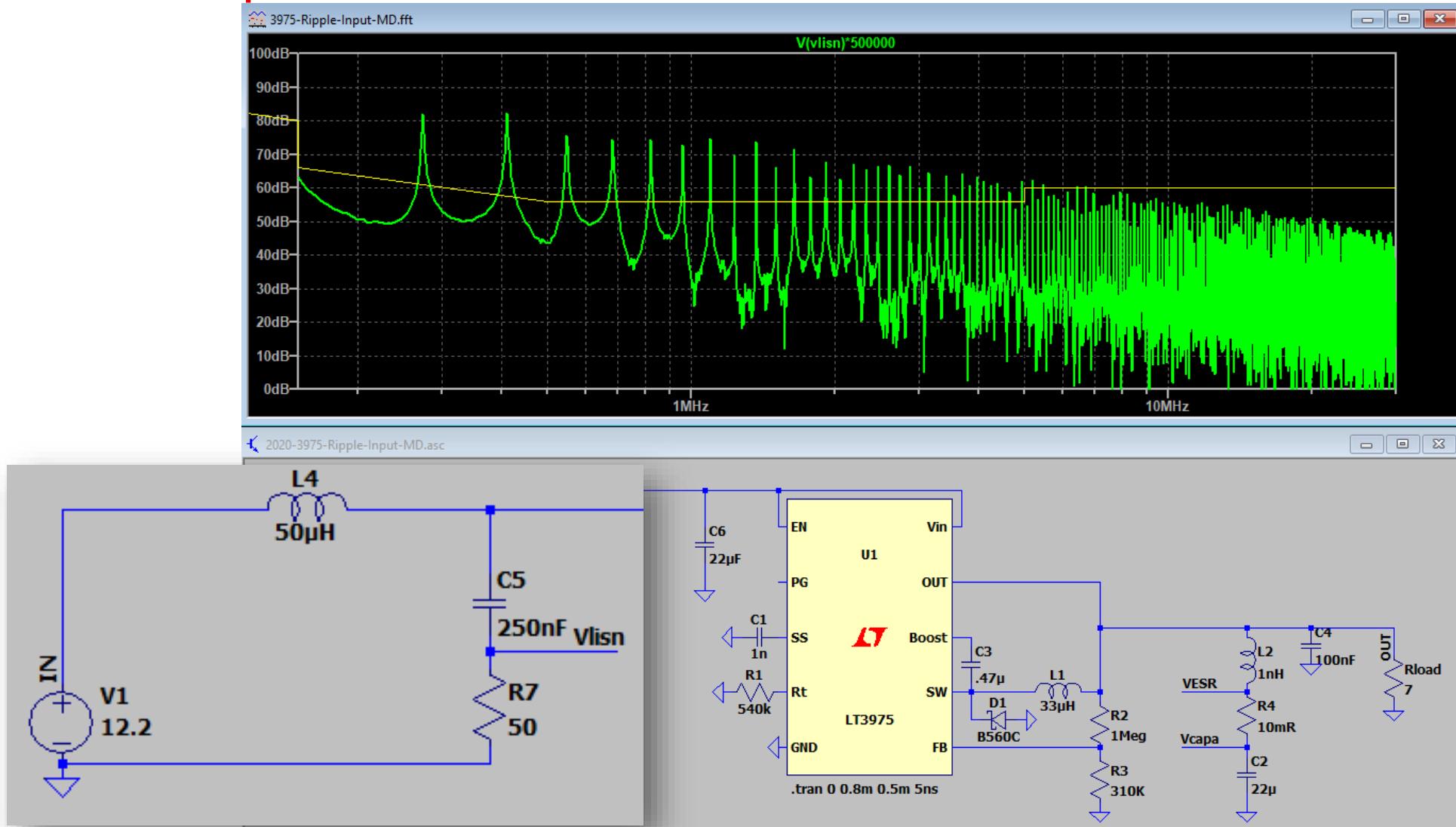
Enabling EMC accurate measurement in LTSpice

What is the keystone of conducted emissions ?



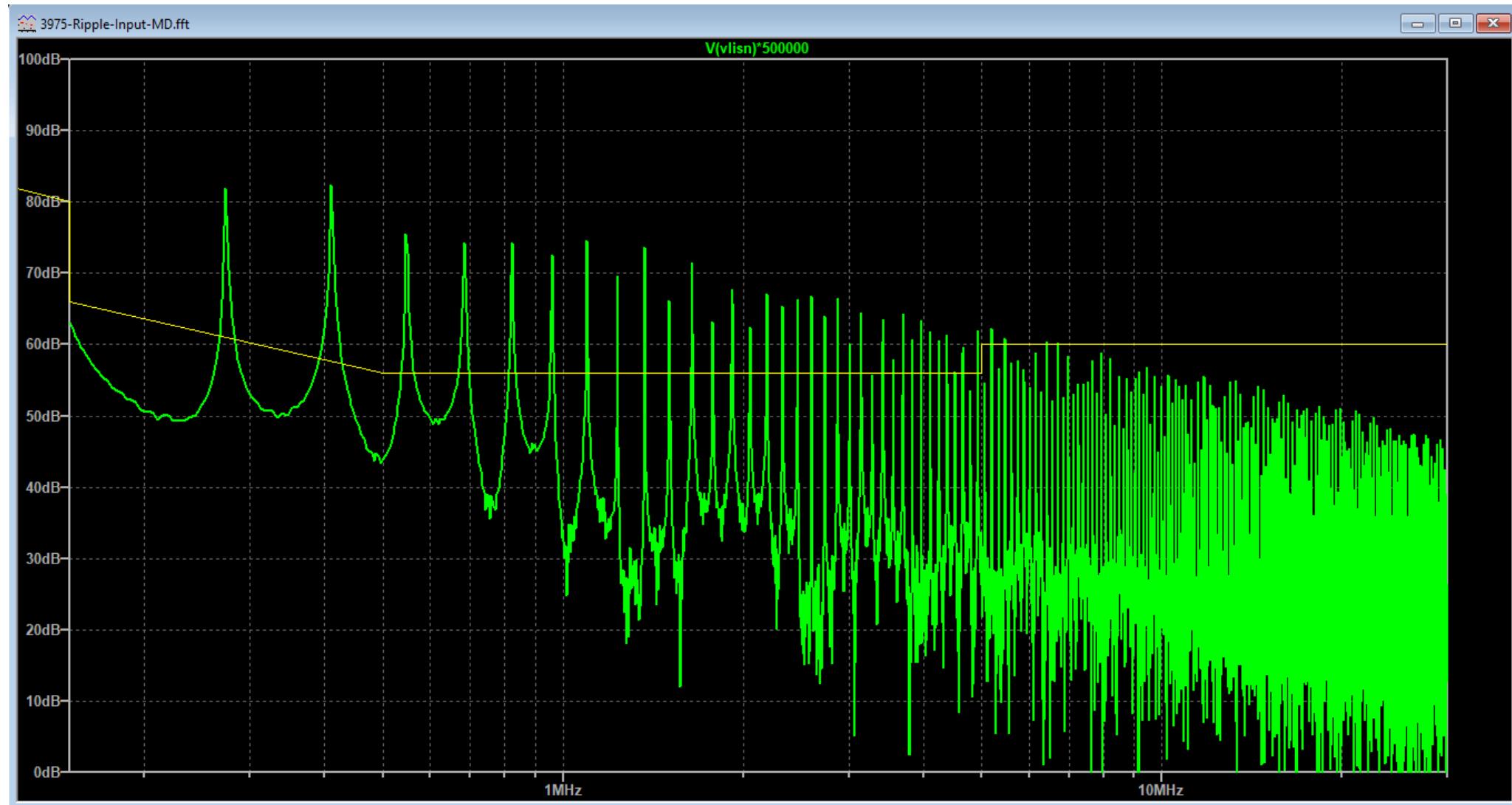
Enabling EMC accurate measurement in LTSpice

FFT with simplified LISN



Reality VS Simulation

FFT with simplified LISN



Reality VS Simulation

Conducted Emissions measurement



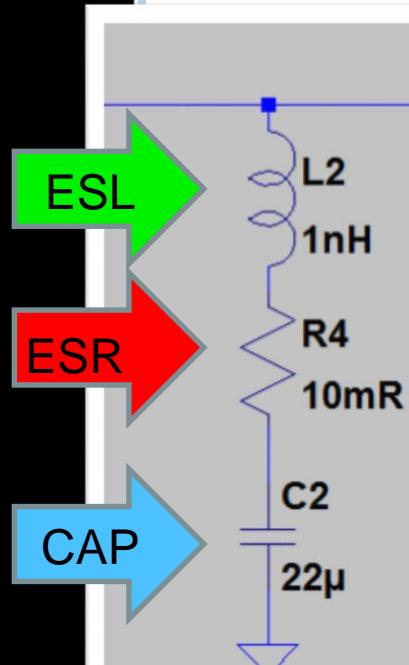
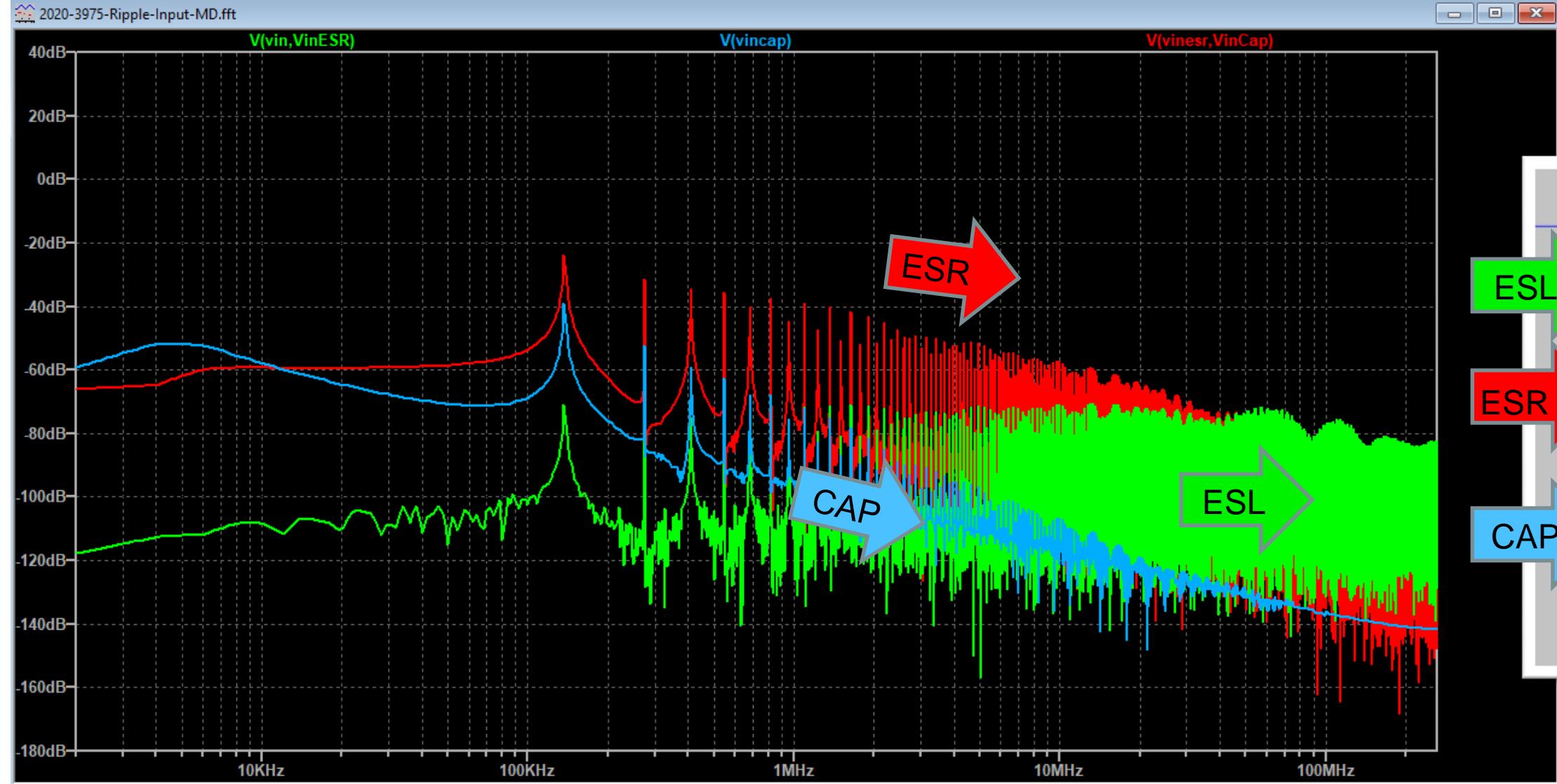
Reality VS Simulation

Conducted Emissions measurement



Reality VS Simulation

ESR / ESL / CAP breakdown in frequency



Reality VS Simulation

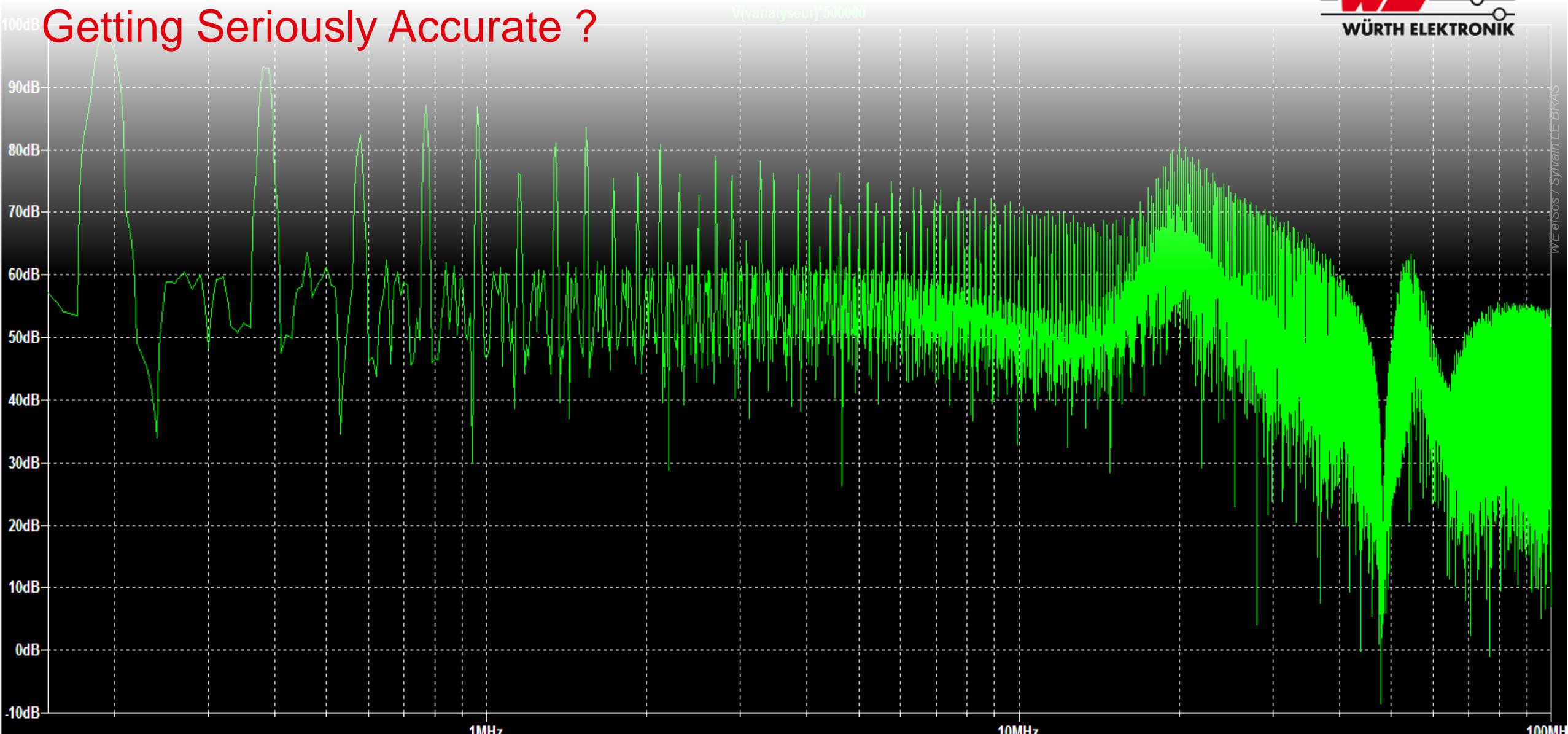


EMI measurement = Σ (Common Mode + Differential Mode)



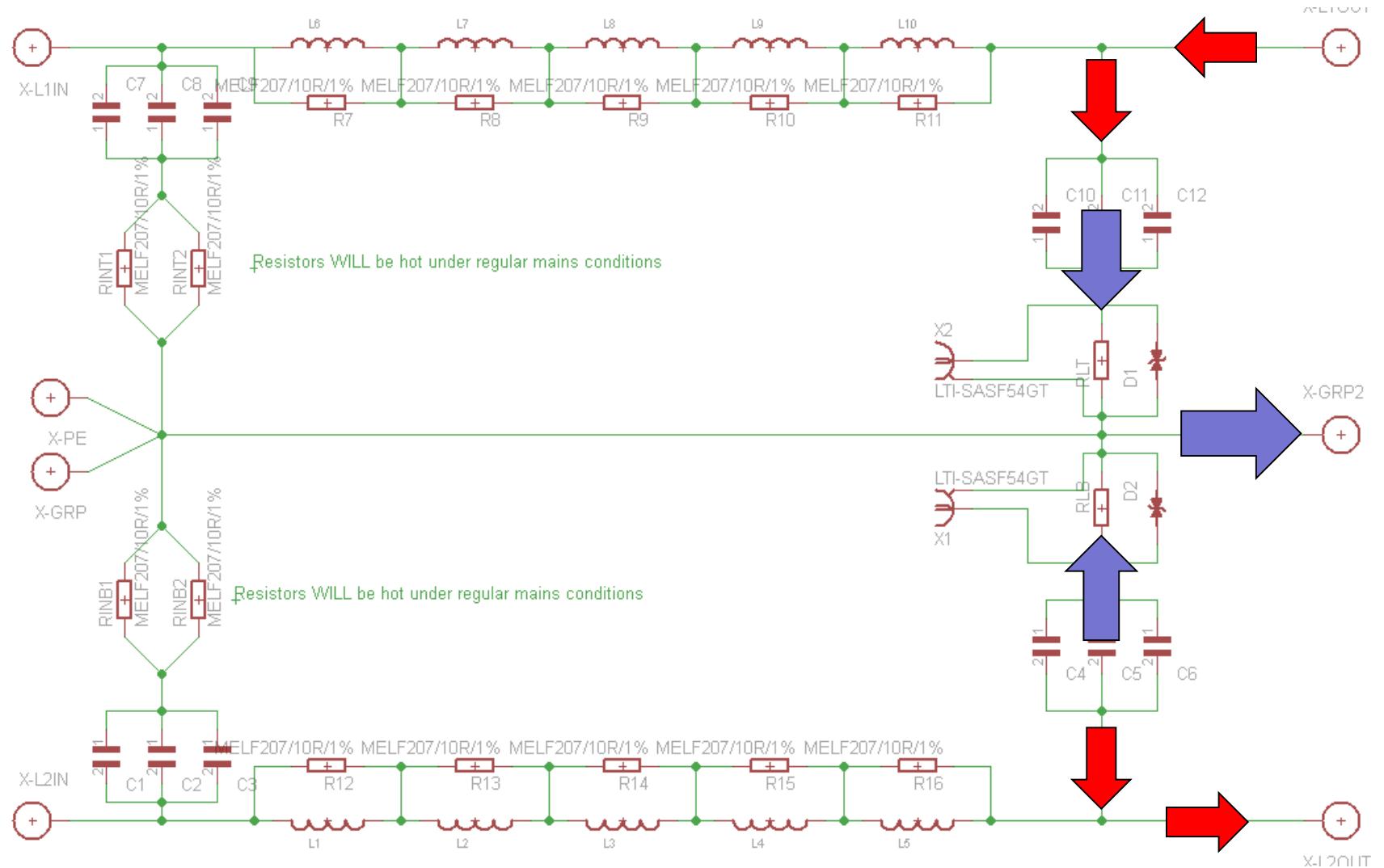
... To EMC simulation

Getting Seriously Accurate ?



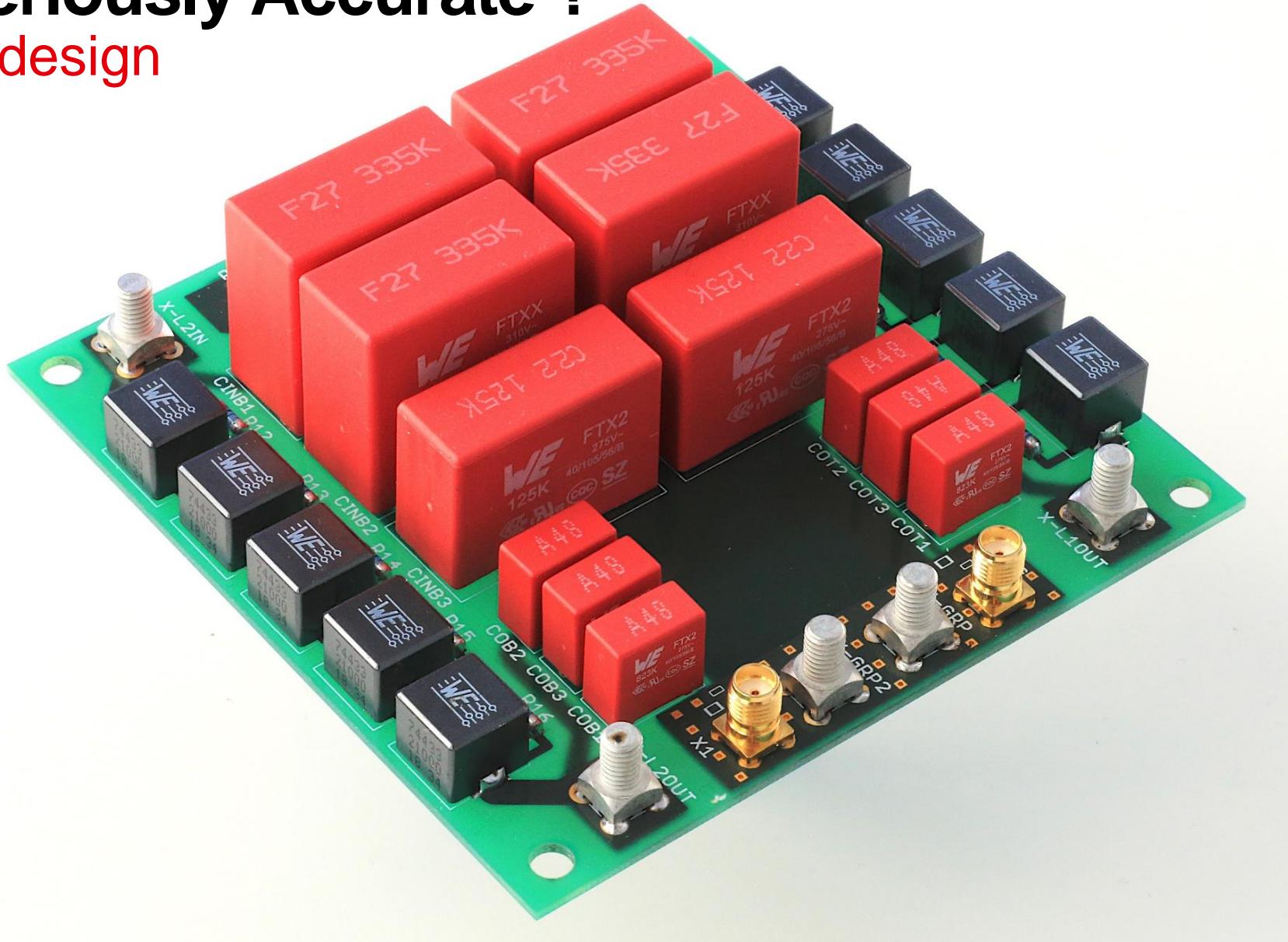
Getting Seriously Accurate ?

Actual LISN design



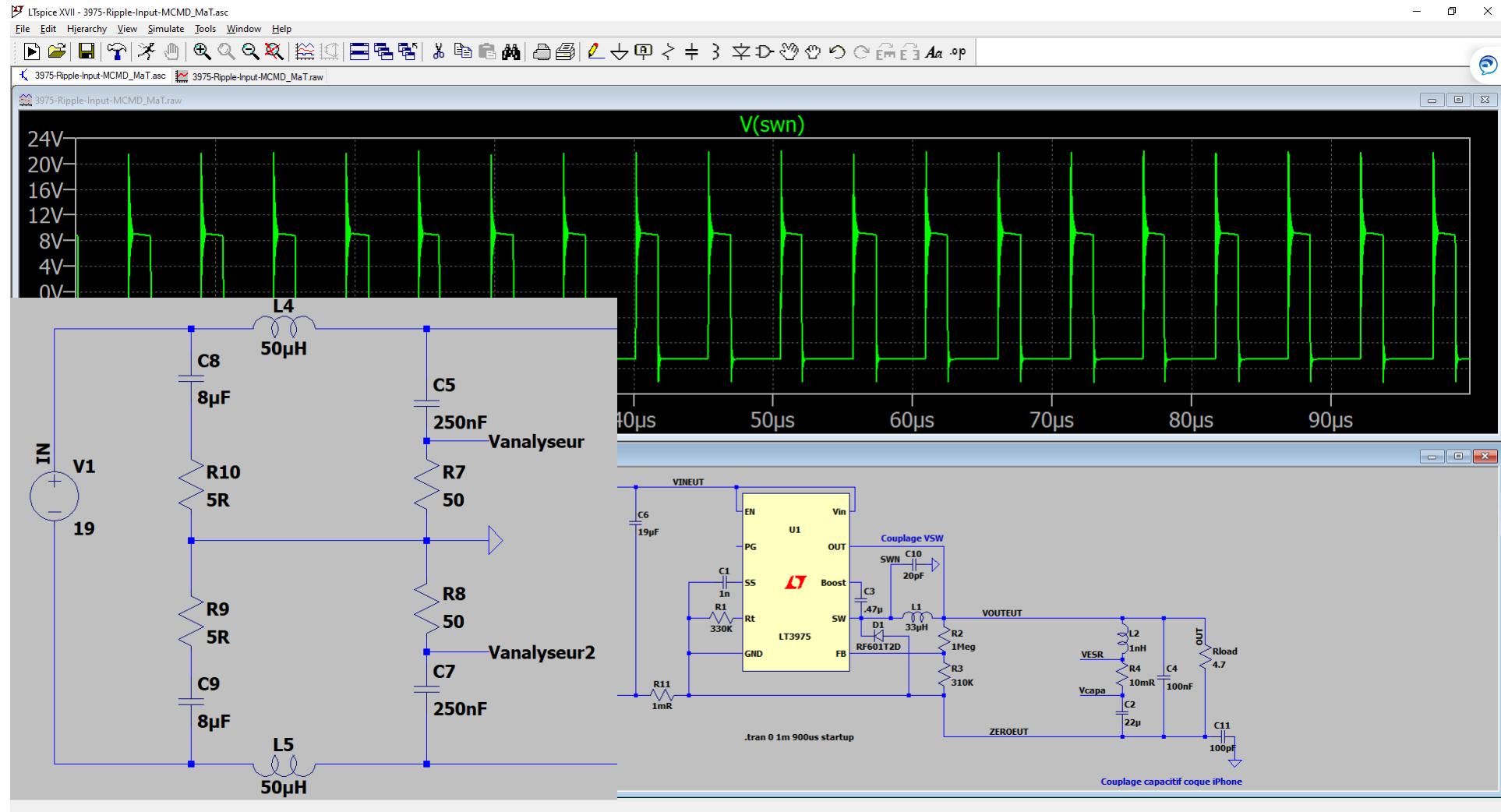
Getting Seriously Accurate ?

Actual LISN design



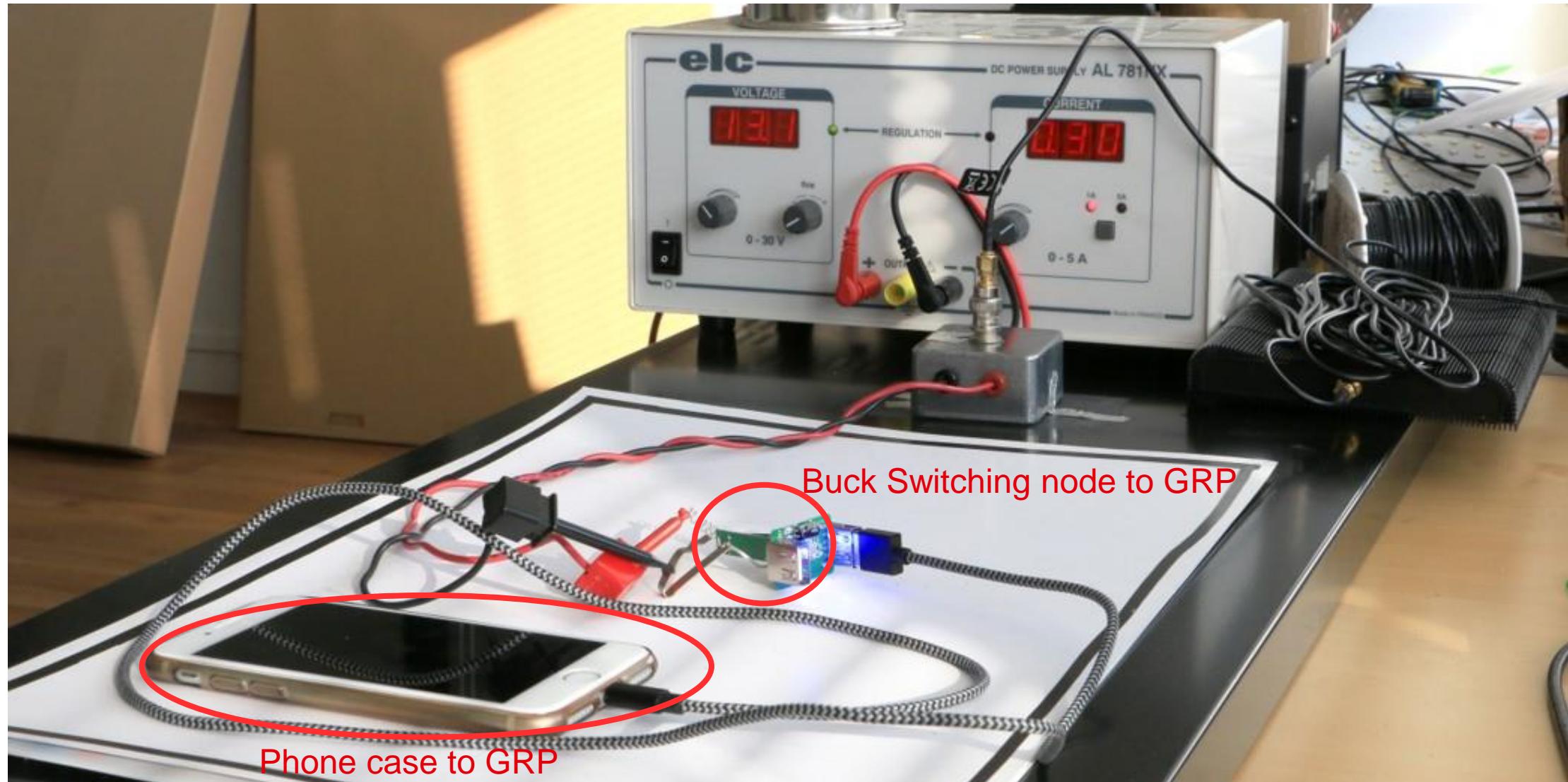
Getting Seriously Accurate ?

Simulation Ready LISN design



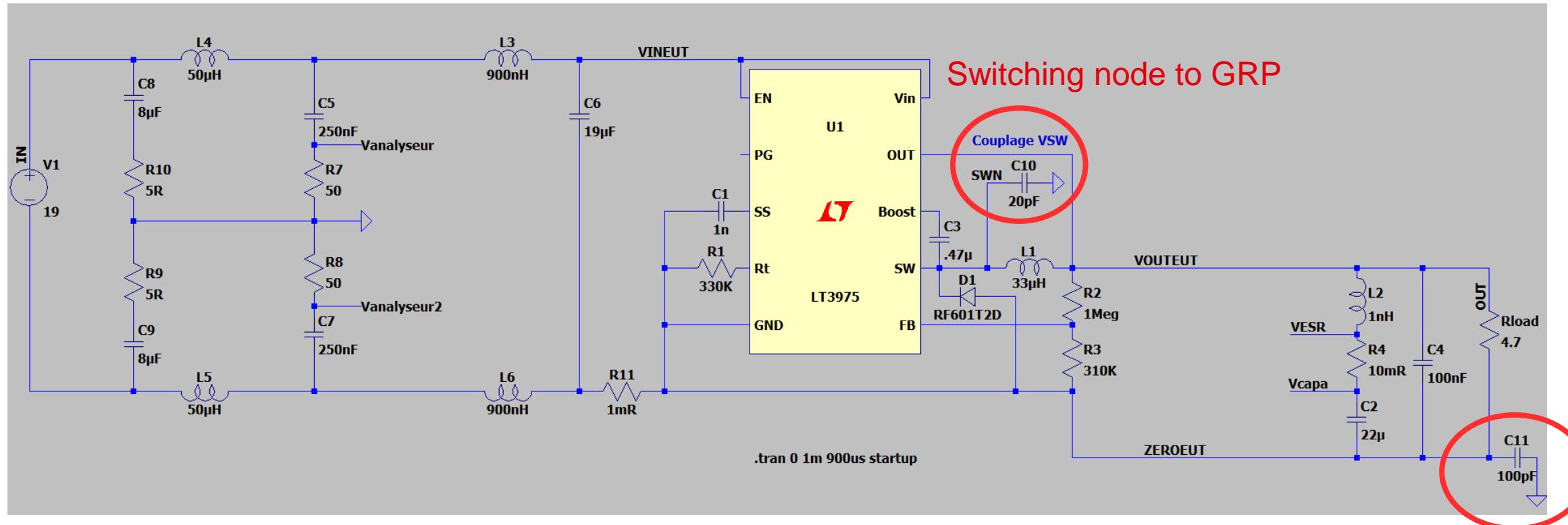
Getting Seriously Accurate ?

Adding E-Field parasitic coupling



Getting Seriously Accurate ?

Adding E-Field parasitic coupling



Phone case to GRP

Getting Seriously Accurate ?

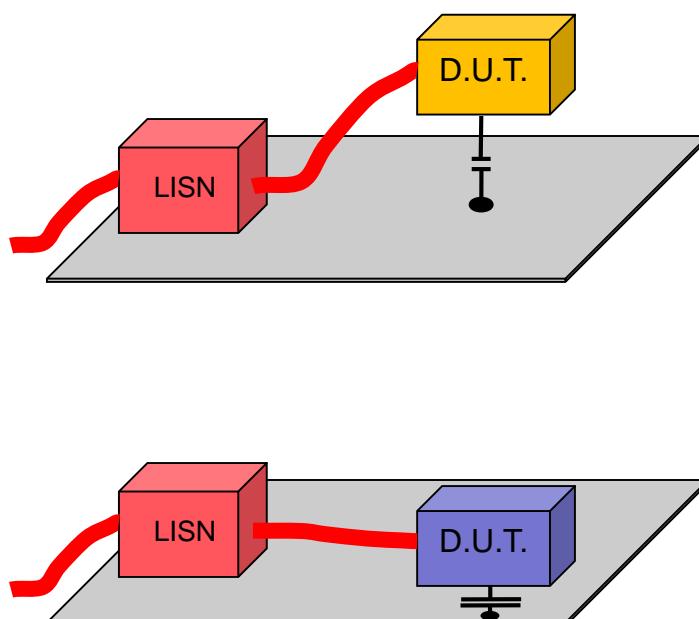
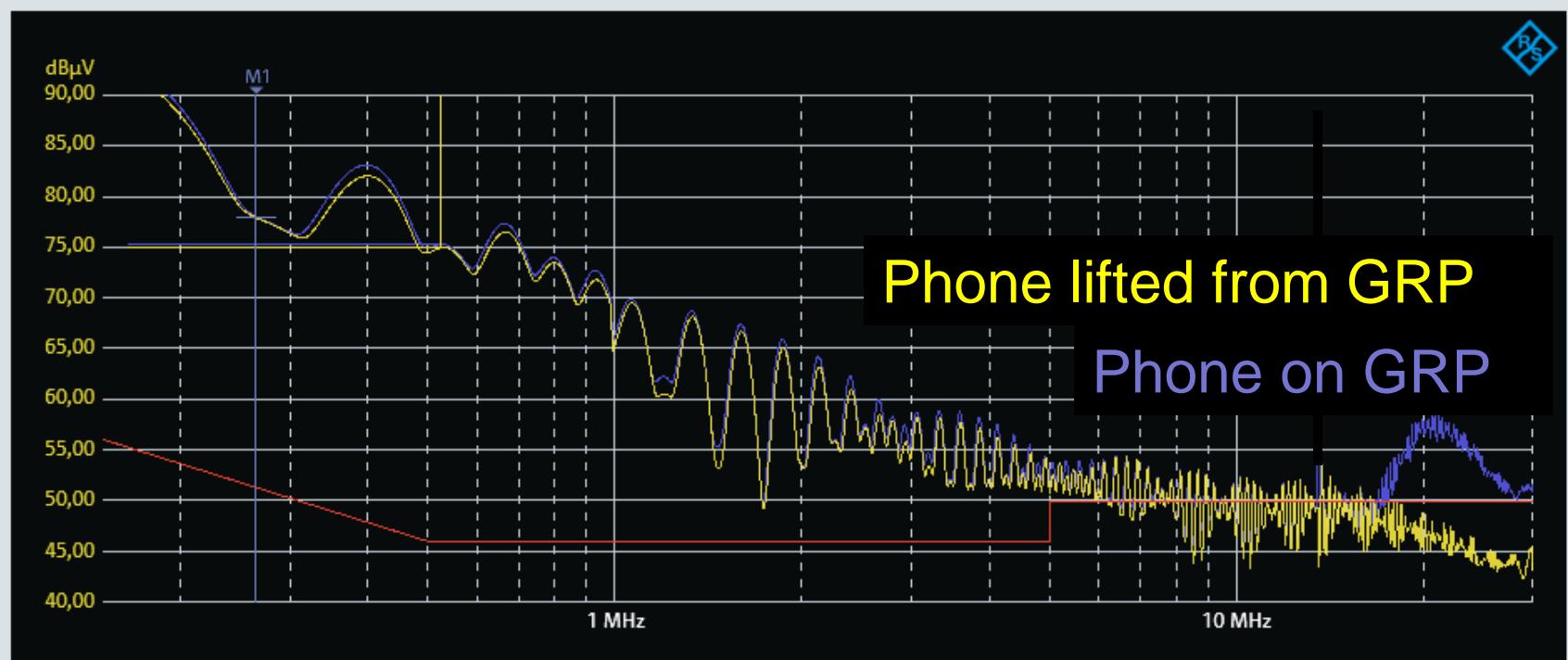
Reality VS Simulation



Frequency Scan

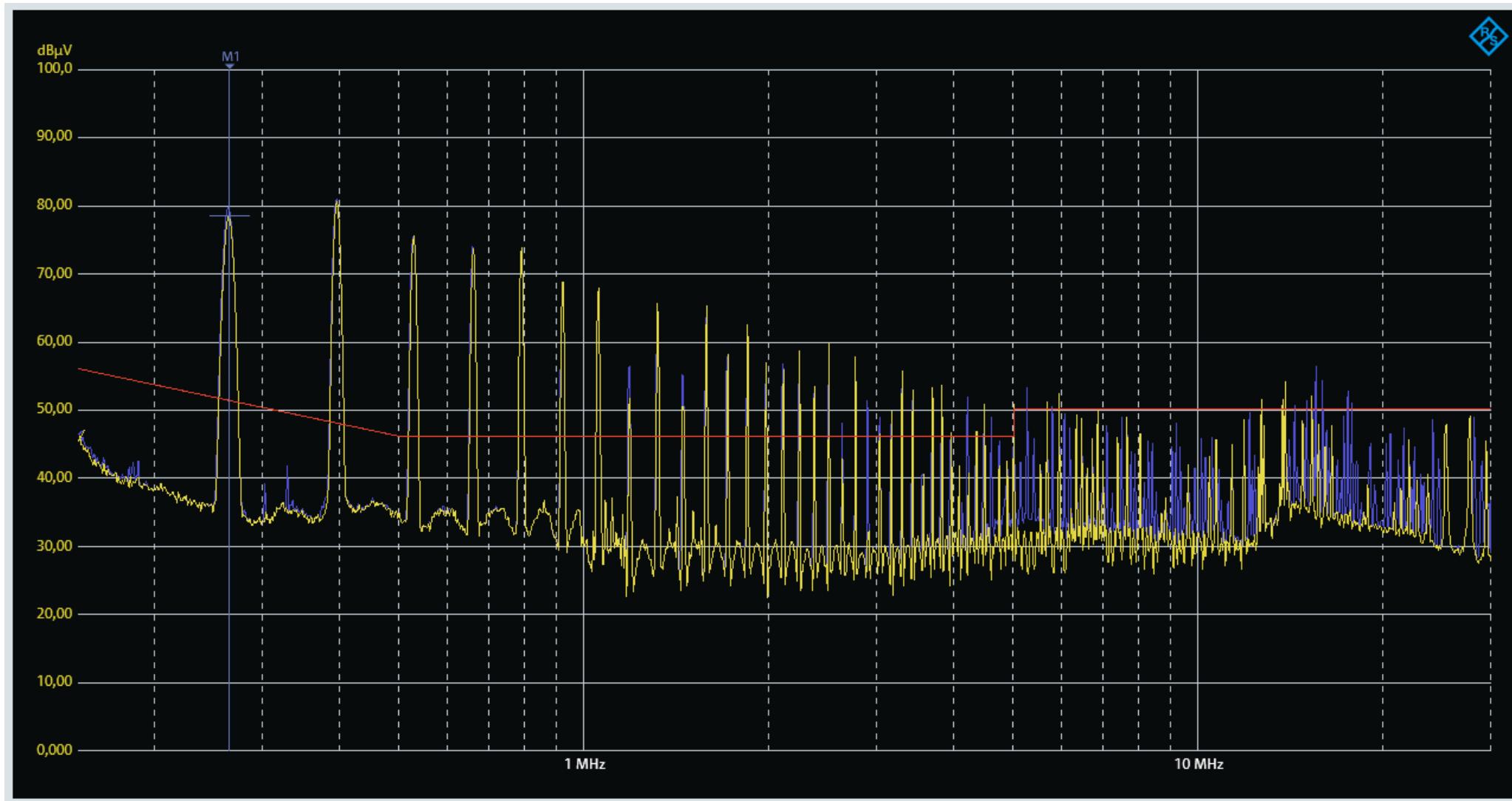
Ref Level 80 dB μ V
 □ RF Attenuator 10 dB
 RBW 100 kHz
 Start Frequency 150 kHz
 Stop Frequency 30 MHz

Measurement Time 10 ms
 Trace Mode Clear / Write
 Trigger Mode Free Run
 Trace Detector Average
 Scan step 0,5 %



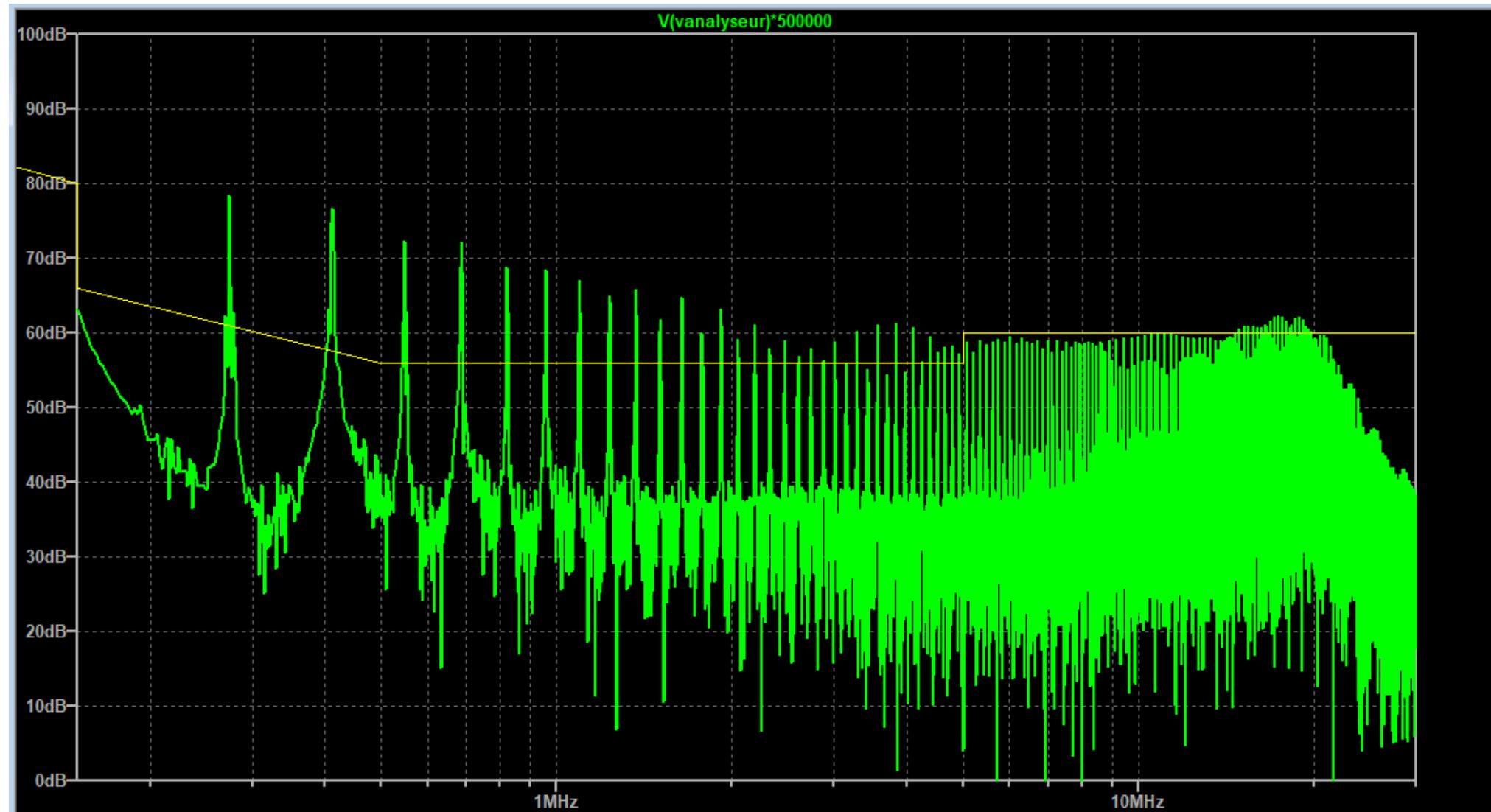
Getting Seriously Accurate ?

Reality VS Simulation



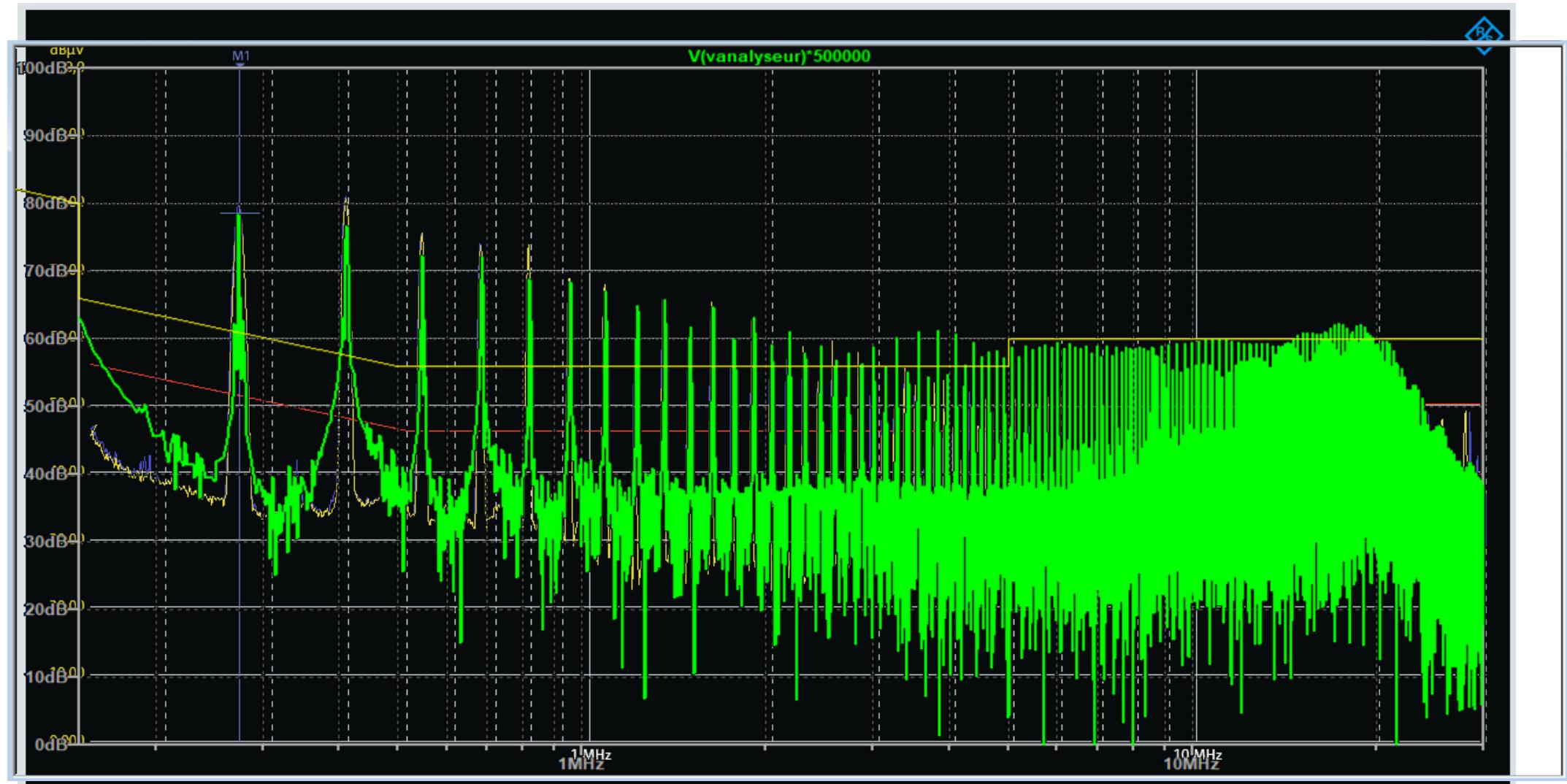
Getting Seriously Accurate ?

Reality VS Simulation



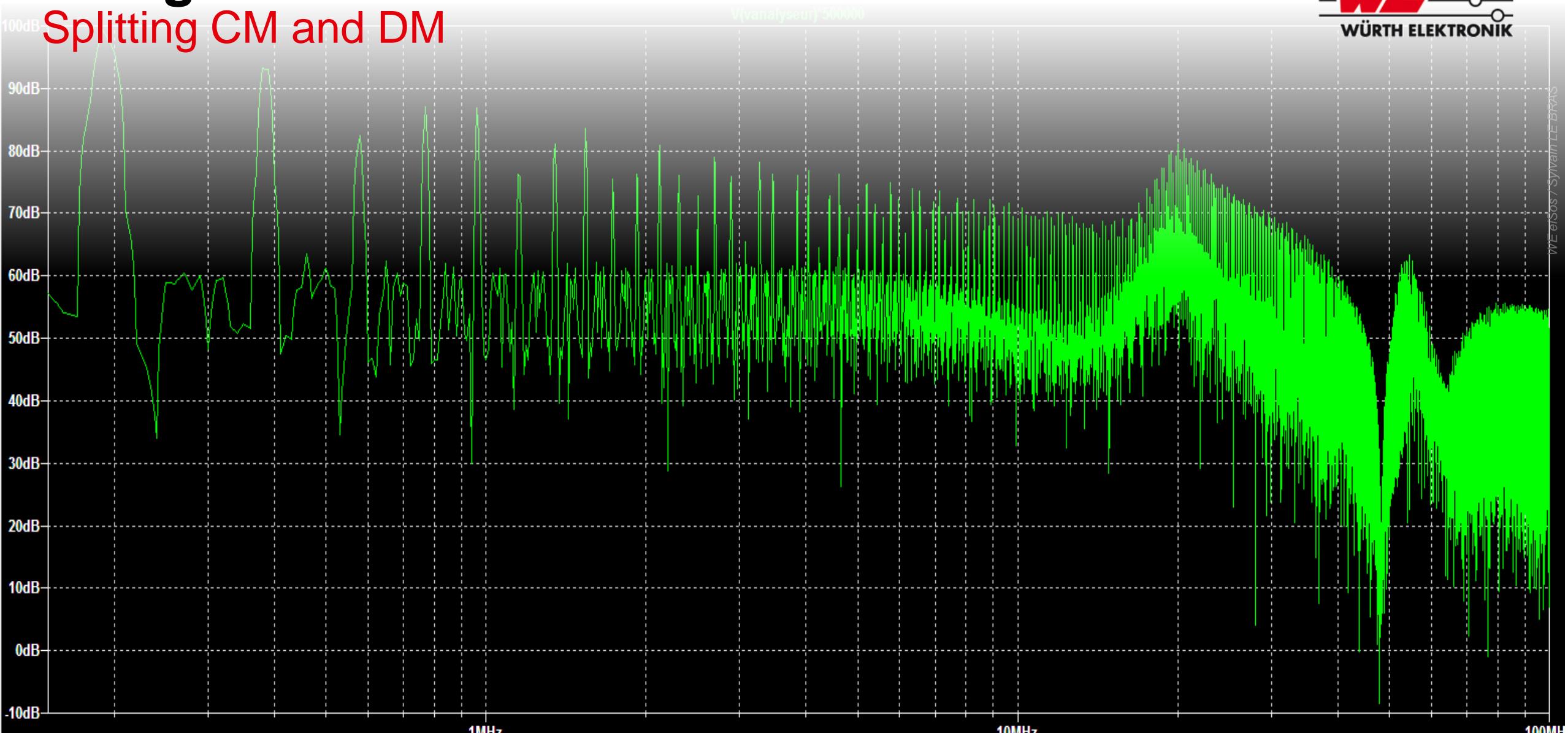
Getting Seriously Accurate ?

Reality VS Simulation



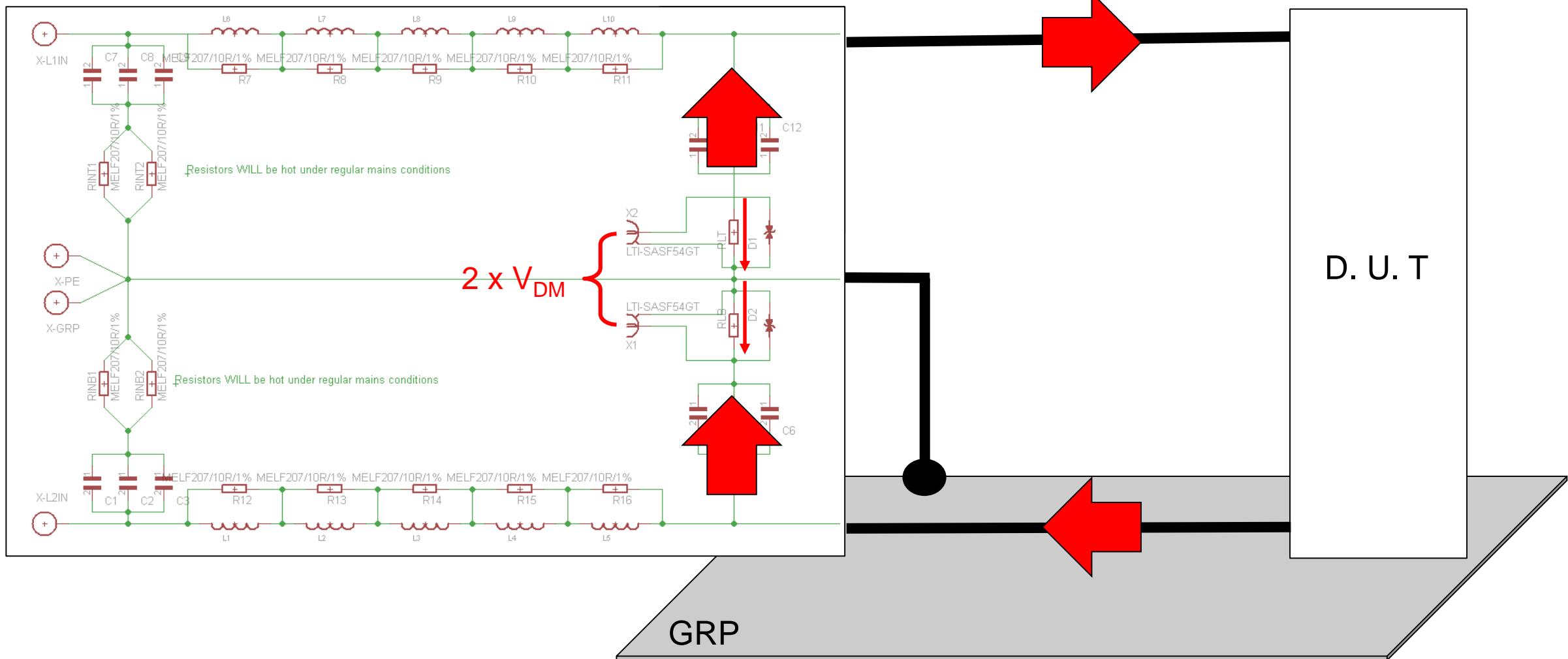
Going further with simulation

Splitting CM and DM



Going further with simulation

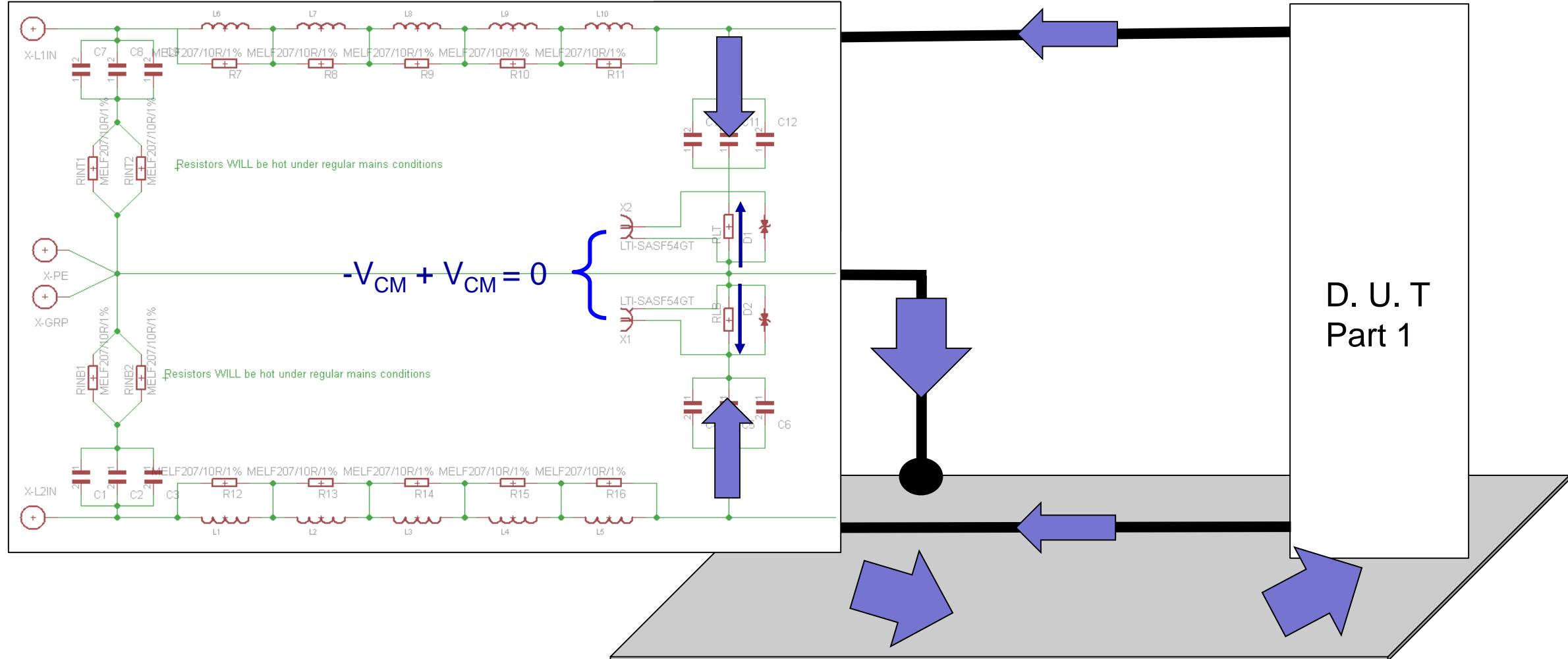
Splitting CM and DM



Going further with simulation

Splitting CM and DM

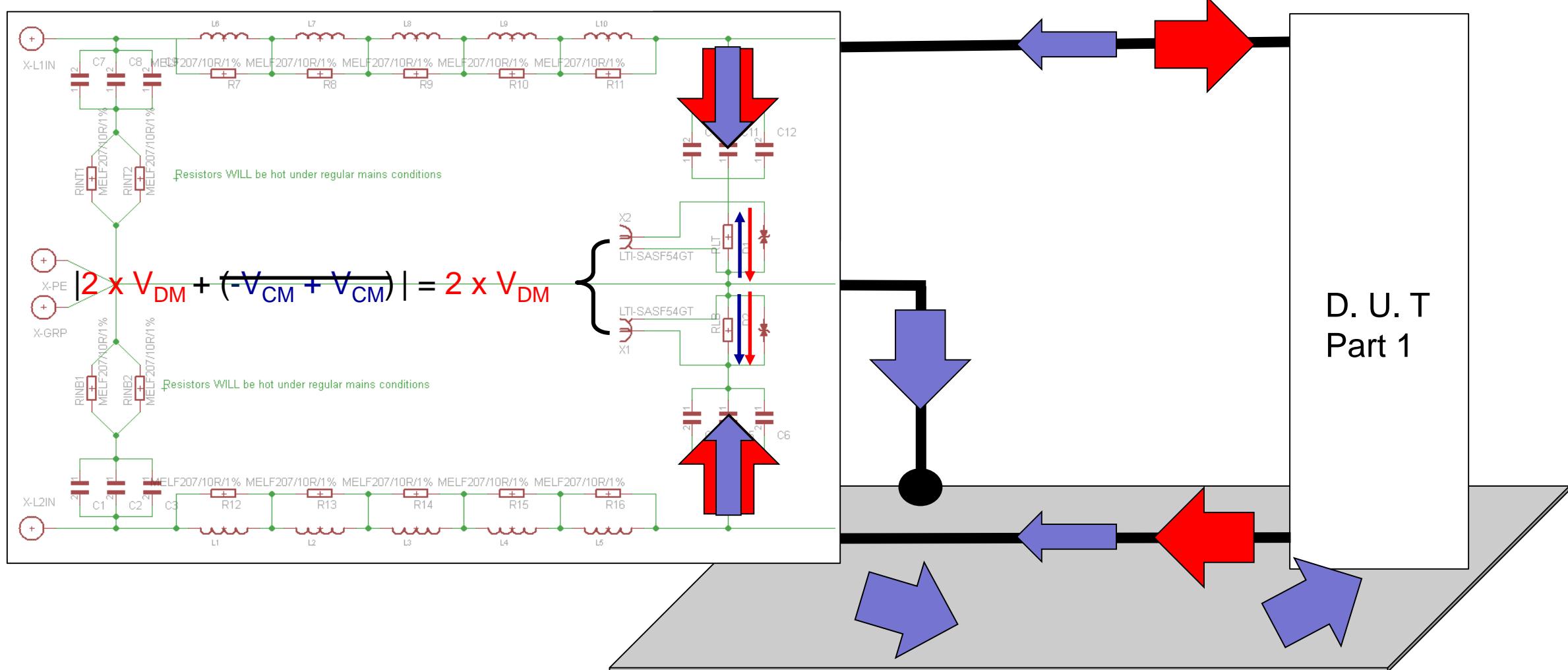
- Asymmetrical interference ?



Going further with simulation

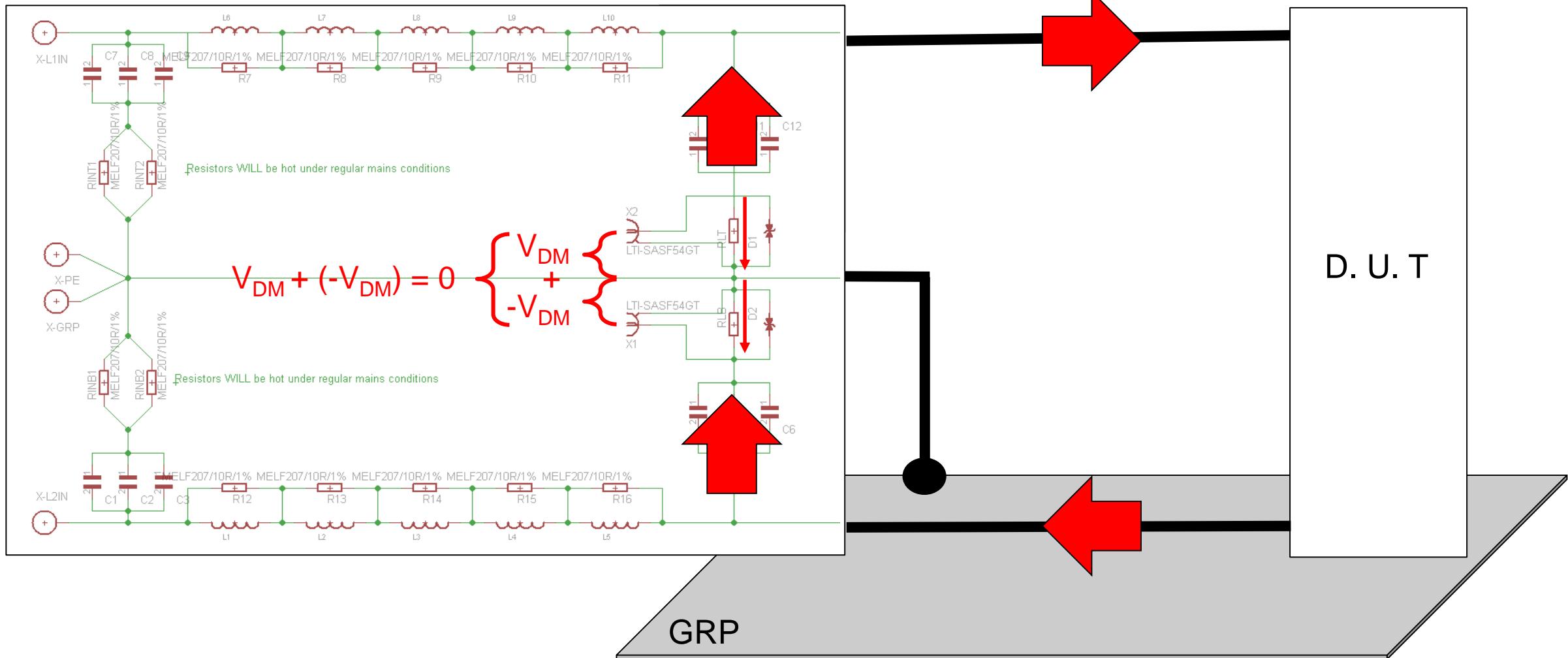
Splitting CM and DM

- Asymmetrical interference ?



Going further with simulation

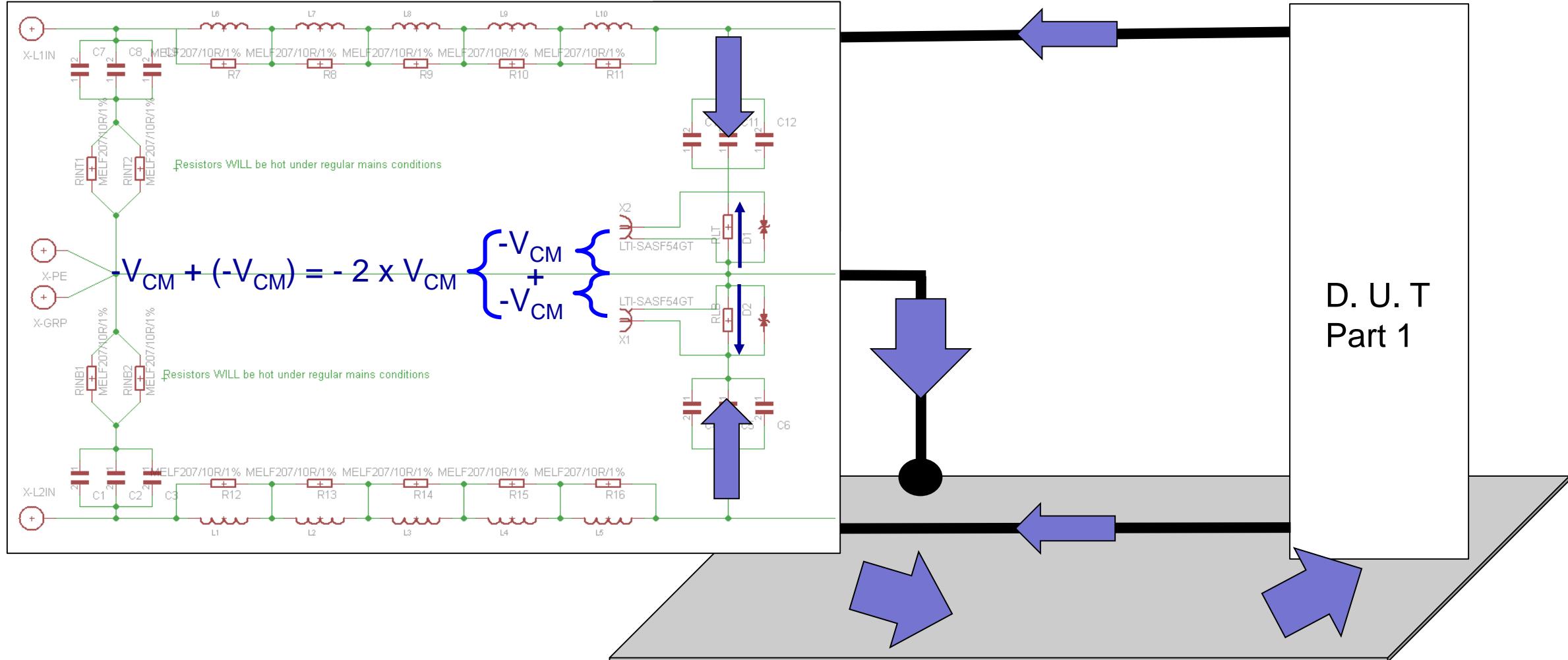
Splitting CM and DM



Going further with simulation

Splitting CM and DM

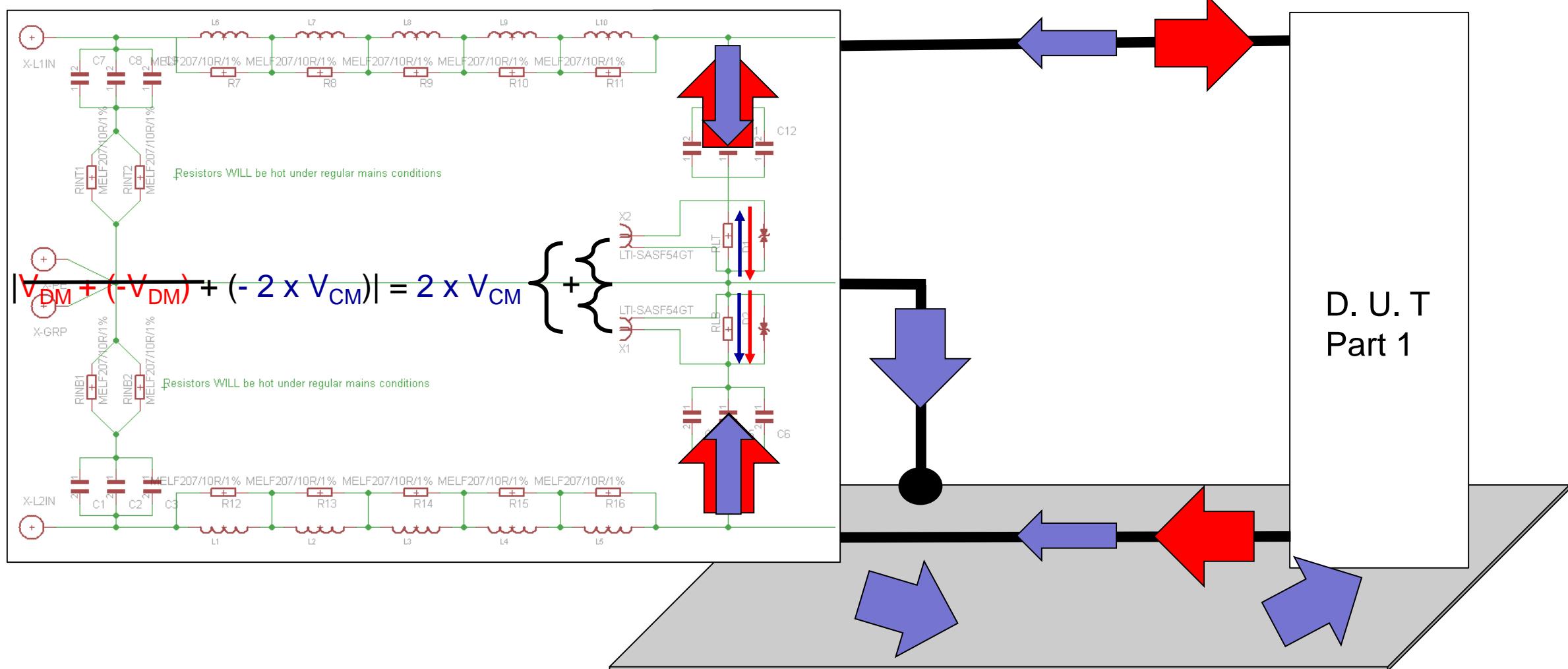
- Asymmetrical interference ?



Going further with simulation

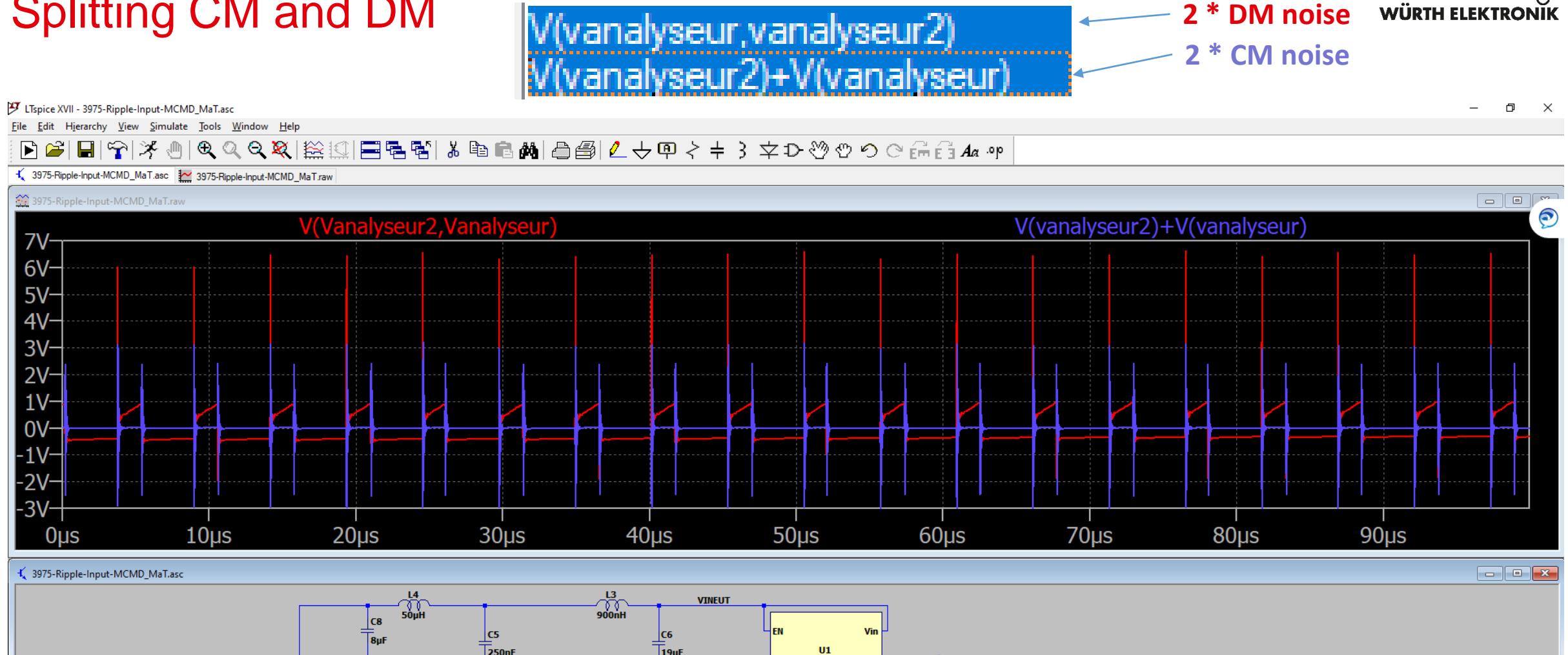
Splitting CM and DM

- Asymetrical interference ?



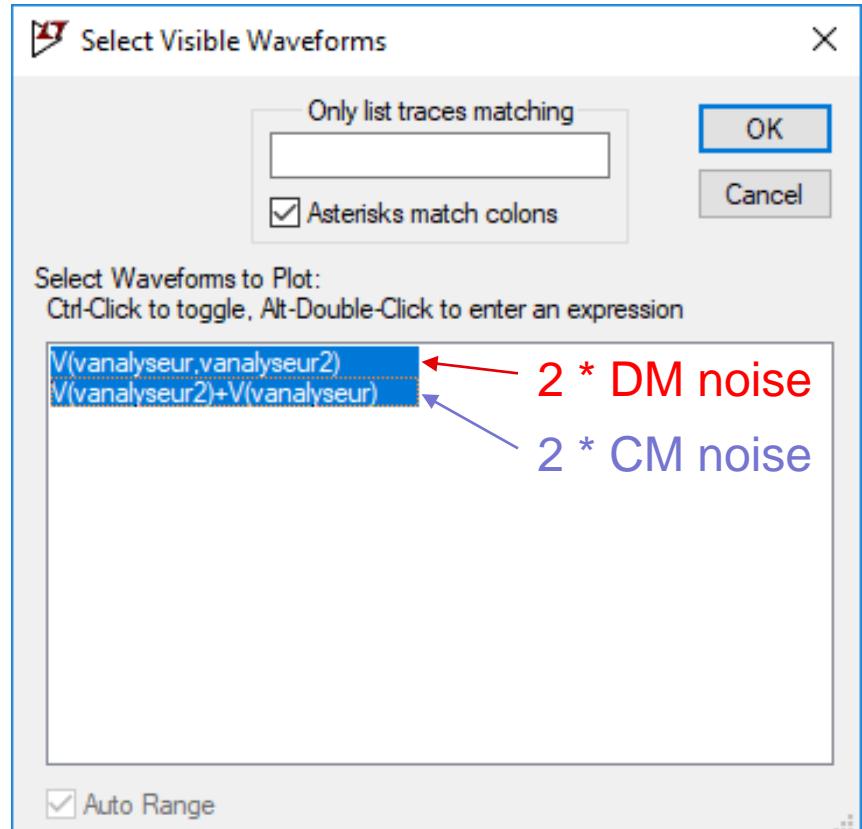
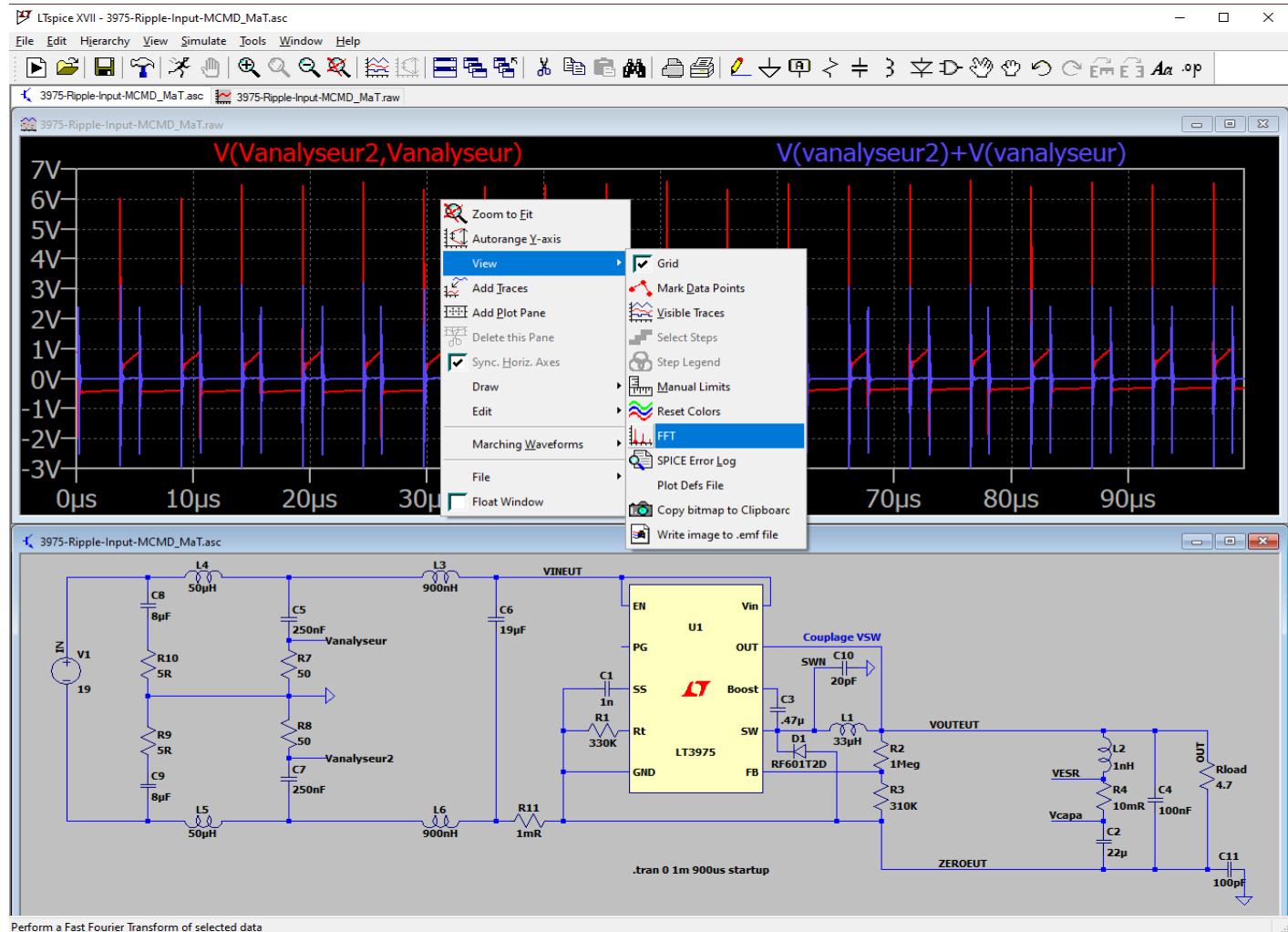
Going further with simulation

Splitting CM and DM



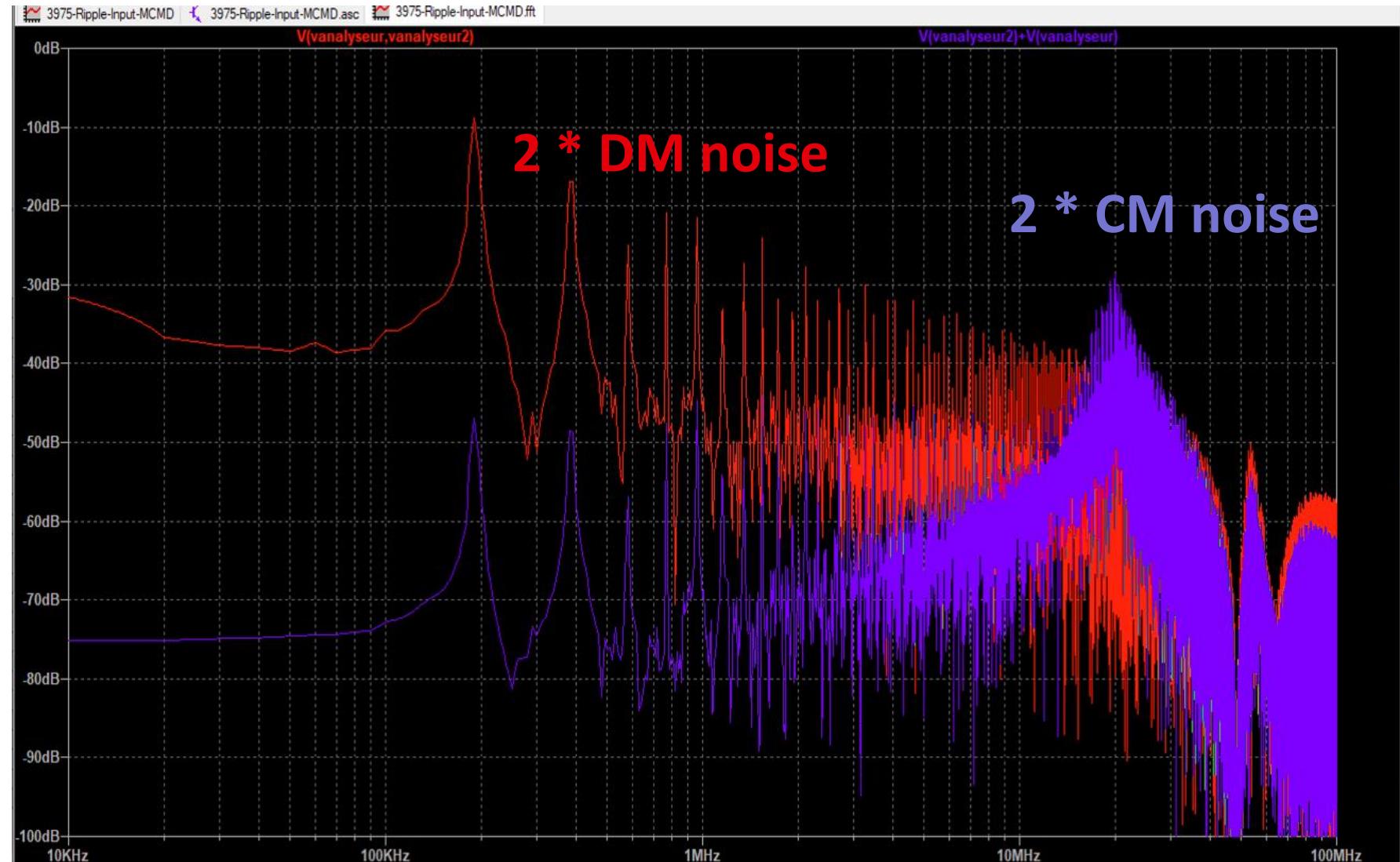
Going further with simulation

Splitting CM and DM



Going further with simulation

Splitting CM and DM

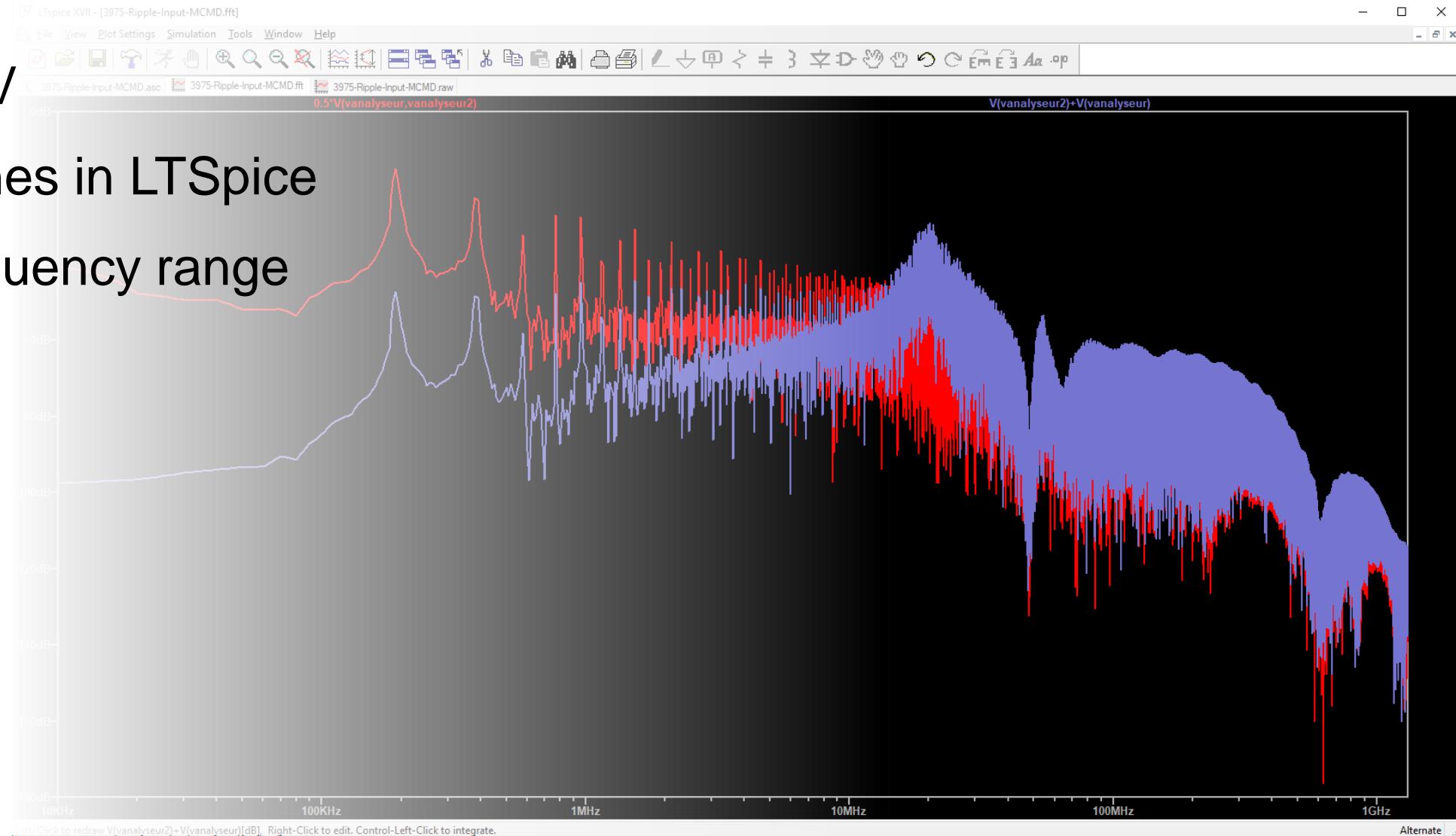


Going further with simulation

Making simulation look real

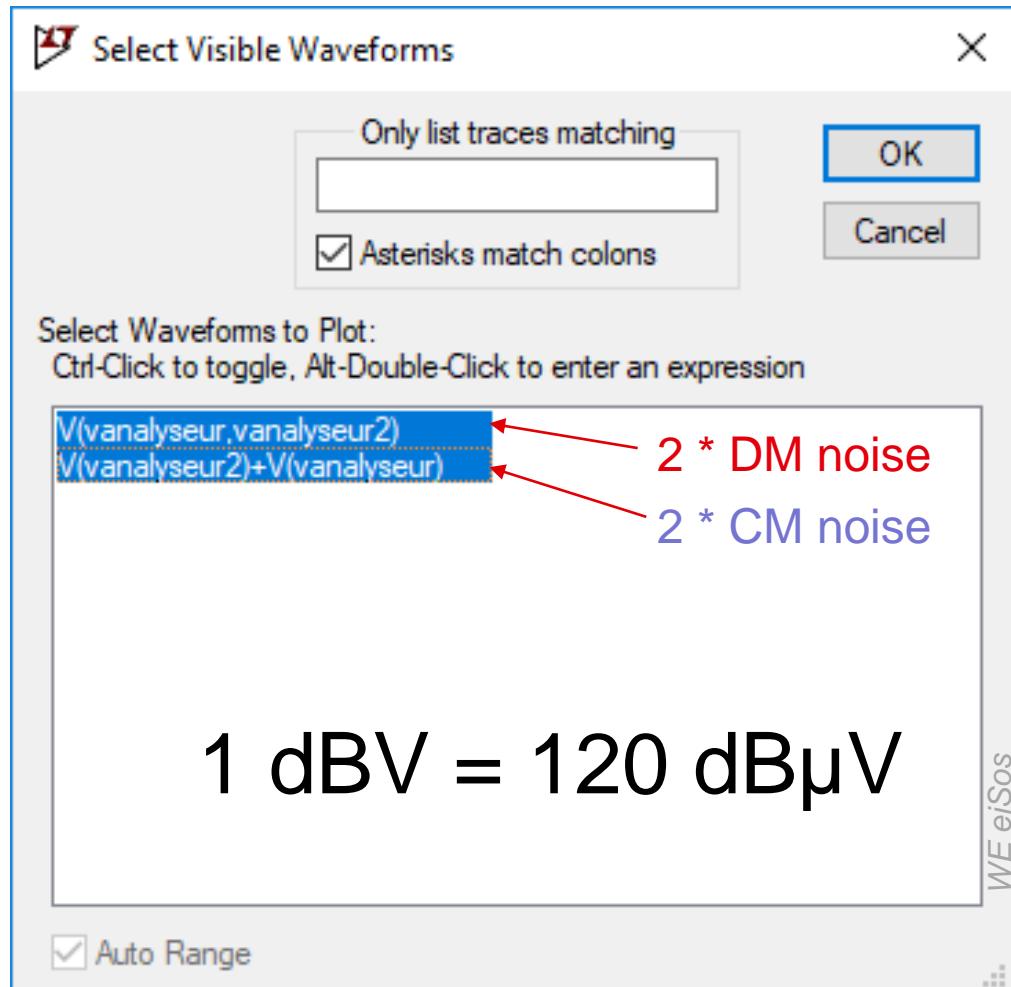


- Scaling to dB μ V
- Loading limit lines in LTSpice
- Defining a Frequency range



Going further with simulation

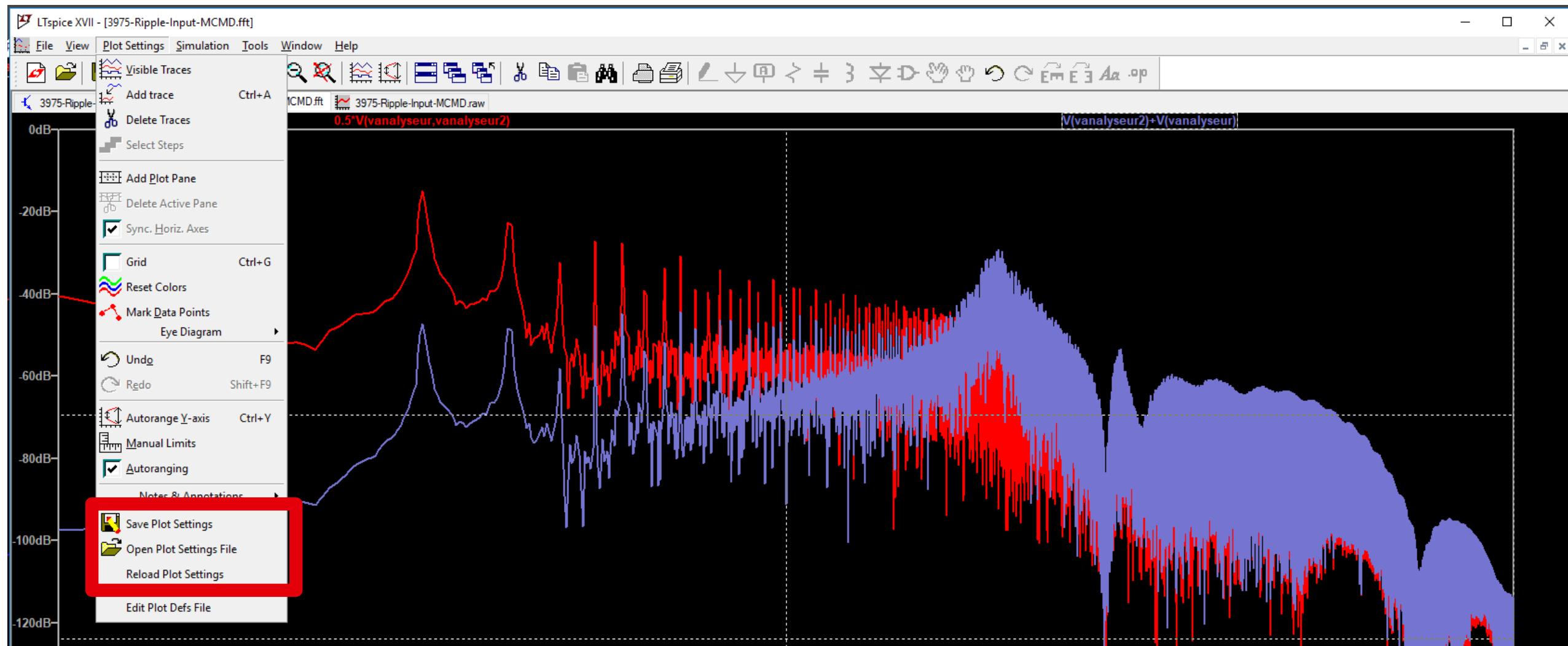
Making simulation look real



$$1 \text{ dBV} = 120 \text{ dB}\mu\text{V}$$

Going further with simulation

Making simulation look real



Going further with simulation

Making simulation look real – Adding limit lines



	Start	End	Amp dB μ V start	Amp dB μ V stop	Line def for LTSPICE
Line	1	9000	50000	110	110 (9000,0.316227766016838) (50000,0.316227766016838)
Line	2	50000	150000	90	80 (50000,0.0316227766016838) (150000,0.01)
Line	3	150000	500000	66	56 (150000,0.00199526231496888) (500000,0.000630957344480192)
Line	4	500000	5000000	56	56 (500000,0.000630957344480192) (5000000,0.000630957344480192)
Line	5	5000000	30000000	60	60 (5000000,0.001) (30000000,0.001)

Fill according to
EMC standards

Copy the result

Paste it here

```
Flyback-example-2-base - Bloc-notes
Fichier Édition Format Affichage Aide
[FFT of time domain data]
{
    Npanes: 1
    {
        traces: 1 {2,0,"V(vanalyseur2)+V(vanalyseur)"}
        X: ('M',0,9000,0,3000000)
        Y[0]: (' ',0,1e-006,10,1)
        Y[1]: (' ',0,-200,40,200)
        Log: 1 2 0
        PltMag: 1
        Line: "dB" 4 0 (9000,0.3162277660168) (50000,0.316227766)
        Line: "dB" 4 0 (50049.8435712172,0.0317065818612387) (150407.110289202,0.0100397786508485)
        Line: "dB" 4 0 (150000,0.00199526231496888) (500000,0.000630957344480192)
        Line: "dB" 4 0 (500000,0.000630957344480192) (5000000,0.000630957344480192)
        Line: "dB" 4 0 (5000000,0.001) (30000000,0.001)
    }
}
```

Windows (CRLF) Ln 10, Col 16 100%

Going further with simulation

Making simulation look real – Defining a range



10kHz to 30 MHz

0 to 120dB μ V

3975-Ripple-Input-MCMD-dbuv.plt - Bloc-notes

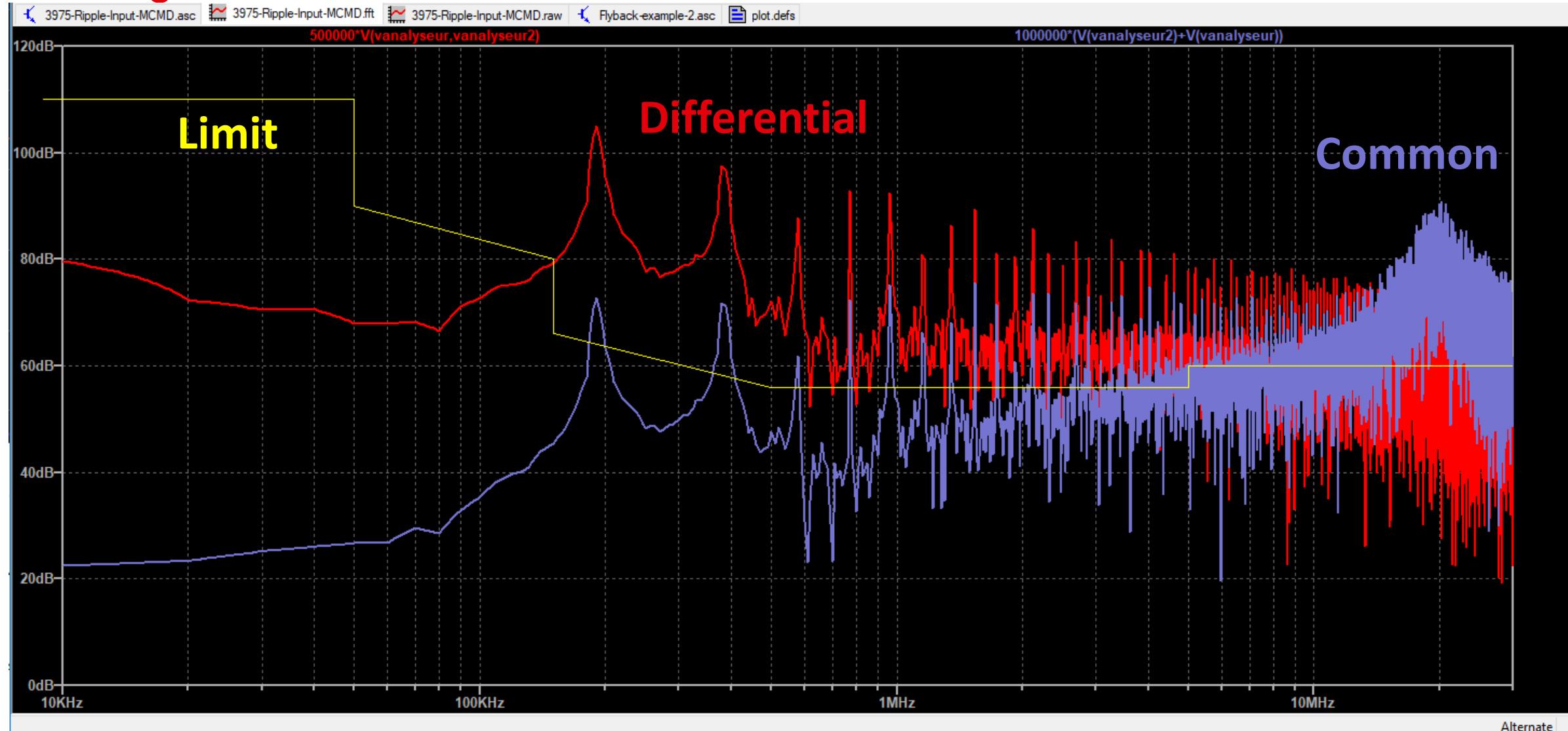
Fichier Edition Format Affichage ?

[FFT of time domain data]

```
{
    Npanes: 1
    {
        traces: 2 {65540,0,"500000*V(vanalyseur,vanalyseur2)"} {65547,0,"1000000*(V(vanalyseur2)+V(vanalyseur))"}
        X: ('M',0,10000,0,3e+007)
        Y[0]: (' ',0,1,20,1e+006)
        Log: 1 2 0
        GridStyle: 1
        PltMag: 1
        Line: "dB" 13 0 (8983.92329505352,319040.747263751) (49889.5367382049,319040.747263751)
        Line: "dB" 13 0 (50000,316227.766016838) (50000,31622.7766016838)
        Line: "dB" 13 0 (50000,31622.7766016838) (150000,10000)
        Line: "dB" 13 0 (150000,10000) (150000,1995.26231496888)
        Line: "dB" 13 0 (150000,1995.26231496888) (500000,630.957344480193)
        Line: "dB" 13 0 (500000,630.957344480193) (5000000,630.957344480193)
        Line: "dB" 13 0 (5000000,630.957344480193) (5000000,1000)
        Line: "dB" 13 0 (5000000,1000) (30000000,1000)
    }
}
```

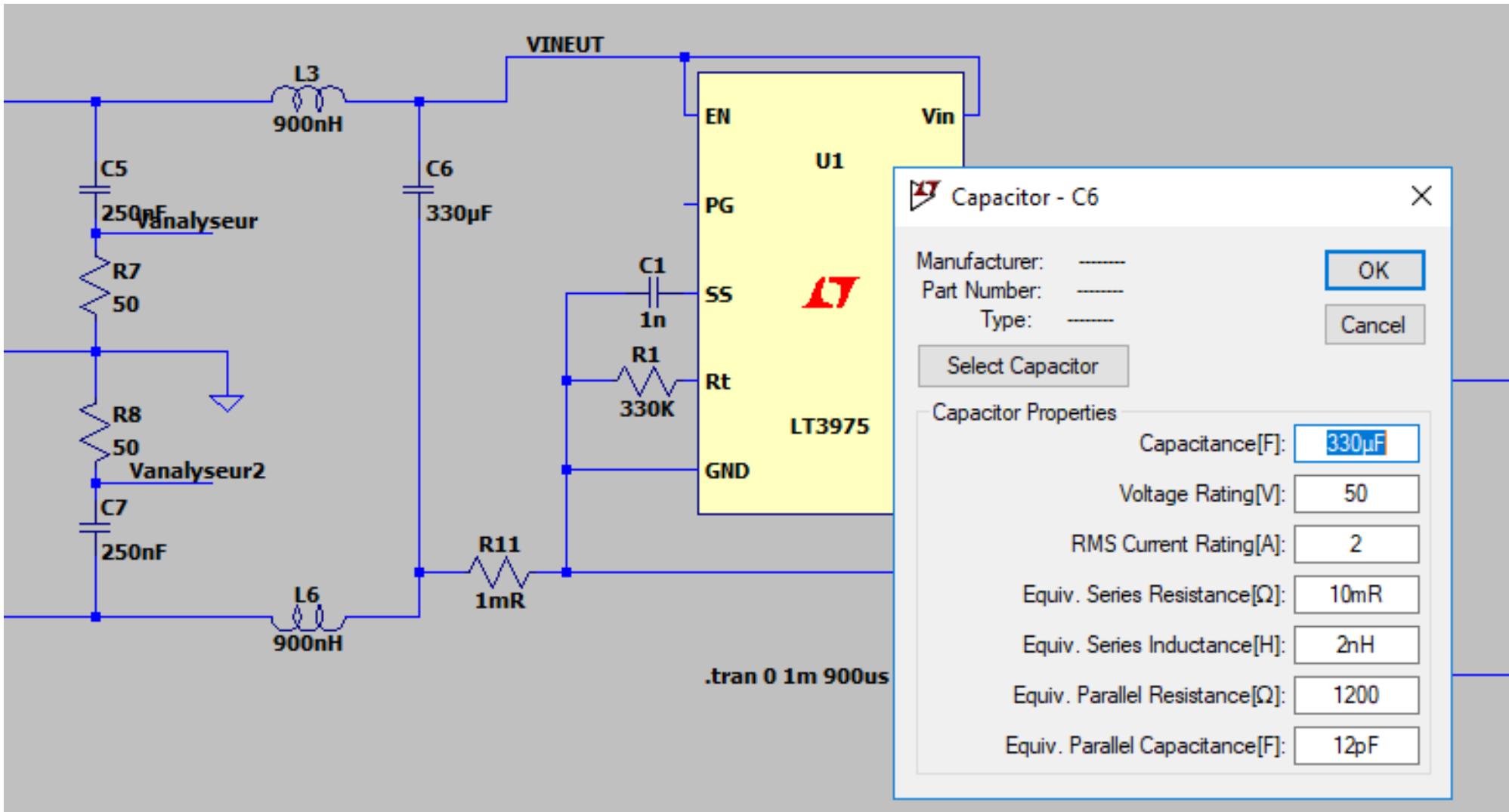
Going further with simulation

Making simulation look real – Result ☺



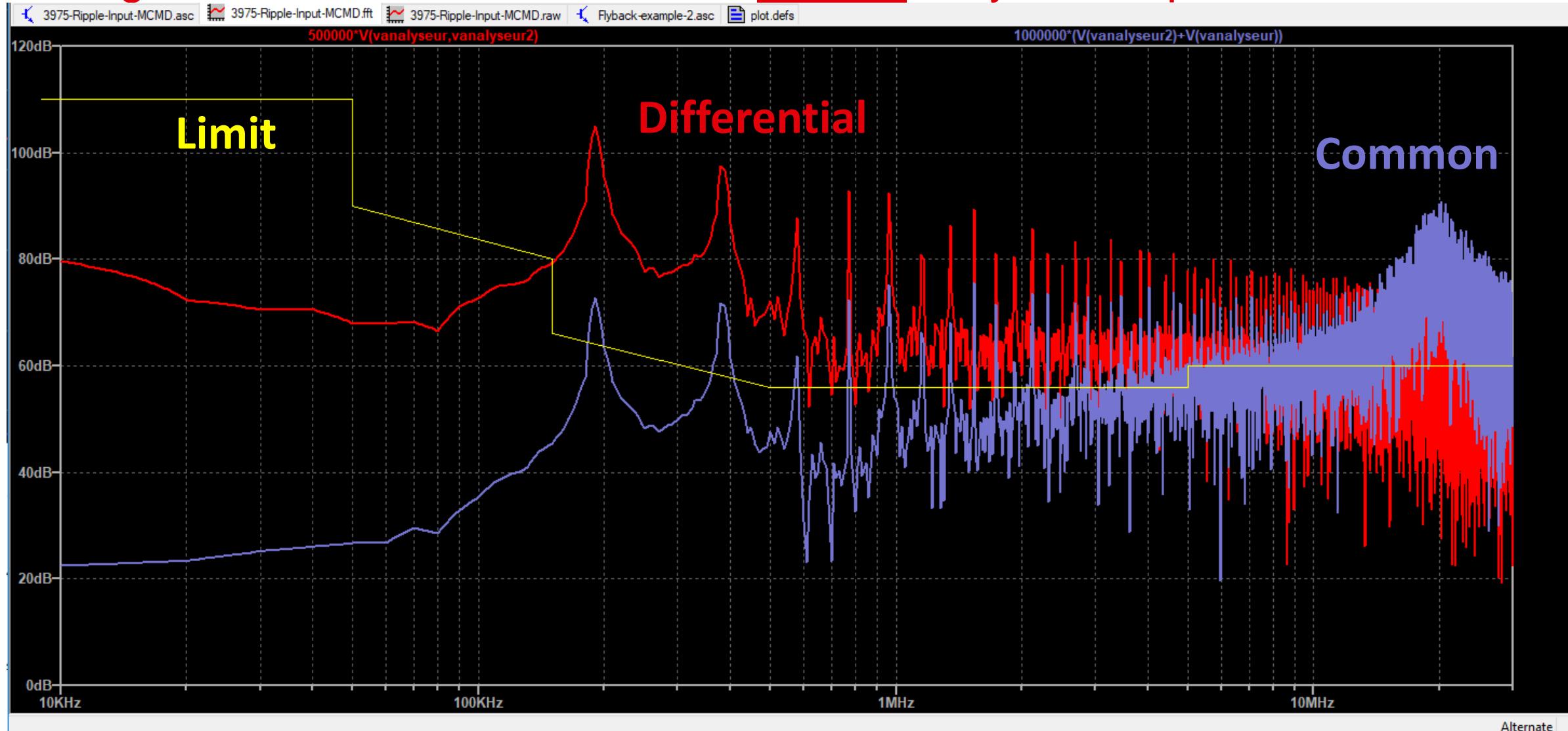
Going further with simulation

Fixing that buck in the simulation – Polymer input cap



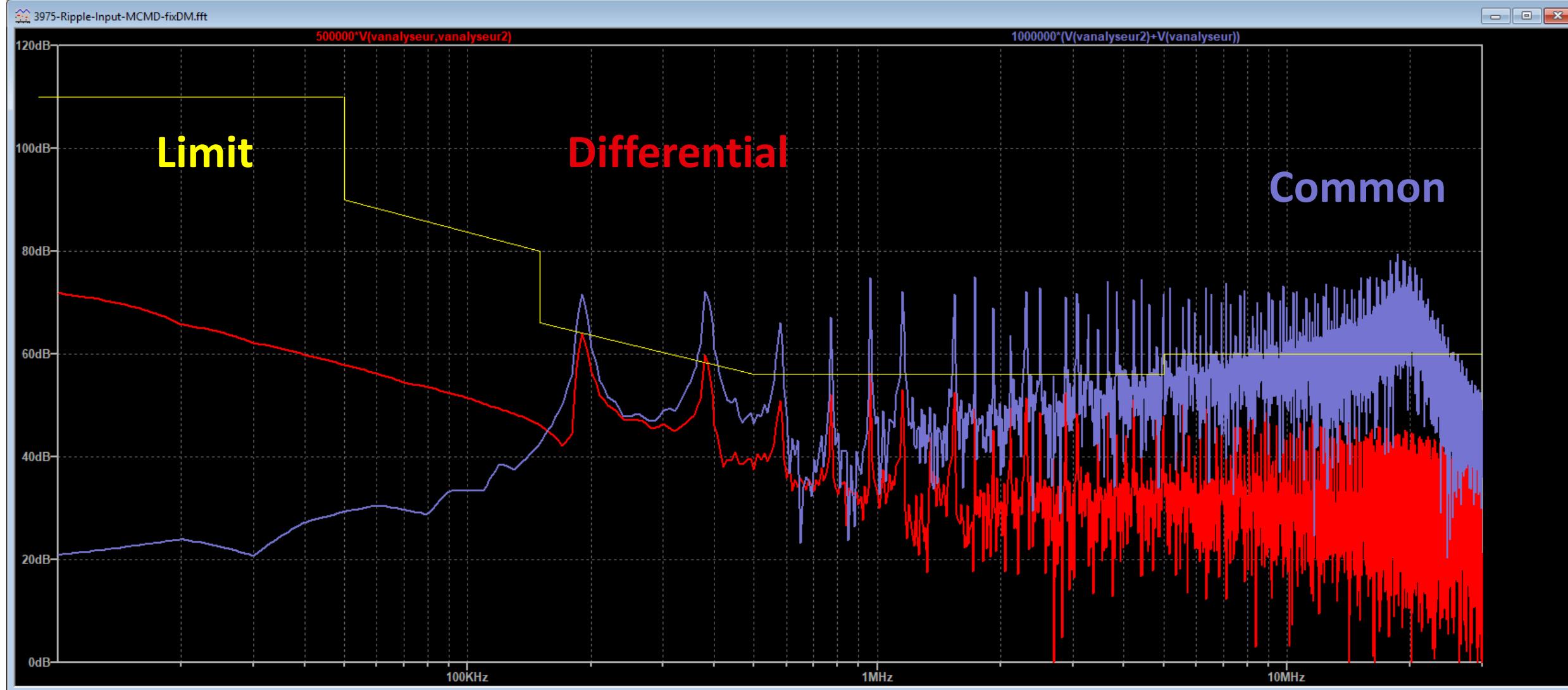
Going further with simulation

Fixing that buck in the simulation – Before Polymer Cap



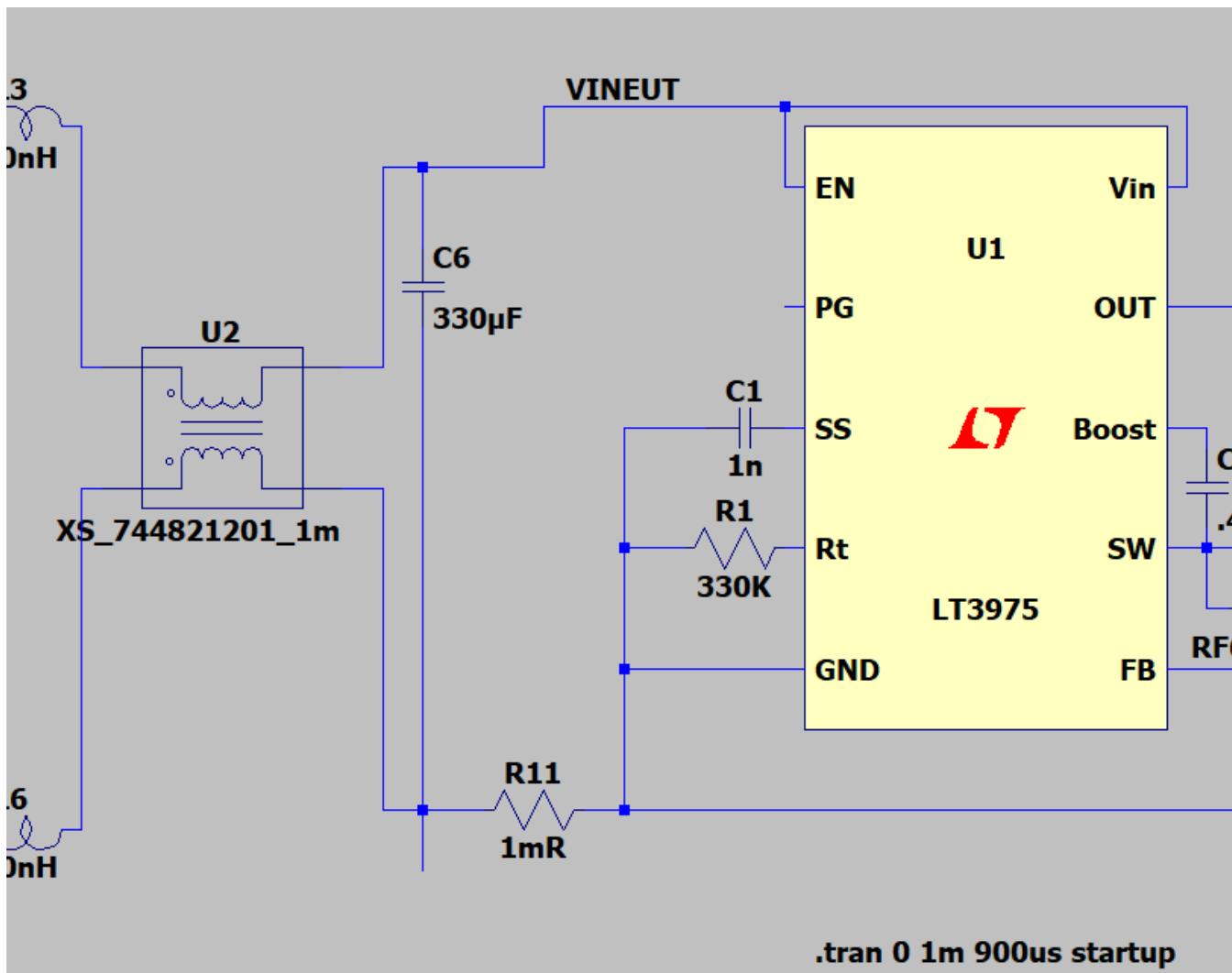
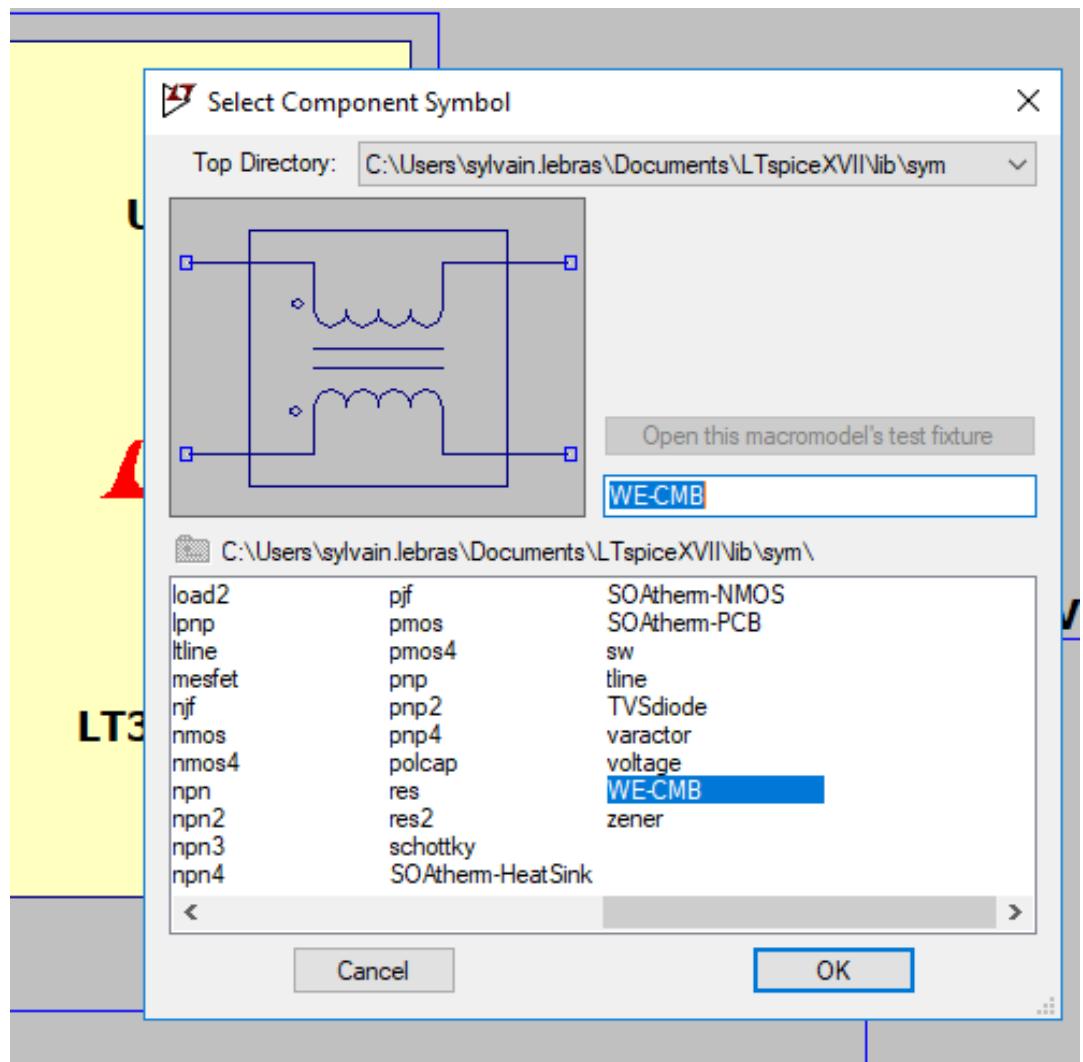
Going further with simulation

Fixing that buck in the simulation – After Polymer Cap



Going further with simulation

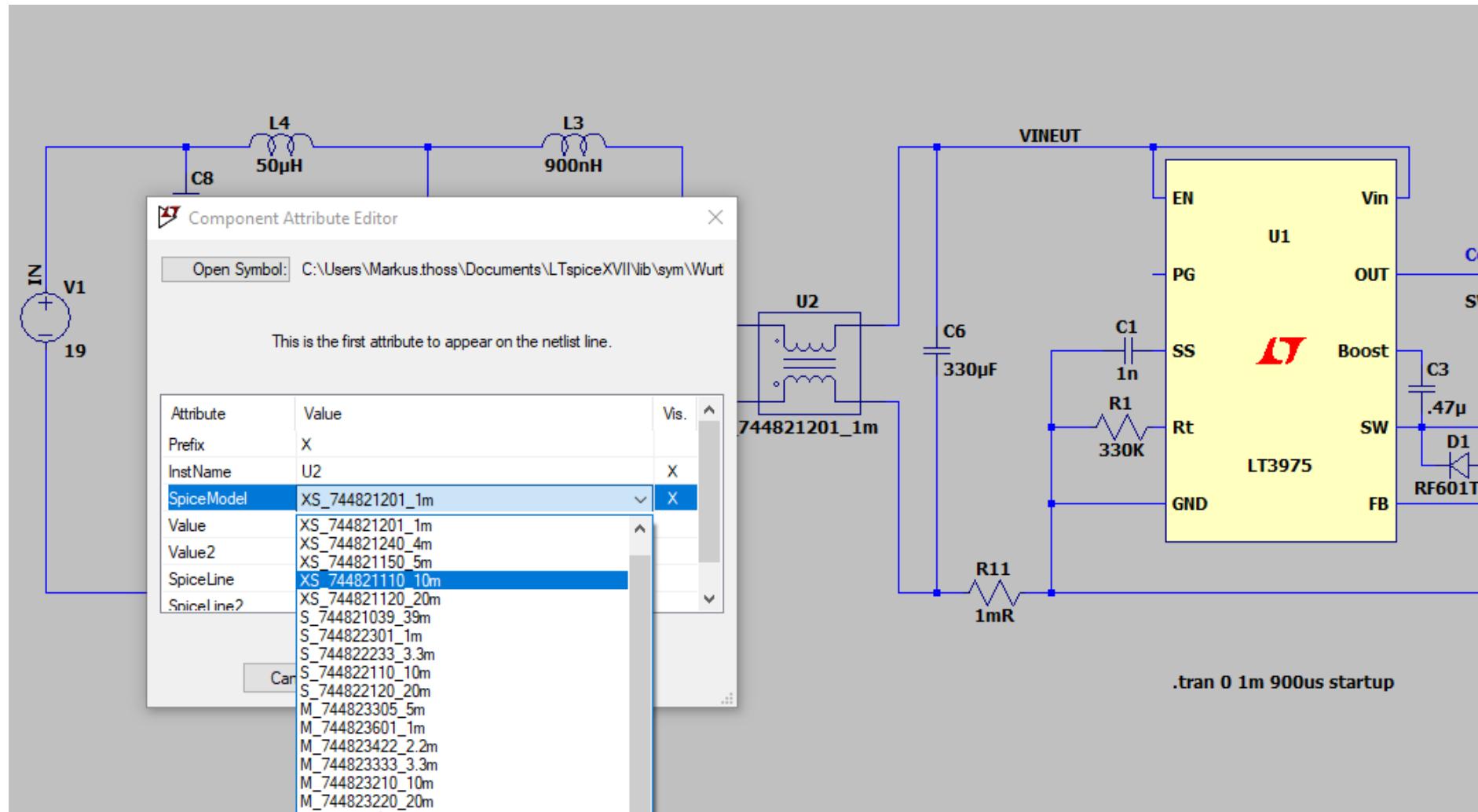
Fixing that buck in the simulation – Common mode choke



.tran 0 1m 900us startup

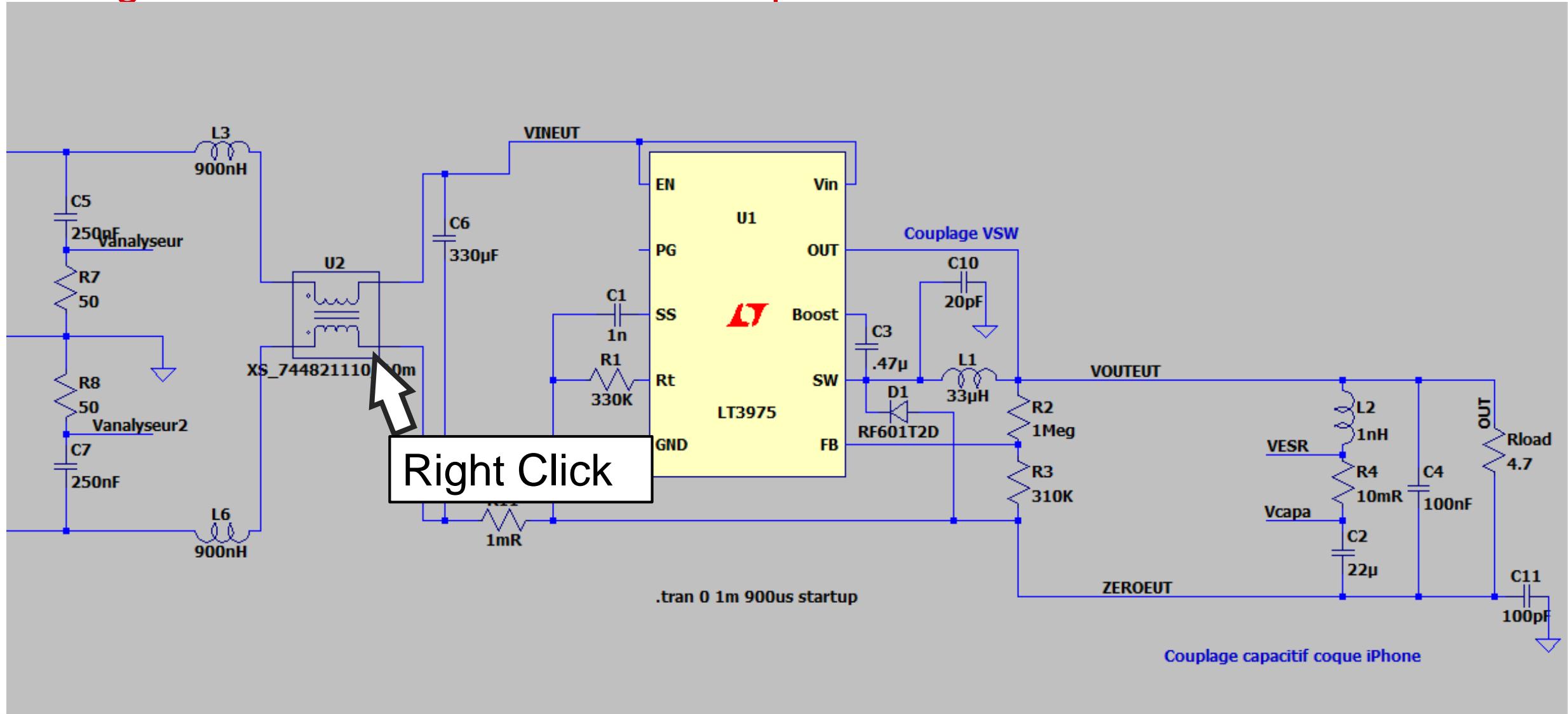
Going further with simulation

Fixing that buck in the simulation – Input Common mode choke



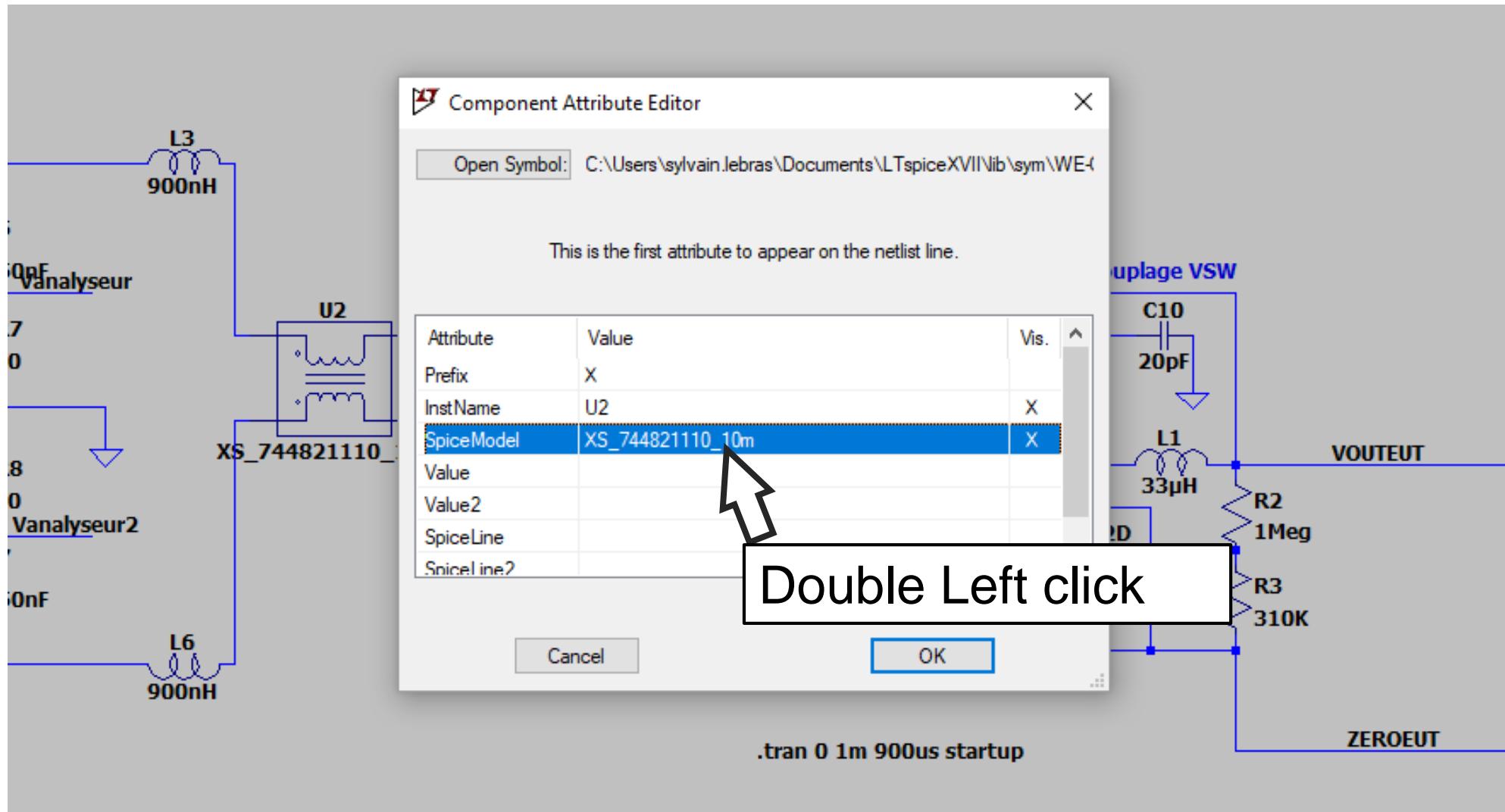
Going further with simulation

Fixing that buck in the simulation – Input Common mode choke



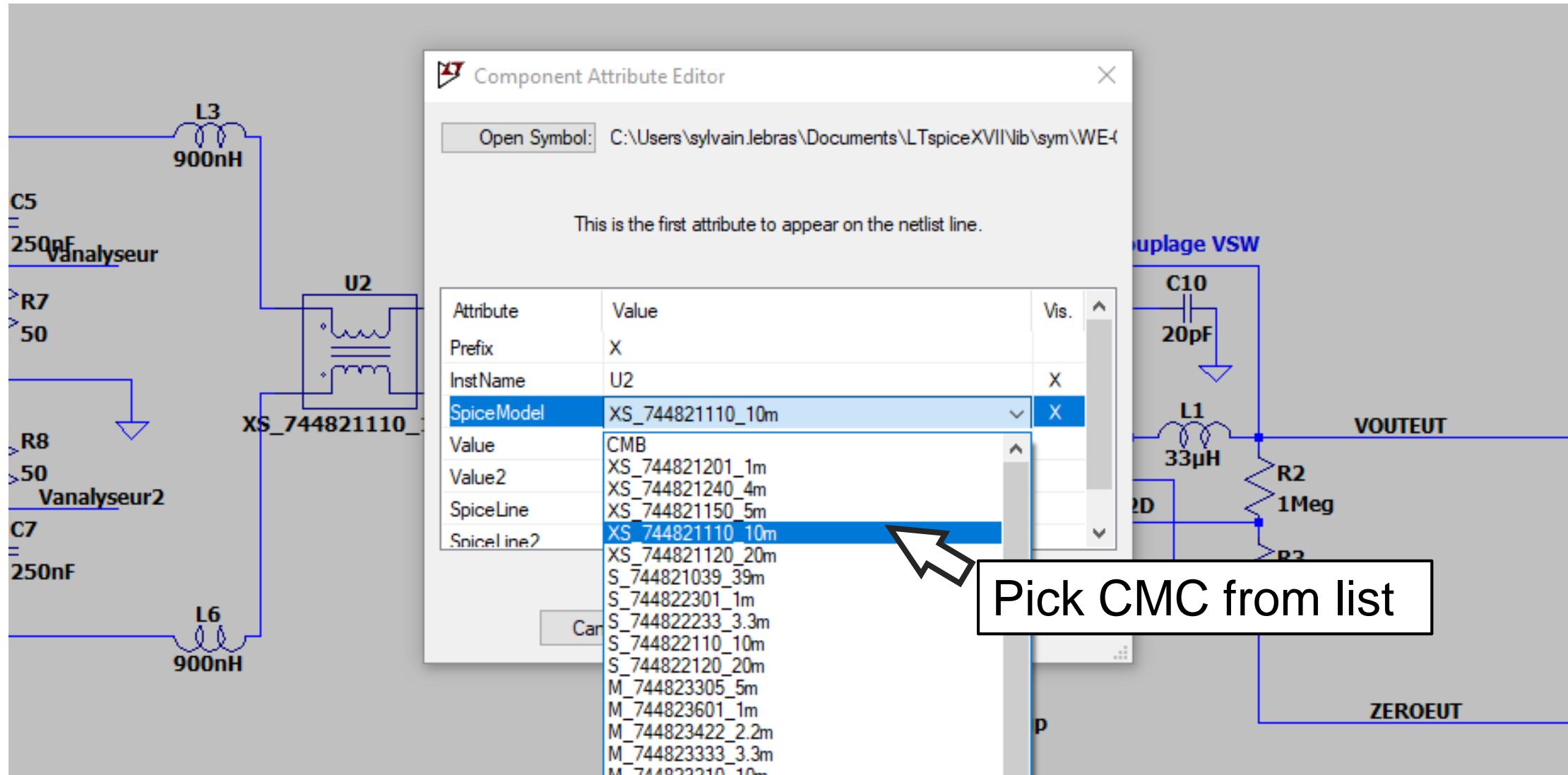
Going further with simulation

Fixing that buck in the simulation – Input Common mode choke



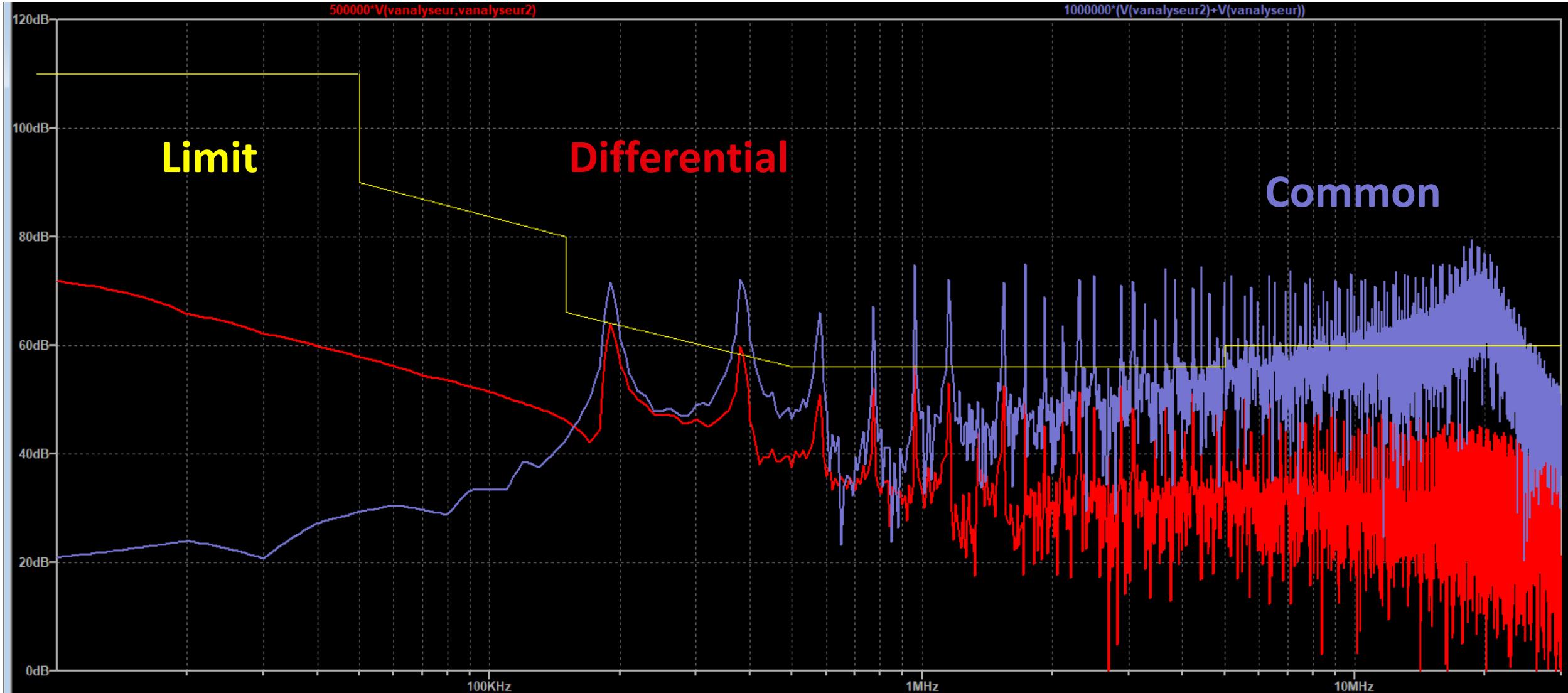
Going further with simulation

Fixing that buck in the simulation – Input Common mode choke



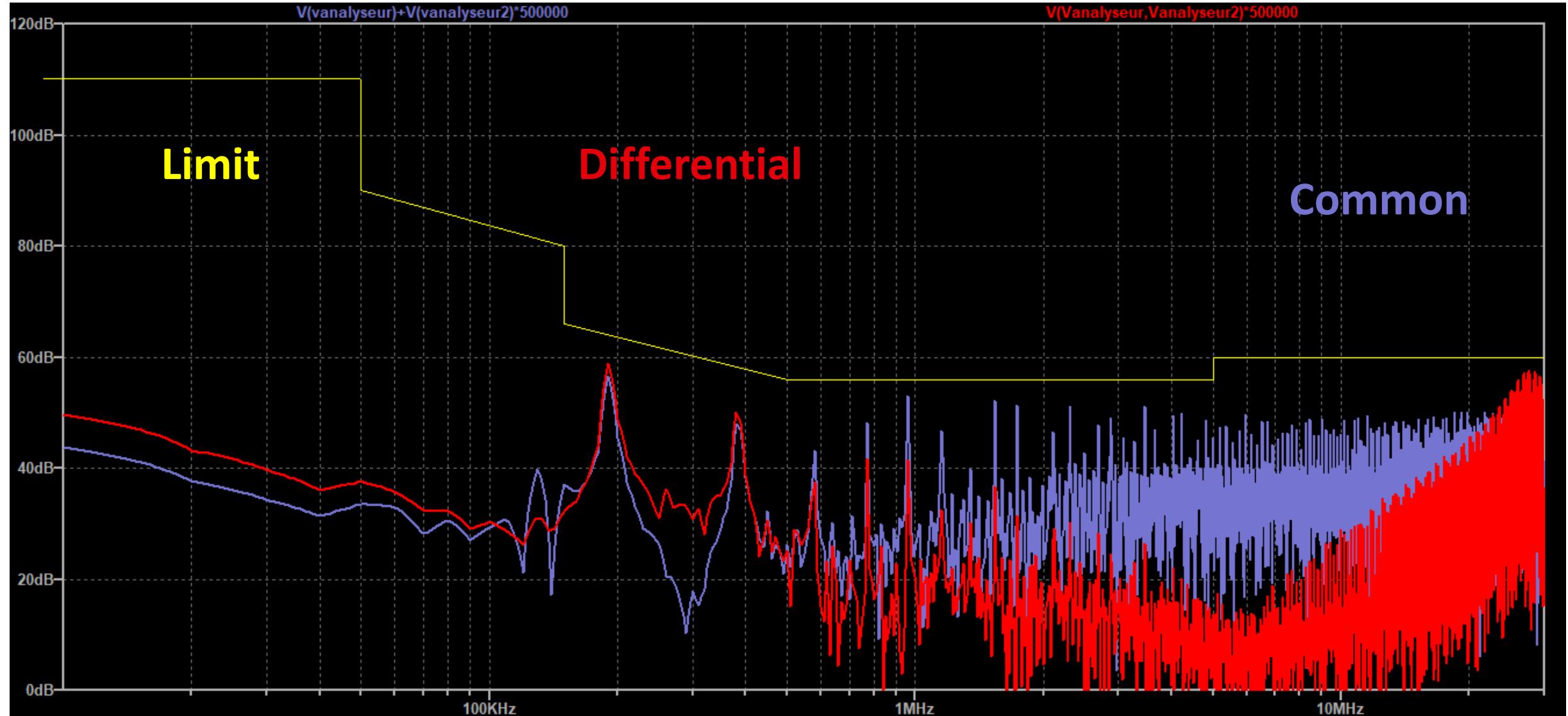
Going further with simulation

Fixing that buck in the simulation – Without Common mode choke



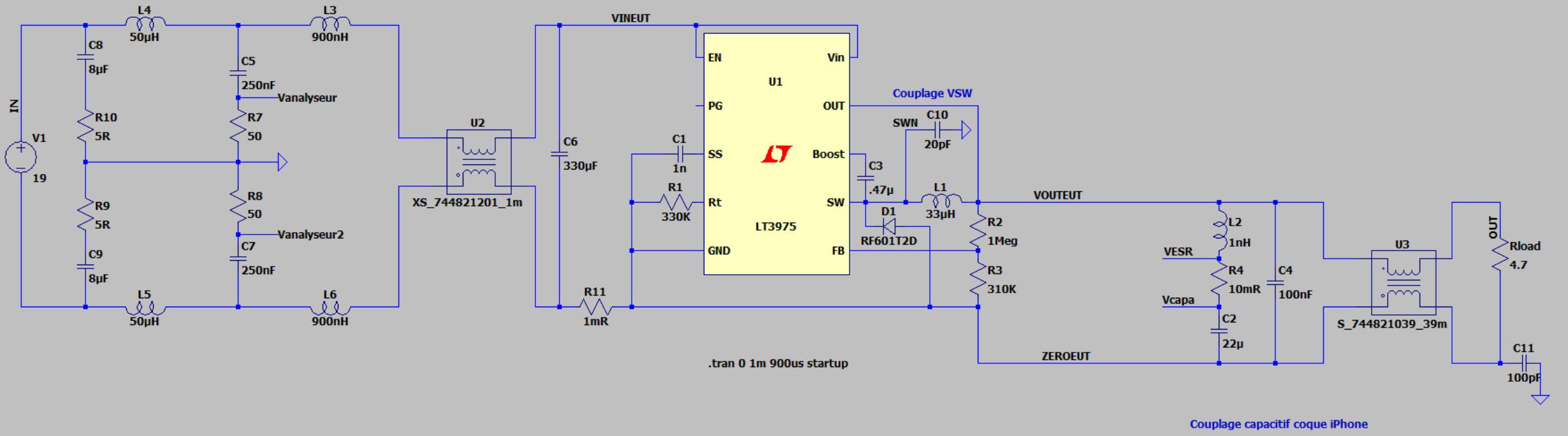
Going further with simulation

Fixing that buck in the simulation – With input Common mode choke



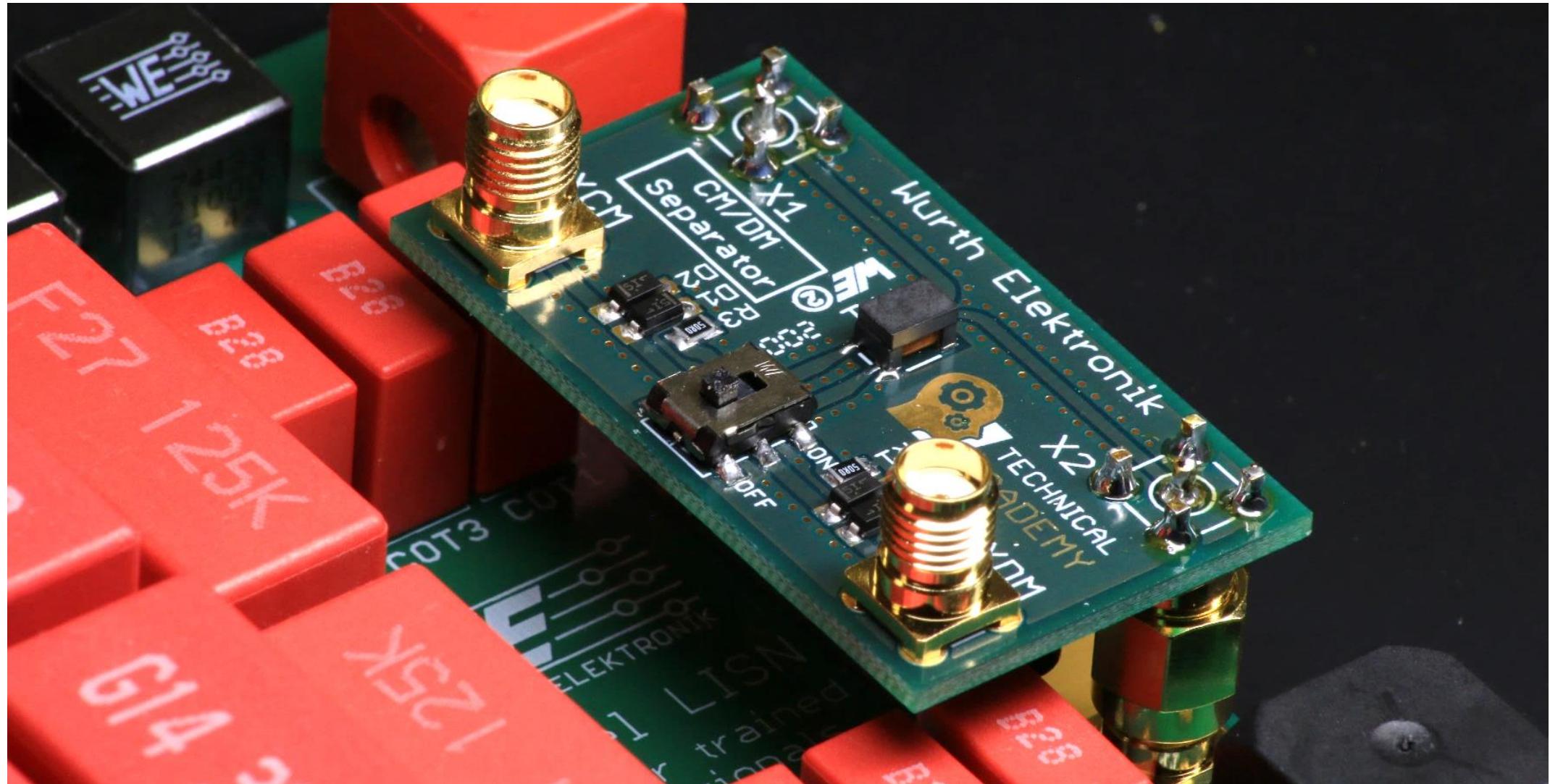
Going further with simulation

Fixing that buck in the simulation – With output CMC



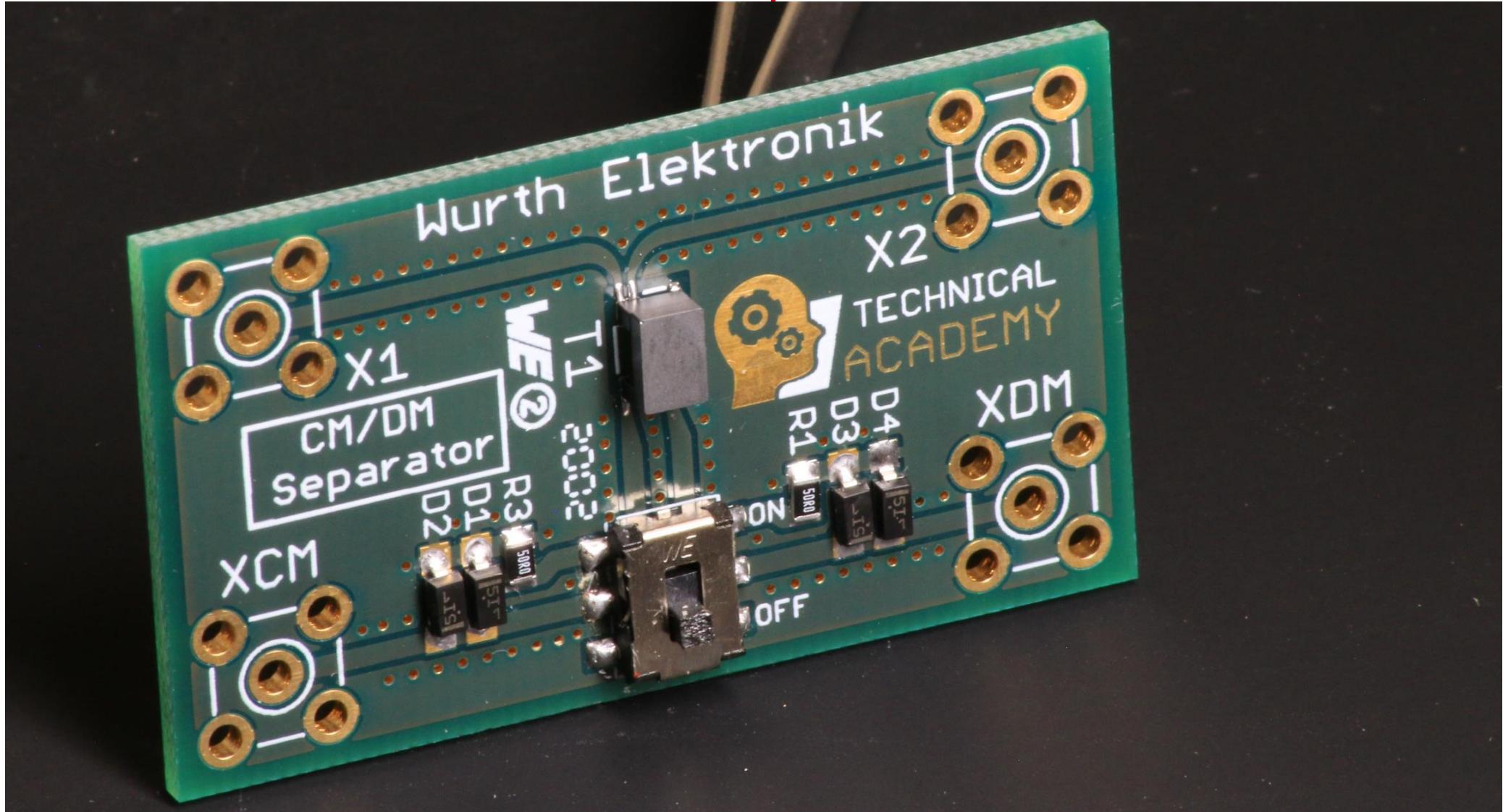
Going further ?

Common mode / Differential Mode separator in real life



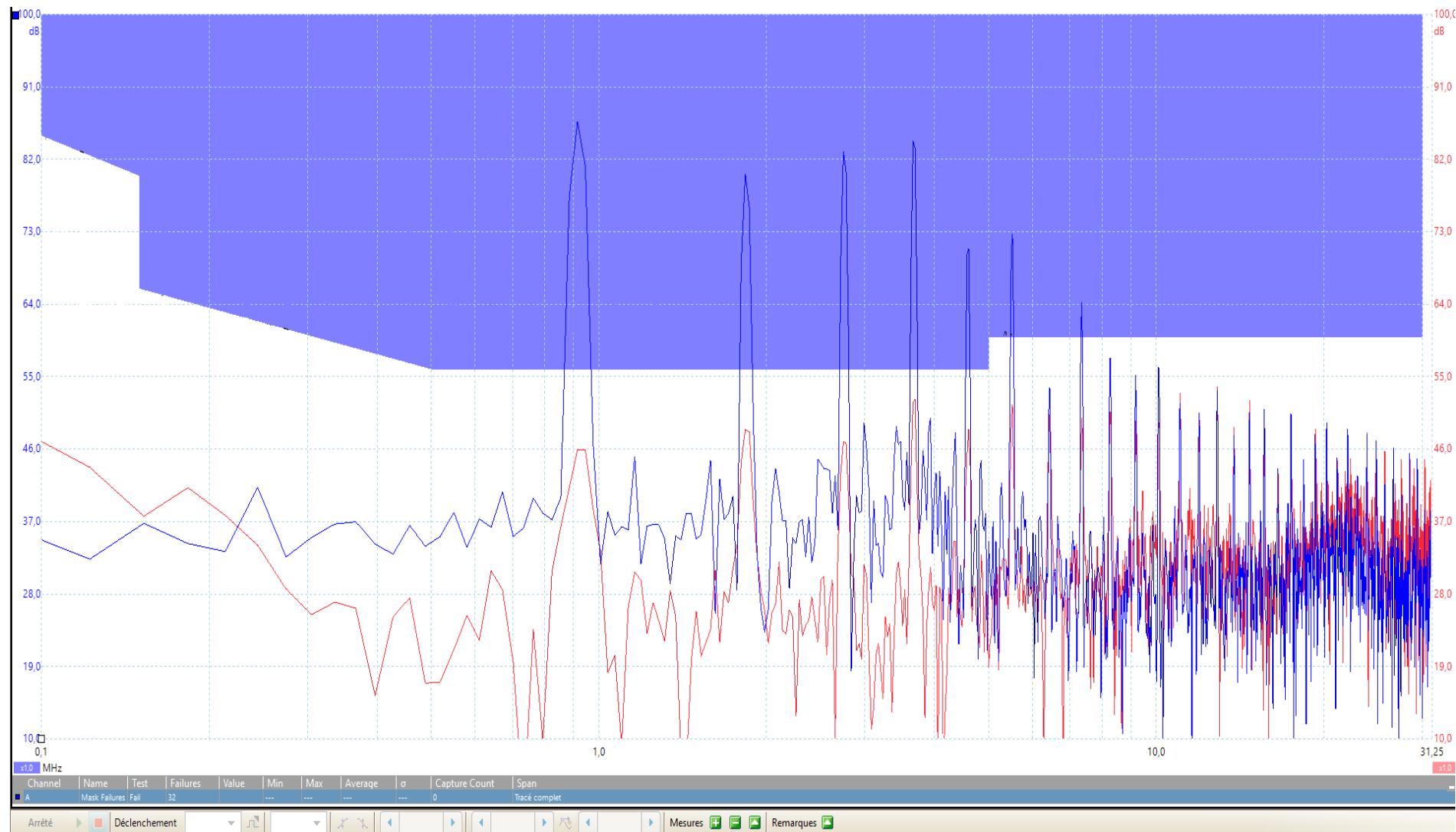
Going further ?

Common mode / Differential Mode separator in real life



Going further ?

Common mode / Differential Mode separator in real life



Modeling Real life examples

Flyback converter for lighting applications



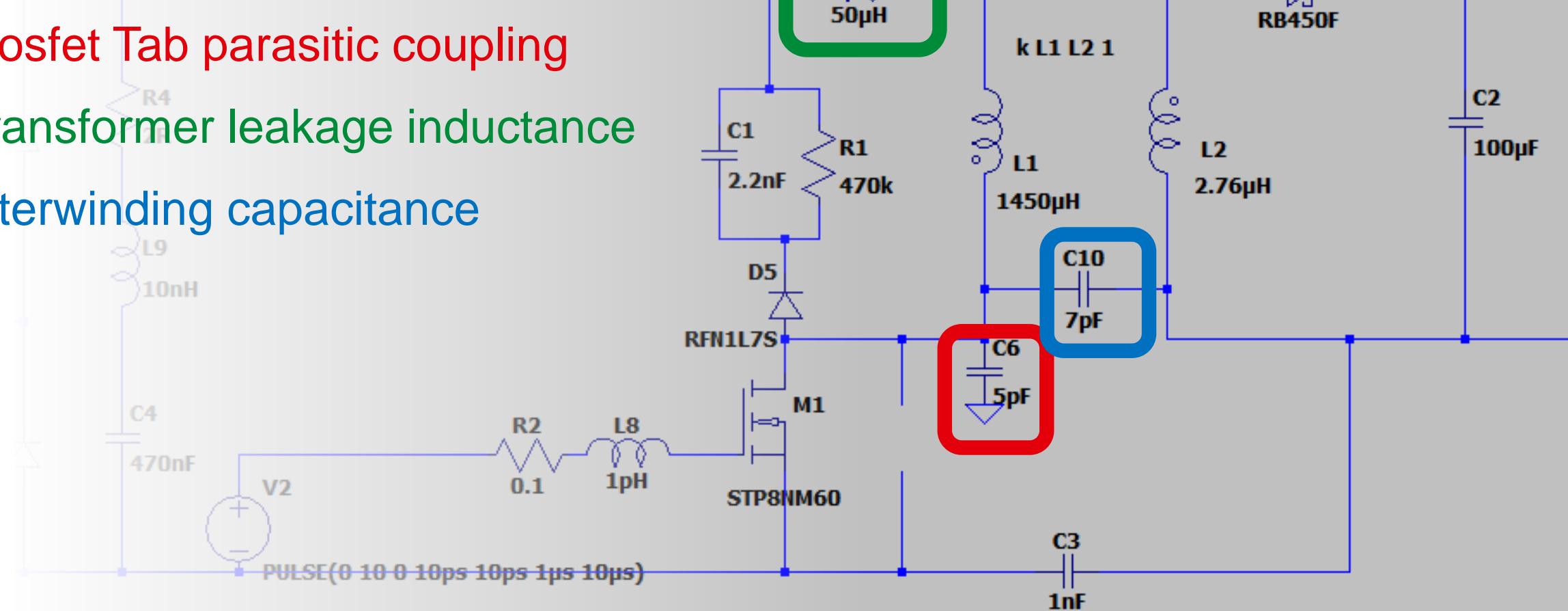
Modeling Real life examples

Flyback converter for lighting applications



- Parasitics :

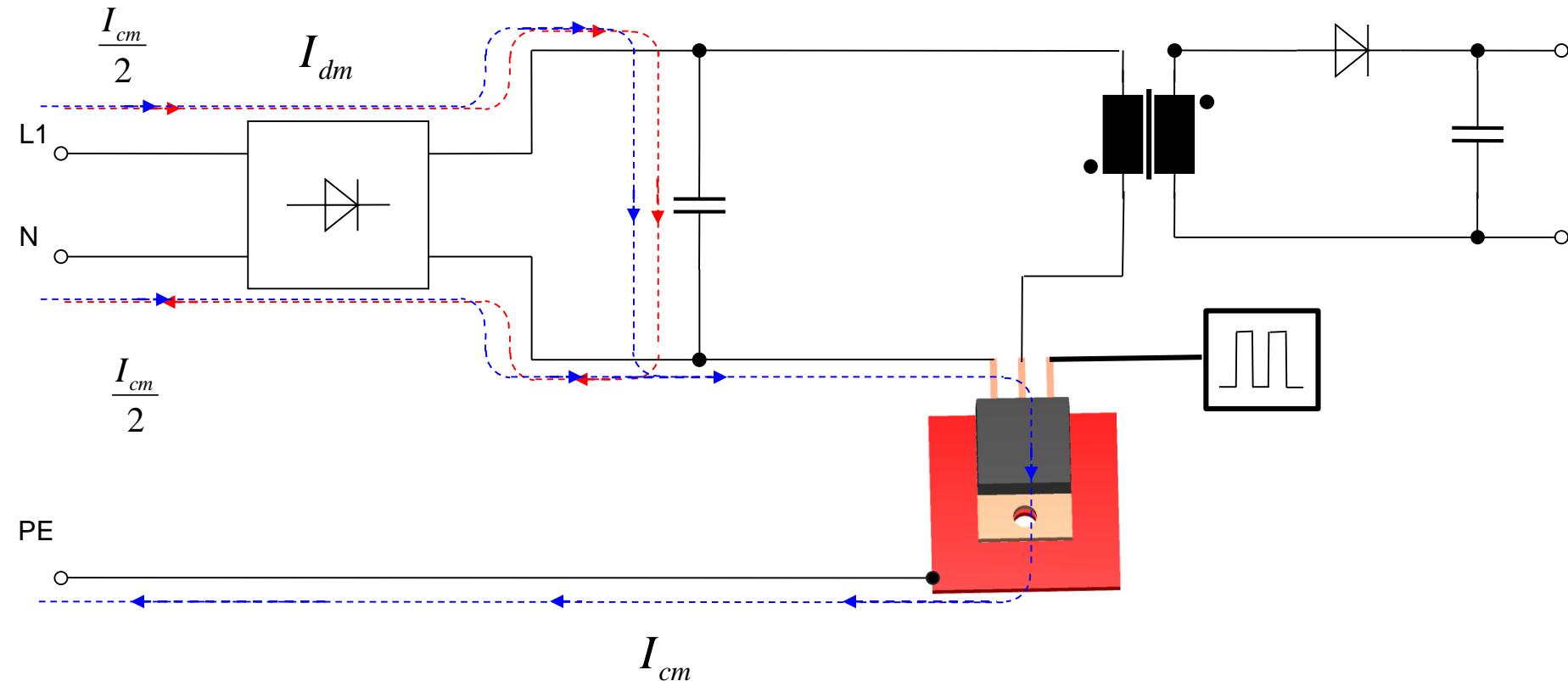
- Mosfet Tab parasitic coupling
- Transformer leakage inductance
- Interwinding capacitance



Real life examples

Flyback converter for lighting applications

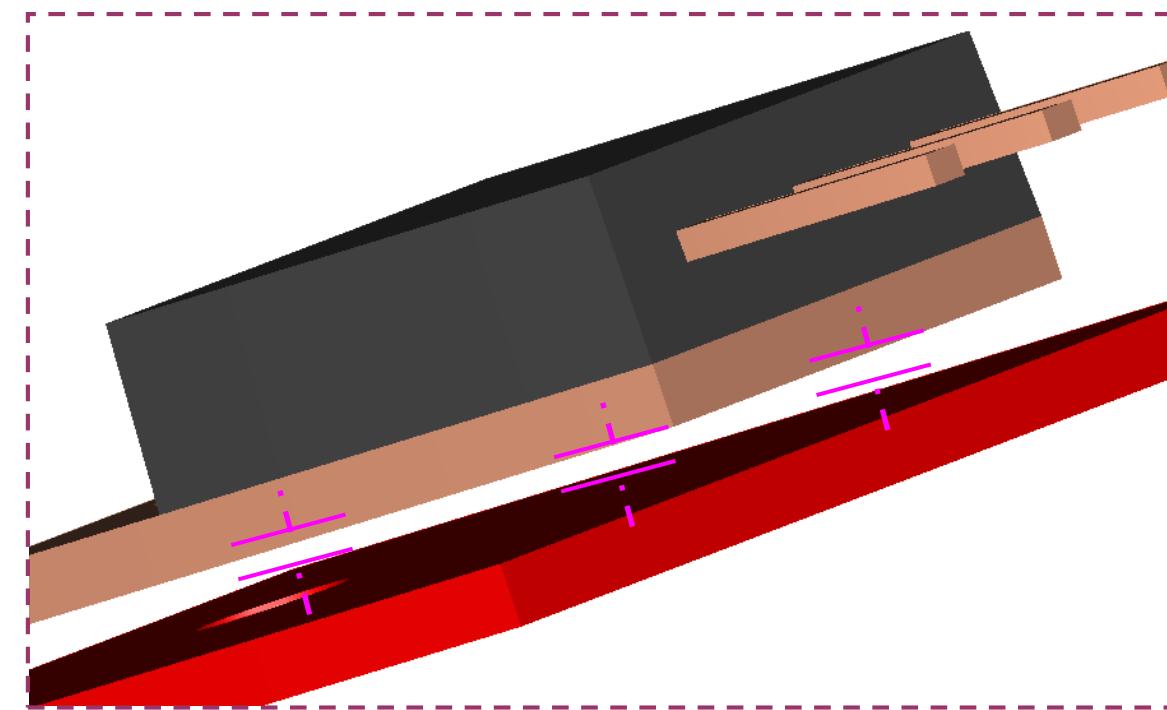
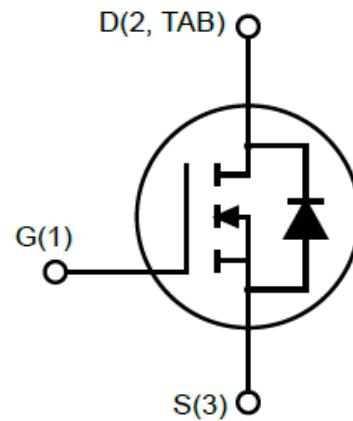
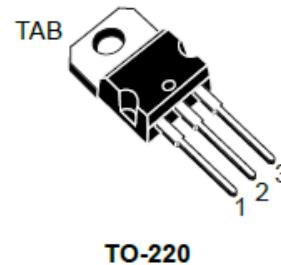
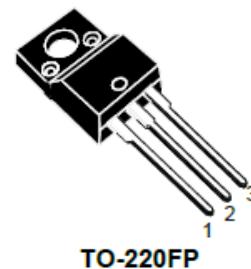
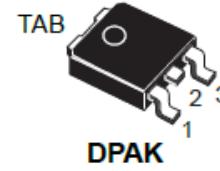
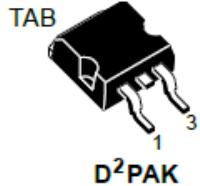
Mosfet Tab parasitic coupling



Real life examples

Flyback converter for lighting applications

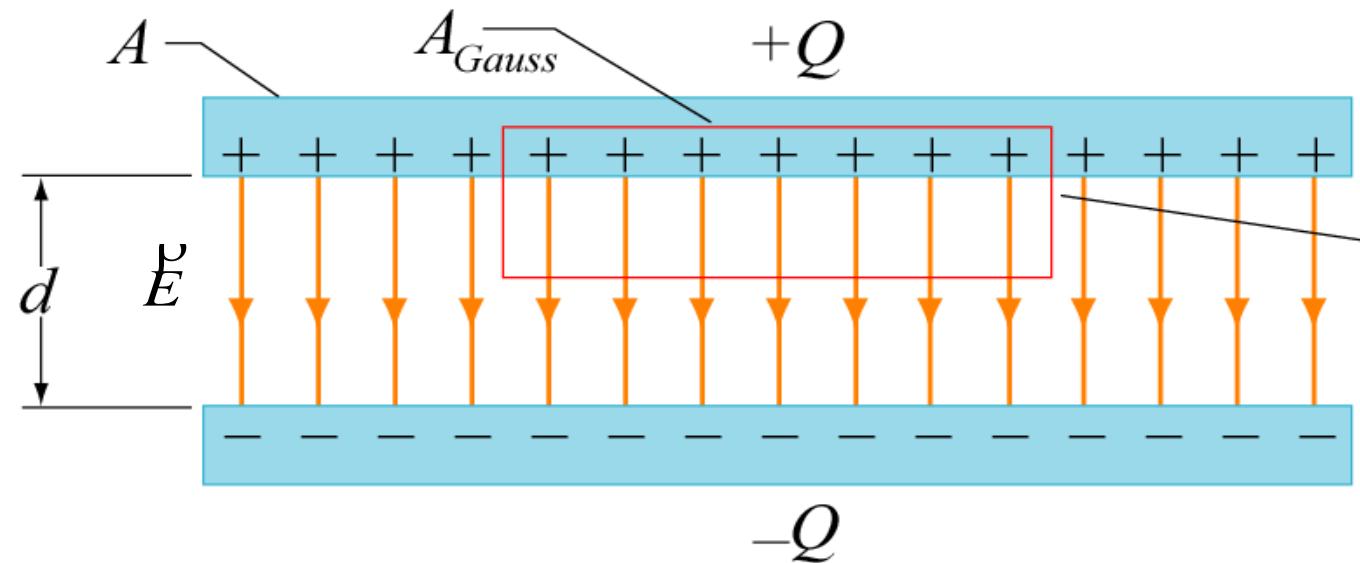
Mosfet Tab parasitic coupling



Real life examples

Flyback converter for lighting applications

Mosfet Tab parasitic coupling



$$C = \frac{\epsilon_0 A}{d}$$

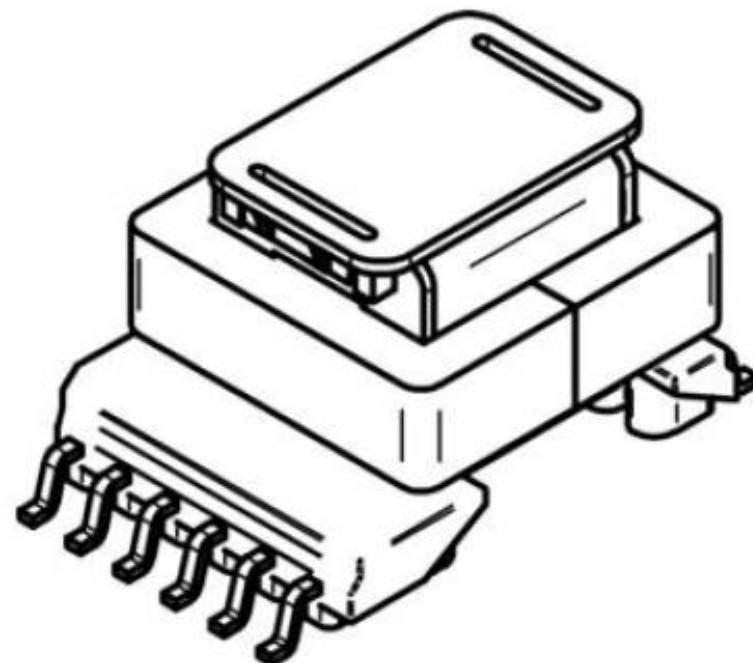
Real life examples

Flyback converter for lighting applications

Primary leakage inductance

D Electrical Properties:

Properties	Test conditions		Value	Unit	Tol.
Inductance	100 kHz/ 100 mV	L	1310	µH	±10%
Turns ratio		n	140 : 6 : 6 : 16		±3%
Saturation current	$ \Delta L / L < 20\%$	I_{sat}	0.8	A	typ.
DC Resistance 1	@ 20°C	R_{DC1}	3000.0	mΩ	max.
DC Resistance 2	@ 20°C	R_{DC2}	25.0	mΩ	max.
DC Resistance 3	@ 20°C	R_{DC3}	25.0	mΩ	max.
DC Resistance 4	@ 20°C	R_{DC4}	450.0	mΩ	max.
Leakage inductance	100 kHz/ 100 mV	L_S	40.0	µH	max.
Insulation test voltage	$W1,4 \Rightarrow W2,3$	U_T	4000	V (AC)	



WE-UOST

Real life examples

Turn ratio to inductance ?



Transformers : from datasheet to LTSpice model

Primary inductance

1310 μH

Lp

Leakage inductance

50 μH

L1

Primary	Secondary	Aux
130	6	16

Secondary inductance

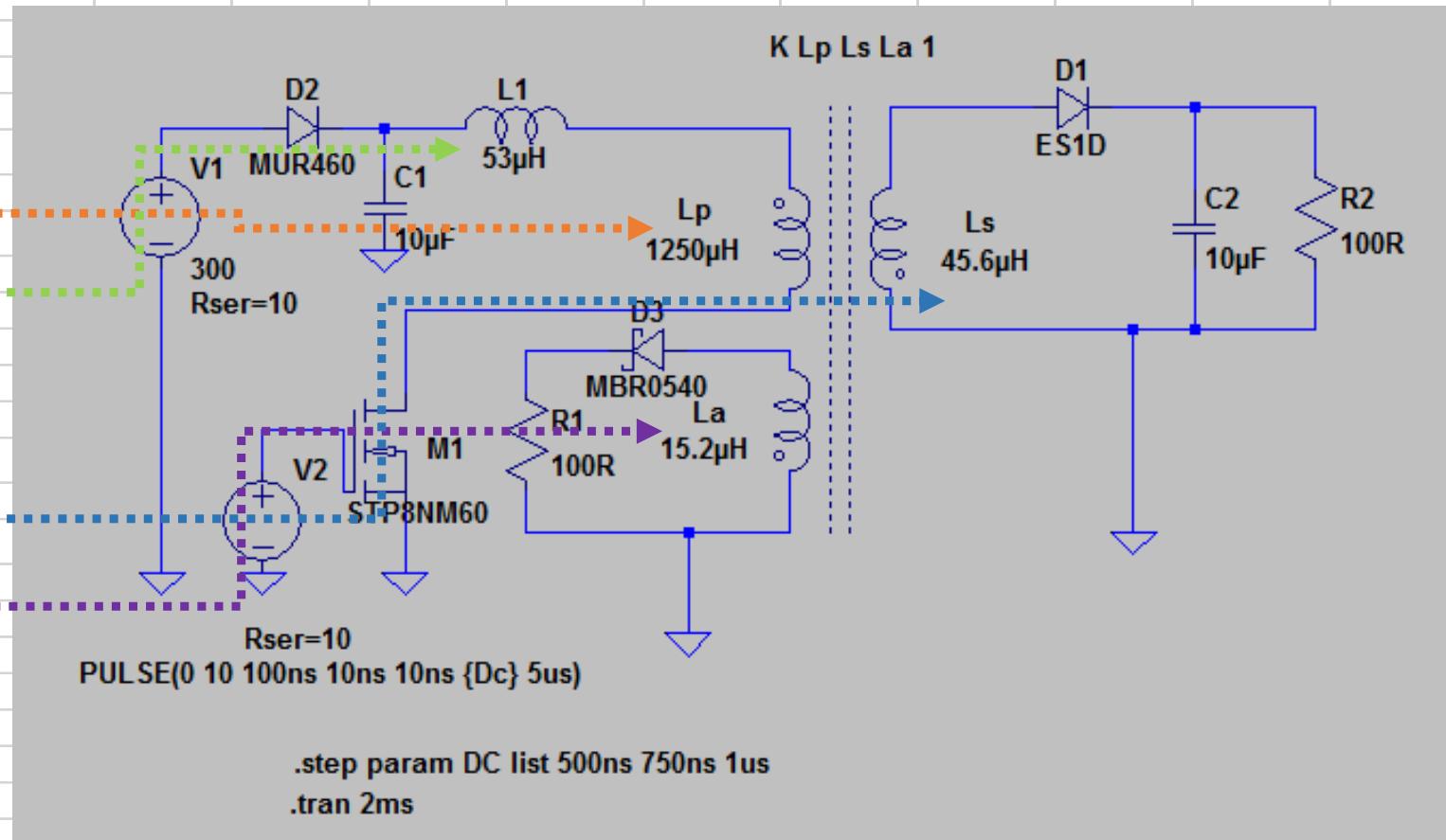
2.79 μH

Ls

Auxiliary inductance

19.84 μH

La

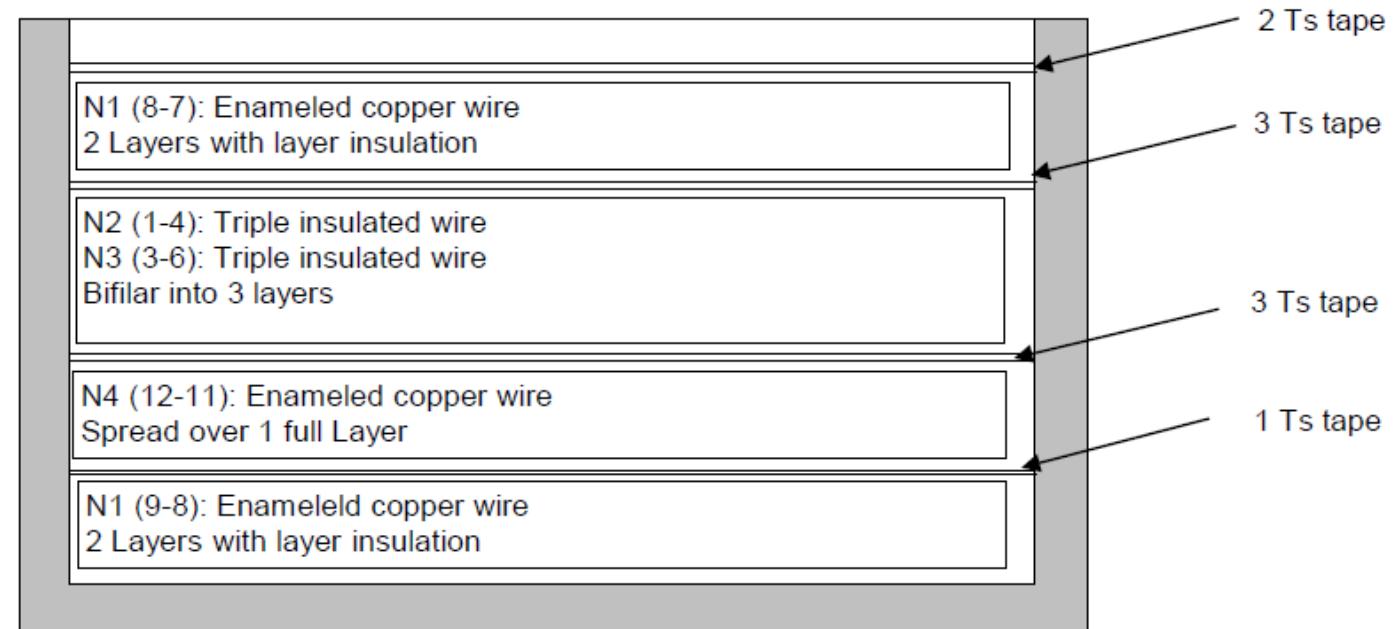
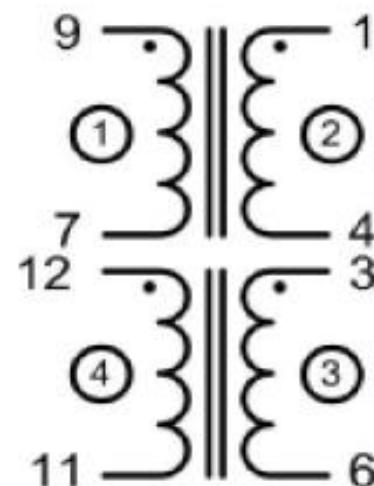


Real life examples

Flyback converter for lighting applications

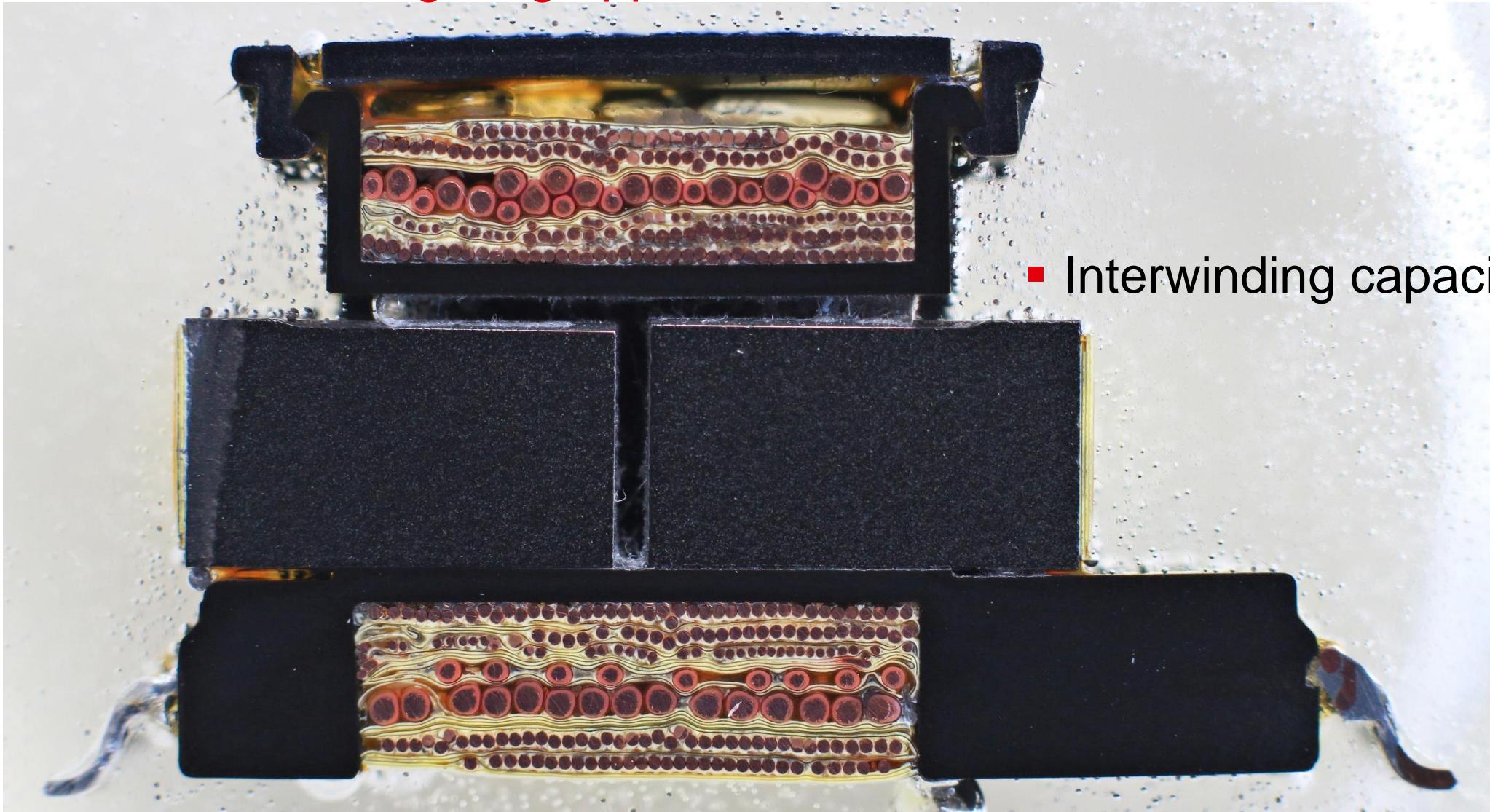


■ Interwinding capacitance ?



Real life examples

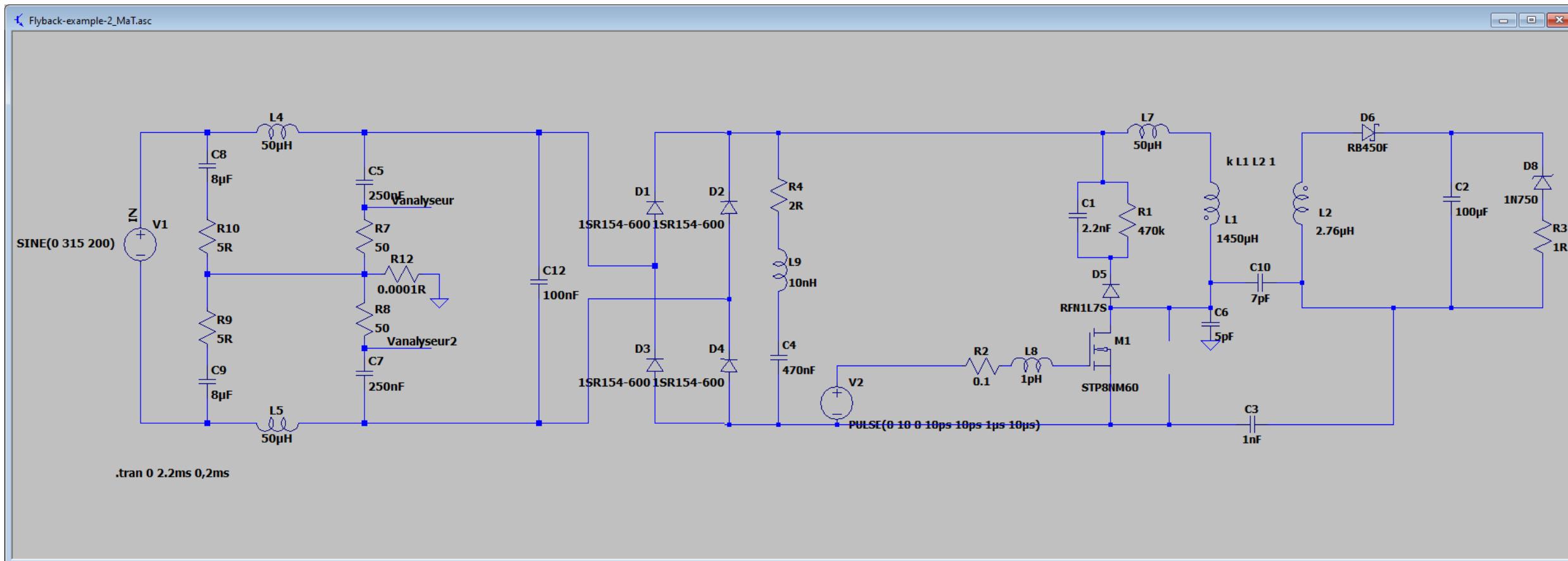
Flyback converter for lighting applications



- Interwinding capacitance ?

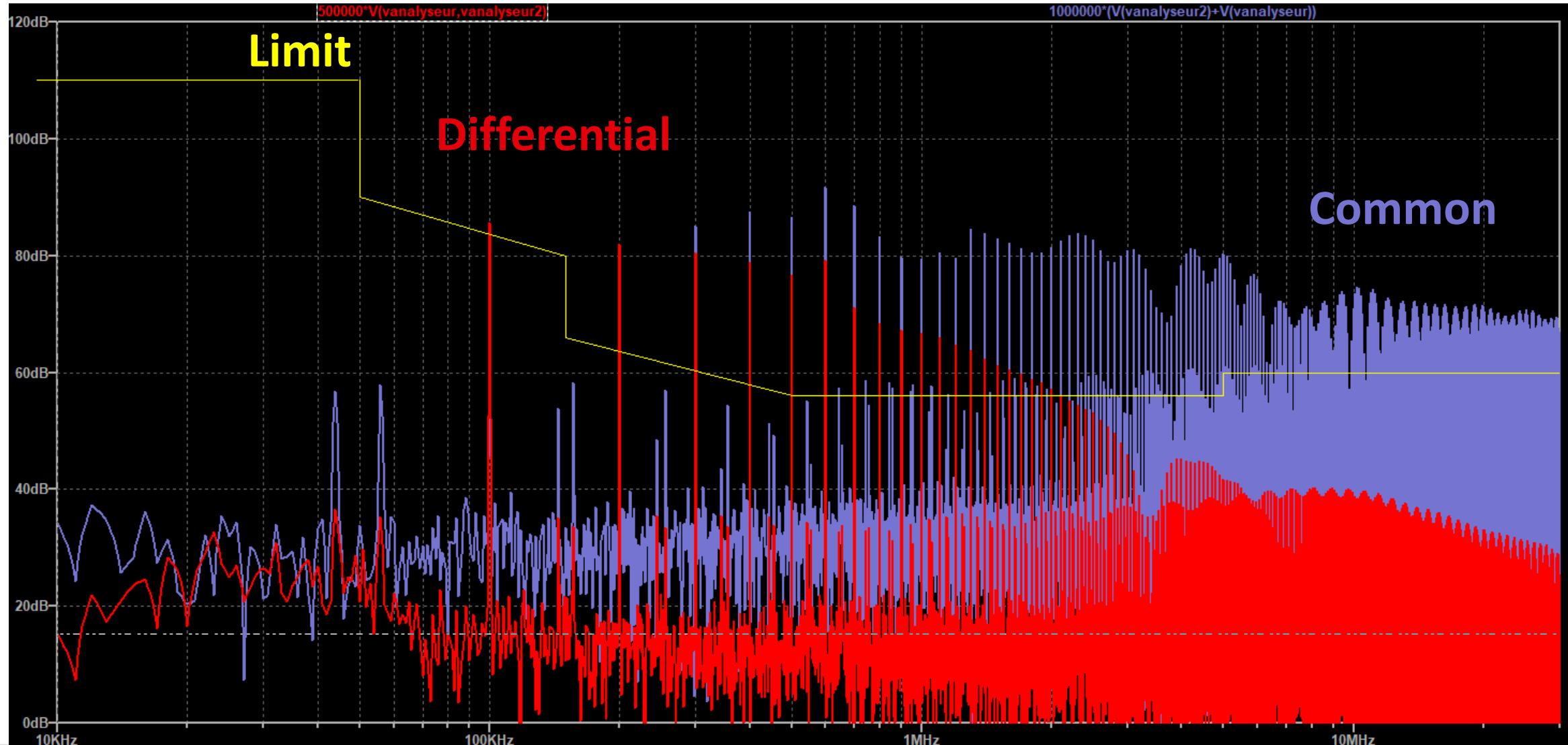
Real life examples

Flyback converter for lighting applications



Real life examples

Flyback converter for lighting applications

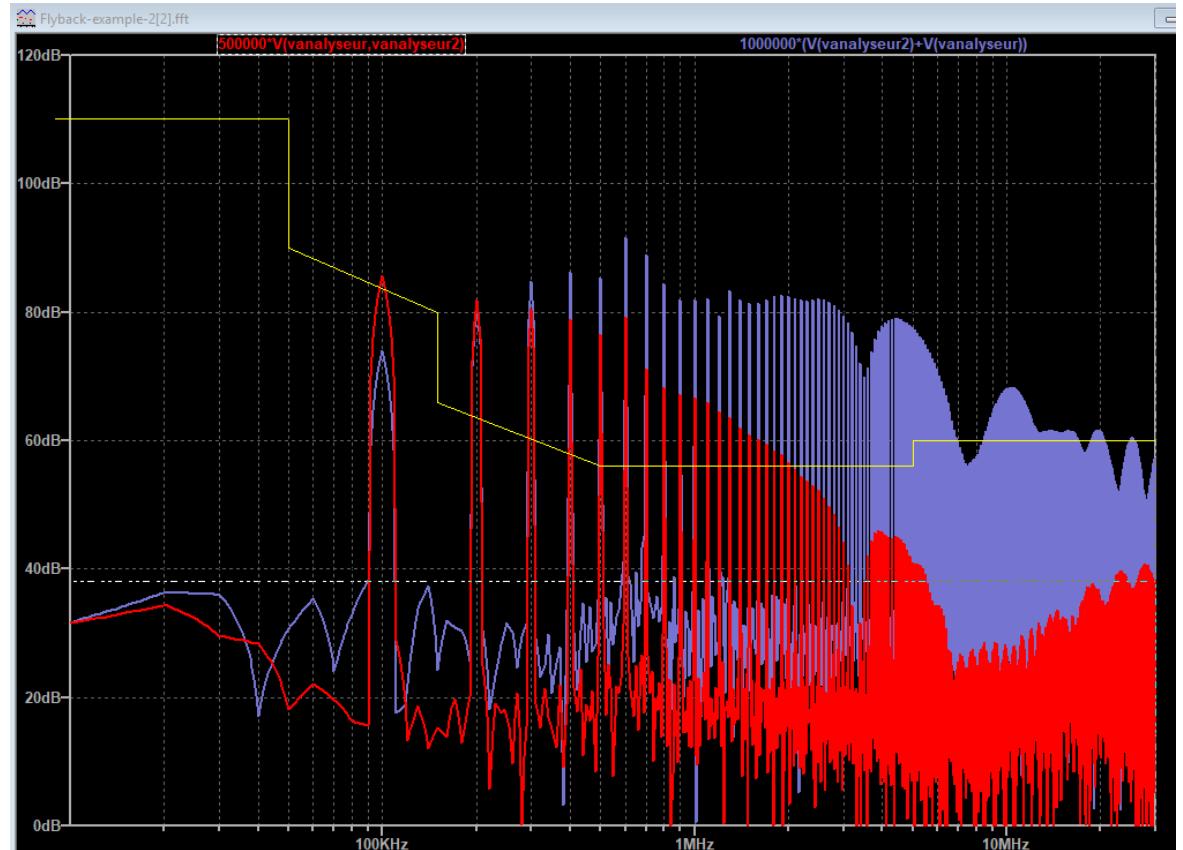


Real life examples

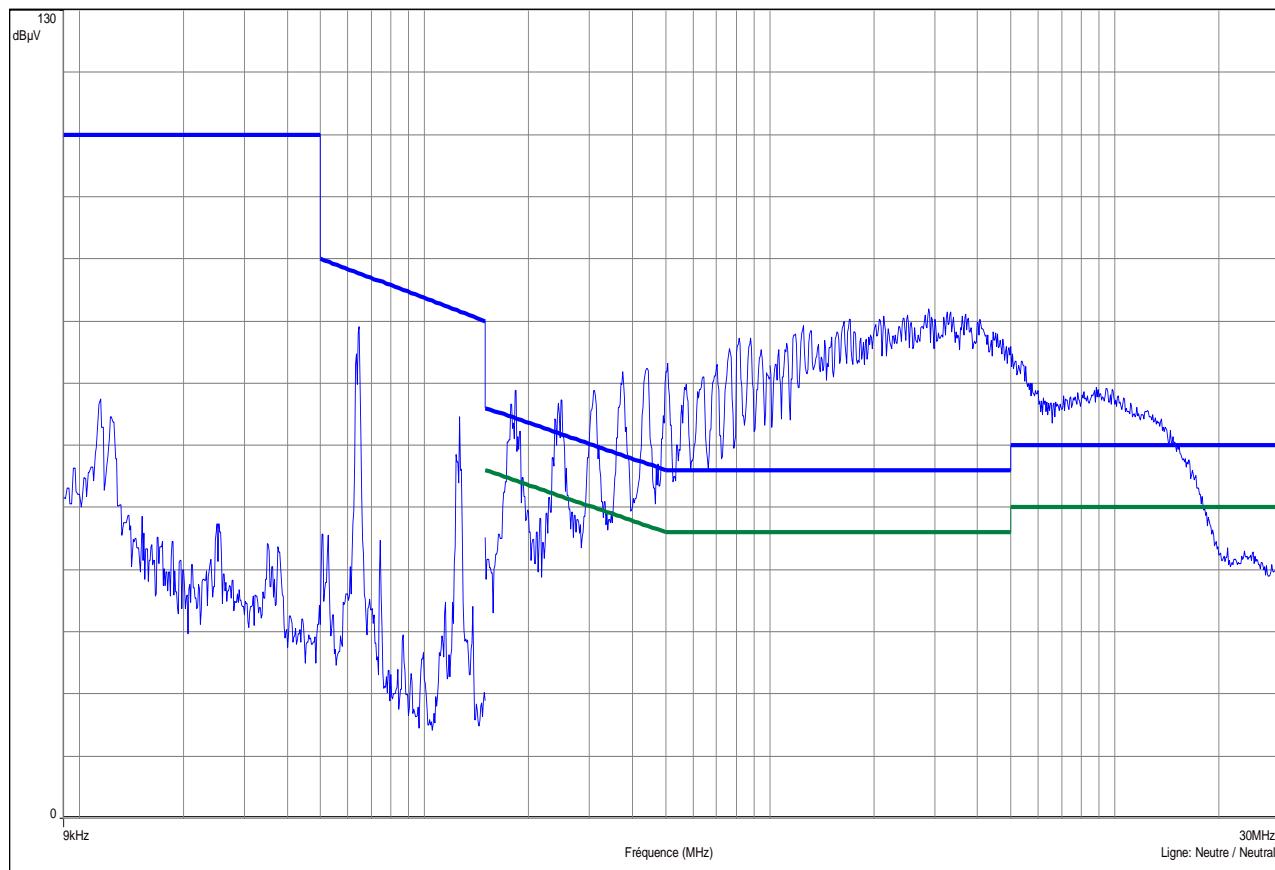
Flyback converter for lighting applications



Simulation



Example of actual measurement



Real life examples

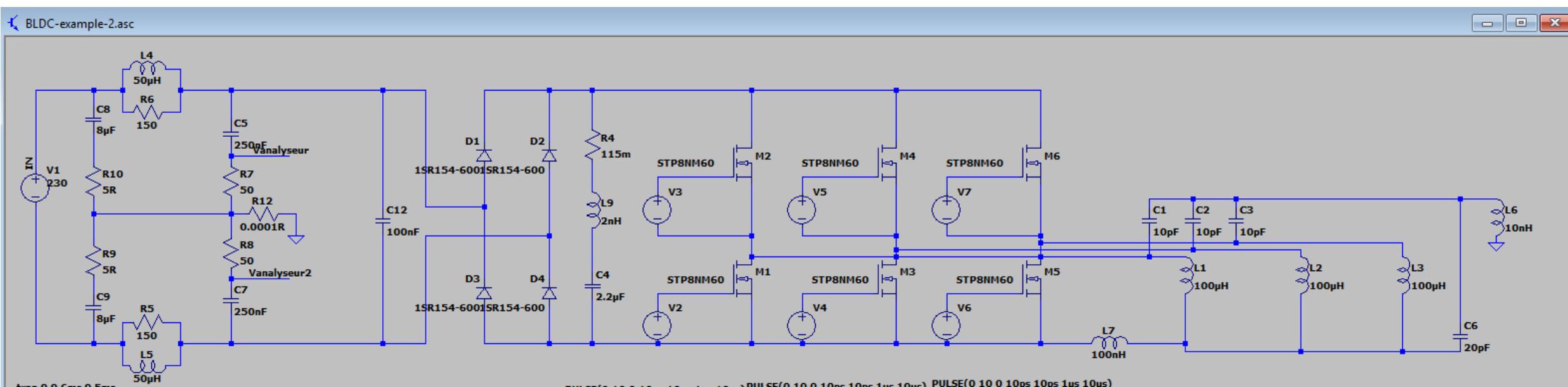
Mains voltage BLDC driver + motor



Real life examples

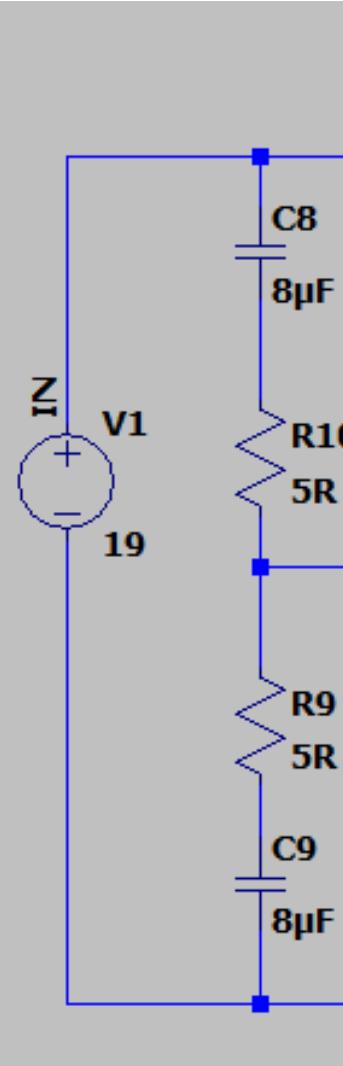
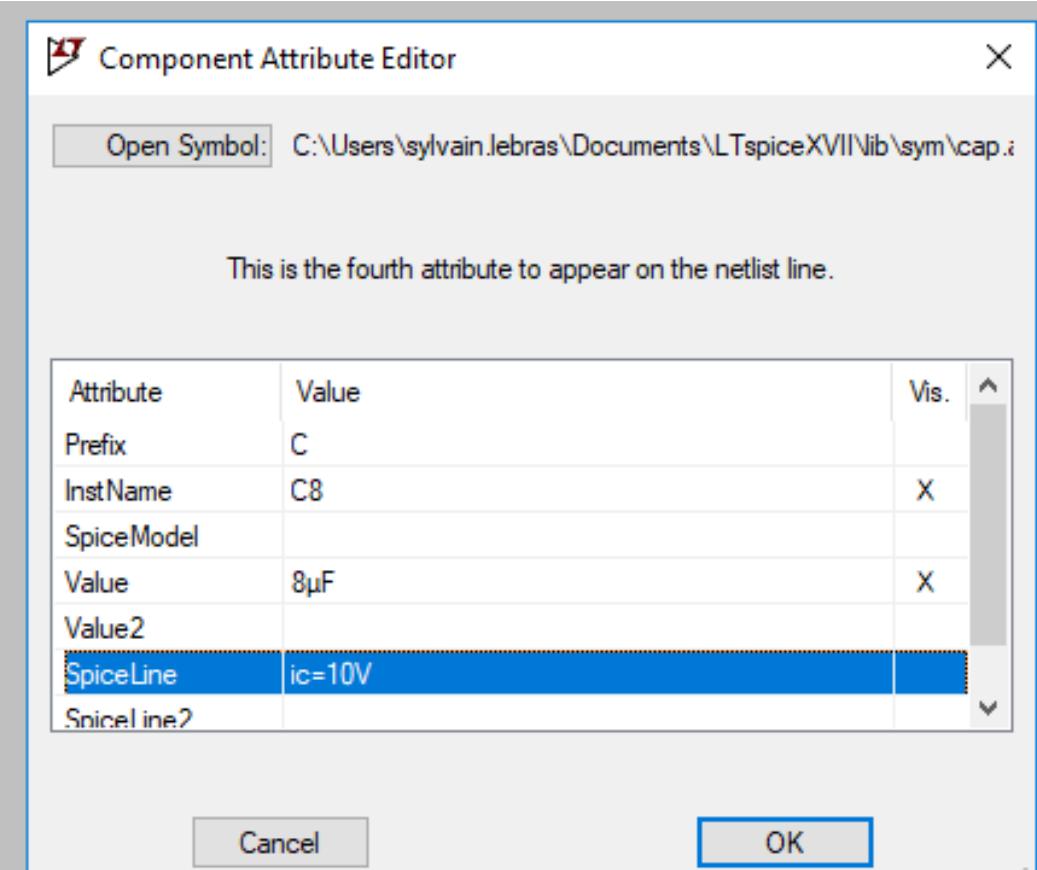
Mains voltage BLDC driver + motor

- Parasitic coupling to and through stator
- Influence of grounding
- Slew rate of driver
- Dead time impact



Good to know

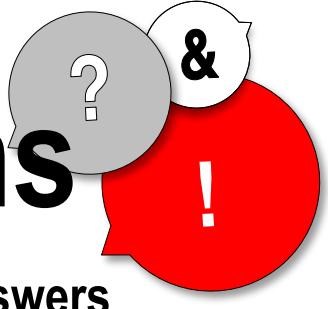
Speed up simulations



Setting initial condition

- Ctrl + Right Click
- SpiceLine
 - $ic=10V$

Questions & Answers



We are here for you now!
Ask us directly via our chat or via E-Mail.



eiSos-webinar@we-online.com
Sylvain.LeBras@we-online.com