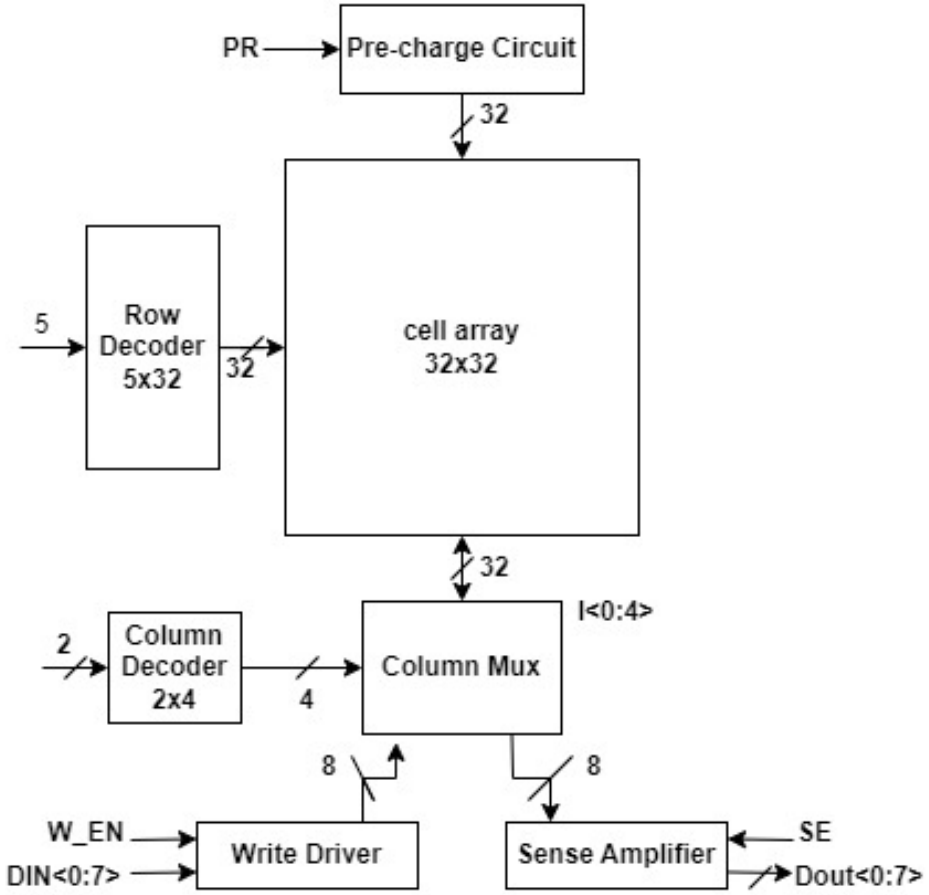
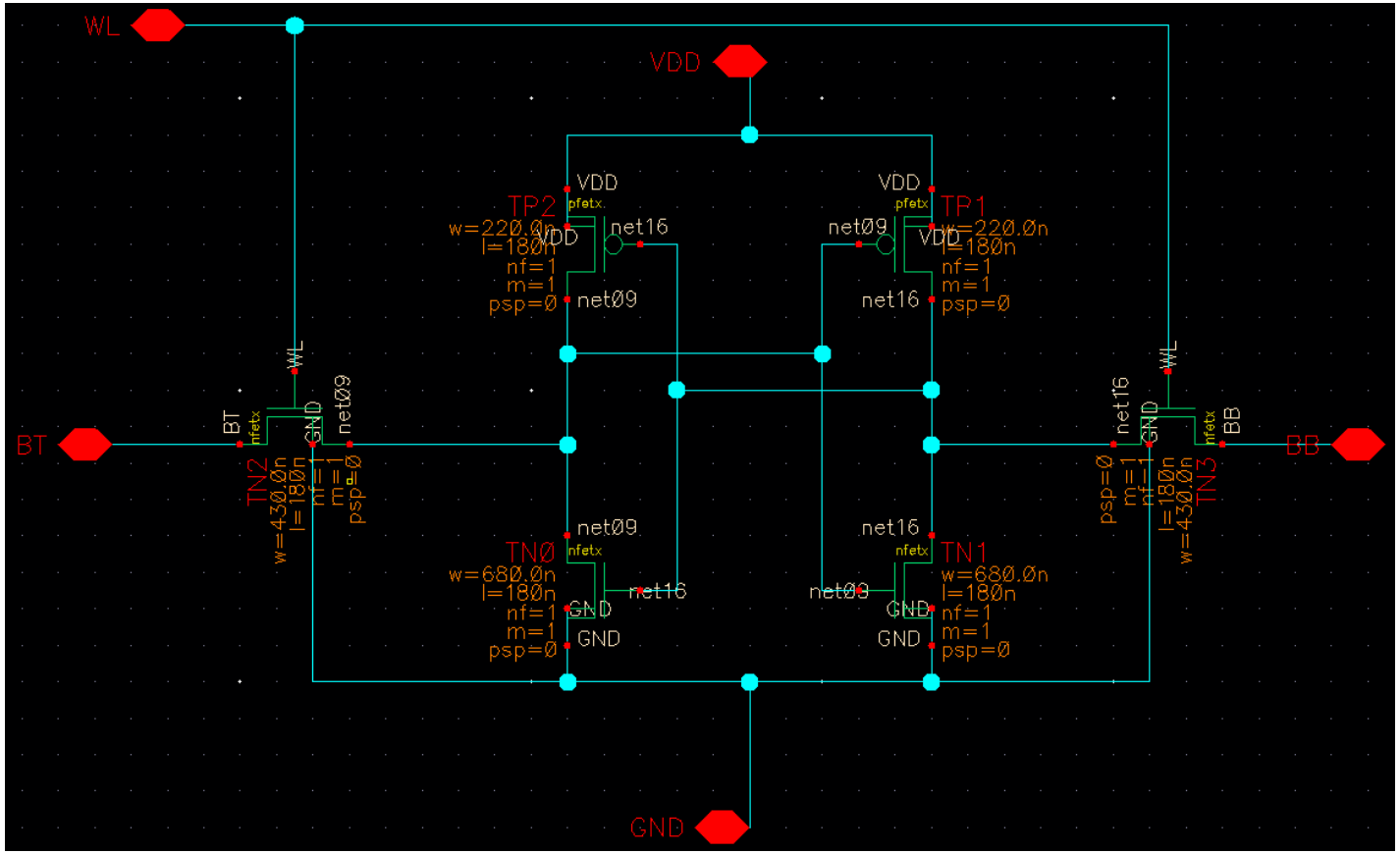
6T-SRAM DESIGN

Block Diagram of 1Kb SRAM Cell



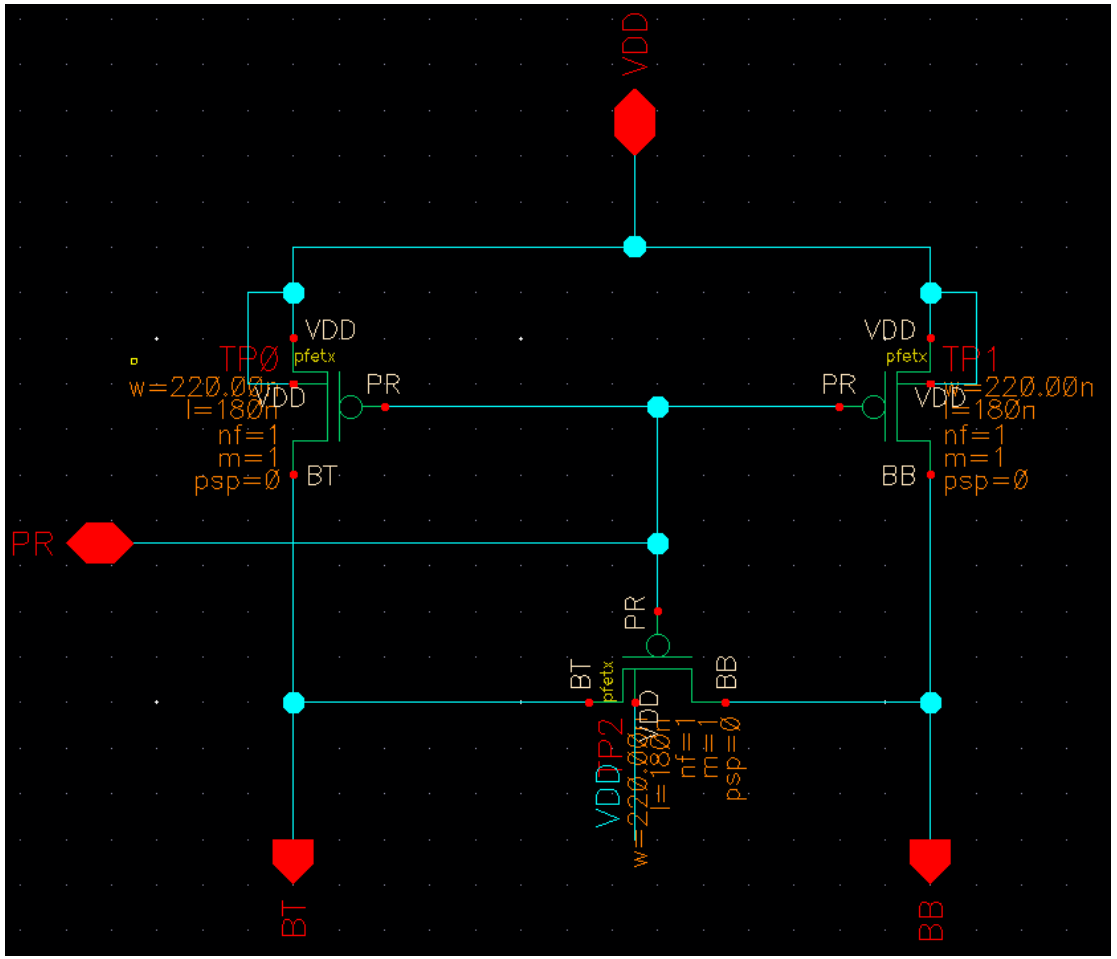
- Block diagram of 1Kb SRAM array consists of SRAM cell, write driver circuit, precharge circuit, sense amplifier ,row and column decoder.
- Since the memory core trade performance and reliability in reduction area, memory design relies exceedingly on the peripheral circuitry to recover both speed and electrical integrity
- For fast read and write operation separate write driver circuit and sense amplifier dedicated to each column.



6T-SRAM Cell

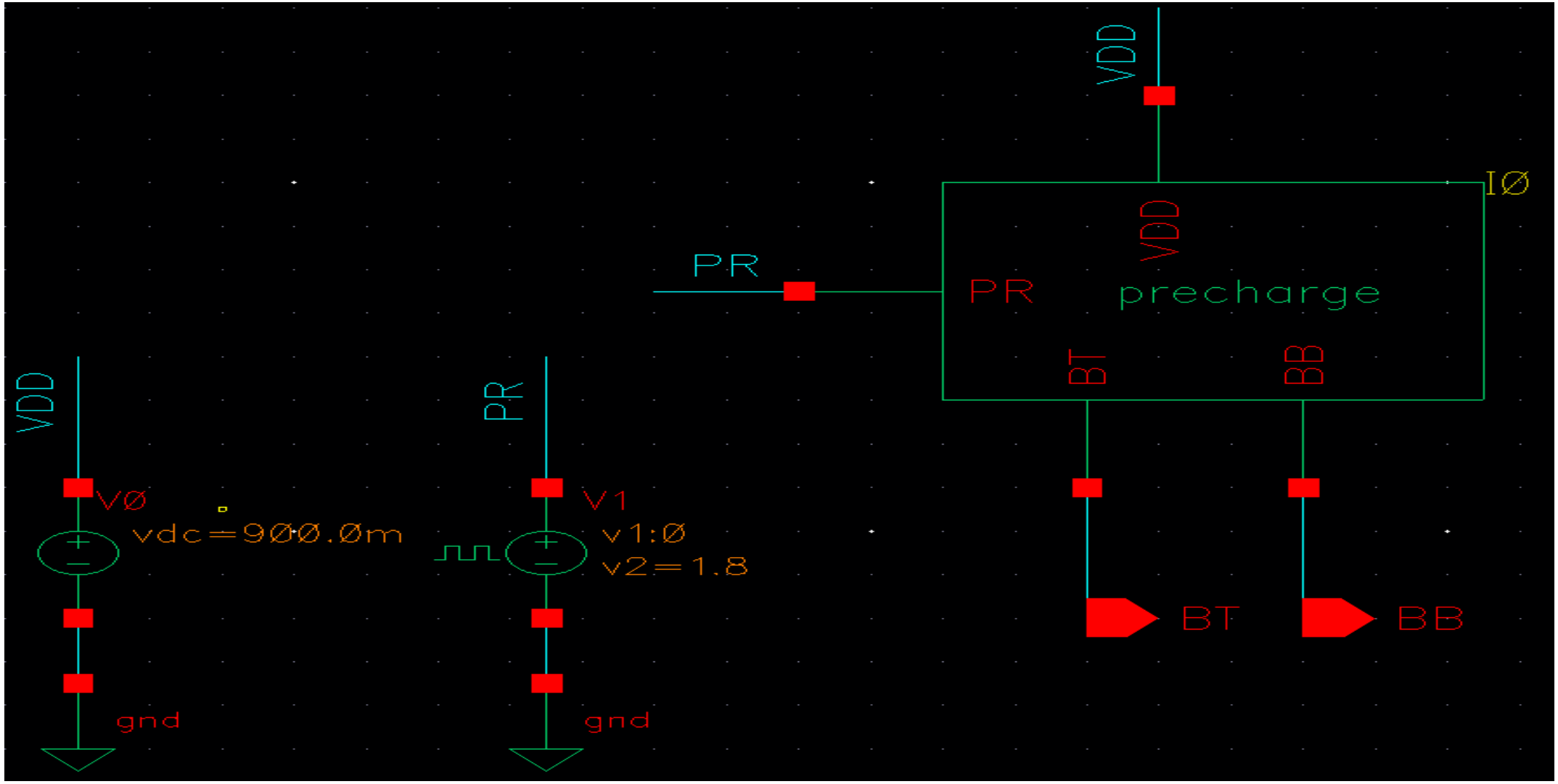
For the faster write operation, PMOS PM1 needs to be weaker than the access transistor NM1.
For faster read from the cell the driver NM3 must be stronger than the access transistor NM1
Use of wider access transistors helps for faster current flow during read/write access.
(W/L)pull-up < (W/L)access << (W/L) pull-down

Pre-charge Circuit

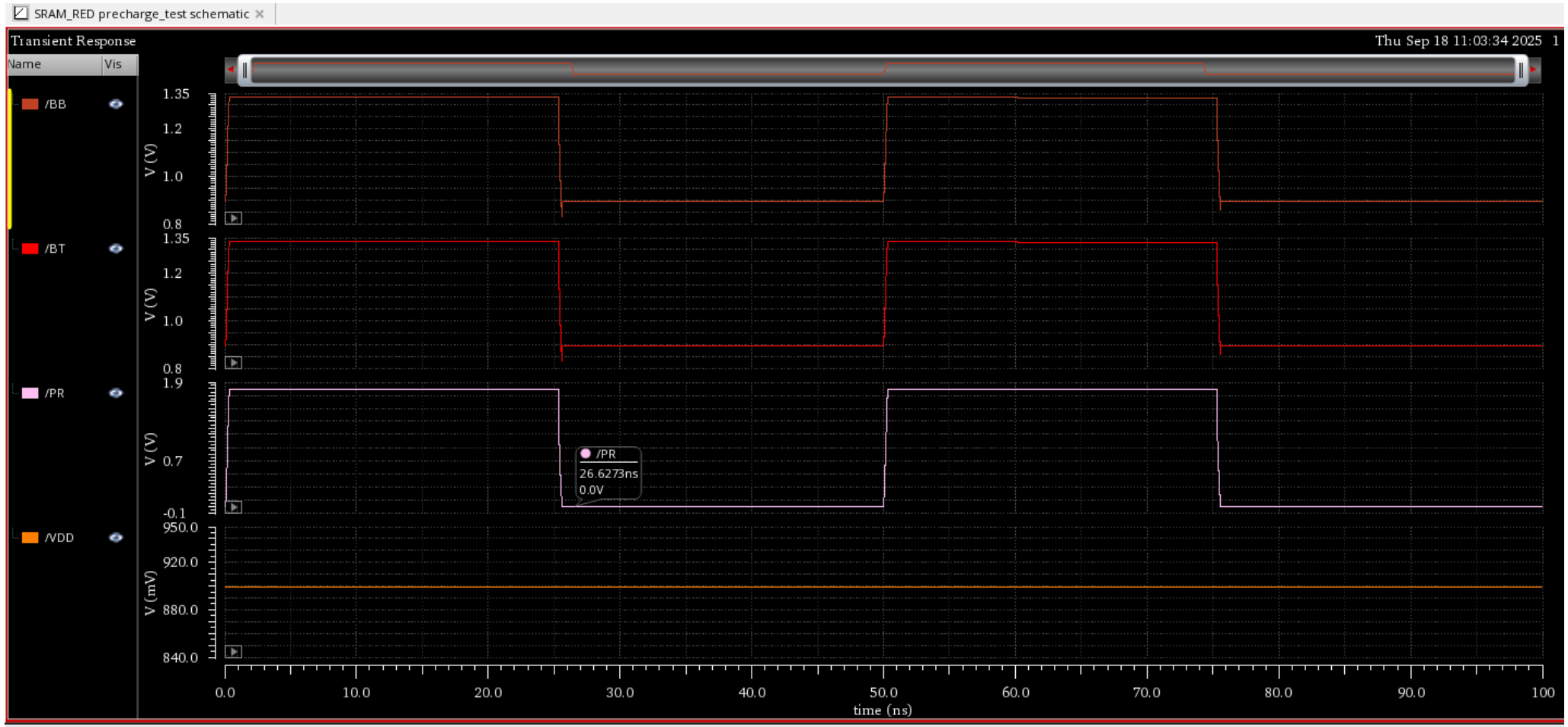


- The pre-charge circuit is one of the vital components that is constantly utilized within the SRAM cell.
- This circuit is used to charge the bit line and bit line bar to supply voltage VDD and pre-charging operation should perform before every write and read operation.
- Transistors M1 and M0 will precharge the bit lines while transistor M2 will equalize them to ensure that both the bit lines within a pair are at the same potential before the cell is read.
- As bit lines have high capacitance, precharge circuit needs to provide large current to bit lines to get charged quickly.

Pre-charge Circuit Simulation Test Bench



Simulation result of Pre-charge

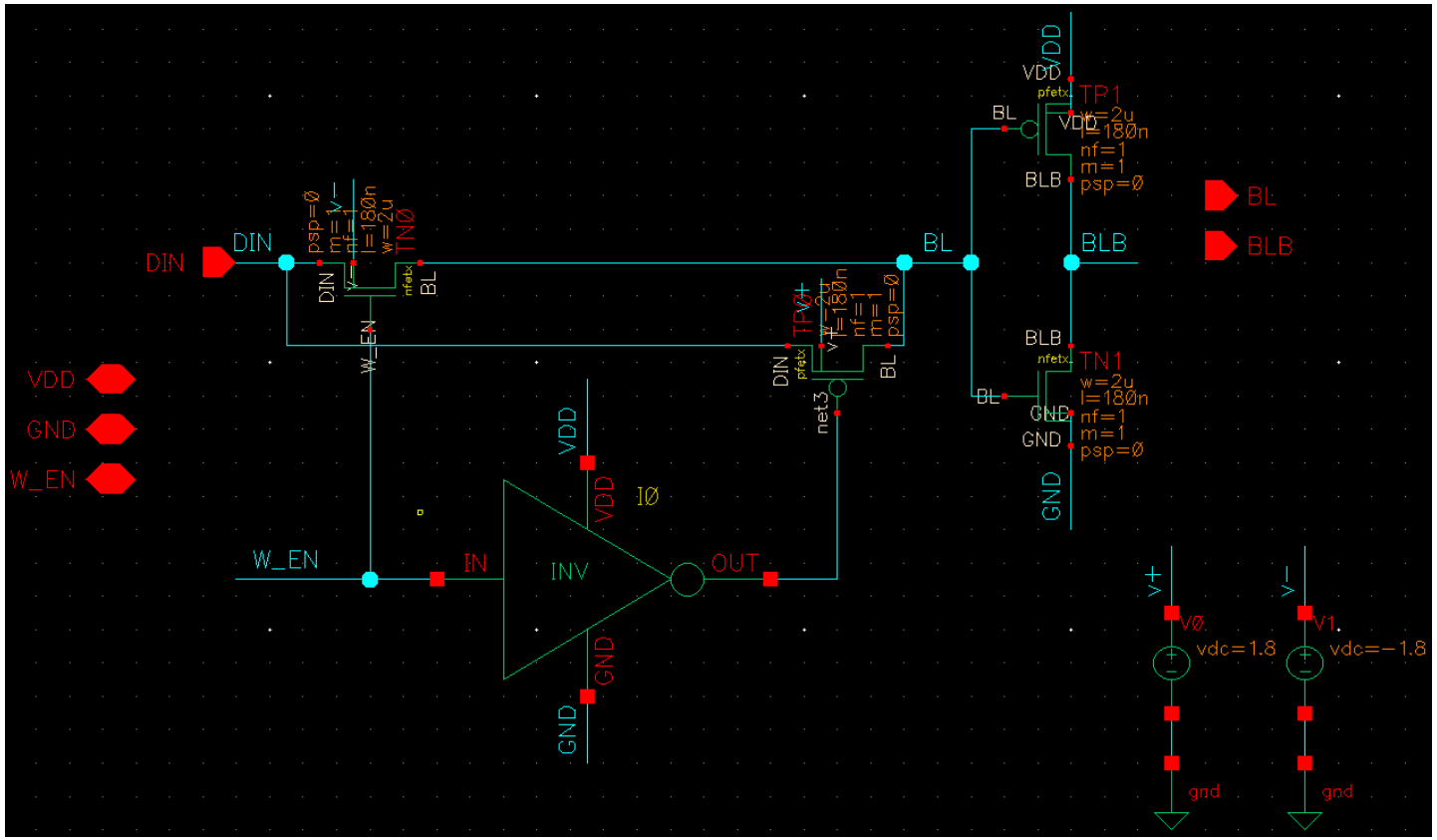


Design and implementation of Write Driver:

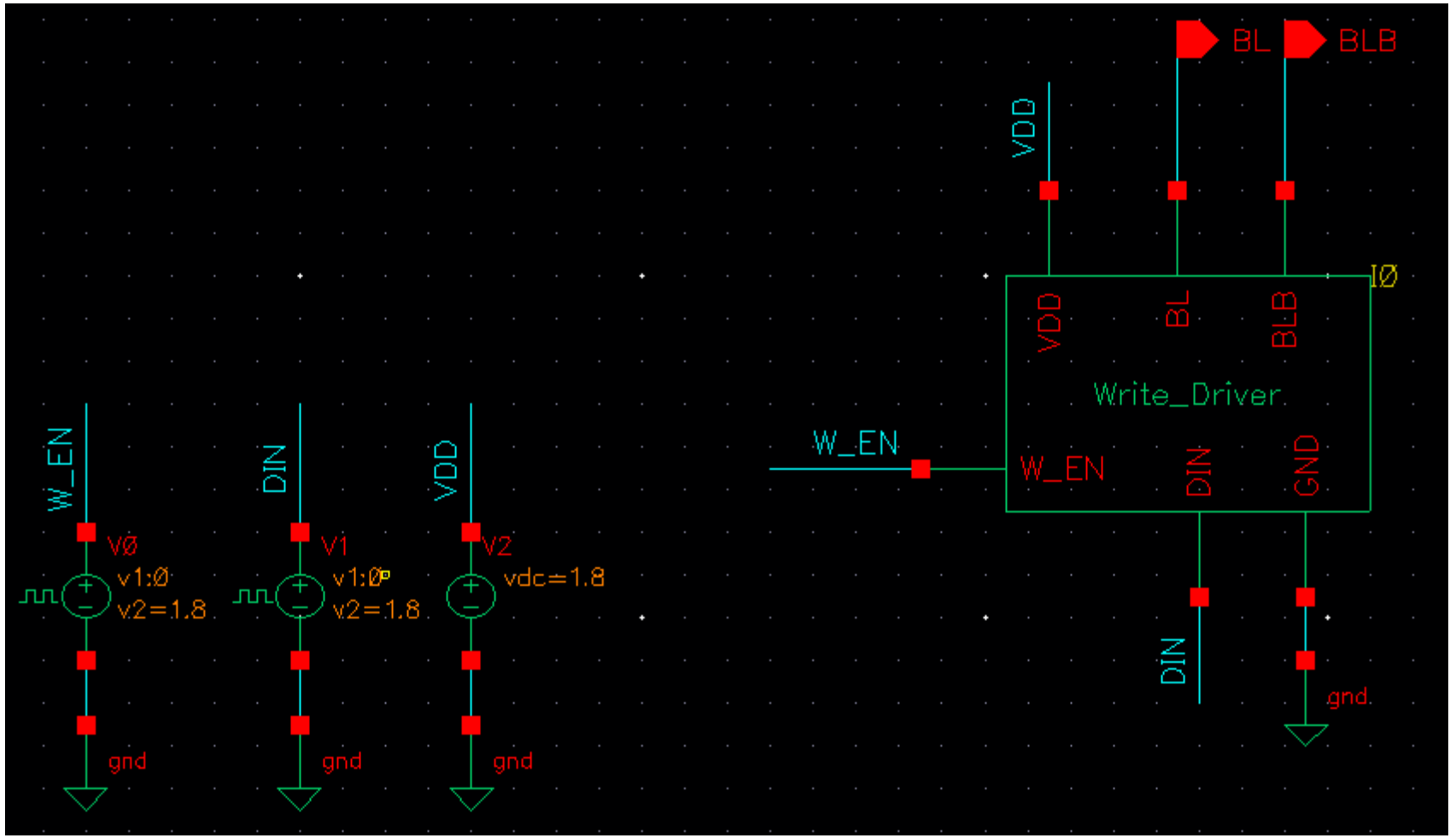
When the write enable signal (WE) is high, the input data (DATA) is written onto the bitlines (BL and BLB) using two pass transistors (NM1 and NM2).

If DATA is high, BL is pulled high and BLB is pulled low, and vice-versa if DATA is low.

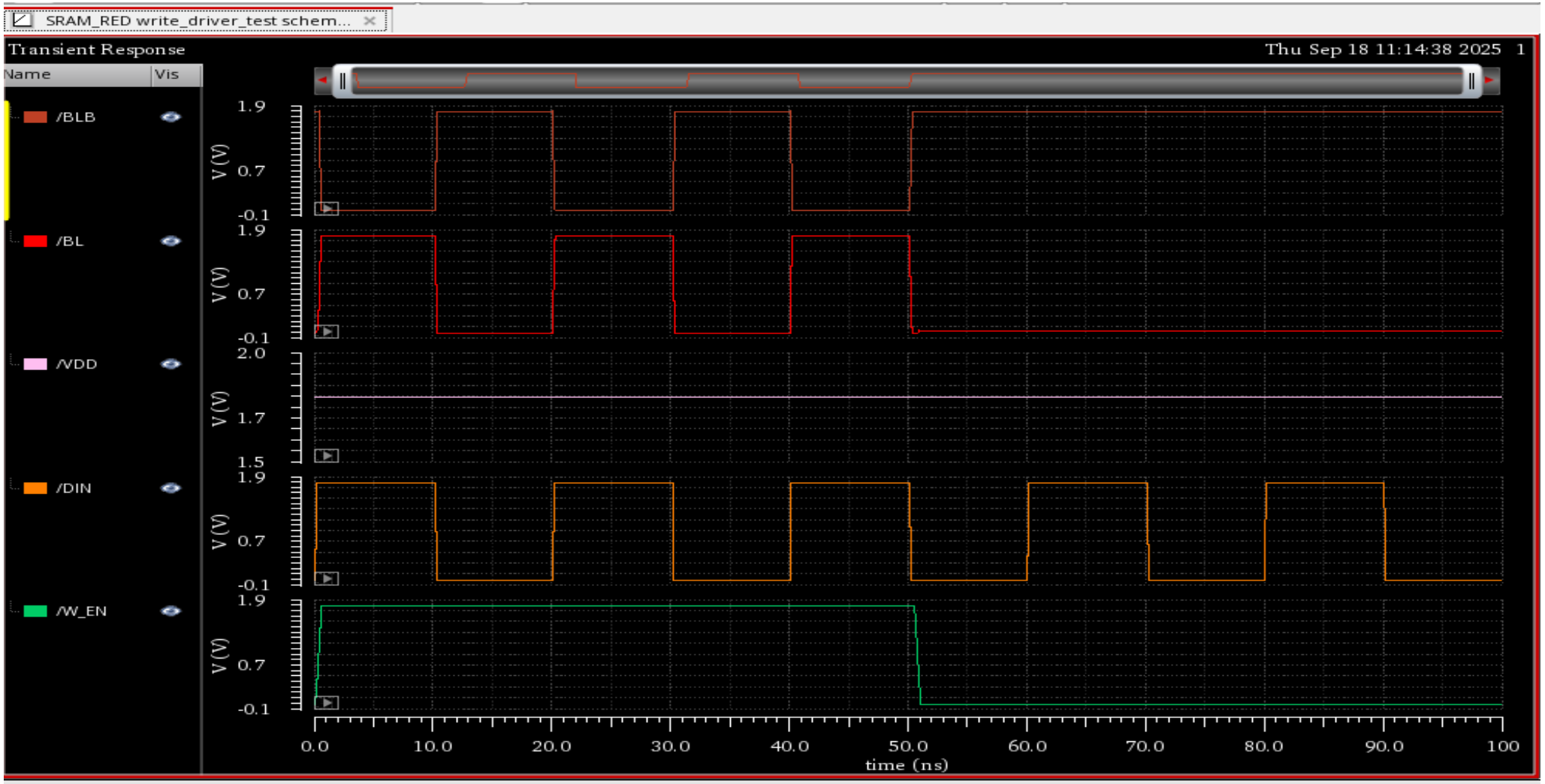
This written data is then stored in the corresponding SRAM cell connected to the activated bitlines.



Write Driver Test Bench



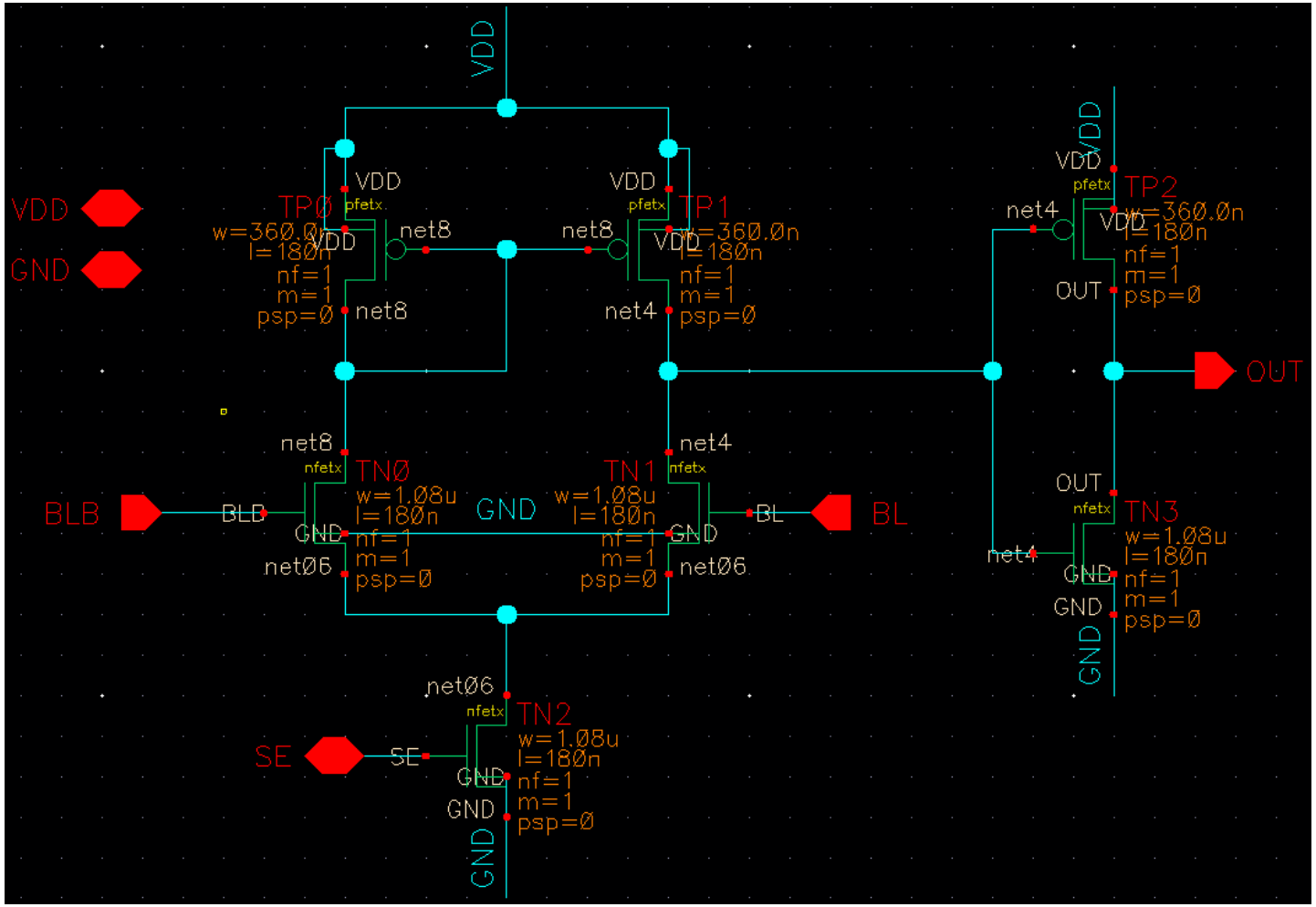
Write Driver Simulation Result



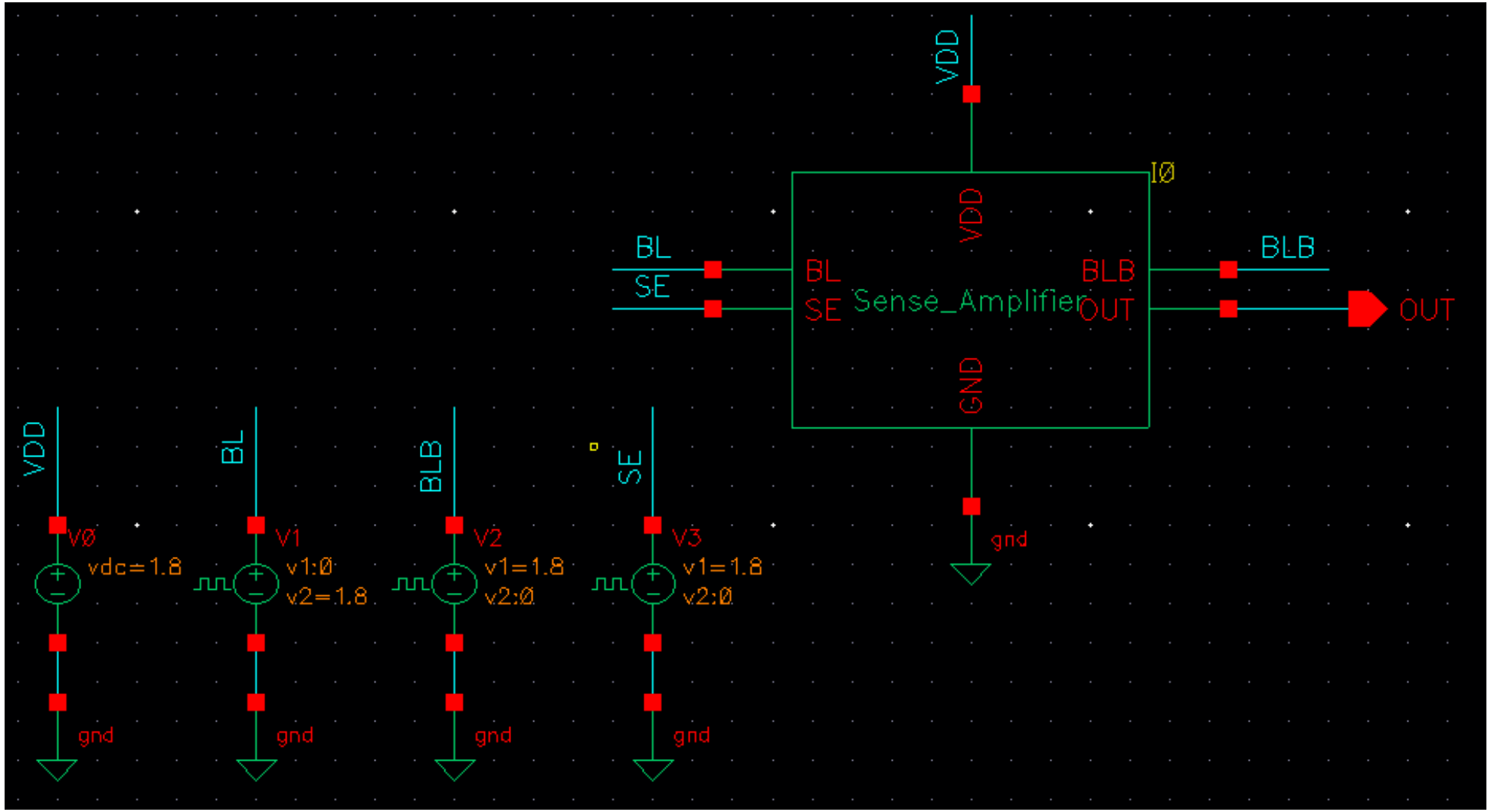
Schematic Representation of Sense Amplifier:

Sense amplifiers are used in the memories to speed up the read operation.
Sense amplifier takes the small signal difference bit line voltage as input and gives full swing single ended output.

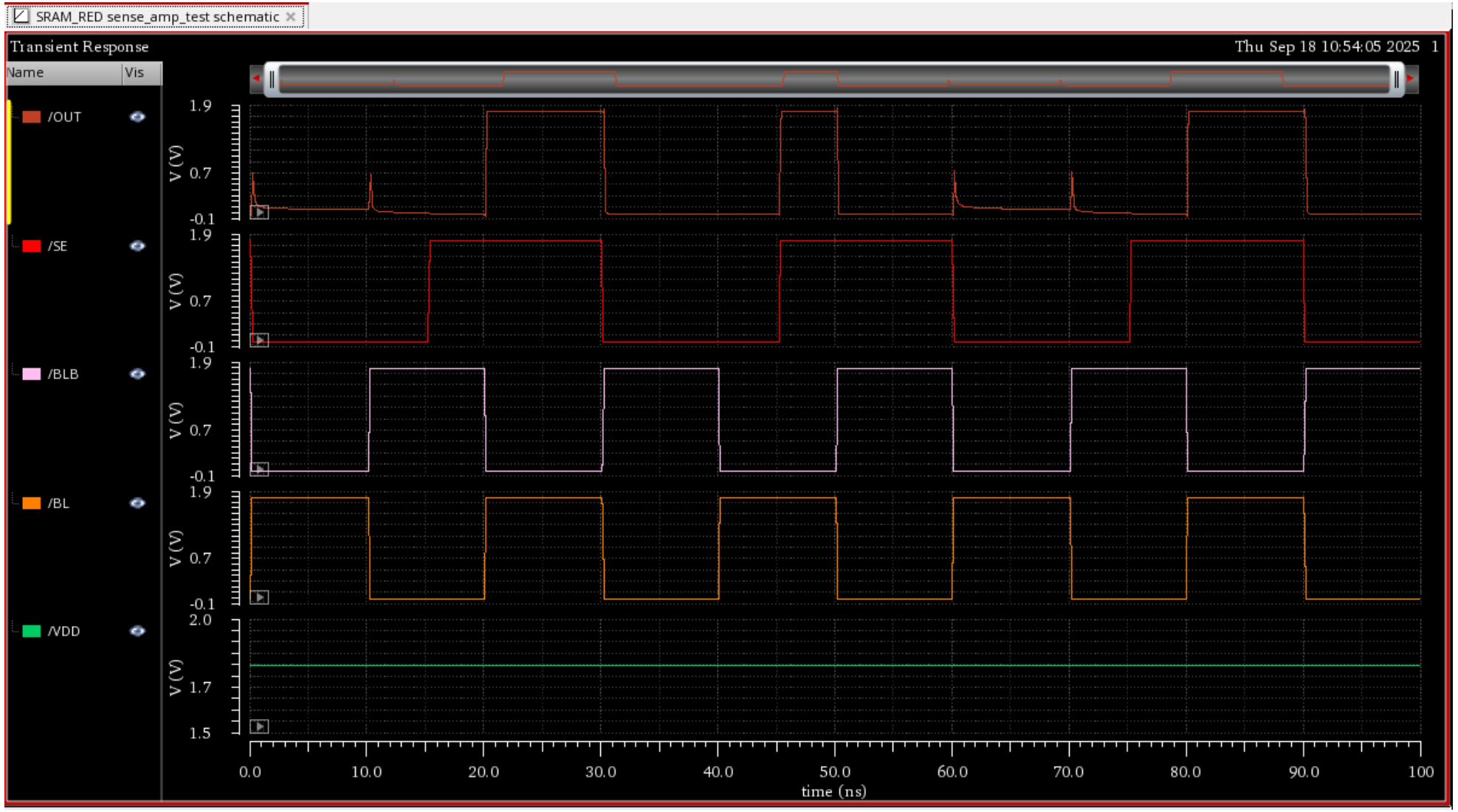
Access time and power consumption of memory is affected by the sense amplifier hence the performance of memory is improved by reducing both sensing delay and power dissipation.



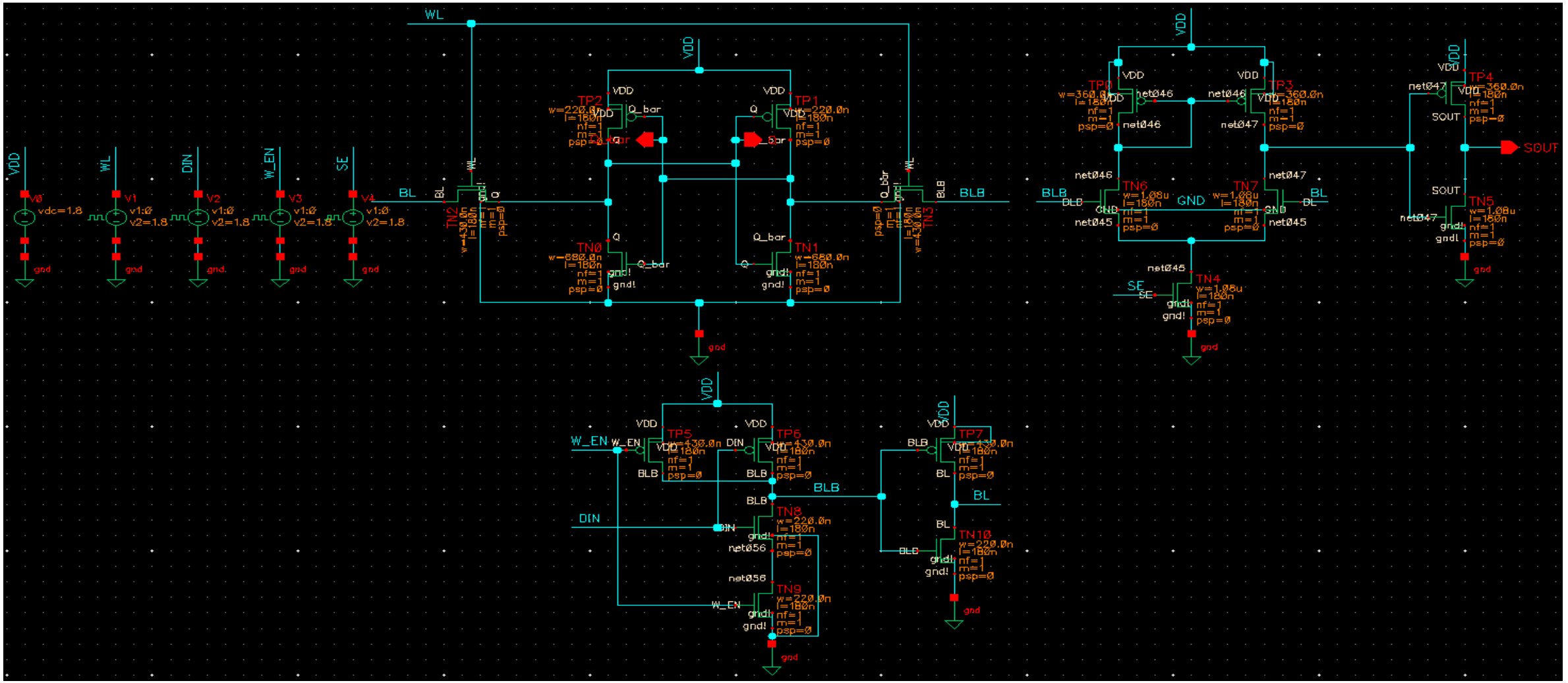
Sense Amplifier Test Bench



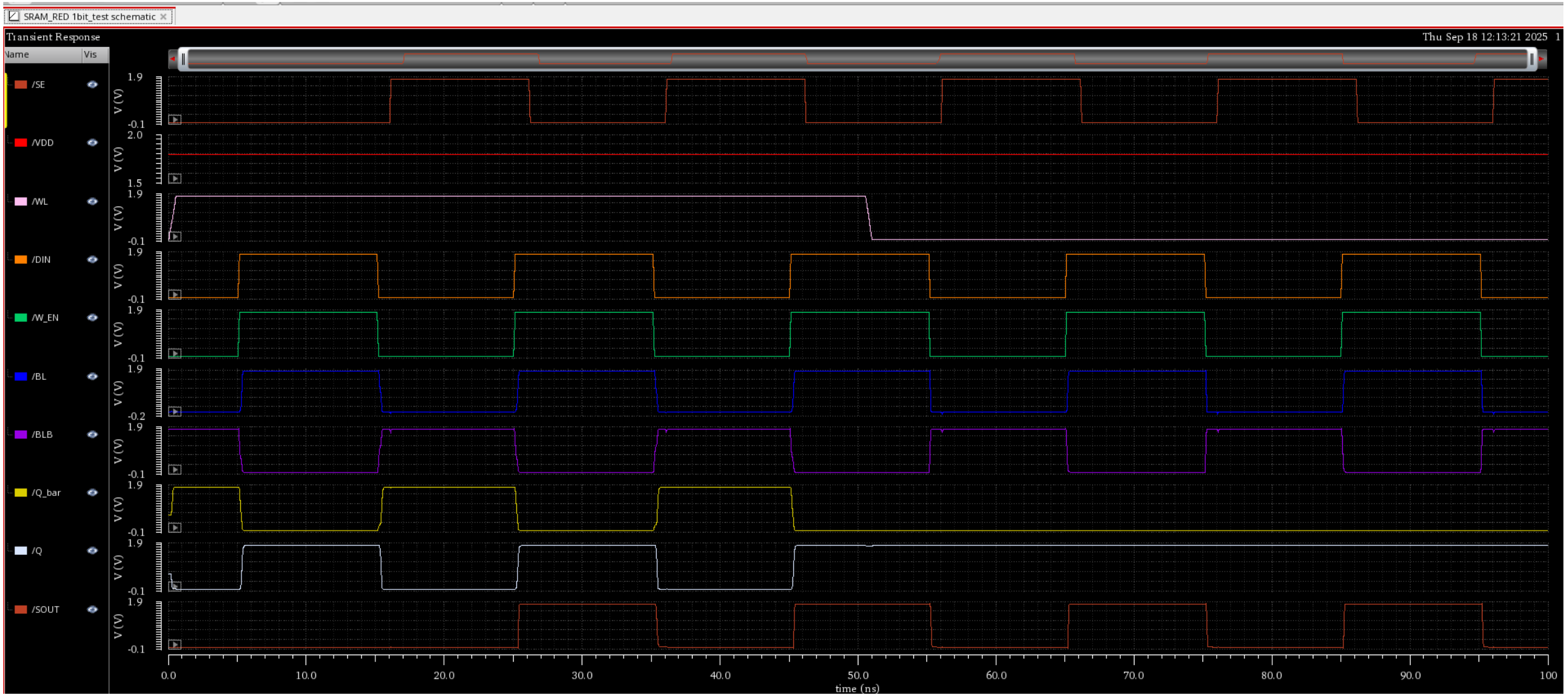
Simulation result of Sense Amplifier



Design and implementation of 1 bit SRAM cell



Simulation result of 1 bit SRAM cell



Design of Row Decoder, Column Decoder and Column MUX

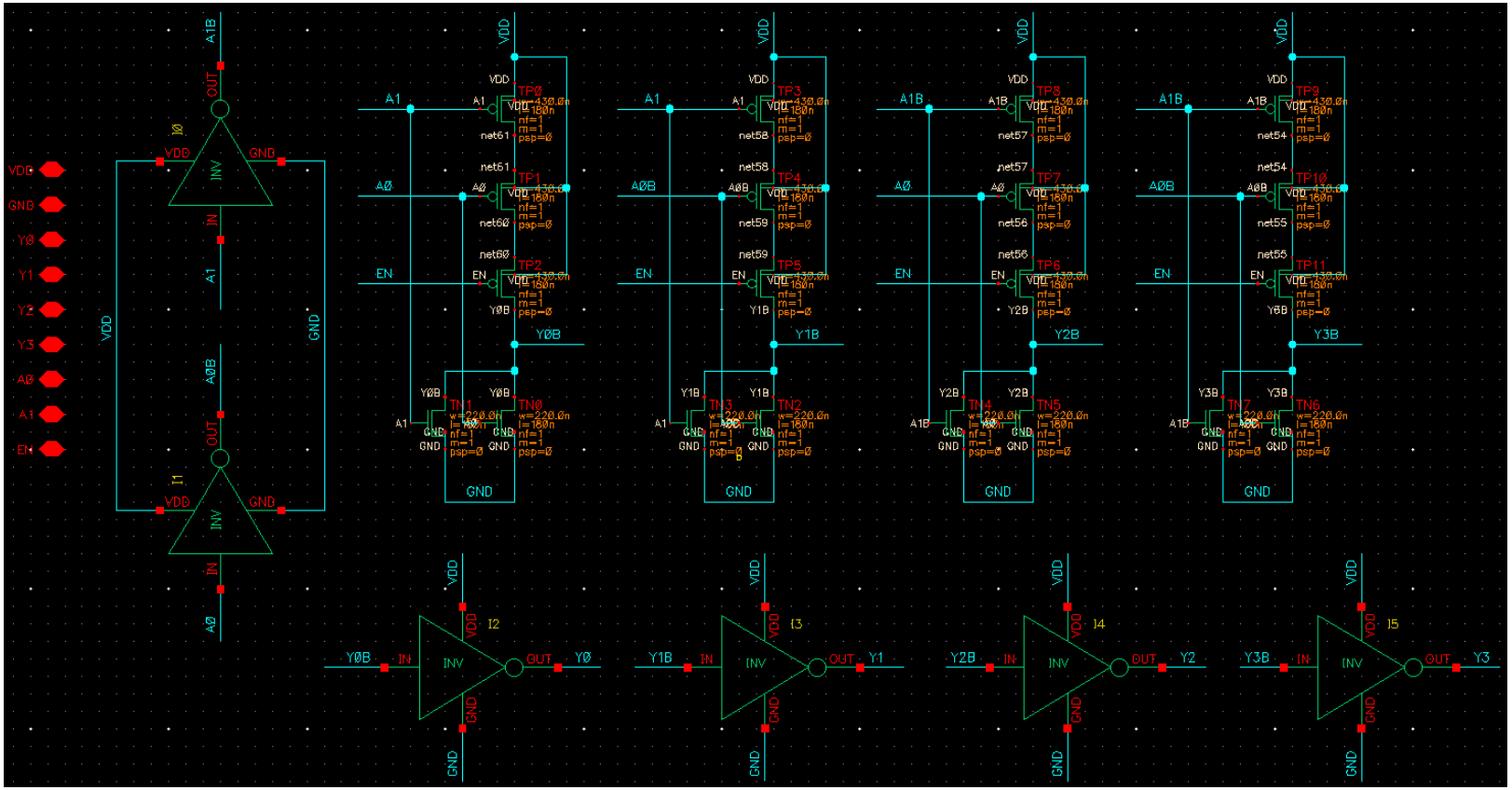
Row decoder, Column Decoder and Column MUX these three components work together to enable efficient and accurate access to the data stored in the SRAM. Without them, it would be difficult to address and retrieve specific data elements from the vast array of memory cells.

Addressing: The row and column decoders ensure that the correct cell is selected for reading or writing.

Data Transfer: The column MUX ensures that the data from the selected columns is properly routed to the output, enabling the transfer of multiple bits of data in parallel.

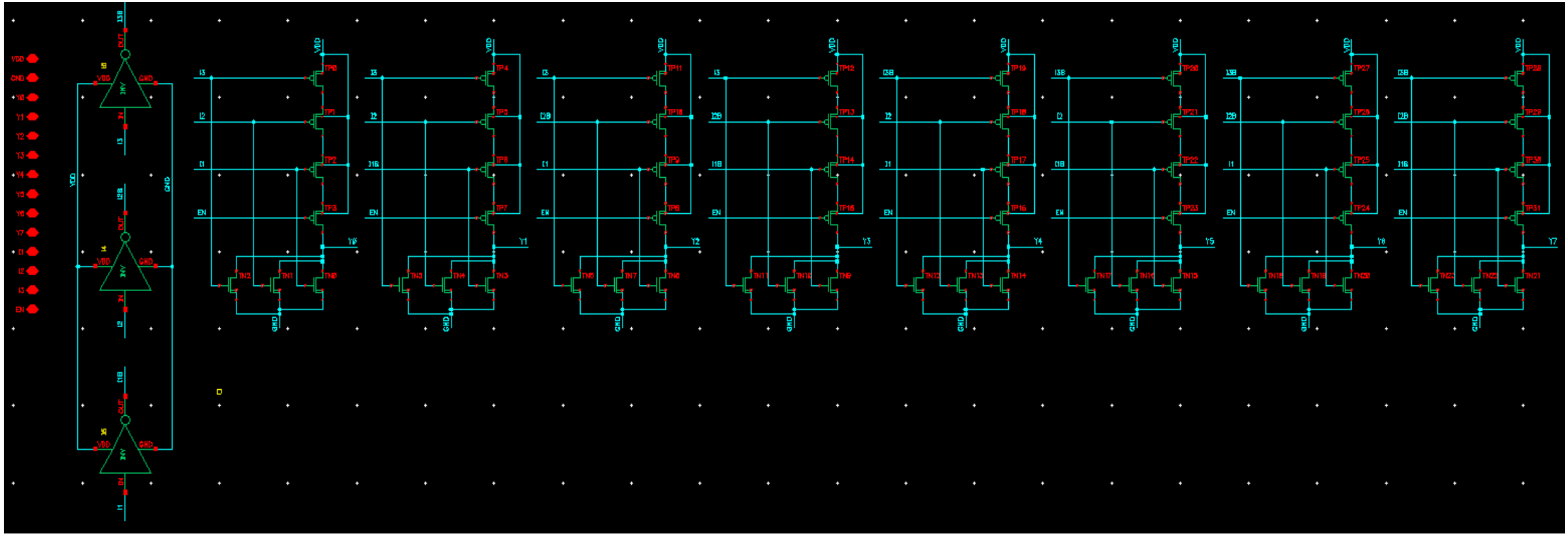
Row Decoder:

Schematic Representation of 2-4 decoder

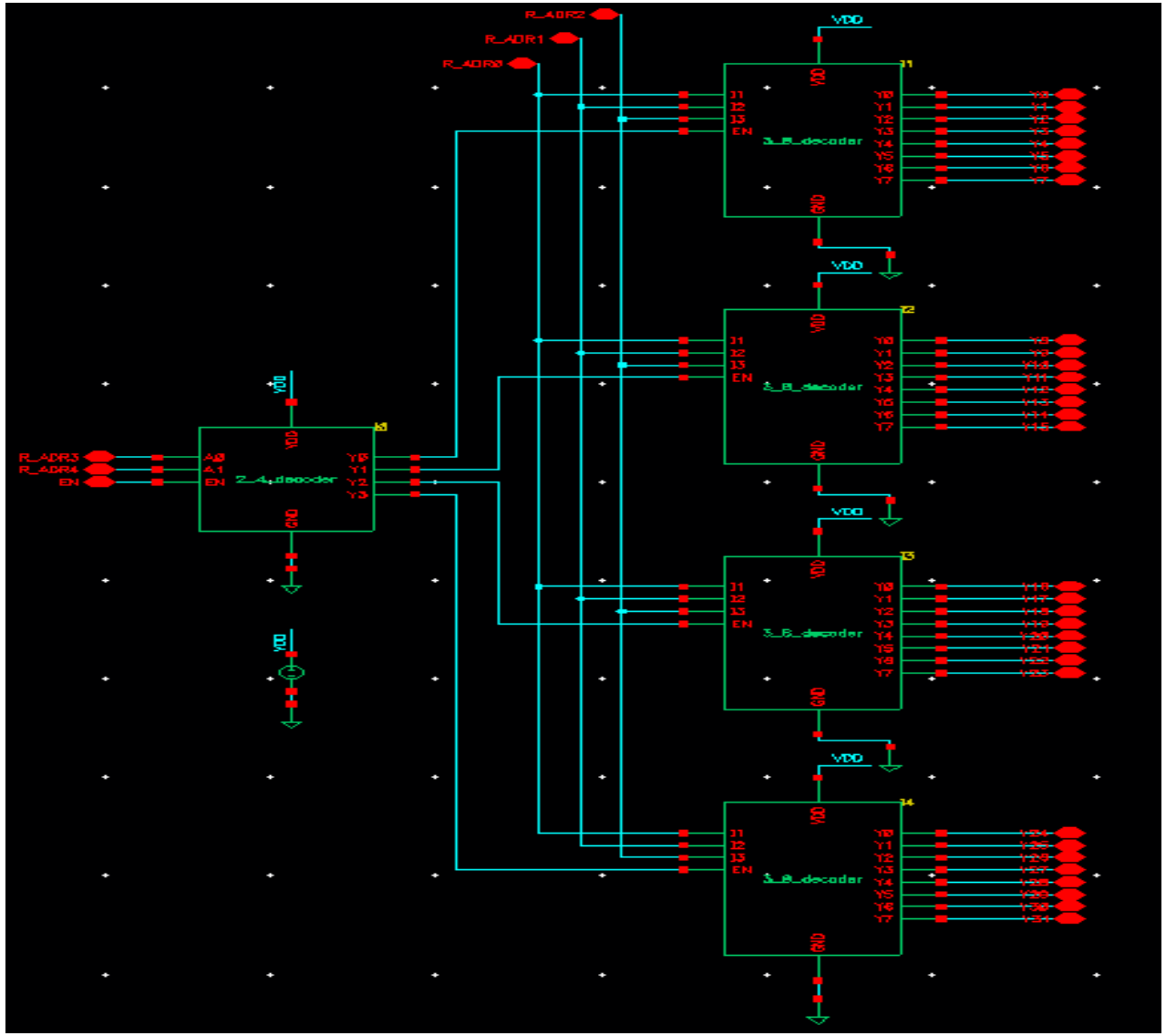


- The circuit diagram depicts a 2-to-4 decoder using CMOS technology.
- It decodes 2 binary inputs into 4 mutually exclusive outputs, activating only one output line corresponding to the input binary code.

Schematic Representation of 3-8 decoder



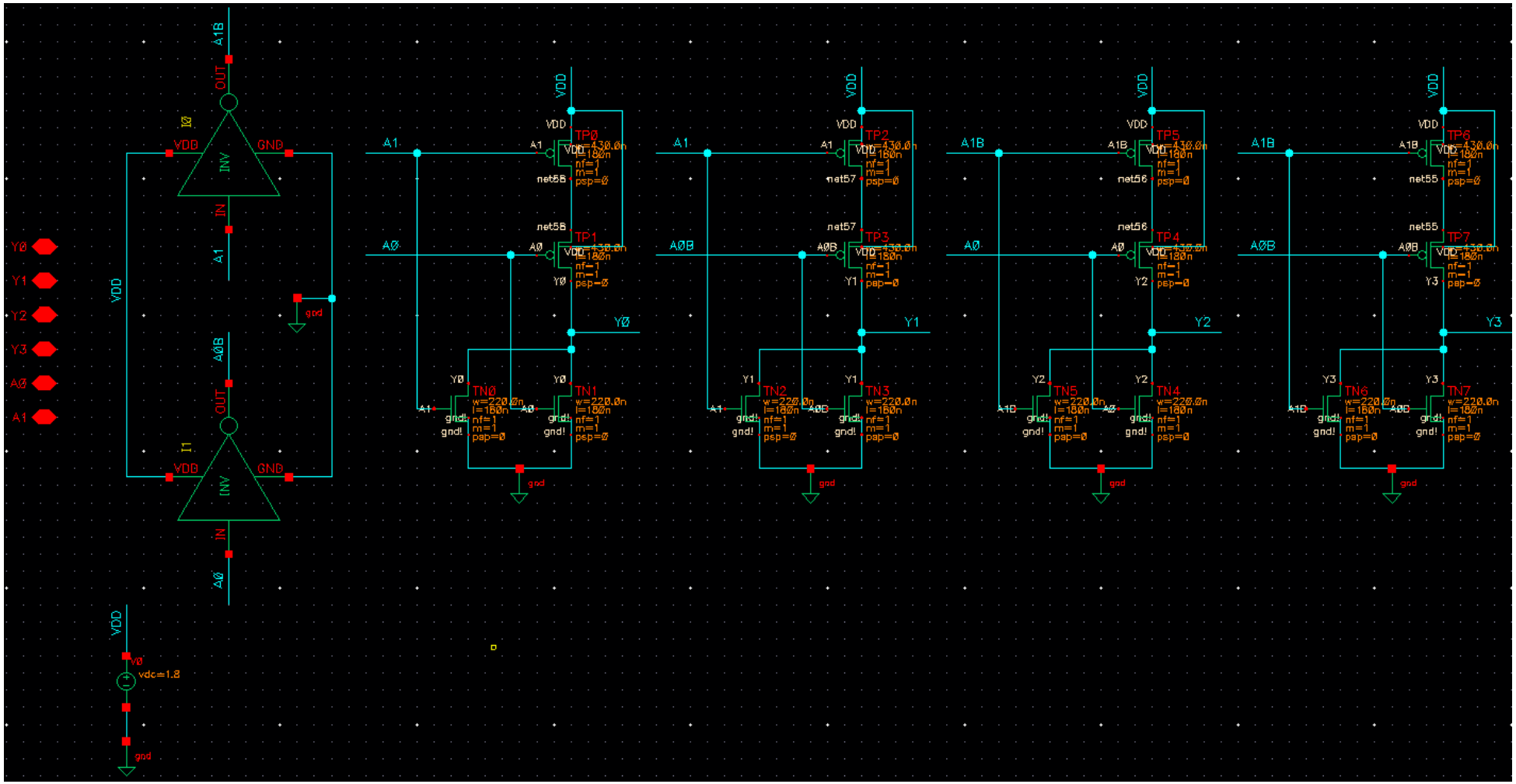
Design and implementation of Row Decoder:



The circuit diagram illustrates a 5-to-32 decoder constructed using four 3-to-8 decoders and one 2-to-4 decoder.

It takes 5 binary inputs (A0-A4) and produces 32 unique outputs (D0-D31), where only one output line is activated high corresponding to the input binary code.

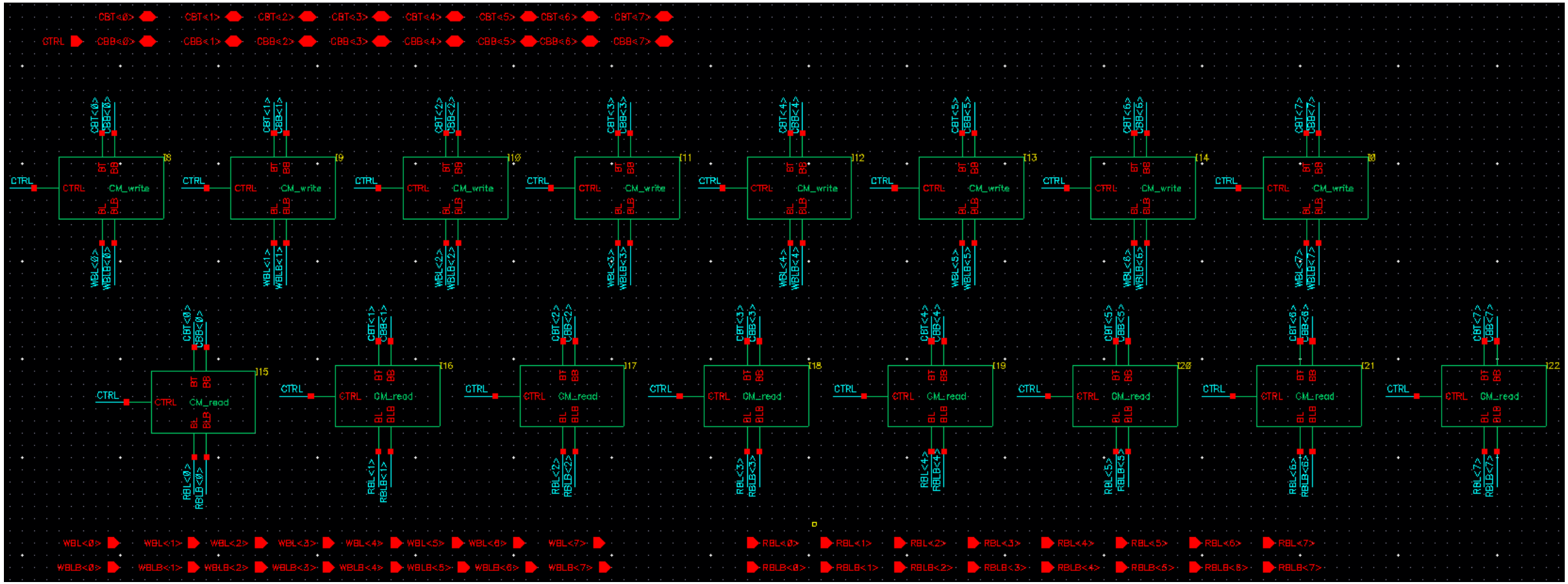
Schematic Representation of Column Decoder



The column decoder is responsible for selecting a specific column mux of the SRAM array based on the address provided.

It takes a binary address input and decodes it into a set of control signals, each of which corresponds to a particular column of an array.

Designing of Column Mux:



Plans for Next Week

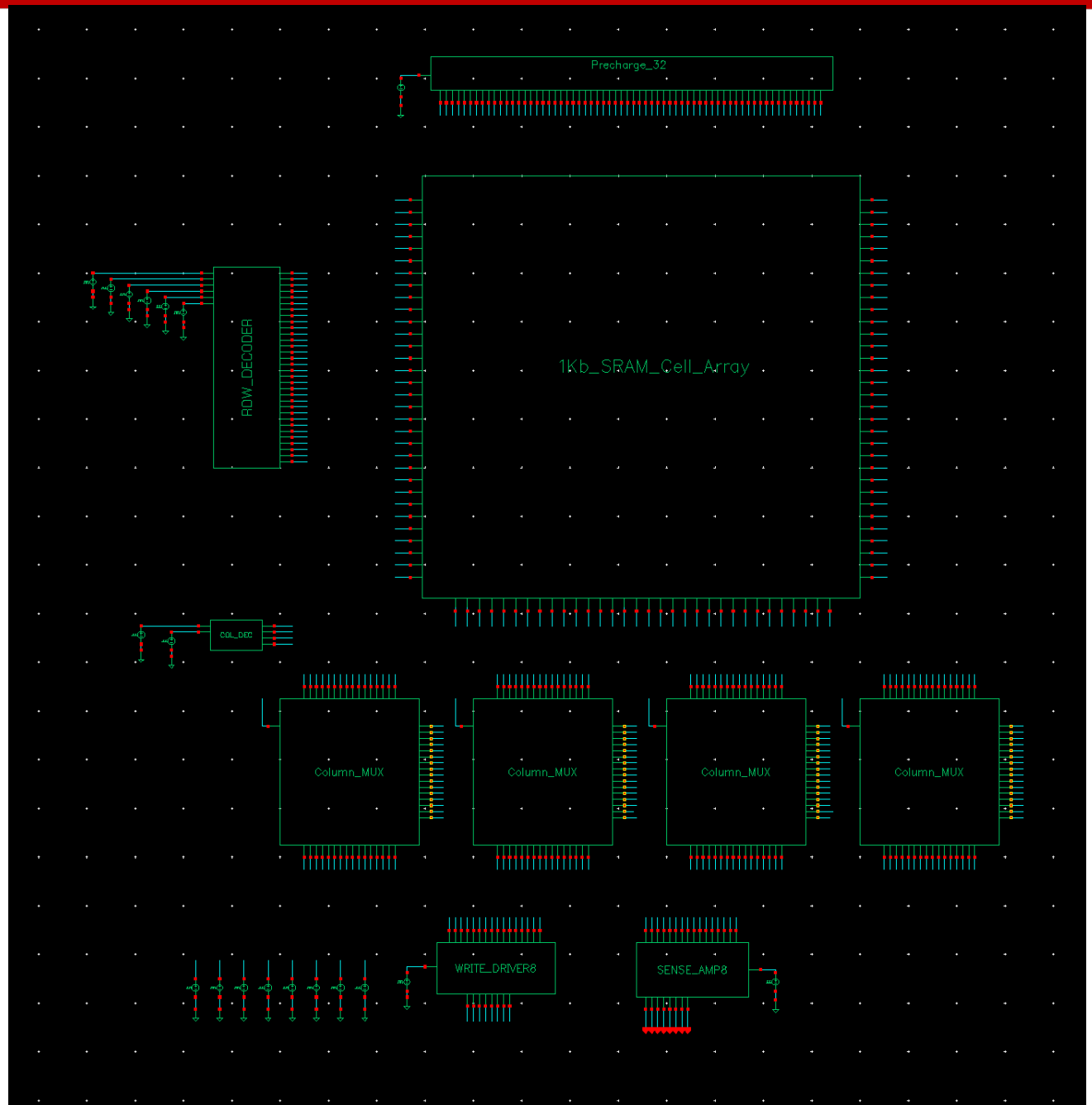
Read Papers on SNNs
- Then pick up from the previous reading on Leaky Integrate-and-Fire Neuron circuits and the Few-Spikes-Neuron-Based SNN Processor introduced in FSNAP paper.

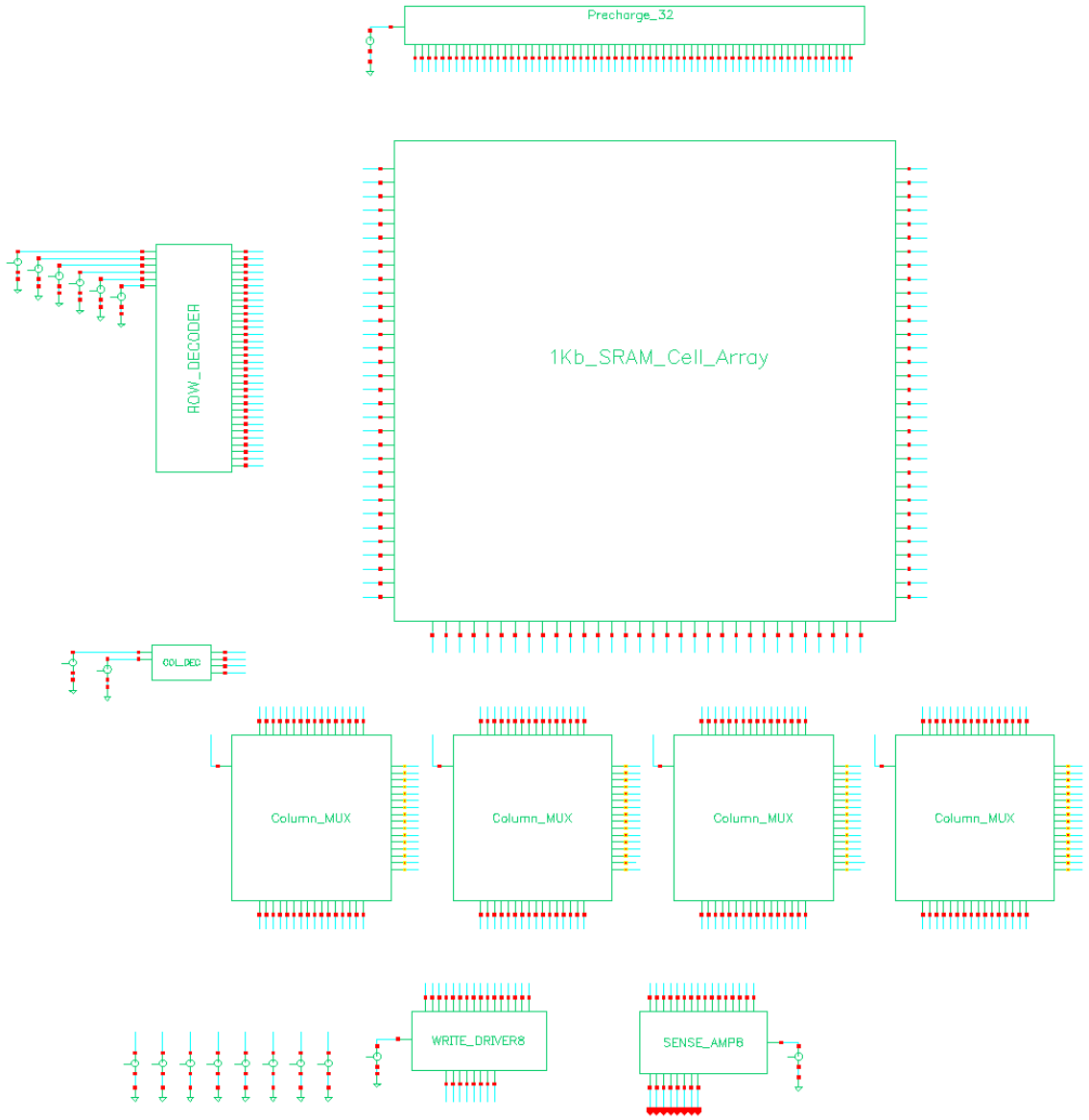
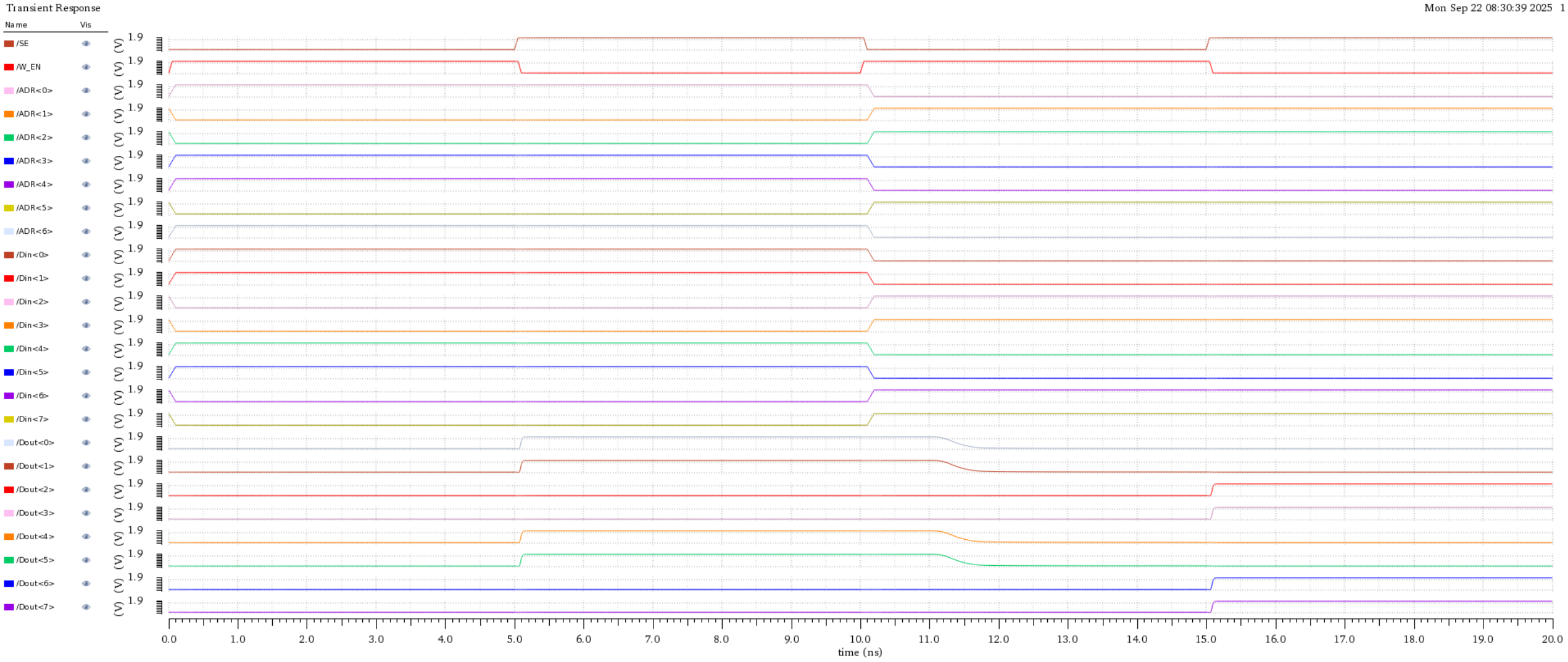
Subgroup meeting paper reading:
- Charge-Mode Neural Stimulator With a Capacitor-Reuse Residual Charge Detector and Active Charge Balancing for Epileptic Seizure Suppression

*Complete the SRAM 1kb (32x32 array) simulation by this weekend.

Design and implementation of 1kb SRAM memory

- Figure shows the complete schematic of 1kb SRAM cell with its peripheral circuits. 1kb
- SRAM memory have the aspect ratio of 32*32.




Precharge_32
ROW_DECODER
1Kb_SRAM_Cell_Array
COL_DEC
Column_MUX
Column_MUX
Column_MUX
Column_MUX
WRITE_DRIVER8
SENSE_AMP8

Simulation results of 1kb SRAM memory