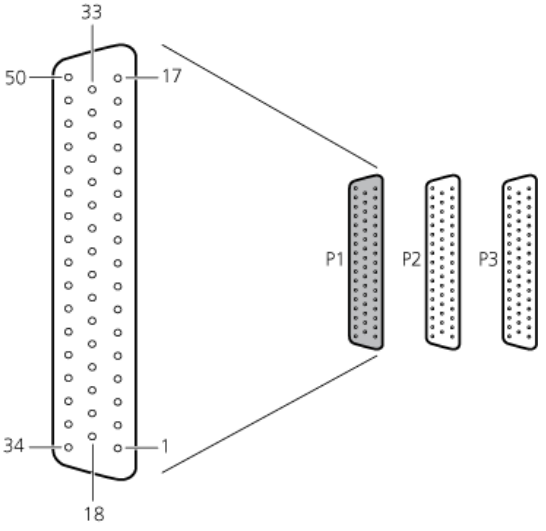


| Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|
| 50 | GND[1)] | 33 | Analog In 5 Ch. 1 Signal | 17 | GND[1)] |
| 49 | Analog In 5 Ch. 1 Reference | 32 | Resistance Out 2 Ch. 6 Reference | 16 | Resistance Out 2 Ch. 6 Signal |
| 48 | Analog Out 7 Ch. 1 Signal | 31 | Digital In 3 Ch. 12 Signal | 15 | Analog Out 7 Ch. 1 Reference |
| 47 | Digital In 3 Ch. 11 Signal | 30 | Digital In 3 Ch. 9 Signal | 14 | Digital In 3 Ch. 10 Signal |
| 46 | Digital Out 3 VBAT 2[2)] | 29 | Digital In 3 Ch. 8 Signal | 13 | GND[1)] |
| 45 | Digital In 3 Ch. 7 Signal | 28 | Digital In 3 Ch. 5 Signal | 12 | Digital In 3 Ch. 6 Signal |
| 44 | Reserved (do not connect) | 27 | Digital In 3 Ch. 4 Signal | 11 | Reserved (do not connect) |
| 43 | Digital In 3 Ch. 3 Signal | 26 | Digital In 3 Ch. 1 Signal | 10 | Digital In 3 Ch. 2 Signal |
| 42 | Digital Out 3 VBAT 1[2)] | 25 | Reserved (do not connect) | 9 | GND[1)] |
| 41 | Reserved (do not connect) | 24 | Digital Out 3 Ch. 13 Signal | 8 | Digital Out 3 Ch. 14 Signal |
| 40 | Reserved (do not connect) | 23 | Digital Out 3 Ch. 12 Signal | 7 | Reserved (do not connect) |
| 39 | Digital Out 3 Ch. 11 Signal | 22 | Digital Out 3 Ch. 9 Signal | 6 | Digital Out 3 Ch. 10 Signal |
| 38 | Digital Out 3 VBAT 2[2)] | 21 | Digital Out 3 Ch. 8 Signal | 5 | GND[1)] |
| 37 | Digital Out 3 Ch. 7 Signal | 20 | Digital Out 3 Ch. 5 Signal | 4 | Digital Out 3 Ch. 6 Signal |
| 36 | Reserved (do not connect) | 19 | Digital Out 3 Ch. 4 Signal | 3 | Reserved (do not connect) |
| 35 | Digital Out 3 Ch. 3 Signal | 18 | Digital Out 3 Ch. 1 Signal | 2 | Digital Out 3 Ch. 2 Signal |
| 34 | Digital Out 3 VBAT 1[2)] | | | 1 | GND[1)] |

1. To improve signal integrity, it is recommended to use all the GND pins in parallel. Each GND pin can carry a maximum of 1 $A_{RMS}$.
2. To improve signal integrity, it is recommended to use all the VBATx pins in parallel. Each VBATx pin can carry a maximum of only 1 $A_{RMS}$.