

1. Description

1.1. Project

Project Name	f103test
Board Name	custom
Generated with:	STM32CubeMX 6.5.0
Date	05/09/2023

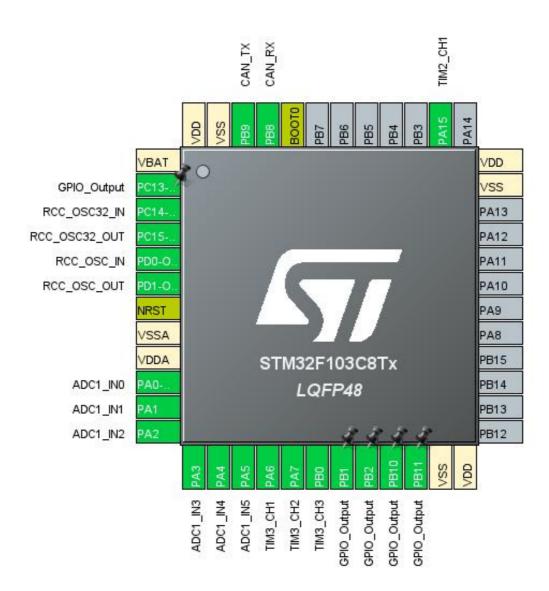
1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103C8Tx
MCU Package	LQFP48
MCU Pin number	48

1.3. Core(s) information

Core(s)	Arm Cortex-M3

2. Pinout Configuration

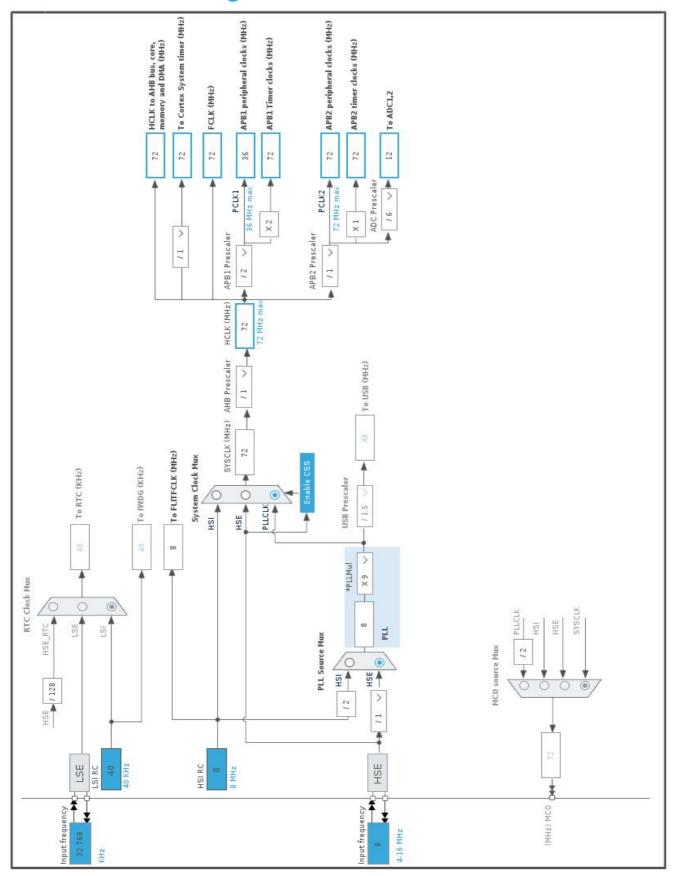


3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP48	(function after		Function(s)	
	reset)			
1	VBAT	Power		
2	PC13-TAMPER-RTC *	I/O	GPIO_Output	
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PD0-OSC_IN	I/O	RCC_OSC_IN	
6	PD1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
10	PA0-WKUP	I/O	ADC1_IN0	
11	PA1	I/O	ADC1_IN1	
12	PA2	I/O	ADC1_IN2	
13	PA3	I/O	ADC1_IN3	
14	PA4	I/O	ADC1_IN4	
15	PA5	I/O	ADC1_IN5	
16	PA6	I/O	TIM3_CH1	
17	PA7	I/O	TIM3_CH2	
18	PB0	I/O	TIM3_CH3	
19	PB1 *	I/O	GPIO_Output	
20	PB2 *	I/O	GPIO_Output	
21	PB10 *	I/O	GPIO_Output	
22	PB11 *	I/O	GPIO_Output	
23	VSS	Power		
24	VDD	Power		
35	VSS	Power		
36	VDD	Power		
38	PA15	I/O	TIM2_CH1	
44	BOOT0	Boot		
45	PB8	I/O	CAN_RX	
46	PB9	I/O	CAN_TX	
47	VSS	Power		
48	VDD	Power		

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value	
Project Name	f103test	
Project Folder	/home/synsi/STM32CubeIDE/workspace_1.9.0/f103test	
Toolchain / IDE	STM32CubeIDE	
Firmware Package Name and Version	STM32Cube FW_F1 V1.8.4	
Application Structure	Advanced	
Generate Under Root	Yes	
Do not generate the main()	No	
Minimum Heap Size	0x200	
Minimum Stack Size	0x400	

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_CAN_Init	CAN
5	MX_TIM1_Init	TIM1
6	MX_ADC1_Init	ADC1
7	MX_TIM2_Init	TIM2
8	MX_TIM3_Init	TIM3

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
мси	STM32F103C8Tx
Datasheet	DS5319_Rev17

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

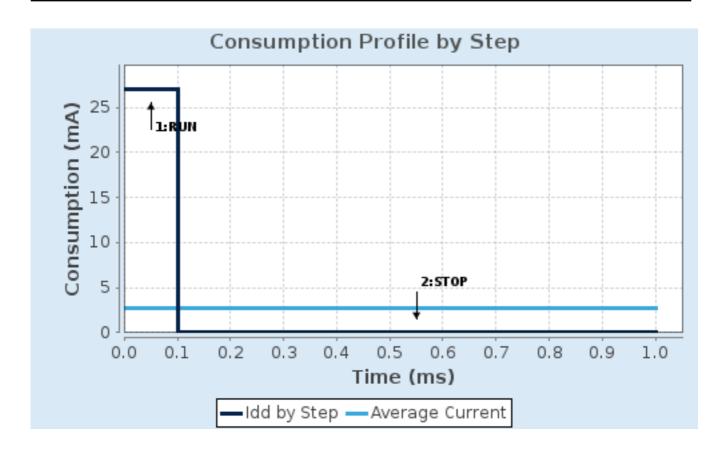
6.4. Sequence

	1	
Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	72 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	27 mA	14 µA
Duration	0.1 ms	0.9 ms
DMIPS	90.0	0.0
Ta Max	100.1	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	2.71 mA
Battery Life	1 month, 21 days,	Average DMIPS	61.0 DMIPS
	17 hours		

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC1
mode: IN0
mode: IN1
mode: IN2
mode: IN3
mode: IN4
mode: IN5

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Data Alignment Right alignment

Scan Conversion Mode Disabled
Continuous Conversion Mode Disabled
Discontinuous Conversion Mode Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions Enable

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

Rank 1

Channel Channel 0
Sampling Time 1.5 Cycles

ADC_Injected_ConversionMode:

Enable Injected Conversions Disable

WatchDog:

Enable Analog WatchDog Mode false

7.2. CAN

mode: Activated

7.2.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum) 16

Time Quantum 444.44444444446 *

Time Quanta in Bit Segment 1 1 Time

Time Quanta in Bit Segment 2 1 Time Time for one Bit 1333 * **Baud Rate** 749999 * 1 Time

ReSynchronization Jump Width

Basic Parameters:

Time Triggered Communication Mode Disable Automatic Bus-Off Management Disable Disable Automatic Wake-Up Mode Automatic Retransmission Disable Receive Fifo Locked Mode Disable Transmit Fifo Priority Disable

Advanced Parameters:

Test Mode Normal

7.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator Low Speed Clock (LSE): Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3 Prefetch Buffer Enabled

Flash Latency(WS) 2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value 16 HSE Startup Timout Value (ms) 100 LSE Startup Timout Value (ms) 5000

7.4. SYS

Debug: No Debug

Timebase Source: TIM4

7.5. TIM1

mode: One Pulse Mode 7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0
Counter Mode Up
Counter Period (AutoReload Register - 16 bits value) 65535
Internal Clock Division (CKD) No Division

Repetition Counter (RCR - 8 bits value) 0
auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

7.6. TIM2

Channel1: PWM Generation CH1

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 65535

Internal Clock Division (CKD) No Division auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)

Disable (Trigger input effect not delayed)

Trigger Event Selection

Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

7.7. TIM3

Combined Channels: XOR ON / Hall Sensor Mode

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0
Counter Mode Up
Counter Period (AutoReload Register - 16 bits value) 65535
Internal Clock Division (CKD) No Division auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection Output Compare (OC2REF)

Hall Sensor:

Prescaler Division Ratio No division
Polarity Rising Edge

Input Filter 0
Commutation Delay 0

7.8. FREERTOS

Interface: CMSIS_V2

7.8.1. Config parameters:

API:

FreeRTOS API CMSIS v2

Versions:

FreeRTOS version 10.0.1 CMSIS-RTOS version 2.00

Kernel settings:

USE_PREEMPTION Enabled

CPU_CLOCK_HZ SystemCoreClock

TICK_RATE_HZ 1000 MAX_PRIORITIES 56 MINIMAL_STACK_SIZE 128 16 MAX_TASK_NAME_LEN USE_16_BIT_TICKS Disabled Enabled IDLE_SHOULD_YIELD Enabled USE_MUTEXES Enabled USE_RECURSIVE_MUTEXES USE_COUNTING_SEMAPHORES Enabled QUEUE_REGISTRY_SIZE USE_APPLICATION_TASK_TAG Disabled ENABLE_BACKWARD_COMPATIBILITY Enabled USE_PORT_OPTIMISED_TASK_SELECTION Disabled Disabled USE_TICKLESS_IDLE USE_TASK_NOTIFICATIONS Enabled

RECORD_STACK_HIGH_ADDRESS Disabled

Memory management settings:

Memory Allocation Dynamic / Static

TOTAL_HEAP_SIZE 4096 *
Memory Management scheme heap_4

Hook function related definitions:

USE_IDLE_HOOK Disabled
USE_TICK_HOOK Disabled
USE_MALLOC_FAILED_HOOK Disabled
USE_DAEMON_TASK_STARTUP_HOOK Disabled
CHECK_FOR_STACK_OVERFLOW Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS Disabled
USE_TRACE_FACILITY Enabled
USE_STATS_FORMATTING_FUNCTIONS Disabled

Co-routine related definitions:

USE_CO_ROUTINES Disabled

MAX_CO_ROUTINE_PRIORITIES 2

Software timer definitions:

USE_TIMERS Enabled
TIMER_TASK_PRIORITY 2
TIMER_QUEUE_LENGTH 10
TIMER_TASK_STACK_DEPTH 256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY 15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY 5

7.8.2. Include parameters:

Include definitions:

vTaskPrioritySet Enabled Enabled uxTaskPriorityGet Enabled vTaskDelete Disabled vTaskCleanUpResources vTaskSuspend Enabled vTaskDelayUntil Enabled vTaskDelay Enabled xTaskGetSchedulerState Enabled Enabled xTaskResumeFromISR xQueueGetMutexHolder Enabled Disabled xSemaphoreGetMutexHolder

pcTaskGetTaskName Disabled Enabled ux Task Get Stack High Water MarkxTaskGetCurrentTaskHandle Disabled eTaskGetState Enabled $x \\ Event Group Set Bit From ISR$ Disabled xTimerPendFunctionCall Enabled xTaskAbortDelay Disabled xTaskGetHandle Disabled

7.8.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT Enabled *

Project settings (see parameter description first):

Use FW pack heap file Enabled

^{*} User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	n/a	n/a	
	PA1	ADC1_IN1	Analog mode	n/a	n/a	
	PA2	ADC1_IN2	Analog mode	n/a	n/a	
	PA3	ADC1_IN3	Analog mode	n/a	n/a	
	PA4	ADC1_IN4	Analog mode	n/a	n/a	
	PA5	ADC1_IN5	Analog mode	n/a	n/a	
CAN	PB8	CAN_RX	Input mode	No pull-up and no pull-down	n/a	
	PB9	CAN_TX	Alternate Function Push Pull	n/a	High *	
RCC	PC14- OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15- OSC32_OU T	RCC_OSC32_O UT	n/a	n/a	n/a	
	PD0- OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PD1- OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
TIM2	PA15	TIM2_CH1	Alternate Function Push Pull	n/a	Low	
TIM3	PA6	TIM3_CH1	Input mode	No pull-up and no pull-down	n/a	
	PA7	TIM3_CH2	Input mode	No pull-up and no pull-down	n/a	
	PB0	TIM3_CH3	Input mode	No pull-up and no pull-down	n/a	
GPIO	PC13- TAMPER- RTC	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
TIM1_UP	DMA1_Channel5	Memory To Peripheral	Very High *

TIM1_UP: DMA1_Channel5 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Half Word
Memory Data Width: Half Word

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Prefetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	15	0	
System tick timer	true	15	0	
DMA1 channel5 global interrupt	true	5	0	
USB low priority or CAN RX0 interrupts	true	5	0	
TIM4 global interrupt	true	15	0	
PVD interrupt through EXTI line 16	unused			
Flash global interrupt	unused			
RCC global interrupt	unused			
ADC1 and ADC2 global interrupts	unused			
USB high priority or CAN TX interrupts	unused			
CAN RX1 interrupt	unused			
CAN SCE interrupt	unused			
TIM1 break interrupt	unused			
TIM1 update interrupt	unused			
TIM1 trigger and commutation interrupts	unused			
TIM1 capture compare interrupt	unused			
TIM2 global interrupt	unused			
TIM3 global interrupt	unused			

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false

Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler
	sequence ordering	handler	
System tick timer	false	false	true
DMA1 channel5 global interrupt	false	true	true
USB low priority or CAN RX0 interrupts	false	true	true
TIM4 global interrupt	false	true	true

^{*} User modified value

9. System Views

- 9.1. Category view
- 9.1.1. Current

SYS 🤡



10. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32f1_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32ibis.zip

System View https://www.st.com/resource/en/svd/stm32f1_svd.zip

Description

BSDL files https://www.st.com/resource/en/bsdl_model/stm32f1_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32ibis.zip

System View https://www.st.com/resource/en/svd/stm32f1_svd.zip

Description

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stm8_embedded_software_solutions.pdf

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- Application Notes https://www.st.com/resource/en/application_note/an3070-managing-the-driver-enable-signal-for-rs485-and-iolink-communications-with-the-stm32s-usart-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an3095-stevalisv002v1-stevalisv002v2-3-kw-gridconnected-pv-system-based-on-the-stm32f103xx-stmicroelectronics.pdf
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of-stm32-mcus-and-mpus-stmicroelectronics.pdf

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stm32f0f1f3cxgxlx-series-dma-controller-stmicroelectronics.pdf

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for related Tools freertos-guide-stmicroelectronics.pdf

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