NC STATE UNIVERSITY
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
ECE 463/521 · FALL 2016

Project 3: Dynamic Instruction Scheduling

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CONTENTS

1 Effects of IQ_SIZE with a large ROB

1.1 Plot 1

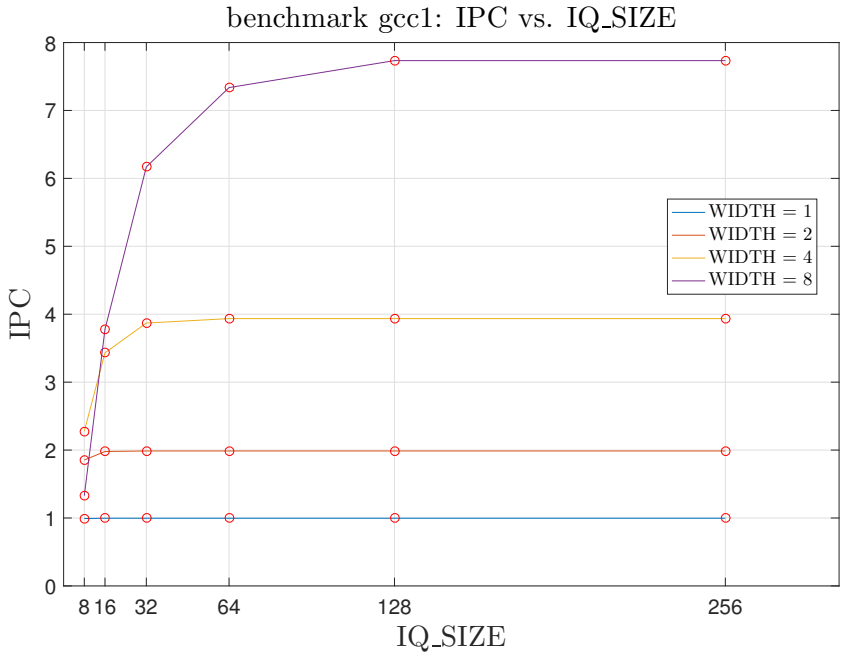

Figure 1.1: Bimodal Predictor Performance in benchmark gcc

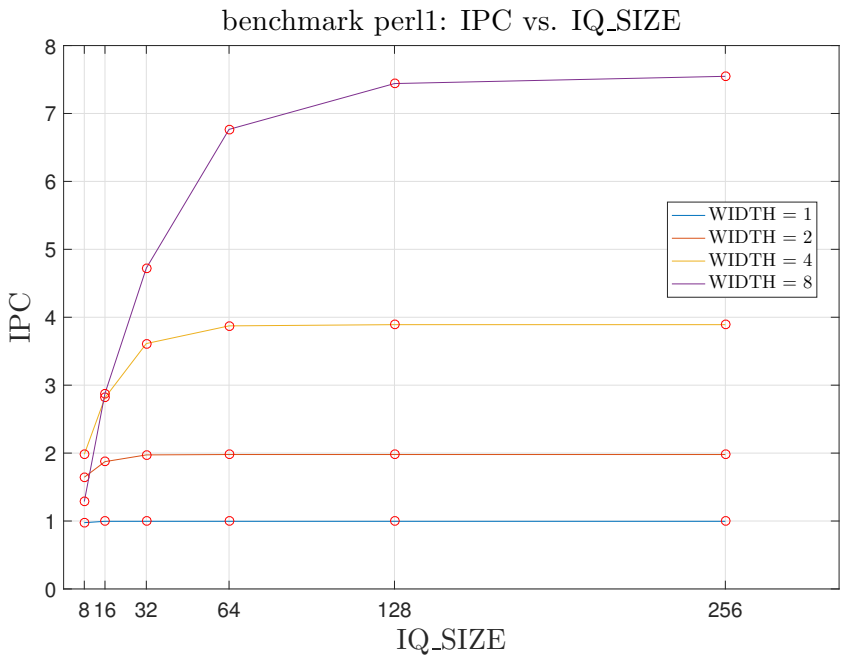

Figure 1.2: Bimodal Predictor Performance in benchmark jpeg

1.2 Analysis

	Optimized IQ_SIZE per WIDTH	
	Benchmark: gcc1	Benchmark: perl1
WIDTH = 1	8	8
WIDTH = 2	16	32
WIDTH = 4	32	64
WIDTH = 8	128	128

1.3 Discussion

1.3.1 (a)

No matter what value WIDTH is, IPC increases as IQ_SIZE increases at first. After IQ_SIZE is more than about eight to sixteen times larger than WIDTH, that is to say, IQ_SIZE is much more larger, IPC becomes to saturate at a value very close to WIDTH. Before IPC saturation, the larger IQ_SIZE is, the less probability of stall caused by insufficient issue queue size is and therefore the higher IPC is. After issue queue is large enough to held nearly all stalled instructions, IQ_SIZE has no influence on IPC and thus IPC saturation occurs.

1.3.2 (b)

Benchmark gcc1 shows higher IPC than benchmark perl1 for the same microarchitecture configuration. This might be because perl1 has more data dependency than gcc1 which causes more instruction to stall in issue stage. This also explains why optimized IQ_SIZE for benchmark perl1 is higher than that for benchmark gcc1.

2 Effect of ROB_SIZE

2.1 Plot 2

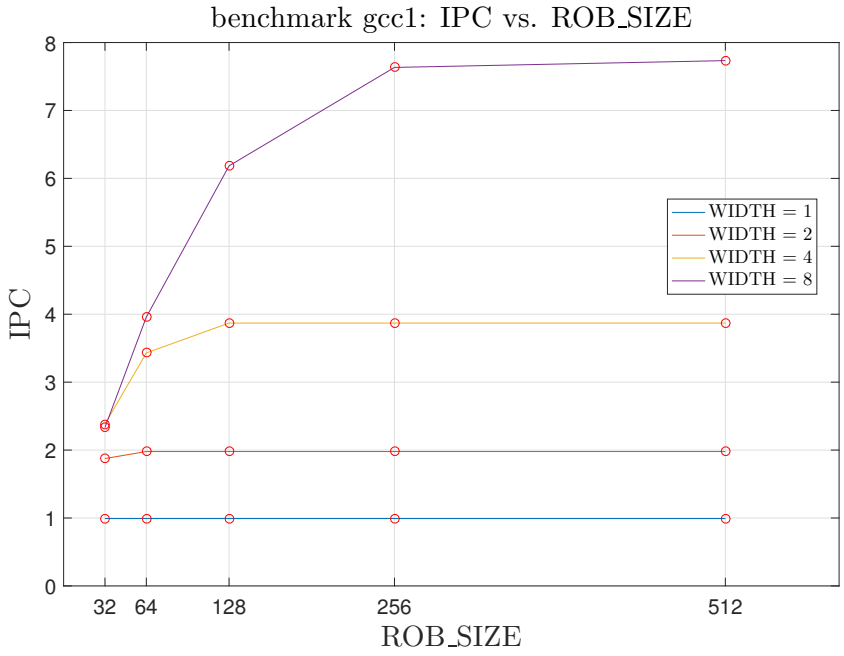

Figure 2.1: Bimodal Predictor Performance in benchmark gcc

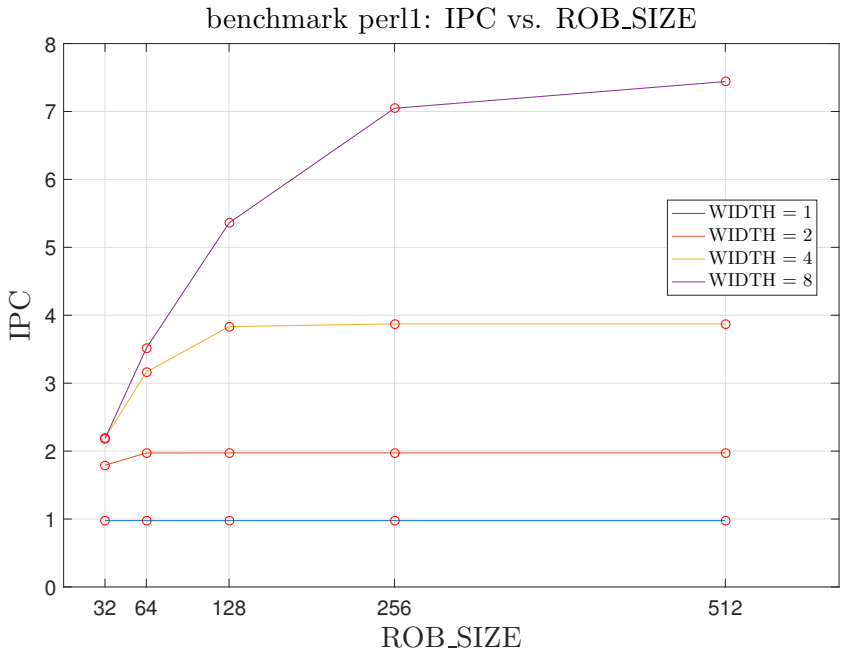

Figure 2.2: Bimodal Predictor Performance in benchmark jpeg

3 Effect of Instruction Cache

3.1 Plot 3

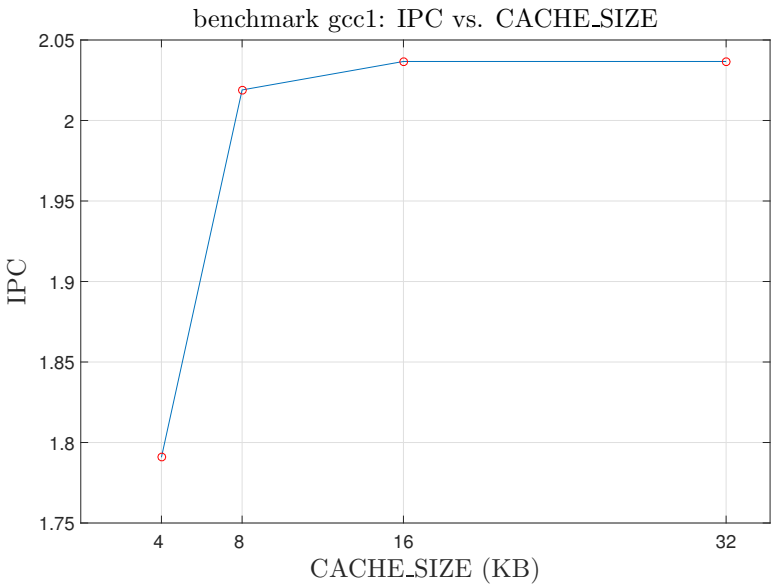

Figure 3.1: Bimodal Predictor Performance in benchmark gcc

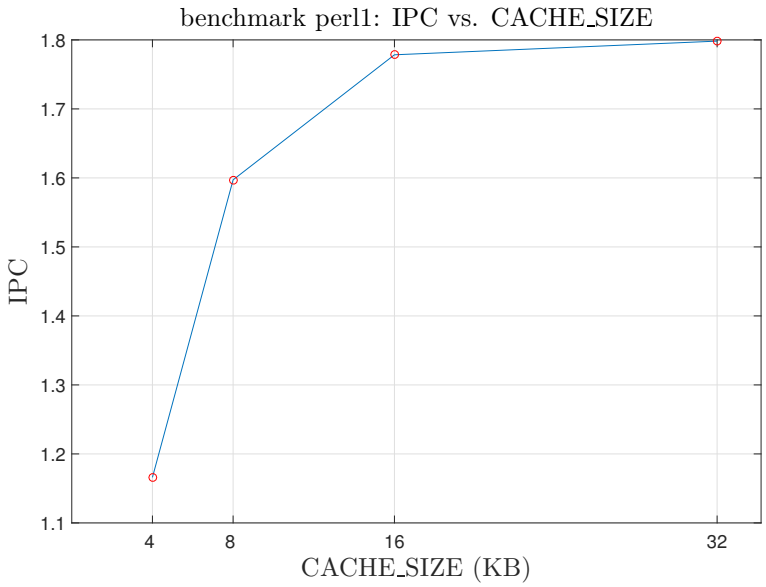

Figure 3.2: Bimodal Predictor Performance in benchmark jpeg

3.2 Discussion

From comparison between Figure 2.1 and 3.1, Figure 2.2 and 3.2, ILP is smaller with cache. This is because miss penalty caused by cache miss increases stalls and thus IPC. However, IPC increases as CACHE_SIZE increases. This is because the larger cache is, the lower cache miss rate is and therefore the higher IPC is.

4 Effect of Prefetching

4.1 Plot 4

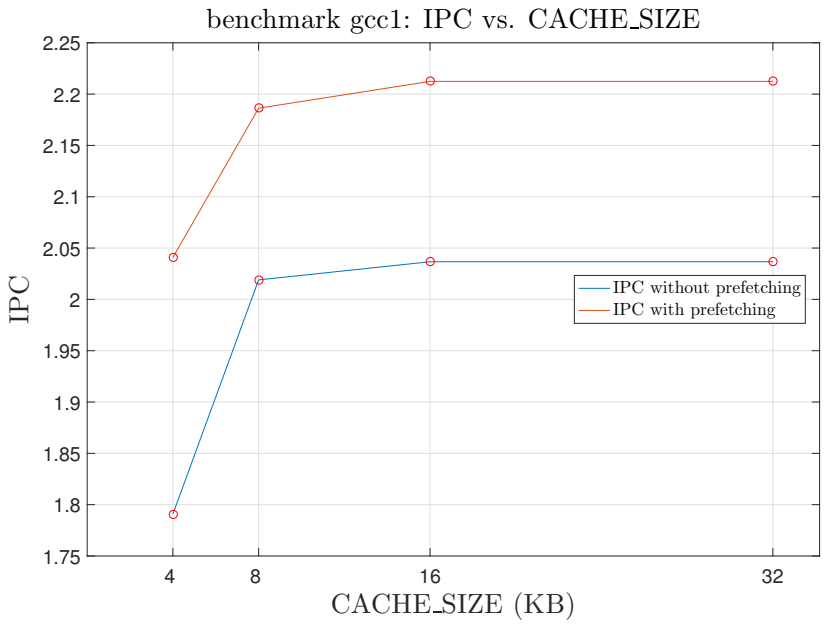

Figure 4.1: Bimodal Predictor Performance in benchmark gcc

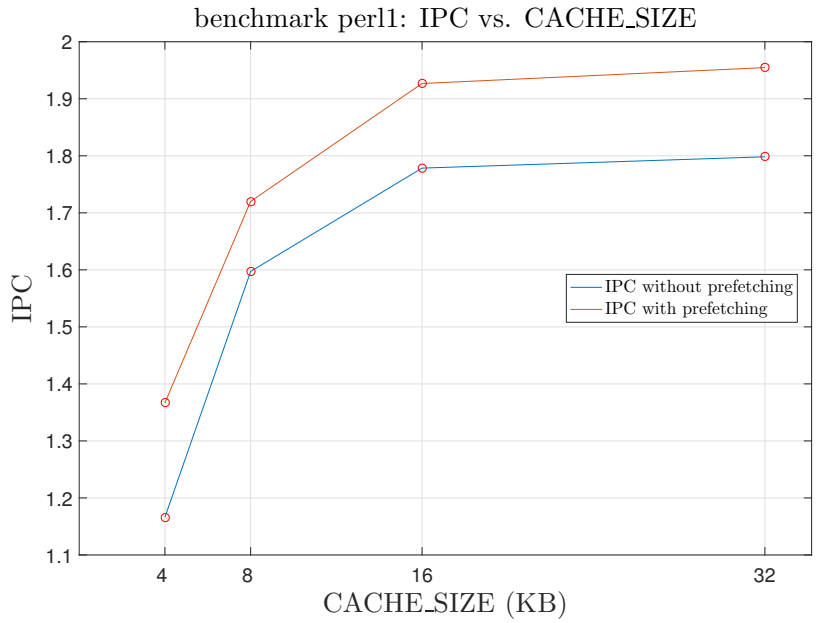

Figure 4.2: Bimodal Predictor Performance in benchmark jpeg

4.2 Discussion

From Figure 4.1 and 4.2, IPC is higher with prefetching. Therefore, prefetching does help the performance. Besides, prefetching helps more when CACHE_SIZE is small.