CSU22022 Computer Architecture I

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Processor Assignment: Full Project

20th November 2022

Version 1.0

The Schematics on the following pages depict the Processor that you need to implement. You need to build a new project in Vivado to run simulations and generate schematics for all entities of the assignment.

You Vivado project should be named “CPU_XXXXXXXX”, with XXXXXXXX as your student number. Save you Datapath project milestone and import the entities from the project into your CPU_XXXXXXXX project.

The project requires the following entities. Please see tables and schematics on the following page.

For details regarding the implementation of the Datapath see:

- Assignment - Project Milestone Register File
- Processor Assignment: Project Milestone Datapath

Number of Intantiations		
	Instantiation Name	**Entity Name**
Processor		
1		CPU_Processor_XXXXXXXX
Datapath		
1	Datapath	DP_Datapath_XXXXXXXX
Register File		
1	RegFile	RF_RegisterFile_32_15_XXXXXXXX
1	DestReg_Decoder	RF_DestReg_Decoder_XXXXXXXX
1	DestTempReg_Decoder	RF_TempDestReg_Decoder_XXXXXXXX
32 15 1	RegisterXX, XX=00 to 31 TempRegXX, XX=01 to 15 PC *	RF_Register32Bit_XXXXXXXX
1 1	Mux32_A Mux32_B	RF_Mux32_32Bit_XXXXXXXX
1 1	Mux16_A Mux16_B	RF_Mux16_32Bit_XXXXXXXX
		* used in processor

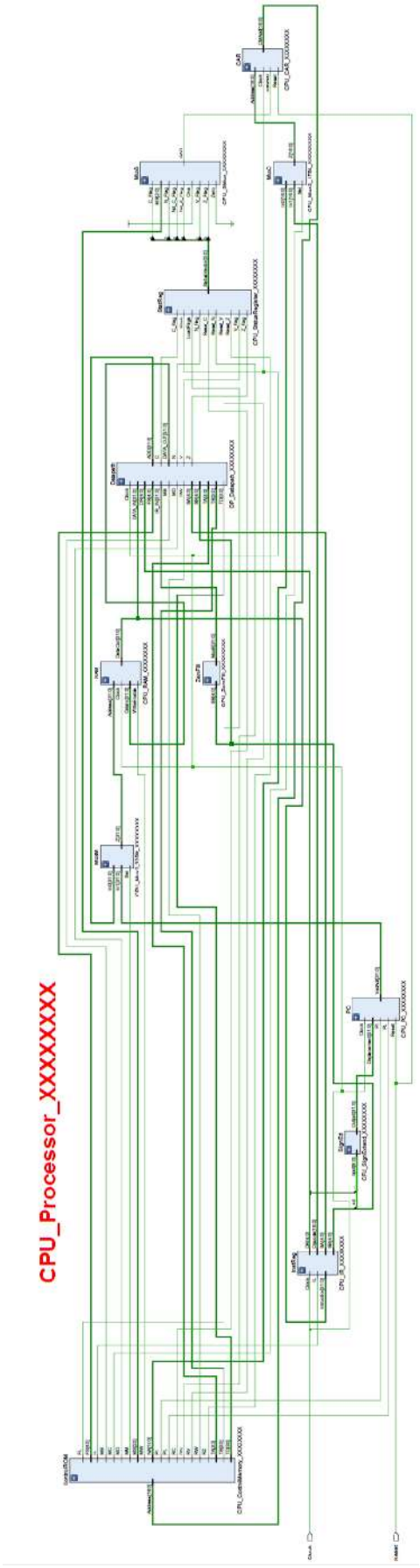
Number of Intantiations	Instantiation Name	Entity Name
	Functional unit	
1	FunctionalUnit	DP_FunctionalUnit_XXXXXXXX
1	ALU	DP_ArithmeticLogicUnit_XXXXXXXX
32	BITXX, XX=00 to 31	DP_FullAdder_XXXXXXXX
1 1	Adder Adder *	DP_RippleCarryAdder32Bit_XXXXXXXX
32	BITXX, XX=00 to 31	DP_SingleBit_B_Logic_XXXXXXXX
1	BLogic	DP_32Bit_B_Logic_XXXXXXXX
32	BITXX, XX=00 to 31	DP_SingleBit_LogicCircuit_XXXXXXXX
1	LogicCircuit	DP_32Bit_LogicCircuit_XXXXXXXX
32	BITXX, XX=00 to 31	DP_Mux3_1Bit_XXXXXXXX
1	CFlagMux	DP_ShifterCFlagMux2_1Bit_XXXXXXXX
1	Shifter	DP_Shifter_XXXXXXXX
1	C_Flag	DP_CFlagMux2_1Bit_XXXXXXXX
1	Z_Flag	DP_ZeroDetection_XXXXXXXX
1 1 1 1 1 1 1	MuxB MuxD MuxF ALUMux PL_PI_Mux * ResetMux * MuxM *	CPU_Mux2_32Bit_XXXXXXXX
		* used in processor

Number of Intantiations		
	Instantiation Name	**Entity Name**
	Processor	
1	RAM	CPU_RAM_XXXXXXXX
1	ControlROM	CPU_ControlMemory_XXXXXXXX
1	InstReg	CPU_IR_XXXXXXXX
1	ZeroFill	CPU_ZeroFill_XXXXXXXX
1	PC	CPU_PC_XXXXXXXX
1	SignExt	CPU_SignExtend_XXXXXXXX
1	MuxS	CPU_SMux_XXXXXXXX
1	MuxC	CPU_Mux2_17Bit_XXXXXXXX
1	CAR	CPU_CAR_XXXXXXXX
1 1 1 1	CFlag VFlag NFlag ZFlag	CPU_DFlipFlop_XXXXXXXX
1	StatReg	CPU_StatusRegister_XXXXXXXX

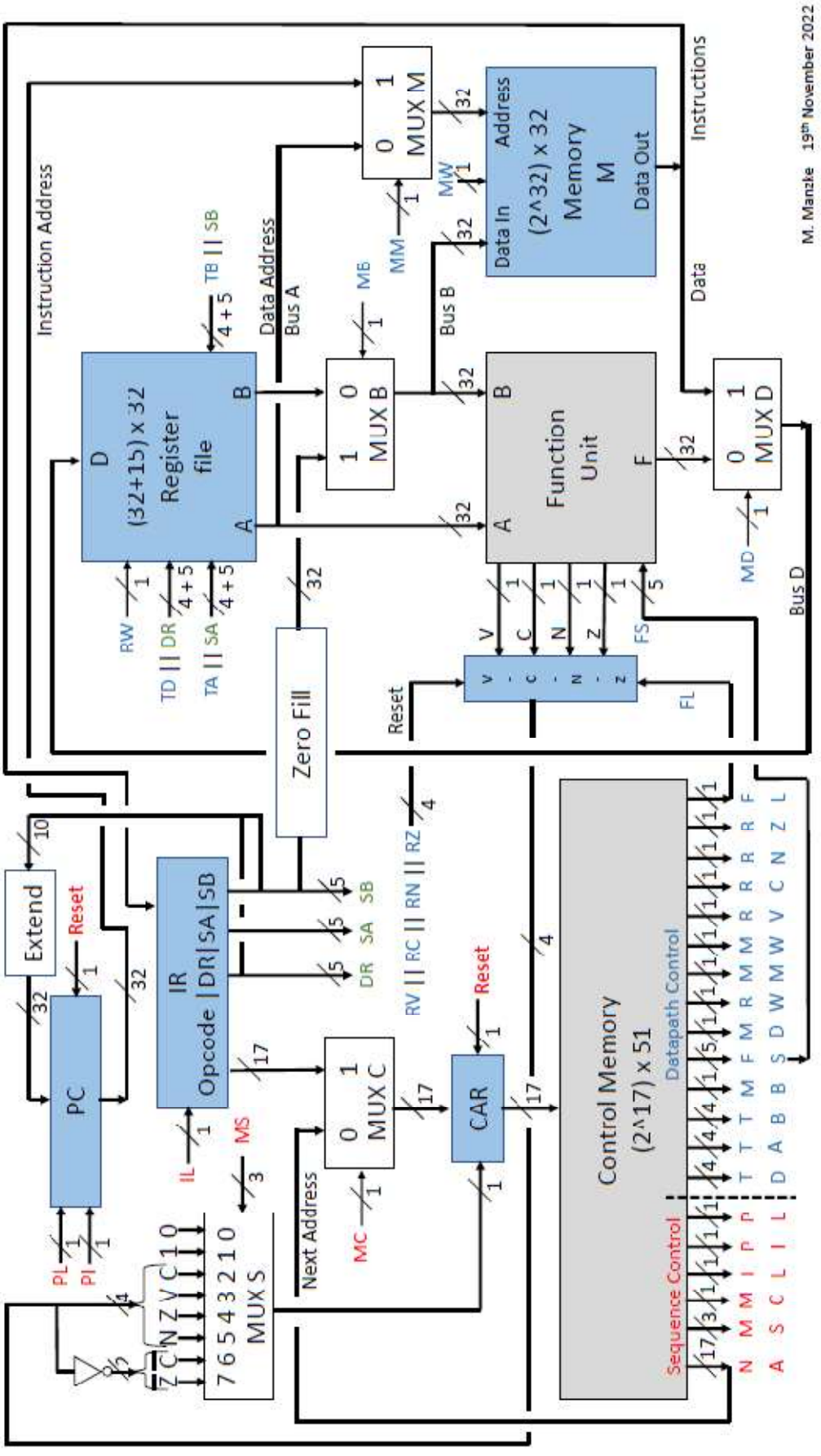
Number of Intantiations		
	Instantiation Name	
		Entity Name
Processor Tests		
1		CPU_Processor_Test01_XXXXXXXX
1		CPU_Processor_Test02_XXXXXXXX
1		CPU_Processor_Test03_XXXXXXXX
1		CPU_Processor_Test04_XXXXXXXX

FS Code

FS					MF Select	G Select				H Select		Micro-operation
S3 FS(4)	S2 FS(3)	S1 FS(2)	S0 FS(1)	C FS(0)	S3	S2	S1	S0	C	S2	S1	
0	0	0	0	0	0	0	0	0	0	0	0	F = A
0	0	0	0	1	0	0	0	0	1	0	0	F = A + 1
0	0	0	1	0	0	0	0	1	0	0	0	F = A + B
0	0	0	1	1	0	0	0	1	1	0	0	F = A + B + 1
0	0	1	0	0	0	0	1	0	0	0	1	F = A + NOT(B)
0	0	1	0	1	0	0	1	0	1	0	1	F = A + NOT(B) + 1
0	0	1	1	0	0	0	1	1	0	0	1	F = A - 1
0	0	1	1	1	0	0	1	1	1	0	1	F = A
0	1	0	0	0	0	1	0	0	0	1	0	F = A AND B
0	1	0	1	0	0	1	0	1	0	1	0	F = A OR B
0	1	1	0	0	0	1	1	0	0	1	1	F = A XOR B
0	1	1	1	0	0	1	1	1	0	1	1	F = NOT(A)
1	0	0	0	0	1	0	0	0	0	0	0	F = B
1	0	1	0	0	1	0	1	0	0	0	1	F = srB
1	1	0	0	0	1	1	0	0	0	1	0	F = slB



For more detail see CPU_Processor_XXXXXXXX_Schematic01.pdf



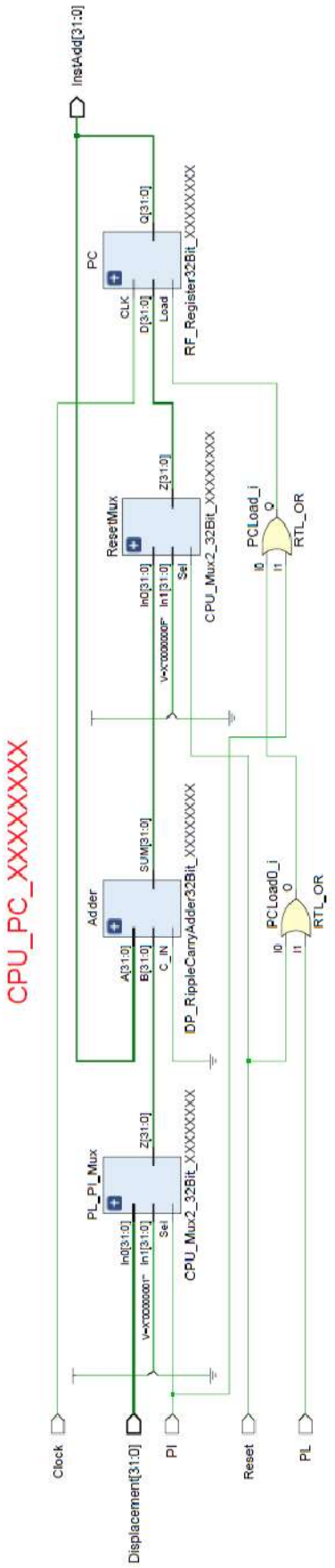
For more details see Processor32bit_2022_2023.pdf

Once your Datapath is fully working, you must implement the following entities. Do not connect these entities to the Datapath. Please follow the order specified in the Checklist (CSU22022 Processor Project 2022-2023 Checklist V1.0.pdf)

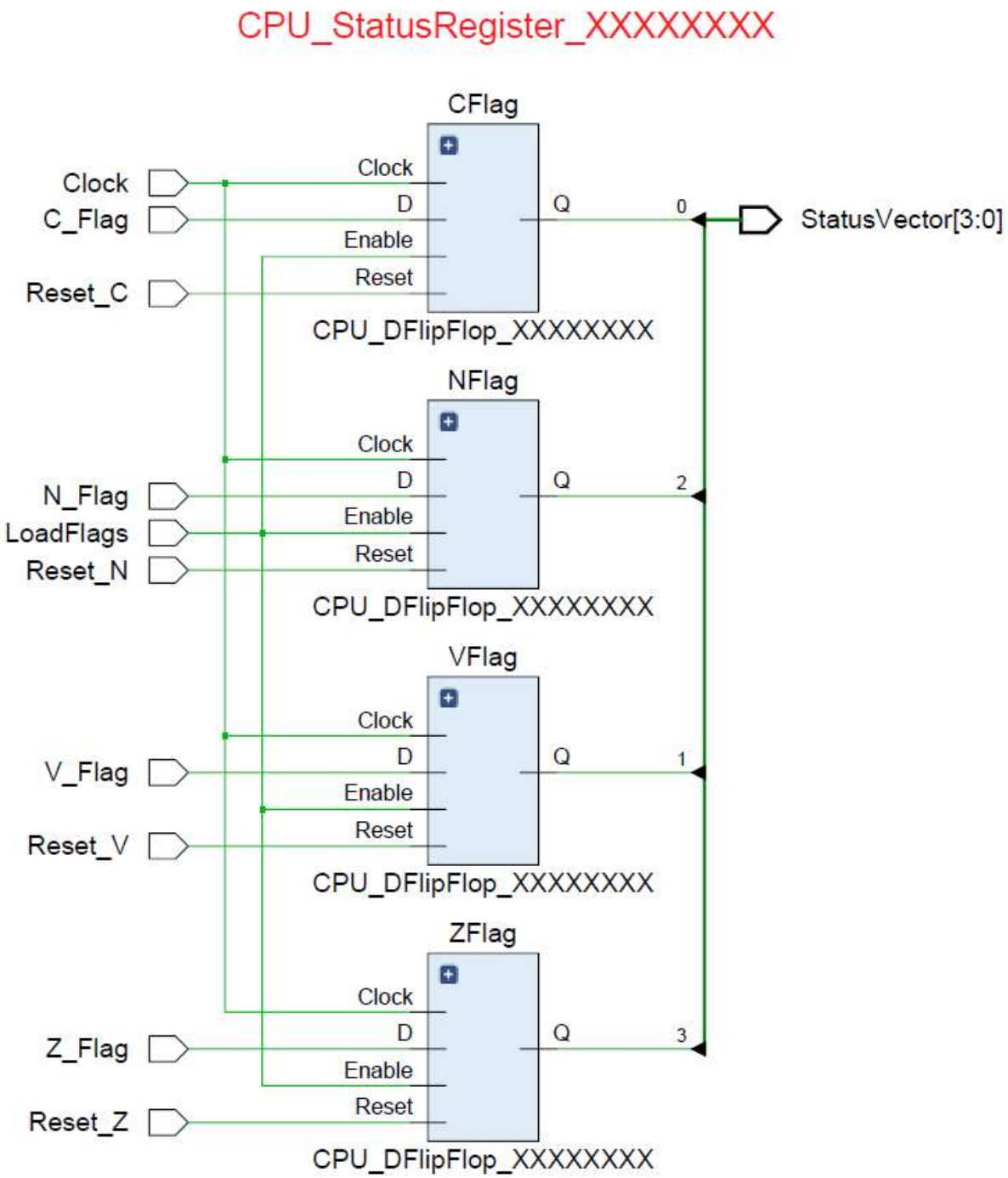
Lecture note 14-CSU22022_processor_fourteenth_lecture_2022_2023.pdf provides information regarding the implementation of the CPU_RAM_XXXXXXXX. Your design should have 128 memory addresses (using the 7 least significant bits of the 32 bit address).

Lecture note 15-CSU22022_processor_fiveteenth_lecture_2022_2023.pdf provides information regarding the implementation of the CPU_ControlMemory_XXXXXXXX. Your design should have 128 memory addresses (using the 7 least significant bits of the 17 bit address).

Number of Intantiations	**Instantiation Name**	**Entity Name**
	Processor	
1	RAM	CPU_RAM_XXXXXXXX
1	ControlROM	CPU_ControlMemory_XXXXXXXX
1	InstReg	CPU_IR_XXXXXXXX
1	ZeroFill	CPU_ZeroFill_XXXXXXXX
1	PC	CPU_PC_XXXXXXXX
1	SignExt	CPU_SignExtend_XXXXXXXX
1	MuxS	CPU_SMux_XXXXXXXX
1	MuxC	CPU_Mux2_17Bit_XXXXXXXX
1	CAR	CPU_CAR_XXXXXXXX
1 1 1 1	CFlag VFlag NFlag ZFlag	CPU_DFlipFlop_XXXXXXXX
1	StatReg	CPU_StatusRegister_XXXXXXXX

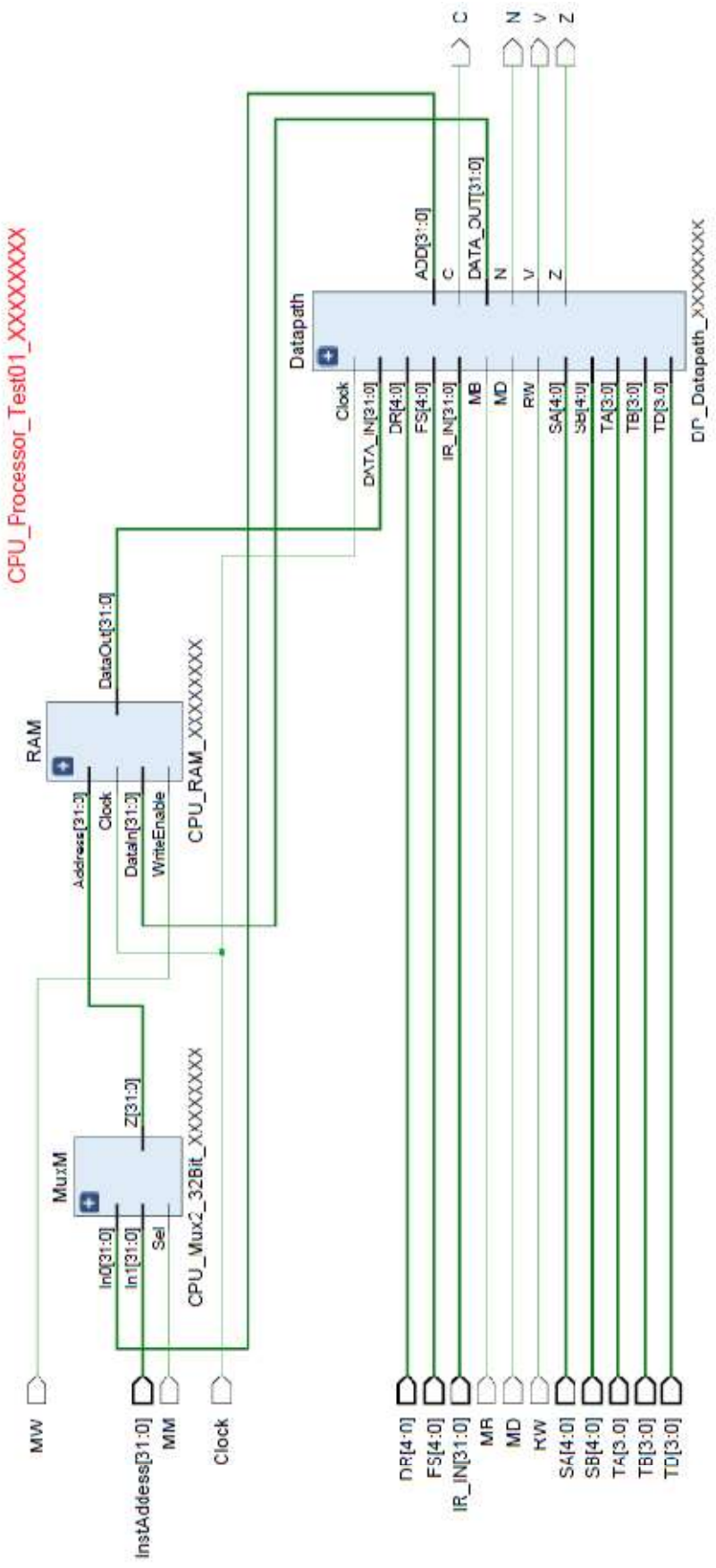


For more details see CPU_PC_XXXXXXXX_Schematic01.pdf

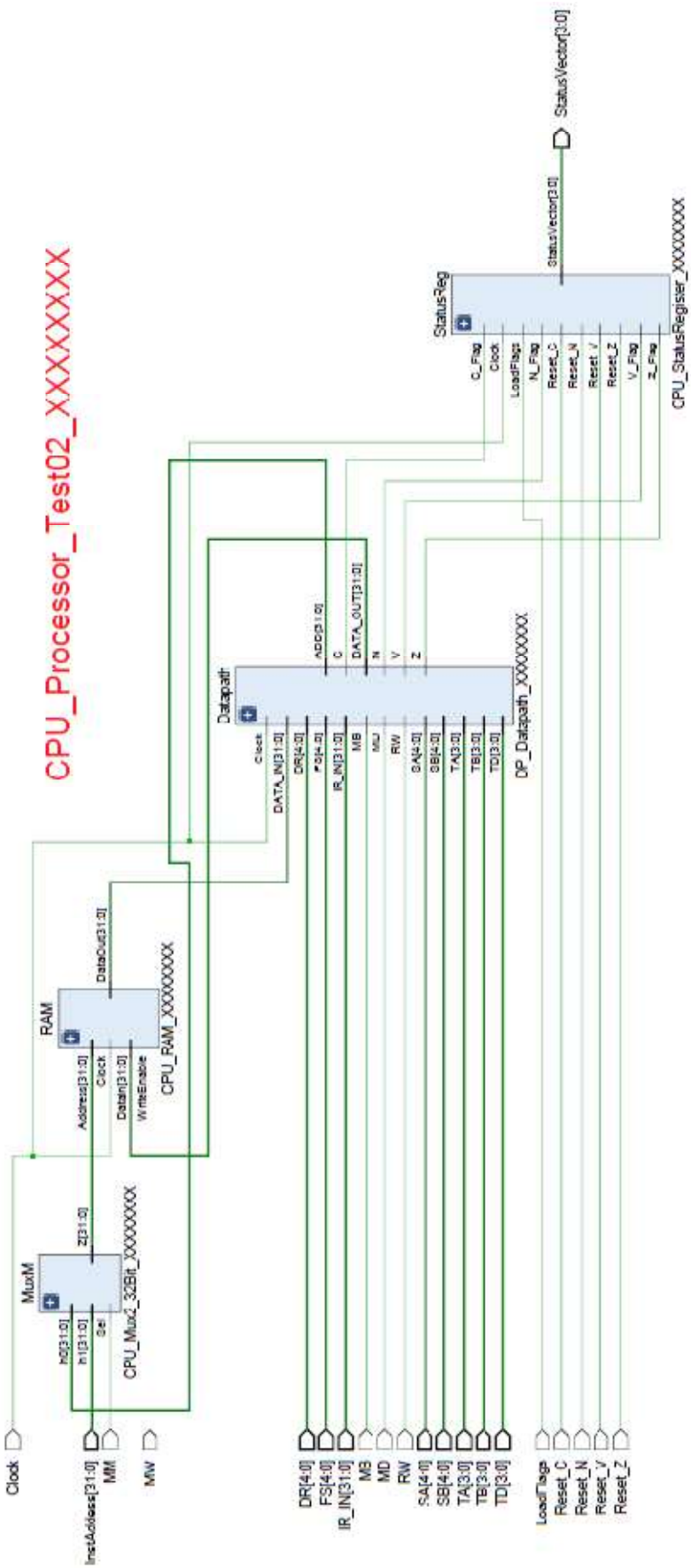


For more details see CPU_StatusRegister_XXXXXXXX_Schematic01.pdf

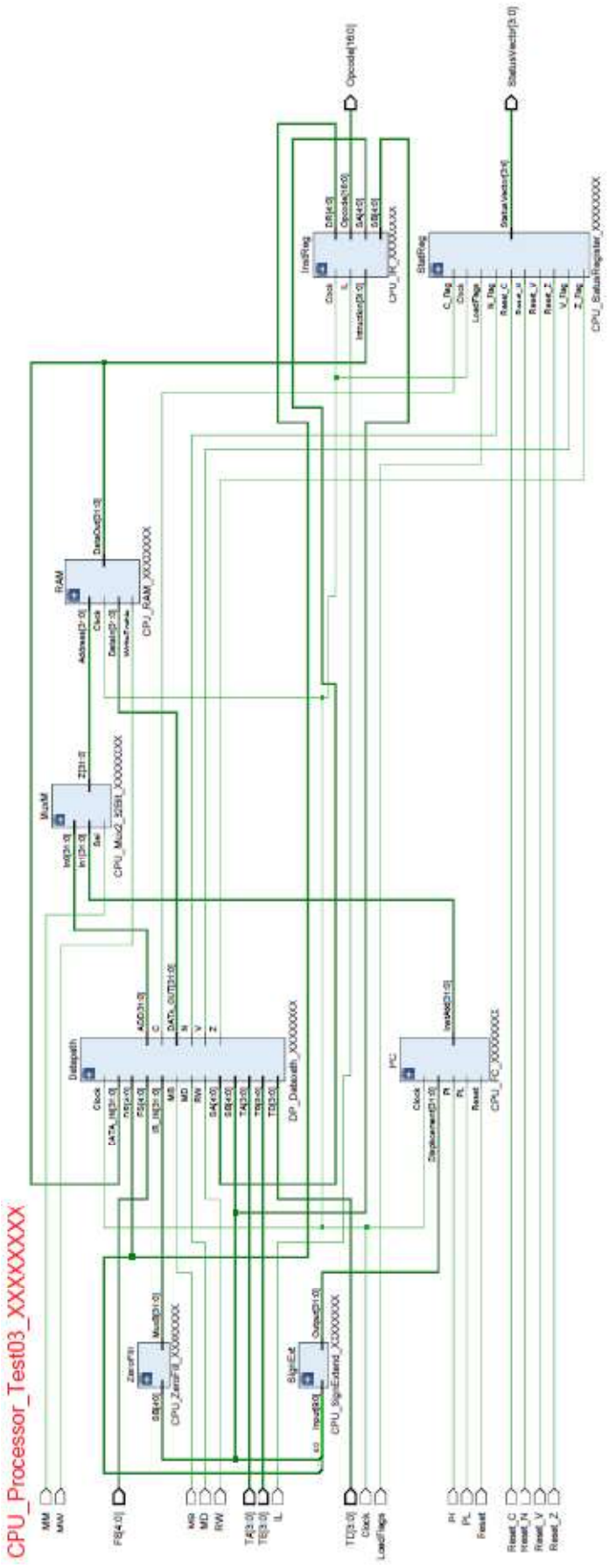
Once we have build and tested all these entities, we will then build the processor incrementally in five steps:



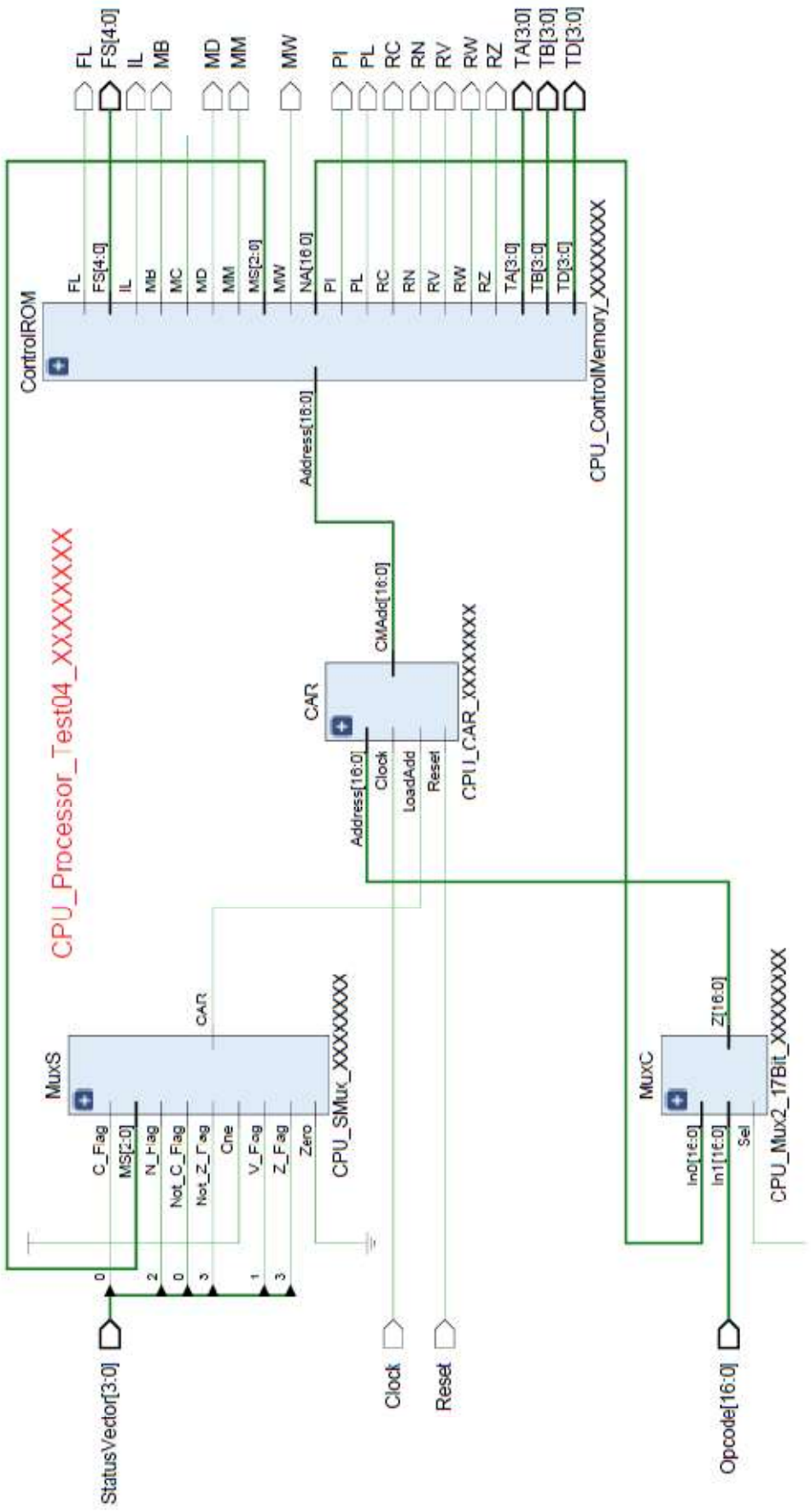
For more details see CPU_Processor_Test01_XXXXXXXX_Schematic01.pdf



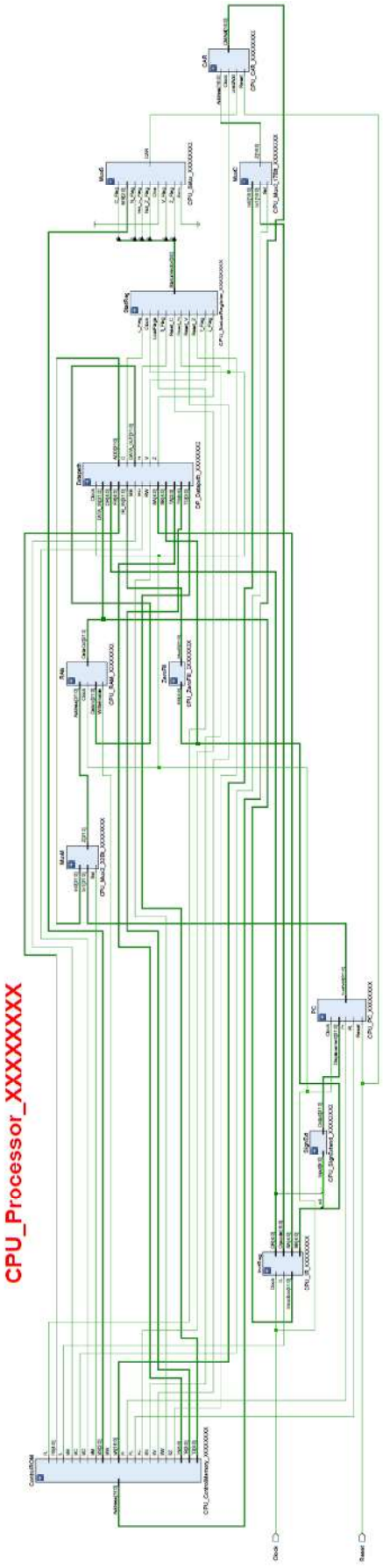
For more details see CPU_Processor_Test02_XXXXXXXX_Schematic01.pdf



For more details see CPU_Processor_Test03_XXXXXXXX_Schematic01.pdf



For more details see CPU_Processor_Test04_XXXXXXXX_Schematic01.pdf



For more details see CPU_Processor_XXXXXXXX_Schematic01.pdf

A detailed simulation procedure is coming soon!