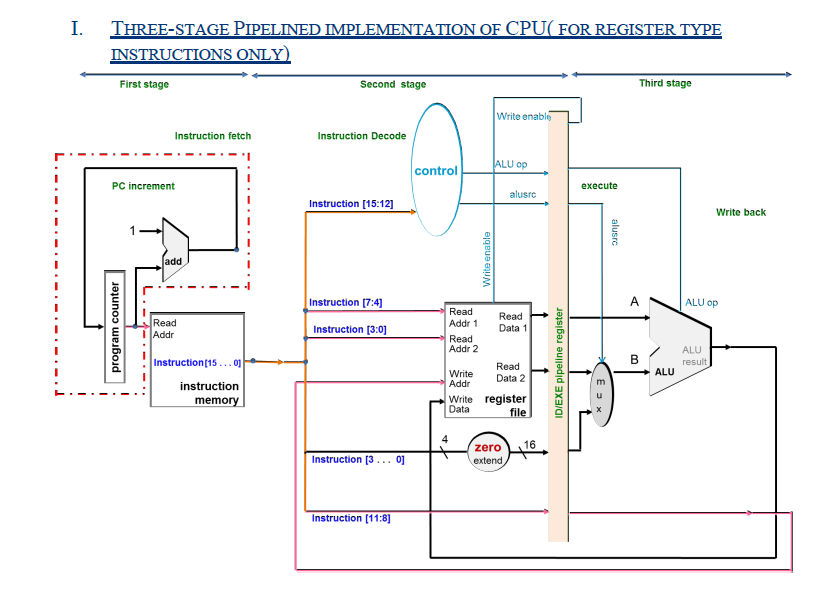
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SS3

CZ3001 Lab 3 Report

1. Explain the function of three-stage pipelined datapath with testbench for the execution of R-type instruction with the necessary RTL-block diagram.



The 3 stage pipeline allows the for fetch stage, decode stage and execute/write stage to run concurrently as different parts of the CPU is utilised for each process. The PC and instruction memory is used for fetch. The control unit and multiplexor is used for decode while the ALU is used for execute/write. This maximises CPU efficiency.

2. What modification you made for converting the datapath from R –type to be used for both R& I type? Explain the testbench output for the execution of R & I type instructions for three- stage pipelined datapath (clearly show the R and I type instructions in the testbench simulation)

In order to convert datapath from R -type to both R&I type, we need to sign extend ‘inst[3:0]’ to 16 bits.

3.Explain the function of four-stage pipelined R & I type datapath with the help of testbench output. (Clearly show the R & I instructionsin the test bench simulation for 4-

stage pipeline)

4.Synthesize the three-stage and four-stage pipelined R & I type CPU and find the number of slices and minimum period.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| CPU | BANDWIDTH | No. Of LUT slices | No. of registers | Minimum period in ns |
| Three-stage Pipelined CPU (R&I type) implementation | 16 | 642 | 330 | 8.103 |
| Four-stage Pipelined CPU implementation | 16 | 635 | 348 | 6.404 |

5. Justify the synthesis result.

The average period is lower for four-stage pipeline compared to three-stage pipeline because the execute/decode stage for the three-stage is broken into two parts (execute & decode). Each of these parts requires less time than both combined , resulting in the average period to decrease for four-stage pipeline to decrease. The