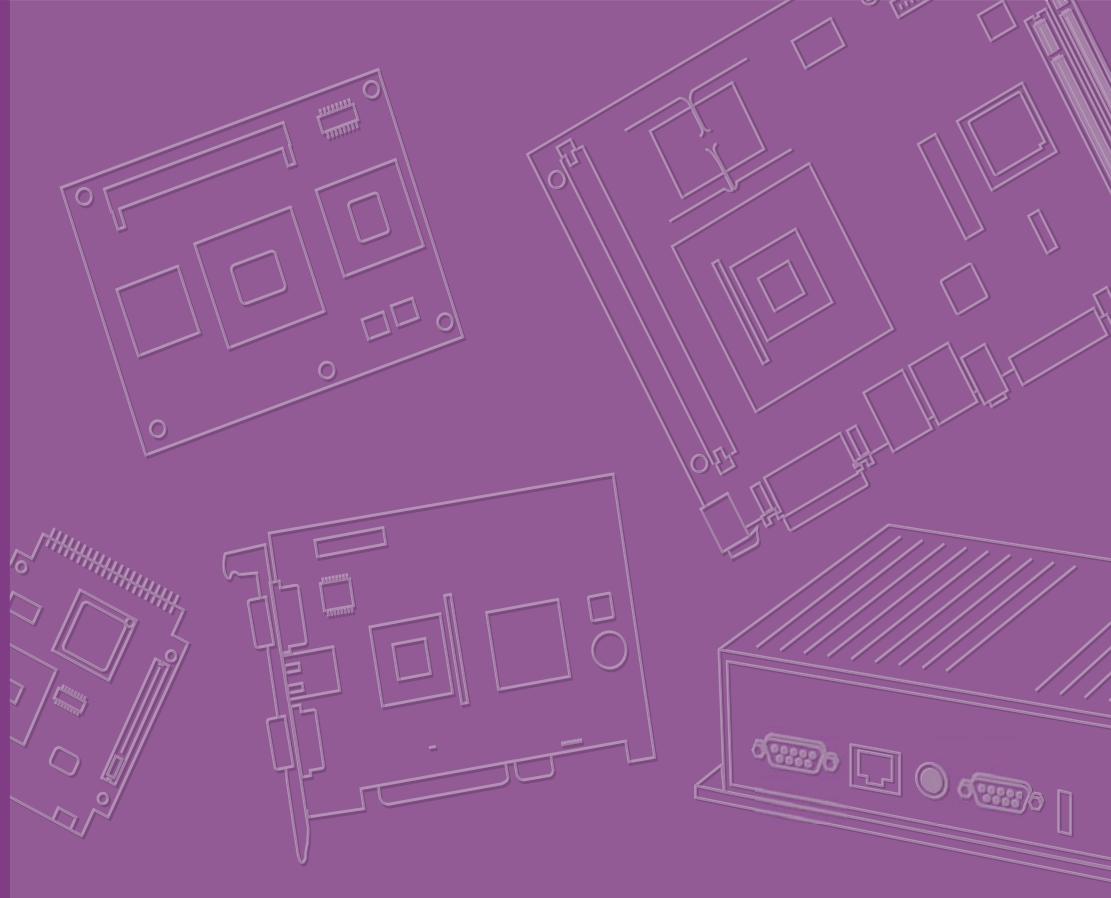


# User Manual



## AIMB-586

**Intel® Xeon® E3/Core™ i7/i5/i3  
LGA1151 MicroATX with HDMI / 2  
DP / eDP(LVDS), 6 COM, Quad  
LAN, DDR4, PCIe x 16, PCIe x 8  
and SATAIII, 4 x USB3.1(Gen2),  
6 USB 2.0, 2USB3.0**

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## CPU Compatibility

CPU Family	Power	Freq (GHz)	Mfg. Tech	HT	L2 cache	Smart cache (L3)	Package Type	Result	Supports Model
Intel Xeon E-2176G	80W	3.7G	14nm	Y	NA	12MB	LGA1151	PASS	WG2
Intel Xeon E-2124G	71W	3.4G	14nm	Y	NA	8MB	LGA1151	PASS	WG2
Intel i7-8700	65W	3.2G	14nm	Y	NA	12MB	LGA1151	PASS	QG2/L
Intel i7-8700T	35W	2.4G	14nm	Y	NA	12MB	LGA1151	PASS	QG2/L
Intel i5-8500	65W	3.0G	14nm	Y	NA	9MB	LGA1151	PASS	QG2/L
Intel I5-8500T	35W	2.1G	14nm	Y	NA	9MB	LGA1151	PASS	QG2/L
Intel i3-8100	65W	3.6G	14nm	-	NA	6MB	LGA1151	PASS	WG2/QG2/L
Intel I3-8100T	35W	3.1G	14nm	-	NA	6MB	LGA1151	PASS	WG2/QG2/L
Intel Pentium® Processor G5400	65W	3.7G	14nm	-	NA	4MB	LGA1151	PASS	WG2/QG2/L
Intel Pentium® Processor G5400T	35W	3.1G	14nm	-	NA	4MB	LGA1151	PASS	WG2/QG2/L
Intel Celeron® Processor G4900	65W	3.1G	14nm	-	NA	2M	LGA1151	PASS	QG2/WG2/L
Intel Celeron® Processor G4900T	35W	2.9G	14nm	-	NA	2M	LGA1151	PASS	QG2/WG2/L

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Because of Advantech's high quality-control standards and rigorous testing, most of our customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, you will be billed according to the cost of replacement materials, service time and freight. Please consult your dealer for more details.

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2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain an RMA (return merchandise authorization) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a fully-completed Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.
5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

# Ordering Information

P/N	Chipset	USB 3.1	USB 3.0	USB 2.0	DP/HDMI	eDP (LVDS)	GbE LAN	SATAIII	COM	PClex16	PClex8	PClex4	PClex1	M.2 E-key	M.2 M-key	TPM
AIMB-586QG2-00A1E	Q370	4	2	6+(2)	2/1**	1/(1)	2+(2)	6	1	(2)	1	1	1	1	1	(1)
AIMB-586WG2-00A1E	C246	4	2	6+(2)	2/1**	1/(1)	2+(2)	8	6	(1)	2	1	1	1	1	(1)
AIMB-586L-00A1E	H310	0	4	6+(2)	2/1	(1)/0	1***	4	2+(4)	1	0	1	0	0	0	(1)

\*() BOM options available on MP version.

\*\* HDMI 1.2 colay HDMI2.0 a (BOM option)

\*\*\* eDP can BOM option to LVDS

## Initial Inspection

Before you begin installing your motherboard, please make sure that the following materials have been shipped:

- 1 x AIMB-586 Intel LGA 1151 Xeon E3 & Core i7/i5/i3 Micro ATX Motherboard
- 2 x SATA HDD cable
- 2 x SATA Power cable
- 1 x I/O port bracket
- 1 x Startup manual
- 1 x Warranty card
- 2 x M.2 screws (QG2/WG2)

If any of these items are missing or damaged, contact your distributor or sales representative immediately. We have carefully inspected the AIMB-586 mechanically and electrically before shipment. It should be free of marks and scratches and in perfect working order upon receipt. As you unpack the AIMB-586, check it for signs of shipping damage. (For example, damaged box, scratches, dents, etc.) If it is damaged or it fails to meet the specifications, notify our service department or your local sales representative immediately. Also notify the carrier. Retain the shipping carton and packing material for inspection by the carrier. After inspection, we will make arrangements to repair or replace the unit.

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# **Chapter 1**

**General Information**

## 1.1 Introduction

AIMB-586 is designed with the Intel Q370/C246/H310 for industrial applications that require both performance computing and enhanced power management capabilities. The motherboard supports Xeon E-2124G/ E-2176G/ Core i7-8700/ Core i5-8500/ Core i3-8100/ Pentium G5400/ Celeron G4900 processor up to 12 MB L3 cache and DDR4 2666 MHz up to 64GB, per slot up to 16 GB. A rich I/O connectivity of 6 serial ports, 6 USB 2.0, 6 USB 3.1, up to quad GbE LAN, up to 8 SATA III ports.

## 1.2 Features

- **Rich I/O connectivity:** up to Quad GbE LAN via PCIe x1 bus, 1 x PCIe x16 slot (Gen 3) BOM option to 2 x PCIe x8 slot (Gen 3), 1 x PCIe x4 slot (Gen 3), 1 x PCIe x1 slot (Gen 3), 6 USB 2.0 ports and 6 USB 3.1 ports.
- **Standard Micro ATX form factor with industrial features:** The AIMB-586 is a full featured Micro ATX motherboard with balanced expandability and performance.
- **Wide selection of storage devices:** SATAIII HDD, customers benefit from the flexibility of using the most suitable storage device for larger capacity.
- **Optimized integrated graphic solution:** With Intel® Flexible Display Interface, it supports versatile display options and 32-bit 3D graphics engine.

## 1.3 Specifications

### 1.3.1 System

- **CPU:** Intel 8th generation Xeon E3 and Core i7/i5/i3 processor
- **BIOS:** AMI EFI 128 Mbit SPI BIOS
- **System chipset:** Intel® C246/Q370/H310
- **SATA hard disk drive interface:** On-board SATA connectors with data transmission rate up to 600 MB (QG2:6 / WG2:8 / L:4)

### 1.3.2 Memory

- **RAM:** Up to 64 GB in 4 slots 288-pin DIMM sockets. Supports dual-channel DDR4 2666/2400MHz SDRAM.
  - AIMB-586QG2 & AIMB-586L supports non-ECC unbuffered DIMMs and do not support any memory configuration that mixes non-ECC with ECC unbuffered DIMMs.
  - AIMB-586WG2 supports ECC & non-ECC buffered DIMMs.

### 1.3.3 Input/Output

- **PCIe slot:** 1 PCIe x16 expansion slot BOM option to 2 PCIe x 8 expansion slot, 1 PCIe x4 expansion slot, 1 PCIe x1 expansion slot
- **Serial port:** Six serial ports, one is RS-232/422/485 with hardware auto-flow control and five are RS-232. One DB-9 connectors located in rear panel are RS-232.
- **Keyboard and PS/2 mouse connector:** Two 6-pin mini-DIN connectors are located on the mounting bracket for easy connection to PS/2 keyboard and mouse.
- **USB port:** Supports up to 6 USB 2.0 ports with transmission rates up to 480 Mbps and 6 USB 3.1 ports with transmission rates up to 10 Gbps.

**Note!** 6 USB 3.1



4 ports in rear support to USB 3.1 (gen2);

2 ports on board support to USB 3.1 (gen1)

- **GPIO:** AIMB-586 supports 16-bit GPIO from super I/O for general purpose control application.

### 1.3.4 Graphics

- **Controller:** Intel® HD Graphics
- **Display memory:** 1 GB maximum shared memory with 2GB and above system memory installed
- **HDMI:** Supports HDMI 1.2 1920x1200@60Hz (colay HDMI2.0a 4096x2160 @60Hz)
- **Display Port:** 2, Supports max resolution 4096 x 2304 @60Hz
- **eDP:** Support max resolution 3840 x 2160 @ 60Hz (BOM option to LVDS)
- **Triple Display:** HDMI + eDP (LVDS)+ DP, DP+eDP (LVDS)+ DP, HDMI+DP+DP
- **Dual Display:** HDMI+eDP (LVDS), HDMI+DP, eDP (LVDS) + DP, DP+ DP

### 1.3.5 Ethernet LAN

- Supports up to quad 10/100/1000 Mbps Ethernet port (s) via PCI Express x1 bus which provides 500 MB/s data transmission rate
- **Controller:** LAN1: Intel I219LM; LAN2:Intel I211AT/Intel I210AT(WG2); LAN3/ LAN4: Realtek 8111G

### 1.3.6 Industrial features

- **Watchdog timer:** Can generate a system reset. The watchdog timer is programmable, with each unit equal to one second or one minute (255 levels)

### 1.3.7 Mechanical and environmental specifications

- **Operating temperature:** 0 ~ 60° C (32 ~ 140° F, Depending on CPU)
- **Storage temperature:** -40 ~ 85° C (-40 ~ 185° F)
- **Humidity:** 5 ~ 95% non-condensing
- **Power supply voltage:** +3.3 V, +5 V, +12 V, -12 V, 5 Vsb
- **Power consumption:**  
LAG1151 Core i7-8700 3.4 GHz, 12MB L3 Cache, 4pcs 8GB DDR4 2666MHz memory  
+5 V      3.3 V      12 V      5 Vsb      -12 V

1.6 A    0.47 A    0.365 A    0 A    0 A

Measure the maximum current value which system under maximum load (CPU: Top speed, RAM & Graphic: Full loading)

- **Board size:** 244 mm x 244 mm (9.6" x 9.6")
- **Board weight:** 0.365 kg

## 1.4 Jumpers and Connectors

Connectors on the AIMB-586 motherboard link it to devices such as hard disk drives and a keyboard. In addition, the board has a number of jumpers used to configure your system for your application.

The tables below list the function of each of the board jumpers and connectors. Later sections in this chapter give instructions on setting jumpers. Chapter 2 gives instructions for connecting external devices to your motherboard.

**Table 1.1: Jumpers**

Label	Function
JFP1	Power Switch/ Reset/ External Speaker/ SATA HDD LED/ SMBus connector
JFP2	Power LED/ Keyboard Lock
JSETCOM2	Serial port:RS232/RS422/RS485 jumper setting
JCMOS1	CMOS clear (default 1-2 pin)
JCASE1	Case open connector
JEDP1	eDP power jumper
JIR1+JOBS1 +JWDT1	Jumper for CIR/Watchdog/OBS
JUSBPWR2	USB power selection for USB0910, USB1112, USB1314
JUSBPWR1	USB power selection for LAN1_USB12, LAN2_USB34, USB5678

**Table 1.2: Connectors**

Label	Function
COM1	Serial Port 1 (RS-232)
COM2	Serial Port COM2, pin header 2 x 5, COM2 supports RS232/422/485
COM3/4/5/6	Serial port: COM 3/4/5/6, box header 2x 20
HDMI	HDMI connector
DP	DP connector
LAN1_USB12	LAN1 & USB12 Connector
LAN2_USB34	LAN2 & USB34 Connector
LANLED1	Front Panel LAN Indicator connector
USB5/6/7/8	USB port 5-8
USB1112/1314	USB1112 (internal 2 x 5 pin header on board); USD1314 (internal 2 x 10 pin header on board)
USB9/10	USB 9/10 from Renesas (internal 2 x 10 pin header on board) (Optional)
SATA1-8	Serial III ATA connector
CPUFAN1	CPU FAN connector (4 pin)
SYS-FAN1/2/3/4	System FAN Power Connector (4 pin) (Fan3/Fan4 Optional)

eDP1	eDP connector (2 x 20 pin header)
KBMS1	On board external keyboard and Mouse connector
AUDIO1	Line Out, Mic IN connector
FPAUDIO1	Front Panel audio connector (FP_AU-DIO)
PSON1	AT(1-2) / ATX (2-3) (Default 2-3)
SPI_CN1	SPI flash programming connector
GPIO1	GPIO pin header (SMD pitch=2.0 mm)
SMBUS1	SMBUS expansion pin header 1 x 4 p
ATX12V1	ATX 4pin 12V Auxiliary power connector
EATXPWR1	ATX 24pin power connector
INV1	ePD inverter
VOLT1	Voltage Display connector
SPDIF1	Digital Audio connector 4 x 1 header pitch = 2.54 mm
LPC1	Low pin count interface (2 x 7 pin header)

## 1.5 Board layout: Jumper and Connector Locations

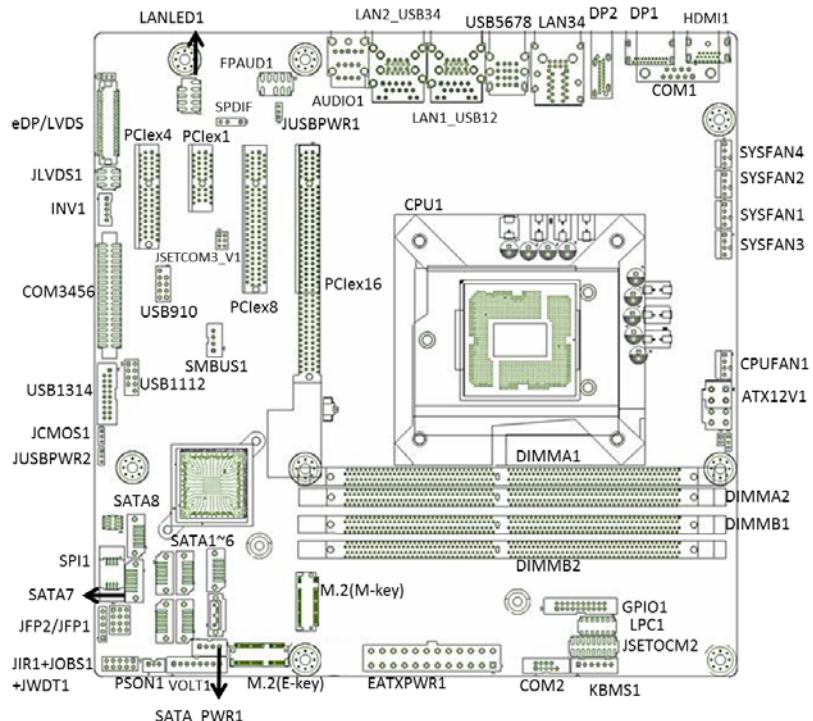


Figure 1.1 Jumper and Connector Location

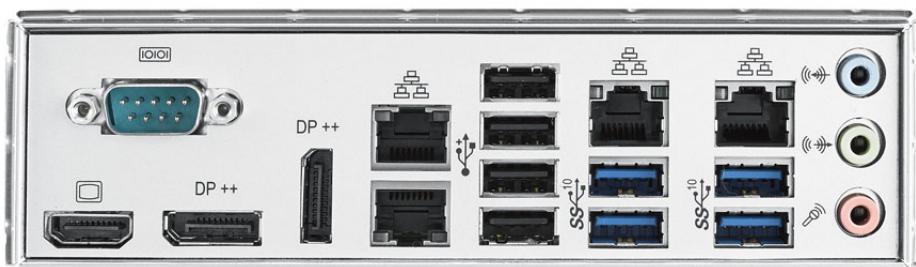


Figure 1.2 I/O Connectors

## 1.6 AIMB-586 Board Diagram

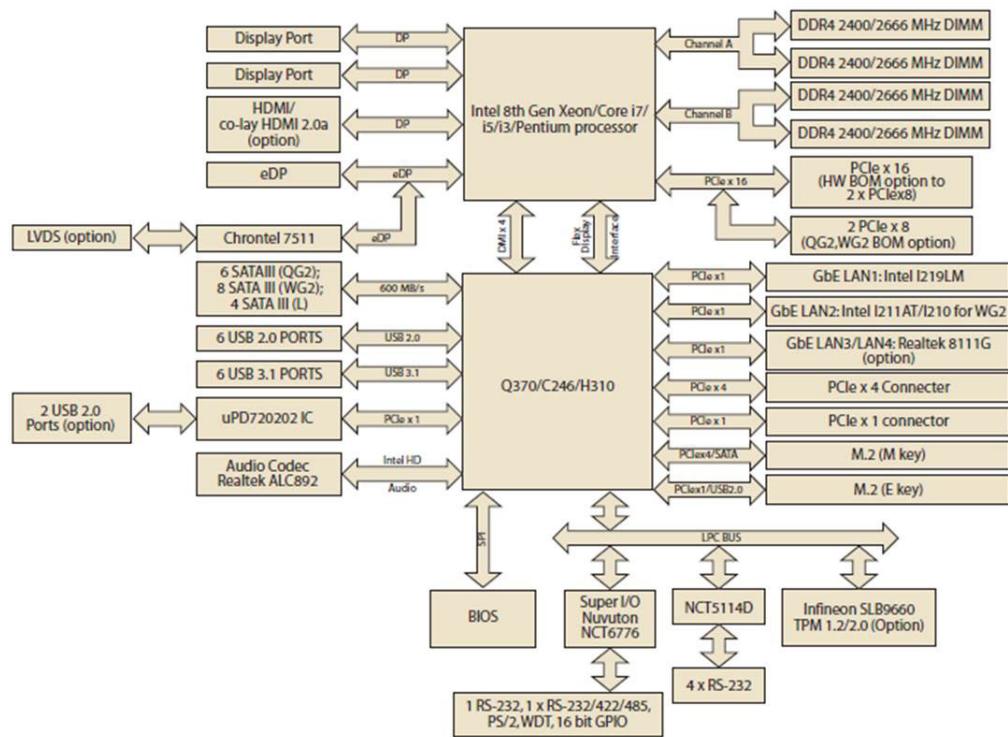


Figure 1.3 AIMB-586 Block Diagram

## 1.7 Safety Precautions

**Warning!** Always completely disconnect the power cord from chassis whenever you work with the hardware. Do not make connections while the power is on. Sensitive electronic components can be damaged by sudden power surges. Only experienced electronics personnel should open the PC chassis.

**Caution!** Always ground yourself to remove any static charge before touching the motherboard. Modern electronic devices are very sensitive to electrostatic discharges. As a safety precaution, use a grounding wrist strap at all times. Place all electronic components on a static-dissipative surface or in a static-shielded bag when they are not in the chassis.

**Caution!** The computer is provided with a battery-powered real-time clock circuit. There is a danger of explosion if battery is incorrectly replaced. Replace only with same or equivalent type recommended by the manufacturer. Discard used batteries according to manufacturer's instructions.

**Caution!** There is a danger of a new battery exploding if it is incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.

## 1.8 Jumper Settings

This section provides instructions on how to configure your motherboard by setting the jumpers. It also includes the motherboards's default settings and your options for each jumper.

### 1.8.1 How to Set Jumpers

You can configure your motherboard to match the needs of your application by setting the jumpers. A jumper is a metal bridge that closes an electrical circuit. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To "close" (or turn ON) a jumper, you connect the pins with the clip. To "open" (or turn OFF) a jumper, you remove the clip. Sometimes a jumper consists of a set of three pins, labeled 1, 2, and 3. In this case you connect either pins 1 and 2, or 2 and 3. A pair of needle-nose pliers may be useful when setting jumpers.

## 1.8.2 CMOS Clear (CMOS1)

The AIMB-586 motherboard contains a jumper that can erase CMOS data and reset the system BIOS information. Normally this jumper should be set with pins 1-2 closed. If you want to reset the CMOS data, set CMOS1 to 2-3 closed for just a few seconds, and then move the jumper back to 1-2 closed. This procedure will reset the CMOS to its default setting.

**Table 1.3: CMOS1**

Function	Jumper Setting
*Keep CMOS data	
Clear CMOS data	

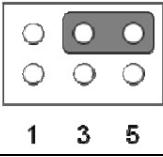
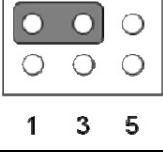
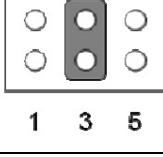
\* Default

## 1.8.3 JEDP1: eDP Power 3.3 V/ 5 V/ 12 V Selector

**Table 1.4: JeDP1: eDP Power 3.3 V/5 V/ 12 V Selector**

Closed Pins	Result
*JEDP1, 4-6	Jumper for +3.3 V
EDP1, 2-4	Jumper for +V5
JEDP1, 3-4	Jumper for +12 V

\*Default

Jumper position for +3.3V (Default)	
Jumper position for +5V	
Jumper position for +12V	

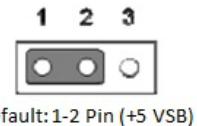
### 1.8.4 JUSBPWR1-2 (USB Power Selection Connector)

JUSBPWR1: selection for LAN1\_USB12, LAN2\_USB34, USB5678

JUSBPWR2: selection for USB910,USB1112,USB1314

**Table 1.5: JUSBPWR1-2 (USB Power Selection Connector)**

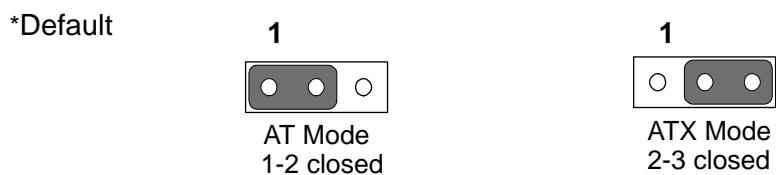
Pin	Pin Name
1	+V5_Vsb
2	+V5_USB
3	+V5



### 1.8.5 PSON1: ATX, AT Mode Selector

**Table 1.6: PSON1: ATX, AT Mode Selector**

Closed Pins	Result
1-2	AT Mode
2-3*	ATX Mode

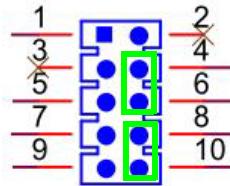


### 1.8.6 JIR1+JOB1+JWD1: Watchdog Timer Output, OBS Alarm Option, and CIR interface

**Table 1.7: JIR1+JOB1+JWD1: Watchdog Timer Output and OBS Alarm Connector**

Pin	Pin Name
1	+V5
2	NC
3	NC
4	Watch dog reset# output
5	IRRX
6	System reset input#
7	GND
8	SIO Warning Beep output
9	IRTX
10	SP1 Buzzer Beep input

Note: Watch dog time-out reset# (4-6 short) / SIO Warning Beep enable (8-10 short)



### 1.8.7 JSETCOM2: COM2 RS232, RS422, RS485 Selection

**Table 1.8: COM2 RS232, RS422, RS485 Selection**

Pin	Signal	Pin	Signal
1	UART_SIN [2]	2	RXD_RS485
3	UART_SIN [2]	4	RXD_RS422
5	UART_SIN [2]	6	RXD_RS232
7	DCDB	8	SOUT [2]
9	COM2_DCD#	10	COM2_SOUT
11	COM2_RXD485-	12	COM2_RXD485+
13	SIN [B]	14	DTR [B]
15	COM2_SIN	16	COM2_DTR#
17	COM2_RXD485+	18	COM2_RXD485-

RS-232 Mode (Default)									
2	4	6	8	10	12	14	16	18	
1	3	5	7	9	11	13	15	17	
RS-422 Mode									
2	4	6	8	10	12	14	16	18	
1	3	5	7	9	11	13	15	17	
RS-485 Mode									
2	4	6	8	10	12	14	16	18	
1	3	5	7	9	11	13	15	17	

### 1.8.8 JCASE1: Case Open Sensor

The AIMB-586 motherboard contains a jumper that provides a chassis open sensor. The buzzer on the motherboard beeps when the case is opened.

### 1.8.9 JCASEOP\_SW1: Case Open Selection Pin Header

**Table 1.9: JCASEOP\_SW1: Case Open Selection Pin Header**

Closed Pins	Result
1-2	Normal Mode
2-3*	Normal Open (Default)
*Default	

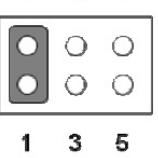
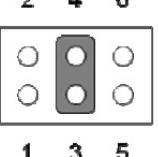
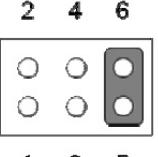


1  
Normal Close  
1-2 closed



1  
Normal Open (Default)  
2-3 closed

### 1.8.10 JSETCOM1\_V1: COM1\_RI# Pin RI# / 5V / 12V

Jumper position for RI# (Default)	 <p>2 4 6 1 3 5</p>
Jumper position for +5V	 <p>2 4 6 1 3 5</p>
Jumper position for +12V	 <p>2 4 6 1 3 5</p>

## 1.9 System Memory

AIMB-586 has four 288-pin memory sockets for 2666/2400 MHz memory modules with maximum capacity of 64 GB (Maximum 16 GB for each DIMM). AIMB-586QG2/L supports only non-ECC DDR4 memory modules and do not support registered DIMMs (RDIMMs). AIMB-586WG2 can support ECC/non-ECC DDR4 memory module.

## 1.10 Memory Installation Procedures

To install DIMMs, first make sure the two handles of the DIMM socket are in the “open” position, i.e., the handles lean outward. Slowly slide the DIMM module along the plastic guides on both ends of the socket. Then firmly but gently (avoid pushing down too hard) press the DIMM module well down into the socket, until you hear a click when the two handles have automatically locked the memory module into the correct position of the DIMM socket. To remove the memory module, just push both handles outward, and the memory module will be ejected by the mechanism.

---

## **1.11 Cache Memory**

The AIMB-586 supports a CPU with one of the following built-in full speed L3 caches:

12MB for Intel Xeon E-2176G

8MB for Intel Xeon E-2124G

12MB for Intel Core i7 8700

12MB for Intel Core i7 8700T

9MB for Intel Core i5 8500

9MB for Intel Core i5 8500T

6MB for Intel Core i3 8100

6MB for Intel Core i3 8100T

4MB for Intel Pentium G5400/G5400T

2MB for Intel Celeron G4900/G4900T

The built-in second-level cache in the processor yields much higher performance than conventional external cache memories.

## **1.12 Processor Installation**

The AIMB-586 is designed for LGA1151, Intel Xeon and Intel Core i7/Core i5/Core i3/Pentium/Celeron processor.

# Chapter 2

Connecting  
Peripherals

## 2.1 Introduction

You can access most of the connectors from the top of the board as it is being installed in the chassis. If you have a number of cards installed or have a packed chassis, you may need to partially remove the card to make all the connections.

## 2.2 USB Ports (LAN1\_USB12/LAN2\_USB34/LAN3/LAN4/USB5678/USB910/USB1112/USB1314)

The AIMB-586 provides up to 14 USB ports. The USB interface complies with USB Specification Rev 2.0 supporting transmission rates up to 480 Mbps and Rev 3.0 supporting transmission rate up to 5 Gbps, Rev 3.1 Gen2 supporting transmission rate up to 10 Gbps and is fuse protected. The USB interface can be disabled in the system BIOS setup. (Note: Per Intel EDS specification, once CNVI M.2 WIFI Module is inserted, then USB12 Port will not work.)

The AIMB-586 is equipped with up to four high-performance 1000 Mbps Ethernet LAN adapters, both of which are supported by all major network operating systems. The RJ-45 jacks on the rear panel provides convenient LAN connection.

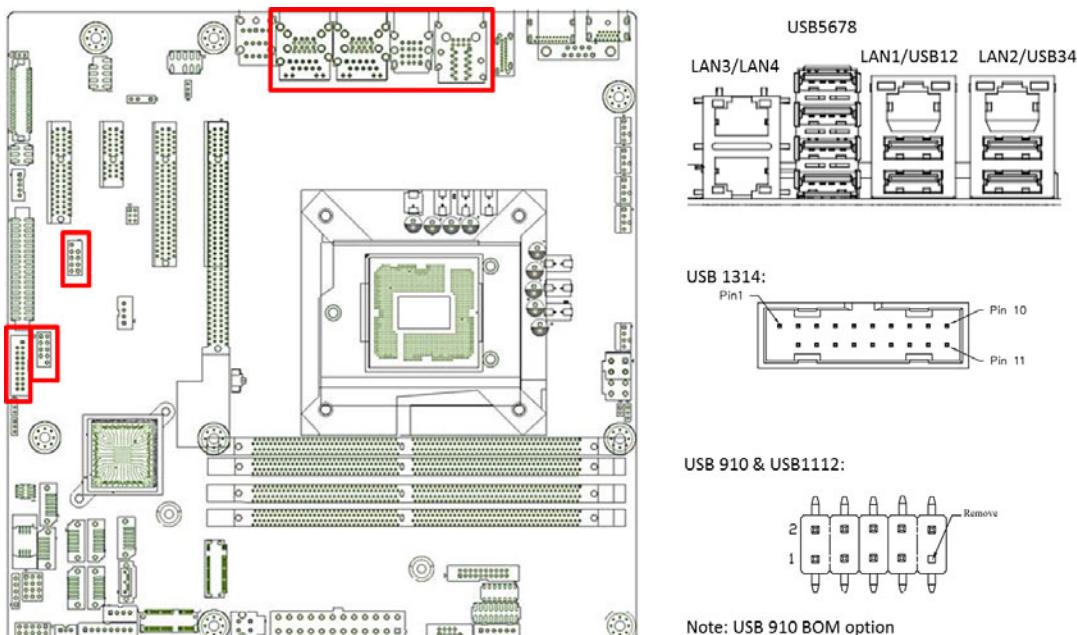
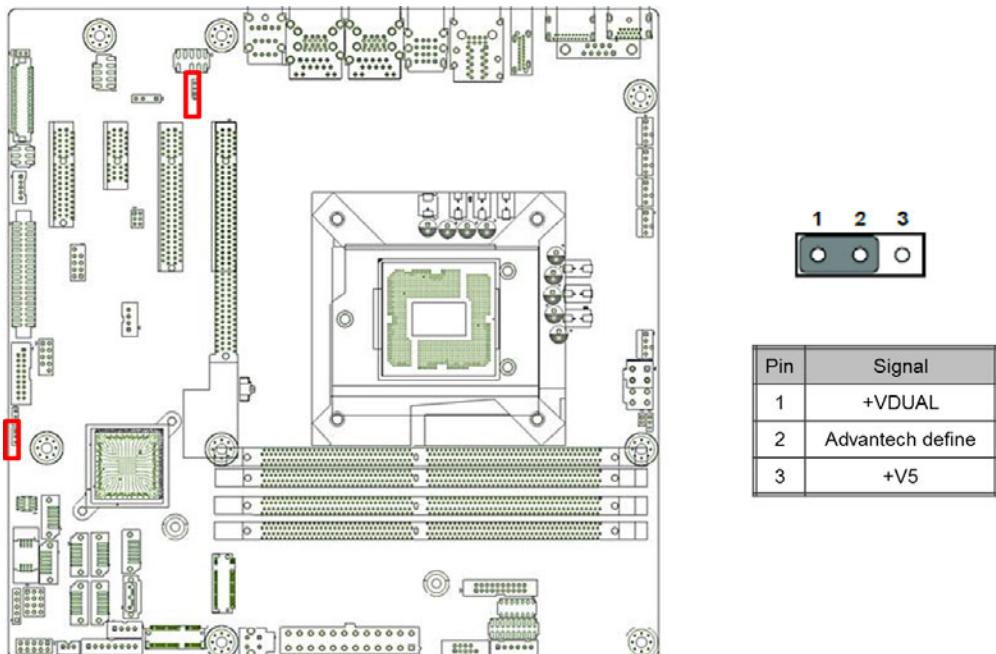


Table 2.1: LAN LED Indicator

LAN Mode	LAN Indicator
LAN1/LAN2 indicator	LED1 (Right) off for mal-link; Link (On) / Active (Flash)
	LED2 (Left) 100 Mbps (On) / 10 Mbps (Off); Color: Orange
	LED2 (Left) 1000 Mbps (On); Color: Green
LAN3/LAN4 indicator	LED1 (Right) off for mal-link; Link (On) / Active (Flash)
	LED2 (Left) 100 Mbps (On) / 10 Mbps (Off); Color: Orange
	LED2 (Left) 1000 Mbps (On); Color: Green

## 2.3 USB Power Switch (JUSBPWR1/JUSBPWR2)

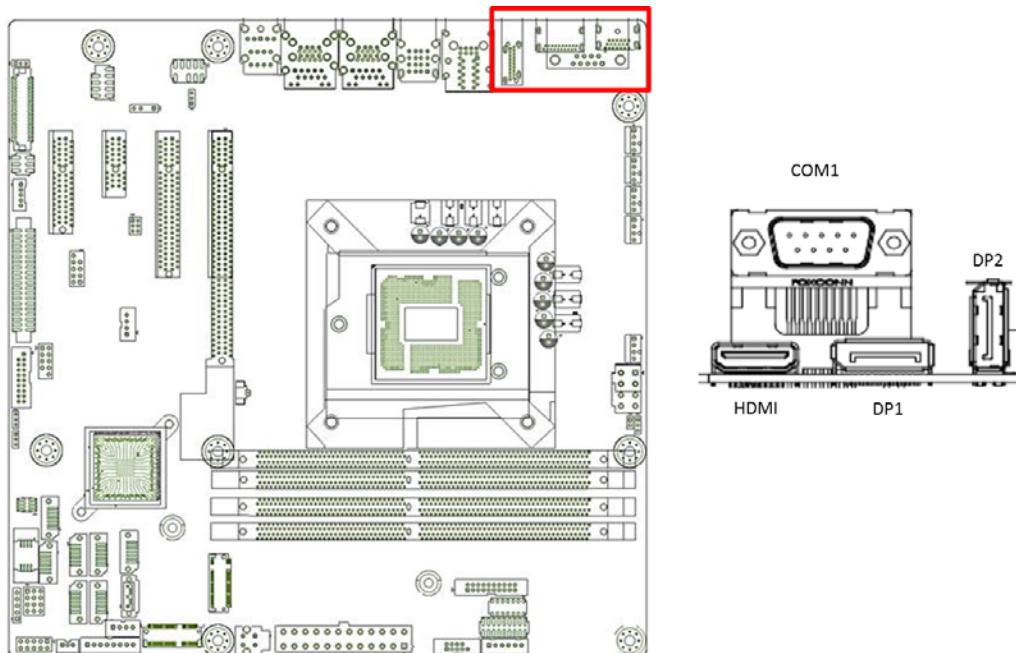
AIMB-586 allows users to set USB power between +5 VSB and +5 V. When the jumper is set as +5 V (default 2-3 pin), the board doesn't support wake from S3 via keyboard or mouse. If you need to set it to +5 Vsb, you need to modify the jumper (1-2 pin). There is another way to control USB power by GPIO. But this kind of behavior need to apply BOM option by HW design. Each GPIO can control all rear USB ports or all USB ports on board pin header.



**Note!** When USB power is switched to +5V, it can't be connected with power KVM.



## 2.4 COM1/HDMI/DP1/DP2 Connector



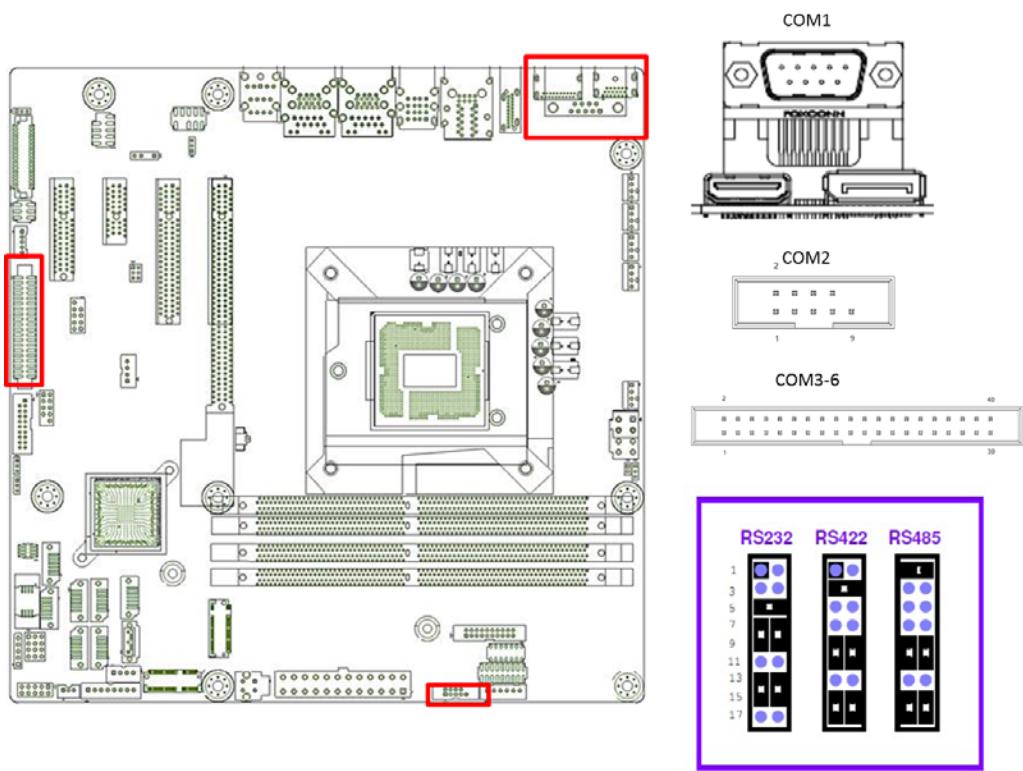
AIMB-586 includes COM1 and HDMI, DP interfaces that can drive conventional COM1 and HDMI, DP displays. COM1 is a standard 9-pin connector support RS-232. Pin assignments for COM1 and HDMI, DP connectors are detailed in Appendix B.

DP max resolution support to 4096 x 2304 @ 60 Hz

HDMI default is support to HDMI 1.2.

Can do BOM option to support HDMI 2.0a (4096 x 2160 @ 60 Hz)

## 2.5 Serial Ports (COM1~COM6)



COM2 RS232/422/485 Jumper setting

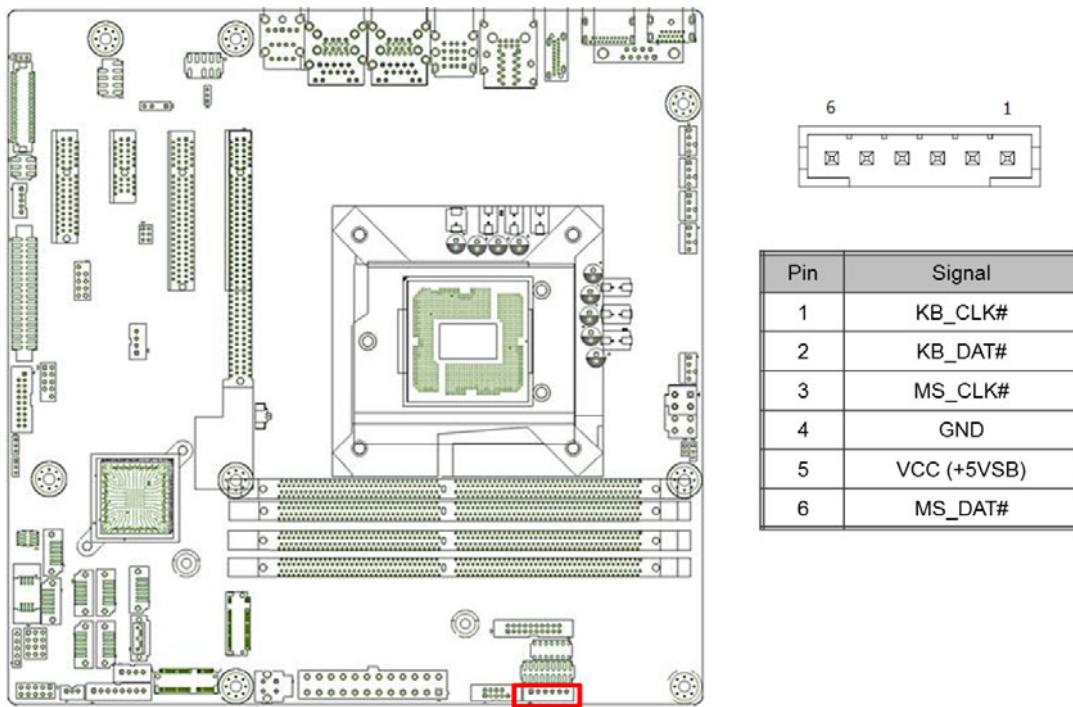
AIMB-586 supports six serial ports. COM1, COM2, COM4-6 supports RS-232. COM2 supports RS-232/422/485 (with 5V/12V power). JSETCOM2 is used to select the RS-232/422/485 mode for COM2.

These ports can connect to serial devices, such as a mouse or a printer, or to a communications network.

The IRQ and address ranges for both ports are fixed. However, if you want to disable the port or change these parameters later, you can do this in the system BIOS setup.

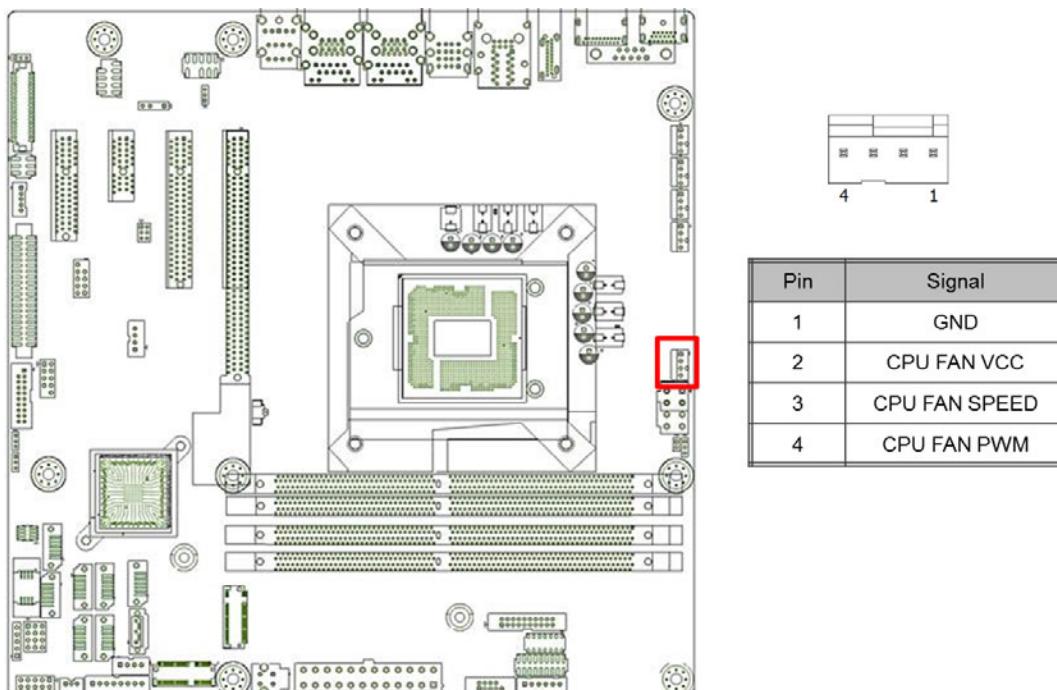
Different devices implement the RS-232 standards in different ways. If you have problems with a serial device, be sure to check the pin assignments for the connector.

## 2.6 PS/2 Keyboard and Mouse Connector



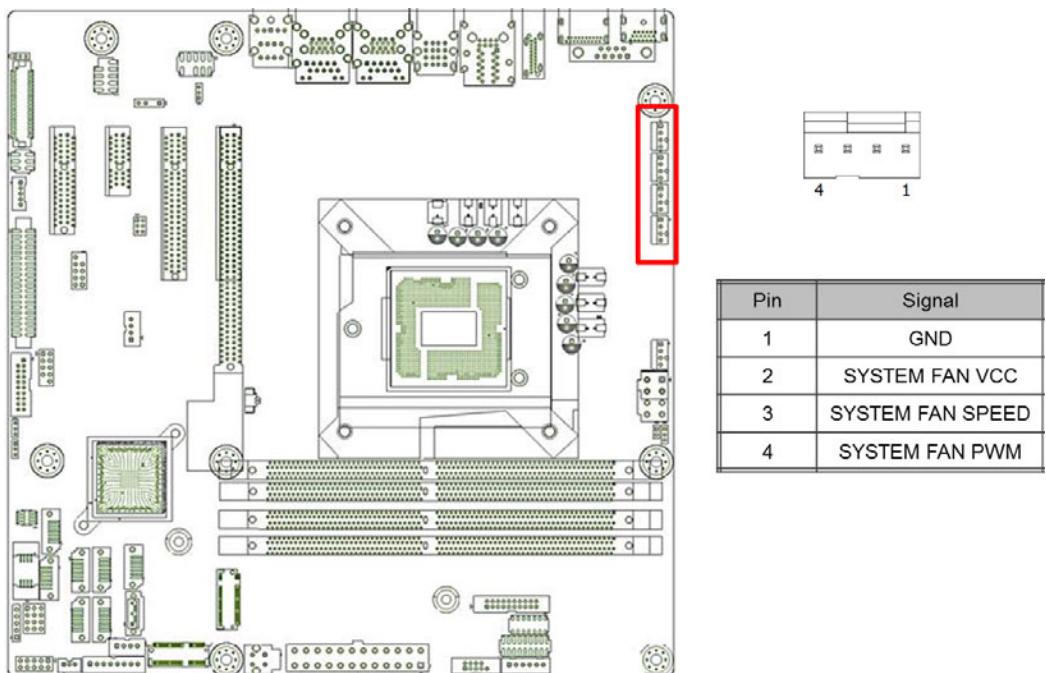
6-pin mini-DIN connectors (KBMS1, 2.54pitch) is for supporting the PS/2 keyboard and PS/2 mouse by a cable P/N 1700018699.

## 2.7 CPU Fan Connector (CPU\_FAN1)



If a fan is used, this connector supports cooling fans of 1500 mA (18 W) or less.

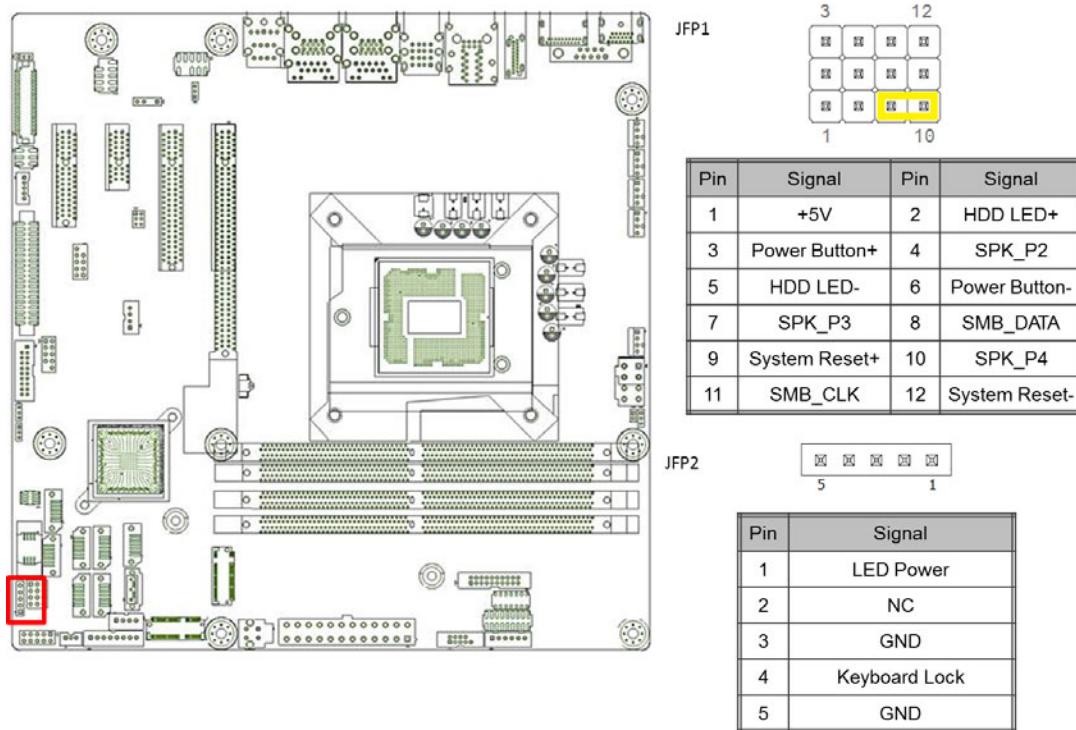
## 2.8 System FAN Connector (SYSFAN1/2/3/4)



If a fan is used, this connector supports cooling fans of 1500 mA (18 W) or less. Default only with System fan 1 & System fan 2. System fan 3 and System fan 4 are BOM optional. Please notice that, system fan 3 and system fan 4 can't be read rotational speed in BIOS. And system fan 3 will be controlled with system fan 1, system fan 4 will be controlled with system fan 2.

## 2.9 Front Panel Connectors (JFP1/JFP2)

There are several headers for monitoring and controlling the AIMB-586.



### 2.9.1 ATX soft power switch (JFP1/PWR\_SW)

If your computer case is equipped with an ATX power supply, you should connect the power on/off button on your computer case to (JFP1/ PWR\_SW), for convenient power on and off.

### 2.9.2 Reset (JFP1/RESET)

Many computer cases offer the convenience of a reset button. Connect the wire for the reset button.

### 2.9.3 HDD LED (JFP1/HDDLED)

You can connect an LED to connector (JFP1/HDDLED) to indicate when the HDD is active.

### 2.9.4 External speaker (JFP1/SPEAKER)

JFP2/SPEAKER is a 4-pin connector for an external speaker. If there is no external speaker, the AIMB-586 provides an onboard buzzer as an alternative. To enable the buzzer, set pins 7 & 10 as closed.

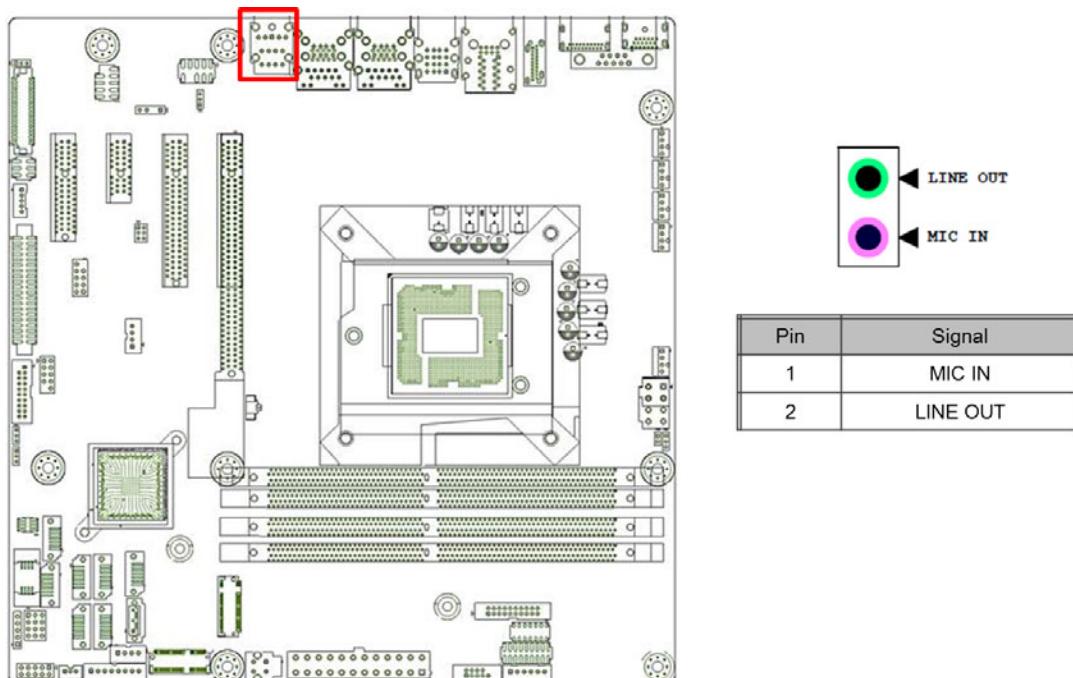
## 2.9.5 Power LED and keyboard lock connector (JFP2/PWR\_LED & KEY LOCK)

(JFP2/PWR\_LED & KEY LOCK) is a 5-pin connector for the power on LED and Key Lock function. Refer to Appendix B for detailed information on the pin assignments. The Power LED cable should be connected to pin 1-3. The key lock button cable should be connected to pin 4-5. There are 3 modes for the power supply connection. The first is “ATX power mode”; the system turns on/off by a momentary power button. The second is “AT Power Mode”; the system turns on/off via the power supply switch. The third is another “AT Power Mode” which makes use of the front panel power switch. The power LED status is indicated in the following table:

**Table 2.2: ATX Power Supply LED Status (No support for AT power)**

Power mode	LED (ATX Power Mode) (On/off by momentary button)	LED (AT power Mode) (On/off by switching power supply)	LED (AT power Mode) (On/off by front panel switch)
PSON1 (on back plane) jumper setting	pins 2-3 closed	pins 1-2 closed	Connect pins 1 & 2 to panel switch via cable
System On	On	On	On
System Off	Off ( Windows 7) Slow Flashes (Window 8)	Off	Off
S3	Fast flashes	N/A	N/A
S4	Slow flashes	N/A	N/A

## 2.10 Line Out, Mic In Connector (AUDIO1)



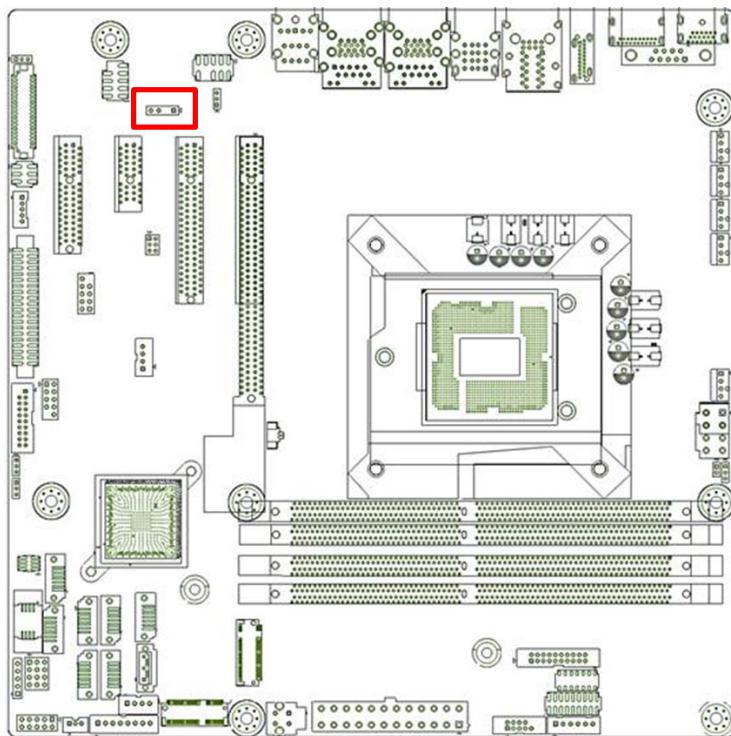
**Note!** Note: default audio support 2 ports.

But can BOM option to support 3 ports.(line-in/line out/ Mic in)



## 2.11 Digital Audio Connector (SPDIF\_OUT1)

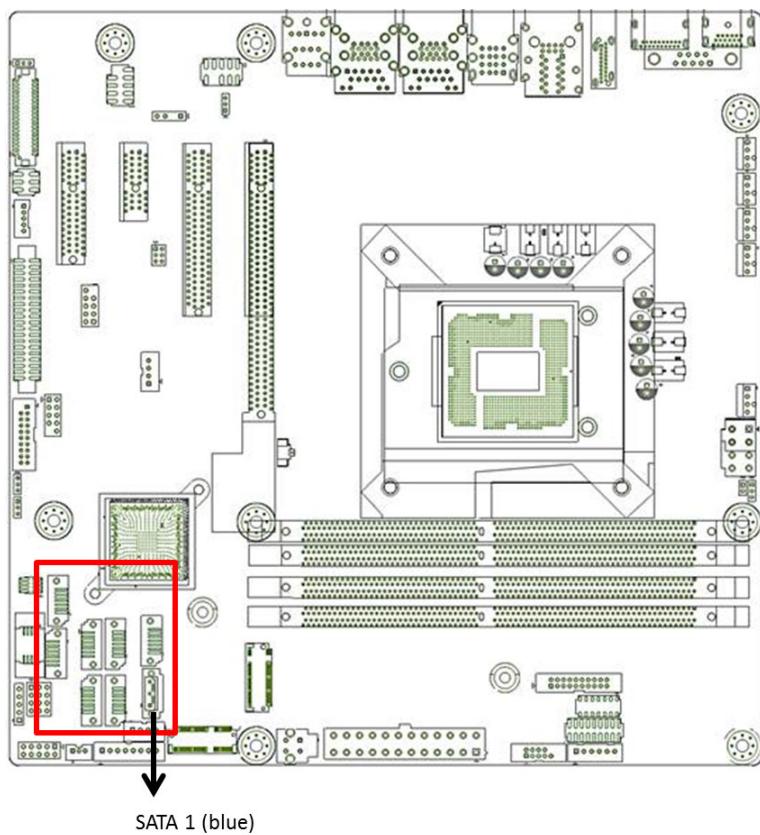
This connector is for the S/PDIF audio module to allow digital output sound. Connect one end of the S/PDIF audio cable to this connector and the other end to the S/PDIF module.



**Note!** The S/PDIF module should be purchased separately by end user.



## 2.12 Serial ATA Interface (SATA1 ~ SATA8)



AIMB-586 features a high performance Serial ATA III interface (up to 600 MB/s) which eases hard drive cabling with thin, space-saving cables. In QG2,WG2 sku, SATA1 colay with M.2 E-key SATA interface.

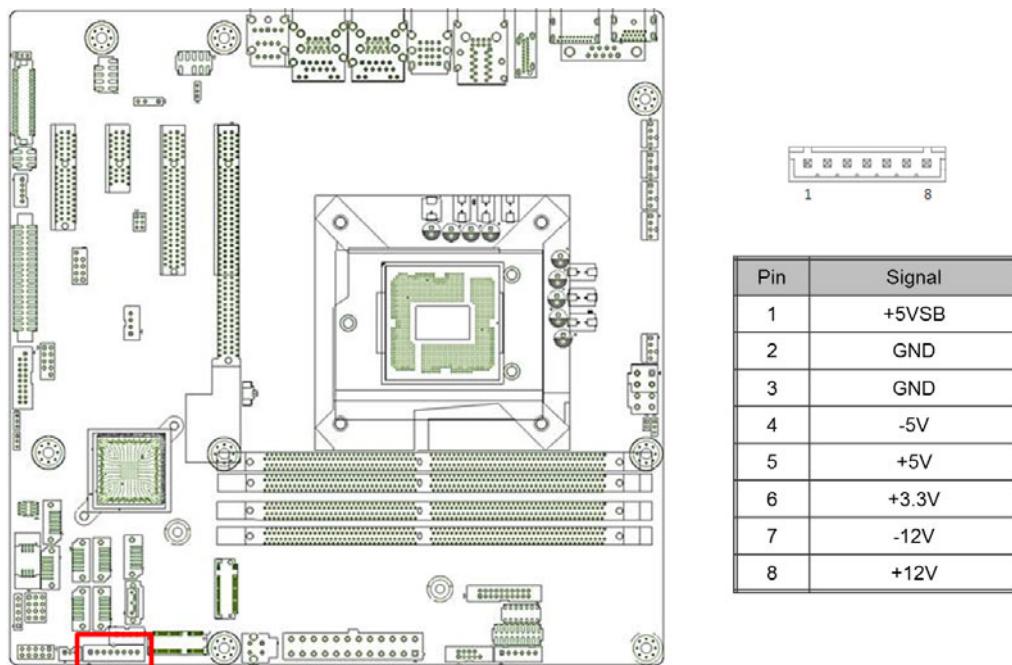
If M.2 E-key with PCIe interface, SATA1 can be used normally.

- AIMB-586QG2-00A1E: support SATA 1~ SATA6
- AIMB-586WG2-00A1E: support SATA 1~ SATA8
- AIMB-586L-00A1E: support SATA1~SATA4

**Note!** QG2, WG2 sku can support Intel RAID.

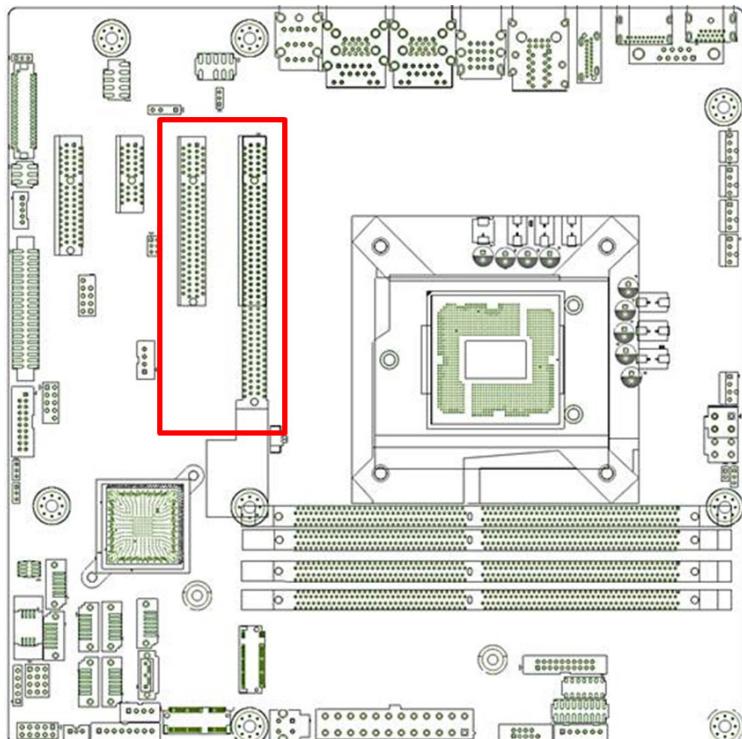


## 2.13 8-pin Alarm Board Connector (VOLT1)



VOLT1 connects to the alarm board on the chassis. These alarm boards give warnings if a power supply or fan fails, or if the chassis overheats.

## 2.14 PCI Express x16 Slot / PCI Express x 8



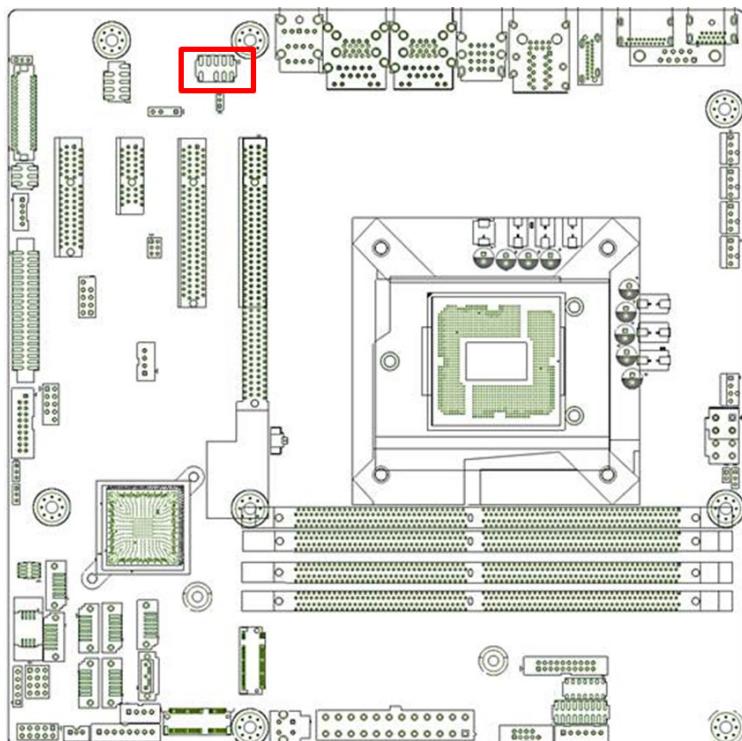
AIMB-586 provides a PCIe x16 slot ,which can BOM option to 2 PCIe x8 for users to install add-on cards when their applications require higher graphic performance than the CPU embedded graphics controller can provide.

**Note!** BOM option to 2 PCIe x8, When PCIe x8 slot is used, PCIe x16 slot only supports x8 bandwidth.



## 2.15 Front Panel Audio Connector (FPAUD1)

This connector is for a chassis-mounted front panel audio I/O module that supports either HD Audio or legacy AC'97 (optional) audio standard. Connect this connector with the front panel audio I/O module cable.

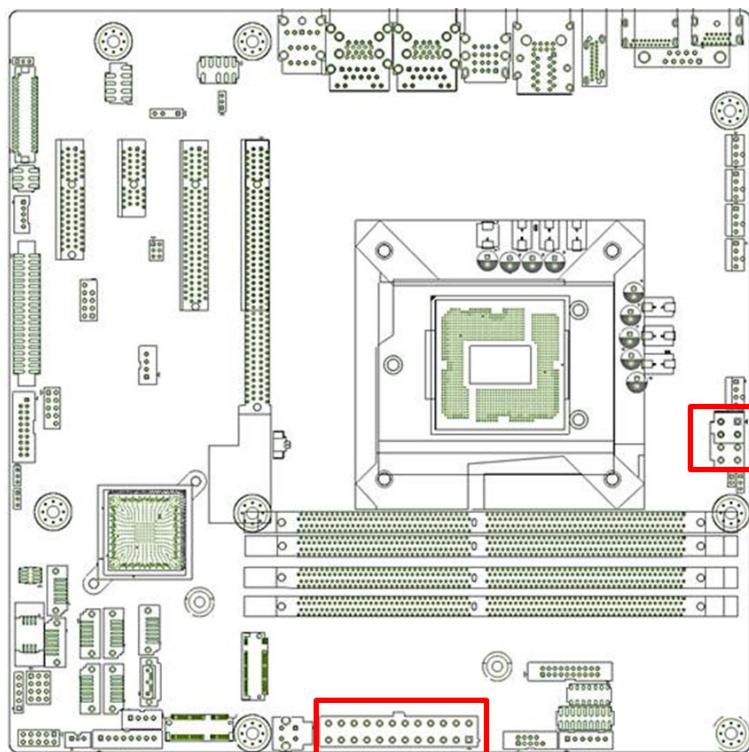


**Note!** For motherboards with the optional HD Audio feature, we recommend that you connect a high-definition front panel audio module to this connector to take advantage of the motherboard's high definition audio capability.



## 2.16 ATX Power Connector (EATXPWR1, ATX12V1)

This connector is for an ATX Micro-Fit power supply. The plugs from the power supply are designed to fit these connectors in only one direction. Determine the proper orientation and push down firmly until the connectors mate completely.

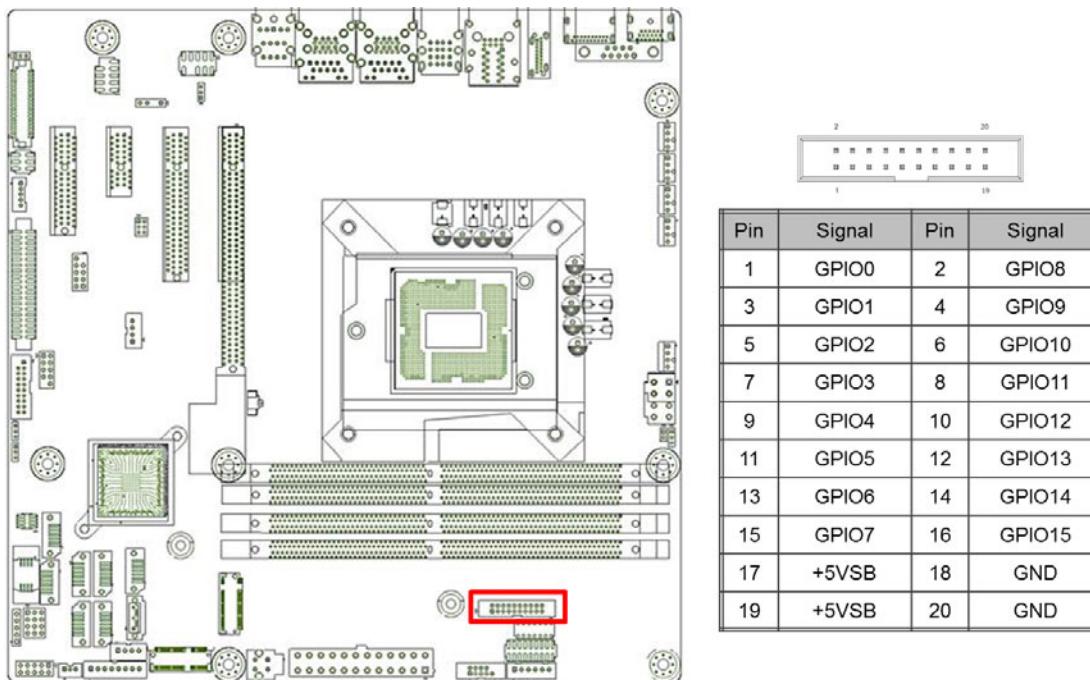


**Note!**

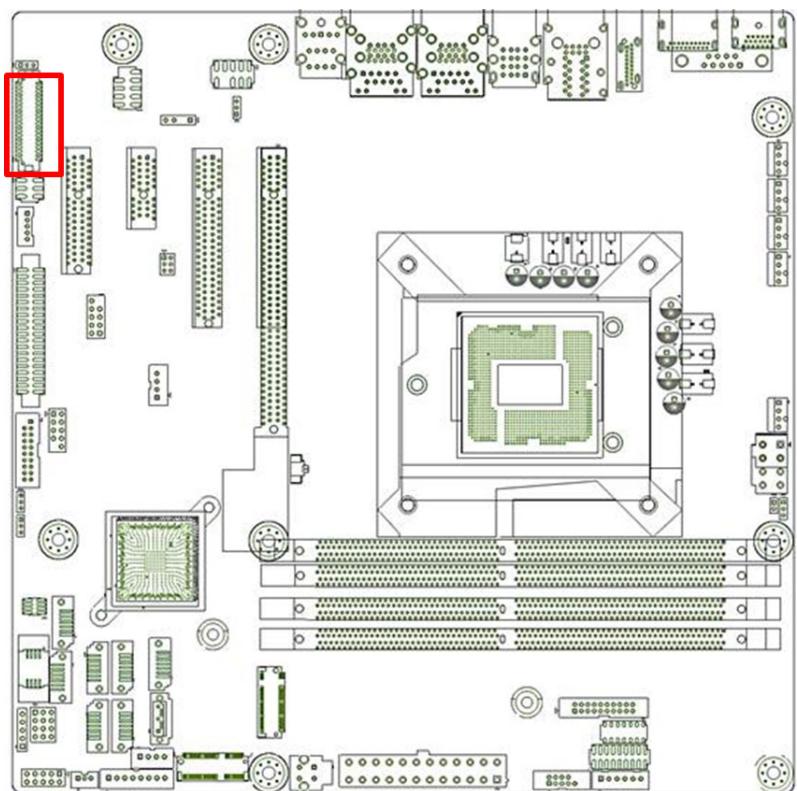


1. Please connect the ATX12V1 connector with the PSU ATX 12V 4-pin connector.
2. For a fully configured system, we recommend that you use a power supply unit (PSU) that complies with ATX 12 V Specification 2.0 (or later version) and provides a minimum power of 180 W.
3. AIMB-586 can support 12V DC-in @ ATX12V3 by HW BOM option.

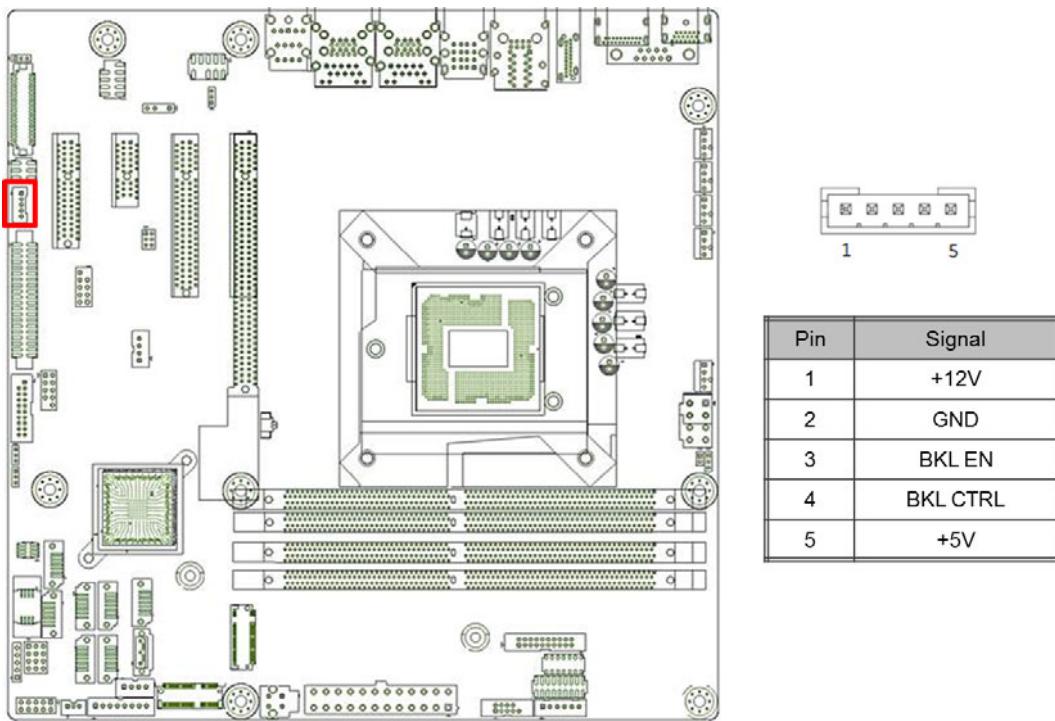
## 2.17 General purpose I/O Connector (GPIO1)



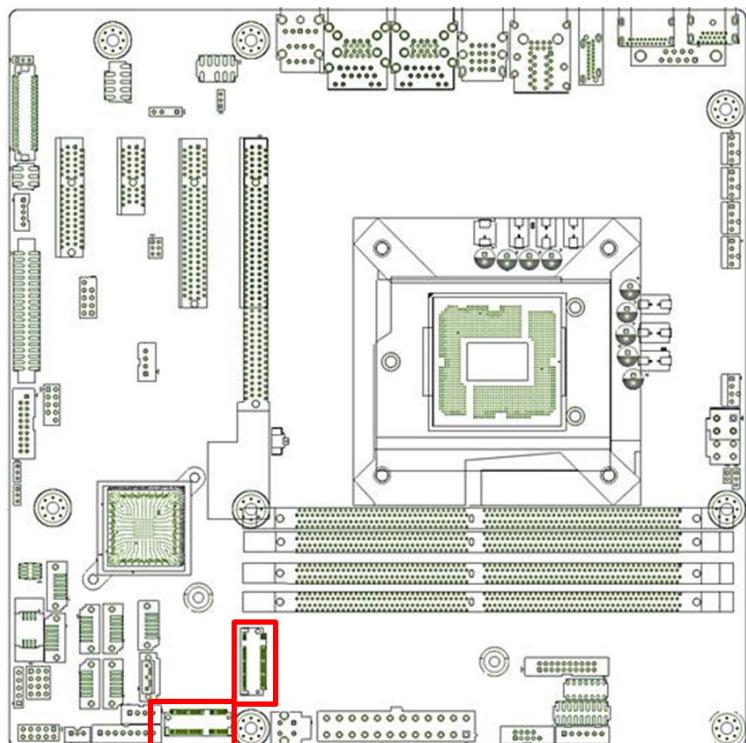
## 2.18 eDP/LVDS Connector (eDP1)



## 2.19 EDP Backlight inverter(INV1)



## 2.20 M.2 (E-key)/ M.2 (M-key)



- M.2 M-key : 2280, support SATA or PClex4 interface, and can support NVMe devices.
- M.2 E-key: 2230, support USB, PClex1 interface, can support wifi module devices and Intel CNVi module.

# Chapter 3

BIOS Operation

## 3.1 Introduction

AMI BIOS has been integrated into many motherboards, and has been very popular for over a decade. With the AMI BIOS Setup program, you can modify BIOS settings to control the special features of your computer. The Setup program uses a number of menus for making changes. This chapter describes the basic navigation of the AIMB-586 setup screens.

## 3.2 BIOS Setup

The AIMB-586 Series system has AMI BIOS built in, with a SETUP utility that allows users to configure required settings or to activate certain system features.

The SETUP saves the configuration in the FLASH of the motherboard. When the power is turned off, the battery on the board supplies the necessary power to preserve the FLASH.

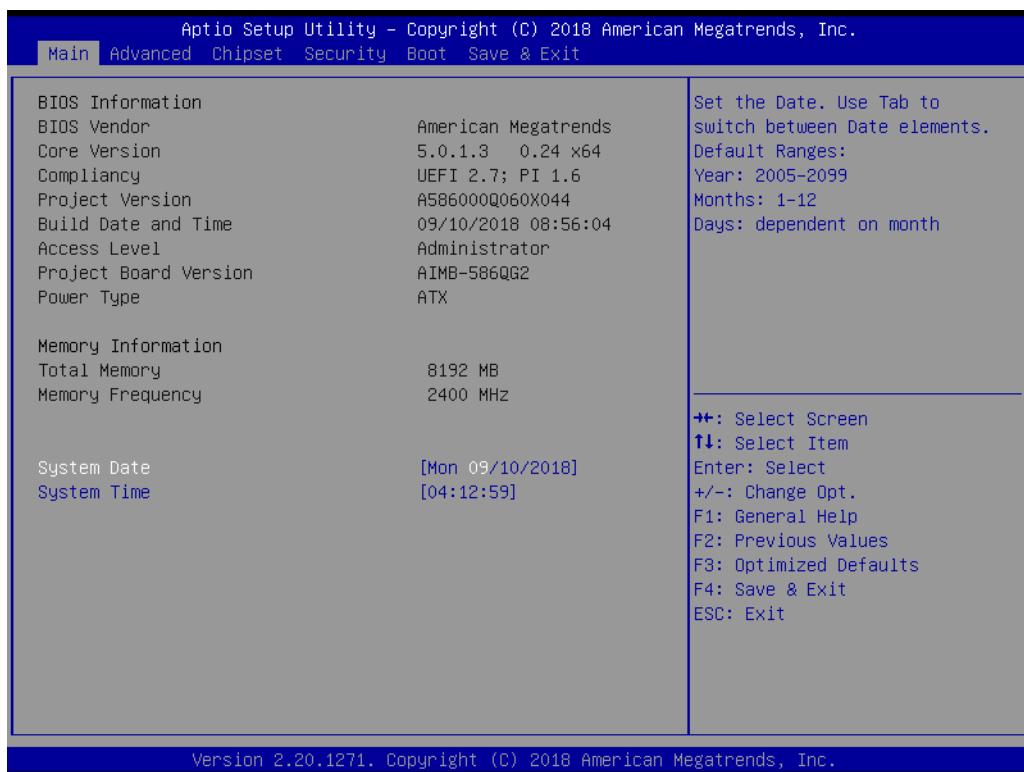
When the power is turned on, press the <Del> or <Esc> button during the BIOS POST (Power-On Self Test) to access the CMOS SETUP screen.

### Control Keys

< ← >< → >	Select Screen
< ↑ >< ↓ >	Select Item
<Enter>	Select
<+/->	Change Opt
<F1>	General help
<F2>	Previous Values
<F3>	Optimized Defaults
<F4>	Save & Exit
<Esc>	Exit

### 3.2.1 Main Menu

Press <Del> or <Esc> to enter AMI BIOS CMOS Setup Utility, the Main Menu will appear on the screen. Use arrow keys to select among the items and press <Enter> to accept or enter the sub-menu.



The Main BIOS setup screen has two main frames. The left frame displays all the options that can be configured. Grayed-out options cannot be configured; options in blue can. The right frame displays the key legend.

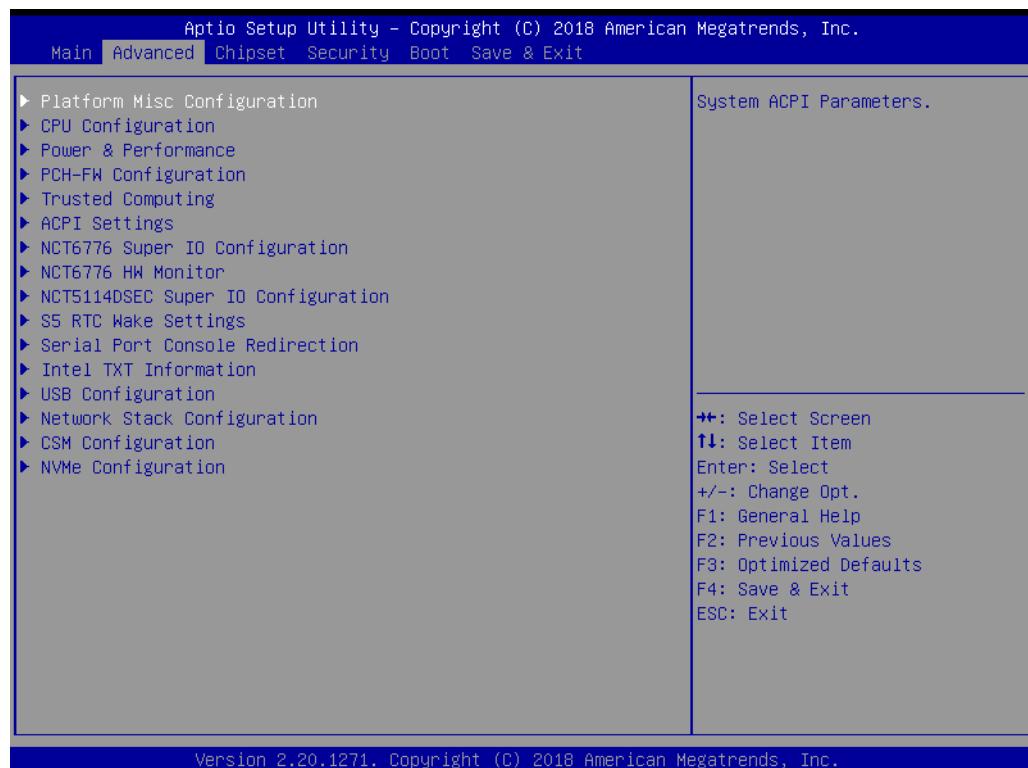
Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

#### ■ System time / System date

Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time must be entered in HH:MM:SS format.

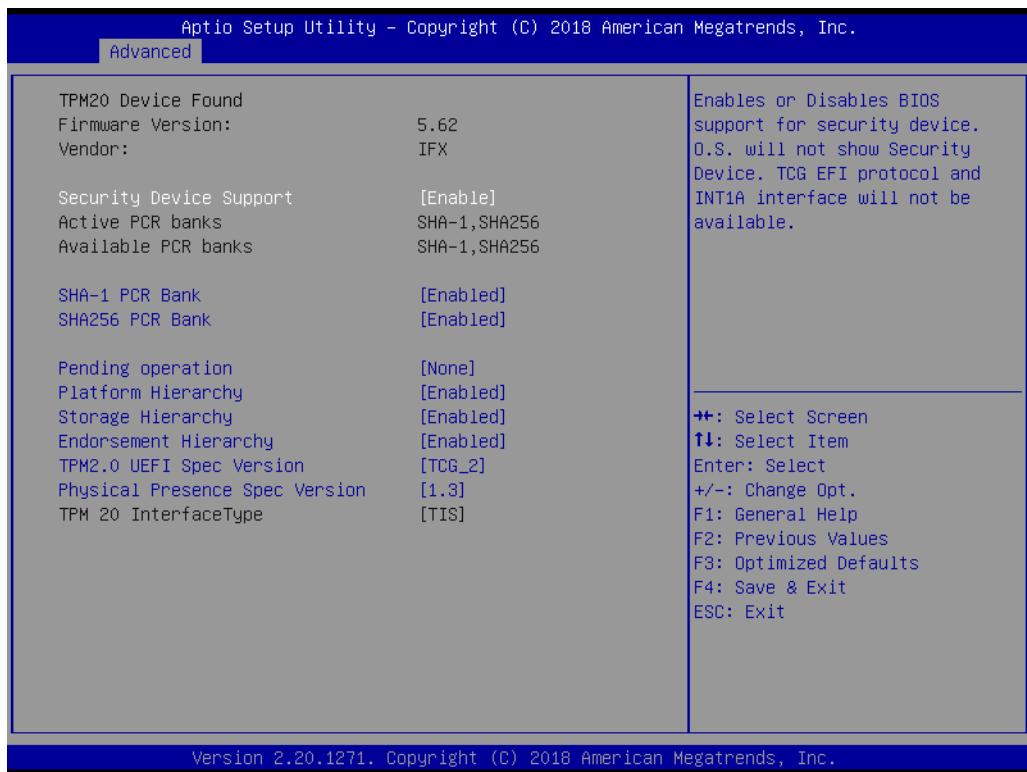
### 3.2.2 Advanced BIOS Features

Select the Advanced tab from the AIMB-586 setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as CPU Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screen is shown below. The sub menus are described on the following pages.



### 3.2.2.1 Trusted Computing

To enable/disable TPM (TPM 1.2/2.0) set up in BIOS. TPM (Trusted Platform Module) is a secure key generator and key cache management component, enables protected storage of encryption keys and authentication credentials for enhanced security capabilities.

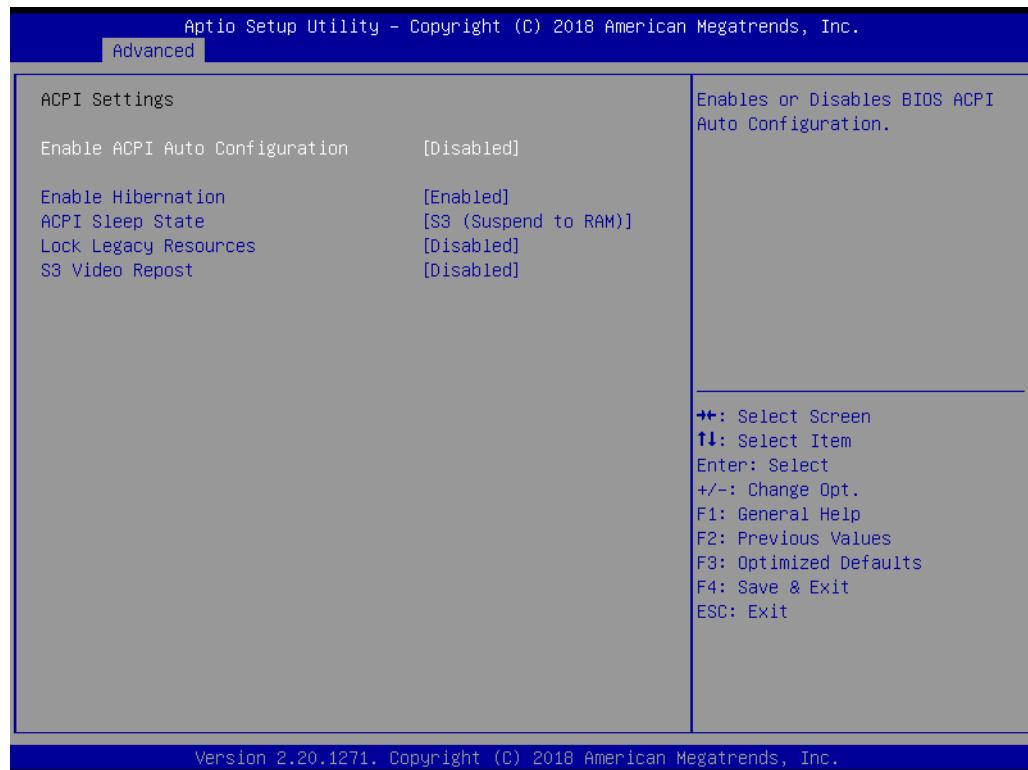


#### ■ Security Device Support [ Disable ]

**Note!** *TCG EFI Protocol and INT1A interface won't be available.*



### 3.2.2.2 ACPI Settings



- **Enable ACPI Auto Configuration [ Disabled ]**

Enable or disable BIOS ACPI auto configuration.

- **Enable Hibernation [ Enabled ]**

Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.

- **ACPI Sleep State [ Auto ]**

Select ACPI sleep state the system will enter when the SUSPEND button is pressed.

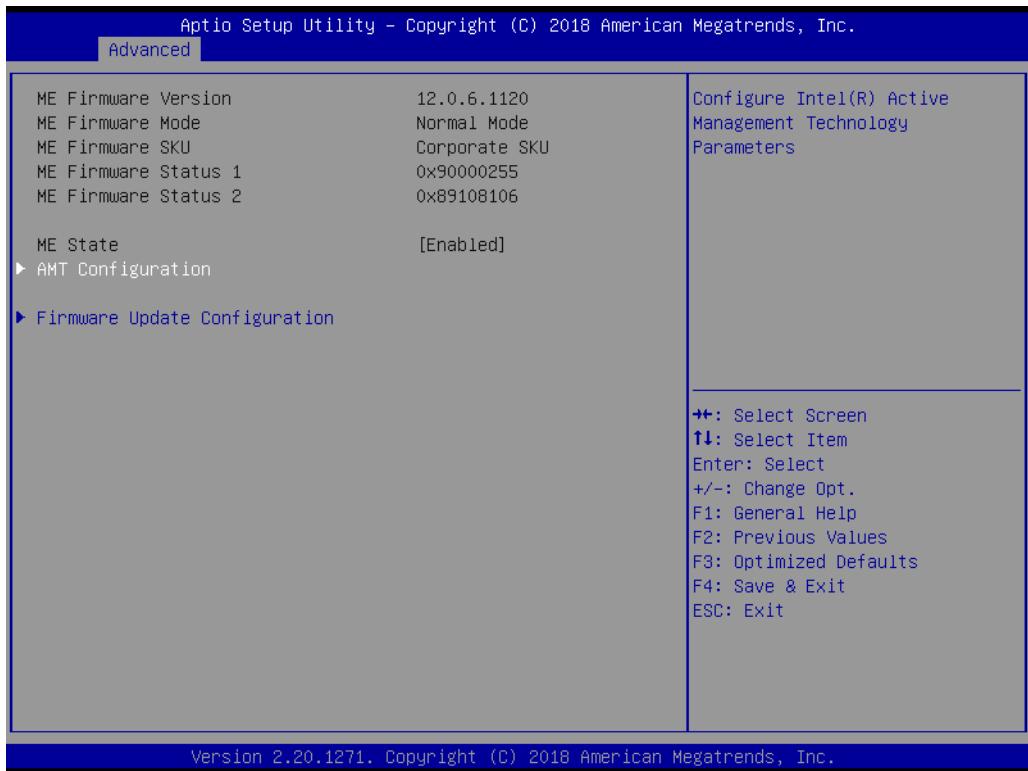
- **Lock Legacy Resources [ Disabled ]**

Enables or Disables Lock of Legacy Resources.

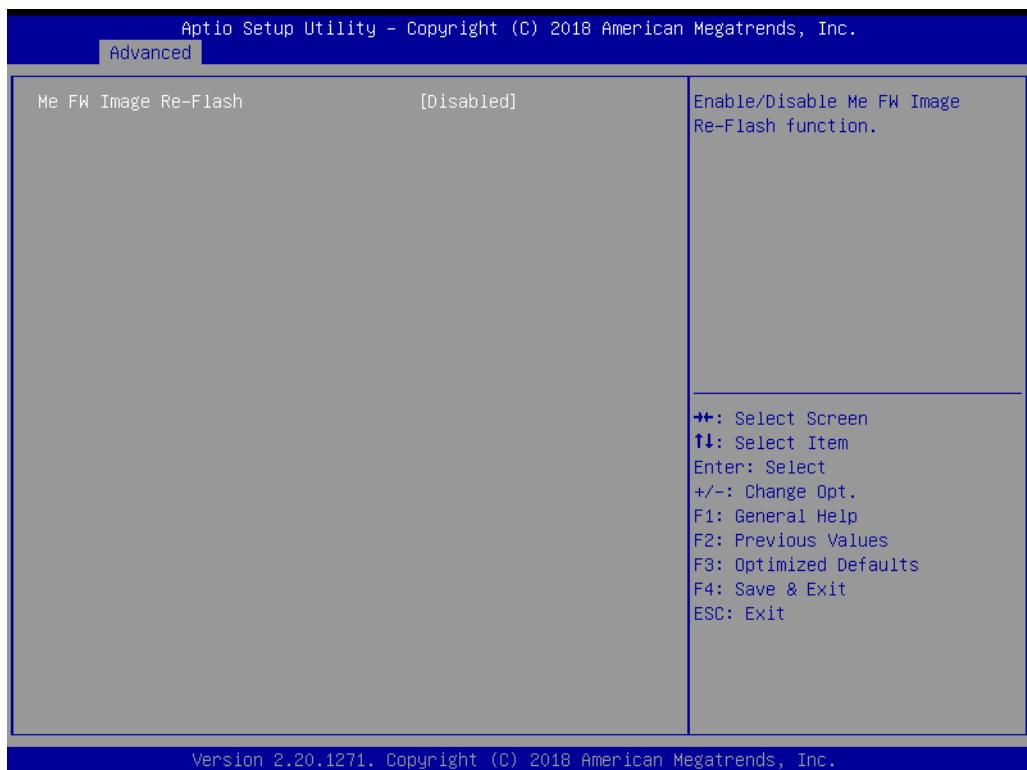
- **S3 Video Repost [ Disabled ]**

Enable or Disable S3 Video Repost.

### 3.2.2.3 PCH FW Configuration

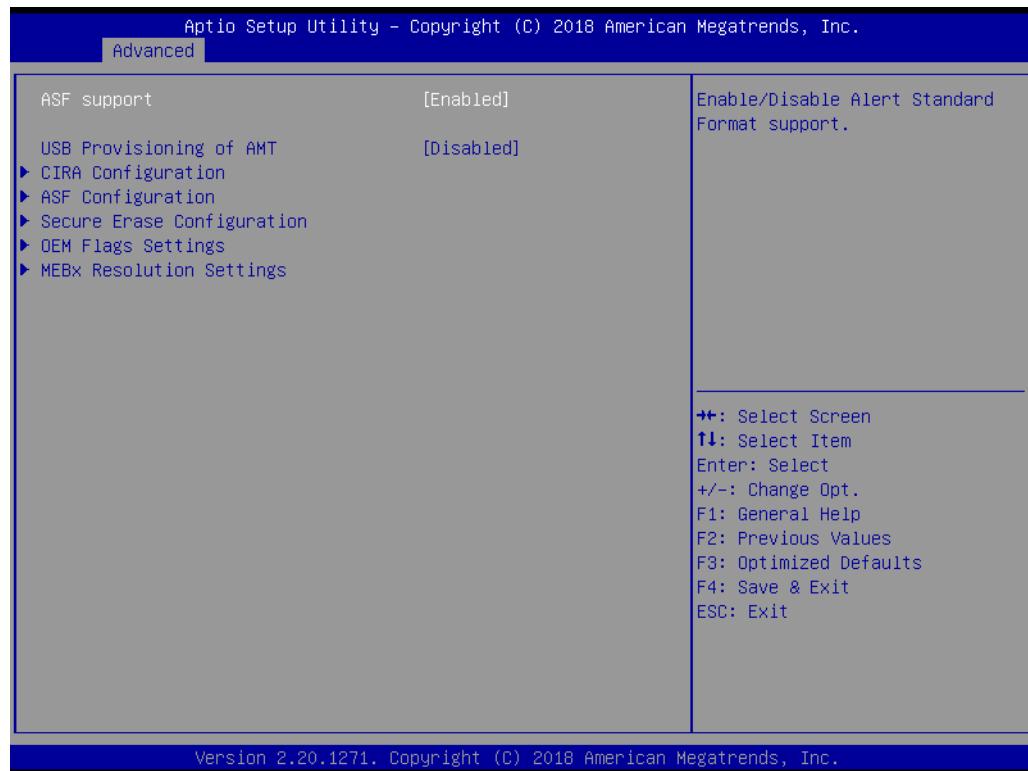


- **MEDS BIOS Status Code [ Disable ]**
- **Firmware update Configuration**



- **ME FW Image Re-Flash [ Disabled ]**

### 3.2.2.4 AMT Configuration



#### ■ Intel ASF [ Enabled ]

This item allows users to enable or disable Intel Alert Standard Format.

#### ■ OEM Flags Settings

- MEBx Hotkey Pressed [ Disabled ]

Enable/Disable BIOS hotkey press.

- MEBx Select Screen [ Disabled ]

Enable/Disable MEBx selection screen.

- Hide Un-Configure ME Confirmation [ Disabled ]

Hide Un-Configure ME without password Confirmation Prompt.

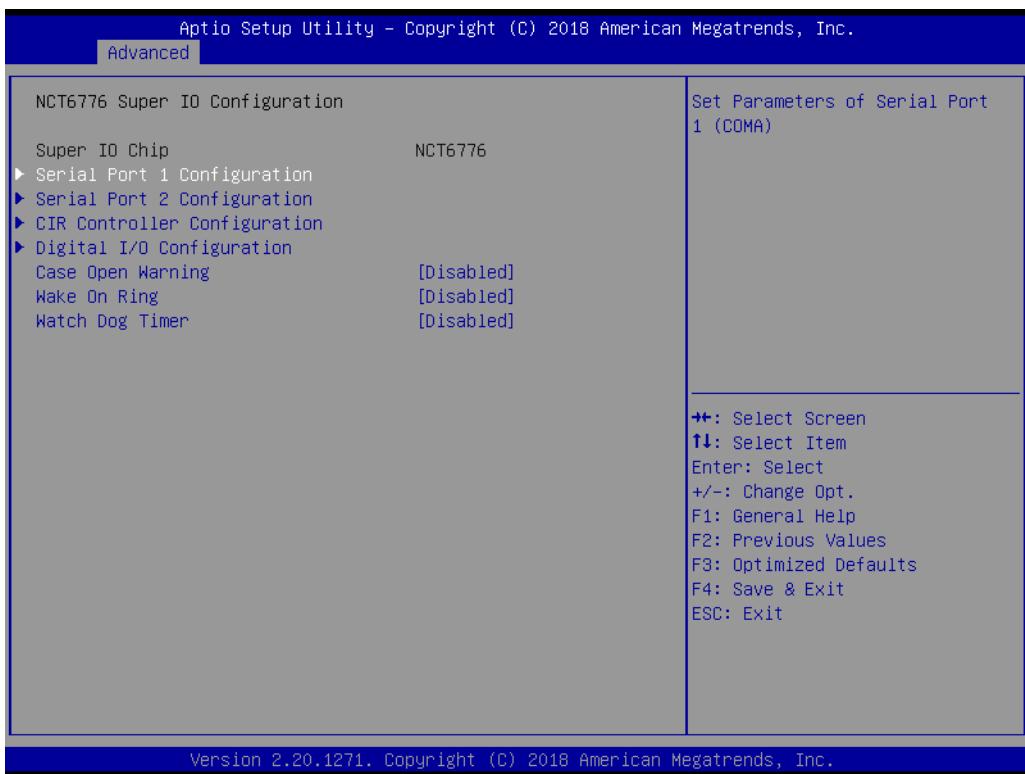
- MEBx Debug Message Output [ Disabled ]

Enable MEBx debug message output.

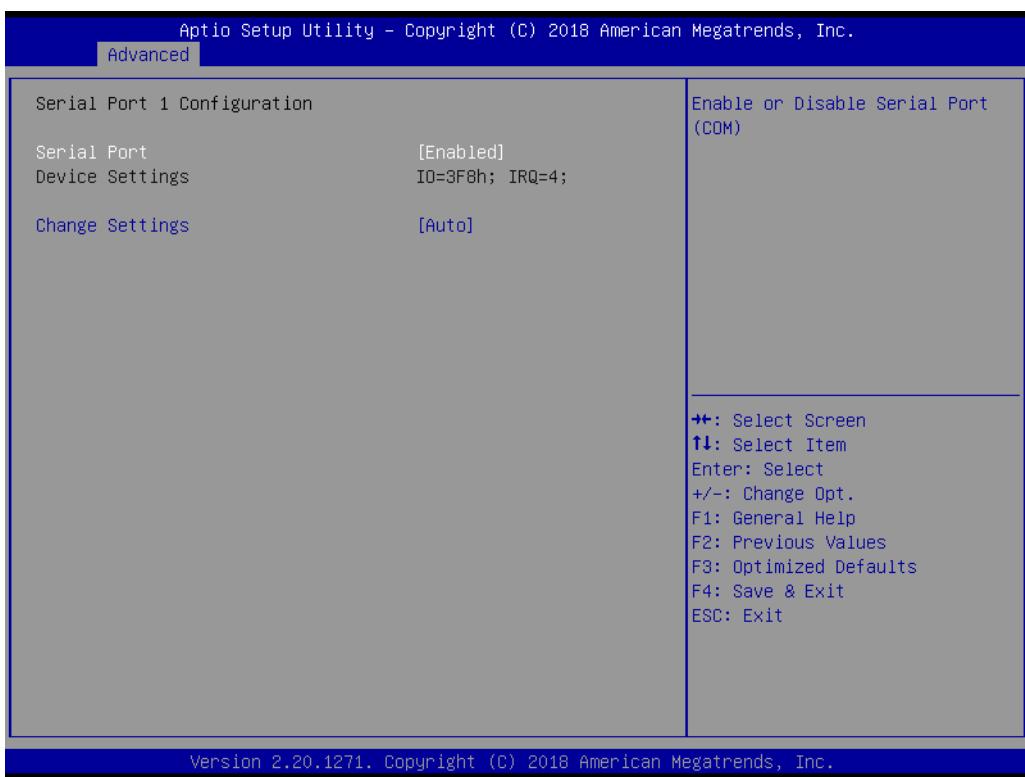
- Un-Configure ME [ Disabled ]

Sets this item to [Disabled] to unconfigure AMT/ME without using a password or set it as [Enabled] to use a password.

### 3.2.2.5 NCT6776 Super IO Configuration

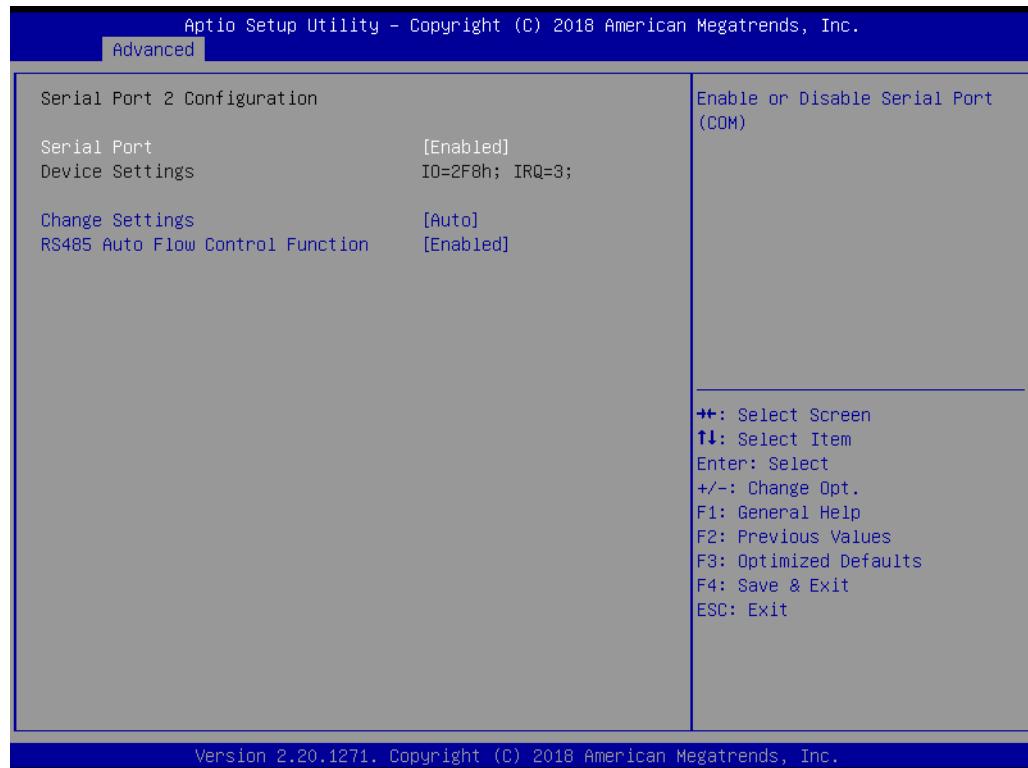


- **Super IO Chip [ NCT6776 ]**
- **Serial Port 1 Configuration**



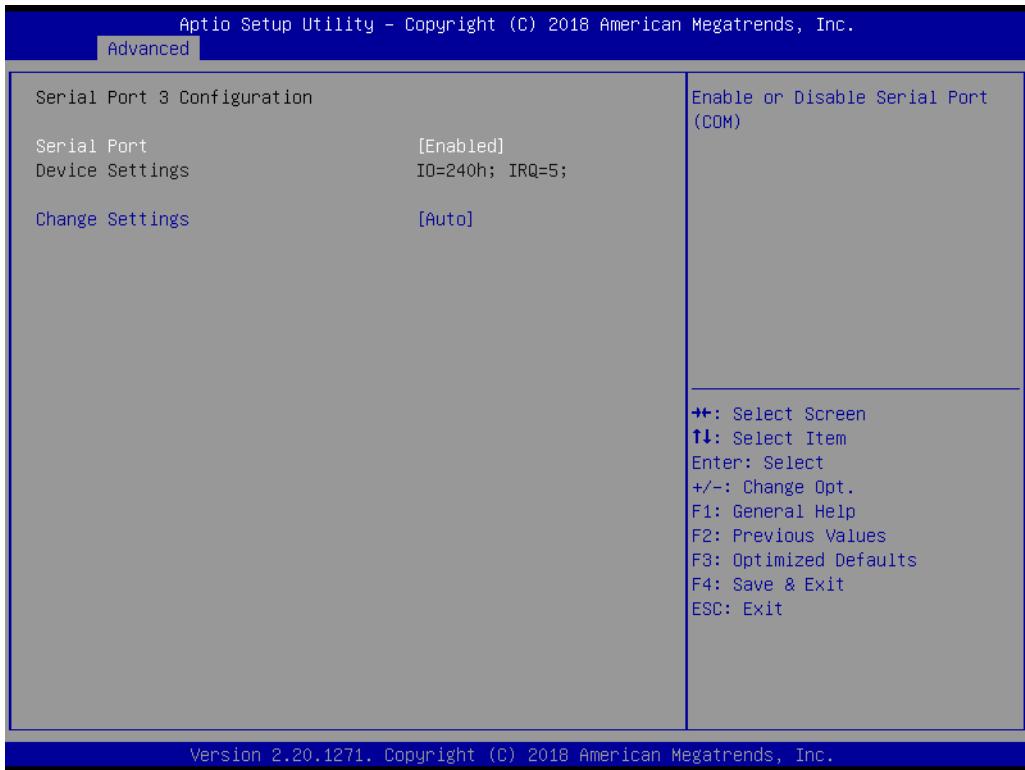
- **Serial Port [ Enabled ]**
- **Device Settings: IO=3F8h; IRQ =4**
- **Change Settings [ Auto ]**  
To select an optimal setting for serial port 1.

## ■ Serial Port 2 Configuration



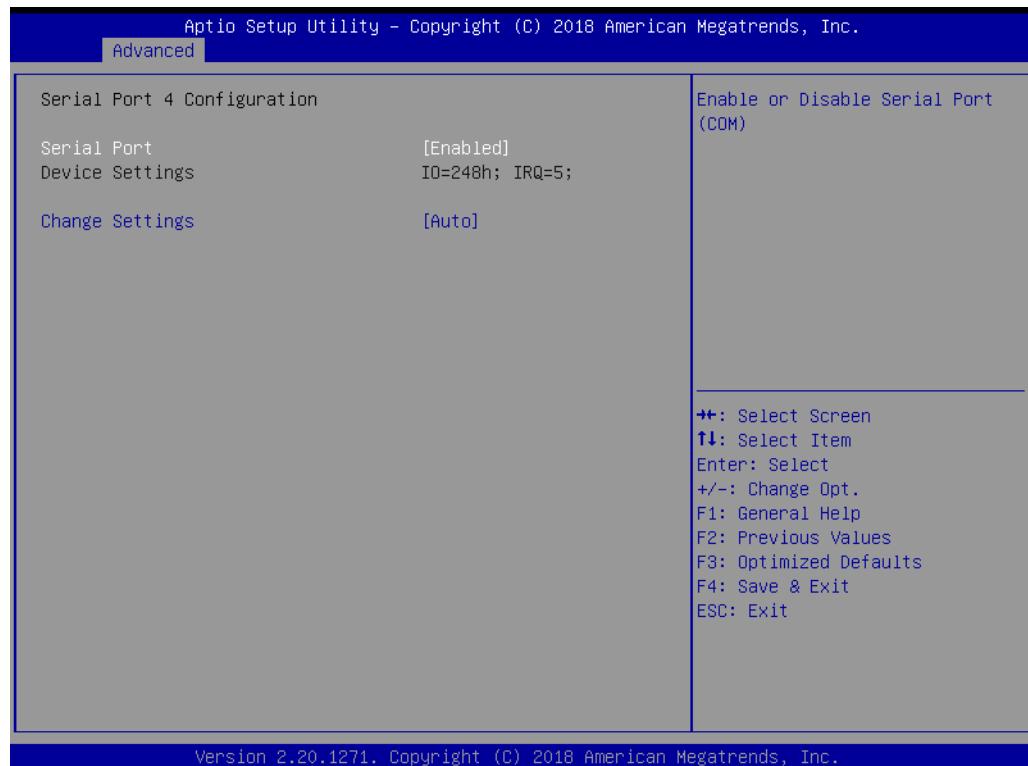
- **Serial Port [ Enabled ]**
- **Device Settings: IO=2F8h; IRQ =3**
- **Change Setting [ Auto ]**  
To select an optimal setting for serial port 2.

### 3.2.2.6 NCT5114DSEC Super IO Configuration



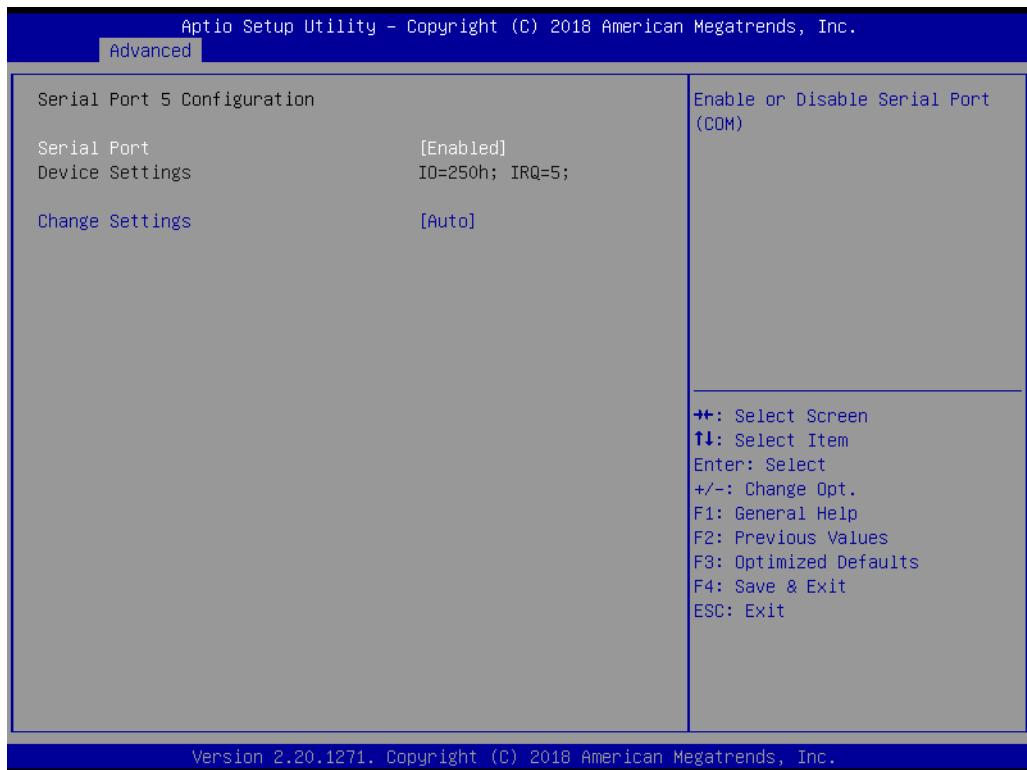
- **Serial Port [ Enabled ]**  
To “enable or disable” Serial Port 3.
- **Device Settings: IO=240H; IRQ=5**
- **Change Settings [ Auto ]**  
To select an optimal setting for serial port 3.

## ■ Serial Port 4 Configuration



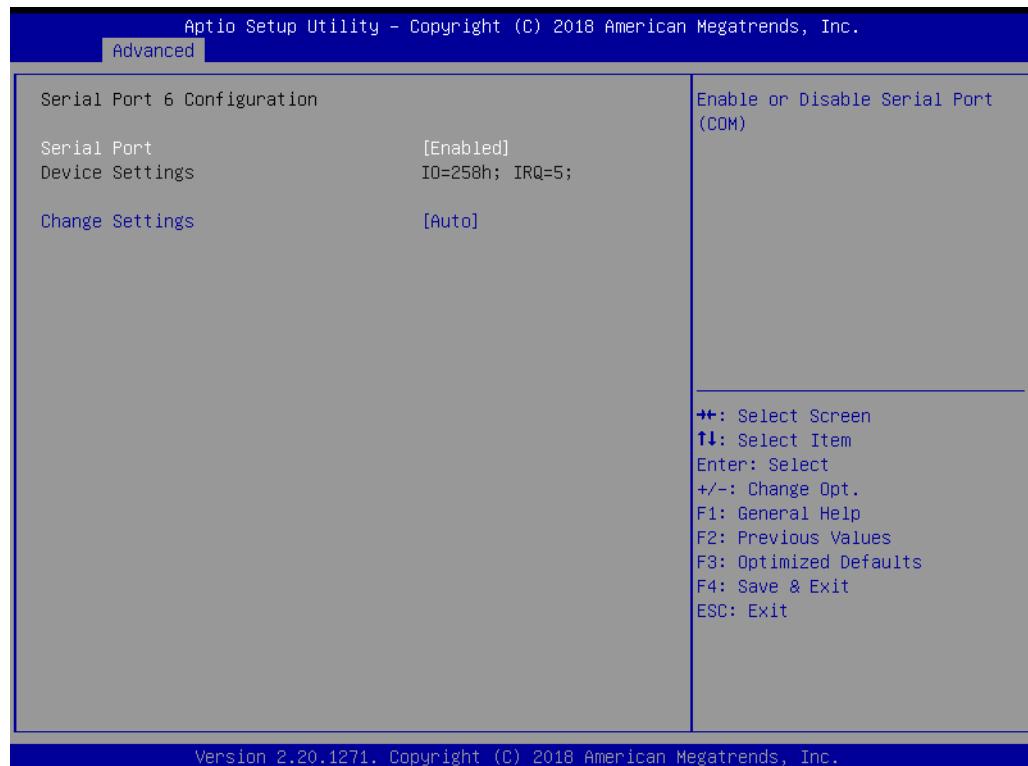
- **Serial Port [Enabled]**  
To "enable or disable" serial port 4.
- **Device Settings: IO=248H; IRQ=5**
- **Change Settings [ Auto ]**  
To select an optimal setting for serial port 4.

## ■ Serial Port 5 Configuration



- **Serial Port [Enabled]**  
To “enable or disable” serial port 5.
- **Device Settings: IO=250H; IRQ=5**
- **Change Settings [ Auto ]**  
To select an optimal setting for serial port 5.

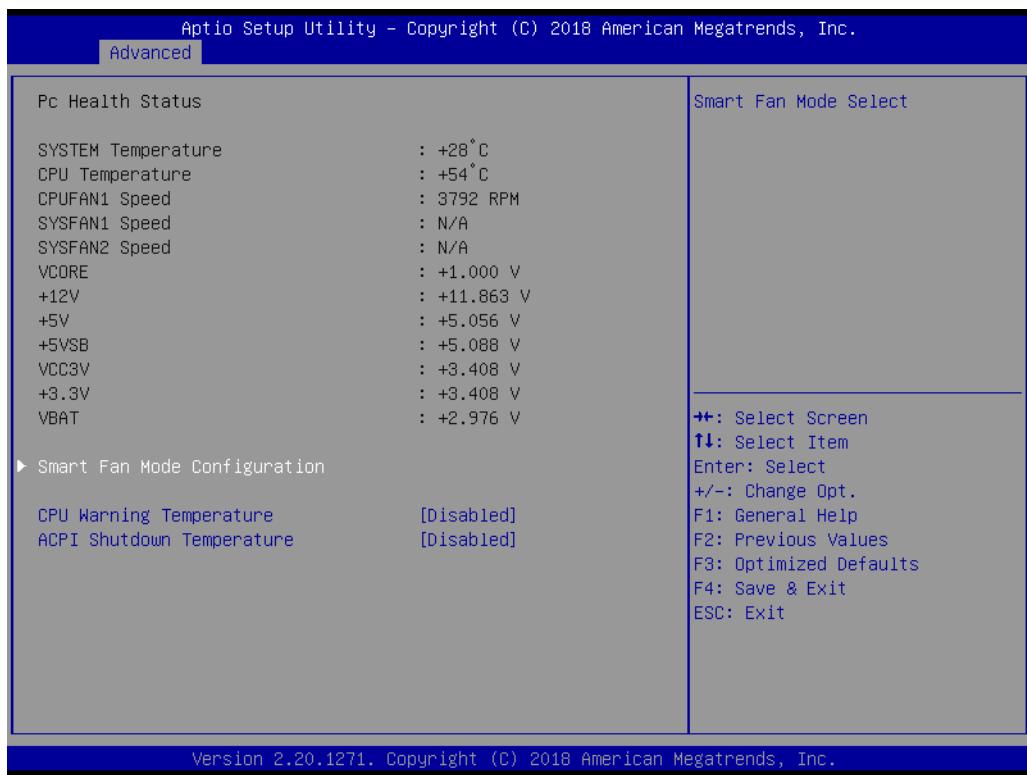
## ■ Serial Port 6 Configuration



- **Serial Port [ Enabled ]**  
To “enable or disable” serial port 6.
- **Device Settings: IO=258H; IRQ=5**
- **Change Setting [ Auto ]**  
To select an optimal setting for serial port 6.

### 3.2.2.7 NCT6776 Configuration

#### ■ PC Health Status



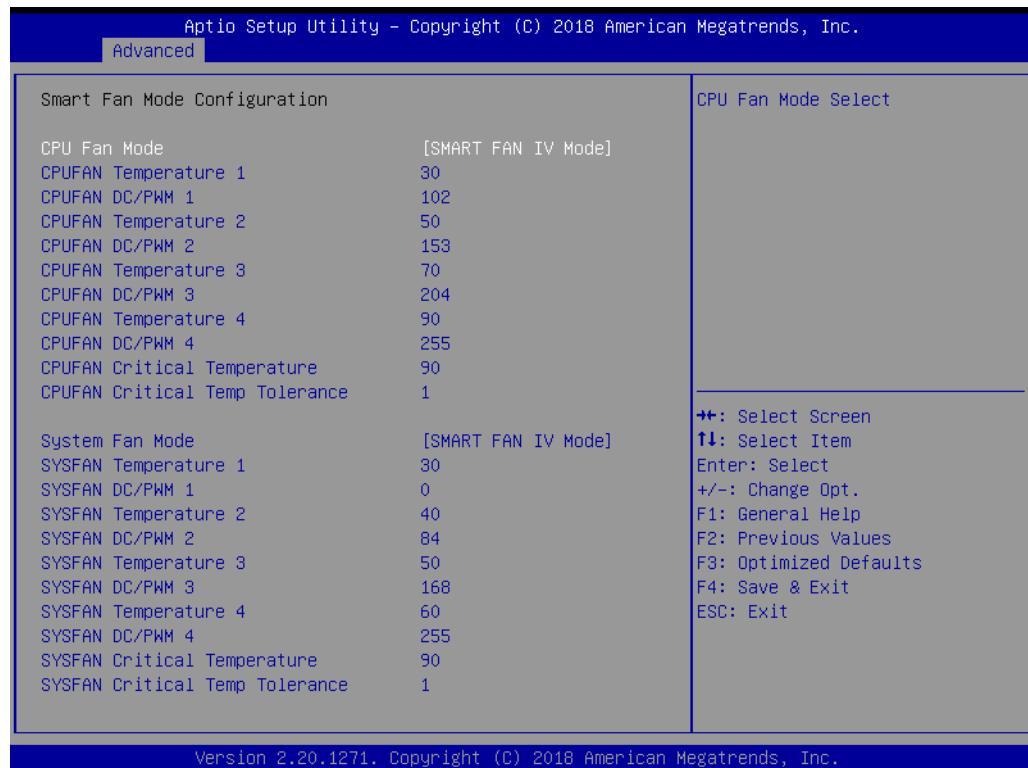
#### – CPU Warning Temperature [ Disabled ]

Use this to set the CPU warning temperature threshold. When the system reaches the warning temperature, the speaker will beep.

#### – ACPI Shutdown Temperature [ Disabled ]

Use this to set the ACPI shutdown temperature threshold. When the system reaches the shutdown temperature, it will be automatically shut down by ACPI OS to protect the system from overheating damage.

## ■ Smart Fan Mode Configuration



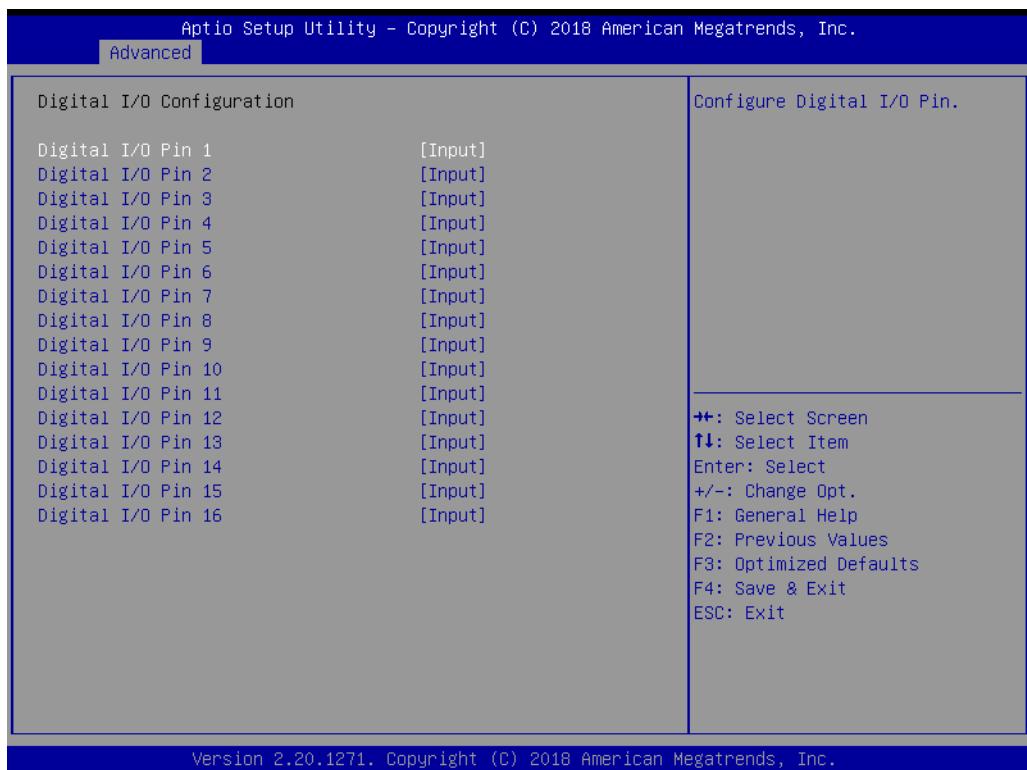
### ■ CPU FAN Mode [ SMART FAN IV Mode ]

The item shows you CPU temperature and fan speed (PWM) information.

### ■ SYSFAN Mode [ SMART FAN IV Mode ]

The item shows you system temperature and fan speed (PWM) information.

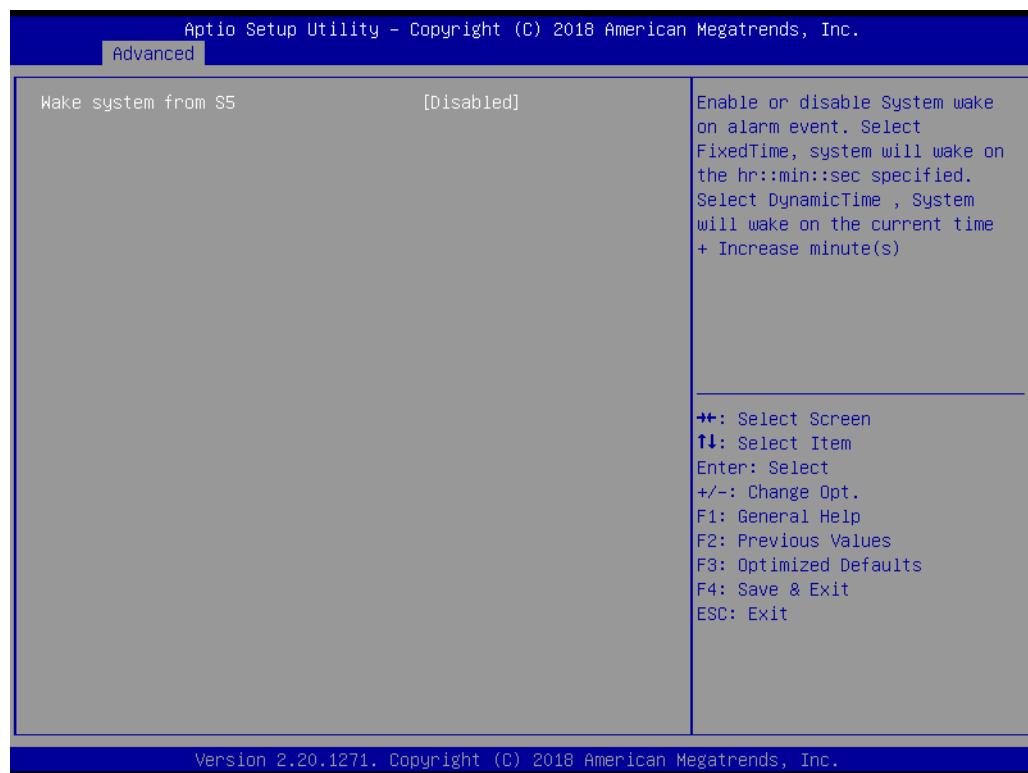
## ■ Digital I/O Configuration



### – Digital I/O Pin 1 - 16 [ Input ]

### 3.2.2.8 S5RTC Wake Settings

The item allow you enable or disable system wake up on alarm event.

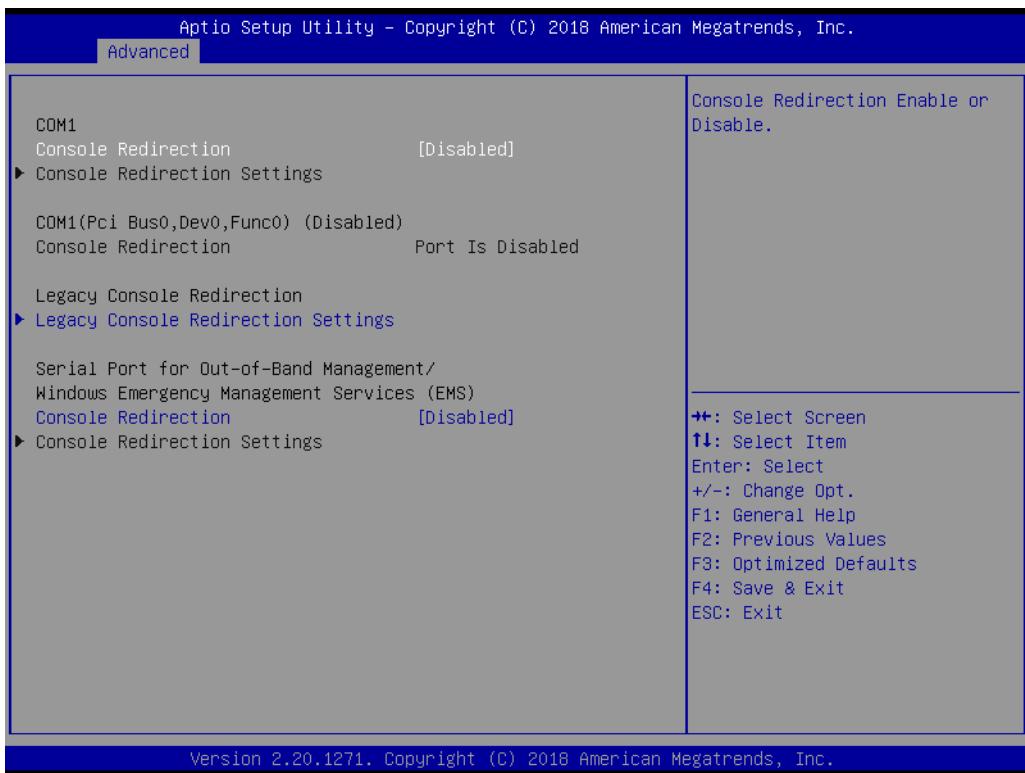


#### ■ Wake system with Fixed Time [ Disabled ]

**Note!** When enabled, system will wake up on the specified time.



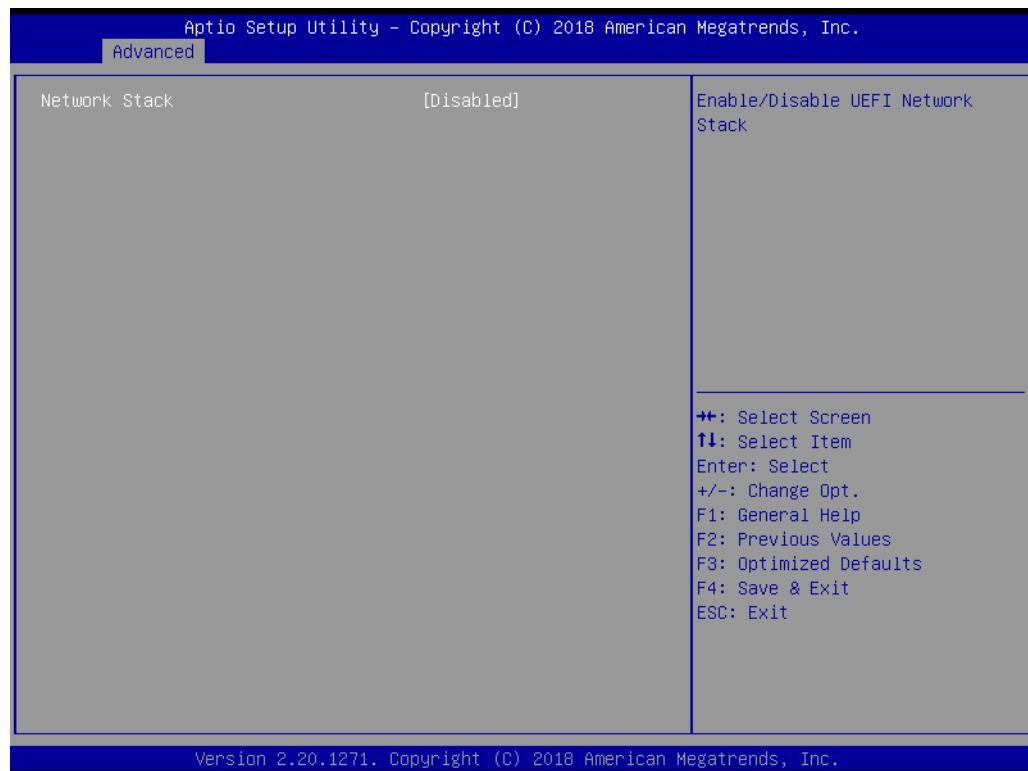
### 3.2.2.9 Serial Port Console Redirection



#### ■ **Console Redirection [ Disabled ]**

Enable or disable the console redirection feature

### 3.2.2.10 Network Stack Configuration[Disabled]

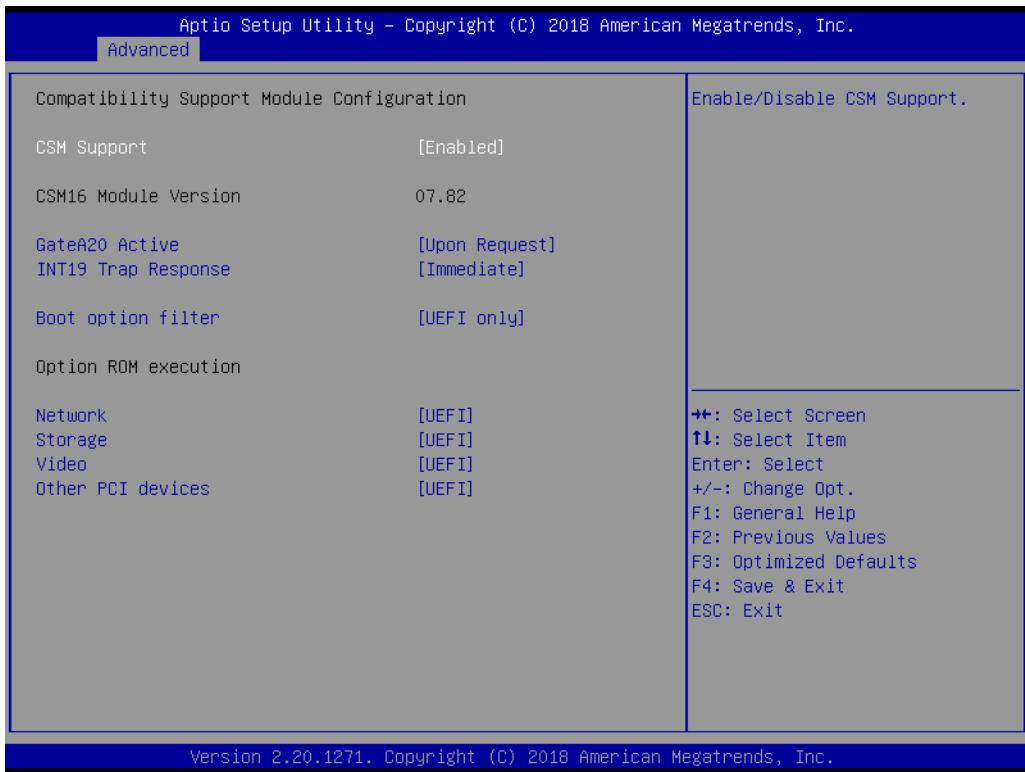


#### ■ Enable/Disable UEFI Network Stack

**Note!** When network stack [enable], item must enable: LANx PXE OpROM [enable]



### 3.2.2.11 CSM Configuration



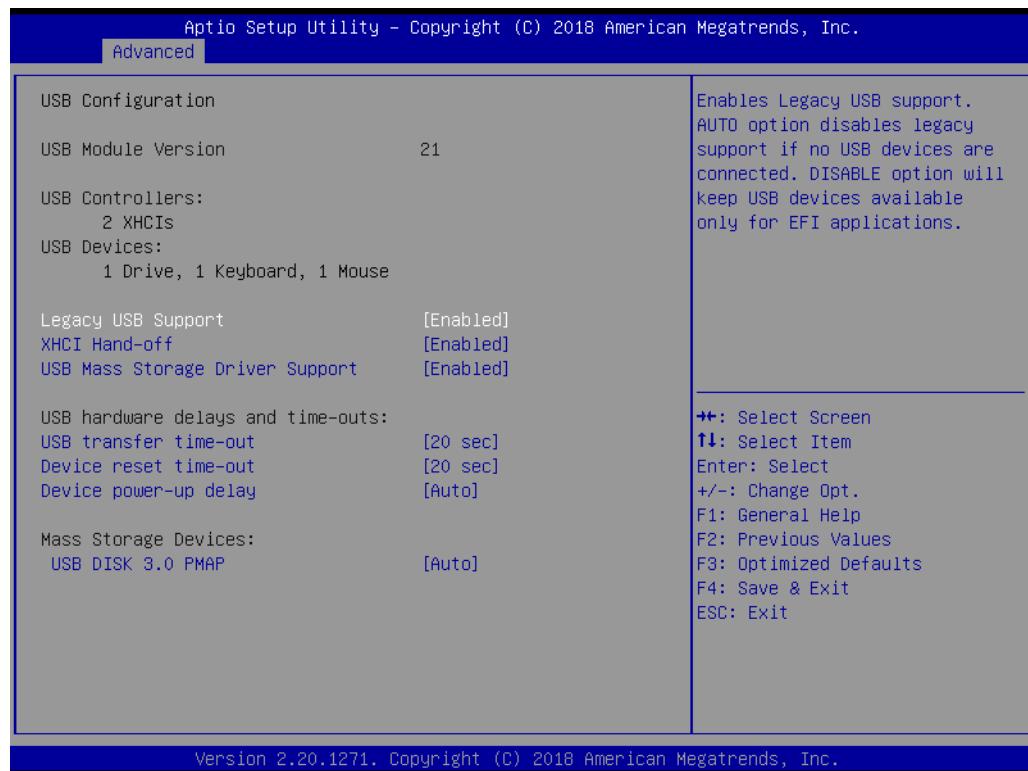
- **Boot option filter**    [UEFI only]
- **Network**            [UEFI]
- **Storage**            [UEFI]
- **Video**              [UEFI]
- **Other PCI device** [UEFI]

**Note!** If your HDD or other boot device is installed as Legacy mode, it may cause blue screen situation. There are 2 ways to solve this:



1. Re-install your OS as UEFI Mode
2. Change all of settings above as "Legacy"
  - \* Boot option filter-> Legacy Only
  - \* Network -> Legacy
  - \* Storage -> Legacy
  - \* Video -> Legacy
  - \* Other PCI devices -> Legacy

### 3.2.2.12 USB Configuration



- **Legacy USB Support [ Enabled ]**

Enables support for legacy USB. Auto option disables legacy support if no USB devices are connected.

- **XHCI Hand-off [ Enabled ]**

- **USB Mass Storage Driver Support [ Enabled ]**

- **USB hardware delays and time-outs**

USB Device transfer & reset time-out and delay setting.

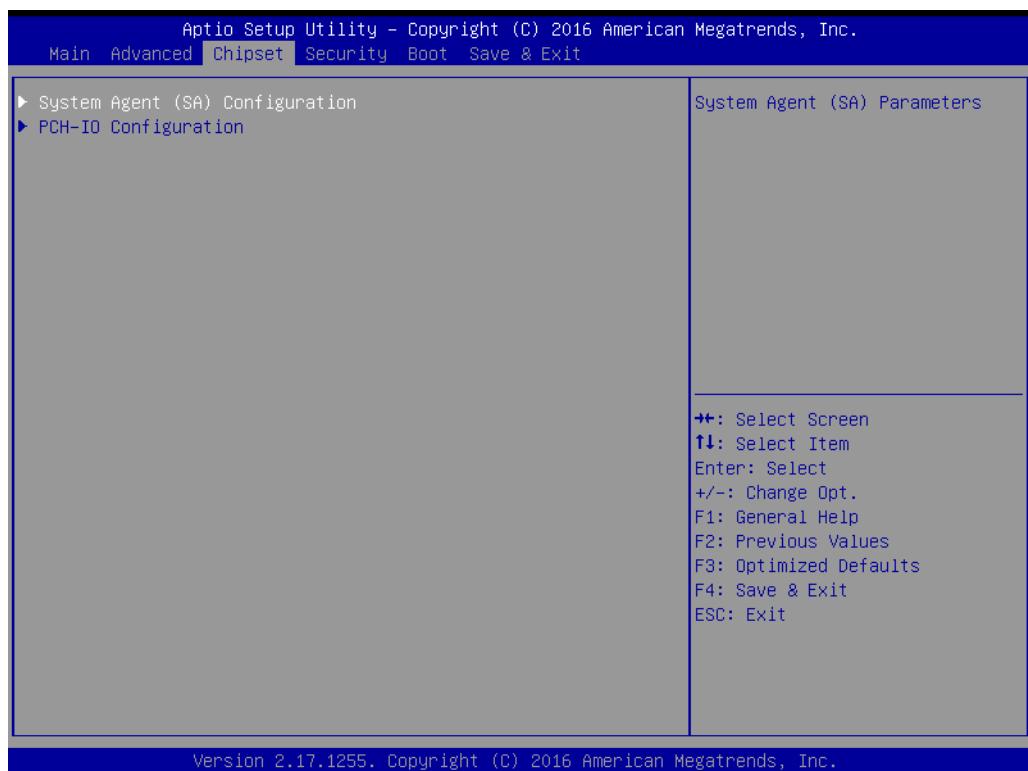
- **Mass Storage Devices [ Auto ]**

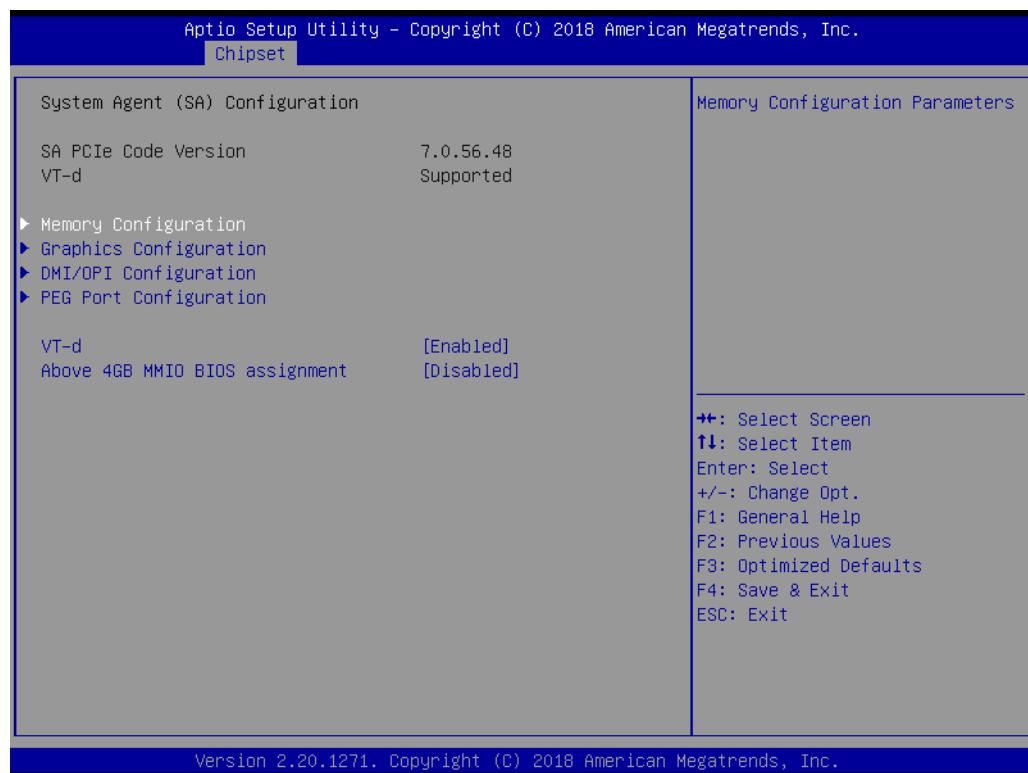
Shows USB mass storage device information.

## 3.3 Chipset Configuration Setting

Select the chipset tab from the BIOS setup screen to enter the Chipset Setup screen. Users can select any item in the left frame of the screen, such as PCI express Configuration, to go to the sub menu for that item. Users can display a Chipset Setup option by highlighting it using the <Arrow> keys. All Chipset Setup options are described in this section. The Chipset Setup screens are shown below. The sub menus are described on the following pages.

### 3.3.1 System Agent (SA) Configuration

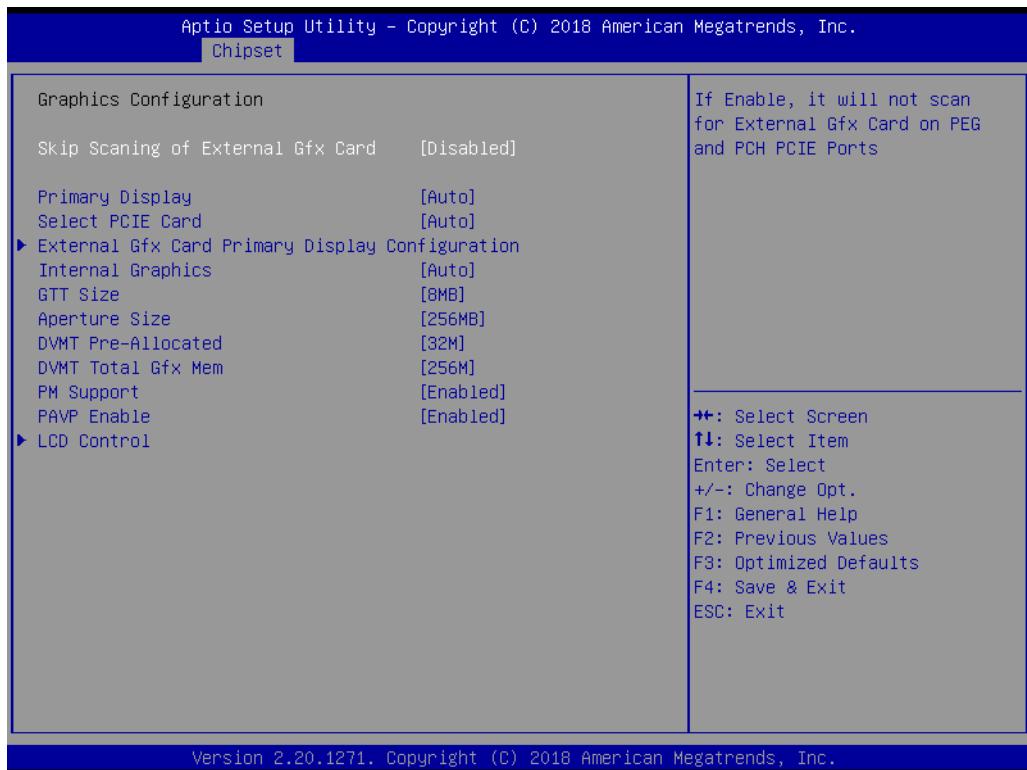




## ■ VT-d [ Enabled ]

Disable or enable VT-d function on MCH.

### 3.3.1.1 Graphics Configuration



- **Skip Scaning of External Gfx Card [disabled]**
- **Primary Display [ Auto ]**  
Select which of IGFX/PEG/PCI Graphics device should be Primary Display
- **Internal Graphics [ Auto ]**  
Keep IGD enabled based on the setup options.
- **GTT size [8MB]**
- **Aperture Size [ 256MB ]**
- **DVMT Pre-Allocated [ 32M ]**  
Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.
- **DVMT Total Gfx Mem [ 256M ]**  
Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device.

**Note!** When BIOS set as "Auto", only single display under DOS.



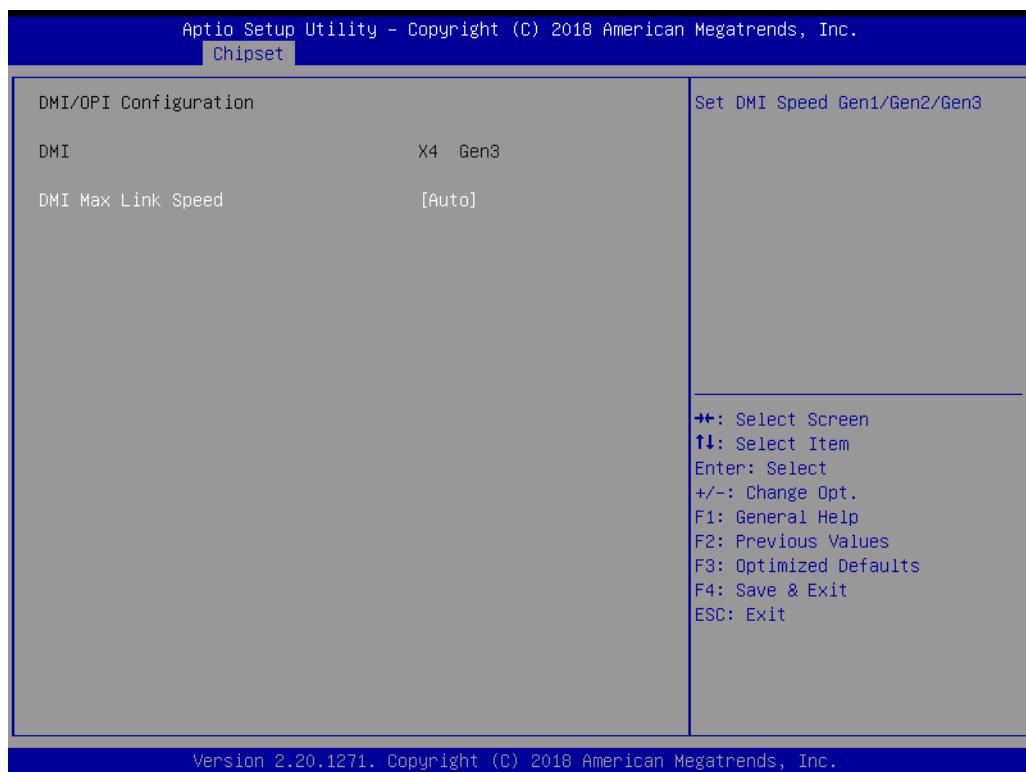
**Note!** The triple display can only working PASS under Windows 10, the 2nd and 3rd display can not work under DOS.



Here is 2-3 displays combination table and all of these combinations are verified and tested properly already.

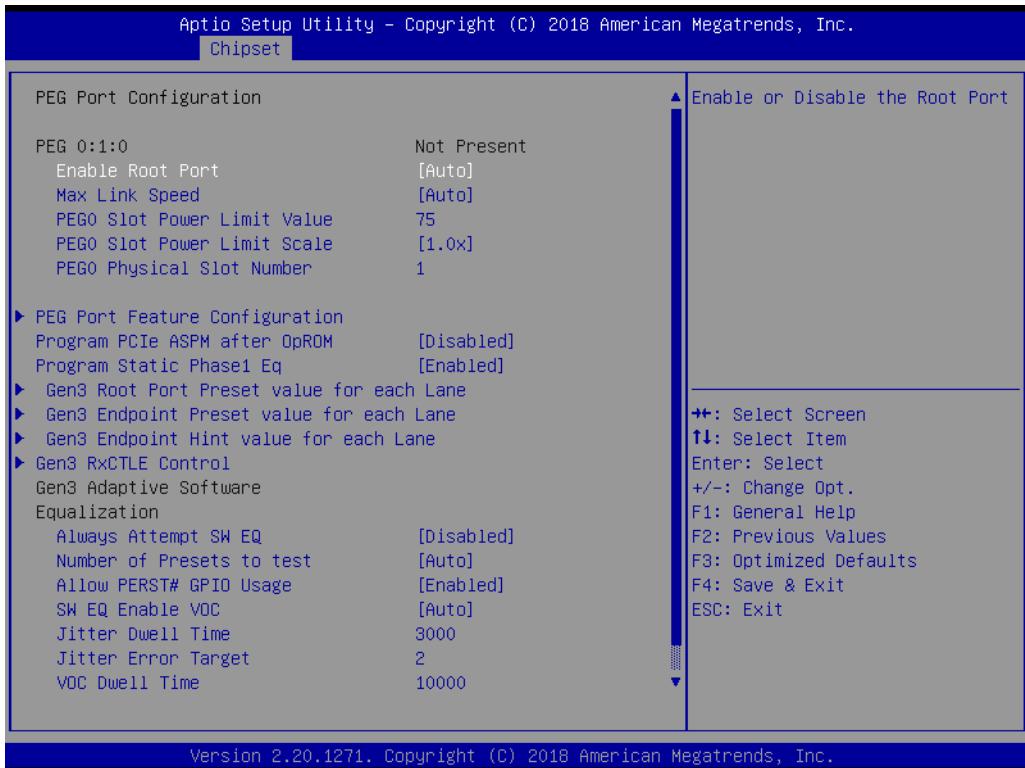
Display Combination List	BIOS	DOS	WES 10
<b>Single Display</b>			
DP1	PASS	PASS	PASS
DP2	PASS	PASS	PASS
EDP	PASS	PASS	PASS
HDMI	PASS	PASS	PASS
<b>Dual Display</b>			
DP1/DP2+HDMI	NA	NA	PASS
DP1+DP2	NA	NA	PASS
DP1/DP2+EDP	NA	NA	PASS
eDP+HDMI	NA	NA	PASS
<b>Triple Display</b>			
DP1+HDMI+DP2	NA	NA	PASS
DP1+HDMI+eDP	NA	NA	PASS
DP2+eDP+HDMI	NA	NA	PASS

### 3.3.1.2 DMI Configuration



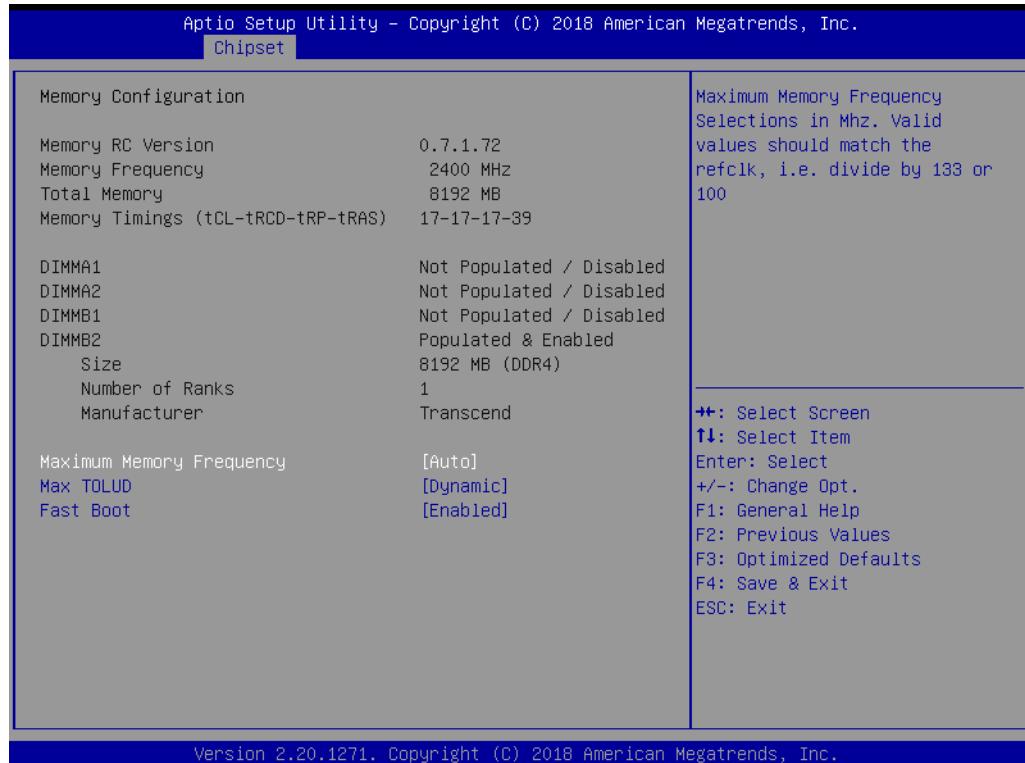
#### ■ DMI MAX Link Speed [ Auto ]

### 3.3.1.3 PEG Port Configuration



- **Enable Root Port [ Auto ]**
- **Max Link Speed [Auto]**
- **Program PCIe ASPM after OpROM [ Disabled ]**  
Enabled: PCIe ASPM will be programmed after OpROM.  
Disabled: PCIe ASPM will be programmed before OpROM.
- **Program Static Phase1 Eq [Enabled]**
- **PEG Gen3 Root Port Preset Value for each Lane**  
Root Port Preset Value Per lane for Gen3 Equalization.
- **PEG Gen3 Endpoint Preset Value each Lane**  
Endpoint Preset Value Per lane for Gen3 Equalization.
- **PEG Gen3 Endpoint Hint Value each Lane**  
Endpoint Hint Value Per lane for Gen3 Equalization.

### 3.3.1.4 Memory Configuration



The item shows you memory specification included RC version, Frequency, size and voltage information etc.

- **Max TOLUD [ Dynamic ]**

Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller.

- **Fast Boot [Enabled]**

Enable or disable Fast Boot support.

### 3.3.2 PCH-IO Configuration



- **PCI Express Configuration**  
Details of PCI Express items. (See 3.3.2.1)
- **Security Configuration**  
Details of BIOS security items. (See 3.3.2.3)
- **LAN 1 controller [ Enabled ]**  
Enable or disable the LAN 1 controller.
- **LAN 2 controller [ Enabled ]**
- **LAN 3 controller [ Enabled ]**
- **LAN 4 controller [ Enabled ]**
- **PCIE Wake [ Disabled ]**  
Enable or disable PCIE to wake the system from S5.
- **High Precision Timer [ Enabled ]**  
Enable or Disable High Precision Timer.
- **State After G3 [ Power Off ]**  
This item allows users to select off, on and last state.

### 3.3.2.1 PCI Express Configuration



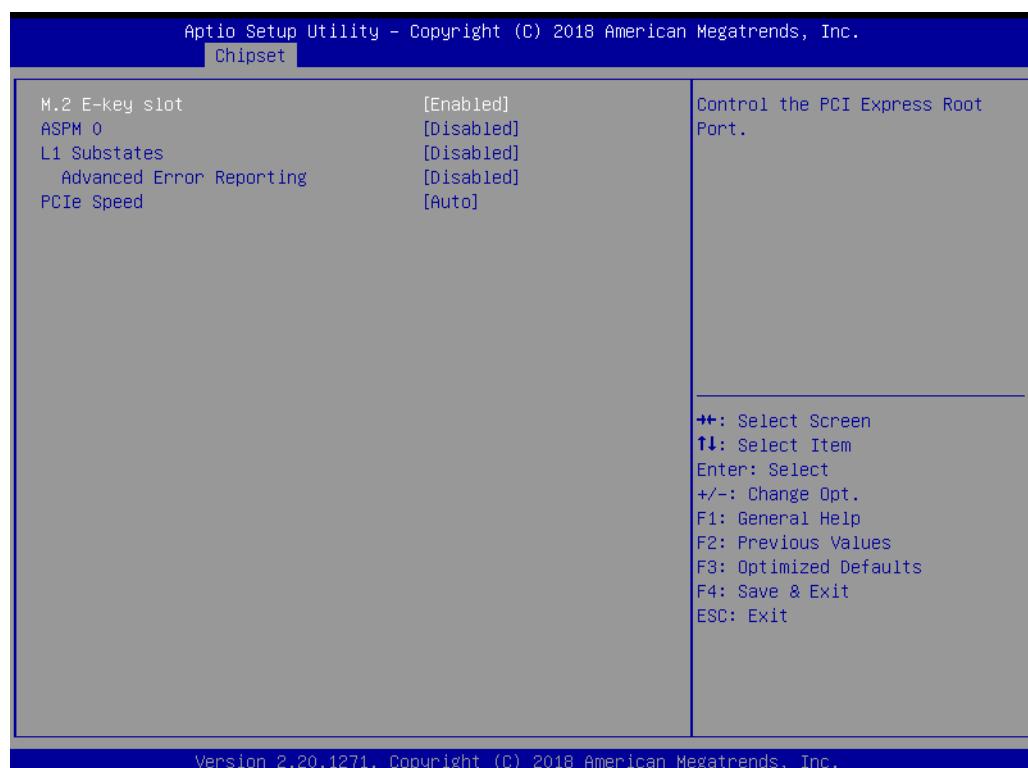
#### ■ PCI Express Clock Gating [ Enabled ]

Enable or Disable PCI Express clock gating for each port.

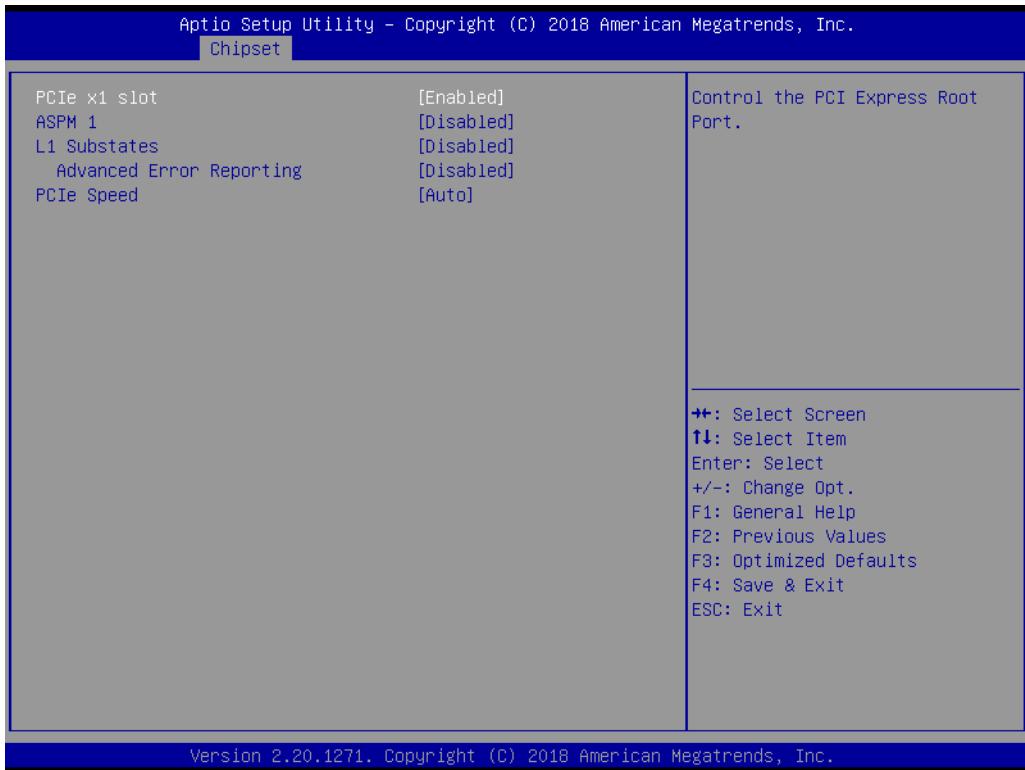
#### ■ PCIe-USB Glitch W/A [ Disabled ]

PCIe-USB Glitch W/A for bad USB device(s) connected behind PCIE/PEG Port.

#### ■ M.2 E -key slot

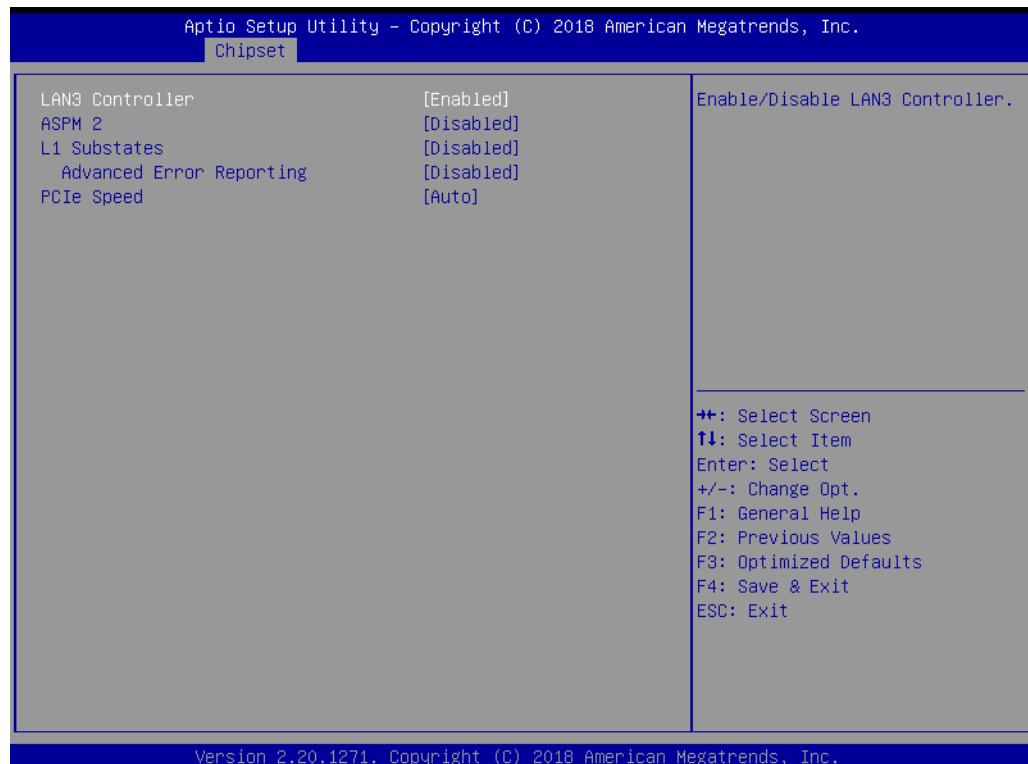


## ■ PCI Express x1 slot

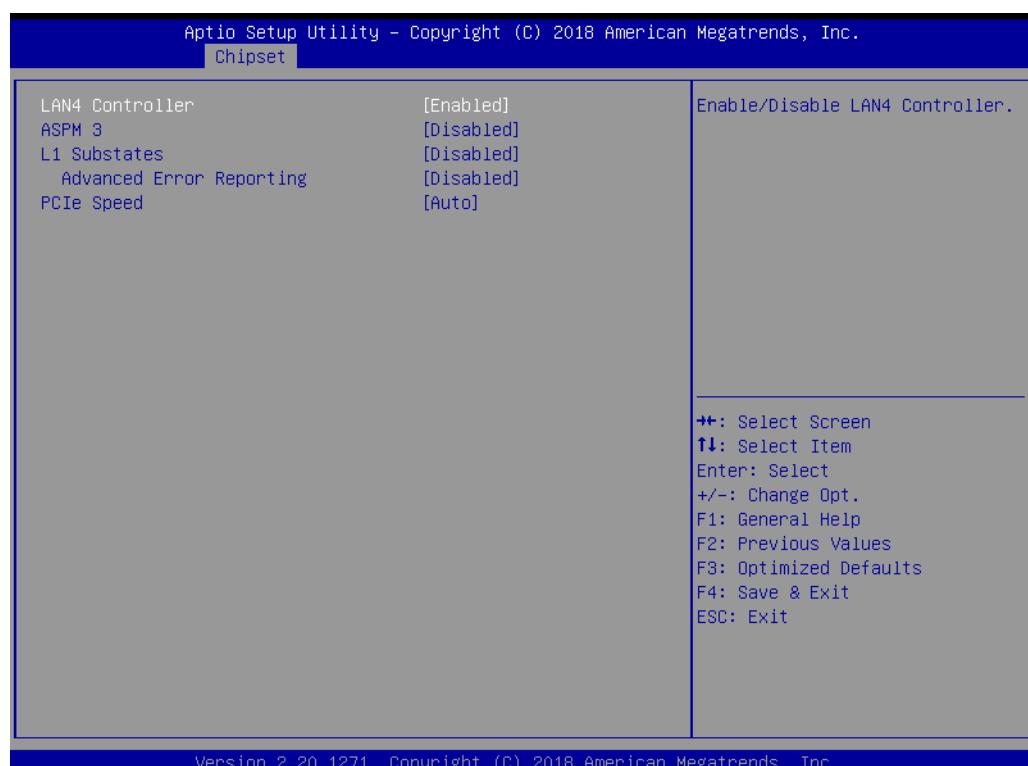


- **PCI Express Root Port 1 [ Enabled ]**  
Control the PCI Express Root Port.
- **ASPM Support [ Auto ]**  
Set the ASPM Level: Force L0s - Force all links to L0s State : AUTO - BIOS auto configure : DISABLE - Disables ASPM
- **L1 Substates PCI Express L1 Substates settings.**
- **PCIe Speed [ Auto ]**  
Select PCI Express port speed.

## ■ LAN3 Controller



## ■ LAN4 Controller

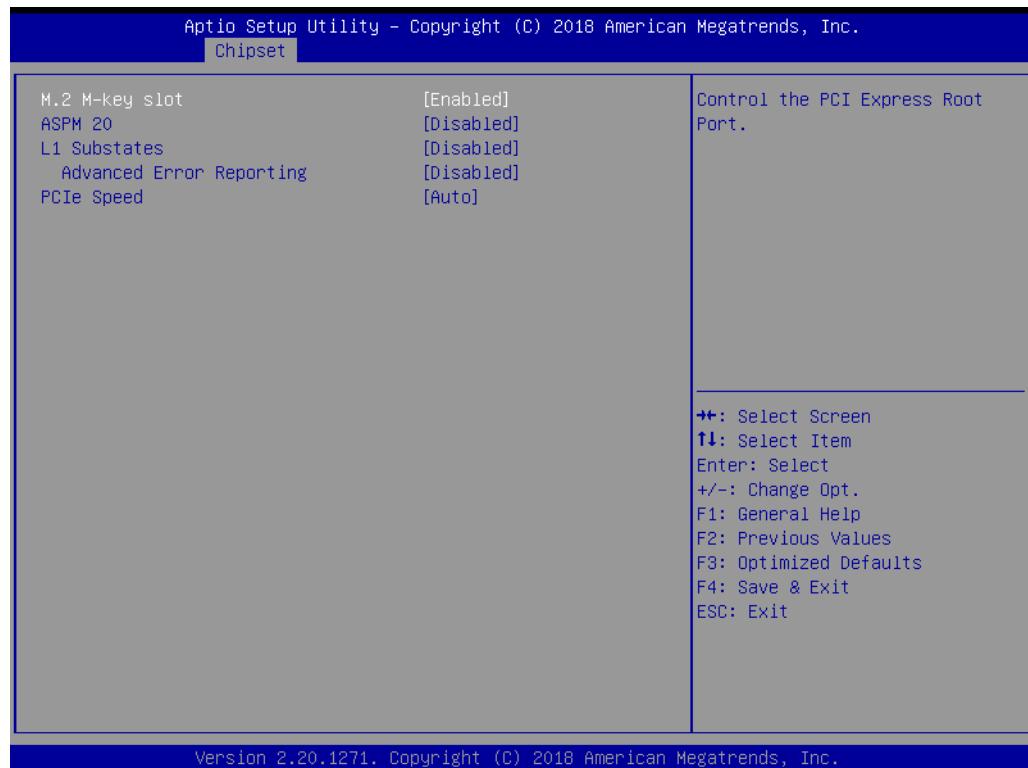


## ■ PCI Express x4 slot



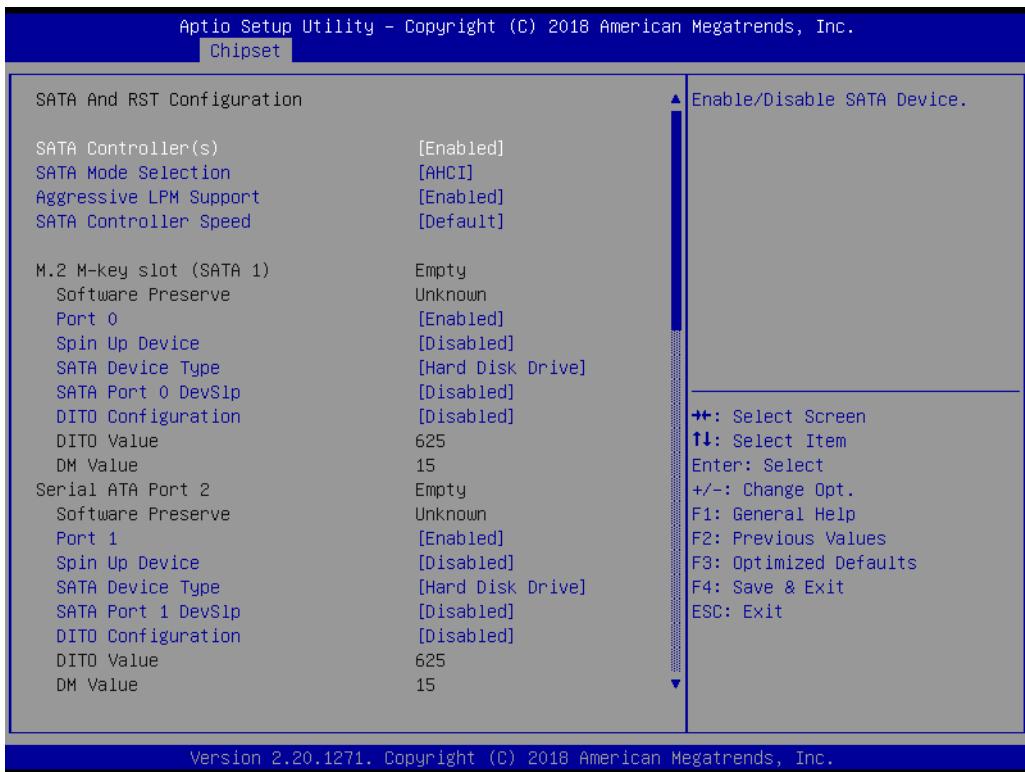
- **PCI Express x4 [ Enabled ]**  
Control the PCI Express Root Port.
- **ASPM Support [ Auto ]**  
Set the ASPM Level: Force L0s - Force all links to L0s State : AUTO - BIOS auto configure : DISABLE - Disables ASPM
- **L1 Substates PCI Express L1 Substates settings.**
- **PCIe Speed [ Auto ]**  
Select PCI Express port speed.

## ■ M.2 M-key slot

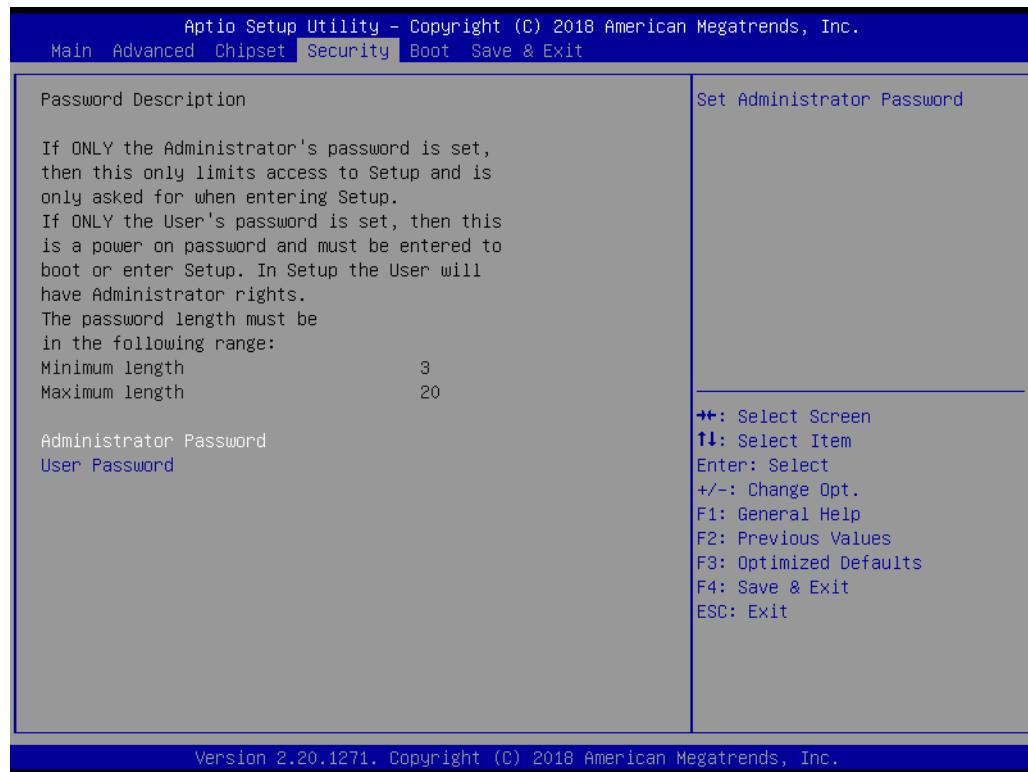


- **M.2 M-key slot [ Enabled ]**  
Control the Mini PCI Express Root Port.
- **ASPM Support [ Auto ]**  
Set the ASPM Level: Force L0s - Force all links to L0s State : AUTO - BIOS auto configure : DISABLE - Disables ASPM
- **L1 Substates PCI Express L1 Substates settings.**
- **PCIe Speed [ Auto ]**  
Select Mini PCI Express port speed.

### 3.3.2.2 SATA and RST Configuration



## 3.4 Security Setting



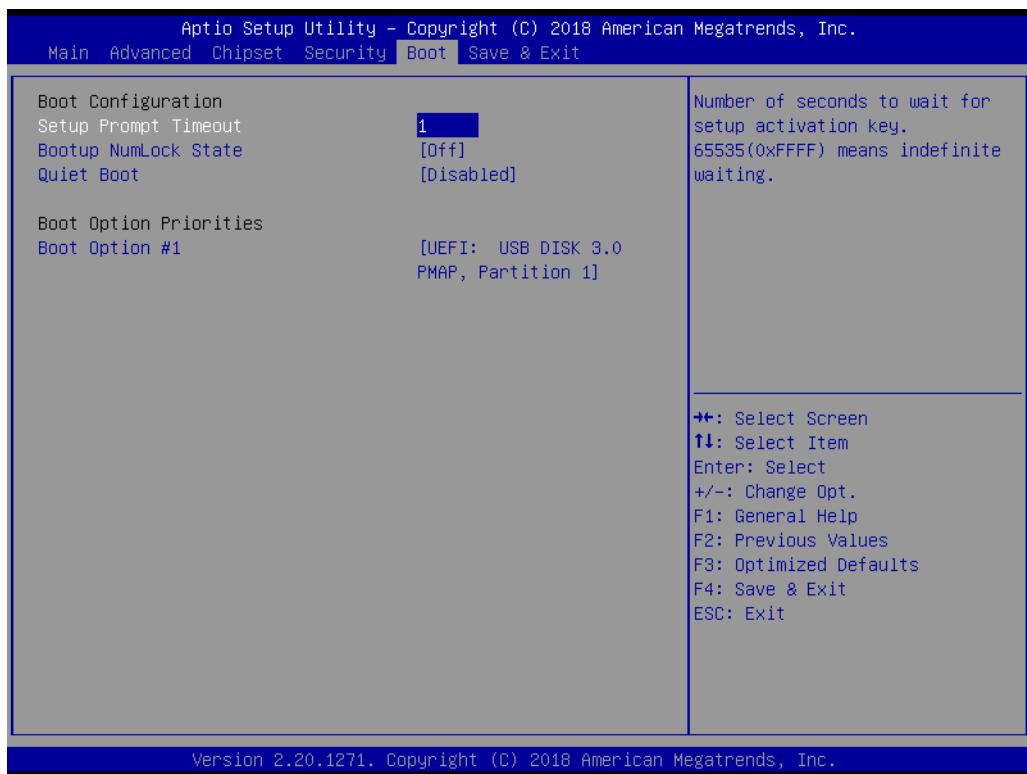
### ■ Administrator Password

Select this option and press <ENTER> to access the sub menu, and then type in the password. Set the Administrator password.

### ■ User Password

Select this option and press <ENTER> to access the sub menu, and then type in the password. Set the User Password.

## 3.5 Boot Setting



### ■ Setup Prompt Timeout

User the <+> and <-> keys to adjust the number of seconds to wait for setup activation key.

### ■ Bootup NumLock State [ On ]

On or Off power on state for the NumLock

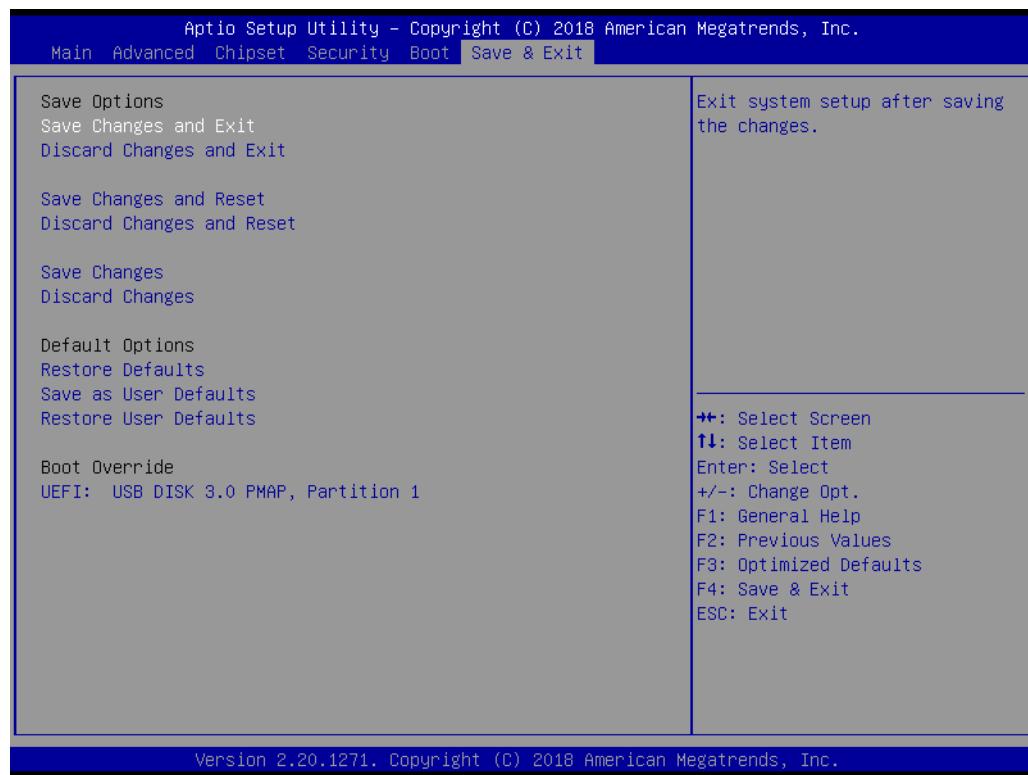
### ■ Quiet Boot [ Disabled ]

If this option is set to disabled, the BIOS displays normal POST messages. If enabled, an OEM logo is shown instead of POST messages.

### ■ Boot Option #1/#2

Choose boot priority from boot device

## 3.6 Save & Exit Configuration



### ■ Save Changes and Exit

When users have completed system configuration, select this option to save changes, exit BIOS setup menu and reboot the computer to take effect all system configuration parameters.

1. Select Exit Saving Changes from the Exit menu and press <Enter>. The following message appears: Save Configuration Changes and Exit Now? [Ok] [Cancel]
2. Select Ok or cancel.

### ■ Discard Changes and Exit

Select this option to quit Setup without making any permanent changes to the system configuration.

1. Select Exit Discarding Changes from the Exit menu and press <Enter>. The following message appears: Discard Changes and Exit Setup Now? [Ok] [Cancel]
2. Select Ok to discard changes and exit. Discard Changes  
Select Discard Changes from the Exit menu and press <Enter>.

### ■ Save Changes and Reset

When users have completed system configuration, select this option to save changes, exit BIOS setup menu and reboot the computer to take effect all system configuration parameters.

1. Select Exit Saving Changes from the Exit menu and press <Enter>. The following message appears: Save Configuration Changes and Exit Now? [Ok] [Cancel]
2. Select Ok or cancel.

### ■ Discard Changes and Reset

Select this option to quit Setup without making any permanent changes to the system configuration.

1. Select Reset Discarding Changes from the Exit menu and press <Enter>. The following message appears: Discard Changes and Exit Setup Now? [Ok] [Cancel]
  2. Select Ok to discard changes and reset. Discard Changes  
Select Discard Changes from the Exit menu and press <Enter>.
- **Restore Default**  
The BIOS automatically configures all setup items to optimal settings when users select this option. Defaults are designed for maximum system performance, but may not work best for all computer applications. In particular, do not use the Defaults if the user's computer is experiencing system configuration problems. Select Restore Defaults from the Exit menu and press <Enter>.
  - **Save as User Default**  
Save the all current settings as a user default.
  - **Restore User Default**  
Restore all settings to user default values.



# **Chapter 4**

**Software Introduction  
& Service**

## 4.1 Introduction

The mission of Advantech Embedded Software Services is to "Enhance quality of life with Advantech platforms and Microsoft® Windows® embedded technology." We enable Windows® Embedded software products on Advantech platforms to more effectively support the embedded computing community. Customers are freed from the hassle of dealing with multiple vendors (hardware suppliers, system integrators, embedded OS distributors) for projects. Our goal is to make Windows® Embedded Software solutions easily and widely available to the embedded computing community.

## 4.2 Value-Added Software Services

**Software API:** An interface that defines the ways by which an application program may request services from libraries and/or operating systems. Provides not only the underlying drivers required but also a rich set of user-friendly, intelligent and integrated interfaces, which speeds development, enhances security and offers add-on value for Advantech platforms. It plays the role of catalyst between developer and solution, and makes Advantech embedded platforms easier and simpler to adopt and operate with customer applications.

### 4.2.1 Software API

#### 4.2.1.1 Control

##### GPIO



General Purpose Input/Output is a flexible parallel interface that allows a variety of custom connections. It allows users to monitor the level of signal input or set the output status to switch on/off the device. Our API also provides Programmable GPIO, which allows developers to dynamically set the GPIO input or output status.

##### SMBus



SMBus is the System Management Bus defined by Intel Corporation in 1995. It is used in personal computers and servers for low-speed system management communications. The SMBus API allows a developer to interface a embedded system environment and transfer serial messages using the SMBus protocols, allowing multiple simultaneous device control.

#### 4.2.1.2 Display

##### Brightness Control



The Brightness Control API allows a developer to access embedded devices and easily control brightness.

##### Backlight



The Backlight API allows a developer to control the backlight (screen) on/off in embedded devices.

#### 4.2.1.3 Monitor

##### Watchdog



A watchdog timer (WDT) is a device that performs a specific operation after a certain period of time if something goes wrong and the system does not recover on its own. A watchdog timer can be programmed to perform a warm boot (restarting the system) after a certain number of seconds.

##### Hardware Monitor



The Hardware Monitor (HWM) API is a system health supervision API that inspects certain condition indexes, such as fan speed, temperature and voltage.

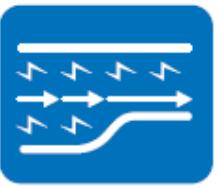
#### 4.2.1.4 Power Saving

##### CPU Speed



Makes use of Intel SpeedStep technology to save power consumption. The system will automatically adjust the CPU speed depending on the system loading.

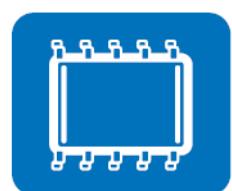
##### System Throttling



Refers to a series of methods for reducing power consumption in computers by lowering the clock frequency. This API allows the user to adjust the clock from 87.5% to 12.5%.

## 4.2.2 Software Utility

### BIOS Flash



The BIOS Flash utility allows customers to update the flash ROM BIOS version, or use it to back up current BIOS by copying it from the flash chip to a file on the customers' disk. The BIOS Flash utility also provides a command line version and an API for fast implementation into customized applications.

### Monitoring



Monitoring is a utility for customers to monitor system health, like voltage, CPU and system temperature and fan speed. These items are important to a device, if critical errors occur and are not solved immediately, permanent damage may be caused.

# **Chapter 5**

**Chipset Software  
Installation Utility**

## 5.1 Before You Begin

To facilitate the installation of the enhanced display drivers and utility software, read the instructions in this chapter carefully. The drivers for AIMB-586 are located on Advantech website. (<http://support.advantech.com/Support/>) Updates are provided via Service Packs from Microsoft\*.

Before you begin, it is important to note that most display drivers need to have the relevant software application already installed in the system prior to installing the enhanced display drivers. In addition, many of the installation procedures assume that you are familiar with both the relevant software applications and operating system commands. Review the relevant operating system commands and the pertinent sections of your application software's user manual before performing the installation.

## 5.2 Introduction

The Intel® Chipset Software Installation (CSI) utility installs the Windows INF files that outline to the operating system how the chipset components will be configured. This is needed for the proper functioning of the following features:

- Core PCI PnP services
- IDE Ultra ATA 100/66/33 and Serial ATA interface support
- Identification of Intel® chipset components in the Device Manager

**Note!** *This utility is used for the following versions of Windows, and it has to be installed **before** installing all the other drivers:*



- Windows 10 (64 bit)

## 5.3 Windows 10 Driver Setup

- When enter the website of Advantech, then search product AIMB-586. There is "Chipset" driver inside.

### Win 10(64bit) Driver for AIMB-568

Solution : Win 10(64bit) Driver for AIMB-568

Download File	Released Date	Download Site	
AIMB-586_Audio_Win10(64bit).zip	2018-09-12	Primary	Secondary
AIMB-586_Chipset_Win(64bit).zip	2018-09-12	Primary	Secondary
AIMB-586_Graphic_Win10(64bit).zip	2018-09-12	Primary	Secondary
AIMB-586_Intel LAN_Win10(64bit).zip	2018-09-12	Primary	Secondary
AIMB-586_Intel ME_AMT_Win10(64bit).zip	2018-09-12	Primary	Secondary
AIMB-586_Intel RAID_AHCI_Win10(64bit).zip	2018-09-12	Primary	Secondary
AIMB-586_Others_Win10(64bit).zip	2018-09-12	Primary	Secondary
AIMB-586_Realtek LAN_Win10(64bit).zip	2018-09-12	Primary	Secondary



# Chapter 6

VGA Setup

## 6.1 Introduction

The Intel Xeon, Core i7/i5/i3, Pentium and Celeron CPUs are embedded with an integrated graphics controller. You need to install the VGA driver to enable this function.

Optimized integrated graphic solution: With flexible Intel Graphics, versatile display options and 32-bit 3D graphics engine are supported. Dual independent displays and enhanced display modes for widescreen flat panels include extended, twin, and clone dual display modes, plus optimized 3D support delivers an intensive and realistic visual experience.

## 6.2 Windows 10 VGA Driver Installation

**Note!**

 Before installing this driver, make sure the CSI utility has been installed in your system. See Chapter 5 for information on installing the CSI utility.

When enter the website of Advantech, then search product AIMB-586.

There is "Graphic" driver inside.

Win 10(64bit) Driver for AIMB-586

Solution : Win 10(64bit) Driver for AIMB-586

Download File	Released Date	Download Site
AIMB-586_Audio_Win10(64bit).zip	2018-09-12	<a href="#">Primary</a> <a href="#">Secondary</a>
AIMB-586_Chipset_Win(64bit).zip	2018-09-12	<a href="#">Primary</a> <a href="#">Secondary</a>
AIMB-586_Graphic_Win10(64bit).zip	2018-09-12	<a href="#">Primary</a> <a href="#">Secondary</a>
AIMB-586_Intel LAN_Win10(64bit).zip	2018-09-12	<a href="#">Primary</a> <a href="#">Secondary</a>
AIMB-586_Intel ME_AMT_Win10(64bit).zip	2018-09-12	<a href="#">Primary</a> <a href="#">Secondary</a>
AIMB-586_Intel RAID_AHCI_Win10(64bit).zip	2018-09-12	<a href="#">Primary</a> <a href="#">Secondary</a>
AIMB-586_Others_Win10(64bit).zip	2018-09-12	<a href="#">Primary</a> <a href="#">Secondary</a>
AIMB-586_Realtek LAN_Win10(64bit).zip	2018-09-12	<a href="#">Primary</a> <a href="#">Secondary</a>

# Chapter 7

LAN Configuration

## 7.1 Introduction

The AIMB-586 has dual Gigabit Ethernet LANs via dedicated PCI Express x1 lanes (Intel I219LM (LAN1), I211AT (LAN2), Realtek 8111G (LAN3/LAN4)) that offer bandwidth of up to 500 MB/sec, eliminating the bottleneck of network data flow and incorporating Gigabit Ethernet at 1000 Mbps.

## 7.2 Features

- Integrated 10/100/1000 Mbps transceiver
- 10/100/1000 Mbps triple-speed MAC
- High-speed RISC core with 24-KB cache
- On-chip voltage regulation
- Wake-on-LAN (WOL) support
- PCI Express X1 host interface

## 7.3 Installation

**Note!** Before installing the LAN drivers, make sure the CSI utility has been installed on your system. See Chapter 5 for information on installing the CSI utility.

The AIMB-586's Intel i219LM (LAN1), i211AT (LAN2), Realtek 8111G(LAN3/LAN4) Gigabit integrated controllers support all major network operating systems. However, the installation procedure varies from system to system. Please find and use the section that provides the driver setup procedure for the operating system you are using.

## 7.4 Windows® 10 Driver Setup (Intel I219LM/ Intel I211AT)

When enter the website of Advantech, then search product AIMB-586.  
There is "LAN" driver inside.

### Win 10(64bit) Driver for AIMB-586

Solution : Win 10(64bit) Driver for AIMB-586

Download File	Released Date	Download Site	
AIMB-586_Audio_Win10(64bit).zip	2018-09-12	Primary	Secondary
AIMB-586_Chipset_Win(64bit).zip	2018-09-12	Primary	Secondary
AIMB-586_Graphic_Win10(64bit).zip	2018-09-12	Primary	Secondary
AIMB-586_Intel LAN_Win10(64bit).zip	2018-09-12	Primary	Secondary
AIMB-586_Intel ME_AMT_Win10(64bit).zip	2018-09-12	Primary	Secondary
AIMB-586_Intel RAID_AHCI_Win10(64bit).zip	2018-09-12	Primary	Secondary
AIMB-586_Others_Win10(64bit).zip	2018-09-12	Primary	Secondary
AIMB-586_Realtek LAN_Win10(64bit).zip	2018-09-12	Primary	Secondary



# Appendix A

Programming the  
Watchdog Timer

---

## A.1 Programming the Watchdog Timer

AIMB-586's watchdog timer can be used to monitor system software operation and take corrective action if the software fails to function within the programmed period. This section describes the operation of the watchdog timer and how to program it.

### A.1.1 Watchdog Timer Overview

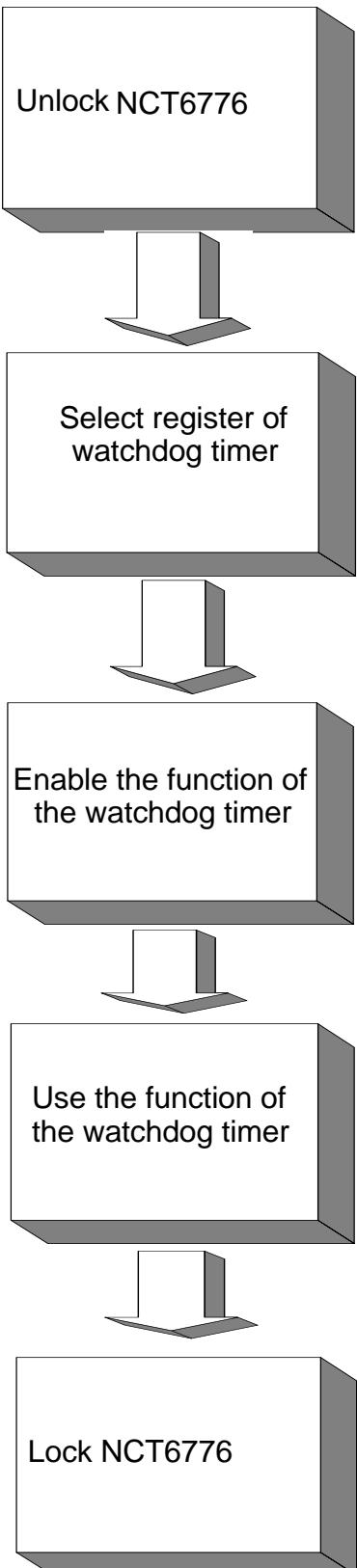
The watchdog timer is built into the super I/O controller Nuvoton NCT6776. It provides the following user-programmable functions:

- Can be enabled and disabled by user program
- Timer can be set from 1 to 255 seconds or 1 to 255 minutes
- Generates an interrupt or resets signal if the software fails to reset the timer before time-out

### A.1.2 Programming the Watchdog Timer

The I/O port address of the watchdog timer is 2E (hex) and 2F (hex). 2E (hex) is the address port. 2F (hex) is the data port. You must first assign the address of register by writing an address value into address port 2E (hex), then write/read data to/from the assigned register through data port 2F (hex).

# Appendix A Programming the Watchdog Timer



**Table A.1: Watchdog Timer Registers**

<b>Address of Register (2E) Attribute</b>		
Read/Write	Value (2F) & description	
87 (hex)	-----	Write this address to I/O address port 2E (hex) twice to unlock the NCT6106D.
07 (hex)	write	Write 08 (hex) to select register of watchdog timer.
30 (hex)	write	Write 01 (hex) to enable the function of the watchdog timer. Disabled is set as default.
F5 (hex)	write	Set seconds or minutes as units for the timer. Write 0 to bit 3: set second as counting unit. [default] Write 1 to bit 3: set minutes as counting unit.
F6 (hex)	write	0: stop timer [default] 01~FF (hex): The amount of the count, in seconds or minutes, depends on the value set in register F5 (hex). This number decides how long the watchdog timer waits for strobe before generating an interrupt or reset signal. Writing a new value to this register can reset the timer to count with the new value.
F7 (hex)	read/write	Bit 7: Write 1 to enable mouse to reset the timer, 0 to disable [default]. Bit 6: Write 1 to enable keyboard to reset the timer, 0 to disable. [default] Bit 5: Write 1 to generate a timeout signal immediately and automatically return to 0. [default=0] Bit 4: Read status of watchdog timer, 1 means timer is “timeout”.
AA (hex)	-----	Write this address to I/O port 2E (hex) to lock the watchdog timer 2.

### A.1.3 Example Program

1. Enable watchdog timer and set 10 sec. as timeout interval

```
;-----  
Mov dx,2eh ; Unlock NCT6776  
Mov al,87h  
Out dx,al  
Out dx,al  
;-----  
Mov al,07h ; Select registers of watchdog timer  
Out dx,al  
Inc dx  
Mov al,08h  
Out dx,al  
;-----  
Dec dx ; Enable the function of watchdog timer  
Mov al,30h  
Out dx,al  
Inc dx  
Mov al,01h  
Out dx,al  
;-----  
Dec dx ; Set second as counting unit  
Mov al,0f5h  
Out dx,al  
Inc dx  
In al,dx  
And al,not 08h  
Out dx,al  
;-----  
Dec dx ; Set timeout interval as 10 seconds and start counting  
Mov al,0f6h  
Out dx,al  
Inc dx  
Mov al,10  
Out dx,al  
;-----  
Dec dx ; Lock NCT6106D  
Mov al,0aah  
Out dx,al
```

2. Enable watchdog timer and set 5 minutes as timeout interval

```
;-----  
Mov dx,2eh ; Unlock NCT6776  
Mov al,87h  
Out dx,al  
Out dx,al
```

```
;-----  
Mov al,07h ; Select registers of watchdog timer  
Out dx,al  
Inc dx  
Mov al,08h  
Out dx,al  
;-----  
Dec dx ; Enable the function of watchdog timer  
Mov al,30h  
Out dx,al  
Inc dx  
Mov al,01h  
Out dx,al  
;-----  
Dec dx ; Set minute as counting unit  
Mov al,0f5h  
Out dx,al  
Inc dx  
In al,dx  
Or al,08h  
Out dx,al  
;-----  
Dec dx ; Set timeout interval as 5 minutes and start counting  
Mov al,0f6h  
Out dx,al  
Inc dx  
Mov al,5  
Out dx,al  
;-----  
Dec dx ; Lock NCT6776  
Mov al,0aah  
Out dx,al  
3.   Enable watchdog timer to be reset by mouse  
;-----  
Mov dx,2eh ; Unlock NCT6776  
Mov al,87h  
Out dx,al  
Out dx,al  
;-----  
Mov al,07h ; Select registers of watchdog timer  
Out dx,al  
Inc dx  
Mov al,08h  
Out dx,al  
;-----
```

```
Dec dx ; Enable the function of watchdog timer
Mov al,30h
Out dx,al
Inc dx
Mov al,01h
Out dx,al
;-----
Dec dx ; Enable watchdog timer to be reset by mouse
Mov al,0f7h
Out dx,al
Inc dx
In al,dx
Or al,80h
Out dx,al
;-----
Dec dx ; Lock NCT6776
Mov al,0aah
Out dx,al
4.   Enable watchdog timer to be reset by keyboard
;-----
Mov dx,2eh ; Unlock NCT6776
Mov al,87h
Out dx,al
Out dx,al
;-----
Mov al,07h ; Select registers of watchdog timer
Out dx,al
Inc dx
Mov al,08h
Out dx,al
;-----
Dec dx ; Enable the function of watchdog timer
Mov al,30h
Out dx,al
Inc dx
Mov al,01h
Out dx,al
;-----
Dec dx ; Enable watchdog timer to be strobed reset by keyboard
Mov al,0f7h
Out dx,al
Inc dx
In al,dx
Or al,40h
Out dx,al
```

```
;-----  
Dec dx ; Lock NCT6776  
Mov al,0aah  
Out dx,al  
5. Generate a time-out signal without timer counting  
;-----  
Mov dx,2eh ; Unlock NCT6776  
Mov al,87h  
Out dx,al  
Out dx,al  
;-----  
Mov al,07h ; Select registers of watchdog timer  
Out dx,al  
Inc dx  
Mov al,08h  
Out dx,al  
;-----  
Dec dx ; Enable the function of watchdog timer  
Mov al,30h  
Out dx,al  
Inc dx  
Mov al,01h  
Out dx,al  
;-----  
Dec dx ; Generate a time-out signal  
Mov al,0f7h  
Out dx,al ;Write 1 to bit 5 of F7 register  
Inc dx  
In al,dx  
Or al,20h  
Out dx,al  
;-----  
Dec dx ; Lock NCT6776  
Mov al,0aah  
Out dx,al
```

# **Appendix B**

## **Pin Assignments**

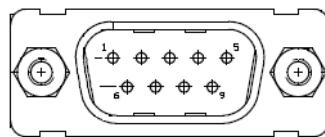
## B.1 High Definition Multimedia Interface (HDMI1)



**Table B.1: High Definition Multimedia Interface (HDMI1)**

Pin	Signal	Pin	Signal
1	HDMI1_Z_D2+	11	GND
2	GND	12	HDMI1_Z_CLK-
3	HDMI1_Z_D2-	13	x
4	HDMI1_Z_D1+	14	x
5	GND	15	HDMI1_SCL
6	HDMI1_Z_D1-	16	HDMI1_SDA
7	HDMI1_Z_D0+	17	GND
8	GND	18	+V5_HDMI
9	HDMI1_Z_D0-	19	HDMI1_HPD
10	HDMI1_Z_CLK+	20	x

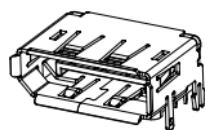
## B.2 COM1 connector (COM1)



**Table B.2: COM1 connector (COM1)**

Pin	Signal	Pin	Signal
1	DCD# [1]	6	DSR# [1]
2	RXD [1]	7	RTS# [1]
3	TXD [1]	8	CTS# [1]
4	DTR# [1]	9	RI# [1]
5	GND		

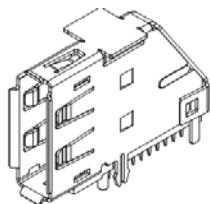
## B.3 DisplayPort1 (DP1)



**Table B.3: COM1 connector (COM1)**

Pin	Signal	Pin	Signal
1	DCD# [1]	11	GND
2	RXD [1]	12	DP1_3-
3	TXD [1]	13	DP1_AUX_EN#
4	DTR# [1]	14	GND
5		15	DP1_AUX+
6		16	GND
7		17	DP1_AUX-
8		18	DP1_HPD
9		19	GND
10		20	+V3.3_DP1

## B.4 DisplayPort2 (DP2)



**Table B.4: DisplayPort2 (DP2)**

Pin	Signal	Pin	Signal
1	DP2_0+	11	GND
2	GND	12	DP2_3-
3	DP2_0-	13	DP2_AUX_EN#
4	DP2_1+	14	GND
5	GND	15	DP2_AUX+
6	DP2_1-	16	GND
7	DP2_2+	17	DP2_AUX-
8	GND	18	DP2_HPD
9	DP2_2-	19	GND
10	DP2_3+	20	+V3.3_DP1

## B.5 RJ45 Port 3/Port4 connector (LAN34)

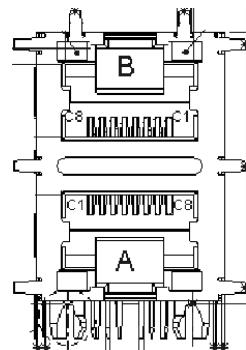
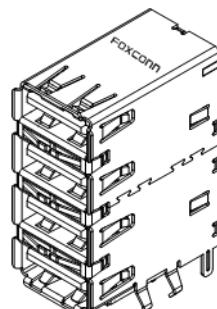


Table B.5: RJ45 Port 3/Port4 connector (LAN34)

Pin	Signal	Pin	Signal
A1	MDI_LAN3_DP0	B6	MDI_LAN4_DN2
A2	MDI_LAN3_DN0	B7	MDI_LAN4_DP3
A3	MDI_LAN3_DP1	B8	MDI_LAN4_DN3
A4	MDI_LAN3_DN1	B9	LAN4_CON
A5	MDI_LAN3_DP2	B10	GND
A6	MDI_LAN3_DN2	11	LAN4_LED0_100M#
A7	MDI_LAN3_DP3	12	LAN4_LED2_1G#
A8	MDI_LAN3_DN3	13	+V3.3_DUAL
A9	LAN3_CON	14	LAN4_LED1_ACT#
A10	GND	15	LAN3_LED2_100M#
B1	MDI_LAN4_DP0	16	LAN3_LED1_1G#
B2	MDI_LAN4_DN0	17	+V3.3_DUAL
B3	MDI_LAN4_DP1	18	LAN3_LED0_ACT#
B4	MDI_LAN4_DN1		
B5	MDI_LAN4_DP2		

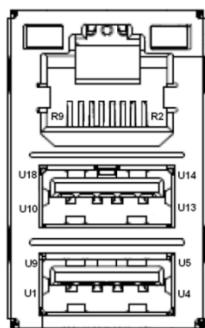
## B.6 Universal Serial Bus Port 5 / 6 / 7 / 8 (USB5678)



**Table B.6: Universal Serial Bus Port 5 / 6 / 7 / 8 (USB5678)**

Pin	Signal	Pin	Signal
A1	+USBV3 (*)	C1	+USBV3 (*)
A2	USB_CM_N5	C2	USB_CM_N7
A3	USB_CM_P5	C3	USB_CM_P7
A4	GND	C4	GND
B1	+USBV3 (*)	D1	+USBV3 (*)
B2	USB_CM_N6	D2	USB_CM_N8
B3	USB_CM_P6	D3	USB_CM_P8
B4	GND	D4	GND

## B.7 RJ45 + USB3.1 stack connector (LAN1\_USB12)

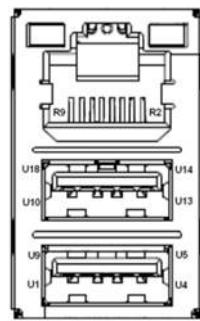
**Table B.7: RJ45 + USB3.1 stack connector (LAN1\_USB12)**

Pin	Signal	Pin	Signal
U1	VBUS (*)	U10	VBUS (*)
U2	D_-1	U11	D_-2
U3	D+_-1	U12	D+_-2
U4	GND	U13	GND
U5	RX_-1	U14	RX_-2
U6	RX+_-1	U15	RX+_-2
U7	GND	U16	GND
U8	TX_-1	U17	TX_-2
U9	TX+_-1	U18	TX+_-2

(\*) Depends on JUSBPWR2 Jump Setting

Pin	Signal	Pin	Signal
R2	MDI_0+	R6	MDI_2+
R3	MDI_0-	R7	MDI_2-
R4	MDI_1+	R8	MDI_3+
R5	MDI_1-	R9	MDI_3-

## B.8 RJ45 + USB3.0 stack connector (LAN2\_USB34)



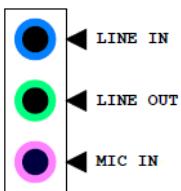
**Table B.8: RJ45 + USB3.0 stack connector (LAN2\_USB34)**

Pin	Signal	Pin	Signal
U1	VBUS (*)	U10	VBUS (*)
U2	D-_3	U11	D-_4
U3	D+_3	U12	D+_4
U4	GND	U13	GND
U5	RX-_3	U14	RX-_4
U6	RX+_3	U15	RX+_4
U7	GND	U16	GND
U8	TX-_3	U17	TX-_4
U9	TX+_3	U18	TX+_4

(\*) Depends on JUSBPWR1 Jump Setting

Pin	Signal	Pin	Signal
R2	MDI_0+	R6	MDI_2+
R3	MDI_0-	R7	MDI_2-
R4	MDI_1+	R8	MDI_3+
R5	MDI_1-	R9	MDI_3-

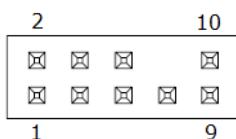
## B.9 HD Audio Interface (AUDIO1)



**Table B.9: HD Audio Interface (AUDIO1)**

Pin	Signal
1	MIC IN
2	LINE OUT
3	LINE IN

## B.10 Front panel audio pin header (FPAUD1)



**Table B.10: Front panel audio pin header (FPAUD1)**

Pin	Signal	Pin	Signal
1	MIC IN-L	2	GND
3	MIC IN-R	4	FPAUD_DETECT#
5	LINE OUT-R	6	SENSE R1
7	SENSE	8	KEY
9	LINE OUT-L	10	SENSE R2

## B.11 USB Power selection header #1 (JUSBPWR1)



**Table B.11: USB Power selection header #1 (JUSBPWR1)**

Pin	Signal
1	+VDUAL
2	Advantech define
3	+V5

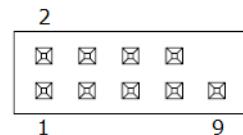
## B.12 HD Audio interface (SPDIF1)



**Table B.12: HD Audio interface (SPDIF1)**

Pin	Signal
1	+5V
2	KEY
3	SPDIF OUT
4	GND

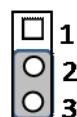
## B.13 LAN LED (LANLED1)



**Table B.13: LAN LED (LANLED1)**

Pin	Signal	Pin	Signal
1	LAN1 ACTIVE	2	LAN2 ACTIVE
3	LAN1 LED PWR	4	LAN2 LED PWR
5	LAN1 LINK1000	6	LAN2 LINK1000
7	LAN1 LINK100	8	LAN2 LINK100
9	+3.3VSB		

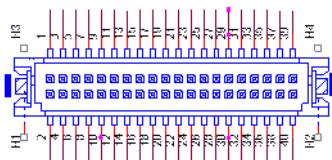
## B.14 LVDS VESA, JEIDA format selection pin header (JLVDS\_VCON1)



**Table B.14: LVDS VESA, JEIDA format selection pin header (JLVDS\_VCON1)**

Pin	Signal
1	+3.3V
2	OPTION
3	GND

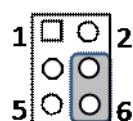
## B.15 LVDS Panel Connector (LVDS1)



**Table B.15: LVDS Panel Connector (LVDS1)**

Pin	Signal	Pin	Signal
1	+VDD_LVDS1	2	+VDD_LVDS1
3	LVDS_DET#	4	GND
5	+VDD_LVDS1	6	+VDD_LVDS1
7	LVDS1_A0N	8	LVDS1_A4N
9	LVDS1_A0P	10	LVDS1_A4P
11	GND	12	GND
13	LVDS1_A1N	14	LVDS1_A5N
15	LVDS1_A1P	16	LVDS1_A5P
17	GND	18	GND
19	LVDS1_A2N	20	LVDS1_A6N
21	LVDS1_A2P	22	LVDS1_A6P
23	GND	24	GND
25	LVDS1_CLK1N	26	LVDS1_CLK2N
27	LVDS1_CLK1P	28	LVDS1_CLK2P
29	GND	30	GND
31	LVDS1_SCD	32	LVDS1_SDD
33	GND	34	LVDS1_PIN34
35	LVDS1_A3N	36	LVDS1_A7N
37	LVDS1_A3P	38	LVDS1_A7P
39	LVDS1_ENBKL	40	LVDS1_VCON

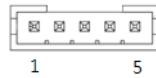
## B.16 LVDS Panel Voltage Selection (JLVDS1)



**Table B.16: LVDS Panel Voltage Selection (JLVDS1)**

Pin	Signal	Pin	Signal
1	NC	2	+5V
3	+12V	4	EDP1 VDD
5	NC	6	+3.3V

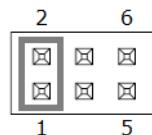
## B.17 LVDS Backlight inverter power connector (INV1)



**Table B.17: LVDS Backlight inverter power connector (INV1)**

Pin	Signal
1	+12V
2	GND
3	BKL EN
4	BKL CTRL
5	+5V

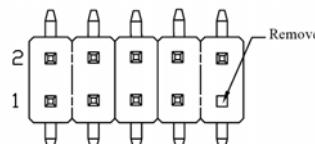
## B.18 COM3 RI# selection pin header (JSETCOM3\_V1)



**Table B.18: COM3 RI# selection pin header (JSETCOM3\_V1)**

Pin	Signal	Pin	Signal
1	RI# [1]	2	Advantech define
3	Advantech define	4	+5V
5	+12V	6	Advantech define

## B.19 USB 2.0 Connector (USB910)

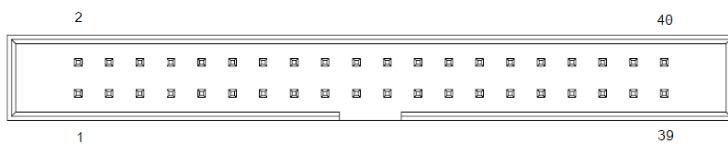


**Table B.19: USB 2.0 Connector (USB910)**

Pin	Signal	Pin	Signal
1	VBUS (*)	2	VBUS (*)
3	PCIE_USB_D2-	4	PCIE_USB_D1-
5	PCIE_USB_D2+	6	PCIE_USB_D1+
7	GND	8	GND

(\*) Depends on JUSBPWR2 Jump Setting

## B.20 COM3 ~ COM6 box header (COM3456)



**Table B.20: COM3 ~ COM6 box header (COM3456)**

Pin	Signal	Pin	Signal
1	DCD# [3]	2	DSR# [3]
3	RXD [3]	4	RST# [3]
5	TXD [3]	6	CTS# [3]
7	DTR# [3]	8	RI# [3]
9	GND	10	GND
11	DCD# [4]	12	DSR# [4]
13	RXD [4]	14	RST# [4]
15	TXD [4]	16	CTS# [4]
17	DTR# [4]	18	RI# [4]
19	GND	20	GND
21	DCD# [5]	22	DSR# [5]
23	RXD [5]	24	RST# [5]
25	TXD [5]	26	CTS# [5]
27	DTR# [5]	28	RI# [5]
29	GND	30	GND
31	DCD# [6]	32	DSR# [6]
33	RXD [6]	34	RST# [6]
35	TXD [6]	36	CTS# [6]
37	DTR# [6]	38	RI# [6]
39	GND	40	GND

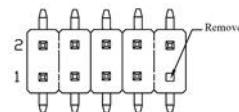
## B.21 SMBUS connector from PCH (SMBUS1)



**Table B.21: SMBUS connector from PCH (SMBUS1)**

Pin	Signal
1	+5VSB
2	SMB CLK
3	SMB DAT
4	GND

## B.22 USB 2.0 Connector (USB1112)

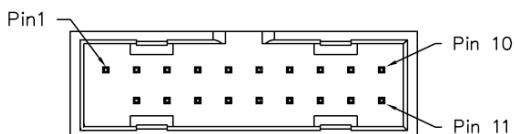


**Table B.22: USB 2.0 Connector (USB1112)**

Pin	Signal	Pin	Signal
1	VBUS (*)	2	VBUS (*)
3	USB_CM_N12	4	USB_CM_N13
5	USB_CM_P12	6	USB_CM_P13
7	GND	8	GND

(\*) Depends on JUSBPWR2 Jump Setting

## B.23 Dual port USB3.0 header (USB1314)

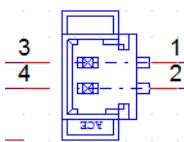


**Table B.23: Dual port USB3.0 header (USB1314)**

Pin	Signal	Pin	Signal
1	VBUS (*)	11	D+_11
2	RX-_5	12	D-_11
3	RX+_5	13	GND
4	GND	14	TX+_6
5	TX-_5	15	TX-_6
6	TX+_9	16	GND
7	GND	17	RX+_6
8	D-_10	18	RX-_6
9	D+_10	19	VBUS (*)
10	NC		

(\*) Depends on JUSBPWR2 Jump Setting

## B.24 CMOS battery connector (BAT1)



**Table B.24: CMOS battery connector (BAT1)**

Pin	Signal
1	VBAT
2	GND

## B.25 COMS Mode selection (JCOMS1)



**Table B.25: COMS Mode selection (JCOMS1)**

Pin	Signal
1	VBAT
2	RTC RESET#
3	GND

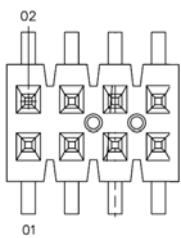
## B.26 USB Power selection header #2 (JUSBPWR2)



**Table B.26: USB Power selection header #2 (JUSBPWR2)**

Pin	Signal
1	+VDUAL
2	Advantech define
3	+V5

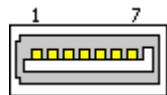
## B.27 SPI Pin Header (SPI\_CN1)



**Table B.27: SPI Pin Header (SPI\_CN1)**

Pin	Signal	Pin	Signal
1	+3.3VSB	2	GND
3	CS#	4	SCLK
5	MISO	6	MOSI
		8	NC

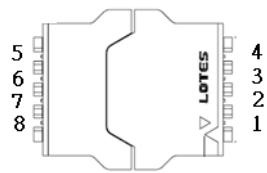
## B.28 Serial ATA interface connector (SATA8)



**Table B.28: Serial ATA interface connector (SATA8)**

Pin	Signal
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND

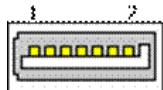
## B.29 SPI BIOS flash socket (SPI1)



**Table B.29: SPI BIOS flash socket (SPI1)**

Pin	Signal	Pin	Signal
1	CS#	5	MOSI
2	MISO	6	SCLK
3	WP# / IO2	7	HOLD# / IO3
4	GND	8	+V3.3_SPI

## B.30 Serial ATA interface connector (SATA7)



**Table B.30: Serial ATA interface connector (SATA7)**

Pin	Signal
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND

## B.31 Power switch/HDD LED/SMBus/Speaker pin header (JFP1)

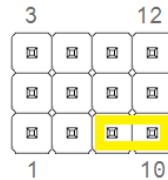


Table B.31: Power switch/HDD LED/SMBus/Speaker pin header (JFP1)

Pin	Signal	Pin	Signal
1	+5V	2	HDD LED+
3	Power Button+	4	SPK_P2
5	HDD LED-	6	Power Button-
7	SPK_P3	8	SMB_DATA
9	System Reset+	10	SPK_P4
11	SMB_CLK	12	System Reset-

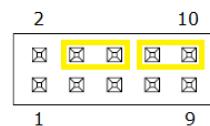
## B.32 Power LED and keyboard lock pin header (JFP2)



Table B.32: Power LED and keyboard lock pin header (JFP2)

Pin	Signal
1	LED Power
2	NC
3	GND
4	Keyboard Lock
5	GND

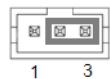
## B.33 CIR interface, Watchdog timer output and OBS beep (JIR1+JOBS1+JWDT1)



**Table B.33: CIR interface, Watchdog timer output and OBS beep (JIR1+JOBS1+JWDT1)**

<b>Pin</b>	<b>Signal</b>	<b>Pin</b>	<b>Signal</b>
1	+5V	2	NC
3	NC	4	Watch Dog Reset# output
5	IRRX	6	System Reset input#
7	GND	8	SIO Warning Beep output
9	IRTX	10	SP1 Buzzer Beep input

## B.34 AT/ATX Mode selection (PSON1)

**Table B.34: AT/ATX Mode selection (PSON1)**

<b>Pin</b>	<b>Signal</b>
1	AT
2	+3.3V
3	ATX

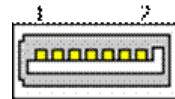
## B.35 Alarm Board/CMM Power Connector (VOLT1)



**Table B.35: AT/ATX Mode selection (PSON1)**

Pin	Signal
1	+5VSB
2	GND
3	GND
4	-5V
5	+5V
6	+3.3V
7	-12V
8	+12V

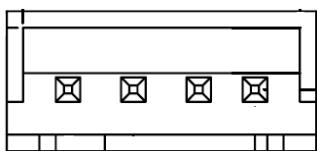
## B.36 Serial ATA interface connector (SATA1~6)



**Table B.36: Serial ATA interface connector (SATA1~6)**

Pin	Signal
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND

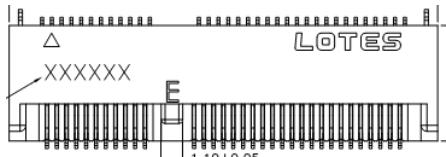
## B.37 SATA Power Connector (SATA\_PWR1)



**Table B.37: SATA Power Connector (SATA\_PWR1)**

Pin	Signal
1	+V5
2	GND
3	GND
4	+V12

## B.38 M.2 E Key connector (M2E1)



**Table B.38: M.2 E Key connector (M2E1)**

Pin	Signal	Pin	Signal
1	GND	2	3.3V
3	USB_D+	4	3.3V
5	USB_D-	6	LED1# (I)(OD)
7	GND	8	PCM_CLK/I2S SCK (O/I)(0/1.8V)
9	CNV_WR_D1-	10	PCM_SYNC/I2S WS (I/O)(0/1.8V)
11	CNV_WR_D1+	12	PCM_IN/I2S SD_IN (I)(0/1.8V)
13	GND	14	PCM_OUT/I2S SD_OUT (O)(0/1.8V)
15	CNV_WR_D0-	16	LED2# (I)(OD)
17	CNV_WR_D0+	18	GND
19	GND	20	UART_WAKE# (I)(0/3.3V)
21	CNV_WR_CLK-	22	UART_RXD (I)(0/1.8V)
23	CNV_WR_CLK+	24	Connector Key
25	Connector Key	26	Connector Key
27	Connector Key	28	Connector Key
29	Connector Key	30	Connector Key
31	Connector Key	32	CNV_RGI_DT
33	GND	34	CNV_RGI_RSP
35	PETp0	36	CNV_BRI_DT
37	PETn0	38	PCH_CLINK_RST#
39	GND	40	PCH_CLINK_DATA
41	PERp0	42	PCH_CLINK_CLK
43	PERn0	44	CNV_GNSS_BLANKING
45	GND	46	CNV_MUART2_TXD
47	REFCLKp0	48	CNV_MUART2_RXD
49	REFCLKn0	50	SUSCLK(32kHz) (O)(0/3.3V)
51	GND	52	PERST0# (O)(0/3.3V)
53	CLKREQ0# (I/O)(0/3.3V)	54	W_DISABLE2# (O)(0/3.3V)
55	PEWAKE0# (I/O)(0/3.3V)	56	W_DISABLE1# (O)(0/3.3V)

**Table B.38: M.2 E Key connector (M2E1)**

57	GND	58	RESERVED
59	RESERVED/PETp1	60	RESERVED
61	RESERVED/PETn1	62	RESERVED
63	GND	64	M.2_38P4M_REFCLK
65	RESERVED/PERp1	66	RESERVED
67	RESERVED/PERn1	68	RESERVED
69	GND	70	PCIE_WAKE#
71	RESERVED/REFCLKp1	72	3.3V
73	RESERVED/REFCLKn1	74	3.3V
75	GND		

## B.39 M.2 M Key connector (M2M1)

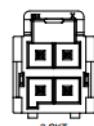
**Table B.39: M.2 M Key connector (M2M1)**

Pin	Signal	Pin	Signal
1	GND	2	3.3V
3	GND	4	3.3V
5	PERn3	6	N/C
7	PERp3	8	N/C
9	GND	10	DAS/DSS# (I/O)/LED1# (I)(0/3.3V)
11	PETn3	12	3.3V
13	PETp3	14	3.3V
15	GND	16	3.3V
17	PERn2	18	3.3V
19	PERp2	20	N/C
21	GND	22	N/C
23	PETn2	24	N/C
25	PETp2	26	N/C
27	GND	28	N/C
29	PERn1	30	N/C
31	PERp1	32	N/C
33	GND	34	N/C
35	PETn1	36	N/C
37	PETp1	38	DEVSLP (O)
39	GND	40	N/C
41	PERn0/SATA-B+	42	N/C
43	PERp0/SATA-B-	44	N/C

**Table B.39: M.2 M Key connector (M2M1)**

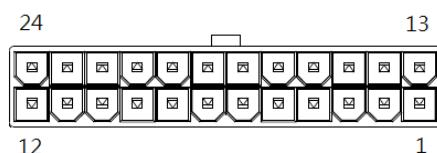
45	GND	46	N/C
47	PETn0/SATA-A-	48	N/C
49	PETp0/SATA-A+	50	PERST# (O)(0/3.3V) or N/C
51	GND	52	CLKREQ# (I/O)(0/3.3V) or N/C
53	REFCLKn	54	PEWAKE# (I/O)(0/3.3V) or N/C
55	REFCLKp	56	N/C
57	GND	58	N/C
59	Connector Key	60	Connector Key
61	Connector Key	62	Connector Key
63	Connector Key	64	Connector Key
65	Connector Key	66	Connector Key
67	N/C	68	SUSCLK(32kHz) (O)(0/3.3V)
69	PEDET (NC-PCIe/ GND-SATA)	70	3.3V
71	GND	72	3.3V
73	GND	74	3.3V
75	GND		

## B.40 SATA Power Connector (SATA\_PWR2)

**Table B.40: SATA Power Connector (SATA\_PWR2)**

Pin	Signal
1	+V5
2	+V5
3	GND
4	GND

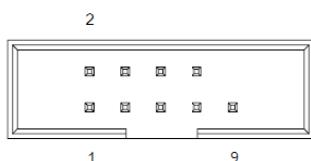
## B.41 ATX 24pin power connector (EATXPWR1)



**Table B.41: ATX 24pin power connector (EATXPWR1)**

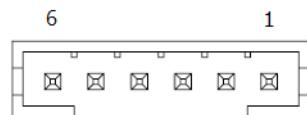
<b>Pin</b>	<b>Signal</b>	<b>Pin</b>	<b>Signal</b>
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	GND	15	GND
4	+5V	16	PSON#
5	GND	17	GND
6	+5V	18	GND
7	GND	19	GND
8	PWROK	20	-5V
9	+5VSB	21	+5V
10	+12V	22	+5V
11	+12V	23	+5V
12	+3.3V	24	GND

## B.42 COM2 box header (COM2)

**Table B.42: COM2 box header (COM2)**

<b>Pin</b>	<b>Signal</b>	<b>Pin</b>	<b>Signal</b>
1	DCD# [2]	2	DSR# [2]
3	RXD [2]	4	RST# [2]
5	TXD [2]	6	CTS# [2]
7	DTR# [2]	8	RI# [2]
9	GND		

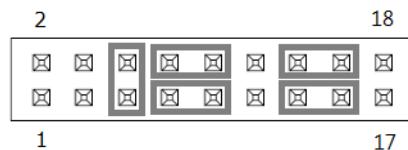
## B.43 Keyboard & Mouse connector (KBMS1)



**Table B.43: Keyboard & Mouse connector (KBMS1)**

Pin	Signal
1	KB_CLK#
2	KB_DAT#
3	MS_CLK#
4	GND
5	VCC (+5VSB)
6	MS_DAT#

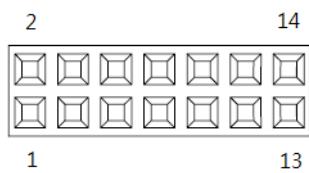
## B.44 COM2 RS232, RS422, RS485 selection pin header (JSETCOM2)



**Table B.44: COM2 RS232, RS422, RS485 selection pin header (JSETCOM2)**

Pin	Signal	Pin	Signal
1	UART_SIN [2]	2	RXD_RS485
3	UART_SIN [2]	4	RXD_RS422
5	UART_SIN [2]	6	RXD_RS232
7	DCDB	8	SOUT [2]
9	COM2_DCD#	10	COM2_SOUT
11	COM2_RXD485-	12	COM2_RXD485+
13	SIN [B]	14	DTR [B]
15	COM2_SIN	16	COM2_DTR#
17	COM2_TXD485+	18	COM2_RXD485-

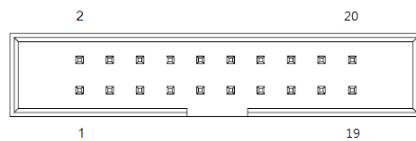
## B.45 Low pin count interface connector (LPC1)



**Table B.45: Low pin count interface connector (LPC1)**

Pin	Signal	Pin	Signal
1	CLK (24MHz)	2	AD1
3	RESET#	4	AD0
5	FRAME#	6	+3.3V
7	AD3	8	GND
9	AD2	10	SMB CLK
11	SERIRQ	12	SMB DAT
13	+5VSB	14	+5V

## B.46 16-bits General Purpose I/O pin header (GPIO1)



**Table B.46: 16-bits General Purpose I/O pin header (GPIO1)**

Pin	Signal	Pin	Signal
1	GPIO0	2	GPIO8
3	GPIO1	4	GPIO9
5	GPIO2	6	GPIO10
7	GPIO3	8	GPIO11
9	GPIO4	10	GPIO12
11	GPIO5	12	GPIO13
13	GPIO6	14	GPIO14
15	GPIO7	16	GPIO15
17	+5VSB	18	GND
19	+5VSB	20	GND

## B.47 Case Open selection pin header (JCASEOP\_SW1)



**Table B.47: Case Open selection pin header (JCASEOP\_SW1)**

Pin	Signal
1	Normal Open
2	Advantech define
3	Normal Close

## B.48 Case Open connector (JCASE1)



**Table B.48: Case Open connector (JCASE1)**

Pin	Signal
1	Case Open
2	GND

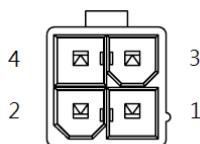
## B.49 ATX 8 Pin main power connector (ATX12V2)



**Table B.49: ATX 8 Pin main power connector (ATX12V2)**

Pin	Signal	Pin	Signal
1	GND	2	+12V
3	GND	4	+12V
5	GND	6	+12V
7	GND#	8	+12V

## B.50 ATX 4 Pin main power connector (ATX12V1)



**Table B.50: ATX 4 Pin main power connector (ATX12V1)**

Pin	Signal
1	GND
2	GND
3	+12V
4	+12V

## B.51 CPU FAN connector (CPUFAN1)



**Table B.51: CPU FAN connector (CPUFAN1)**

Pin	Signal
1	GND
2	CPU FAN VCC
3	CPU FAN SPEED
4	CPU FAN PWM

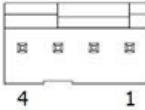
## B.52 System Fan #3 connector (SYSFAN3)



**Table B.52: System Fan #3 connector (SYSFAN3)**

Pin	Signal
1	GND
2	SYSTEM FAN VCC
3	SYSTEM FAN SPEED
4	SYSTEM FAN PWM

## B.53 System Fan #1 connector (SYSFAN1)



**Table B.53: System Fan #1 connector (SYSFAN1)**

Pin	Signal
1	GND
2	SYSTEM FAN VCC
3	SYSTEM FAN SPEED
4	SYSTEM FAN PWM

## B.54 System Fan #2 connector (SYSFAN2)



**Table B.54: System Fan #2 connector (SYSFAN2)**

Pin	Signal
1	GND
2	SYSTEM FAN VCC
3	SYSTEM FAN SPEED
4	SYSTEM FAN PWM

## B.55 System Fan #4 connector (SYSFAN4)



**Table B.55: System Fan #4 connector (SYSFAN4)**

Pin	Signal
1	GND
2	SYSTEM FAN VCC
3	SYSTEM FAN SPEED
4	SYSTEM FAN PWM

### Jumper Setting List:

**Table B.56: Jumper Setting List**

	Description	Part Reference
1	USB Power selection for USB910, USB1112, USB1314	JUSBPWR2
2	USB Power selection for LAN1_USB12, LAN2_USB34, USB5678	JUSBPWR1
3	LVDS VESA, JEIDA format selection pin header	JLVDs_VCON1
4	RTC / CMOS clear	JCOMS1
5	PWRBTN#/ RESET#/HDD LED/ Serial bus from HW monitor IC/Internal Buzzer / External Speaker header	JFP1
6	CIR interface, Watchdog timer output and OBS beep	JIR1+JOBS1+JWDT1
7	AT / ATX Mode selection	PSON1
8	COM2 RS232, RS422, RS485 selection pin header	JSETCOM2
9	Case open selection pin header	JCASEOP_SW1
10	COM1_RI# Pin selection pin header	JSETCOM1_V1
11	LVDS Panel Voltage Selection	JLVDs1

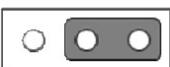
### B.56 USB Power selection for USB910, USB1112, USB1314 (JUSBPWR2)

**Table B.57: USB Power selection for USB910, USB1112, USB1314 (JUSBPWR2)**

Function	Jumper Setting						
Set USB VBUS as +5VSB (Default)	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>1</td><td>2</td><td>3</td></tr> <tr> <td><input type="radio"/></td><td><input type="radio"/></td><td><input type="radio"/></td></tr> </table>	1	2	3	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
1	2	3					
<input type="radio"/>	<input type="radio"/>	<input type="radio"/>					
Set USB VBUS as +5V	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>1</td><td>2</td><td>3</td></tr> <tr> <td><input type="radio"/></td><td><input checked="" type="radio"/></td><td><input type="radio"/></td></tr> </table>	1	2	3	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>
1	2	3					
<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>					

## B.57 USB Power selection for LAN1\_USB12, LAN2\_USB34, USB5678 (JUSBPWR1)

**Table B.58: USB Power selection for LAN1\_USB12, LAN2\_USB34, USB5678 (JUSBPWR1)**

Function	Jumper Setting
Set USB VBUS as +5VSB (Default)	1    2    3 
Set USB VBUS as +5V	1    2    3 

## B.58 LVDS VESA, JEIDA format selection pin header (JLVDS\_VCON1)

**Table B.59: LVDS VESA, JEIDA format selection pin header (JLVDS\_VCON1)**

Function	Jumper Setting
Setting :+V3.3	1    2    3 
Setting :GND (Default)	1    2    3 

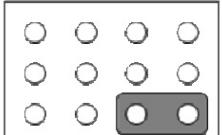
## B.59 CMOS clear (JCOMS1)

**Table B.60: CMOS clear (JCOMS1)**

Function	Jumper Setting
Keep CMOS Data (Default)	1    2    3 
Clear CMOS Data	1    2    3 

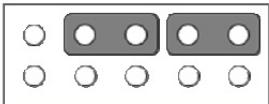
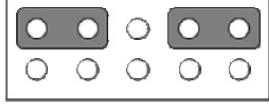
## B.60 PWRBTN#/ RESET#/HDD LED/ Serial bus from HW monitor IC/Internal Buzzer / External Speaker header (JFP1)

**Table B.61: PWRBTN#/ RESET#/HDD LED/ Serial bus from HW monitor IC/Internal Buzzer / External Speaker header (JFP1)**

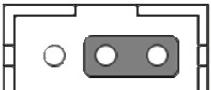
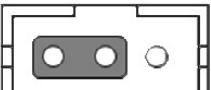
Function	Jumper Setting				
	3	12			
Internal Buzzer (Default)		1	7	10	

## B.61 CIR interface, Watchdog timer output and OBS beep (JIR1+JOBS1+JWDT1)

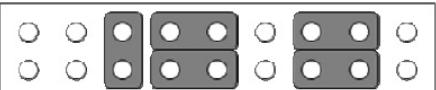
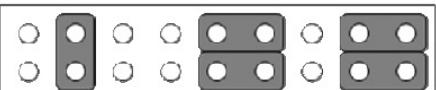
**Table B.62: CIR interface, Watchdog timer output and OBS beep (JIR1+JOBS1+JWDT1)**

Function	Jumper Setting				
	2	4	6	8	10
Watchdog Timer Output (4-6) (Default) OBS BEEP (8-10) (Default)		1	3	5	7
Watchdog Timer Disable (2-4) OBS BEEP(8-10) (Default)		1	3	5	7

## B.62 AT / ATX Mode selection (PSON1)

Table B.63: AT / ATX Mode selection (PSON1)		
Function	Jumper Setting	
ATX Mode (Default)		1    2    3
AT Mode		1    2    3

## B.63 COM2 RS232, RS422, RS485 selection pin header (JSETCOM2)

Table B.64: COM2 RS232, RS422, RS485 selection pin header (JSETCOM2)																				
Function		Jumper Setting																		
		2	4	6	8	10	12	14	16	18	2	4	6	8	10	12	14	16	18	
RS-232 Mode (Default) (5-6) (7-9) (8-10) (13-15) (14-16)			1	3	5	7	9	11	13	15	17	1	3	5	7	9	11	13	15	17
RS-422 Mode (3-4) (9-11) (10-12) (15-17) (16-18)			1	3	5	7	9	11	13	15	17	2	4	6	8	10	12	14	16	18
RS-485 Mode (1-2) (9-11) (10-12) (15-17) (16-18)			1	3	5	7	9	11	13	15	17	2	4	6	8	10	12	14	16	18

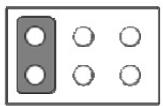
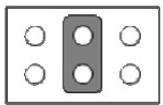
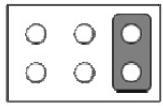
## B.64 Case open selection pin header (JCASEOP\_SW1)

**Table B.65: Case open selection pin header (JCASEOP\_SW1)**

Function	Jumper Setting
Normal Close	1    2    3 
Normal Open (Default)	1    2    3 

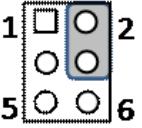
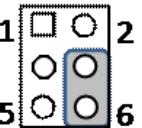
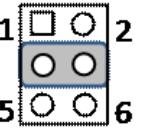
## B.65 COM1\_RI# Pin RI# / 5V / 12V selection (JSETCOM1\_V1)

**Table B.66: COM1\_RI# Pin RI# / 5V / 12V selection (JSETCOM1\_V1)**

Function	Jumper Setting
Jumper position for RI# (Default)	2    4    6  1    3    5
Jumper position for +5V	2    4    6  1    3    5
Jumper position for +12V	2    4    6  1    3    5

## B.66 LVDS Panel Voltage Selection (JLVDS1)

**Table B.67: LVDS Panel Voltage Selection (JLVDS1)**

Function	Jumper Setting
Jumper position for 5V	
Jumper position for 3.3V (Default)	
Jumper position for 12V	

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