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POWERLINK IP-Core
Xilinx FPGA Documentation

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I Versions

Version	Date	Comment	Edited by
0.1	Dec 14, 2011	First Edition	Zelenka Joerg
0.2	Jan 4, 2012	Added FPGA Resource Utilization	Zelenka Joerg
0.3	Feb 6, 2012	Revised FPGA Resource Utilization	Zelenka Joerg

Table 1: Versions

II Safety Notices

Safety notices in this document are organized as follows:

Safety notice	Description
Danger!	Disregarding the safety regulations and guidelines can be life-threatening.
Warning!	Disregarding the safety regulations and guidelines can result in severe injury or heavy damage to material.
Caution!	Disregarding the safety regulations and guidelines can result in injury or damage to material.
Information:	Important information used to prevent errors.
Example:	Functionality is described with an example to prevent errors.

Table 2: Safety notices

III Table of Contents

1 Introduction

The POWERLINK IP-Core is provided as ready-to-use in Xilinx Platform Studio (XPS) version 13.2. This documentation presents the integration of the IP-Core into the XPS, as well as timing considerations and interfacing to the software development environment.

If you require detailed information about the POWERLINK IP-Core itself, please refer to the "POWERLINK IP-Core Generic Documentation" (POWERLINK-IP-Core_Generic.pdf).

The POWERLINK IP-Core is implemented generically, which enables to use the same VHDL-sources in any FPGA environment. For instance memory components are given in extra VHDL-files ready to use in Cyclone III or IV devices. Experienced users can modify these files easily to port the IP-Core to other devices.
The IP-Core configuration is supported by an easy-to-use graphical user interface (GUI) in XPS. This enables the user to define several parameters for the POWERLINK node, like the type of API (e.g. SPI or parallel interface), the number of process data objects (PDO) or enabling low-jitter synchronization feature.

It has to be emphasized that no VHDL or FPGA knowledge is required to setup a POWERLINK node on an FPGA successfully. The entire necessary configuration is done depending on the settings defined in XPS.

2 Xilinx Platform Studio (XPS) Integration

3 Timing Consideration

4 Software Interface

5 FPGA Resource Utilization

The POWERLINK IP-core is used in combination with other components in an FPGA, hence the resource utilization and the circuit's performance (f_{max}) given in this section is an estimation only. The BRAM utilization is not given since it depends on several parameters given in the GUI. Note that the parameters not given in the table are set to default values (not changed in GUI).

Tab. 1: Resource utilization on Spartan 6 FPGA (XC6SL16CSG324-2C)

PARAMETERS								FITTER Results				
IP CORE MODE	PACKET BUFFER LOCATION [1]	USE RMII	USE 2ND PHY	NUMBER OF RPDO	LOW-JITTER SYNC	EVENT HW SUPPORT	PAP DATA WIDTH	FFs (POWERLINK [2])	LUTs (POWERLINK [2])	FFs (SYSTEM [3])	LUTs (SYSTEM [3])	fmax [MHz] [4]
Direct I/O	0	✓	✓	3	-	-	-	1102	1262	3860	4057	105
Parallel Interface	0	✓	✓	3	×	×	8	1372	1728	4400	4665	107
Parallel Interface	0	✓	✓	1	×	×	16	1348	1744	4376	4693	106
Parallel Interface	0	✓	✓	2	×	×	16	1360	1753	4388	4702	105
Parallel Interface	0	✓	✓	3	×	×	16	1382	1722	4410	4691	104
Parallel Interface	0	✓	✓	3	✓	×	16	1442	1817	4470	4773	105
Parallel Interface	0	✓	✓	3	✓	✓	16	1478	1864	4506	4860	106
SPI	0	✓	✓	3	×	×	-	1409	1782	4437	4739	106
PLB [5]	0	✓	✓	3	×	×	-	1475	1748	5520	6165	103
openMAC only	0	✓	✓	-	-	-	-	1058	1311	3815	4100	106
openMAC only	0	✓	×	-	-	-	-	995	1191	3752	3987	102
openMAC only	1	✓	✓	-	-	-	-	1374	1519	4193	4518	102

Table note:

1. The Packet Buffer Location determines the location of the openMAC's packet buffers (0 = "TX and RX into DPRAM" or 1 = "TX into DPRAM and RX over PLB).
2. The fitter results are given for the POWERLINK IP-Core only.
3. The fitter results are given for the whole system design including the recommended component setup in XPS (e.g. Microblaze, PLB and memory controller).
4. The f_{max} values give the circuit's performance of the 100 MHz clock in slow corner.
5. The "PLB" mode refers to a second Microblaze CPU within the FPGA, which executes the application. Note that the application-specific logic is considered in the system's area utilization, as well as in the circuit's performance (f_{max}).
6. Unused parameters are identified with a hyphen ("-").

6 Files

7 Definitions and Abbreviations

AP	Application Processor
BUF	MAC-internal packet buffer
CMD	Command
CMP	Compare Unit
CN	POWERLINK Controlled Node
DPR	Dual Ported RAM
DPRAM	Dual Ported RAM
FF	Flip Flop
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
GUI	Graphical User Interface
IP	Intellectual Property
IRQ	Interrupt Request
MII	Media Independent Interface
MN	POWERLINK Managing Node
PCB	Printed Circuit Board
PCP	Powerlink Communication Processor
PDI	Process Data Interface
PDO	Process Data Object
PReq	Poll Request (POWERLINK frame type)
PRes	Poll Response (POWERLINK frame type)
RD	Read
RDY	Ready
RMII	Reduced Media Independent Interface
RO	Read Only
SDO	Service Data Object
SMI	Serial Management Interface (Ethernet phy register access)
SMP	Simple I/O Port
SoA	Start of Asynchronous (POWERLINK frame type)
SoC	Start of Cyclic (POWERLINK frame type)
SPI	Serial Peripheral Interface
SYNC	Synchronization (Clock Domain Crossing)
WR	Write

8 References

[1] ???

9 Figure Index

Fehler! Es konnten keine Einträge für ein Abbildungsverzeichnis gefunden werden.

10 Table Index

11 Index