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POWERLINK IP-Core
Xilinx FPGA Documentation

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I Versions

Version	Date	Comment	Edited by
0.1	Dec 14, 2011	First Edition	Zelenka Joerg
0.2	Jan 4, 2012	Added FPGA Resource Utilization	Zelenka Joerg

Table 1: Versions

II Safety Notices

Safety notices in this document are organized as follows:

Safety notice	Description
Danger!	Disregarding the safety regulations and guidelines can be life-threatening.
Warning!	Disregarding the safety regulations and guidelines can result in severe injury or heavy damage to material.
Caution!	Disregarding the safety regulations and guidelines can result in injury or damage to material.
Information:	Important information used to prevent errors.
Example:	Functionality is described with an example to prevent errors.

Table 2: Safety notices

III Table of Contents

1 Introduction

2 Xilinx Platform Studio (XPS) Integration

3 Timing Consideration

4 Software Interface

5 FPGA Resource Utilization

The POWERLINK IP-core is used in combination with other components in an FPGA, hence the resource utilization and the circuit's performance (f_{max}) given in this section is an estimation only. The BRAM utilization is not given since it depends on several parameters given in the GUI. Note that the parameters not given in the table are set to default values (not changed in GUI).

Tab. 1: Resource utilization on Spartan 6 FPGA (XC6SLX45T-FGG484-2)

PARAMETERS									MAP Results			
C_IP_CORE_MODE [1]	C_PACKET_LOCATION [2]	C_USE_RMII	C_USE_2ND_PHY	C_PDI_NUM_RPDO	C_PDI_GEN_TIME_SYNC	C_PDI_GEN_SECOND_TIMER	C_PDI_GEN_EVENT	C_PAP_DATA_WIDTH	Slices	FFs	LUTs	f_{max} [MHz]
0	1	F	T	3	-	-	-	-	813	1539	1645	116
1	1	F	T	3	F	F	F	8	1027	1654	1960	121
1	1	F	T	3	F	F	F	16	1049	1671	1987	118
3	1	F	T	3	F	F	F	-	986	1687	1973	120
4	1	F	T	1	F	F	F	-	1017	1721	1964	118
4	1	F	T	2	F	F	F	-	1049	1743	1976	102
4	1	F	T	3	F	F	F	-	1032	1747	1975	123
4	1	F	T	3	F	T	F	-	1037	1780	1969	124
4	1	F	T	3	T	T	F	-	1040	1803	2007	121
4	1	F	T	3	T	T	T	-	1081	1842	2053	119
5	0	F	T	-	-	-	-	-	547	1056	1131	123
5	1	F	T	-	-	-	-	-	704	1381	1527	119

Table note:

1. The IP-Core Mode determines the available features (0 = "Direct I/O", 1 = "Parallel Interface", 3 = "SPI", 4 = "PLB" or 5 = "openMAC only").
2. The Packet Location determines the location of the openMAC's packet buffers (0 = "TX and RX into DPRAM", 1 = "TX into DPRAM and RX over PLB" or 2 = "TX and RX over PLB")
3. Boolean parameters are set to TRUE ("T") or FALSE ("F").
4. Unused parameters are identified with a hyphen ("-")

6 Files

7 Definitions and Abbreviations

AP	Application Processor
BUF	MAC-internal packet buffer
CMD	Command
CMP	Compare Unit
CN	POWERLINK Controlled Node
DPR	Dual Ported RAM
DPRAM	Dual Ported RAM
FF	Flip Flop
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
GUI	Graphical User Interface
IP	Intellectual Property
IRQ	Interrupt Request
MII	Media Independent Interface
MN	POWERLINK Managing Node
PCB	Printed Circuit Board
PCP	Powerlink Communication Processor
PDI	Process Data Interface
PDO	Process Data Object
PReq	Poll Request (POWERLINK frame type)
PRes	Poll Response (POWERLINK frame type)
RD	Read
RDY	Ready
RMII	Reduced Media Independent Interface
RO	Read Only
SDO	Service Data Object
SMI	Serial Management Interface (Ethernet phy register access)
SMP	Simple I/O Port
SoA	Start of Asynchronous (POWERLINK frame type)
SoC	Start of Cyclic (POWERLINK frame type)
SPI	Serial Peripheral Interface
SYNC	Synchronization (Clock Domain Crossing)
WR	Write

8 References

[1] ???

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