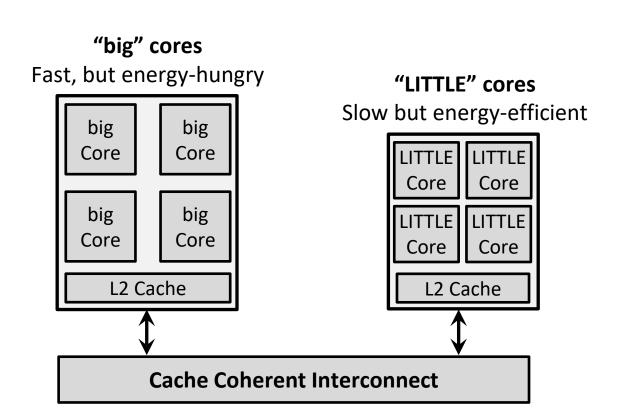
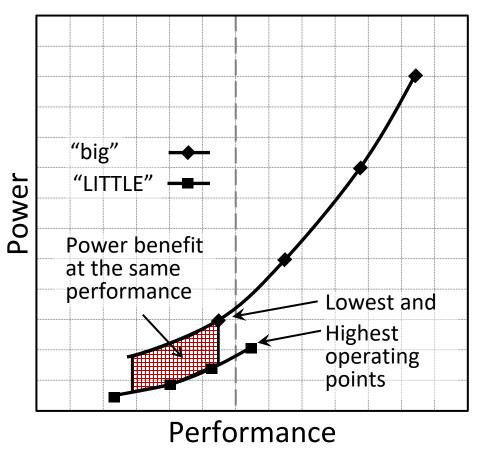


Time vs Energy Trade-off: ARM big.LITTLE Case



Trade-off

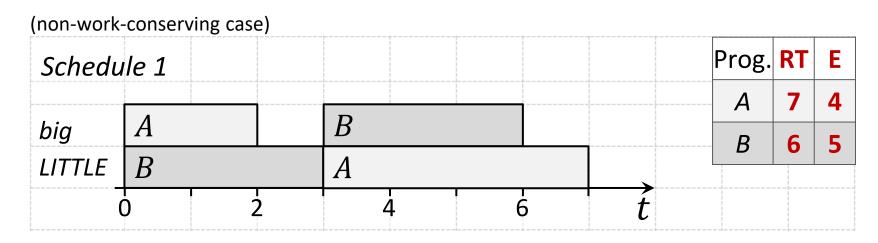


Drog	"big" Core		"LITTLE" Core	
Prog.	Time	Energy	Time	Energy
Α	5	2	8	1
В	4	4	10	3

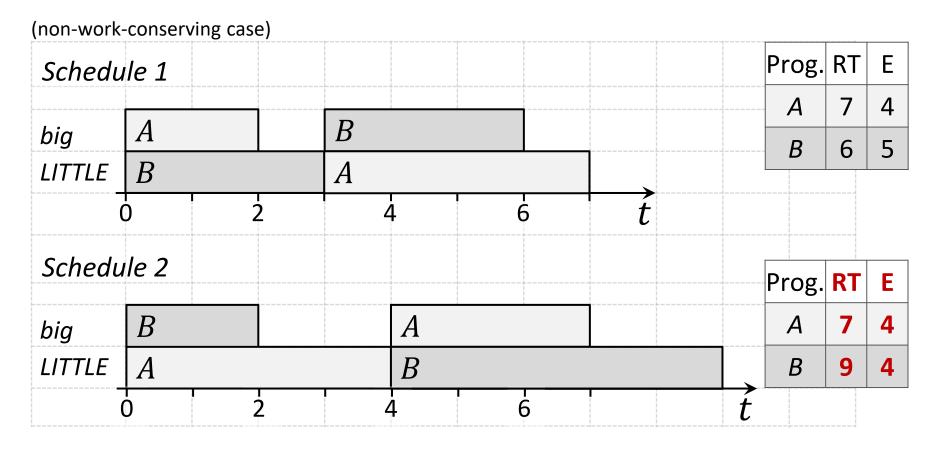
Drog	"big" Core		"LITTLE" Core	
Prog.	Time	Energy	Time	Energy
Α	5	2	8	1
В	4	4	10	3

Prog.	"big" Core		"LITTLE" Core	
	Time	Energy	Time	Energy
Α	5	2	8	1
В	4	4	10	3

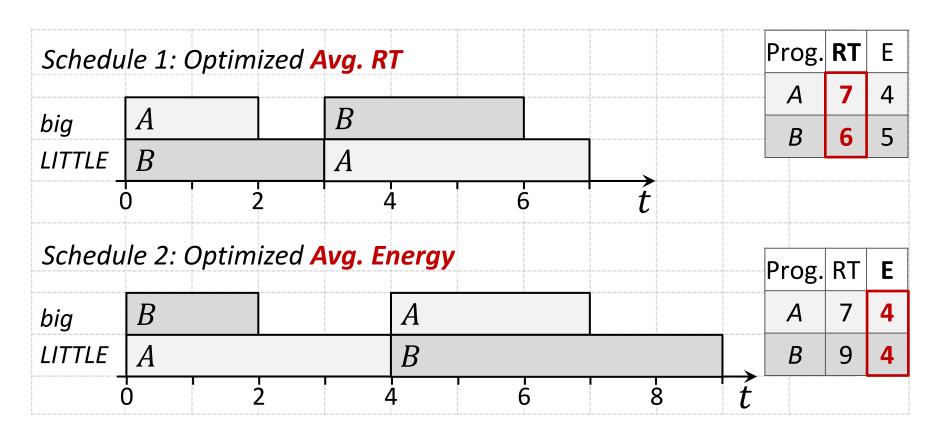
Drog	"big" Core		"LITTLE" Core	
Prog.	Time	Energy	Time	Energy
Α	5	2	8	1
В	4	4	10	3



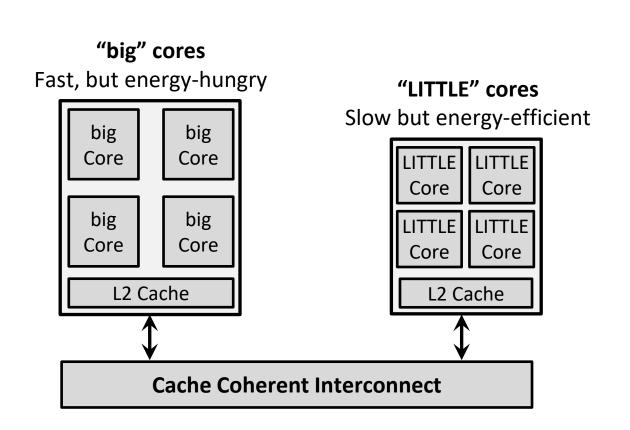
Drog	"big" Core		"LITTLE" Core	
Prog.	Time	Energy	Time	Energy
Α	5	2	8	1
В	4	4	10	3

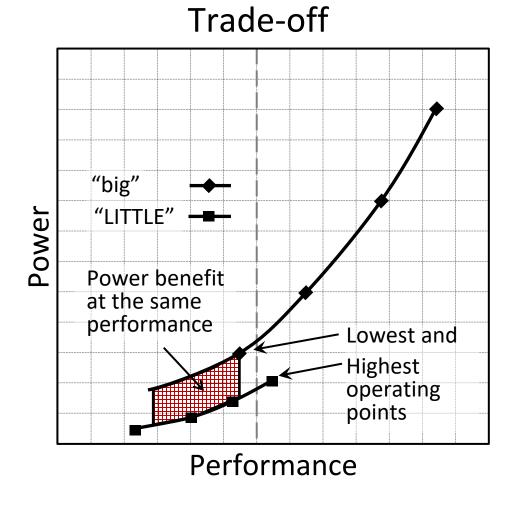


Drog	"big" Core		"LITTLE" Core	
Prog.	Time	Energy	Time	Energy
Α	5	2	8	1
В	4	4	10	3



Time vs Energy Trade-off: ARM big.LITTLE Case





- Scheduler affects time and energy consumption;
- Efficient scheduler is demanded (e.g. for mobile devices)

Existing Heterogeneous Schedulers

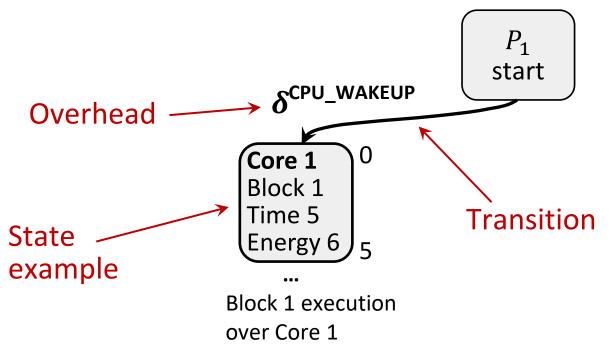
HEFT: Heterogeneous Earliest Finish Time;

HASS: Heterogeneity-Aware Signature-Supported

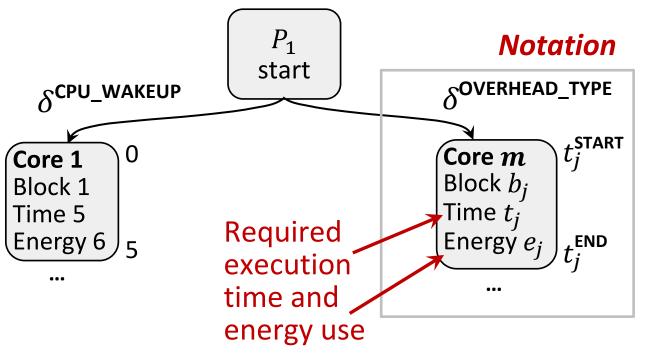
Properties c	Properties of HEFT and HASS Schedulers			
Objective	Response times minimization			
Principle	Greedy-based heuristics			
Limitations	Suboptimal; Energy consumption not considered			

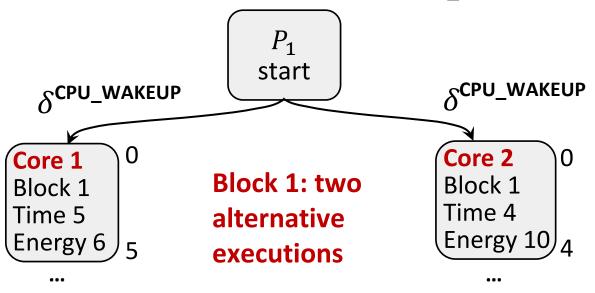
 P_1 start

Blocks	Param	Core 1	Core 2
Block 1	Time	5	4
DIOCK 1	Energy	6	10
DI - I 2	Time	3	2
Block 2	Energy	3	7
Dlook 2	Time	2	2
Block 3	Energy	3	6

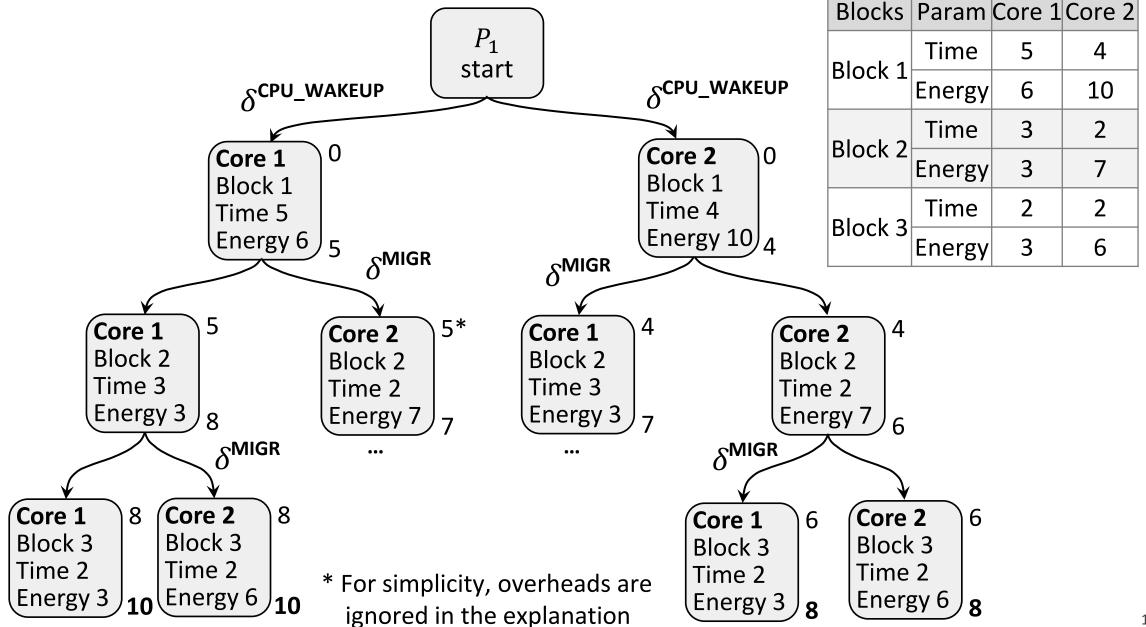


Blocks	Param	Core 1	Core 2
Block 1	Time	5	4
DIOCK T	Energy	6	10
Block 2	Time	3	2
	Energy	3	7
Block 3	Time	2	2
DIOCK 5	Energy	3	6





Blocks	Param	Core 1	Core 2
Diagk 1	Time	5	4
Block 1	Energy	6	10
Block 2	Time	3	2
	Energy	3	7
Dlock 2	Time	2	2
Block 3	Energy	3	6



P_1 requirements State-Transition Graph for a Solo Program P_1 Blocks | Param | Core 1 | Core 2 | P_1 Time 5 4 start Block 1 SCPU_WAKEUP **∠CPU_WAKEUP** Energy 6 10 3 2 Time Block 2 Core 2 Core 1 3 Energy Block 1 Block 1 2 Time Time(4) Time 5 Block 3 Energy 10/₄ Energy 6 3 6 Energy δ^{MIGR} δ^{MIGR} 5 4 Core 1 Core 1 Core 2 Core 2 Block 2 Block 2 Block 2 Block 2 Time 3 Time 2 Time 3 Time(2) Energy 3 Energy 3 Energy 7 Energy 7 δ^{MIGR} $\mathcal{L}^{\mathsf{MIGR}}$ ••• Core 2 Core 1 8 8 Core 2 Core 1 6 6 Block 3 Block 3 Block 3 Block 3 Time 2 Time 2 **Minimized RT: 8** Time 2 Time(2) Energy 6 Energy 6

High energy use: 20

Energy 3

Energy 3

P_1 requirements State-Transition Graph for a Solo Program P_1 Blocks Param Core 1 Core 2 P_1 Time 5 4 start Block 1 SCPU_WAKEUP **∠CPU_WAKEUP** Energy 6 10 3 2 Time Block 2 Core 2 Core 1 Energy 3 Block 1 Block 1 2 Time Time(5) Time(4) Block 3 Energy 6 Energy 10/4 6 Energy δ^{MIGR} δ^{MIGR} 5 4 Core 1 Core 1 Core 2 Core 2 Block 2 Block 2 Block 2 Block 2 Time(3) Time 3 Time 2 Time 2 Energy 3 8 Energy 7 Energy 3 Energy 7 δ^{MIGR} **∠**MIGR ••• Core 2 8 Core 1 8 Core 2 6 Core 1 6 Block 3 Block 3 Block 3 Block 3 Time(2) Time 2 High RT: 10 Time 2 **RT: 8** Time(2)

Min. Energy: 12

Energy 6

Energy 3

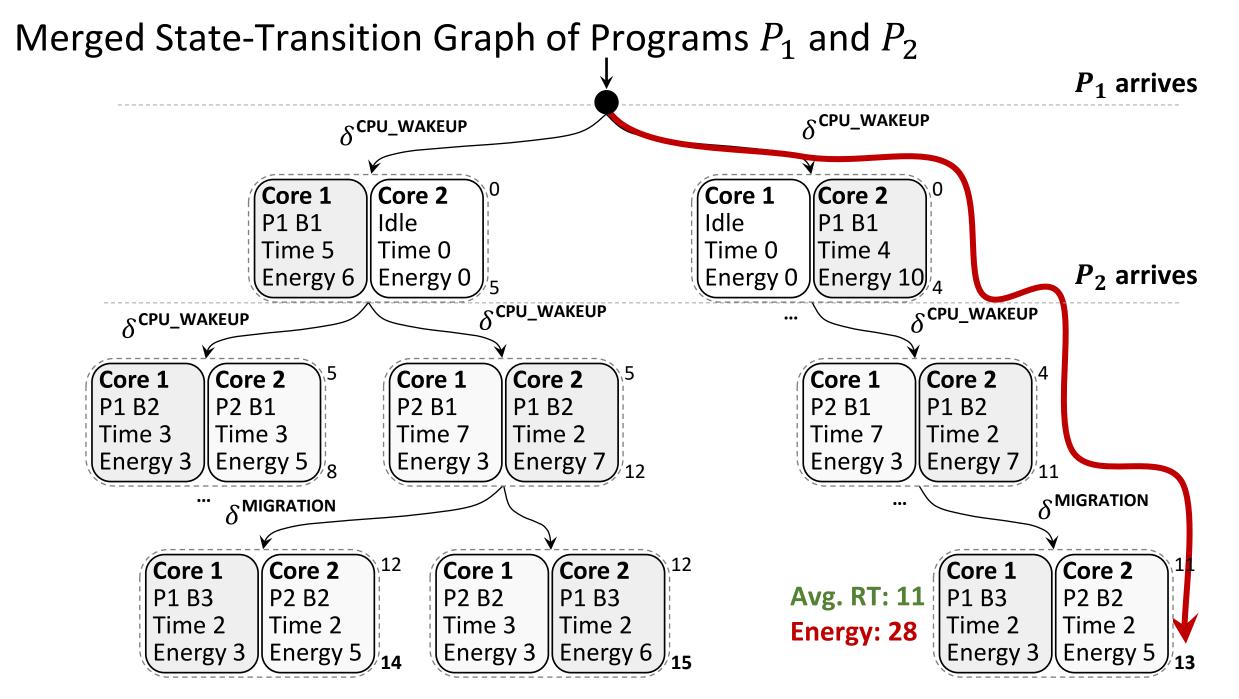
Energy 6

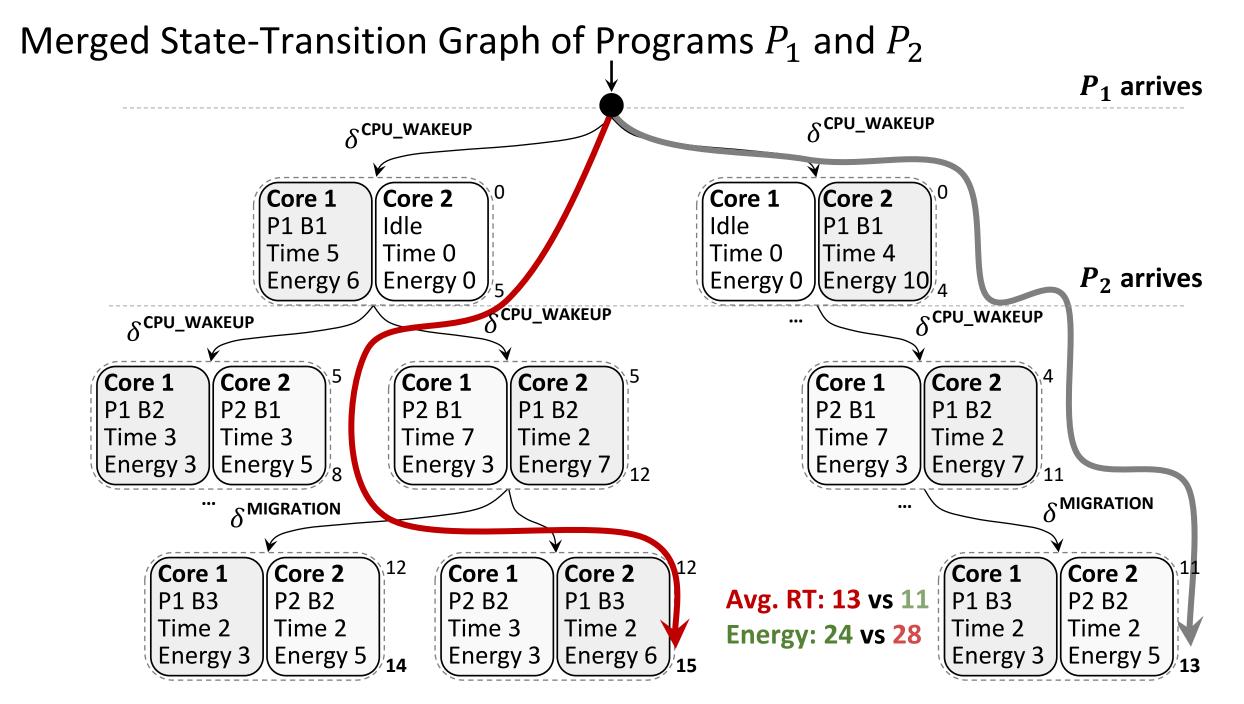
Energy 3

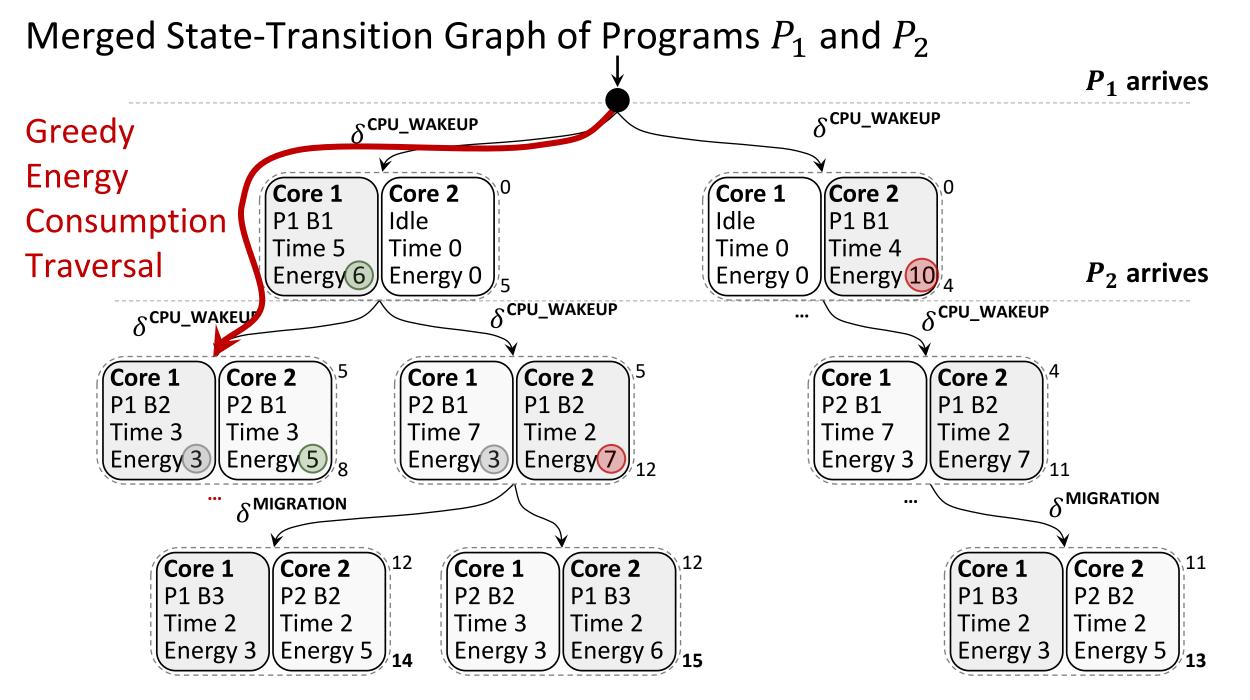
Energy: 20

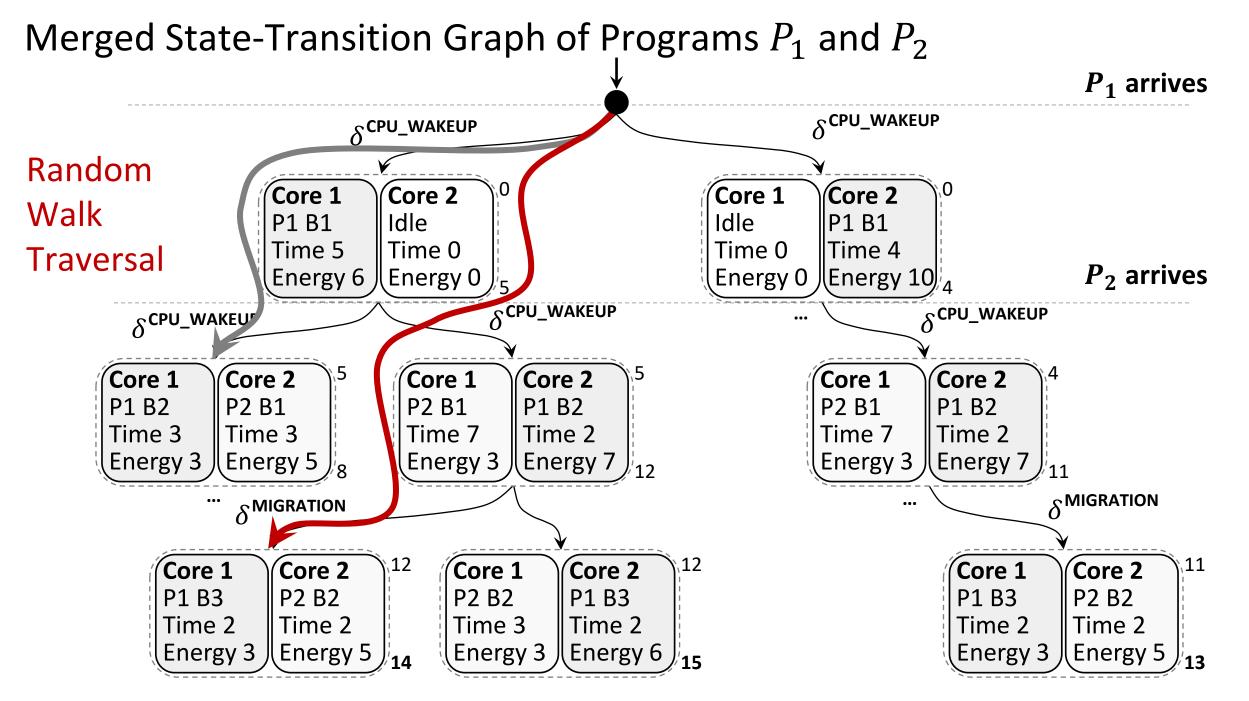
Merged State-Transition Graph of Programs P_1 and P_2 P_2 requirements P_1 arrives δ^{CPU} WAKEUP δ^{CPU} WAKEUP Bi t/e Core 1 Core 2 t B1 Core 1 3 Core 2 Core 1 Core 2 Idle Idle P1 B1 P1 B1 B2 Time 5 Time 4 P_2 arrives Energy 6 (Energy 10) δ CPU_WAKEUP $\mathcal{S}^{\mathsf{CPU}}$ WAKEUP δ CPU_WAKEUP Core 1 Core 1 Core 2 Core 2 Core 1 Core 2 Idle P1 B2 Idle Idle P1 B2 P1 B2 Time 3 Time 2 Time 2 Energy 3 Energy 7 Energy 7 δ MIGRATION δ MIGRATION Core 2 Core 1 Core 2 Core 1 Core 2 Core 1 P1 B3 Idle Idle P1 B3 Idle P1 B3 Time 2 Time 2 Time 2 Energy 3 Energy 6 Energy 3

Merged State-Transition Graph of Programs P_1 and P_2 P_2 requirements P_1 arrives &CPU_WAKEUP δ CPU_WAKEUP Bi t/e Core 1 Core 2 t B1 3 5 Core 2 Core 1 Core 2 Core 1 Idle P1 B1 P1 B1 Idle B2 Time 5 Time 4 5 P_2 arrives Energy 6 (Energy 10) δ CPU_WAKEUP SCPU_WAKEUP δ^{CPU} WAKEUP Core 1 Core 2 Core 2 Core 1 Core 1 Core 2 P2 B1 P1 B2 P2 B1 P1 B2 P2 B1 P1 B2 Time 3 Time 3 Time 7 Time 2 Time 7 Time 2 Energy 3 Energy 5 Energy 7 Energy 7 Energy 3 Energy 3 δ MIGRATION **CMIGRATION** 12 Core 2 Core 2 Core 2 Core 1 Core 1 Core 1 P1 B3 P2 B2 P1 B3 P2 B2 P2 B2 P1 B3 Time 2 Time 2 Time 3 Time 2 Time 2 Time 2 Energy 6 Energy 3 Energy 5 Energy 3 Energy 3 Energy 5









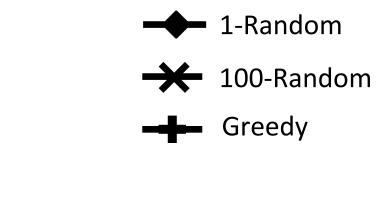
Schedulers Evaluation

Settings: Blocks Requirements per Core 1,2:

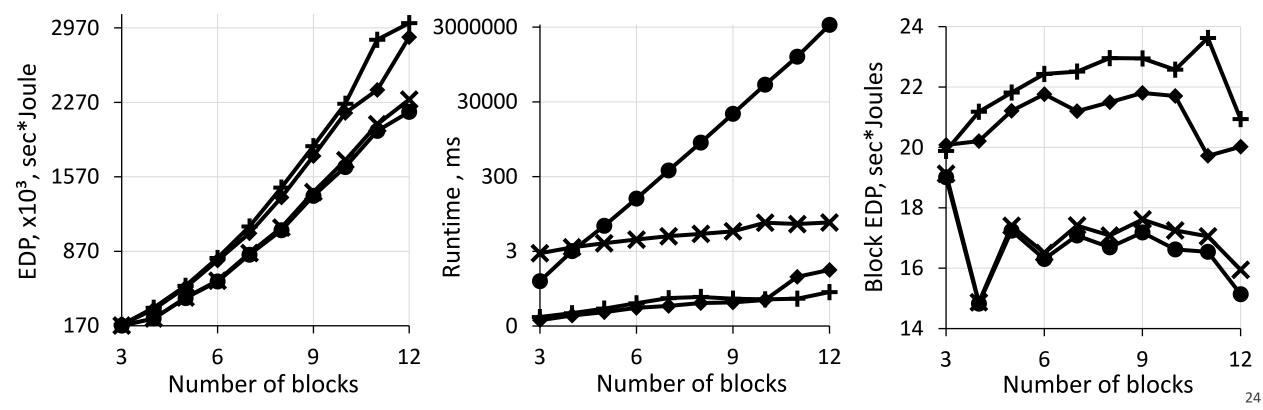
Programs number – 3; Runtime – 1: [220; 250], 2: [210; 230];

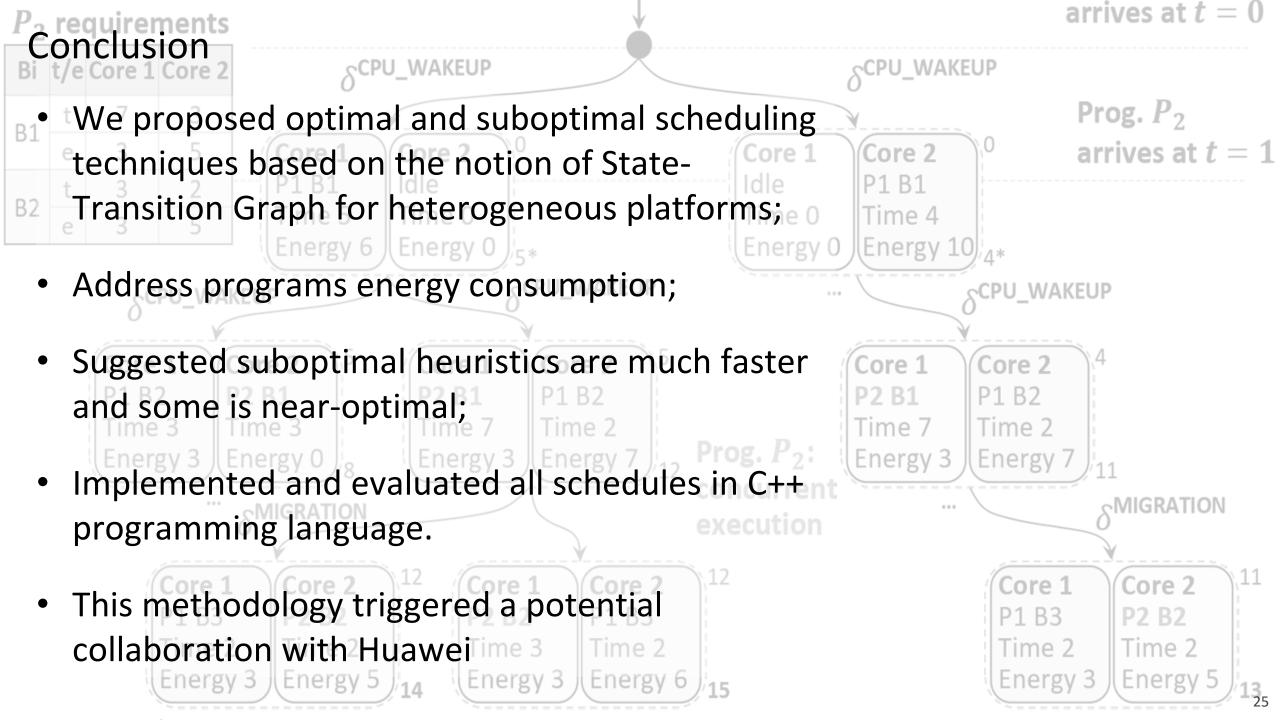
Cores number – 2; Energy use – 1: [120; 130], 2: [125; 150].

Input generation: numbers of programs and cores are fixed, blocks requirements are picked from uniform distributions



Optimal





References

- 1. E. L. Padoin, L. L. Pilla, M. Castro, F. Z. Boito, P. O. Alexandre Navaux, and J.-F. M'ehaut, "Performance/energy trade-off in scientific computing: the case of arm big.little and intel sandy bridge," IET Computers & Digital Techniques, vol. 9, no. 1, pp. 27–35, 2015. [Online]. Available: https://ietresearch.onlinelibrary.wiley.com/doi/abs/10.1049/ietcdt. 2014.0074
- 2. H. Topcuoglu, S. Hariri, and M.-Y. Wu, "Task scheduling algorithms for heterogeneous processors," in Proceedings. Eighth Heterogeneous Computing Workshop (HCW'99), 1999, pp. 3–14;
- 3. D. Shelepov, J. C. Saez Alcaide, S. Jeffery, A. Fedorova, N. Perez, Z. F. Huang, S. Blagodurov, and V. Kumar, "Hass: a scheduler for heterogeneous multicore systems," SIGOPS Oper. Syst. Rev., vol. 43, no. 2, p. 66–75, Apr. 2009. [Online]. Available: https://doi.org/10.1145/1531793.1531804