Registermap

Overview

Name	Address	Description
LEDG	0x4000	Green LED Register
LEDR	0x4002	Red LED Register
HEX0	0x4010	Seven Segment Digit 0 Register
HEX1	0x4012	Seven Segment Digit 1 Register
HEX2	0x4014	Seven Segment Digit 2 Register
HEX3	0x4016	Seven Segment Digit 3 Register
KEY	0x4020	Pushbuttons Register
SW	0x4022	Switch Register
ENDPI0_CONTROL	0x5000	Endpoint In 0 Control Register
ENDPI0_DATA	0x5002	Endpoint In 0 Data Register
ENDPI1_CONTROL	0x5004	Endpoint In 1 Control Register
ENDPI1_DATA	0x5006	Endpoint In 1 Data Register
ENDPO0_CONTROL	0x5040	Endpoint Out 0 Control Register
ENDPO0_DATA	0x5042	Endpoint Out 0 Data Register
USB_CONTROL	0x5100	USB Control Register

Detailed Description

LEDG

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	LEDG							
Mode	r0	r0	r0	r0	r0	r0	r0	r0	w							
Reset	-	-	-	-	-	-	-	-	0x00							

Green LED Register
Address: 0x4000

LEDR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	LEDR									
Mode	r0	r0	r0	r0	r0	r0	w									
Reset	-	-	-	-	-	-	0x000									

Red LED Register
Address: 0x4002

The registers LEDG and LEDR control the eight green and the ten red LEDs of the evaluation board respectively.

A set bit means the LED is on, a reset bit means the LED is off.

HEX0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	HEX0						
Mode	r0	r0	r0	r0	r0	r0	r0	r0	r0	w						
Reset	-	-	-	-	-	-	-	-	-	0x00						

Seven Segment Digit 0 Register
Address: 0x4010

HEX1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	HEX1						
Mode	r0	r0	r0	r0	r0	r0	r0	r0	r0	w						
Reset	-	-	-	-	-	-	-	-	-	0x00						

Seven Segment Digit 1 Register
Address: 0x4012

HEX2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	HEX2						
Mode	r0	r0	r0	r0	r0	r0	r0	r0	r0	w						
Reset	-	-	-	-	-	-	-	-	-	0x00						

Seven Segment Digit 2 Register
Address: 0x4014

HEX3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	HEX3						
Mode	r0	r0	r0	r0	r0	r0	r0	r0	r0	w						
Reset	-	-	-	-	-	-	-	-	-	0x00						

Seven Segment Digit 3 Register
Address: 0x4016

The registers HEX0—HEX3 control the segments of the four-digit hexadecimal display of the evaluation board.

A set bit means the segment is on, a reset bit means the segment is off.

KEY

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	-	-	-	KEY			
Mode	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r			
Reset	-	-	-	-	-	-	-	-	-	-	-	-	-			

Pushbuttons Register
Address: 0x4020

The KEY register contains the state of the four pushbuttons of the evaluation board.

A set bit means the button is not pressed, a reset bit means the button is pressed.

SW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	SW									
Mode	r0	r0	r0	r0	r0	r0	r									
Reset	-	-	-	-	-	-	-									

Toggle Switch Register
Address: 0x4022

The SW register contains the state of the ten switches of the evaluation board.

A set bit means the switch is on, a reset bit means the switch is off.

ENDPI0_CONTROL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	-	-	-	-	ZLP	STALL	FULL
Mode	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	w	w	r
Reset	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0

Endpoint In 0 Control Register
Address: 0x5000

Name	Function
ZLP	Zero Length Packet 0: IN response contains data, the data and the CRC will be sent 1: IN response contains no data, only the CRC will be sent
STALL	Stall bit 0: no stall 1: stalled
FULL	FIFO full bit 0: FIFO is not full 1: FIFO is full

The ZLP and the STALL bit will be automatically cleared after the IN transaction.

ENDPI0_DATA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	DATA							
Mode	r0	r0	r0	r0	r0	r0	r0	r0	w							
Reset	-	-	-	-	-	-	-	-	-							

Endpoint In 0 Data Register
Address: 0x5002

A write access to DATA will put a data into the FIFO of the IN endpoint.

ENDPI1_CONTROL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	-	-	-	-	ZLP	STALL	FULL
Mode	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	w	w	r
Reset	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0

Endpoint In 1 Control Register
0x5004

ENDPI1_DATA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	DATA							
Mode	r0	r0	r0	r0	r0	r0	r0	r0	w							
Reset	-	-	-	-	-	-	-	-	-							

Endpoint In 1 Data Register
0x5006

See ENDPI0_CONTROL and ENDPI0_DATA.

ENDPO0_CONTROL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	-	-	-	-	-	RDREQ	EMPTY
Mode	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	w	r
Reset	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0

Endpoint Out 0 Control Register
Address: 0x5040

Name	Function
RDREQ	FIFO read request 0: no action 1: fetch one item from FIFO
EMPTY	FIFO empty bit 0: FIFO contains data 1: FIFO is empty

ENDPO0_DATA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	DATA							
Mode	r0	r0	r0	r0	r0	r0	r0	r0	r							
Reset	-	-	-	-	-	-	-	-	-							

Endpoint Out 0 Data Register
Address: 0x5042

In order to read data from the FIFO of the OUT endpoint the bit ENDPO0_CONTROL.RDREQ must be set first. The following read access of DATA will fetch the FIFO item.

USB_CONTROL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	PID				DEVICE_ADDRESS						
Mode	r0	r0	r0	r0	r0	r				rw						
Reset	-	-	-	-	-	-				0x00						

USB Control Register
Address: 0x5100