

ORIGINAL ARTICLE

A high-precision voltage reference with a curvature-compensated bandgap for fluorescence detection

Bingjun Xiong | Wenji Mo | Feng Yan | Jian Guan | Weijie Ge |
Jingjing Liu 

School of Electronics and Communication Engineering, Sun Yat-Sen University, Shenzhen, China

Correspondence

Jingjing Liu, School of Electronics and Communication Engineering, Sun Yat-Sen University, Shenzhen, China.
Email: liujj77@mail.sysu.edu.cn

Funding information

This work is supported by the National Natural Science Foundation of China with Project Number 62174181.

Summary

Fluorescent optical fiber temperature sensors require accurate online temperature monitoring in hazardous environments with strong electromagnetic fields, high voltages, flammability, or explosiveness. This imposes stringent requirements on the temperature coefficient stability of the bandgap reference (BGR) circuit. To address these challenges, this paper proposes a high-order curvature compensation bandgap reference (HCC_BGR) circuit fabricated using a 0.18- μm bipolar-CMOS-DMOS (BCD) process. A traditional first-order bandgap reference (TRA_BGR) circuit is also fabricated for comparison. Experimental results demonstrate that the proposed HCC_BGR circuit generates a stable 1.22-V reference voltage with a low-temperature coefficient of 5.56 ppm/ $^{\circ}\text{C}$ from -20°C to 85°C . Compared to the TRA_BGR circuit, the HCC_BGR reduces the temperature coefficient by 3.07 times. Furthermore, the low-dropout regulator (LDO) using the proposed HCC_BGR exhibits excellent line sensitivity of 1.52%/V from 3.4 to 5 V.

KEYWORDS

bandgap reference source, high-order curvature compensation, low-dropout regulators, temperature coefficient

1 | INTRODUCTION

The fluorescent optical fiber temperature sensor systems need a low-temperature coefficient and a high-precision voltage reference (VR) circuit. A stable and accurate power supply circuit is crucial to ensuring optimal performance of a fluorescent fiber optic temperature sensor system, as it directly influences the fluorescence detection signal quality and analog-to-digital converter sampling accuracy. Bandgap reference (BGR) voltage sources, renowned for their exceptional robustness, are widely employed in integrated circuit systems such as power management circuits, analog-to-digital and digital-to-analog converters, temperature sensors, clocks, and timing circuits. For fluorescent optical fiber temperature sensors, specifically, it is critical to have a stable reference voltage to ensure a reliable static operating point. In 1971, Widlar proposed a temperature-independent BGR source structure, which was the first time in history to propose the concept of a BGR source.¹ In 2015, Wang et al. realized a voltage-mode reference circuit based on the narrowing effect of the silicon bandgap. The reference has a temperature coefficient of 8.7 ppm/ $^{\circ}\text{C}$ in the temperature range of -55°C to 125°C .² In 2019, Lee et al. proposed a second-order curvature compensation reference source circuit based on a 0.18- μm CMOS process that realized second-order curvature compensation by combining a convex temperature curve and a concave temperature curve. The measurement results show that the best temperature coefficient of this

BGR is 15.33 ppm/°C in the range of −10°C to 120°C.³ In 2021, Chen et al. designed a BGR source circuit with multi-section curvature correction based on a 130-nm complementary metal oxide semiconductor (CMOS) process technology.⁴ This method injects multiple compensation currents at the output of the BGR circuit, and each compensation current could trigger different temperature thresholds to compensate for the nonlinear temperature dependence of the bipolar transistor (BJT) base–emitter voltage. Therefore, a temperature coefficient as low as 8.75 ppm/°C is achieved. In 2022, Palani et al. proposed a new sub-1-V CMOS BGR using discrete-time sampling to eliminate the operational amplifier (OA).⁵ It samples proportional-to-absolute-temperature (PTAT) and complementary-to-absolute-temperature (CTAT) voltages onto a capacitor to generate a 108-mV reference with an 8.5 ppm/°C temperature coefficient from −40°C to 125°C.

Despite using various curvature compensation techniques, conventional BGR circuits still suffer from high-temperature coefficients.^{6–19} Excessive temperature drift of the BGR affects both the power supply voltage accuracy and the DC operating point stability of the fluorescent optical fiber temperature sensor. Consequently, this compromises the accurate detection of the fluorescent signal. Regarding the issue, this work proposes a high-precision BGR integrating high-order curvature compensation to achieve an ultralow-temperature coefficient. A comparative study was conducted between the proposed high-order curvature compensation bandgap reference (HCC_BGR) circuit and traditional BGR circuits in the same low-dropout regulator (LDO) structure, and the results demonstrate that the proposed circuit achieves superior precision. The rest of this paper is structured as follows: Section 2 describes the circuit implementation and simulation results; Section 3 presents the measurement results of the proposed BGR and LDO; and Section 4 summarizes the conclusions.

2 | CIRCUIT IMPLEMENTATION AND SIMULATIONS

The fluorescent optical fiber temperature sensor system and a typical LDO circuit diagram are shown in Figure 1. The fluorescent optical fiber temperature sensor requires a variety of stable voltage sources to supply power for different loads, such as a microcontroller unit (MCU) control system, a light source drive circuit, a photoelectric conversion circuit, and an amplifier circuit. A stable power supply voltage is the premise of the stable operation of the whole system, and the accuracy of the reference source determines the robustness of the power supply voltage.^{20–27} When the loop gain β of the LDO is large enough, the relationship between the LDO output voltage V_{OUT} and the reference voltage can be obtained, as shown in (1). Any error in the obtained reference voltage would be amplified by $1/\beta$ times by the LDO, thereby affecting the robustness of the power supply voltage. The fluctuations in the power supply voltage would have a large impact on the signal readout of the fluorescent fiber optic temperature sensor.

$$V_{OUT} \approx V_{REF} \cdot \frac{R_{f1} + R_{f2}}{R_{f2}} = \frac{V_{REF}}{\beta} \quad (1)$$

The basic design idea of the BGR source circuit is that two parameters having opposite temperature coefficients are added with proper weighting. This results in a zero temperature coefficient (TC). The schematic circuit of the traditional BGR source is shown in Figure 2. The VR core circuit utilizes the current mode structure proposed by Banba et al.¹⁹ The reference uses an OA to clamp both ends of the resistors R_1 and R_2 , so that the currents flowing through the resistors R_1 and R_2 are almost equal. Consequently, resistor R_3 generates an I_{PTAT} current directly proportional to the absolute temperature, while resistor R_2 produces an I_{CTAT} current complementary to the absolute temperature. The I_{PTAT} and I_{CTAT} currents flow through resistor R_4 via a current mirror structure composed of transistors M_{11} and M_{12} . Appropriately adjusting the resistance ratio of R_1 to R_4 allows for the achievement of a V_{REF} output voltage with a zero-temperature coefficient. The output reference voltage can be represented by (2).

$$V_{REF} = \frac{R_4}{R_2} \cdot V_{BE,Q1} + \frac{R_4}{R_3} \cdot V_T \ln(n) \quad (2)$$

The DC simulation results of the traditional BGR source are shown in Figure 3A. The simulation results show that the output voltage of the BGR is 1.24 V, and its temperature coefficient is 13.66 ppm/°C in the temperature range of −20°C to 85°C. Although this structure can produce an output voltage that is independent of process, temperature, and

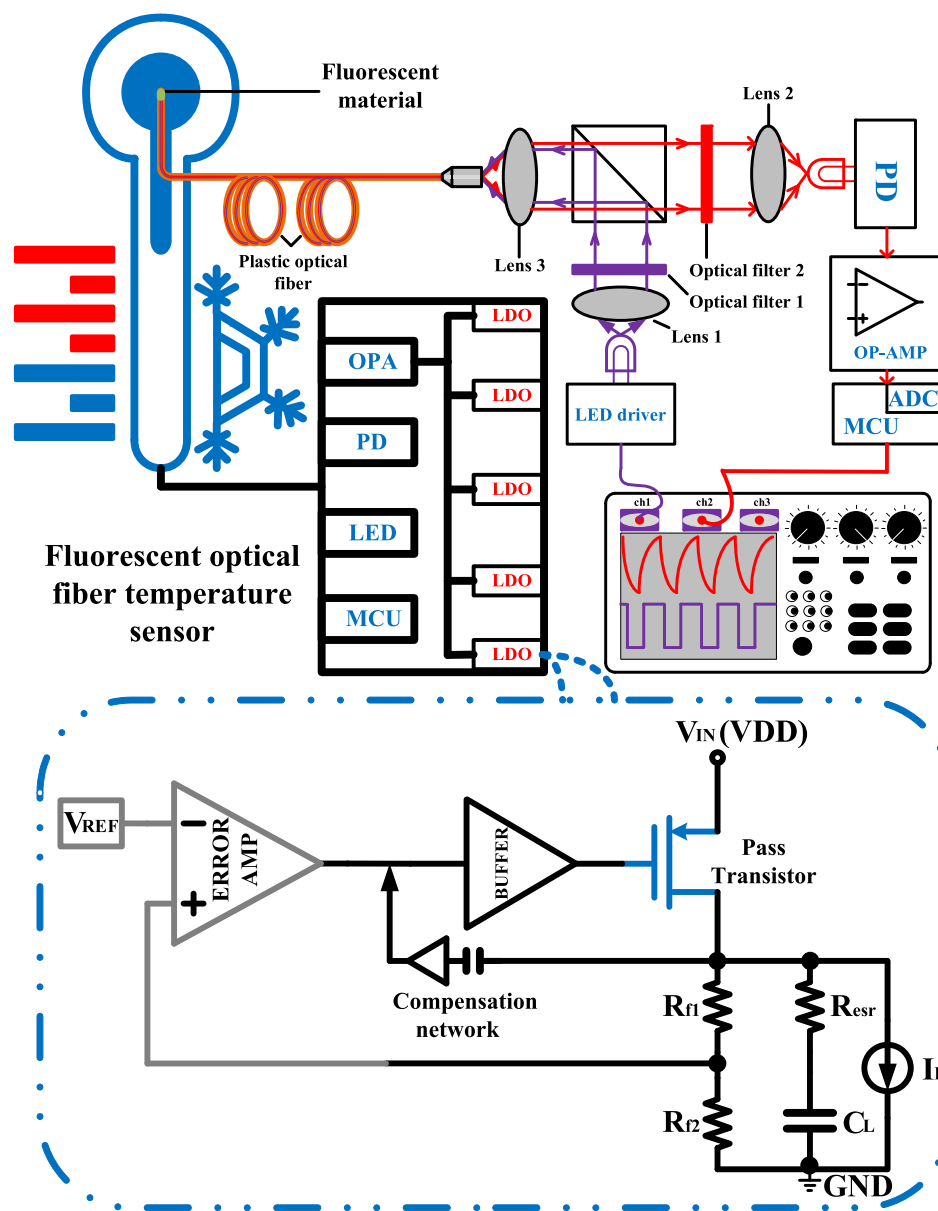


FIGURE 1 The structure diagram of a fluorescent optical fiber temperature sensor and typical LDO.

supply voltage, its temperature coefficient is still relatively high. It can be seen from (1) that when this reference is applied to the LDO, it will affect the accuracy of the output voltage.

The relationship between base-emitter voltage V_{BE} and temperature T can be obtained from the literature.¹⁵ In addition to the constant term and first-order coefficient term, there are also higher order nonlinear terms in the $V_{BE}(T)$ expression. The circuit structure of the traditional BGR source only cancels out the first-order coefficient term, so the existence of the high-order nonlinear term $T \cdot \ln(T)$ would have an impact on the temperature characteristics of the reference source, which is one of the main reasons why the traditional reference source structures are difficult to obtain lower temperature coefficients. In this paper, a compensation circuit structure with a $T \cdot \ln(T)$ correction term is designed to directly cancel the influence of high-order nonlinear terms in the reference output voltage, thereby effectively compensating the temperature coefficient to improve the temperature characteristic of the reference source. The proposed HCC_BGR circuit is designed and manufactured with the 0.18- μm bipolar-CMOS-DMOS (BCD) process. Figure 4 shows the detailed transistor-level circuit diagram. The diagram indicates that the circuit consists of a startup circuit, an OA, a VR core circuit, and a high-order curvature compensation circuit. The high-order curvature

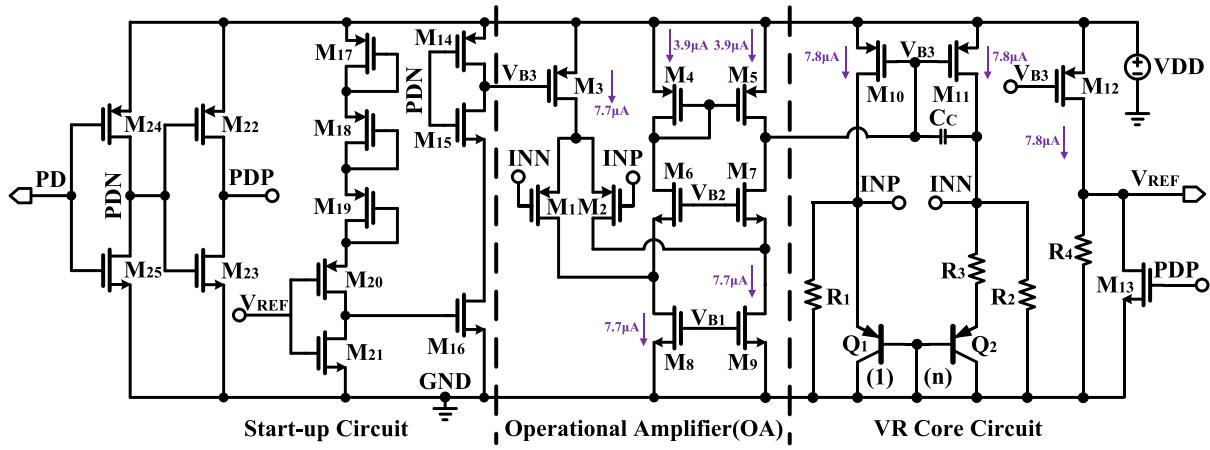


FIGURE 2 The circuit diagram of the traditional reference source circuit.

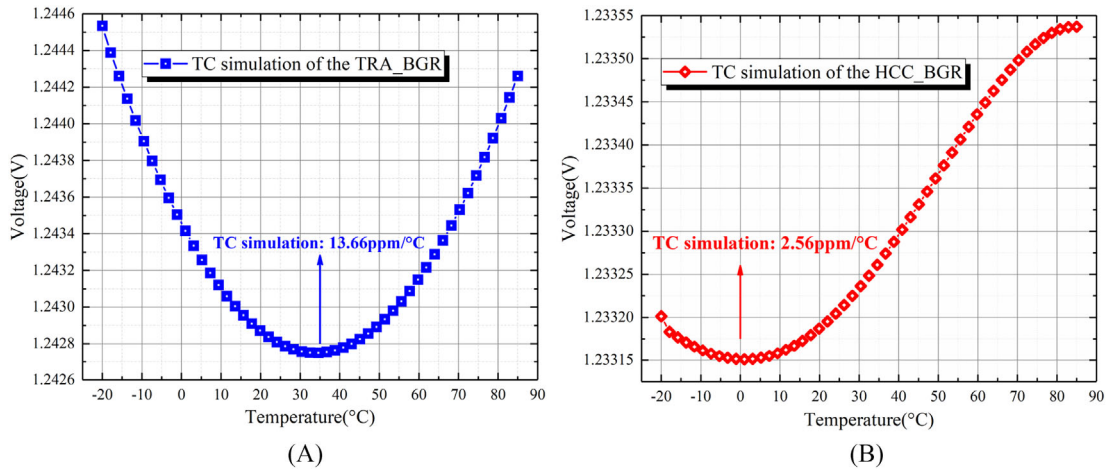


FIGURE 3 (A) Simulated results of TC for TRA_BGR. (B) Simulated results of TC for HCC_BGR.

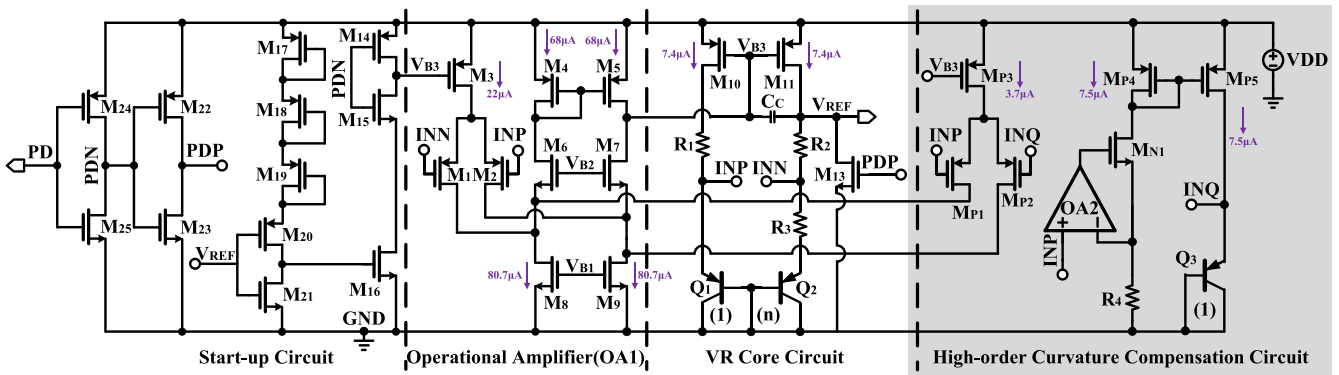


FIGURE 4 The circuit diagram of the high-order curvature compensation BGR.

compensation circuit is formed by transistors M_{P1} to M_{P5} , M_{N1} , bipolar transistor Q_3 , resistor R_4 , and OA2. The operational amplifier OA2 working in the deep negative feedback state makes the emitter of Q_1 and the resistor R_4 have the same voltage. Then a nonlinear term with $T \cdot \ln(T)$ is generated between the V_{BE} voltage differences of Q_3 and Q_1 , and

this voltage is set as $\beta \cdot T \cdot \ln(T)$. In addition, the V_{BE} voltage difference between Q_3 and Q_1 also contains a term proportional to temperature, which is set as $\gamma \cdot T$. The $\Delta V_{BE1.2}$ voltage of the bipolar transistors Q_1 and Q_2 is used as the input of the differential pair G_{m1} to form the traditional BGR source structure. The $\Delta V_{BE1.3}$ voltage of the bipolar transistors Q_1 and Q_3 is used as the input of the differential pair G_{m2} . Consequently, the compensation voltage V_{out} is introduced at the OA1's output. The V_{out} can be expressed as

$$V_{out} = G_{m2} \cdot \Delta V_{BE1.3} \cdot R_{out} = G_{m2} \cdot [\beta \cdot T \cdot \ln(T) + \gamma \cdot T] \cdot R_{out} \quad (3)$$

where G_{m2} denotes the transconductance of the differential pair, comprising transistors M_{P1} and M_{P2} , and R_{out} signifies the output impedance of the OA2. Consequently, the compensation voltage V_{out} diminishes the differential voltage signal caused by the input pair M_1/M_2 , whose inputs are defined by the base-emitter voltage difference $\Delta V_{BE1.2}$ between bipolar transistors Q_1 and Q_2 . As a result, using the attenuated differential signal as a correction factor, we can derive the correction term V_{CT} as follows:

$$V_{CT} = \frac{V_{out}}{R_{out} \cdot G_{m1}} = \frac{G_{m2} \cdot [\beta \cdot T \cdot \ln(T) + \gamma \cdot T]}{G_{m1}} \quad (4)$$

where G_{m1} denotes the transconductance of the differential pair M_1/M_2 . Consequently, the revised expression for $\Delta V_{BE1.2}$ is derived as follows:

$$\Delta V_{BE1.2} = V_T \cdot \ln(n) - V_{CT} = \left[\frac{k}{q} \cdot \ln(n) - \frac{G_{m2}}{G_{m1}} \cdot \gamma \right] \cdot T - \frac{G_{m2}}{G_{m1}} \cdot \beta \cdot T \cdot \ln(T) \quad (5)$$

By properly adjusting the ratio of G_{m2}/G_{m1} , the high-order nonlinear term in the temperature coefficient of the traditional BGR circuit can be compensated, and then the temperature coefficient of the V_{REF} can be improved. The output voltage expression of the proposed BGR source with high-order curvature compensation can be expressed as

$$V_{REF} = V_{BE2} + \frac{R_2 + R_3}{R_3} \cdot \left\{ \left[\frac{k}{q} \cdot \ln(n) - \frac{G_{m2}}{G_{m1}} \cdot \gamma \right] \cdot T - \frac{G_{m2}}{G_{m1}} \cdot \beta \cdot T \cdot \ln(T) \right\} \quad (6)$$

where k is the Boltzmann constant. It can be seen that the temperature compensation for V_{BE} can be realized by properly adjusting the transconductance ratio G_{m2}/G_{m1} of the two differential input pairs. The ratio of G_{m2}/G_{m1} can be expressed as (7) and is basically determined by the W/L ratio of CMOS pairs, so the high accuracy of G_{m2}/G_{m1} could be achieved by careful layout design. Therefore, the compensation accuracy can be precisely designed.

$$\frac{G_{m2}}{G_{m1}} = \sqrt{\frac{2\mu_p \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_{G_{m2}} \cdot I_2}{2\mu_p \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_{G_{m1}} \cdot I_1}} = \sqrt{\frac{\left(\frac{W}{L}\right)_{G_{m2}} \cdot I_2}{\left(\frac{W}{L}\right)_{G_{m1}} \cdot I_1}} = \sqrt{\frac{N_2}{N_1}} \quad (7)$$

where N_1 and N_2 denote the width-to-length ratios of the input pair transistors and their corresponding tail current transistors, respectively. Adjusting N_1 and N_2 , thereby altering the G_{m2}/G_{m1} ratio, allows for precise control over the output voltage's compensation accuracy. In this design, N_1 and N_2 are set to 12 and 2, respectively. Table 1 presents the design parameters and critical dimensions of the proposed HCC_BGR circuit.

The simulation results of HCC_BGR output voltage temperature characteristics at the optimal compensation point are shown in Figure 3B. Simulation outcomes reveal that the HCC_BGR's output reference voltage (V_{REF}) stands at 1.23 V, exhibiting a temperature coefficient as low as 2.56 ppm/°C, spanning the temperature range of -20°C to 85°C . Compared with the traditional first-order bandgap reference (TRA_BGR), its accuracy is improved by 5.34 times. Figure 5 displays the outcomes of 200 Monte Carlo simulations for the HCC_BGR circuit's output reference voltage (V_{REF}) and its temperature coefficient. The simulation results indicate that V_{REF} averages 1.233 V, with a standard deviation of 3.376 mV. Across the temperature range from -20°C to 85°C , the temperature coefficient of V_{REF} averages 7.28 ppm/°C, with a standard deviation of 5.31 ppm/°C. Figure 6 shows the results of 200 Monte Carlo simulations for

TABLE 1 Design parameters and critical dimensions of the proposed HCC_BGR circuit.

Transistor	W/L × M	Transistor	W/L × M	Transistor	W/L × M	Device	Parameter
M ₁	24/4 × 12	M ₁₀	16/4 × 4	M ₂₀	2/1 × 1	M _{P4}	16/4 × 2
M ₂	24/4 × 12	M ₁₁	16/4 × 4	M ₂₁	2/0.6 × 1	M _{P5}	16/4 × 2
M ₃	16/4 × 12	M ₁₃	8/0.6 × 1	M ₂₂	4/0.6 × 1	M _{N1}	4/1 × 1
M ₄	16/4 × 12	M ₁₄	4/0.6 × 1	M ₂₃	4/0.6 × 1	Q ₁ = Q ₃	5/5 × 1
M ₅	16/4 × 12	M ₁₅	4/1 × 1	M ₂₄	4/0.6 × 1	Q ₂	5/5 × 8
M ₆	4/1 × 12	M ₁₆	4/0.6 × 1	M ₂₅	4/0.6 × 1	R ₁ = R ₂	77 kΩ
M ₇	4/1 × 12	M ₁₇	2/1 × 1	M _{P1}	24/4 × 2	R ₃	8 kΩ
M ₈	32/8 × 22	M ₁₈	2/1 × 1	M _{P2}	24/4 × 2	R ₄	88 Ω
M ₉	32/8 × 22	M ₁₉	2/1 × 1	M _{P3}	16/4 × 2	C _C	2.3 pF

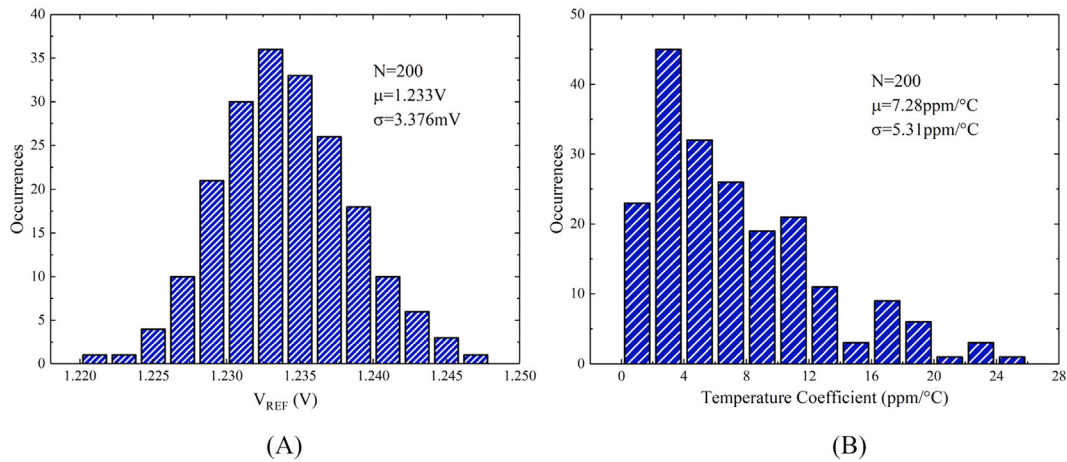
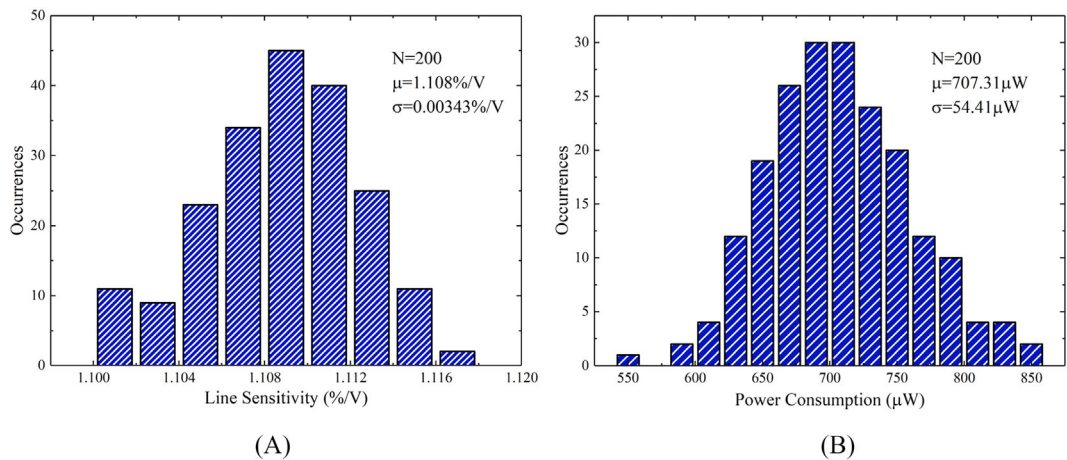
FIGURE 5 (A) Monte Carlo simulation results of V_{REF} . (B) Monte Carlo simulation results of TC of V_{REF} .

FIGURE 6 (A) Monte Carlo simulation results of LS. (B) Monte Carlo simulation results of power consumption.

the line sensitivity (LS) and power consumption of the HCC_BGR circuit in the 2.4- to 5-V supply range. These simulation results reveal that the average LS is 1.108%/V, with a standard deviation of 0.00343%/V. Simultaneously, the average power consumption is 707.31 μW , with a standard deviation of 54.41 μW .

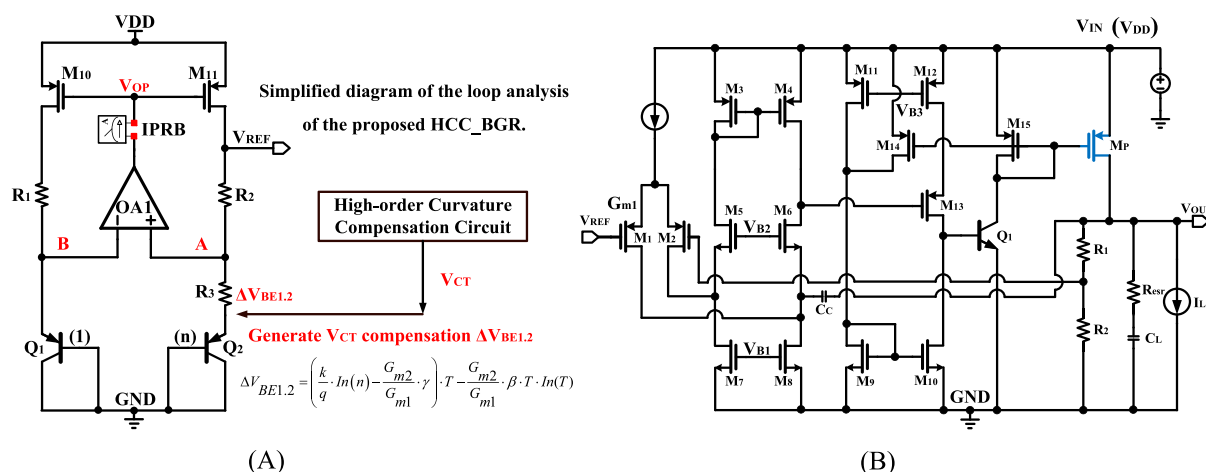


FIGURE 7 (A) Simplified diagram of the loop analysis of the proposed HCC_BGR. (B) The circuit diagram of the LDO.

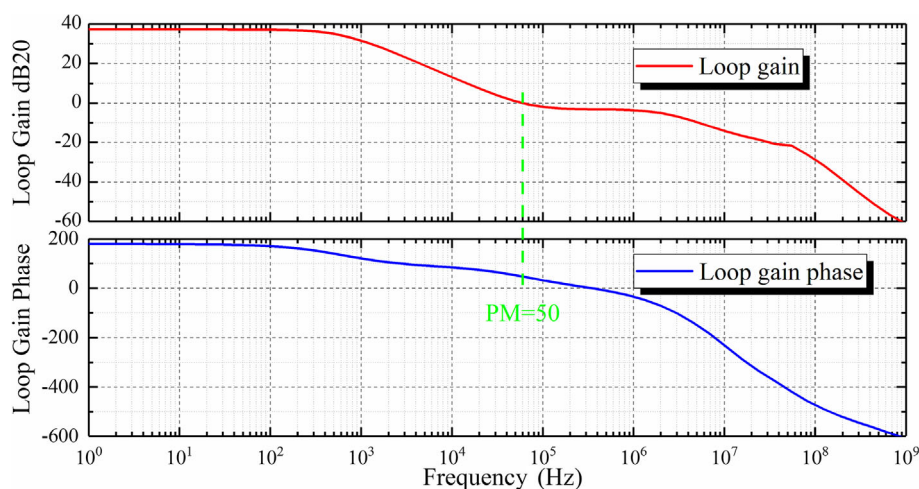


FIGURE 8 Loop stability simulation results of the proposed HCC_BGR.

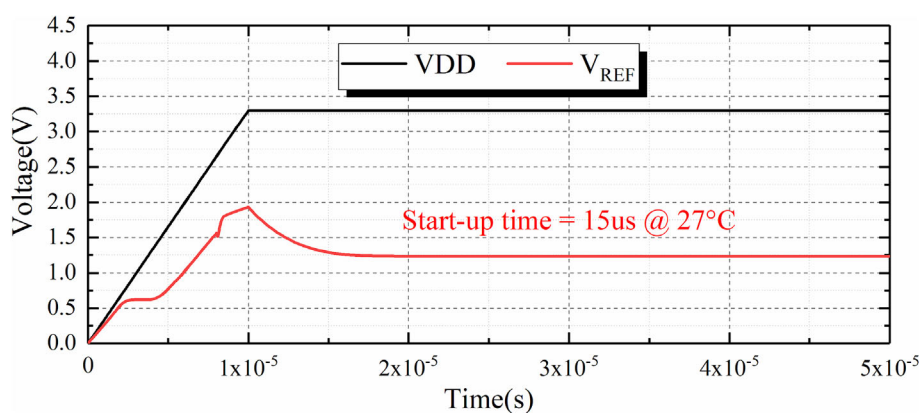


FIGURE 9 Transient simulation results of the proposed HCC_BGR.

The proposed HCC_BGR circuit includes feedback loops. For stable operation across diverse process-voltage-temperature (PVT) conditions, the circuit's negative feedback loop must surpass its positive counterpart. The simplified diagram of the loop analysis of the proposed HCC_BGR is shown in Figure 7A. The operational amplifier OA1's non-

inverting and inverting terminal voltages are denoted as V_A and V_B , respectively, with the output voltage labeled V_{OP} and its gain denoted as A_V .

Consequently, the negative feedback loop follows the V_A - V_{OP} - M_{11} - R_2 - V_A pathway, whereas the positive feedback loop follows the V_B - V_{OP} - M_{10} - R_1 - V_B pathway. The negative feedback loop employs a common source amplifier with transistor M_{11} as the input device and bipolar transistor Q_2 along with resistors R_2 and R_3 as the load. Similarly, the positive feedback loop utilizes a common source amplifier with transistor M_{10} as the input device and bipolar transistor Q_1 along with resistor R_1 as the load. Figure 8 presents the loop stability simulation results for the proposed HCC_BGR circuit. The simulations reveal a loop gain of 37 dB and a phase margin of 50° for the VR source; therefore, the HCC_BGR circuit is stable.

Figure 9 presents the transient simulation results for the HCC_BGR circuit, specifically examining the startup circuit's performance. The results indicate that as the power supply voltage (V_{DD}) steadily rises to 3.3 V within 10 μ s, the VR's output voltage V_{REF} stabilizes at 1.23 V in just 15 μ s. This demonstrates the VR circuit's effective operation under the step-response condition of the voltage supply. In order to better reflect the advantages of the proposed high-order curvature-compensated BGR source, the two BGR sources are applied in the same LDO circuit. Figure 7B shows the

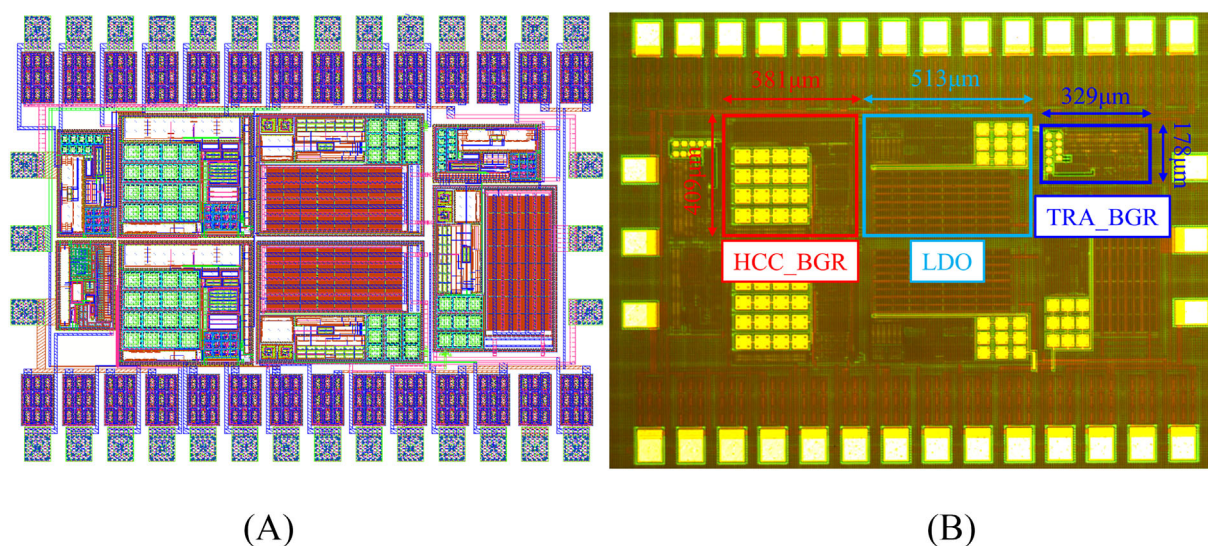


FIGURE 10 (A) The layout of the proposed HCC_BGR, TRA_BGR, and LDO. (B) The micrograph of the proposed HCC_BGR, TRA_BGR, and LDO.

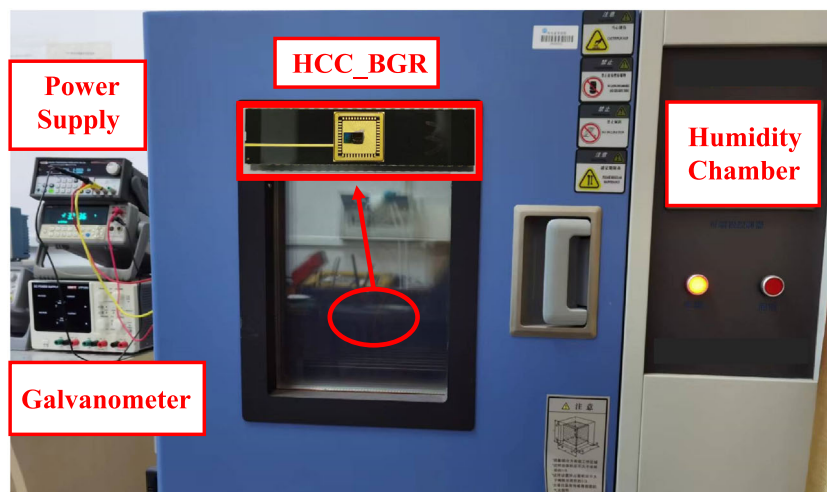


FIGURE 11 Experimental platform for the chip measurement.

schematic circuit diagram of the LDO. This LDO can stably convert the external input voltage to 3.3 V and then power the fluorescent fiber optic temperature sensor system to achieve accurate temperature measurement.

3 | MEASUREMENT RESULTS OF THE PROPOSED BGR AND LDO

The proposed BGR voltage source circuit with curvature compensation is fabricated using a standard 0.18- μm BCD process. The micrograph of the chip is shown in Figure 10. The total chip area is $1800\ \mu\text{m} \times 1366\ \mu\text{m}$, with the proposed HCC_BGR of $381\ \mu\text{m} \times 409\ \mu\text{m}$, the TRA_BGR of $329\ \mu\text{m} \times 178\ \mu\text{m}$, and the LDO of $513\ \mu\text{m} \times 409\ \mu\text{m}$. The measurement platform is shown in Figure 11, in which the humidity chamber can realize high- and low-temperature tests. The galvanometer can measure the reference voltage value of this chip at each stable temperature point.

When the power supply voltage VDD is 3.3 V, the chip is placed in the humidity chamber for the high- and low-temperature tests. In the measurement, the temperature varies from -20°C to 85°C . The output voltage values of the

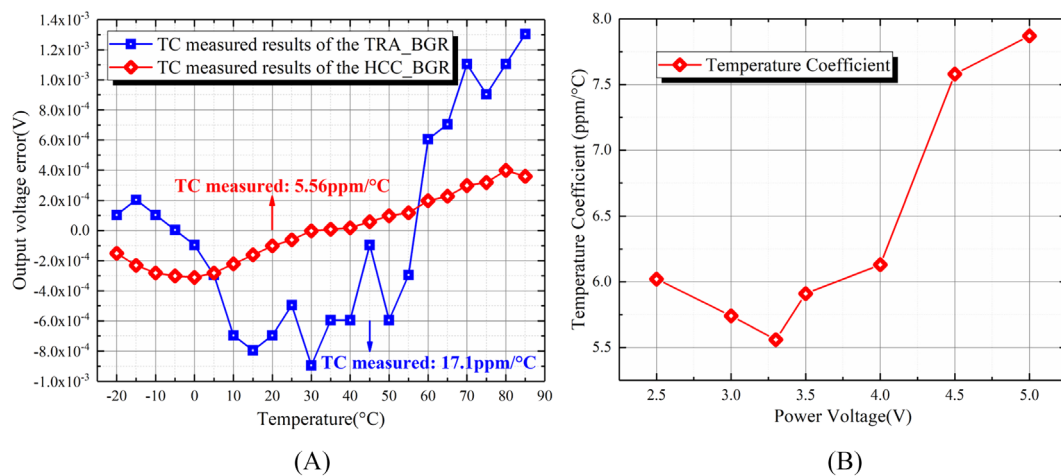


FIGURE 12 (A) Measurement results of TC for the proposed HCC_BGR and TRA_BGR from -20°C to 85°C . (B) Measurement results of HCC_BGR's TC versus VDD.

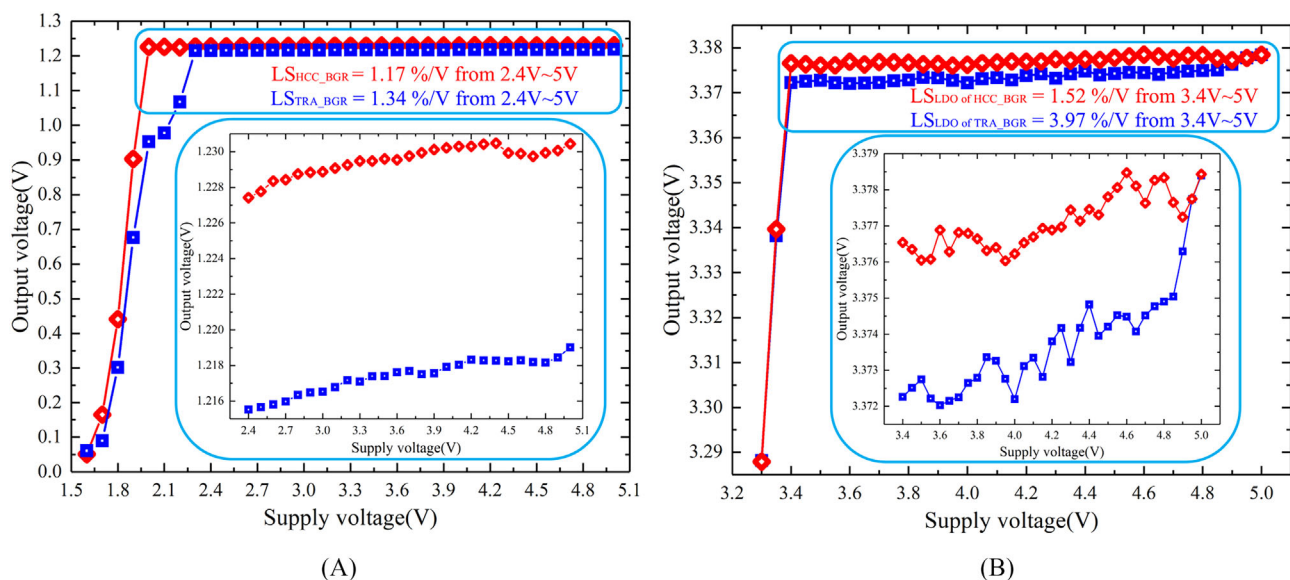


FIGURE 13 (A) Measured LS of BGR circuits from 2.4 to 5 V. (B) Measured LS of the LDOs from 3.4 to 5 V.

chip were recorded at each temperature, and the average value was obtained. The difference between each value and the average is plotted in Figure 12A. The blue and red curves are the measurement results of the traditional BGR and the proposed high-order curvature-compensated design, respectively. The temperature characteristic curve of the TRA_BGR is similar to a parabola with an upward opening and has a zero TC voltage point at -5°C and 56°C . Through calculation, the temperature coefficient of TRA_BGR is $17.1\text{ ppm}/^{\circ}\text{C}$ from -20°C to 85°C . The proposed HCC_BGR TC curve is relatively linear and has a temperature coefficient of $5.56\text{ ppm}/^{\circ}\text{C}$, which is 3.07 times lower than the traditional design. The zero TC voltage point is in the range of $30\text{--}40^{\circ}\text{C}$ and close to room temperature. Figure 12B displays the relationship between the supply voltage VDD and the TC of HCC_BGR. At a 3.3-V supply voltage, the TC reaches its optimum of $5.56\text{ ppm}/^{\circ}\text{C}$. Above this voltage, TC exhibits a steady increase with the increments of VDD. This shows that the proposed high-order curvature-compensated BGR source has higher voltage accuracy. When it is applied to the

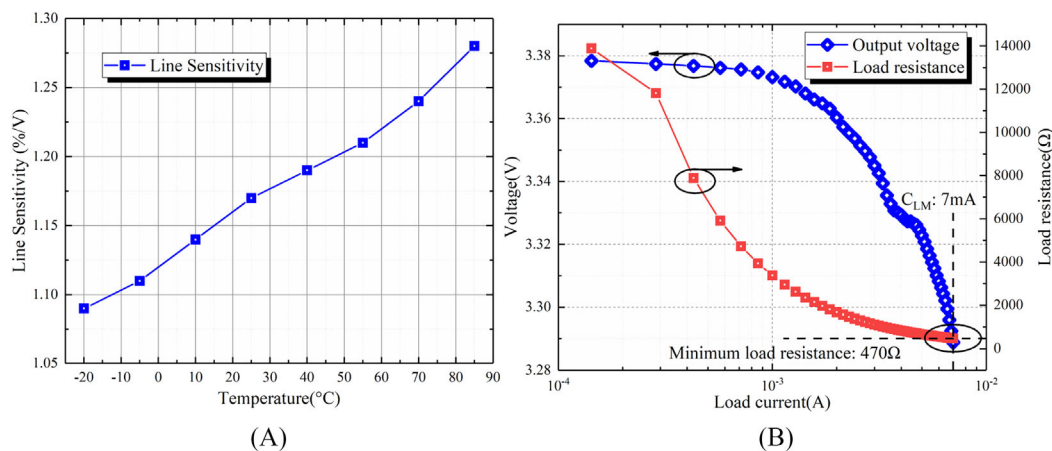


FIGURE 14 (A) Measured LS of the proposed HCC_BGR from -20°C to 85°C . (B) Load resistance measurement results when the HCC_BGR is applied to an LDO.

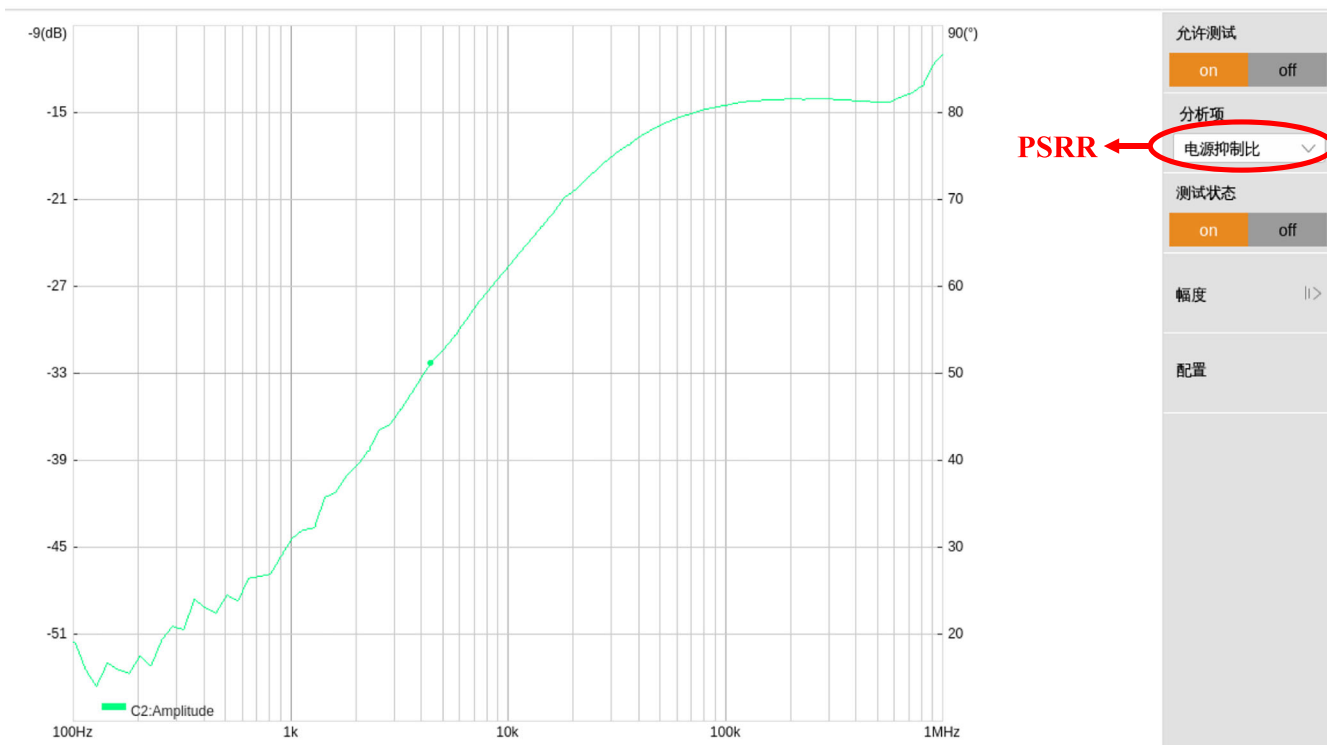


FIGURE 15 Measured PSRR of the proposed HCC_BGR.

LDO circuits, it can improve the stability of the power supply, thereby ensuring the temperature measurement accuracy of the fluorescent fiber optic stabilized sensor system.

Figure 13A shows the measured results of the LS. When the power supply changes from 2.4 to 5 V, the HCC_BGR output voltage slightly drifts to 3.051 mV, and the resulting LS is 1.17%/V. The LS of TRA_BGR is 1.34%/V. When the TRA_BGR and HCC_BGR circuits are used in the same LDO, the corresponding LS of the LDO is also measured. The measurement results are shown in Figure 13B. When the supply voltage increases from 3.4 to 5 V, the LDO with the proposed HCC_BGR has an LS of 1.52%/V, while the LS of the LDO with TRA_BGR is 3.97%/V. This corresponds to an improvement of approximately 2.61 times, which benefits from the proposed higher order curvature compensation circuit. The LS of HCC_BGR was measured across various temperature points to determine its dependency on

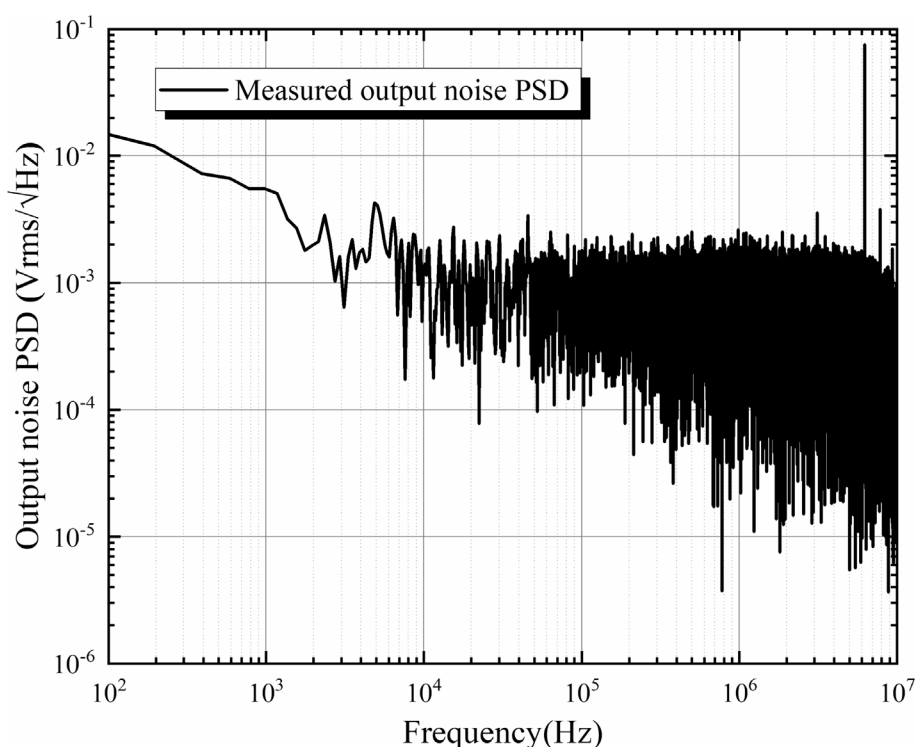


FIGURE 16 Measured noise PSD of the proposed HCC_BGR.

TABLE 2 Performance of this work compared to other references.

	This work	Ref. [4] JSSC 2021	Ref. [8] TCAS I 2016	Ref. [12] ISSCC 2015	Ref. [14] TVLSI 2020	Ref. [15] TCAS I 2022	Ref. [17] TCAS II 2019
Tech. (nm)	180	130	180	130	65	180	130
Type	BCD	CMOS	CMOS	CMOS	CMOS	CMOS	CMOS
Min VDD (V)	2	3.3	1.3	0.5	1	3.2	0.3
V _{REF} (V)	1.22	1.16	0.547	0.498	0.43	0.8	0.2418
LS (%/V)	1.17	0.03	0.08	2	2.63	0.0146	18
Temp. range (°C)	−20 to 85	−40 to 150	−40 to 140	0 to 80	−30 to 90	−25 to 125	0 to 80
Nominal current (μA)	220	120	28	0.064	2.25	409	4.12
Noise PSD (V _{rms} /√Hz)	113 μ	175.5 μ	0.356 μ	N/A	N/A	0.44 μ	N/A
PSRR (dB)	51	75	N/A	40	N/A	56.5	34.7
Area (mm ²)	0.155	0.08	0.009	0.0264	0.014	0.256	0.014
TC best (ppm/°C)	5.56	5.78	1.67	75	22	0.7	24.2

temperature. Figure 14A reveals a direct correlation, indicating a consistent increase in LS with the rise in temperature. In the integration of HCC_BGR with an LDO, the Keysight B2910BL precision source/measure unit is used to measure the load capacity. Figure 14B illustrates that increasing the load current to 7 mA leads to a reduction in output voltage from 3.38 to 3.3 V. Meanwhile, this measurement result demonstrates that the HCC_BGR, combined with an LDO, supports a minimum load resistance of 470 Ω . Therefore, the higher order curvature compensation reference source proposed in this work can improve the robustness of the power supply, thus ensuring an accurate temperature measurement.

To evaluate the power supply rejection ratio (PSRR) of the proposed HCC_BGR, we utilized the SDS6000 Pro digital storage oscilloscope in conjunction with the SAG1021 arbitrary waveform generator. Figure 15 demonstrates that HCC_BGR's PSRR is 51 dB at 100 Hz and decreases to 45 dB as the frequency increases to 1 kHz. Furthermore, to evaluate the noise performance of the HCC_BGR, the RIGOL MSO8204 oscilloscope was utilized for FFT analysis of its output voltage. The oscilloscope's built-in V_{rms} measurement tool (part of its FFT function) was used to ascertain V_{REF} 's effective amplitude in the frequency domain, reflecting HCC_BGR's output noise. Figure 16 displays the noise power spectral density (PSD) measurement results of the HCC_BGR. It shows that the output noise is 504 μV_{rms} at 1 kHz, which reduces to 113 μV_{rms} at 10 kHz. Table 2 summarizes the circuit performance of this work and other references. This work is better than the circuits proposed in other references in terms of temperature coefficients and circuit complexity.

4 | CONCLUSIONS

In this paper, a BGR circuit with high-order curvature compensation is proposed. Two LDOs with the proposed HCC_BGR and TRA_BGR are also designed and manufactured using a standard 0.18- μm BCD process. The measurement results show that the proposed HCC_BGR can output a reference voltage with a value of 1.22 V, and its temperature coefficient is 5.56 ppm/ $^{\circ}\text{C}$ in the temperature range of -20°C to 85°C , which is 3.07 times lower than the TRA_BGR. When the supply voltage changes from 3.4 to 5 V, the LDO with the proposed HCC_BGR circuit has an LS of 1.52%/V, corresponding to an enhancement by a factor of ~ 2.61 compared to the conventional structure. In summary, the HCC_BGR circuit proposed in this paper has a very low-temperature coefficient, which can provide a good reference solution for the fluorescent optical fiber temperature sensor system.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available on request from the corresponding author.

ORCID

Jingjing Liu  <https://orcid.org/0000-0001-5285-4997>

REFERENCES

1. Widlar RJ. New developments in IC voltage regulators. *IEEE J Sol State Circuits*. 1971;6(1):2-7. doi:10.1109/JSSC.1971.1050151
2. Wang B, Law MK, Bermak A. A precision CMOS voltage reference exploiting silicon bandgap narrowing effect. *IEEE Trans Electron Dev*. 2015;62(7):2128-2135. doi:10.1109/TED.2015.2434495
3. Lee SY, Liao ZX, Lee CH. Energy-harvesting circuits with a high-efficiency rectifier and a low temperature coefficient bandgap voltage reference. *IEEE Trans Very Large Scale Integr (VLSI) Syst*. 2019;27(8):1760-1767. doi:10.1109/TVLSI.2019.2908670
4. Chen K, Petruzzi L, Hulfachor R, Onabajo M. A 1.16-V 5.8-to-13.5-ppm/ $^{\circ}\text{C}$ curvature-compensated CMOS bandgap reference circuit with a shared offset-cancellation method for internal amplifiers. *IEEE J Sol State Circuits*. 2021;56(1):267-276. doi:10.1109/JSSC.2020.3033467
5. Palani RK, Bhagavatula S, Yuen DK. A sub-1-V 8.5-ppm/ $^{\circ}\text{C}$ sampled bandgap voltage reference. *IEEE Trans Circuits Syst II Express Briefs*. 2022;69(10):4153-4157.
6. Lee CC, Chen HM, Lu CC, et al. A high-precision bandgap reference with a V-curve correction circuit. *IEEE Access*. 2020;8:62632-62638. doi:10.1109/ACCESS.2020.2984800
7. Seung M, Choi W, Hur S, Kwon I. Cold junction compensation technique of thermocouple thermometer using radiation-hardened-by-design voltage reference for harsh radiation environment. *IEEE Trans Instr Meas*. 2022;71:2005807. doi:10.1109/TIM.2022.3205931
8. Chen HM, Lee CC, Jheng SH, Chen WC, Lee BY. A sub-1 ppm/ $^{\circ}\text{C}$ precision bandgap reference with adjusted-temperature-curvature compensation. *IEEE Trans Circuits Syst I: Reg Papers*. 2017;64(6):1308-1317. doi:10.1109/TCSI.2017.2658186

9. Kim DK, Shin SU, Kim HS. A BGR-recursive low-dropout regulator achieving high PSR in the low- to mid-frequency range. *IEEE Trans Power Electron.* 2020;35(12):13441-13454. doi:[10.1109/TPEL.2020.2996771](https://doi.org/10.1109/TPEL.2020.2996771)
10. Khan SR. Sub-1 V, 5.5 ppm/°C, high PSRR all CMOS bandgap voltage reference. *IETE J Res.* 2020;66(4):527-532. doi:[10.1080/03772063.2018.1497550](https://doi.org/10.1080/03772063.2018.1497550)
11. Vergine T, De Matteis M, Michelis S, Traversi G, De Canio F, Baschiroto A. A 65 nm rad-hard bandgap voltage reference for LHC environment. *IEEE Trans Nucl Sci.* 2016;63(3):1762-1767. doi:[10.1109/TNS.2016.2550581](https://doi.org/10.1109/TNS.2016.2550581)
12. Shrivastava A, Craig K, Roberts NE, Wentzloff DD, Calhoun BH. "5.4 A 32 nW bandgap reference voltage operational from 0.5V supply for ultra-low power systems," 2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers, San Francisco, CA, USA. 2015;1-3.
13. Fu X, Colombo DM, Yin Y, El-Sankary K. Low noise, high PSRR, high-order piecewise curvature compensated CMOS bandgap reference. *IEEE Access.* 2022;10:110970-110982. doi:[10.1109/ACCESS.2022.3215544](https://doi.org/10.1109/ACCESS.2022.3215544)
14. Zhou B, Jin Y, Zhao F. Sub-1-V BGR and POR hybrid circuit with 2.25-μA current dissipation and low complexity. *IEEE Trans Very Large Scale Integr (VLSI) Syst.* 2020;28(10):2228-2232. doi:[10.1109/TVLSI.2020.3009452](https://doi.org/10.1109/TVLSI.2020.3009452)
15. Huang S, Li M, Li H, et al. A sub-1 ppm/°C bandgap voltage reference with high-order temperature compensation in 0.18-μm CMOS process. *IEEE Trans Circuits Syst I: Reg Papers.* 2022;69(4):1408-1416.
16. Parisi A, Finocchiaro A, Papotto G, Palmisano G. Nano-power CMOS voltage reference for RF-powered systems. *IEEE Trans Circuits Syst II Express Briefs.* 2018;65(10):1425-1429.
17. Toledo P, Cordova D, Klimach H, Bampi S, Crovetto PS. A 0.3–1.2 V Schottky-based CMOS ZTC voltage reference. *IEEE Trans Circuits Syst II Express Briefs.* 2019;66(10):1663-1667.
18. Ji Y, Lee J, Kim B, Park H-J, Sim J-Y. A 192-pW voltage reference generating bandgap- V_{th} with process and temperature dependence compensation. *IEEE J Sol State Circuits.* 2019;54(12):3281-3291. doi:[10.1109/JSSC.2019.2942356](https://doi.org/10.1109/JSSC.2019.2942356)
19. Banba H, Shiga H, Umezawa A, et al. A CMOS bandgap reference circuit with sub-1-V operation. *IEEE J Sol State Circuits.* 1999;34(5):670-674. doi:[10.1109/4.760378](https://doi.org/10.1109/4.760378)
20. Duan Q, Roh J. A 1.2-V 4.2-ppm/°C high-order curvature-compensated CMOS bandgap reference. *IEEE Trans Circuits Syst I: Reg Papers.* 2015;62(3):662-670. doi:[10.1109/TCSI.2014.2374832](https://doi.org/10.1109/TCSI.2014.2374832)
21. Aminzadeh H. Subthreshold reference circuit with curvature compensation based on the channel length modulation of MOS devices. *Int J Circ Theory Appl.* 2022;50(4):1082-1100. doi:[10.1002/cta.3201](https://doi.org/10.1002/cta.3201)
22. Liu N, Geiger RL, Chen D. Sub-ppm/°C bandgap references with natural basis expansion for curvature cancellation. *IEEE Trans Circuits Syst I: Reg Papers.* 2021;68(9):3551-3561. doi:[10.1109/TCSI.2021.3096166](https://doi.org/10.1109/TCSI.2021.3096166)
23. Aminzadeh H, Valinezhad MM. 0.7-V supply, 21-nW all-MOS voltage reference using a MOS-only current-driven reference core in digital CMOS. *Microelectron J.* 2020;102:104841. doi:[10.1016/j.mejo.2020.104841](https://doi.org/10.1016/j.mejo.2020.104841)
24. Aminzadeh H, Valinezhad MM. Picowatt 0.3-V MOS-only voltage reference based on a picoamp cascode current generator. *Dermatol Int.* 2022;87:284-292. doi:[10.1016/j.vlsi.2022.07.014](https://doi.org/10.1016/j.vlsi.2022.07.014)
25. Shao CZ, Kuo SC, Liao YT. A 1.8-nW, -73.5-dB PSRR, 0.2-ms startup time, CMOS voltage reference with self-biased feedback and capacitively coupled schemes. *IEEE J Sol State Circuits.* 2021;56(6):1795-1804. doi:[10.1109/JSSC.2020.3028506](https://doi.org/10.1109/JSSC.2020.3028506)
26. Thakur A, Pandey R, Rai SK. Low temperature coefficient and low line sensitivity subthreshold curvature-compensated voltage reference. *Int J Circ Theory Appl.* 2020;48(11):1900-1921. doi:[10.1002/cta.2857](https://doi.org/10.1002/cta.2857)
27. Aminzadeh H, Valinezhad MM. A nano-power sub-bandgap voltage and current reference topology with no amplifier. *AEU Int J Electron Commun.* 2022;148:154174. doi:[10.1016/j.aeue.2022.154174](https://doi.org/10.1016/j.aeue.2022.154174)

How to cite this article: Xiong B, Mo W, Yan F, Guan J, Ge W, Liu J. A high-precision voltage reference with a curvature-compensated bandgap for fluorescence detection. *Int J Circ Theor Appl.* 2024;52(11):5437-5449. doi:[10.1002/cta.4054](https://doi.org/10.1002/cta.4054)