On-Chip Power Source Using Optimized On-Chip Solar Cells Based on a Standard Bulk CMOS Process for Single-Chip Self-Powered Smart Microsensors

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On-Chip Power Source Using Optimized On-Chip Solar Cells Based on a Standard Bulk CMOS Process for Single-Chip Self-powered Smart Microsensors

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Enhancing the photoelectric conversion efficiency of on-chip solar cells can significantly improve the performance of on-chip solar energy harvesting systems. This advancement is important for the realization of self-powered smart microsensors for Internet of Everything (IoE) applications. To enhance the photoelectric conversion performance of on-chip solar cells based on a standard bulk CMOS process, the surface electrode models for the solar cell is constructed. It is verified by simulations and measurements that square ring electrode (RE) and center electrode (CE) do not cause significant differences in the internal resistance of on-chip solar cells. Adopting the CE instead of the RE electrodes in the layout can greatly reduce the shadowing effect of the surface electrodes. In addition, to solve the problem of light blockage caused by the large number of interconnections in the segmented on-chip solar cells, highly doped regions are used to replace some of the metal interconnections, which can significantly reduce the shadowing of metals. A 0.01 mm^2 segmented triple-well on-chip solar cells with the CEs and highly doped region as interconnection techniques is fabricated using a standard 0.18μm CMOS process. Measurement results show a 25.79% photoelectric conversion efficiency under solar simulator illuminations and has a 17.49% improvement compared to the conventional design. Utilizing the proposed on-chip solar cells, an on-chip energy harvesting power source has been realized, achieving a maximum conversion efficiency of 10.20% from incident solar power to voltage output power. Despite variations in illumination and load, this energy harvesting power source is still able to maintain a relatively stable output voltage of 1V.

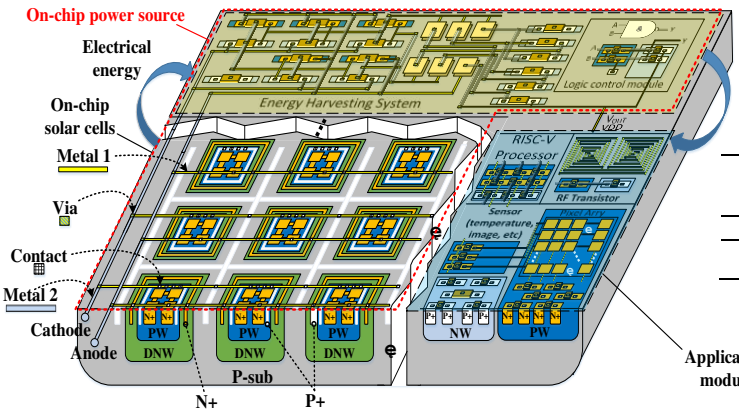


TABLE I
THE POWER CONSUMPTIONS OF TEMPERATURE SENSOR

Temperature Sensor	[6]	[7]	[8]	[9]	[10]
CMOS Process	0.18μm	0.15μm	0.15μm	0.13μm	0.13μm
Power	75nw	2.5nw	23nw	150nw*	150nw

*Simulation result

Fig. 1 | Conceptual diagram of on-chip solar cells and energy harvesting system forming an on-chip power source to power single-chip smart microsensors. The proportion of the on-chip power source is enlarged respect to others for illustration purpose.

Microsensors with self-powered capabilities have substantial potential in Internet of Everything applications, as they are small and can operate independently without reliance on electrical grid supply, harvesting energy from the ambient environment instead [1-4]. By implementing solar cells using standard CMOS processes, the size of these sensors would be significantly reduced, as it integrates solar cells, energy harvesting systems, and sensor systems on a single chip, as shown in Fig. 1. The application modules can realize functions such as temperature sensing, image sensing, simple signal processing and data transmission. The on-chip solar cells and energy harvesting systems form an on-chip power source that provides a stable, adapted working voltage to the application modules under certain lighting conditions. Compatibility and ease of integration with CMOS technology are additional key requirements for realizing low-cost, large-scale systems for the consumer market [5]. This self-powered microsensor on a single chip can be manufactured using only standard CMOS processes and simple packaging, without any special fabrication processes.

The evolution of low-power consumption sensor technology has led to the creation of CMOS sensors that function effectively on mere nano-watts of power, as shown through representative works in TableI [6-10]. Solar light, a pervasive and high-density energy source, with an energy density reaching up to 0.16μW/lux·cm2, could provide sufficient energy for microsensors through small size on-chip solar cells. The application of on-chip integrated energy harvesting systems to collect solar energy in microsensors has been successfully implemented in various studies [11, 12].

The proposed on-chip power source includes an energy harvesting system and solar cells. The overall energy conversion efficiency is determined by the voltage conversion efficiency of the energy harvesting system and the photoelectric conversion efficiency of the on-chip solar cells. The former one is well investigated by researchers, but few studies have been done for the latter. Therefore, enhancing the photoelectric conversion efficiency of on-chip solar cells is an effective method to improve the performance of on-chip solar energy harvesting power source. However, optimizing the efficiency of on-chip solar cells involves a tradeoff between photon-generated charge collection and electrode shadowing [13,14]. Although larger electrodes improve conductivity and reduce internal resistance, they also increase cell shadowing due to larger metal coverage, compromising photoelectric conversion capability. Conversely, poor electrode designs degrade conductivity, raising internal resistance and decreasing photoelectric efficiency. While there have been studies using backside electrodes [15] or transparent electrodes [16] to mitigate electrode shadowing, such special processes raise manufacturing cost and integration challenges. Due to the constraints of standard bulk CMOS processes, it is important to optimize the surface electrode design of on-chip solar cells in order to enhance their photoelectric conversion efficiency. Existing studies focuses largely on repurposing electrodes as gratings [17] or capacitors [18], with little exploration of optimized layouts to balance the internal resistance and shadowing.

A common ring electrode layout for on-chip solar cells, depicted in Fig. 2, has been widely utilized [19-22]. Researchers apply this topology with vague rationale and random dimensions and positions. For example, one variant has a large ring electrode along the N-well inner edge, as shown in Figure 2a, the other has a smaller ring for the electrode in Figure 2b. In the literature, there is no theoretical analysis to prove which one is better and what dimensions are the optimized design. S_0 determining an optimal electrode layout remains an important open question.

Existing researches indicate that using Maximum Power Point Tracking (MPPT) technology combined with off-chip energy storage is a common strategy for energy harvesting. Employing an off-chip miniaturized battery storage system to collect excess energy during strong illumination can provide energy supplementation during insufficient light conditions to maintain normal operation of the load [23,24]. However, in pursuit of a fully on-chip power source system, we have not utilized off-chip storage components. Under standard Bulk CMOS processes, on-chip energy storage is challenging to implement, leading us to abandon the strategy of storing excess energy. Instead, a direct output strategy is adopted. Therefore, to enable the chip to function under lower light conditions or to handle more load under the same illumination conditions, improving the photoelectric conversion capability of the on-chip solar cells is one of the most effective methods.

As the on-chip solar cells and the energy harvesting system are integrated on the same substrate, the P-type regions in the on-chip solar cells, namely PW and P-sub, are utilized as the cathode and grounded; whereas the N-type regions, DNW and N+, function as the anode for electrical energy output. Due to the voltage in the N-type region being lower than that in the P-type region under illuminations, the anode outputs a negative voltage, implying that the designed energy harvesting system needs to be capable of handling negative voltages. Additionally, as we adopt a direct output strategy, it necessitates the conversion of light energy into directly usable electrical energy. Surveys of some low-power sensors based on CMOS processes indicate that their operating voltages range from 0.8 to 1.2V; therefore, the proposed energy harvesting system should output a voltage within this range. In this work, the energy harvesting system is designed to output a voltage of 1V. Furthermore, in practical applications, as both the illumination environment and the load are dynamically changing, it is also necessary to ensure the stability of the 1V output voltage.

This work investigates various surface electrode layouts to improve on-chip solar cell photoelectric conversion efficiency, examining tradeoffs between internal resistance and shadowing. An optimized electrode layout technique is proposed to minimize the internal resistance while significantly reducing the shadowing. By applying the proposed surface electrode and highly doped region as interconnection, a segmented triple-well on-chip solar cell design is optimized based on a standard bulk CMOS process. Additionally, this work proposes an energy harvesting system that can convert the low negative voltage output from the optimized on-chip solar cells into a stable 1V voltage, maintaining stability amidst variations in load or illumination. The rest of this paper is organized as follows.

Lateral Resistance

The internal resistance of on-chip solar cells includes lateral resistance and vertical resistance of doped silicon region, and electrode resistance. However, the doped region is extremely thin and metal electrode resistance is much smaller than the lateral resistance. Consequently, the latter two components can be ignored and the lateral resistance within the doped silicon predominantly dictates the internal resistance. In order to analyze the lateral resistance, the electric field distribution of the N+ thin layer needs to be obtained. Hence, a highly doped N-type square silicon with one small anode and one large cathode square ring electrodes is simulated. Figure 2c illustrates the electric field distribution of the surface. It can be seen that the equipotential lines between electrodes are primarily circular and become more square-like close to the electrodes. In 3D, the circular and square equipotential lines form their respective circular and square equipotential surface.

Based on the above simulation results, equivalent circuit models of on-chip

solar cell with electrodes could be constructed. Figure 2d illustrates a square N-type highly doped silicon with one large anode and one small cathode square ring electrodes. The distances between the two electrodes to the center are Ln and L0 respectively. Resistance r between the two electrodes can be expressed by (1).

$$r = \frac{\rho \cdot L}{S} \tag{1}$$

where ρ is the doped region resistivity, L is the resistor length, and S is the resistor cross-sectional area, which is equal to the equipotential surface. From the cathode to the anode, S increases as the equipotential surface increases. In the circular region, SC is approximated to be 2πlh, while in the square region, SS is approximated to be 8lh, where l is the distance from equipotential surface to the center and h is the thickness of the doped region. Considering the circular equipotential surfaces, rc is equal to (2); rs for square surfaces, is equal to (3).

$$r_c = \int_{L_0}^{L_n} \frac{\rho}{2\pi l h}\, dl \tag{2}$$

$$r_s = \int_{L_0}^{L_n} \frac{\rho}{8 l h}\, dl \tag{3}$$

Through calculation and simplification, (2) and (3) can be reduced to (4) and (5) respectively.

$$r_c = \frac{\rho}{2\pi h} \cdot \ln \frac{L_n}{L_0} \tag{4}$$

$$r_s = \frac{\rho}{8h} \cdot \ln \frac{L_n}{L_0} \tag{5}$$

Due to the coexistence of circular and square equipotential surfaces in reality, the resistance r must satisfy (6).

$$\frac{\rho}{8h} \cdot \ln \frac{L_n}{L_0} \le r \le \frac{\rho}{2\pi h} \cdot \ln \frac{L_n}{L_0} \tag{6}$$

Square Ring Electrodes

Figure 2e illustrates an on-chip solar cell with a square N+/P-sub structure, where the N+ region utilizes a conventional large square ring electrode layout. The square ring electrode RE lies near to the N+ edge at a distance LRE to the center. The P-sub contact electrode encircles the N+ periphery. For simplified analysis, it is assumed that the equipotential lines are circular.

When the on-chip solar cell is under illumination, photogenerated carriers appearing in the region between L0 and Ln can overcome the lateral resistance to reach the electrode.

On the other hand, in the central small region within L0, experience similar electric field strengths in all directions, causing near-zero net electric force. Moreover, the central region has the largest lateral resistance to the electrode. These impede the large ring electrode from collecting these central carriers. The small inner central region contributes negligible photogenerated current. It can be regarded as a wasted region. Therefore, our model reasonably omits this L0 inner area.

Figure 2f presents the equivalent circuit model for the on-chip solar cell's large square ring electrode, with current sources denoting photogenerated current from the regions along each N+ doped equipotential surface. The lateral resistance between adjacent equipotential surface is Rn-i. Importantly, equipotential lines farther from the center correspond to larger surface area,

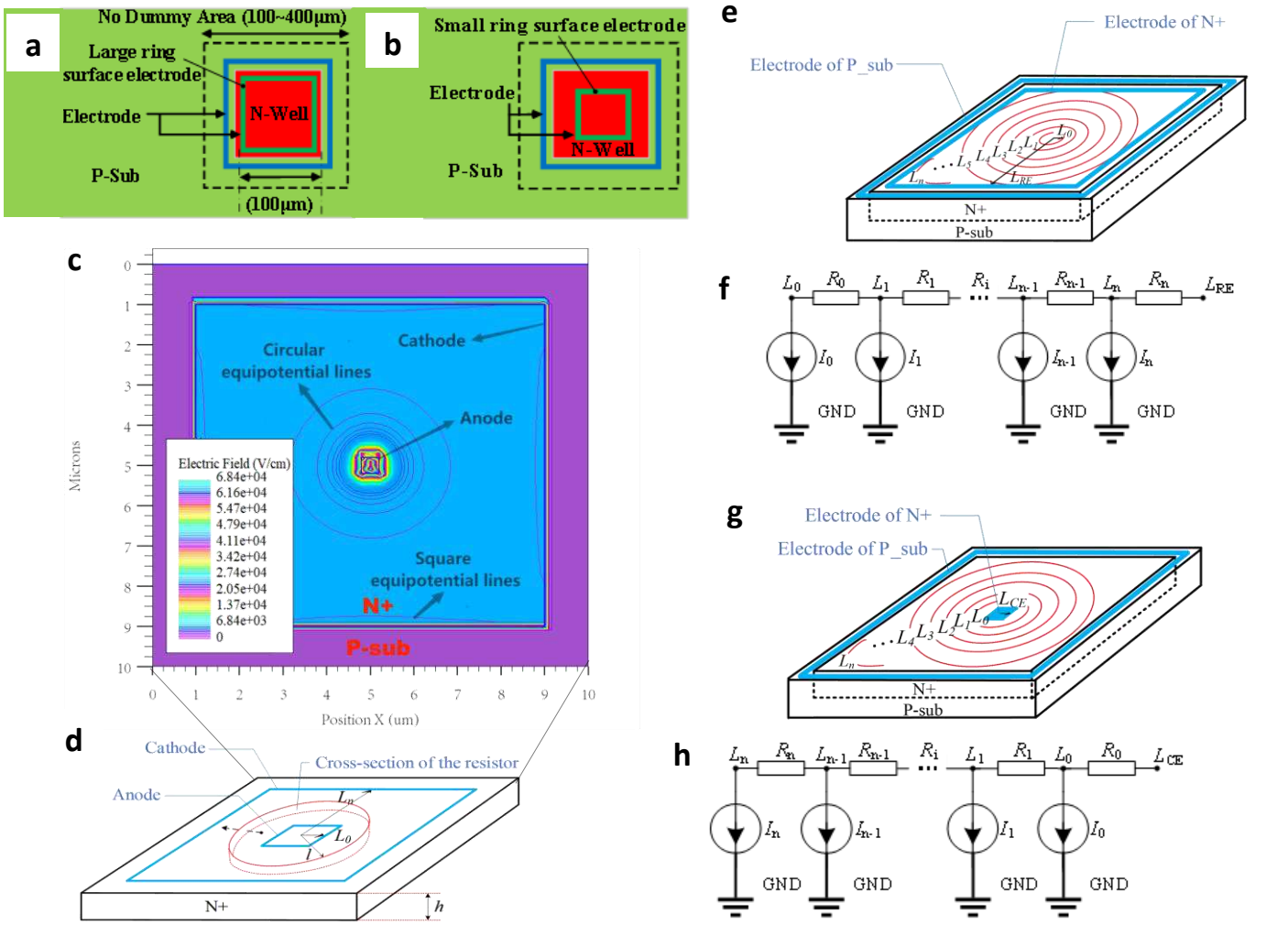


Fig. 2 | Modeling of surface electrodes. a, Layout diagram of a large ring-shaped surface electrode [19]. **b**, Layout diagram of a small ring-shaped surface electrode. **c**, Electric field distribution of the square silicon N+ in the P-sub. There are one large and one small square ring electrodes inside the N+. The large ring is grounded as the cathode, and the small ring is connected to 1V as the anode. **d**, The lateral resistance model of a N-type highly doped silicon. **e**, The on-chip solar cell with a large square ring electrode in the N+ region. **f**, Equivalent circuit of the on-chip solar cell with large square ring electrode. **g**, The on-chip solar cell with a small central electrode in the N+ region. **h**, The equivalent circuit of the on-chip solar cell with a central electrode.

producing more photocurrent. Hence, outer current sources are larger than the inner ones. Equivalent circuit analysis yields the N+ doped region's total lateral resistance rRE as (7).

$$r_{RE} = \sum_{i=0}^{n} \frac{I_{n-i}}{I_0+I_1+\cdots+I_n} \cdot \sum_{j=0}^{i} R_{n-j} \tag{7}$$

Applying (4), we sequentially determine the lateral resistance from Ln, Ln-1, ..., L2, L1 to the N+ electrode respectively. Substituting them into (7) yields the N+ region's equivalent resistance rRE as (8).

$$r_{RE} = \sum_{i=0}^{n} \frac{I_{n-i}}{I_0+I_1+\cdots+I_n} \cdot \frac{\rho}{2\pi h} \cdot \ln \frac{L_i}{L_0} \tag{8}$$

where Li=L0+idl. As dl approaches 0, n approaches infinity. After simplification, the N+ region's equivalent resistance rRE approximates to be (9). When accounting for near-electrode square equipotential surfaces, rRE is rewritten as (10), where k represents the percentage of the circular equipotential surface.

$$r_{RE} = \frac{\rho}{2\pi h} \cdot \ln \frac{L_n}{3L_0} \tag{9}$$

$$r_{RE} = k \cdot \frac{\rho}{2\pi h} \cdot \ln \frac{L_n}{3L_0} + (1-k) \cdot \frac{\rho}{8h} \cdot \ln \frac{L_n}{3L_0} \tag{10}$$

Square Center Electrodes

The on-chip solar cell shown in Figure 2g is similar to the structure in Figure 2e, except that the large square ring electrode in the N+ region is replaced by a small central electrode. The central electrode is located within the region L_0 from the center point, which is the region wasted by the large ring electrode case. The equivalent circuit is illustrated in Figure 2h. Following the analysis approach described earlier, considering only circular equipotential surfaces, the equivalent resistance r_{CE} of the on-chip solar cell with a central electrode in the N+ region can be approximated as (11). In the case when circular and square equipotential surfaces are considered simultaneously, r_{CE} can be expressed as (12).

$$r_{CE} = \frac{\rho}{2\pi h} \cdot \ln \frac{2L_n}{3L_0} \tag{11}$$

$$r_{CE} = k \cdot \frac{\rho}{2\pi h} \cdot \ln \frac{2L_n}{3L_0} + (1-k) \cdot \frac{\rho}{8h} \cdot \ln \frac{2L_n}{3L_0} \tag{12}$$

$$r_{CE} = k \cdot \frac{\rho}{2\pi h} \cdot \left(\ln \frac{L_n}{3L_0} + \ln 2\right) + (1-k) \cdot \frac{\rho}{8h} \cdot \left(\ln \frac{L_n}{3L_0} + \ln 2\right) \tag{13}$$

$$\Delta r = [k \cdot \frac{\rho}{2\pi h} + (1-k) \cdot \frac{\rho}{8h}] \cdot \ln 2 \tag{14}$$

Equation (12) can be expanded to be (13). Subtracting (10) from (13) yields the difference Δr between r_{CE} and r_{RE}, as shown in (14). It can be observed that there is a constant difference between the lateral resistances of r_{CE} and r_{RE}. When the on-chip solar cell has a large area, that is, Ln/3L0 is much larger than 2 (which can be easily satisfied), the constant term Δr can be neglected, i.e., $r_{CE} \approx r_{RE}$. This implies that for on-chip solar cells with large area, the layout configuration of CE and RE will result in nearly equivalent conductivity, but obviously CE has much lower shading rate. Therefore, in comparison to the RE, the CE has more advantages in terms of photoelectric conversion efficiency improvement.

Reducing metal1 contacts can effectively decrease the metal-induced recombination rate, thereby improving the photoelectric conversion capability of the solar cell [25]. For on-chip solar cells with very small areas, even if the effect caused by the constant term Δr cannot be neglected, the CE has more significant benefits in terms of reducing shading rate and reducing metal-induced recombination rate compared to the small advantage gained by the RE in improving conductivity. Therefore, the layout configuration of CE is still recommended.

Simulation of surface electrodes

The theoretical models are validated using both simulation and experimental results with fabricated devices. 3D simulations are first performed to validate the theoretical derivations by constructing three distinct surface electrodes, RE1, RE2, and CE, on an N+/P-sub cell as depicted in Fig. 3. The simulations model the influence of different electrodes on the load curve of a solar cell under vertical solar illumination with the same intensity. They can be divided into two groups. As shown in Figure 3a, the first group of simulations have RE1, RE2, and CE individually serving as the N+ connecting electrode, while floating the others. The second group of simulations, as shown in Figure 3b, c, and d, have RE1, RE2, and CE individually serving as the N+ connecting electrode, while eliminating the others. Figure 3e shows the simulation results. The first group results show that the short circuit current of CE is 12.0% higher than that of RE1, reflecting that even under the same shading rate, the smaller metal-induced recombination rate can enable CE to have a better performance. The second group of simulation results suggest that under the dual advantages of smaller metal-induced recombination rate and smaller shading rate, the short circuit current of CE in Figure 3d is 15.4% higher than that of RE1 in Figure 3b. The trends in the simulation results are consistent with our analysis, and the key parameter values are summarized in Table II.

Testing of surface electrodes

To undertake experimental studies, a 0.1mm^2 on-chip solar cell of N+/P-sub using a standard 0.18μm CMOS process is designed and fabricated, whose micrograph is shown in Figure 3f. Similar to Fig. 3, its surface electrodes are divided into RE1, RE2, and CE. The rest square rings in the N+ region are just floating metals. The size of CE LCE uses the minimum metal1 size with single contact via regulated by the layout design rules. The ratio of N+ size to LCE is 124. The on-chip solar cell is optically tested under vertical illumination of a Xenon lamp with 100 klux. The I-V curves of RE1, RE2, and CE are shown in Figure 3f. It can be seen that there is no significant difference between the I-V curves of RE1, RE2, and CE, which agrees with the analysis and simulation results. If without RE metal shadowing, the performance of CE would be better.

Using CE as the surface electrode of on-chip solar cells can not only ensure conductivity but also greatly reduce the metal coverage area and shadowing. Compared to the large number of contacts of RE, CE has only a small number of metal1 contacts, thereby improving the photoelectric conversion capability of the solar cell. Therefore, CE has more number of contacts of RE, CE has only a small number of advantages over RE. In addition, the simulation and measurement results also show that the on-chip solar cells with different sizes of concentric ring surface electrodes have only subtle differences in their conductivity.

Surface electrode optimization

Figure 4a shows the structure of a conventional triple-well on-chip solar cell, which consists of three doped regions with different concentrations and depths (N+, PW, DNW). Deep n-Well (DNW) is located in the P-Substrate (P-sub). P-well (PW) is located in DNW, and diffusion (N+) is located in PW.

Typically, PW is connected to P-sub as the ground of the solar cell, and DNW is shorted with N+ as the output terminal of the solar cell [26]. The photoelectric conversion efficiency can be improved by segmenting on-chip solar cells' large-doped regions into numerous small doped sub-cells, because this provides larger vertical PN junction depletion region [27-29]. For segmented on-chip solar cells, each sub-cell necessitates surface electrodes for photocurrent extraction and hence, the segmentation design increases electrodes extensively.

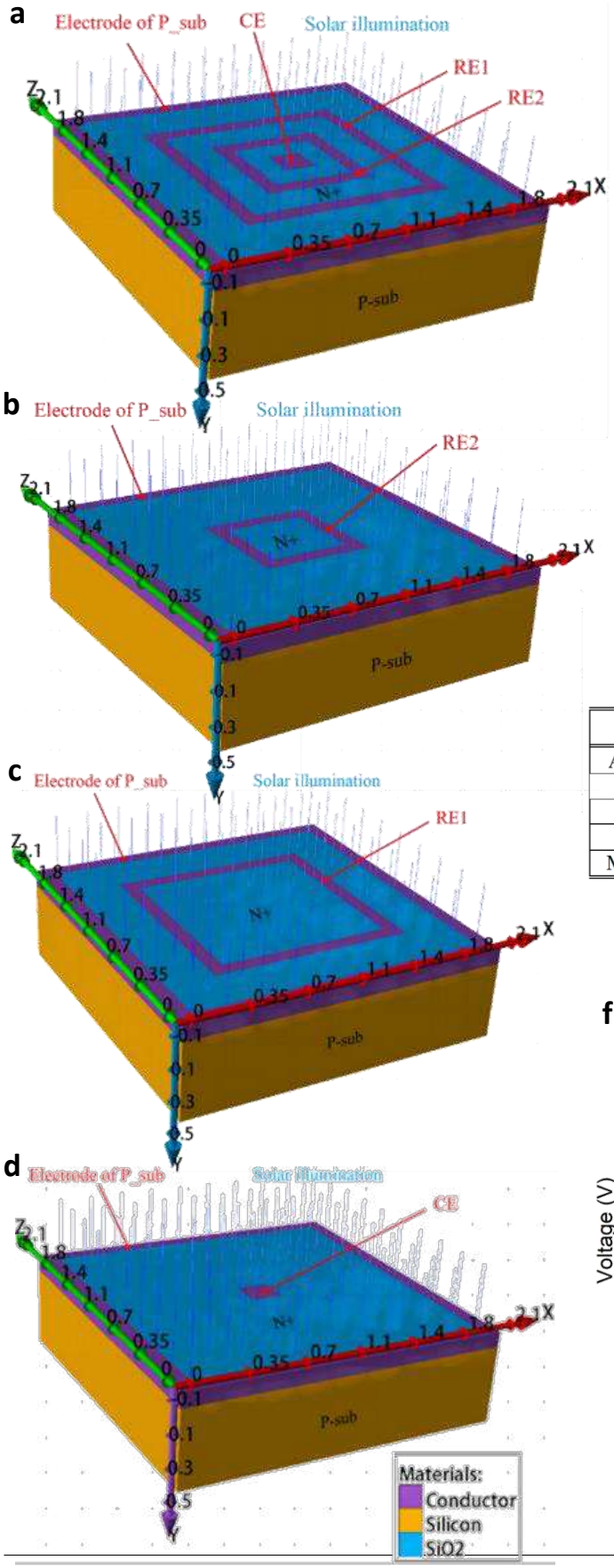
Based on (15), it is known that there is an optimal solution for the segmentation method of solar cells [11], where l0 represents the side length of the small doped area unit after segmentation, a/b is the ratio of the transverse light sensitivity coefficient to the longitudinal light sensitivity coefficient, d0 represents the spacing of the small doped area unit after segmentation, and S0 represents the shadow area of the surface electrode. Therefore, according to (15), under other unchanged conditions, the smaller the value of S0, the smaller the calculated value of l0, which means more small doped area units are generated, resulting in more vertical edge light-sensitive PN junctions, and thus enhancing the photoelectric conversion capability of the on-chip solar cells.

$$l_0 = (1 + \frac{a}{b} \cdot \frac{S_0}{2}) / (\frac{1}{d_0} - \frac{a}{2b}) \tag{15}$$

Clearly, the large shadowing of RE inhibits the on-chip solar cell from being fully divided, while the small shadowing CE enables deeper segmentation of the on-chip solar cell for stronger photoelectric conversion capability.

A deeply segmented triple-well on-chip solar cell using the CE with a significantly reduced light-blocking rate is designed, as shown in Figure 4c. However, during the design process, a problem is encountered. The deep segmentation of the triple-well on-chip solar cell results in numerous sub-cells. The electrodes of similar type of sub-cells need to be connected and led out through metal wires. Although the CE can reduce the metal coverage area, the high density of sub-cell interconnections would increase the light-blocking rate of the on-chip solar cell. This leads to a substantial metal coverage on the

deeply segmented triple-well on-chip solar cell, thereby hindering the CE



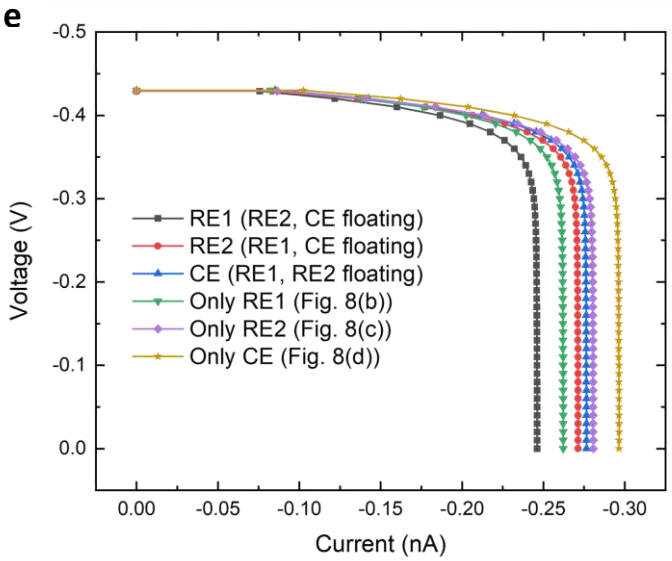


TABLE II
SUMMARY OF KEY PARAMETERS FROM FIG. 9

	RE1*	RE2*	CE*	RE1#	RE2#	CE#
Area of device	2.1μm × 2.1μm					
Illumination	The solar spectrum					
V_{oc} (V)	-0.43	-0.43	-0.43	-0.43	-0.43	-0.43
I_{sc} (nA)	-0.25	-0.27	-0.28	-0.26	-0.28	-0.3
Max. P_{out} (pW)	83.65	92.35	94.32	89.55	95.49	101.7

* One of RE1, RE2, or CE acts as the N+ electrode, while the rest are left floating.
# One of RE1, RE2, or CE acts as the N+ electrode, while the rest were removed.

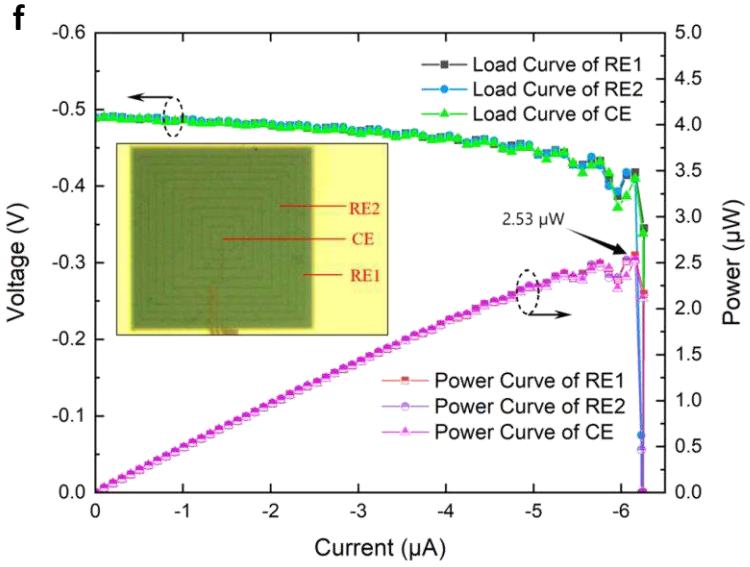


Fig. 3 | 3D Simulation Model of N+/P-Substrate Cell with Six Surface Electrode Conditions and Measurement Results. a, RE1, RE2, and CE individually act as the N+ connecting electrode, while keeping other electrodes floating. **b**, Only RE1 acts as the N+ connecting electrode. **c**, Only RE2 acts as the N+ connecting electrode. **d**, Only CE acts as the N+ connecting electrode. **e**, Simulated I-V characteristic curves for the solar cell with the six conditions of surface electrodes from Figure 2h. **f**, Measurement results of load curve of three types of surface electrodes and Micrographs of the on-chip solar cell with 0.1mm^2 in this case.

effective enhancement on its photovoltaic conversion capability.

To solve this problem, we have adopted highly doped regions as the interconnection for the sub-cells, replacing some of the metal electrodes. Among various doping options, N+ (P+) doping exhibits the highest conductivity. In the proposed deeply segmented triple-well on-chip solar cell, the N+ doped region is divided into four sections. One section employs a CE as

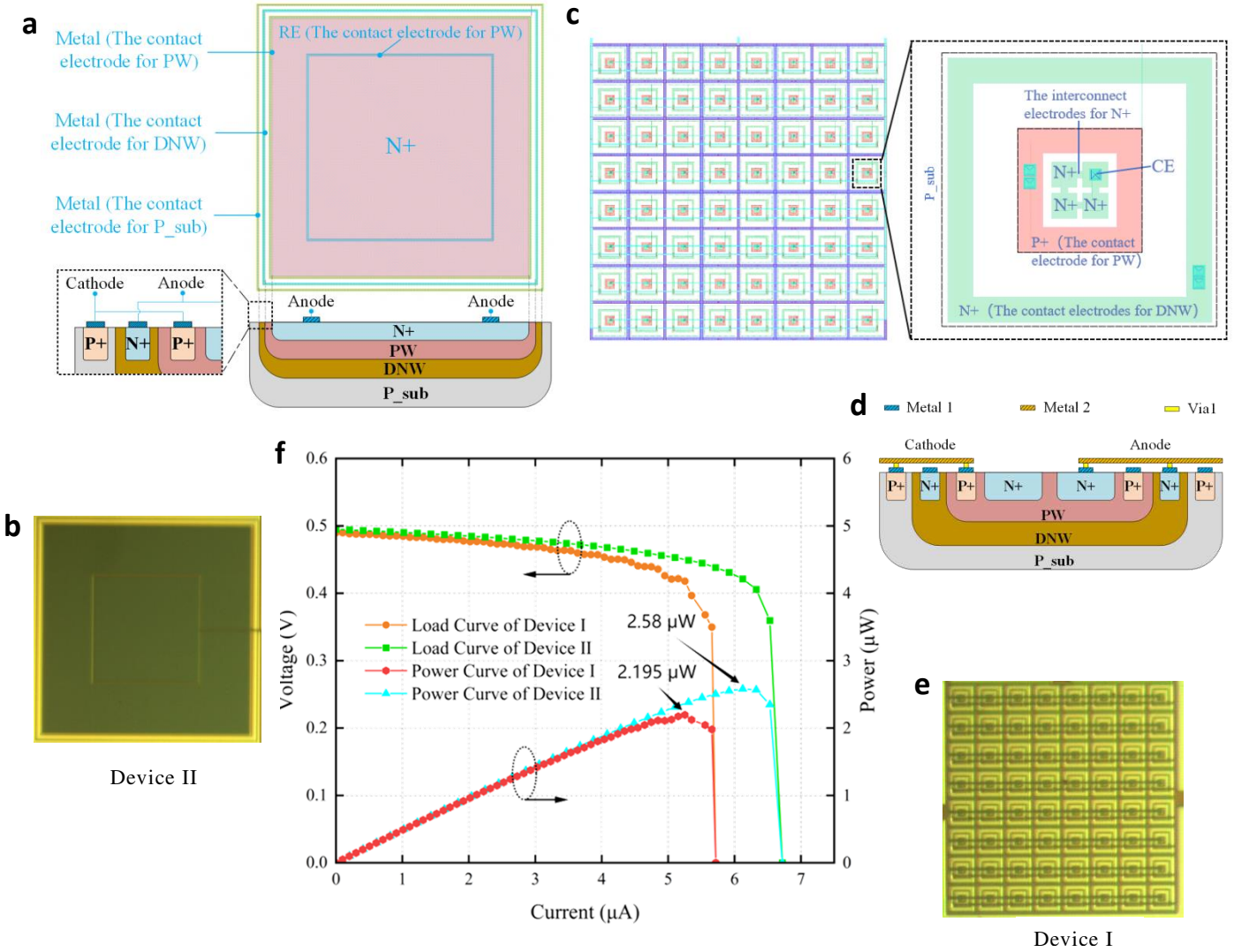


TABLE III
COMPARISON TABLE OF ON-CHIP SOLAR CELLS.

Reference	[18]	[20]	[28]	[29]	[30]	[31]	This work	
Process	0.18 μm Bulk CMOS	0.18 μm Bulk CMOS	0.18 μm Bulk CMOS	0.18 μm CMOS	0.25 μm CMOS	0.18μm Bulk CMOS	0.18 μm Bulk CMOS	
Technical Features	NW with p+ fingers	Backside-illuminated	Triple-well	Triple-well & photodiode stacked	Two photodiodes in series	IBC-PVs	Triple-well (Device I)	Triple-well Segmentation & metal optimization (Device II)
Light source	Green laser (532 nm)	Laser (980nm)	Halogen lamp	White LED	Laser (830 nm)	980 nm illumination	Xenon lamp	Xenon lamp
Incident light intensity	34.2 μW	5 mW	1.13 mW/mm^2	31 klux	3.87 μW/mm^2	1 mW	1 mW /mm^2	1 mW/mm^2
Footprint Area (mm^2)	0.000338	1.52	1.3+0.24	0.69* 1.38^	0.2+1.3	N/A	0.01	0.01
V_{oc} (V)	0.533	0.6	0.53	0.52*	N/A	N/A	0.49	0.495
I_{sc} (μA)	680	3826	750	17.5*	N/A	N/A	5.72	6.72
P_{out} (μW)	225	1668.9	322	7.14*	0.2	N/A	2.195	2.58
FF	0.62	0.73	0.81	0.78	N/A	N/A	0.78	0.78
Eff. (%)	24	33.37	21.9*	9.5*	3.5	20.33	21.95	25.79

*Single photodiode configuration only
^Two-photodiode stacked configuration

Fig. 4 | On-chip solar cell with surface electrode optimization. a, The horizontal and vertical cross-sectional views of a conventional triple-well on-chip solar cells. **b**, The micrograph of the conventional triple-well on-chip solar cell. **c**, The layout of the proposed deeply segmented triple-well on-chip solar cell with the CE and N+ as interconnection. **d**, The cross-sectional views of the proposed deeply-segmented triple-well solar cell sub-cells. **e**, The micrograph of the proposed deeply segmented triple-well on-chip solar cell. **f**, The measurement results of the load curve and power curve for the two 0.01mm^2 triple-well on-chip solar cells. Device I is conventional one and Device II is the proposed one.

the contact electrode, while the remaining three sections do not utilize metal as contact electrodes due to their small size. Instead, they are connected to the N+ doped region with the CE using N+ doping as the interconnection. Although N+ cannot compete with metals in terms of conductivity, the interconnected length of N+ is equal to the minimum distance of two adjacent N+ in the design rule and hence small enough, to significantly affect the performance. This ensures that the contact electrodes and interconnections formed by the highly doped N+ (P+) regions do not introduce excessive resistance. In other words, in the deeply segmented triple-well on-chip solar cell, the numerous sub-cells give rise to a significant number of contact electrodes and N+ interconnections. They are in parallel connection, leading to a total low resistance. As a result, the design of using highly doped regions as some metal interconnections ensures that the surface electrodes have a low light-blocking rate.

The proposed deeply segmented triple-well on-chip solar cell with the size of 0.01mm^2 is fabricated using a standard 0.18μm CMOS process, whose micrograph is shown in Figure 4e. The load curve and power curve of the on-chip solar cells are measured under vertical illumination using a 100k lux Xenon lamp. Figure 4f shows the measurement results. Device I represents a conventional unsegmented triple-well on-chip solar cell with 0.01mm^2 footprint area shown in Figure 4b. Device II refers to the proposed on-chip solar cell with optimized surface electrodes. The measurement results revealed the good performance of the proposed on-chip solar cell with optimized surface electrodes, particularly in terms of its photovoltaic conversion efficiency, which is 25.79%. It's worth noting that the calculation of the photoelectric conversion efficiency is based on the footprint area of the on-chip solar cell. The conventional unsegmented on-chip solar cell has the maximum conversion efficiency of 21.95%. This means the proposed work has 17.49% improvement compared to the conventional design. The comparisons with other works in the literature are summarized in Table III. Additionally, Device II, with a footprint area of 0.01mm², achieves a maximum output power of 2.58μW, as shown in Figure 4f. This value is comparable to the maximum output power of a single PN junction with a footprint area of 0.1mm², as shown in Figure 3f.

On-chip power source

To meet the 1V working voltage requirement of the application circuit, an energy harvesting system is implemented on the same chip as the on-chip solar cells. As illustrated in Fig. 5, this system mainly consists of a self-start module, a voltage conversion module, a monitoring and voltage stabilization module, and a voltage reference module. The self-start module is composed of a low-threshold ring oscillator and a conventional Dickson charge pump. The voltage conversion module includes a primary charge pump and a voltage-controlled oscillator (VCO).

When the illumination enables the anode port of the on-chip solar cell to generate a negative voltage with an absolute value larger than 0.22V, the start-up module converts and boosts the negative voltage at the anode port to a near 1V positive voltage, powering the VCO to make it start working. Driven by the clock signal output from the VCO, the primary charge pump starts operating, the Vout begins to rise and starts to output the power to the load. To avoid the wastage of power, the start-up module ceases operation. At this point, the start-up charge pump stops powering the VCO module, and the primary charge pump begins to power it instead. The voltage reference module uses a simple three-transistor structure to generate the reference voltage required by the system. The monitoring and voltage stabilization module employs the resistive voltage division topology for sampling and compares the sampled voltage with the reference voltage, which ensures the output voltage is maintained at 1V. When fluctuations occur in the load size or light source intensity, the monitoring and voltage stabilization module adjusts the feedback signal TA's voltage to regulate the oscillation frequency of the VCO, thereby ensuring that the energy extracted by the energy harvesting system from the on-chip solar cells is just enough to maintain the output voltage at 1V and support the power consumption required by the current load.

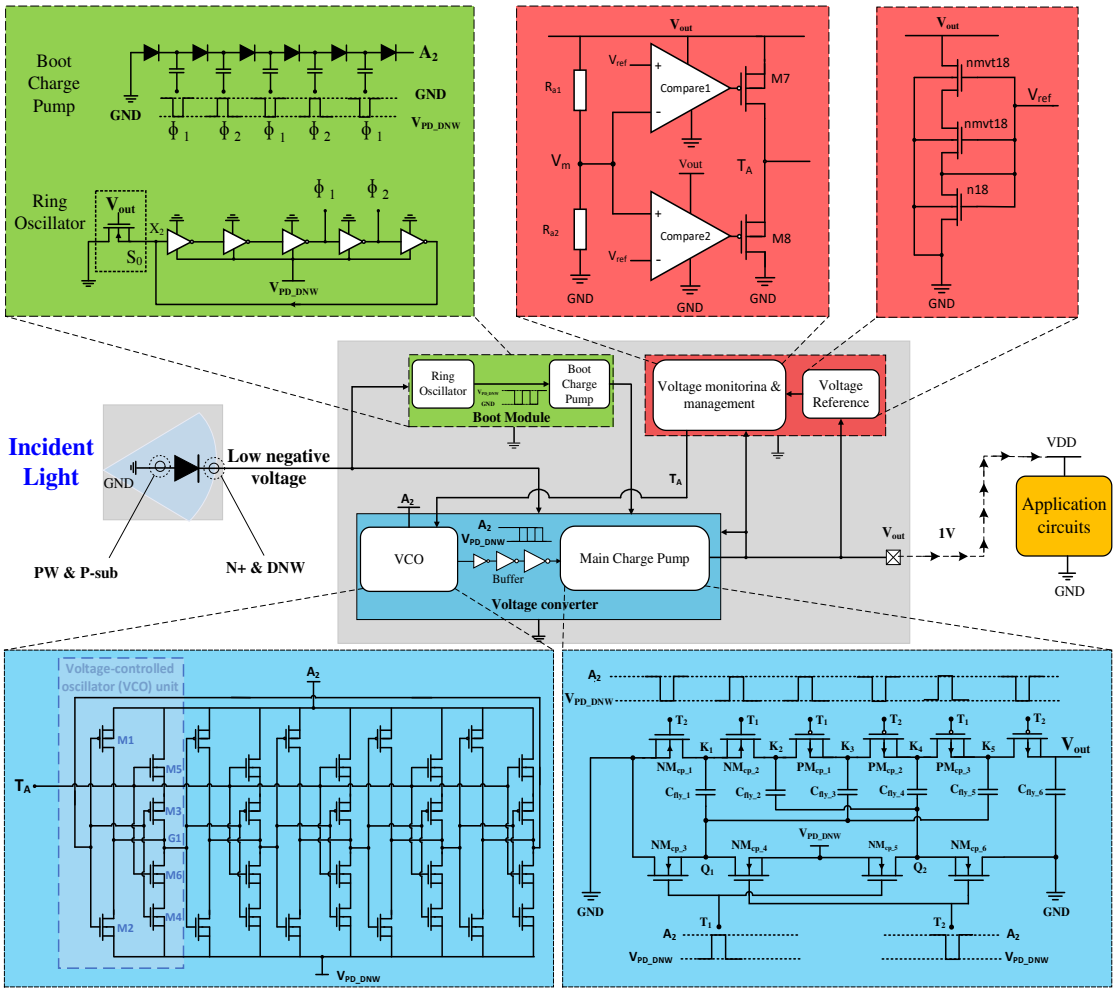


Fig. 5 | Conceptual diagram of on-chip solar cells and energy harvesting system forming an on-chip power source to power single-chip smart microsensors. The proportion of the on-chip power source is enlarged respect to others for illustration purpose.

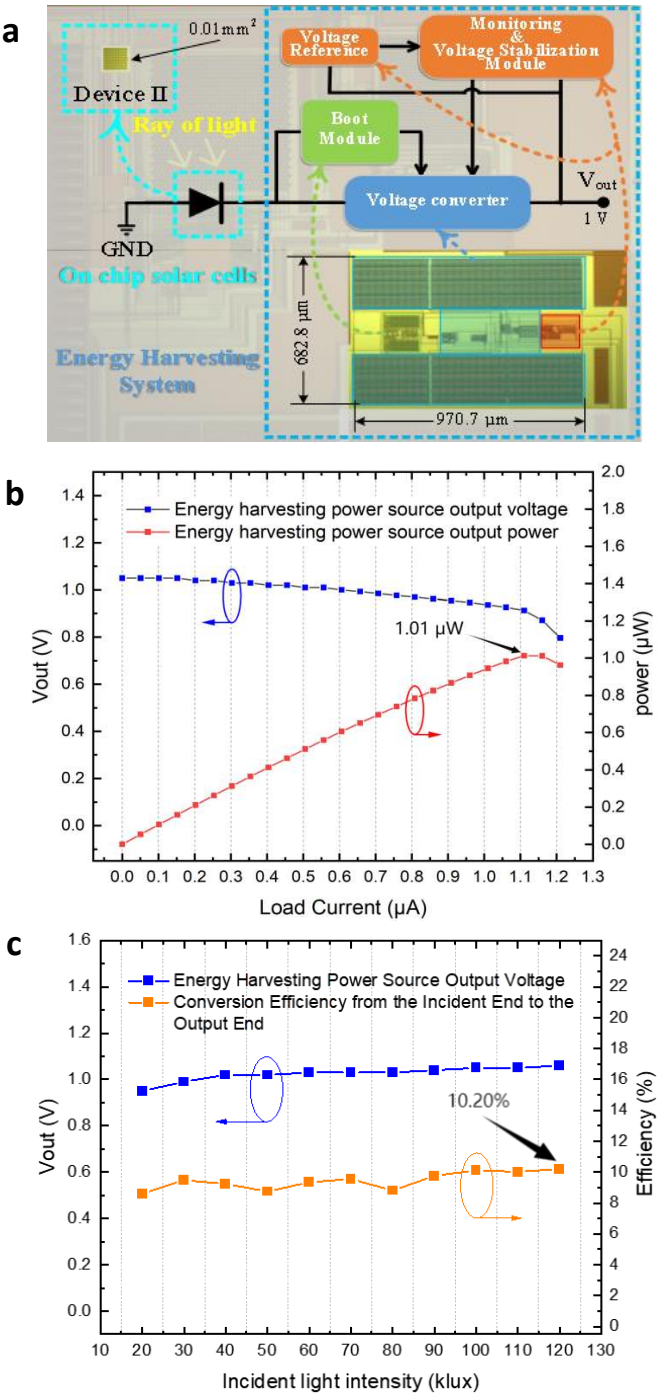


Fig. 6 | Manufacture and measurement of On-chip power source. a, Microscopic Photograph and Structural Schematic of the on-chip power source. **b**, The relationship between the output voltage and output power of the on-chip power source with the load size under 100kLux solar simulator illumination. **c**, The relationship between the output voltage of the on-chip power source and conversion efficiency with the light intensity.

Using a 0.18μm Bulk CMOS process, the on-chip power source comprising the energy harvesting system and the on-chip solar cells was fabricated, with its microphotograph shown in Figure 6a. Under illuminations from a solar simulator, the on-chip power source is tested and the measurement results demonstrated that the energy harvesting system effectively converts the low negative voltage from Device II to a 1V voltage. Figure 6b presents the relationship between the output voltage and output power of the on-chip power source with the load size. The measurement results show that under the illumination of a 100kLux by the solar simulator, the output voltage of the on-chip power source is maintained between 1.05V and 0.91V as the load current changed from 0 to 1.11μA. In this case, the power source can provide a maximum of 1.01μW of output power to the application module of microsensors.

The relationship between the output voltage of the on-chip power source and the light intensity is shown in Figure 6c. The measurement results indicate that the output voltage of the power source range is from 1.06V to 0.96V under light intensities of 20kLux to 120kLux. It should be noted that increasing the footprint of the on-chip solar cells can make the on-chip power source work under lower illuminations. Figure 6c. also demonstrates the conversion efficiency from the incident light power to the output power of the on-chip power source under different light intensities, with an average conversion efficiency of around 9.45%, where the highest conversion efficiency reaches 10.20% at 120kLux. It is worth noting that in this work, Device II is only 0.01mm^2 as the on-chip solar cell in the on-chip power source. The footprint of the on-chip solar cell can be increased for higher power consumption requirement of the application module.

Conclusion

This paper built theoretical models of square ring electrode and center electrode for the on-chip solar cells first. Through theoretical analysis, simulation, and measurement, we have demonstrated that the conductive ability of the CE is almost comparable to that of the RE. Due to its extremely low shading rate and minimal metal-induced recombination rate, the CE exhibits more advantages over the RE as a surface electrode for on-chip solar cells. Then a 0.01mm^2 segmented triple-well on-chip solar cell is designed using the CE to optimize the surface electrodes. Moreover, the interconnections between the sub-cells employs heavily doped areas to replace certain metal surface electrodes. This approach ensured that the shading rate of the designed on-chip solar cell remained consistently low. The measurement results revealed that, by optimizing the surface electrodes of the segmented triple-well solar cell, its photovoltaic conversion efficiency reaches an impressive 25.79%. This means a 17.49% increase compared to the conventional unsegmented triple-well solar cell. These surface electrode optimization techniques demonstrate an effective improvement in the photovoltaic conversion efficiency of on-chip solar cells. An on-chip power source is implemented with the optimized solar cells and the proposed energy harvesting system. Measurement results demonstrate that this on-chip power source can output a voltage of 1V with a maximum conversion efficiency of 10.20% from incident solar power to voltage output power. It ensures relative stability of the output voltage respect to the changes of the illumination and load. The proposed on-chip power source would enable the realization of smart microsensors for IoE applications.

Methods

Fabrication

The on-chip solar cells and energy harvesting system are designed with the assistance of Virtuoso software and fabricated by a wafer foundry using a 0.18μm bulk CMOS process. To compare the effects of different surface metals on the performance of on-chip solar cells, 3D simulations of the on-chip solar cells are conducted using Silvaco TCAD simulation software, as shown in Fig. 3. Due to the confidentiality of the foundry's process parameters, the simulation parameters are estimated based on available data: the doping concentrations of N+ and P-sub are 10^19 n/cm³ and 2x10^15 n/cm³, respectively, with an N+ doping depth of 0.1 μm.

Illumination Environment

A simulated sunlight xenon lamp source from Beijing Princes Science and Technology Co., Ltd., model PL-X500D, capable of producing simulated sunlight with an intensity ranging from 20klux to 120klux, equipped with an AM1.5 filter.

Electrical Measurements

Electrical testing is conducted using Keysight Technologies' B2910BL model single-channel source meter.

References

[1] J. Liu, G. Faulkner, B. Choubey, S. Collins and D. C. O'Brien, "An Optical Transceiver Powered by On-Chip Solar Cells for IoT Smart Dusts With Optical Wireless Communications," in IEEE Internet of Things Journal, vol. 6, no. 2, pp. 3248-3256, April 2019, doi: 10.1109/JIOT.2018.2881424.

[2] Tarancón, A. Powering the IoT revolution with heat. Nat Electron 2, 270–271 (2019). https://doi.org/10.1038/s41928-019-0276-4.

[3] W. Qi, X. Xia, C. Mei, H. Wang and W. Li, "Survey on Energy Harvesting IoT Communication in the Future Network," 2022 International Conference on Information Processing and Network Provisioning (ICIPNP), Beijing, China, 2022, pp. 63-67, doi: 10.1109/ICIPNP57450.2022.00020.

[4] Álvarez-Carulla, A., Saiz-Vela, A., Puig-Vidal, M. et al. High-efficient energy harvesting architecture for self-powered thermal-monitoring wireless sensor node based on a single thermoelectric generator. Sci Rep 13, 1637 (2023). https://doi.org/10.1038/s41598-023-28378-6.

[5] de Cea, M., Atabaki, A.H. & Ram, R.J. Energy harvesting optical modulators with sub-attojoule per bit electrical energy consumption. Nat Commun 12, 2326 (2021). https://doi.org/10.1038/s41467-021-22460-1.

[6] K. Yang, Qing Dong, Wanyeong Jung, Yiqun Zhang, Myungjoon Choi, David Blaauw, Dennis Sylvester, "9.2 A 0.6nJ −0.22/+0.19°C inaccuracy temperature sensor using exponential subthreshold oscillation dependence," 2017 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2017, pp. 160-161, doi: 10.1109/ISSCC.2017.7870310.

[7] W. Arshad, R. Ramzan, A. Beg and N. Bastaki, "Comparison and design of VCOs for ultra-low power CMOS temperature sensors," 2015 International Conference on Communications, Signal Processing, and their Applications (ICCSPA'15), Sharjah, United Arab Emirates, 2015, pp. 1-4, doi: 10.1109/ICCSPA.2015.7081297.

[8] D. A. Kamakshi, A. Shrivastava and B. H. Calhoun, "A 23 nW CMOS ultra-low power temperature sensor operational from 0.2 V," In Proc. Of the 2015 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), Rohnert Park, CA, USA, 2015, pp. 1-3, doi: 10.1109/S3S.2015.7333498.

[9] W. Yang, H. Jiang, Z. Wang and W. Jia, "An Ultra-Low Power Temperature Sensor Based on Relaxation Oscillator in Standard CMOS," In Proc. Of 2018 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), Shenzhen, 2018, pp. 1-2, doi: 10.1109/EDSSC.2018.8487078.

[10] W. Yang, et al., "A 0.0014 mm^2 150 nW CMOS Temperature Sensor with Nonlinearity Characterization and Calibration for the -60 to +40 ° C Measurement Range." Sensors, vol. 19, no. 1777. Apr. 2019, doi:10.3390/s19081777.

[11] J. Guan, J. Liu, Z. Li, W. Mo, K. Sun and F. Yan, "A 10.16% Efficiency On-Chip Solar Cells with Analytical Model Based on a Standard Bulk CMOS Process for Self-Powered Microsensors," in IEEE Electron Device Letters, vol. 44, no. 10, pp. 1664-1667, Oct. 2023, doi: 10.1109/LED.2023.3309868.

[12] A. Dr ă gulinescu and A. -M. Claudia Dr ă gulinescu, "Solar Cell Types and Technologies with Applications in Energy Harvesting," 2020 IEEE 26th International Symposium for Design and Technology in Electronic Packaging (SIITME), Pitesti, Romania, 2020, pp. 323-326, doi: 10.1109/SIITME50350.2020.9292186.

[13] A. Schneider, L. Rubin and G. Rubin, "Solar Cell Efficiency Improvement by New Metallization Techniques - the Day4 Electrode Concept," 2006 IEEE 4th World Conference on Photovoltaic Energy Conference, Waikoloa, HI, USA, 2006, pp. 1095-1098, doi: 10.1109/WCPEC.2006.279333.

[14] Y. S. Khoo, T. M. Walsh and A. G. Aberle, "Optimizing the Front Electrode of Silicon-Wafer-Based Solar Cells and Modules," in IEEE Journal of Photovoltaics, vol. 3, no. 2, pp. 716-722, April 2013, doi: 10.1109/JPHOTOV.2013.2244161.

[15] Y. -J. Hung, H. -W. Su, C. -L. Chun, J. -F. Chen, C. -W. Huang and M. -S. Cai, "Enhanced Efficiency in Backside-Illuminated Deep-n-Well-Assisted CMOS Photovoltaic Devices," in IEEE Electron Device Letters, vol. 36, no. 11, pp. 1169-1171, Nov. 2015, doi: 10.1109/LED.2015.2476380.

[16] S. Fernández, A. F. Braña, J. Grandal, J. P. González, F. García and M. B. Gómez-Mancebo, "ITO-Based Selective Contacts for Silicon Solar Devices," 2018 Spanish Conference on Electron Devices (CDE), Salamanca, Spain, 2018, pp. 1-4, doi: 10.1109/CDE.2018.8596978.

[17] E. G. Fong, N. J. Guilar, T. J. Kleeburg, H. Pham, D. R. Yankelevich and R. Amirtharajah, "Integrated Energy-Harvesting Photodiodes With Diffractive Storage Capacitance," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 21, no. 3, pp. 486-497, March 2013, doi: 10.1109/TVLSI.2012.2189898.

[18] N. Guilar, A. Chen, T. Kleeburg and R. Amirtharajah, "Integrated Solar Energy Harvesting and Storage," ISLPED'06 Proceedings of the 2006 International Symposium on Low Power Electronics and Design, Tegernsee, Germany, 2006, pp. 20-24, doi: 10.1145/1165573.1165580.

[19] D. Zenibayashi, T. Sugiura and N. Nakano, "Performance improvements of on-chip solar cell for microsystem," 2017 International Symposium on Electronics and Smart Devices (ISESD), Yogyakarta, Indonesia, 2017, pp. 282-286, doi: 10.1109/ISESD.2017.8253349.

[20] Y. -J. Hung, H. -W. Su, C. -L. Chun, J. -F. Chen, C. -W. Huang and M. -S. Cai, "Enhanced Efficiency in Backside-Illuminated Deep-n-Well-Assisted CMOS Photovoltaic Devices," in IEEE Electron Device Letters, vol. 36, no. 11, pp. 1169-1171, Nov. 2015, doi: 10.1109/LED.2015.2476380.

[21] Y. -J. Hung, Meng-Syuan Cai，Jia-Fa Chen，Hsiu-Wei Su，Po-Chang Jen，Poki Chen，Chih-Cheng Shih，Ting-Chang Chang, "High-Voltage Backside-Illuminated CMOS Photovoltaic Module for Powering Implantable Temperature Sensors," in IEEE Journal of Photovoltaics, vol. 8, no. 1, pp. 342-347, Jan. 2018, doi: 10.1109/JPHOTOV.2017.2775440.

[22] T. Sugiura, H. Miura and N. Nakano, "Double-Ring Shaded-Contact Photovoltaic Cell Designed on Standard CMOS Process," in IEEE Electron Device Letters, vol. 44, no. 6, pp. 887-890, June 2023, doi: 10.1109/LED.2023.3265810.

[23] M. Fojtik et al., "A Millimeter-Scale Energy-Autonomous Sensor System With Stacked Battery and Solar Cells," in IEEE Journal of Solid-State Circuits, vol. 48, no. 3, pp. 801-813, March 2013, doi: 10.1109/JSSC.2012.2233352.

[24] H. Shao, X. Li, C. -Y. Tsui and W. -H. Ki, "A Novel Single-Inductor Dual-Input Dual-Output DC‑DC Converter With PWM Control for Solar Energy Harvesting System," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 8, pp. 1693-1704, Aug. 2014, doi: 10.1109/TVLSI.2013.2278785.

[25] D. Inns and D. Poplavskyy, "Measurement of metal induced recombination in solar cells," 2015 IEEE 42nd Photovoltaic Specialist Conference (PVSC), New Orleans, LA, USA, 2015, pp. 1-4, doi: 10.1109/PVSC.2015.7356056.

[26] F. Horiguchi, "Integration of Series-Connected On-Chip Solar Battery in a Triple-Well CMOS LSI," in IEEE Transactions on Electron Devices, vol. 59, no. 6, pp. 1580-1584, June 2012, doi: 10.1109/TED.2012.2189116.

[27] S. Ghosh, W. D. Leon-Salas and J. Wrobel, "A fractal-based photodiode for on-chip energy harvesting," SENSORS, 2010 IEEE, Waikoloa, HI, USA, 2010, pp. 1169-1172, doi: 10.1109/ICSENS.2010.5690657.

[28] D. Zenibayashi, T. Sugiura and N. Nakano, "Performance improvements of on-chip solar cell for microsystem," 2017 International Symposium on Electronics and Smart Devices (ISESD), Yogyakarta, Indonesia, 2017, pp. 282-286, doi: 10.1109/ISESD.2017.8253349.

[29] Z. Chen, M. -K. Law, P. -I. Mak and R. P. Martins, "A Single-Chip Solar Energy Harvesting IC Using Integrated Photodiodes for Biomedical Implant Applications," in IEEE Transactions on Biomedical Circuits and Systems, vol. 11, no. 1, pp. 44-53, Feb. 2017, doi: 10.1109/TBCAS.2016.2553152.

[30] J. J. Liu, G. E. Faulkner, B. Choubey, J. Liu, R. Q. Chen, D. C. O'Brien and S. Collins, "Optically powered energy source in a standard CMOS process for integration in smart dust applications", IEEE Journal of Electron Devices Society, vol.

[31] Y. -J. Hung, J. -F. Chen and C. -L. Chun, "Improved Performance in Mirror-Assisted Back-Contact CMOS Photovoltaic Devices," in IEEE Electron Device Letters, vol. 36, no. 5, pp. 478-480, May 2015, doi: 10.1109/LED.2015.2411152