A Second-Order Charge Pump Noise-Shaping SAR ADC

Haoning Sun, Yuchen Wang, Wenji Mo, Kangkang Sun and Jingjing Liu*

Sun Yat-Sen University, Shenzhen, China

* sunhn3@mail2.sysu.edu.cn, liujj77@mail.sysu.edu.cn

2024 IEEE 17th International Conference on Solid-State & Integrated Circuit Technology (ICSICT) | 979-8-3503-6183-4/24/$31.00 ©2024 IEEE | DOI: 10.1109/ICSICT62049.2024.10831599

***Abstract*—In this paper, a low-power, high-precision passive charge pump noise-shaping (NS) successive approximation register (SAR) analog-to-digital converter (ADC) is proposed for ultrasonic sensor applications in the Internet of Things (IoT). A residual voltage integration technique is introduced to realize a second-order noise transfer function (NTF), thereby achieving a trade-off between the power consumption and accuracy. To address the charge loss issue during the noise-shaping integration process, a charge pump (CP) voltage-multiplying principle is employed, which compensates for the charge loss to a certain extent. The proposed NS SAR ADC is implemented using a standard 180-nm CMOS process. Simulation results demonstrate that the circuit consumes 90.4μW under a 1.2V supply voltage at a sampling rate of 10MS/s. The proposed second-order NS SAR ADC achieves a signal-to-noise and distortion ratio (SNDR) of 87.55dB, an effective number of bits (ENOB) of 14.25bits, a Schreier figure of merit (FoMs) of 178dB.**

Keywords—Analog-to-digital converter, charge pump, noise-shaping, successive approximation register, three-input-pair comparator

I. Introduction

The next-generation Internet of Things (IoT) has become the dominant trend in the future development of the electronics industry [1]. As a critical component, ADC determines the core competitiveness of the entire system. In the IoT application domain, various sensor devices have a strong demand for low-power, high-precision ADCs. With the continuous advancement of technology, the system requirements for ADC accuracy are constantly increasing [2]. Ultrasonic sensors have extensive applications in the IoT, enabling detection and measurement using ultrasound, and they normally require low-power, high-precision (12-14 bits) ADCs [3].

NS SAR ADC is one of the most promising hybrid ADC architectures. Similar to the SAR ADC, it features low power and low cost, while its high signal-to-noise ratio is comparable to that of the Δ-Σ ADC. The first modern NS SAR ADC is implemented using a cascaded integrator feed-forward (CIFF) structure [4]. A loop filter is used and consumes relatively high power. The ADC has limited accuracy due to first-order noise-shaping. Liu incorporates a dynamic amplifier into the NS SAR ADC architecture [5]. It achieves an improved first-order noise-shaping performance. However, the power consumption remains relatively high due to the additional circuitry introduced by the dynamic amplifier and the associated filtering components. Chen employes a capacitor-based charge pump voltage doubler to compensate for the voltage loss during the residue voltage integration process [6]. This design achieves second-order noise-shaping, but only the second-order integration process is compensated. Consequently, the noise shaping performance has a potential for further improvement.

This paper presents a low-power, high-accuracy noise-shaping SAR ADC suitable for ultrasonic sensors in IoT applications. The objective is to enhance the accuracy and reduce power consumption while achieving more efficient noise shaping with a lower raw bit count. This work employs a passive NS technique using residue voltage integration and utilizes a three-input-pair comparator to sum the input voltage and the NS integration voltage. Furthermore, this work leverages the capacitive charge pump voltage-multiplying principle to compensate for the voltage loss during the NS integration process, thereby enhancing the NS performance and improving the accuracy of ADC. By eliminating the need of additional active amplifiers and relying solely on switched-capacitor circuits to implement the noise-shaping functionality, the ADC's power consumption is reduced. The structure of this paper is as follows. Section II presents the proposed NS SAR ADC architecture and its operating principles. The ADC simulation results are provided in Section III. Finally, Section IV concludes the paper.

II. The Proposed CP NS SAR ADC Design

A. Voltage-multiplying charge pump

The voltage-multiplying charge pump can achieve the effect of multiplying the input voltage through periodic charging and discharging processes. As illustrated in Fig. 1, the operating principle of a voltage-multiplying charge pump is demonstrated. The four capacitors, possessing identical capacitance values, are configured with their upper plates connected to *V* and their lower plates grounded.

When the charge pump is in the voltage acquisition stage, the four capacitors form a parallel connection through switch switching, as shown in Fig. 1(a). After charging to a voltage equal to *V* across the four capacitors, the charge pump is ready to enter the voltage-multiplying stage. When the charge pump is in the voltage-multiplying stage, the four capacitors are switched to series connection, as shown in Fig. 1 (b). The

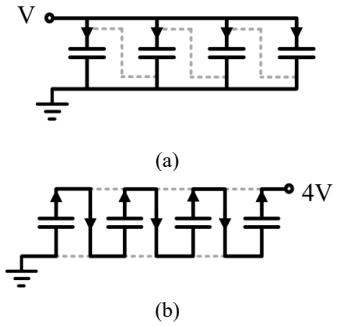

Fig. 1 Voltage-multiplying charge pump working principle, (a) voltage acquisition mode, (b) voltage-multiplying mode.

This work is supported by National Natural Science Foundation of China with project number 62174181.

lower plate of the end capacitor is grounded, and the upper plate of each capacitor is sequentially connected to the lower plate of the next level capacitor. The upper plate of the last capacitor serves as the output terminal. Due to the fact that each capacitor is charged to V during the acquisition mode, when the lower plate of the higher-level capacitor is connected to the upper plate of the lower-level capacitor, this lower plate potential will be raised. And each level of capacitor potential is raised by V. From this, it can be seen that the voltage-multiplying charge pump composed of four capacitors can approximately obtain four times the voltage at the output end. Therefore, this voltage-multiplying charge pump can amplify the input voltage by approximate four times.

B. Second-order CP NS SAR ADC

Fig. 2. illustrates the structure of the designed passive second-order CP NS SAR ADC. For simplicity, the diagram shows the single-ended positive input section of the NS SAR ADC, though the actual design is differential. The structural details of second-order CP NS circuit and the timing diagrams of control signals are depicted in Fig. 3, where C_{res}=C_{DAC} =2C_{int1}=4C_{int2}. The C_{DAC} is the total capacitance of CDAC. CLK_S denotes the ADC sampling clock and CLK_C represents the control clock for the ADC comparator. Φ_{res} controls the integration capacitor C_{res} to sample the residual voltage V_{res}. Φ_1 controls the charge sharing between C_{res} and C_{int1}. Φ_2 controls the charge sharing between C_{res} and C_{int2}. Φ_{CP1} controls the first-stage integration voltage V_{int1} amplification via the charge pump configuration with C_{int1}. Φ_{CP2} controls the second-stage integration voltage V_{int2} amplification via the charge pump configuration with C_{int2}. Φ_{rst} controls the reset operation of the C_{res} voltage.

During one sampling period, the ADC undergoes three phases, including the sampling and second-order NS phase, comparison phase and residue V_{res} collection phase. In the sampling and second-order NS phase, the signal is sampled and sent to the comparator for comparison, and the NS structure performs the integration operation. During the comparison phase, the comparator outputs the comparison result to the SAR logic, which controls the DAC capacitor array C_{DAC} to switch the top plate voltage levels. This process performs a successive approximation and outputs a digital code, completing the quantization task. After the comparison phase, the residual voltage V_{res} on the top plate of the capacitor array is sampled onto capacitor C_{res} via switch Φ_{res}. Due to the voltage loss from charge sharing, the voltage collected on C_{res} is approximately $0.5V_{res}$, which is used as the integration voltage for noise shaping in the subsequent sampling cycle.

At the beginning of the next sampling cycle, Φ_1 is high, while Φ_{CP1} maintains low. At this moment, the two capacitors

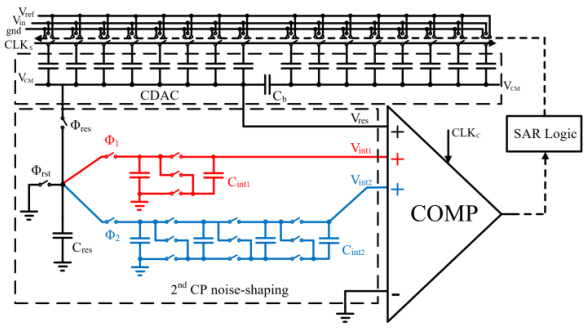

Fig. 2 The architecture of the proposed second-order CP NS SAR ADC.

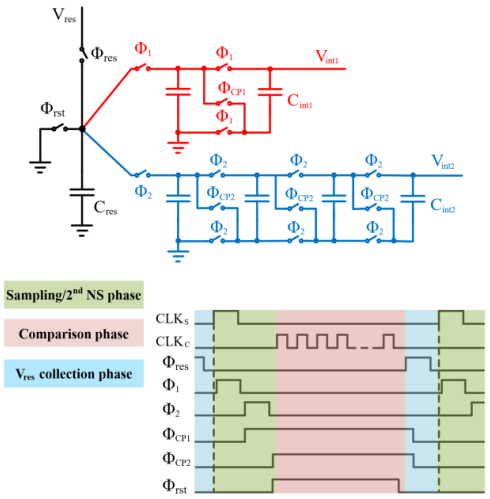

Fig. 3 The architecture of the proposed second-order CP NS circuit and the timing diagrams of control signals.

C_{int1} are connected in parallel, resulting in a total capacitance value of 2C_{int1}. According to the principle of charge conservation, the following can be obtained:

$$0.5V_{res}(z)C_{res}+2V_{int\,1}(z)C_{int\,1}z^{-1}=V_{int\,1}(z)(C_{res}+2C_{int\,1}) \quad (1)$$

Subsequently, Φ_1 switches to low, and the voltage on C_{res} is V_{int1}. Φ_2 is switched to high, while Φ_{CP2} remains low. At this moment, the four capacitors C_{int2} are connected in parallel, resulting in a total capacitance value of 4C_{int2}. According to the principle of charge conservation, (2) can be obtained:

$$V_{int\,1}(z)C_{res}+4V_{int\,2}(z)C_{int\,2}z^{-1}=V_{int\,2}(z)(C_{res}+4C_{int\,2}) \quad (2)$$

Simultaneously, after Φ_1 is at a low level, Φ_{CP1} is at a high level, transitioning C_{int1} capacitors from the integration phase to the amplification phase. At this point, the two capacitors are connected in series, providing the first-order integration voltage $V'_{int\,1}$ = 2 $V_{int\,1}$ to the three-input-pair comparator. Similarly, after Φ_2 is at a low level and Φ_{CP2} is at a high level, transitioning C_{int2} capacitors from the integration phase to the amplification phase. The four capacitors are also connected in series, providing the second-order integration voltage $V'_{int\,2}$ =4 $V_{int\,2}$ to the three-input-pair comparator. Additionally, after Φ_2 is at a low level, Φ_{rst} is at a high level, performing the reset operation on capacitor C_{res}, which means clearing the voltage on C_{res}.

During the comparison phase, the comparator sums and compares the residual voltage V_{res}, first-order integration voltage $V'_{int\,1}$ and second-order integration voltage $V'_{int\,2}$, thereby achieving the second-order noise shaping . Due to the quantization noise Q introduced during the comparator quantization phase, the ADC output D_{out} can be expressed as follows:

$$D_{out}(z)=V'_{int\,1}(z)+V'_{int\,2}(z)+V_{in}(z)+Q(z) \quad (3)$$

Based on (1), (2) and (3), the following relationship can be derived:

$$D_{out}(z)=V_{in}(z)+(1-0.5z^{-1})^2Q(z) \quad (4)$$

It can be observed that this CP NS SAR ADC achieves a second-order noise-shaping function. The NTF is given by

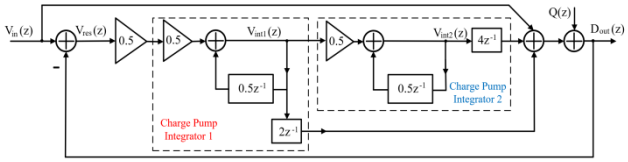

Fig. 4 The signal flow diagram of the proposed CP NS SAR ADC.

$(1-0.5z^{-1})^2$. Fig. 4 shows the signal flow diagram of the proposed CP NS SAR ADC.

III. Simulation Results and Discussion

The proposed second-order CP NS SAR ADC is implemented using a standard 180nm CMOS process. This ADC consumes 90.4μW at a supply voltage of 1.2V. The power consumption breakdown of each block is illustrated in Fig. 5. The spectral density of the proposed ADC is shown in Fig. 6. When the input signal is a sine signal of 38kHz and the sampling rate of ADC is 10MS/s, the output spectrum density shows that SNDR is 87.55dB, corresponding to an ENOB of 14.25bit. The performance comparison with previous noise-shaping ADCs is given in Table I. It can be observed that the proposed CP NS SAR ADC circuit achieves a high precision within an appropriate bandwidth. The obtained SNDR of 87.55dB outperforms other ADCs in the table except [7]. It employs active amplifiers to achieve fourth-order noise shaping in a 28nm process, resulting in high precision but also significant power consumption. The FoM_s

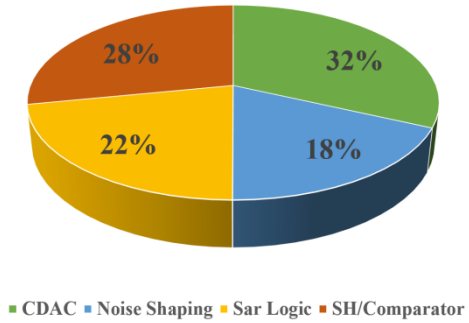

Fig. 5 The power consumption breakdown for each ADC block.

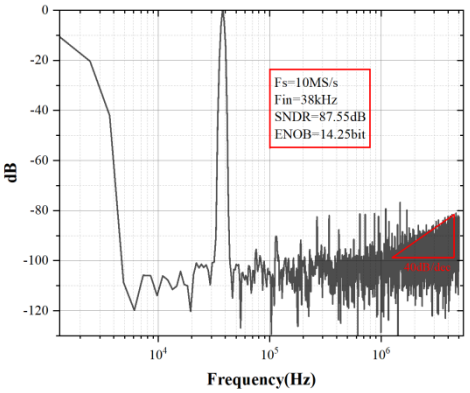

Fig. 6. Simulated spectral density of the proposed ADC for a 38kHz input signal sampled at 10MS/s.

TABLE I. Performance Summary and Comparison

Specifications	[2]	[5]	[6]	[7]	This work
Technology (nm)	65	40	65	28	**180**
Supply (V)	0.8	1.1	1	1	**1.2**
Sampling rate (S/s)	128k	8.4M	64M	2M	**10M**
Bandwidth (kHz)	4	262	8000	100	**100**
Original bit	14	8	8	8	**8**
SNDR(dB)	79.1	80	65	87.6	**87.55**
ENOB(bit)	12.8	13	10.5	14.3	**14.25**
Power(μW)	1.37	143	252.9	120	**90.4**
FoM_s(dB)	173.8	173	169.9	177	**178**

of the proposed CP NS SAR ADC is the best in the table. This indicates that the proposed CP NS SAR ADC achieves a better trade-off among precision, speed, and power consumption.

IV. Conclusion

This paper proposes a second-order CP NS SAR ADC. By using an 8-bit V_{CM}-based SAR ADC, a 14.25-bit ADC suitable for ultrasonic sensors is realized. To achieve high energy efficiency, this work employs a passive NS technique using residue voltage integration and utilizes a three-input-pair comparator to sum the input voltage and the NS integration voltages. The capacitive charge pump voltage-multiplying principle is used to compensate the voltage loss during the NS integration process, thereby enhancing the NS performance and improving the accuracy of the ADC. The FoM_s of the proposed second-order NS SAR ADC is 178dB. It consumes 90.4μW from a 1.2V supply at 10MS/s. The SNDR is 87.55dB, corresponding to an ENOB of 14.25bit. Simulation results demonstrate that the proposed NS SAR ADC achieves a favorable trade-off between conversion accuracy and power consumption.

References

[1] Y. Zhang and J. Zhang, "A 20 MHz Bandwidth 79 dB SNDR SAR-Assisted Noise-Shaping Pipeline ADC With Gain and Offset Calibrations," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 3, pp. 745-756, Mar. 2022.

[2] P. Harpe and E. Cantatore, "An oversampled 12/14b SAR ADC with noise reduction and linearity enhancements achieving up to 79.1dB SNDR," in *IEEE International Solid-State Circuits Conference (ISSCC)*, Mar. 2014, pp. 194-195.

[3] D. Chen and X. Cui, "A Survey on Analog-to-Digital Converter Integrated Circuits for Miniaturized High Resolution Ultrasonic Imaging System," *Micromachines*, vol. 13, no. 1:114, Jan. 2022.

[4] J. A. Fredenburg and M. P. Flynn, "A 90-MS/s 11-MHz-bandwidth 62-dB SNDR noise-shaping SAR ADC," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2898-2904, Dec. 2012.

[5] C. Liu and M. Huang, "A 0.46mW 5MHz-BW 79.7dB-SNDR noise-shaping SAR ADC with dynamic-amplifier-based FIR-IIR filter," in *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2017, pp. 466-467.

[6] Z. Chen, M. Miyahara, and A. Matsuzawa, "A 2nd order fully-passive noise-shaping SAR ADC with embedded passive gain," in *IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Nov. 2016, pp. 309-312.

[7] Y. Shu and L. Kuo, "An Oversampling SAR ADC With DAC Mismatch Error Shaping Achieving 105 dB SFDR and 101 dB SNDR Over 1 kHz BW in 55 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 2928-2940, Dec. 2016.