A 9.68nW 57.51dB SNDR SAR ADC with Dual Bypass Windows Based on Non-binary Split Capacitors for Biomedical Applications

Kangkang Sun, Jingjing Liu, Member, IEEE, Feng Yan, Haoning Sun, Yafei Zhang, Yuan Ren, Linfei Huang, Yao Pi, Wanqing Wu, Jian Guan

***Abstract*—The paper proposes a low-power Successive Approximation Register (SAR) Analog-to-Digital Conversion (ADC) with dual bypass windows based on non-binary split capacitors. To reduce the power consumption, the bypass windows constituted by the split capacitors can maximize the coverage of biological signals both in the resting state and excited state. When the signal falls within the designated window, unnecessary conversion cycles are skipped. This process is mainly judged and controlled by digital circuits, which is highly robust and does not require calibration. Meanwhile, a low-power dynamic CMOS comparator is proposed, which can effectively reduce the voltage variation of the latch node during the comparator's operation, further reducing power consumption. The proposed SAR ADC, based on a 180nm process, measures a power consumption of 9.68nW at a supply voltage of 0.6V and a sampling rate of 5.21kS/s. The signal-to-noise-and-distortion ratio (SNDR) and the spur-free dynamic range (SFDR) are measured at 57.51dB and 71.68dB, respectively. It also achieves an effective number of bits (ENOB) of 9.26 bits and a Walden figure-of-merit (FoM) of 2.9 fJ/conv.-step. The proposed SAR ADC is also verified by collected electromyogram (EMG), electrocardiogram (ECG), and electroencephalogram (EEG) signals. The average power consumption for quantifying EMG signals is 7.95 nW, providing an attractive solution for low-power SAR ADCs in biomedical applications.**

***Index Terms*—SAR ADC, Capacitor Splitting, Bypass Window, Non-binary Quantization, Dynamic CMOS Comparator, EMG, ECG, EEG.**

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I. Introduction

ADVANCED human biomedical signal acquisition systems should be capable of sustained monitoring, user-friendly, and characterized by compactness, lightness, and wireless connectivity to ensure the subject has full mobility. Consequently, low-power design is critical for portable and wearable medical devices that require extended, continuous monitoring, which is one of their core requirements [1]-[6]. Biomedical signals such as EMG, ECG, and EEG often have low-frequency and low-amplitude characteristics [7], [8], requiring precise ADC to ensure accurate signal quantification. To fulfill this requirement, the SAR ADC is an ideal choice due to its low power consumption and moderate precision, especially suitable for wearable cardiac monitors, cranial EEG devices, electromyographic sensor systems, and other biomedical signal acquisition systems with strict power consumption constraints [9]-[15].

EMG is a technique for capturing bioelectrical signals generated by muscle activity, which can monitor muscle contractions. This technology is widely used in various fields such as medical care, rehabilitation, sports science, human-machine interaction, and virtual reality. In particular, surface EMG, which records signals in a non-invasive manner through electrodes on the skin surface, is especially common in muscle function recovery [16]-[18]. As shown in Fig. 1, in the electromyographic signal acquisition and processing systems for motion monitoring and rehabilitation training [19], the EMG acquisition system typically consists of electrodes, an analog front-end (AFE), an ADC, a microcontroller unit (MCU), a modulator, and a transmitter module [20]. In the acquisition system, if the ADC employs a V_{CM}-based SAR ADC, a full binary search process is necessary for each conversion cycle. Biomedical electrical signals undergo high-frequency, substantial change over short time and are in a relatively stable resting state for the majority of the time [21]-[23]. When handling these signals, the V_{CM}-based SAR ADC leads to redundant quantization steps, as depicted in the red section of the Fig.1 (c). Furthermore, the most of biomedical electrical signals are close to V_{CM} and the DAC quantization is focused around V_{CM}. This causes high power consumption and significantly impacts the energy efficiency of the ADC.

There are various methods to improve the quantization

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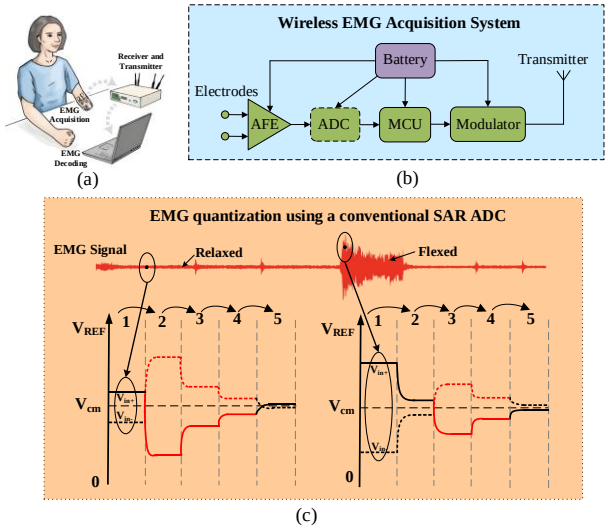


Fig. 1. (a) Illustration of EMG signal acquisition and processing system application. (b) The block diagram of wireless EMG signal acquisition system. (c) The EMG quantization using a conventional SAR ADC.

efficiency of SAR ADCs [24]-[26]. One such method, which is particularly effective for biomedical signals, involves the use of a bypass window technique that is tailored to the distribution characteristics of these signals, thereby reducing unnecessary quantization steps [27]. When the input signal falls within a predetermined window range, this technique skips the redundant comparison steps and DAC capacitor switching, which in turn reduces the quantization power consumption of the SAR ADC. Additionally, skipping certain steps can decrease the accumulation of non-ideal errors, enhancing the static performance of the ADC [28]. Since the amplitude of biomedical signals is often confined to a smaller dynamic range, the bypass window is especially effective during the quantization process of such signals.

A substantial amount of research has attempted to further enhance the efficiency of bypass windows [27], [29]-[32]. An external reference voltage with precision within the least significant bit (LSB) is proposed to define the window range and two comparators are employed to detect whether the signal falls within the window range [27]. Additionally, specialized calibration circuits are needed to address the impact of reference voltage precision and comparator offset voltage on the window boundaries. Wang has designed current correlators in the dynamic comparators, which can generate bypass trigger signals while producing conventional polarity outputs [29]. However, they are all affected by process-voltage-temperature (PVT) variations and require specialized window range calibration. Some works employ the output polarity of the comparator and the comparison time to ascertain the input voltage range, thereby achieving window detection [30]-[32]. However, this detection method requires the design of a dedicated timing detection circuit. These bypass window judgment methods in the analog domain primarily rely on specifically engineered analog circuits. This not only increases additional power consumption but also makes it difficult to mitigate the impact of PVT variations on the precision of the bypass window. Subsequent specialized calibration operations are also required.

To enhance the robustness of the bypass window range and judgment module, a DAC reuse (DACR) window scheme for generating window boundaries by switching the DAC capacitors has been proposed [33]. By reusing the DAC and comparators, the bypass window function can be achieved with only digital control logic and an additional window detection conversion cycle, eliminating the need for calibration and offering better robustness. Furthermore, since the window range is generated by a capacitor array and can be customized according to specific requirements, the DACR window scheme provides flexibility [34]. However, the DACR window scheme utilizes an extra comparator cycle that can only generate a single window boundary, resulting in a low bypass efficiency. And when the input signal is outside the bypass window, it would consume more power due to the additional window detection cycle and DAC switching operations. More importantly, most bypass window ranges are concentrated near the V_{CM}, which is friendly to the low-power quantization comparison when the voltage potential is mainly in a resting state. However, when biomedical signals are in an excited state for a long time, the potential increases, making it difficult for the bypass window to cover, and so it is hard to skip some steps in the quantization process.

This paper proposes a dual bypass window architecture based on non-binary capacitor splitting, aiming to meet the distribution characteristics of biomedical signals. The range of Bypass Window 1 (Win1) is [$3V_{REF}/8$, $5V_{REF}/8$], which is used to encompass the signals in the rest state. Bypass Window 2 (Win2) is [$V_{REF}/8$, $2V_{REF}/8$] & [$6V_{REF}/8$, $7V_{REF}/8$], capable of covering the majority of signals in the excited state with high probability. The Win1 and Win2 schemes achieve reduced quantization power consumption for biomedical signals in both resting and excited states, offering advantages over the conventional bypass window schemes that only cover the range near V_{CM}. The quantization process involves at most one additional comparison cycle, and there is no switching back of capacitor voltages. Compared to the schemes that use analog circuits for bypass window judgment, the bypass window judgment and control module in this work can be implemented with simple digital circuits, providing strong robustness and eliminating the need for additional calibration steps. Additionally, a low-power dynamic CMOS comparator is proposed for this architecture, which can reduce the voltage variation at the circuit nodes during the operation of the latch, thereby achieving a substantial reduction in the comparator's power consumption.

The rest of the paper is organized as follows. Section II introduces the architecture of the proposed SAR ADC. Section III provides a detailed description of the proposed bypass window switching scheme, including its details and implementation methods. Section IV details the specific implementation of the proposed comparator circuit and the logic circuit. Section V explains the measured performance of the ADC and verifies the power consumption for the quantification of biomedical signals. Performance summary and a comparison with the state-of-art works are also included in this section. Finally, Section VI concludes the paper.

II. The Architecture of the Proposed SAR ADC

In a 10-bit SAR ADC with top plate sampling, the unit

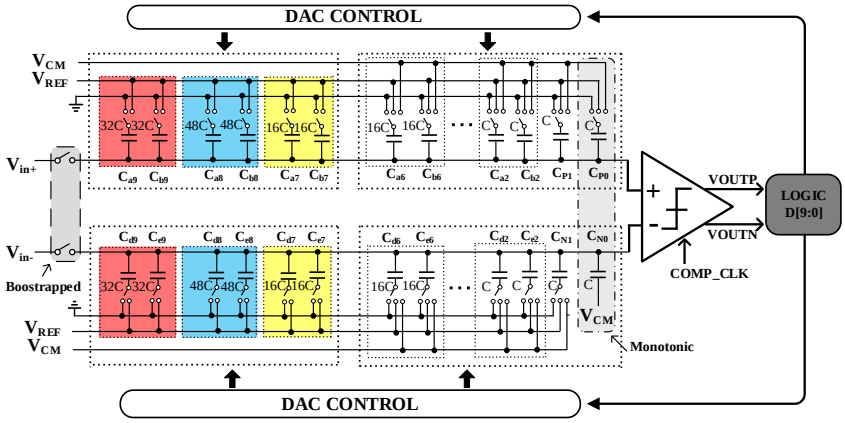


Fig. 2. The proposed SAR ADC architecture.

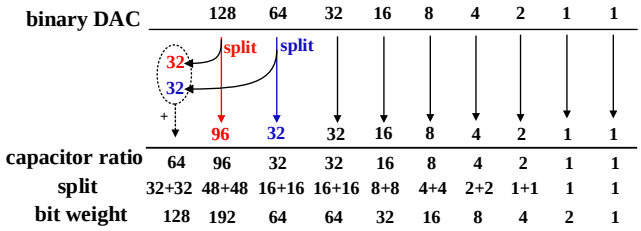


Fig. 3. The illustration of splitting method for the non-binary split capacitor array.

capacitor of the redundant bit is quantified as the LSB using a monotonic approach, and the MSB capacitor in the 10-bit DAC is reduced from 256C to 128C (where C denotes the unit capacitor), thus halving the total capacitance value of the DAC array.

Fig. 2 illustrates the architecture of the proposed 10-bit SAR ADC with a dual bypass window based on split capacitors. It comprises a bootstrap sample-and-hold switch, a differential non-binary split capacitor array, a dynamic comparator, and a logic module. The comparator employs a novel low-power CMOS dynamic latch architecture proposed in this paper. To minimize the power consumption, it operates in a sub-threshold conduction state.

In SAR ADCs, the bypass window can be realized through a split non-binary capacitor array [35][36]. For the proposed ADC, dual bypass windows are defined by the designed non-binary capacitor array, as shown in Fig. 3. In a 10-bit binary DAC array, the first two capacitors (128C and 64C) are divided into three capacitors, with 64C(32C+32C), 96C (128C-32C), and 32C (64C-32C) respectively. The 64C is placed in front of the original Most Significant Bit (MSB) capacitor. Then, the newly formed three capacitors (64C, 96C, 32C) can form two bypass windows of sizes 128 LSBs during the quantization process, namely Win1 and Win2. Concurrently, each capacitor is evenly divided into two equal halves to create a symmetrical common centroid layout in the DAC architecture.

III. The Proposed Bypass Window Switching Scheme

In this section, the working principles of the proposed SAR ADC are described in detail, including the voltage switching of split capacitors, timing diagram, non-binary encoding, and analysis of power consumption.

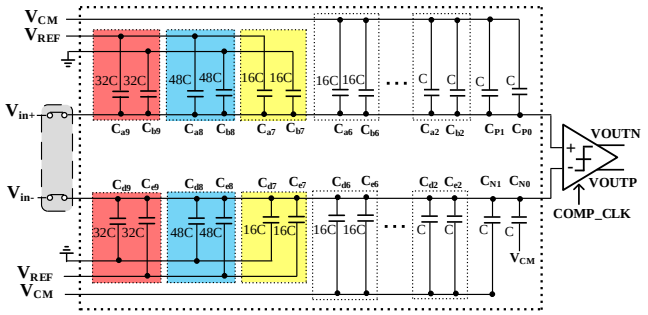


Fig. 4. The sampling process of splitting capacitor array.

A. Voltage Switching of Split Capacitors and Bypass Window

To reduce the quantization power consumption of the DAC capacitor array, this structure employs a V_{CM}-based sampling method for the top plates, as shown in Fig. 4. The input signal is connected to the top plates of the capacitor array, that is: $V_p = V_{in+}$, $V_n = V_{in-}$, where V_p and V_n are defined as the comparator non-inverting and inverting input terminals, respectively. Simultaneously, the bottom plates of C_{a9}, C_{a8}, C_{a7}, C_{e9}, C_{e8}, C_{e7} are tied to V_{REF}, the bottom plates of C_{b9}, C_{b8}, C_{b7}, C_{d9}, C_{d8}, C_{d7} are connected to GND, and the rest capacitor bottom plates are connected to V_{CM}.

The quantization process is divided into three stages: 1) Bypass Window Switching Operation; 2) V_{CM}-based Switching Operation; 3) Monotonic Switching Operation. The quantization timing diagram is shown in Fig. 5. First, compare the sampled voltages V_p and V_n directly. If $V_p > V_n$, D[9] = 1, connect the bottom plates of C_{a9} and C_{d9} to GND and V_{REF}, respectively. If $V_p < V_n$, D[9] = 0, connect the bottom plates of C_{b9} and C_{e9} to V_{REF} and GND, respectively. Then, perform the second voltage comparison. The capacitors "32C+32C, 48C+48C, 16C+16C" are split from "128C, 64C" in the traditional binary quantization array. In the conventional SAR logic, 128C and 64C correspond to quantization results D[8] and D[7]. After the proposed splitting, the capacitors "32C+32C, 48C+48C, 16C+16C" have weights that are no longer in a power-of-two form, and their quantization values are not strictly binary. They must be re-encoded. Designate the quantization results of "32C+32C, 48C+48C, 16C+16C" as M9, M8, and M7, respectively.

For simplicity, take $V_{in+} > V_{in-}$ as an example to describe the

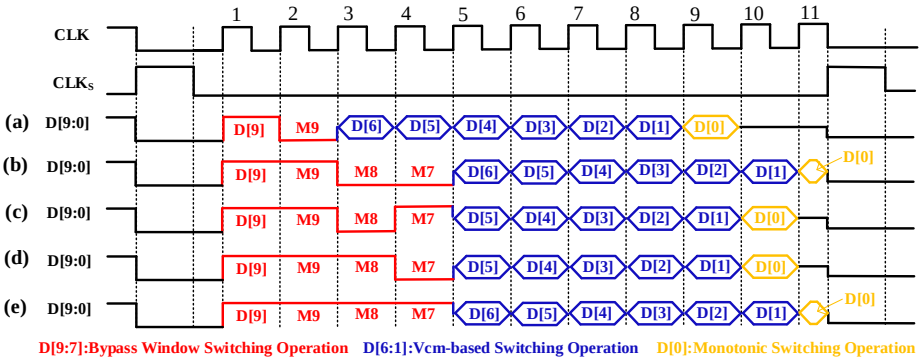


Fig. 5. The timing diagram of the proposed quantization process.

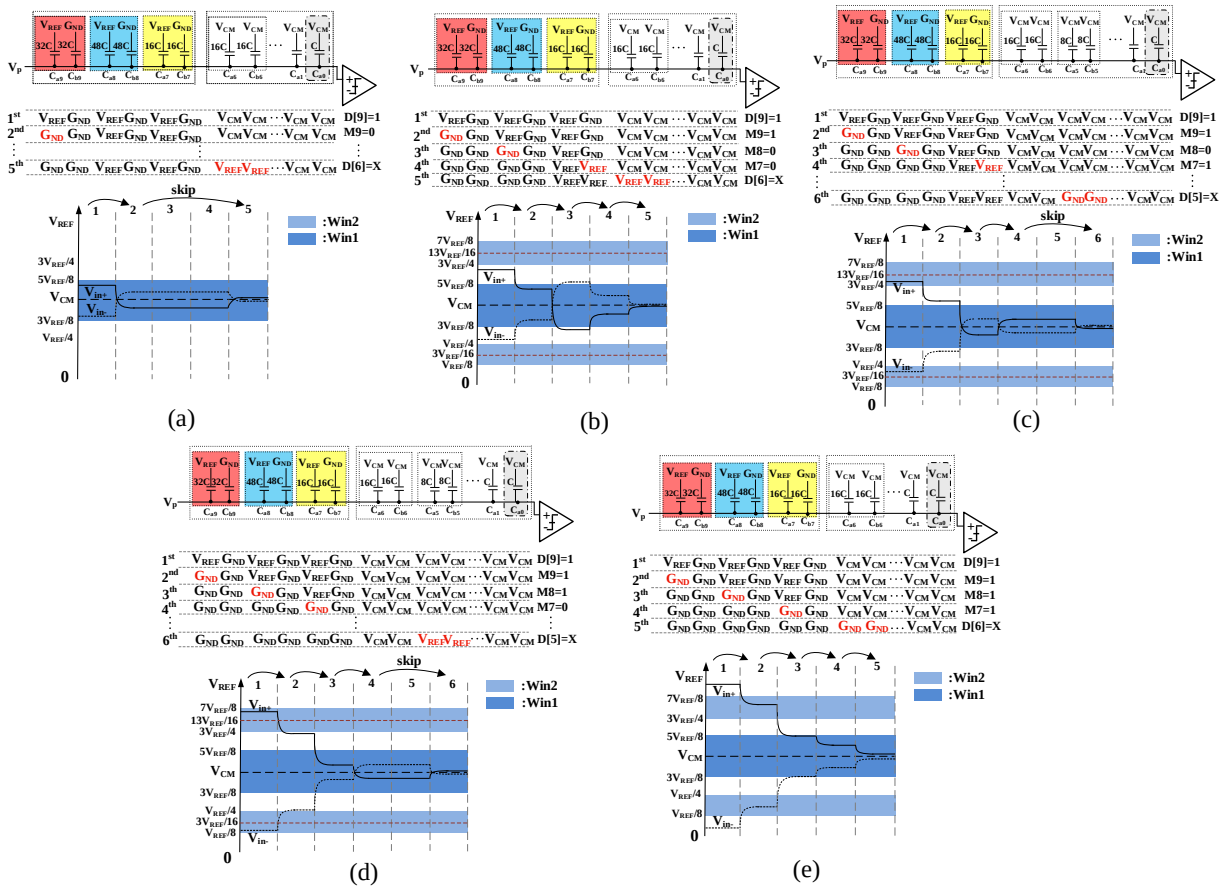


Fig. 6. The illustration of quantization process using the proposed non-binary bypass window technique. (a) D[9] = 1, M9=0, (b) D[9] = 1, M9=1, M8=0, M7=0, (c) D[9] = 1, M9=1, M8=0, M7=1, (d) D[9] = 1, M9=1, M8=1, M7=0, (e) D[9] = 1, M9=1, M8=1, M7=1.

bypass window switching operation and the case of $V_{in+} < V_{in-}$ is opposite. At this time, D[9] = 1, then C_{a9} is connected to GND and C_{d9} is connected to V_{REF}. As shown in Fig. 6(a), if M9=0, the XOR result of D[9] and M9 is 1, indicating that V_p becomes smaller than V_n. And it can be inferred that V_{in+} is within the range of [$4V_{REF}/8$, $5V_{REF}/8$], which is Win1. At this point, following the conventional SAR logic quantization rules for this range, it can be deduced that D[8]=0, D[7]=0, thus allowing the voltage switching of C_{a8}, C_{a7}, C_{b8}, C_{b7}, C_{d8}, C_{d7}, C_{e8}, and C_{e7} to be directly skipped. Afterward, quantization proceeds according to the conventional V_{CM}-based SAR logic and monotonic timing sequence, as shown in Fig. 5(a).

If D[9]=1 and M9=1, the XOR logic result is 0, and V_p is still larger than V_n. Therefore, C_{a8} is connected to GND and C_{d8} is connected to V_{REF} for voltage comparison to determine M8.

If M8=0, following the conventional SAR logic, C_{b7} is connected to V_{REF} and C_{d7} is connected to GND, after which a subsequent voltage comparison is conducted to determine M7.

If M7=0, as shown in Fig. 6 (b), it implies that the quantized voltage V_{in+} falls within the range of [$5V_{REF}/8$, $6V_{REF}/8$]. Consequently, C_{a6} and C_{b6} are connected to V_{REF}, while C_{d6} and C_{e6} are connected to GND. Subsequently, quantization proceeds according to the conventional SAR logic and monotonic timing sequence, as illustrated in the timing diagram of Fig. 5(b).

If M7 = 1, as shown in Fig. 6 (c), it implies that the quantized voltage V_{in+} falls into the range [$6V_{REF}/8$, $13V_{REF}/16$], which is Win2. At this point, following the conventional SAR logic for

TABLE I
THE MAPPING RELATIONSHIP BETWEEN THE PROPOSED BYPASS WINDOW QUANTIZATION AND THE CONVENTIONAL SAR LOGIC QUANTIZATION

MSB	**Quantification results of bypass window capacitance**			**Conventional SAR logic quantification results**			**Voltage range of V_{in+}**
D[9]	M9	M8	M7	D[8]	D[7]	D[6]	
0	0	0	0	0	0	X	[0, V_{REF}/8]
0	0	0	1	0	1	0	[V_{REF}/8, 3V_{REF}/16] ,i.e. Win2
0	0	1	0			1	[3V_{REF}/16, 2V_{REF}/8], i.e. Win2
0	0	1	1	1	0	X	[2V_{REF}/8, 3V_{REF}/8]
0	1	X	X	1	1	X	[3V_{REF}/8, 4V_{REF}/8], i.e. Win1
1	0	X	X	0	0	X	[4V_{REF}/8, 5V_{REF}/8], i.e. Win1
1	1	0	0	0	1	X	[5V_{REF}/8, 6V_{REF}/8]
1	1	0	1	1	0	0	[6V_{REF}/8, 13V_{REF}/16], i.e.Win2
1	1	1	0			1	[13V_{REF}/16, 7V_{REF}/8], i.e. Win2
1	1	1	1	1	1	X	[7V_{REF}/8, V_{REF}]

quantization, it can be deduced that D[8] = 1, D[7] = 0, D[6] = 0. Consequently, the voltage transitions for C_{a6}, C_{b6}, C_{d6}, and C_{e6} can be directly bypassed. C_{a5} and C_{b5} can be connected to GND, while C_{d5} and C_{e5} can be connected to V_{REF}. Quantization then proceeds according to the conventional logic and monotonic timing sequence, as depicted in the timing diagram of Fig. 5(c).

If M9=1 and M8=1, according to the conventional SAR logic, C_{b7} is connected to GND and C_{d7} is connected to V_{REF}, and a voltage comparison is then carried out to obtain M7.

In Fig.6 (d), if M7 = 0, it indicates that V_{in+} has fallen within the voltage range [13V_{REF}/16, 7V_{REF}/8], which is Win2. At this point, following the conventional SAR logic for quantization, it can be deduced that D[8] = 1, D[7] = 0, and D[6] = 1. Consequently, the voltage transitions for C_{a6}, C_{b6}, C_{d6}, and C_{e6} can be directly bypassed, and C_{a5} and C_{b5} can be connected to V_{REF}, while C_{d5} and C_{e5} can be connected to GND. Quantization then proceeds according to the conventional SAR logic and monotonic timing sequence, as depicted in the timing diagram of Fig. 5(d).

If M7 = 1, as shown in Fig. 6 (e), it indicates that V_{in+} has fallen within the range [7V_{REF}/8, V_{REF}]. Therefore, C_{a6} and C_{b6} are connected to GND, while C_{d6} and C_{e6} are connected to V_{REF}. The quantization follows the conventional SAR logic and monotonic timing sequence, as illustrated in the timing diagram of Fig. 5 (e).

The conventional SAR logic employs a V_{CM}-based timing scheme for quantization; the quantization of the LSB utilizes a monotonic sequence. For the next-to-least significant bit (NLST), if $V_p > V_n$, then D[1] = 1, and C_{b1} is switched to GND. On the contrary, if $V_p < V_n$, D[1] = 0, and C_{b1} is switched to V_{REF}. Subsequently, the comparison between V_p and V_n is used to determine the value of D[0].

B. Bypass Window and Non-binary Encoding

Since the capacitance weight after splitting no longer adheres to the binary relationship, it is necessary to re-encode the quantified results of the bypass window capacitance. Based on the ADC quantification process and principles, the corresponding relationship between the proposed SAR ADC with the bypass window using the split capacitors and the conventional SAR logic quantization process with the non-split capacitors has been analyzed, as shown in Table I. For example, when V_{in+} falls within the range [4V_{REF}/8, 5V_{REF}/8], the quantization result for a conventional V_{CM}-based SAR ADC is D[9]=1, D[8]=0, D[7]=0 [35]. In the quantization result of the proposed work, it is D[9]=1, M9=0, and it can bypass certain capacitor switching and infer that D[8]=0, D[7]=0.

The mapping relationship between D[8], D[7], and M9, M8, M7 during the quantization process reveals that when V_{in+} is within the range of Win1, D[9] and M9 differ, resulting in XOR value of 1 and D[8] = D[7] = M9. Conversely, when V_{in+} falls outside the range of Win1, a Karnaugh map is employed to analyze the data, ultimately yielding the expressions for D[8] and D[7]:

$$\begin{aligned} D[8] &= \overline{\overline{M9}M8M7}\,\overline{M9\overline{M8}M7}\,\overline{M9M8\overline{M7}} \\ &= \overline{M9}M8M7 + M9\overline{M8}M7 + M9M8\overline{M7} \end{aligned} \tag{1}$$

$$\begin{aligned} D[7] &= \overline{\overline{M9}M8M7}\,\overline{M9\overline{M8}M7}\,\overline{M9M8\overline{M7}}\,\overline{M9\overline{M8}\overline{M7}} \\ &= \overline{M9}M8M7 + M9\overline{M8}M7 + M9M8\overline{M7} + M9\overline{M8}\overline{M7} \end{aligned} \tag{2}$$

The encoding of D[6] will be discussed in section IV.C. Since the other quantization bits are derived from V_{CM}-based and Monotonic quantization processes, there is no need for special re-encoding of the results.

C. Analysis of Power Consumption

For an N-bit SAR ADC, if the quantization code values are uniformly distributed, the expressions for power consumption in both the capacitor array Monotonic switching scheme [37] and the V_{CM}-based switching scheme [38] can be derived as follows:

$$E_{avg,Monotonic} = \sum_{i=1}^{N-1} 2^{N-i-2} CV_{REF}^2 \tag{3}$$

$$E_{avg,V_{CM}-based} = \sum_{i=1}^{N-1} 2^{N-2i-2}\left(2^{i-1}-1\right)CV_{REF}^2 \tag{4}$$

The proposed quantization scheme is fundamentally based on V_{CM}-based quantization; however, it incorporates the dual bypass windows that omit certain aspects of the quantization process and employ a monotonic method to quantize the LSB. Consequently, the quantization process can be categorized into three distinct situations.

1) When the quantized voltage falls outside the range of bypass windows, it can be expressed as:

$$E_{no,win} = \sum_{i=1}^{N} 2^{N-2i-1}\left(2^{i-1}-1\right)CV_{REF}^2 - \left(2^{-N-1}+2^{N-9}\right)CV_{REF}^2 \tag{5}$$

2) When the quantized voltage falls within the range of Win1, the quantization power consumption of the DAC can be

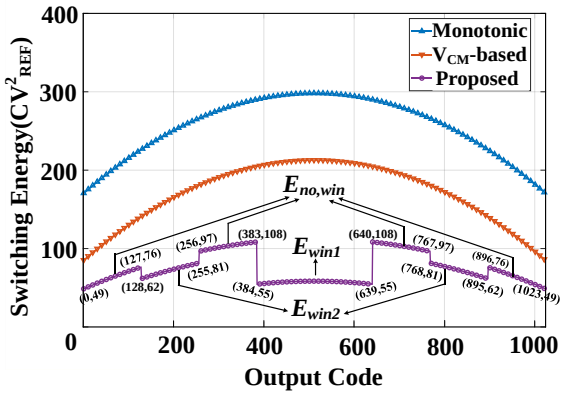


Fig. 7. The simulation results on average switching energy for 10-bit SAR ADCs, including Monotonic, V_{CM}-based and the proposed dual bypass windows based on non-binary split capacitors.

TABLE II
STATISTICS OF SIGNALS IN DIFFERENT RANGES

Signal	EMG	ECG	EEG	Sine
a_1	82.31%	87.23%	75.8%	16.04%
a_2	10.32%	3.15%	8.13%	20.71%
a_3	7.37%	9.62%	16.07%	63.25%

represented as:

$$E_{win1}=\sum_{i=3}^{N}2^{N-2i-1}\left(2^{i-1}-1\right)CV_{REF}^2-\left(2^{-N-1}-2^{N-8}\right)CV_{REF}^2 \quad (6)$$

3) When the quantized voltage falls within the range of Win2, the quantization power consumption of the DAC can be expressed as:

$$E_{win2}=\sum_{i=1}^{N}2^{N-2i-1}\left(2^{i-1}-1\right)CV_{REF}^2-\left(2^{-N-1}+2^{N-7}+2^{N-8}+2^{N-10}\right)CV_{REF}^2 \quad (7)$$

When N=10, the power consumption of DAC quantization is shown in Fig. 7. According to the paper [24], in the process of quantizing biomedical signals, the total average quantization power consumption of the DAC, E_{tot}, should be equal to:

$$E_{tot}=\alpha_1E_{win1}+\alpha_2E_{win2}+\alpha_3E_{no,win} \quad (8)$$

where α_1, α_2, and α_3 represent the probabilities of the signal falling into Win1, Win2 and outside the bypass windows (Out) respectively, and $\alpha_1+\alpha_2+\alpha_3=1$. When the SAR ADC is at full-scale input, Table II illustrates the probabilities of Sine, EMG, ECG, and EEG signals falling within the Win1, Win2, and Out ranges. It can be observed that the Sine signal is primarily distributed outside the window range. For biomedical signals, the coefficient a_1 is significantly greater than a_3 and is close to 1. This is mainly because EMG, ECG, and EEG signals are predominantly located within the Win1 range during the resting state. For EMG signals, there is even a probability of over 10% for falling into the Win2 range. If the EMG signals are in an excited state, this probability may be even higher. At the same time, Win1 corresponds to 9 comparisons for the comparator, Win2 corresponds to 10 comparisons, and Out corresponds to 11 comparisons. Due to the resting characteristics of biomedical signals, α_1 is much larger than α_3, which means that the average number of comparisons is definitely less than 10, which is lower than the number of comparisons in the conventional 10-bit SAR logic.

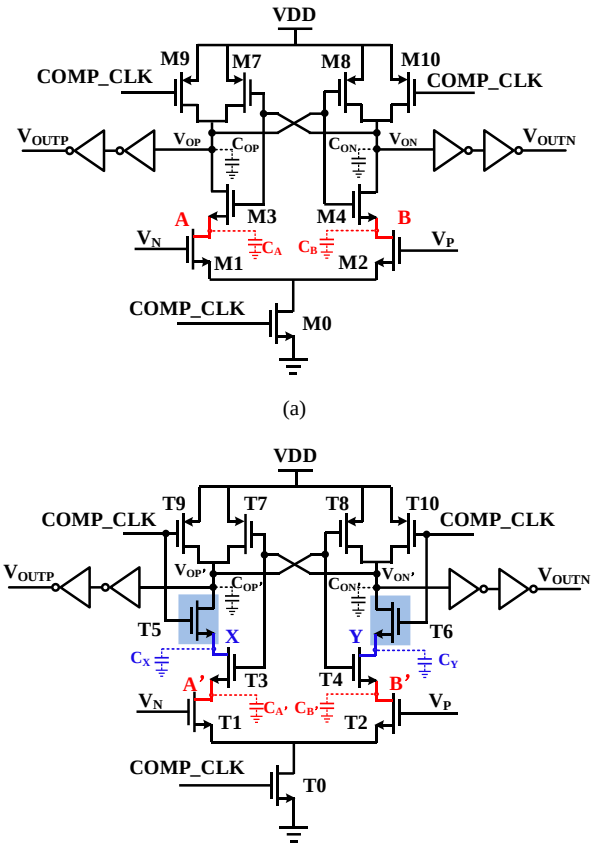


Fig. 8. (a) The conventional dynamic comparator. (b) The proposed low-power dynamic comparator.

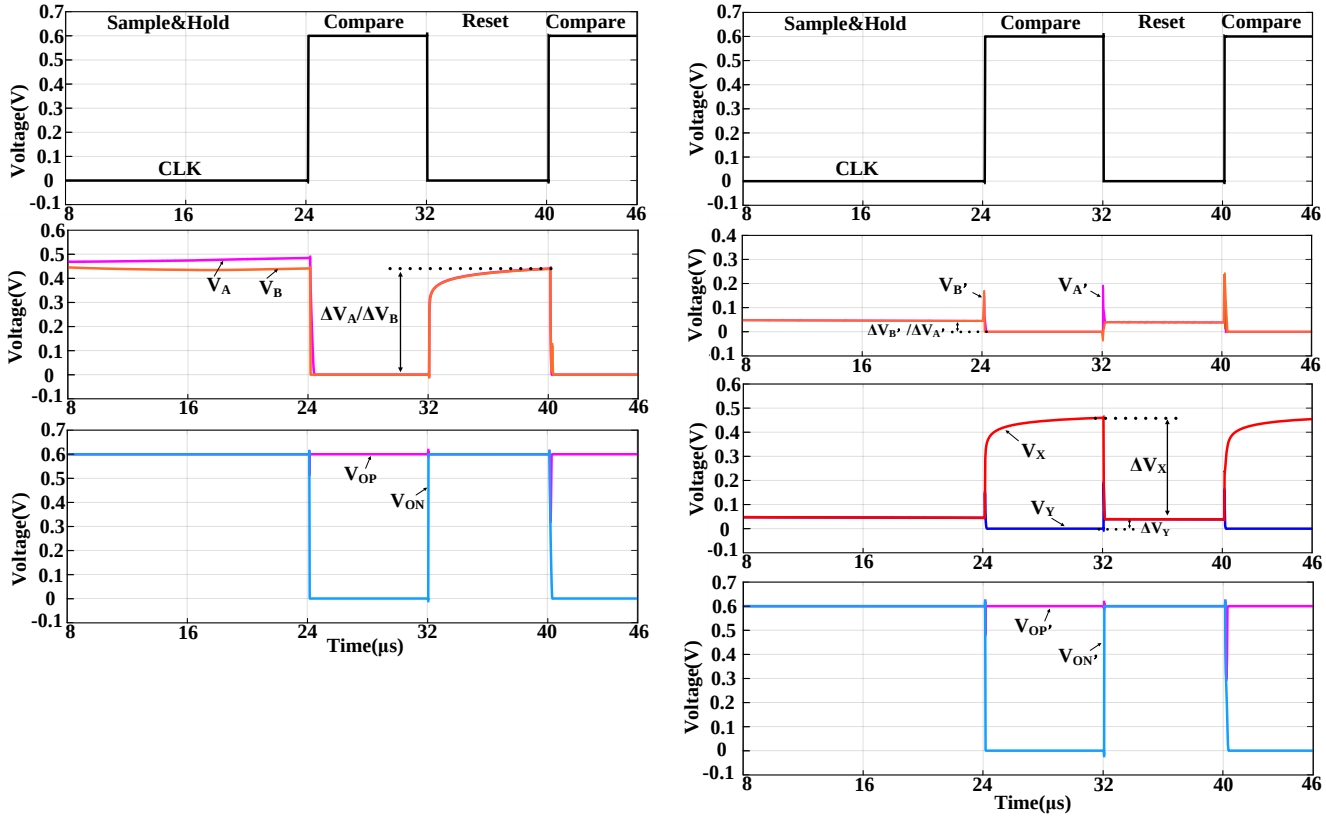
IV. CIRCUIT IMPLEMENTATION OF THE PROPOSED SAR ADC

This section describes the circuit structure and implementation details of the proposed SAR ADC, including the proposed CMOS dynamic latch comparator, SAR logic digital control circuit of the converter, and encoding circuit.

A. *The proposed CMOS dynamic latch comparator*

The comparator is a crucial component of the SAR ADC. Reducing the power consumption of the comparator is significantly important for lowering the overall power consumption of the SAR ADC and extending the battery life of the portable biomedical signal acquisition system. The CMOS dynamic latch comparator consumes zero power when not in operation and employs a positive feedback mechanism with two back-to-back cross-coupled inverters during operation. So it enables the rapid conversion of small input differential voltages into digital logic signals. Consequently, it exhibits characteristics such as low power consumption, full-swing output, and high input impedance, making it the preferred choice for designing low-power SAR ADCs.

Since this work is based on the top plates sampling, the LSB is about 1.2mV, which also leaves more margin for the design of the comparator. To minimize the power consumption of the ADC, the supply voltage is set at 0.6 V, causing the CMOS transistors in the comparator to primarily operate in the sub-threshold region. As illustrated in Fig. 8, the conventional



(a) (b)

Fig. 9. The change in internal node voltage for both the conventional comparator (a) and the proposed comparator (b).

Strong ARM latch comparator structure ensures that each circuit node maintains a high voltage swing during the latch's operation. This condition results in increased power consumption due to the charge and discharge of parasitic capacitances. To mitigate the significant voltage swing at the node during the comparison and RESET switching processes, this paper enhances the latch structure by incorporating transistors T5 and T6. These two transistors deactivate the path from VDD to A', B', X, Y nodes when in the RESET state, allowing them to consistently maintain a lower voltage during operation, thus reducing overall power consumption.

In the RESET state with COMP_CLK=0, for the conventional Strong ARM configuration, transistors M9 and M10 are turned on, resulting in V_{OP} and V_{ON} approaching VDD. As illustrated in Fig. 8 (a), the drain voltages V_{OP} and V_{ON} of transistors M3 and M4 are directly elevated to the levels close to VDD, while the source voltages V_A and V_B are similarly raised near V_{OP} and V_{ON}. In contrast, as depicted in Fig. 8(b), the proposed comparator has transistors T5 and T6 turned off. Since $V_{ON'}$ and $V_{OP'}$ are at a high level, both T3 and T4 are turned on, V_X, $V_{A'}$, V_Y and $V_{B'}$ are all at the low level. In the comparison state with COMP_CLK=1, for the conventional comparator configuration, if $V_P > V_N$, both V_A and V_B discharge to 0, with the B discharge rate faster than node A. The positive feedback in the latch causes V_{OP} to rise to VDD while V_{ON} drops to 0. M3 is turned off and M4 is turned on, leading to $V_A=V_B=V_{ON}=0$ and V_{OP}=VDD. In contrast, for the proposed comparator, T4, T5, and T6 are turned on while T3 is turned off, resulting in $V_Y=V_{B'}=V_{ON'}=0$ and V_X being pulled high,

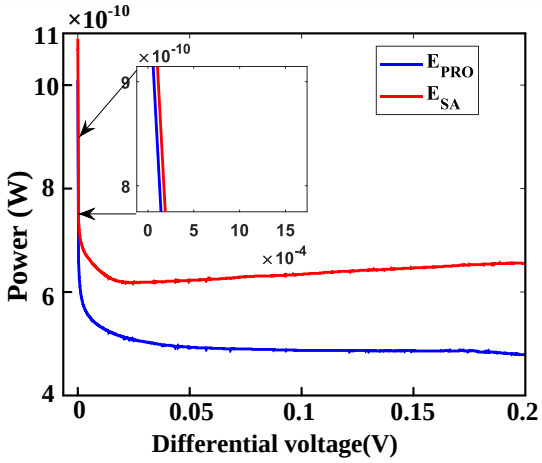


Fig. 10. The power density curves for the conventional Strong ARM comparator and the proposed comparator.

approaching $V_{OP'}$. As illustrated in Fig. 9, during the entire compare and reset process, the voltage changes at the A and B points of the conventional comparator are represented as $\triangle V_A$ and $\triangle V_B$, respectively. In contrast, for the proposed comparator, the voltage changes at the X, Y, A', and B' points are denoted as $\triangle V_X$, $\triangle V_Y$, $\triangle V_{A'}$, and $\triangle V_{B'}$. Notably, $\triangle V_A$ of the conventional comparator is approximately equal to $\triangle V_X$, while $\triangle V_B$ is significantly larger than the sum of $\triangle V_Y$, $\triangle V_{A'}$, and $\triangle V_{B'}$ in the proposed comparator. Additionally, the

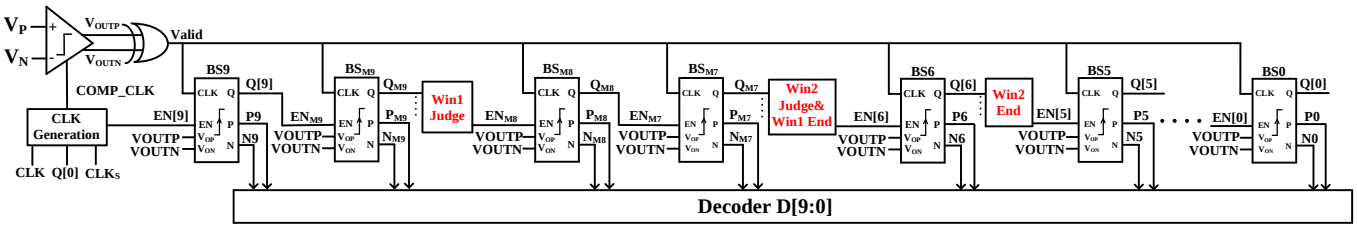


Fig. 11. The logic control circuit for the proposed SAR ADC.

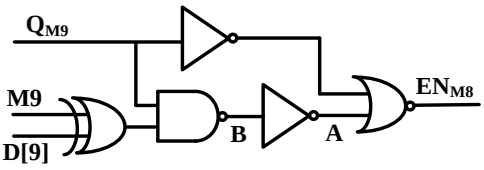


Fig. 12. The logic circuit of Win1 Judge module.

voltage changes at $V_{OP}/V_{OP'}$ and $V_{ON}/V_{ON'}$ for both comparators are nearly identical. This observation is further supported by the power consumption calculation formulas (9) for the Strong ARM comparator and (10) for the proposed comparator.

$$E_{SA} = C_A \Delta V_A^2 + C_B \Delta V_B^2 + C_{OP} \Delta V_{OP}^2 + C_{ON} \Delta V_{ON}^2 \quad (9)$$

$$E_{PRO} = C_{A'} \Delta V_{A'}^2 + C_{B'} \Delta V_{B'}^2 + C_X \Delta V_X^2 + C_Y \Delta V_Y^2 + C_{OP'} \Delta V_{OP'}^2 + C_{ON'} \Delta V_{ON'}^2 \quad (10)$$

Through the transistor-level simulations, the power density curves of the two comparators are illustrated in Fig. 10. When comparing differential voltages of equal magnitude, it is evident that the proposed comparator exhibits a lower power density than the conventional Strong ARM comparator.

For the conventional Strong ARM comparator, the integration gain A_{int} depends on the input transistor g_m/I_D and the threshold voltage V_{THN}:

$$A_{\text{int}} \approx \frac{g_m}{I_D} \cdot V_{THN} \quad (11)$$

The analysis [39] indicates that the input-referred noise of the comparator is primarily governed by the dynamic integrator and the parasitic capacitors $C_{A/B}$:

$$\sigma_{n,\text{int}}^2 \approx \frac{I_D}{g_m} \cdot \frac{4kT\gamma}{V_{THN} C_{A/B}} \quad (12)$$

In dynamic comparators, the noise and offset generated by the latch can be attenuated by the integrator gain A_{int}:

$$\sigma_{n(OS),in} \approx \sqrt{\sigma_{n(OS),\text{int}}^2 + \frac{\sigma_{n(OS),latch}^2}{A_{\text{int}}^2}} \quad (13)$$

The g_m/I_D and the parasitic capacitors $C_{A'/B'}$ of the proposed comparator are comparable to those of the conventional comparator. Therefore, theoretically, the input-referred noise of the proposed comparator should be similar to that of the conventional dynamic comparator. Simulations are also conducted on the input-referred noise of the conventional Strong ARM comparator and the proposed comparator, with results of 113.51 μV and 116.6 μV, respectively. These values are effectively comparable. Although the proposed comparator does not offer an improvement in noise performance relative to the conventional structure, it satisfies the requirements for 10-bit SAR ADCs.

B. SAR logic control circuit

For the proposed ADC architecture, its SAR logic control circuit is shown in Fig. 11. This module uses the Valid obtained by the XOR logic of the comparator output V_{OUTP} and V_{OUTN} as the control signal. The signals CLK_S, CLK, and Q[0] generate two control signals, COMP_CLK and EN[9], through the clock generation module. Notably, EN[9] is the inverse of CLK_S, allowing each bit-slice (BS) module to be activated sequentially by Q[N] = EN[N-1], thereby facilitating the output of each comparator during the quantization process[40].

In the bypass window quantization process, the control signal primarily relies on the quantization results before and after the voltage conversion of the splitting capacitor. Consequently, Win1 Judge, Win2 Judge, Win1 End, and Win2 End are determined based on whether the XOR result of the quantization value is equal to 1. Additionally, due to the timing discrepancies of the BS output signal within the circuit, certain control signals from the BS module need to be incorporated into the actual control circuit.

1) *Win1 Judge*

If the XOR result of D[9] and M9 is 1, it indicates that V_{in+} is within the range of Win1, allowing for the skipping of BS_{M8} and BS_{M7} at this time. Consequently, EN_{M8} is governed by D[9], M9, and Q_{M9}. The circuit of the Win1 Judge is illustrated in Fig. 12.

2) *Win2 Judge&Win1 End*

Given that the output results of Win2 Judge and Win1 End both influence the operational status of BS6, the Win2 opening circuit, Win1 closing circuit, and Q_{M7} collectively control EN[6]. The control logic for Win2 Judge with the input signals of Q_{M7}, M8, and M7, aligns with that of Win1 Judge, and the output is W2.

Based on the quantization timing discussed in the preceding Section III.A, the logical relationship among EN[6], W2, Q_{M7}, and A is presented in Table III. The relationship can be expressed as:

$$EN[6] = \overline{\overline{A Q_7} \, \overline{W_2}} = \overline{B Q_7} \, \overline{W_2} \quad (14)$$

The corresponding control circuit is shown in Fig. 13.

3) *Win2 End*

Since EN[5] is determined by the outputs of Q6 and Win2 Judge, and given that either Q6 or C equals 1, then EN[5] is 1. Therefore, the logical relationship of the circuit is as Fig. 14.

TABLE III
LOGIC RELATIONSHIP BETWEEN EN[6], W2, QM7, AND A

Input			Output
A	Q_{M7}	W2	EN6
1	X	X	1
0	1	0	1
	0	0	0
	0	1	0
	1	1	0

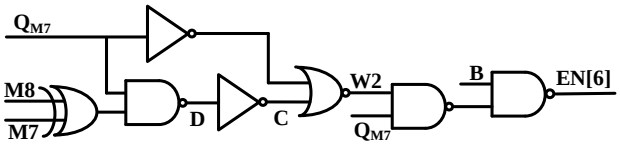


Fig. 13. The logic circuit of Win2 Judge&Win1 End module.

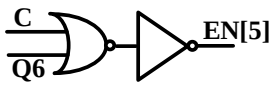


Fig. 14. Circuit for controlling EN[5].

C. *Re-encoding circuit module*

Since the quantization result of the bypass capacitors is non-binary, a specialized re-encoding circuit is necessary to encode this result. As detailed in Section III.B regarding the re-encoding process, when V_{in+} falls within the range of Win1, D[8] = D[7] = M9; when V_{in+} is outside the range of Win1, the expressions for D[8] and D[7] are given by equations (1) and (2), respectively. For D[6], if V_{in+} falls within Win2, D[6] is derived from M7 by inversion; otherwise, it is quantized according to conventional SAR logic, which means D[6] equals P6.

V. MEASUREMENT RESULTS OF THE PROPOSED SAR ADC

In this section, the performance of the proposed SAR ADC is tested, and its power consumption for the quantization of physiological signals is measured. Additionally, its performance is compared with state-of-the-art ADCs.

A. *Sine signal measurement results*

A prototype chip of the proposed non-binary dual bypass window 10-bit SAR ADC has been designed and fabricated using a standard 0.18-μm CMOS process. The chip test platform, PCB test board, and die microphotography are illustrated in Fig. 15. To minimize power consumption of the quantizer while addressing the factors such as switching noise limitations and unit capacitor mismatch, this study employs the smallest size MIM capacitor available in this process, approximately 15.5 fF, as the unit capacitance for the DAC array. Additionally, to mitigate the effects of capacitor size mismatch, a significant number of dummy capacitors have been incorporated into the capacitor array. The core area is 381.7×416.8 μm^2. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) errors are illustrated in

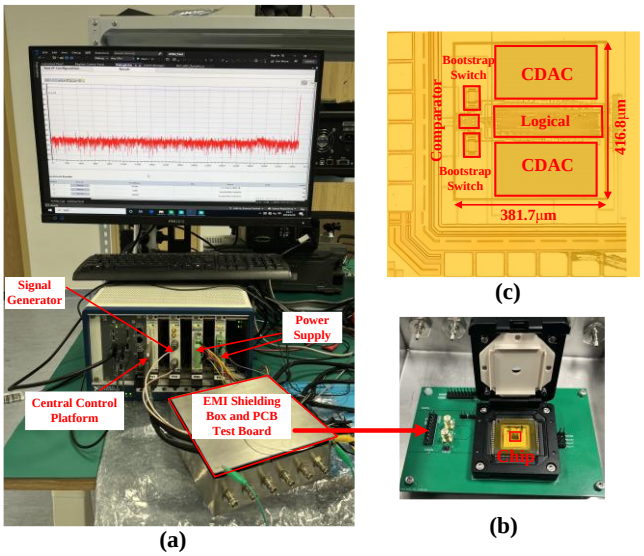


Fig. 15. (a) Test platform, (b) PCB test board, (c) Die microphotography.

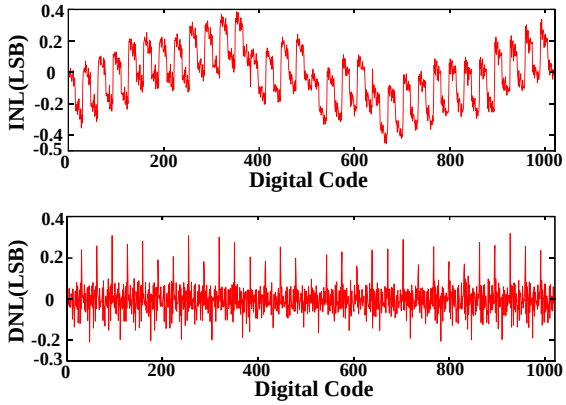


Fig. 16 The measurement results of INL and DNL for the proposed ADC.

Fig. 16, with peak values of DNL and INL recorded at -0.21/0.32 and -0.45/0.38 LSB, respectively. When a 2.56 kHz sine wave signal is digitized at a sampling rate of 5.21 kS/s, the spectrum obtained from the proposed SAR ADC is depicted in Fig. 17(a). The measured SNDR is 57.51 dB, while the measured SFDR is 71.68 dB. A total of 16,384 points are recorded, yielding the ENOB of 9.26 bits at an input frequency near the Nyquist frequency.

To evaluate the robustness of the proposed SAR ADC, the measured SNDR and SFDR values are plotted against various input frequencies at a constant sampling rate, as illustrated in Fig. 17(b). Additionally, it is observed that the maximum sampling rate of the chip reaches 6.94 kS/s, with corresponding SNDR and SFDR values of 56.94 dB and 68.49 dB, respectively, resulting in an ENOB of 9.25 bits. For a full-scale 2.56 kHz sine wave input signal, the measured total power consumption of the SAR ADC at a 5.21 kS/s sampling rate is 9.68 nW. As depicted in Fig. 18, the power contributions of the DAC, logic circuit, improved dynamic CMOS comparator, and other circuits are 54.9%, 33.8%, 9.9%, and 1.4%, respectively. Based on the FoM calculation formula defined by Power/(2^ENOB*2*BW), the FoM is approximately 2.9 fJ/Conv.-step.

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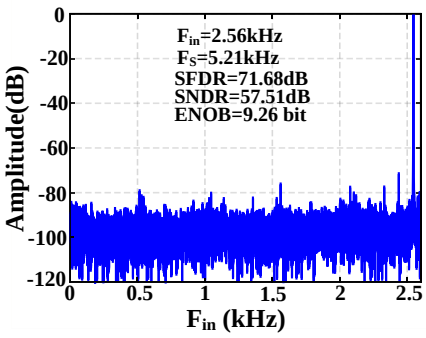
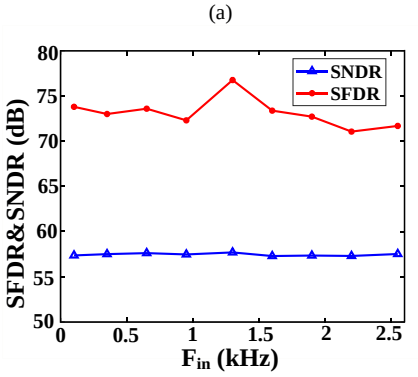


(a)



(b)

Fig. 17. The measurement results of the proposed SAR ADC, (a)the output spectrum at 5.21 kS/s with 2.56-kHz input, (b) the SNDR and SFDR versus input frequency.

To evaluate the power consumption of the proposed SAR ADC, schematic simulations were conducted to calculate the average power consumption within Win1 ($P_{ADC@Win1}$), Win2 ($P_{ADC@Win2}$), and the Out ($P_{ADC@Out}$). In addition, under the same conditions, the power consumption of a SAR ADC without bypass windows ($P_{ADC@W/O}$), a traditional V_{CM}-based SAR ADC ($P_{ADC@V_{CM}-based}$), and the proposed SAR ADC ($P_{ADC@sin}$) during the quantization of a sine signal were also simulated. Using $P_{ADC@W/O}$ as the reference, the percentage of power consumption for each scenario was calculated.

As depicted in Fig. 19, the power consumption of the V_{CM}-based SAR ADC, $P_{ADC@V_{CM}-based}$, represents 120.11% of $P_{ADC@W/O}$. In comparison, the power consumption of the proposed SAR ADC, $P_{ADC@sin}$, is only 96.93% of $P_{ADC@W/O}$, which shows that the proposed is lower than that of a SAR ADC without bypass windows under the same conditions. Within the bypass windows, the average power consumption in Win1, $P_{ADC@Win1}$, is the lowest, at 67.71% of $P_{ADC@W/O}$; the average power consumption in Win2, $P_{ADC@Win2}$, is 95.28% of $P_{ADC@W/O}$. Although the power consumption outside the window, $P_{ADC@Out}$, is higher than $P_{ADC@W/O}$, the statistics of physiological signals shown in Table II reveal that the probability a_3 of falling outside the window is quite low.

B. *Biomedical signal measurement results*

In addition to quantifying the sine signal, the proposed SAR ADC is also assessed its low power consumption and reliability by quantifying the biomedical signals collected through specialized biomedical signal acquisition modules.

As illustrated in Fig. 20(a), the left part depicts the process of collecting EMG signals from the arms, encompassing both relaxation and contraction states of the forearms. The EMG signal is acquired using a gel electrode and is transmitted through a specialized biomedical signal acquisition module. This module includes an amplification circuit based on TI instrumentation amplifier INA141 chip, a filter circuit based on the precision operational amplifier OPA180 chip, as well as the ADC circuit of ADS1292R chip. The extracted EMG digital signal is shown in right part of Fig. 20(a), and input into the signal generator of the test platform. A full-scale differential analog signal derived from the collected EMG digital signal is obtained, which is then input into the proposed SAR ADC. The measured power consumption of the left forearm in the relaxed state is 7.63nW, while the power consumption during the contraction is 8.16nW. For the right forearm, the power consumption in the relaxed state is 7.59nW, and during the contraction, it is 8.2nW. The overall average power consumption is calculated to be 7.9nW.

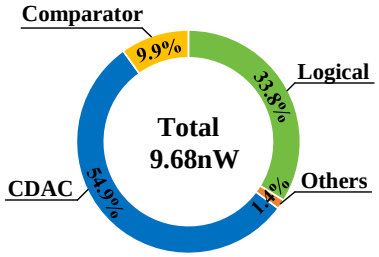


Fig. 18. The measurement results of the power consumption for each block in the proposed SAR ADC.

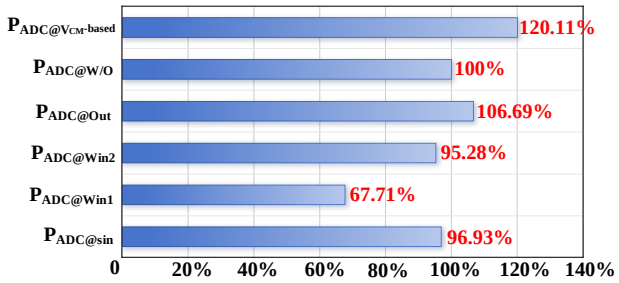


Fig. 19. The Statistics of ADC Power Consumption under Different Structures or States.

As illustrated in Fig. 20(b), a 12-lead ECG signal is generated by the commercial ECG signal generator SKX-2000 to simulate the authentic ECG signal of human. This ECG signal is subsequently collected and processed through the biomedical signal acquisition module and signal generator. The generated differential ECG signals are then input into the proposed SAR ADC through the test platform for quantification. The average power consumption of the 12-lead ECG signal is measured to be 8.13nW.

As shown in Fig. 20(c), the 32-channel EEG signals are collected in a resting state with eyes closed using the NeuSen.W32 device. The 32-channel EEG data are averaged for lead reference, and a MATLAB FIR filter is applied for band-pass filtering in the range of 1-49 Hz, followed by down sampling the signal to 256 Hz. Independent Component Analysis (ICA) is utilized to eliminate eye movement influence, resulting in the final 32-channel waveform. In order to enhance

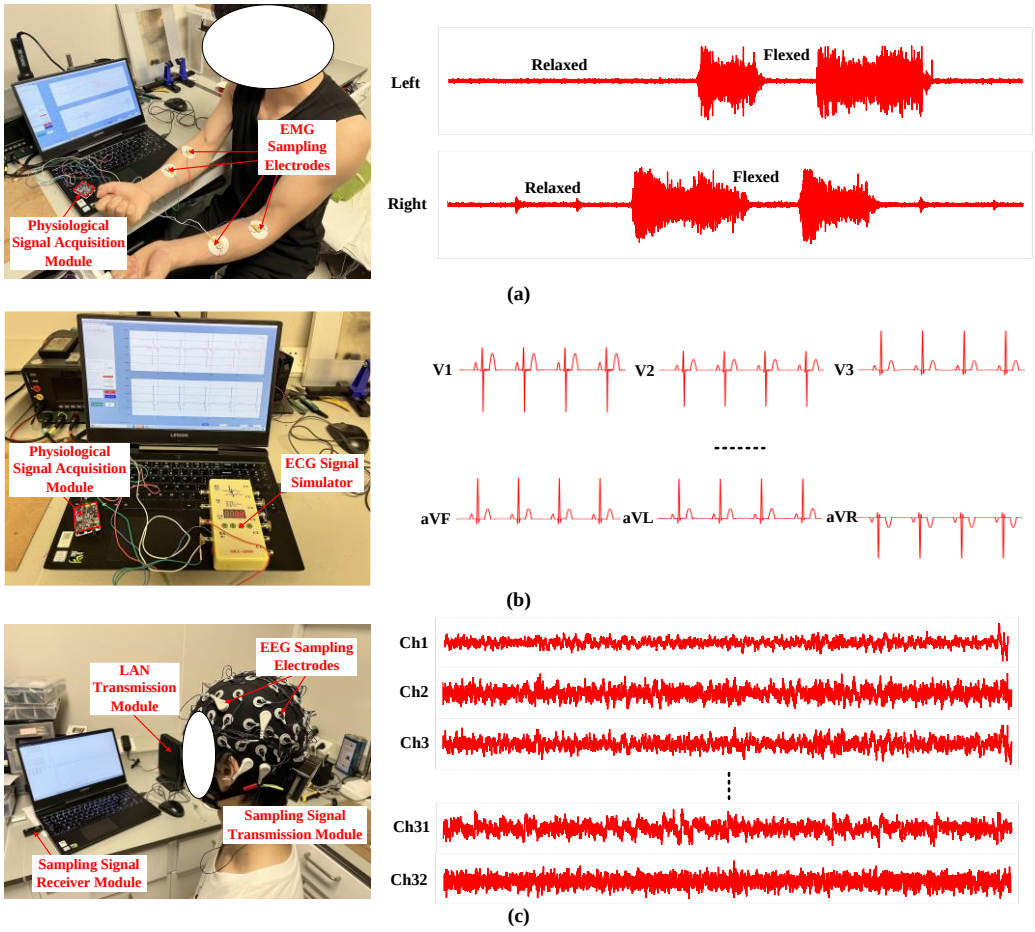


Fig. 20. (a) Acquisition of EMG Signals, (b) Acquisition of Simulated 12-Lead ECG Signals, (c) Acquisition of 32-Channel EEG Signals.

TABLE IV
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART WORKS

	TBCAS' 24[21]	TBCAS' 24[44]	LSSC' 20[45]	TCAS-II' 23[46]	VLSI Circuits' 15[7]	SJ' 20[47]	SL' 23[48]	JSSC' 18[29]		**This work**			
Process	55nm	180nm	65nm	180nm	180nm	180nm	65nm	180nm		**180nm**			
Supply (V)	1.2	0.9	0.55	0.6	0.6	1	1	0.6		**0.6**			
ADC Type	LC+SAR	LC	SAR	SAR	SAR	NS-SAR	NS-SAR	SAR		**SAR**			
Target Signal	Bio	ECG	ECG	ECG	ECG	Bio	Bio	Bio		**Bio**			
Bypass Window	Yes	Yes	Yes	Yes	Yes	No	No	Yes		**Yes**			
Fs (kHz)	-	50.3	1	50	100	-	10	50		**5.21**			
BW (kHz)	25	0.1	0.5	25	-	0.625	0.2	25		**2.6**			
Resolution (bit)	4+4	7	-	12	8	-	-	10		**10**			
ENOB (bit)	-	7.4	-	10.12	7.5	10.5	12.13	9.16		**9.26**			
SFDR(dB)	-	-	-	82.4	-	-	-	-		**76.22**			
SNDR(dB)	51.2 @0.2kHz	46.3	60.43-57.26	62.7	-	65	74.78	56.9		**57.51**			
Power (nW)	440	5.9	2.7-3.9	1540	120	90	1000	144 (sin)	76.1 (ECG)	**9.68 (sin)**	**7.95 (EMG)**	**8.13 (ECG)**	**8.22 (EEG)**
FoM(fJ/Conv.-step)	29.7	174 @0.005	3.1-6.5	27.7	6.6	50	56	3.99	2.66	**2.9**	**2.49**	**2.55**	**2.58**
Calibration	No	No	Yes	No	No	No	No	Yes		**No**			

FoM= Power/(2^ENOB*2*BW)

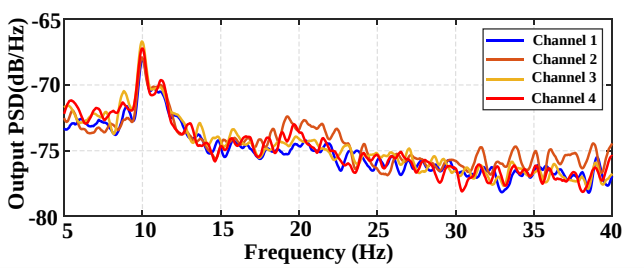


Fig. 21. The first four-channel EEG recording during eyes closed.

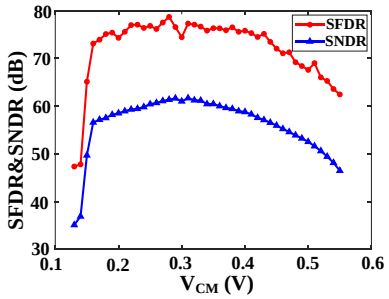


Fig. 22. The variation of SFDR & SNDR with V_{CM}.

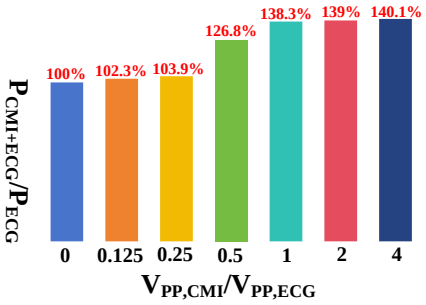


Fig. 23. Quantization power consumption versus CMI intensity.

the clarity and discernibility of EEG signals [41], as depicted in Fig. 21, a frequency-based analysis was performed on the first four channels of EEG. Subsequently, the generated 32-channel EEG signal is produced by the signal generator of the test platform, which creates a differential analog signal. The amplitude is adjusted to match the full-scale range of the proposed SAR ADC. The EEG signal is then quantified, and the average quantization power consumption is measured to be 8.22nW.

During the acquisition of biological signals, motion artifacts and common-mode interference (CMI) often cause shifts in the common-mode voltage of the biological signals, which may differ from the V_{CM} of the bypass window. Theoretically, such shifts should not impact the normal operation of the bypass window or the SAR ADC. This is because the bypass window is primarily determined based on the digital results obtained during the quantization process, and it exhibits strong robustness against interference. Simulations were performed on the proposed SAR ADC circuit under different V_{CM} conditions, and the changes in SFDR and SNDR with V_{CM} were analyzed. As shown in Fig. 22, when the V_{CM} is within the range of [0.16V, 0.46V], both SNDR and SFDR exceed 55dB. Additionally, by examining the internal signals of the circuit, it can be observed that the bypass window continues to function properly after being triggered.

Generally, in a biopotential recording system, if the total common-mode rejection ratio (T-CMRR) of the instrumentation amplifier (IA) is inadequate, residual 60 Hz (or 50 Hz) interference or motion artifacts will be superimposed onto the differential-mode ExG signals [42][43]. These CMI can influence the quantization power consumption of SAR ADCs. Assuming a CMI frequency of 60 Hz, the intensity of CMI is characterized by the ratio of the peak-to-peak voltage of the CMI signal ($V_{PP,CMI}$) to that of the ECG signal ($V_{PP,ECG}$). When the ECG signal with residual CMI is input at full scale into the proposed SAR ADC, simulations reveal the quantization power consumption of the SAR ADC under varying CMI intensity levels, as depicted in Fig. 23. It is evident that as the CMI intensity increases, the ratio of the quantization power consumption of the ECG signal with residual CMI ($P_{CMI+ECG}$) to that of the ECG signal without CMI (P_{ECG}) also increases. When the CMI intensity is below 0.25, the increment in $P_{CMI+ECG}$ is relatively small. This is primarily because, despite the presence of residual CMI, the ECG signal still predominantly falls within the Win1 or Win2 ranges during the quantization process. However, when the CMI intensity exceeds 0.5, $P_{CMI+ECG}$ increases significantly. This is because the higher CMI intensity reduces the probability of the ECG signal with residual CMI falling within the Win1 or Win2 ranges. Under such conditions, the quantization power consumption is even more strongly influenced by CMI.

C. *Performance comparison with state-of-the-art works*

Table IV demonstrates that this work has a significant advantage in power efficiency and robustness compared to other SAR ADCs, especially in the process of quantizing biomedical signals such as ECG/EEG/EMG. The level-crossing (LC) ADC structure is a commonly used architecture in the biopotential recording applications. Although this structure reduces power consumption by using an adequate number of samples and decreasing the operating frequency, thereby benefiting other modules of the system on the chip (including processors and transceivers), it still has a considerable gap in power efficiency, particularly in terms of FoM, compared to this work.

The relationship between ENOB and power consumption is quite complex. For medium-precision (8-12bit) SAR ADCs, ENOB is primarily influenced by quantization noise. However, the capacitance values, capacitance structures, and capacitance switching strategies within the capacitor array determine the quantization noise, and the switching power consumption accounts for the majority of the quantization power consumption of the entire SAR ADC. Therefore, optimizing the capacitor array and its quantization switching strategies is often the main research direction for reducing ADC power consumption. Furthermore, for medium-precision, low-speed SAR ADCs, if the bypass window is realized through capacitor splitting, the design process can achieve a calibration-free configuration by optimizing the PVT-sensitive circuit design and capacitor layout. This approach not only mitigates the power dissipation associated with internal background calibration circuits but also obviates the complexity of foreground calibration procedures. Hence, at present, optimizing the capacitor array and implementing

calibration-free designs are emerging trends in the development of low-power SAR ADCs.

VI. Conclusion

This paper proposes a dual bypass windows structure based on a non-binary split capacitor array for ECG/EEG/EMG signals. This window structure effectively minimizes unnecessary voltage flips and reduces comparator operation times during the quantization process. Additionally, a dynamic CMOS comparator structure is proposed, which mitigates the latch node voltage changes during the operation, thereby further decreasing the power consumption in the comparison process. The entire ADC circuit is fabricated using a 180nm CMOS process. The measurement results indicate: (1) At a power supply of 0.6V, for sine signal input, the ADC achieves an accuracy of 5.21kHz with 9.26 bits, power consumption of 9.68nW, and a FoM of 2.9 fJ/Conv.-step. (2) For EMG signals, the power consumption for the left forearm in a relaxed state is 7.63nW, the overall average power consumption is 7.95nW. (3) For the 12-lead ECG signal, the average quantized power consumption is 8.13nW. (4) The average power consumption for quantifying the 32-lead EEG signal is 8.22nW. As a result, the proposed SAR ADC is highly suitable for serving as a data converter in low-power wearable biomedical signal acquisition systems.

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