# A 0.6-V 9.38-Bit 6.9-kS/s Capacitor-Splitting Bypass Window SAR ADC for Wearable 12-Lead ECG Acquisition Systems

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***Abstract*—This article proposes a fully differential ten-bit energy-efficient successive approximation register (SAR) analog-to-digital converter (ADC) for wearable 12-lead electrocardiogram (ECG) acquisition system. The proposed ADC structure generates two bypass windows through capacitor splitting technique, which can skip unnecessary quantization steps. The judgment module of bypass windows only requires an XOR gate. By introducing redundant capacitors to participate in quantization, the total capacitance value is reduced by half. The proposed SAR ADC is fabricated using a standard 180-nm CMOS process. The measurement results show that it can achieve an effective number of bits (ENOBs) of 9.38 bits and a spurious-free dynamic range (SFDR) of 76.71 dB with a supply voltage of 0.6 V at a sampling rate ($F_S$) of 6.94 kS/s. The power consumption is 15.61 nW when subjected to a 1.17-$V_{PP}$ 3.45-kHz sinusoidal input, resulting in a figure of merit (FoM) of 3.38 fJ/conv.-step. The average power consumption for quantizing 12-lead ECG signals is approximately 12.66 nW, demonstrating the ability to achieve ultralow-power quantization of ECG signals.**

***Index Terms*—12-Lead electrocardiogram (ECG), bypass window, capacitor splitting, low power, successive approximation register (SAR) analog-to-digital converter (ADC).**

## I. Introduction

ELECTROCARDIOGRAM (ECG) is the primary method for detecting heart diseases [1]. The 12-lead ECG shirt based on flexible fiber electrodes, similar to the LifeShirt [2], as shown in Fig. 1, provides exceptional convenience for patients requiring long-term ECG monitoring [3]. The battery and circuit system are both integrated into the clothing, which sets more rigorous requirements for its size and power consumption. In recent years, ECG acquisition systems, which are low-power, high-resolution, and compact, have been increasingly reported [4]. However, a 12-lead ECG theoretically requires 12 analogy front-end (AFE) modules and analog-to-digital converters (ADCs), which greatly increases the area and power consumption [5]. Therefore, as illustrated in Fig. 1, some recent studies have begun to explore shared ADC architectures to quantize front-end signals [6], [7], [8]. However, when sharing ADCs, the summation of ECG signals from multiple leads increases the dynamic range and accumulates in-band noise. As a result, a 16-bit sigma-delta ADC is required, which greatly increases the design complexity and power consumption of the ADC [6], [7]. The commonly used ten-bit successive approximation register (SAR) ADC has advantages in the low-power quantization process of physiological signals, particularly for ECG signals. Additionally, only one multiplexer (MUX) circuit is needed for the shared ADCs [8], [9]. Hence, there is a necessity for a low-power SAR ADC capable of quantifying all 12-lead ECG signals simultaneously.

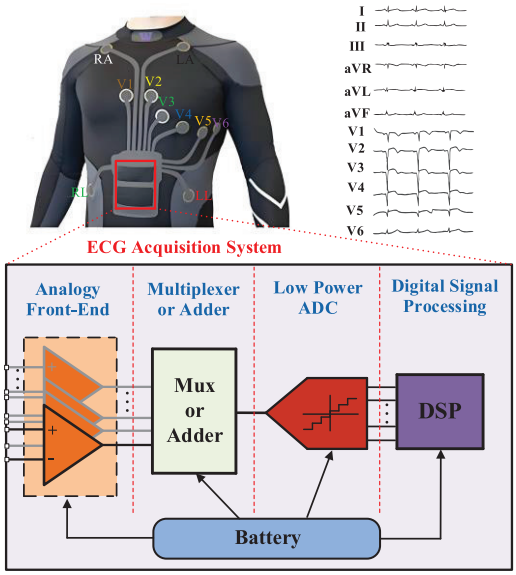


Fig. 1. Diagram of 12-lead ECG System using shared ADC in ECGShirt.

Some methods have been proposed to achieve a reduction in power consumption during ECG signal quantization [10], [11], [12], [13], [14], [15]. Mao introduces a low-power SAR ADC designed for biomedical signal processing, which implements a new digital-analog converter (DAC) architecture that facilitates the segmentation of capacitor array, thereby

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reducing the total number of unit capacitors required [10]. Nevertheless, this new segmented structure is susceptible to the common drawbacks associated with the C-2 C configuration. In [12], an least significant bit (LSB)-first algorithm is reported that it could proportionally decrease overall power consumption in response to the changes in the input signal. However, when input variation rate increases, an N-bit conversion might necessitate up to $2N+1$ comparison cycles, leading to unnecessary power expenditure. Zhang et al. [15] utilize two redundant capacitors to introduce two dynamic tracking windows, enhancing the accuracy of window prediction and consequently reducing the power consumption associated with DAC switches, comparators, and digital control logic. Yet, the input signal frequency in this configuration is significantly lower than the Nyquist rate, which also represents an inefficiency in power usage.

To simplify the reduction of quantization power consumption, the use of fixed bypass windows based on capacitance or voltage can reduce the complexity of the control module and maximize the probability of the ECG signal falling within the window through statistical methods [16], [17]. Wang et al. [17] present a comparator with a current correlator that generates trigger signals for the bypass window during the comparison process. However, this structure necessitates high-precision calibration of the bypass window range. Guerber et al. [18] and Lee et al. [19] introduce the dedicated time detection circuits that use the polarity of the comparator's output and the comparison timing to determine if the signal falls within the bypass window. Nevertheless, this approach has poor process-voltage–temperature (PVT) characteristics, and in some cases, it can lead to capacitive coupling, resulting in power wastage.

To enhance the robustness of the bypass window, bypass techniques incorporating fixed-capacitance windows and digital judgment modules have been successively developed [20], [21], [22]. Wang and Kuo [20] designed a bypass window based on capacitor splitting in the backend ADC of a pipelined-SAR ADC. By detecting that any two consecutive comparison results have opposite polarities, it can be determined that the input lies within the bypass window, thereby skipping power-wasting transitions and reducing the DAC switching power by 42%. However, the bypass window detection requires two additional comparisons, which is not highly efficient. Moreover, both the capacitor array splitting scheme and the quantization scheme can be further optimized. Lee and Lin [21] proposed a bypass window switching method based on a fixed capacitor $C_7$. This method requires no additional analog circuits and is applicable to "set-down" SAR ADCs with variable input common-mode voltages [21]. However, each bypass window determination necessitates a voltage transition of capacitor $C_7$ and an additional comparison cycle. If not, the voltage of $C_7$ must be "switched back," which incurs power consumption and time delays. Liang et al. [22] proposed the fast-window-switching (FWS) technique, which reduces capacitor switching operations by introducing a "window region," thereby mitigating nonlinearity caused by capacitor mismatch. The FWS technique generates window boundary voltages using capacitors and features a simple logic circuit. However, the FWS still involves "switch-back" operation. Most importantly, these bypass window techniques are difficult to adapt to low-power quantization for all 12-lead signals.

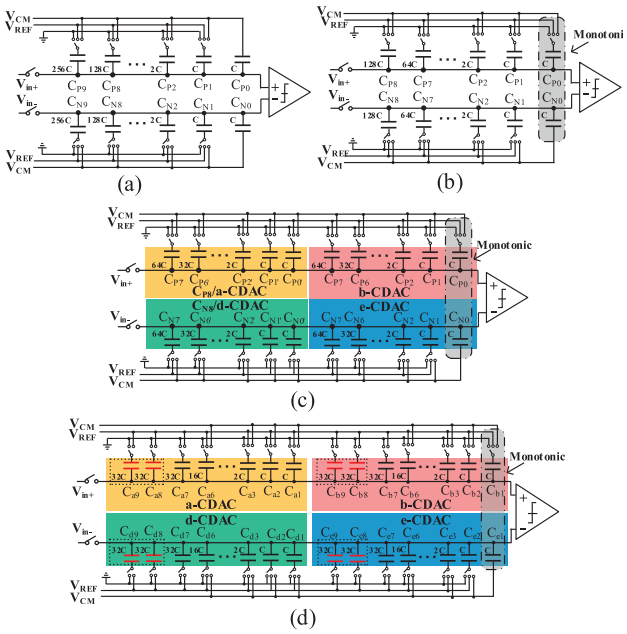



Fig. 2. Capacitor array of a ten-bit SAR ADC. (a) Capacitor array of conventional $V_{CM}$-based SAR ADC. (b) Redundant unit capacitor is quantized through the monotonic method. (c) Splitting of 128C. (d) Proposed split capacitor array.

This article proposes an efficient most significant bit (MSB) capacitor splitting and two bypass windows for the distribution characteristics of 12-lead ECG signals, and the judgment module is very simple and only requires an XOR gate, which has excellent robustness and low power consumption. Moreover, by introducing the redundant bit's unit capacitor through monotonic quantization, the total capacitance of the capacitor array can be reduced from $2^{N-1}$ to $2^{N-2}$, resulting in nearly halving the area of the capacitance of DAC (CDAC) and the switching power in quantization. Additionally, the split capacitor array can be better arranged through a co-centric layout, further enhancing the matching of unit capacitors.

The rest of this article is arranged as follows. Section II describes the proposed SAR ADC structure and the individual circuit modules. Section III discusses the operating principle of the bypass window, power consumption analysis, the quantization of 12-lead ECG signals, and the implementation of the specific logic circuits. Section IV verifies the model by measurement results on a ten-bit SAR ADC design. Finally, Section V concludes this article.

## II. Proposed SAR ADC Architecture

As depicted in Fig. 2(a), in a conventional ten-bit $V_{CM}$-based SAR ADC, the MSB capacitor of the CDAC array is 256C. To reduce the power consumption of CDAC, the redundant capacitors $C_{P0}$ and $C_{N0}$ are quantized using a monotonic quantization method. This allows the total capacitance of the CDAC to be reduced by half, as shown in Fig. 2(b), with the MSB capacitor being 128C. Simultaneously, as depicted

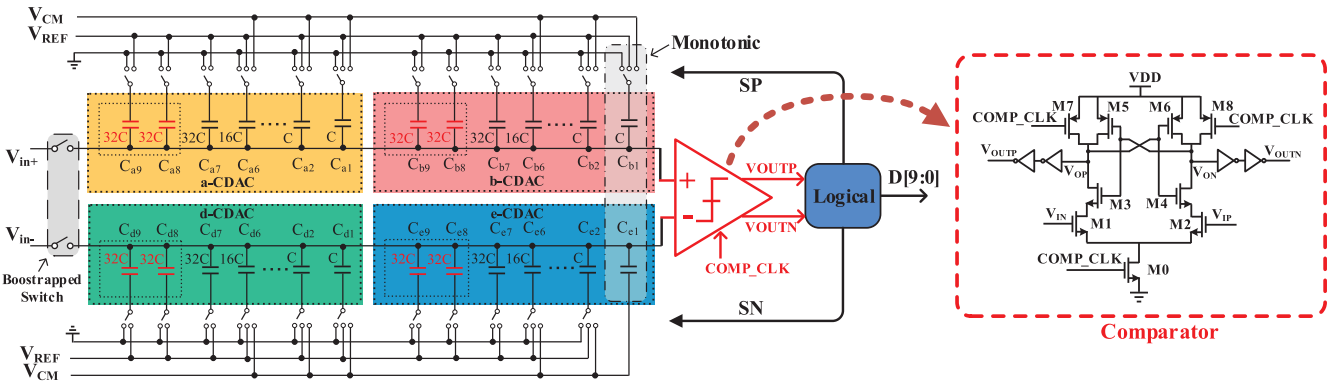



Fig. 3. Block diagram of the proposed ten-bit SAR ADC for 12-lead ECG, detailing the splitting CDAC and the strong ARM latch comparator.

in Fig. 2(c), the capacitor 128C ($C_{P7}$ and $C_{N7}$) is split into subarrays (a-CDAC and d-CDAC) that are consistent with the subsequent capacitor arrays (b-CDAC and e-CDAC), which enables better centroid symmetry and matching in the layout. Moreover, during the quantization process, each voltage switching operation of the CDAC requires the bottom plates of the corresponding capacitors in the four subarrays (a-CDAC, b-CDAC, d-CDAC, and e-CDAC) to switch voltages. This leverages the symmetry of the capacitors to further minimize errors caused by capacitor mismatch. For example, if $V_{in+} > V_{in-}$, the first voltage transition of the capacitor array involves switching the bottom plates of $C_{P7'}$ and $C_{P7}$ from $V_{CM}$ to $V_{REF}$ and the bottom plates of $C_{N7'}$ and $C_{N7}$ from $V_{CM}$ to GND, followed by a voltage comparison. The subsequent voltage transitions in the quantization process follow a similar sequence.

As shown in Fig. 2(d), the 64C capacitors [i.e., $C_{P7'}, C_{N7'}, C_{P7}$, and $C_{N7}$ in Fig. 2(c)] in the CDAC are all split into "32C +32C." Moreover, the bottom plates of the 32 C capacitors (i.e., $C_{a9}$, $C_{a8}$, $C_{a7}$, $C_{b9}$, $C_{b8}$, $C_{b7}$, $C_{d9}$, $C_{d8}, C_{d7}, C_{e9}, C_{e8}$, and $C_{e7}$) are replaced with dual-select switches that can connect to either $V_{REF}$ or GND. During the quantization process, the voltage transitions resulting from the quantization of the split capacitors ("32C +32C") are used to form two bypass windows named Bypass Window 1 (Win1), which is [$3V_{REF}/8$, $5V_{REF}/8$], and Bypass Window 2 (Win2), which is [$2V_{REF}/8$, $3V_{REF}/8$] and [$5V_{REF}/8$, $6V_{REF}/8$]. By monitoring whether the quantization result changes before and after the voltage flip of the "32C +32C" capacitance, it is determined whether the input signal falls within the bypass window. For the signals falling within the window, the quantization process can be further optimized to reduce the power consumption of DAC switches, comparators, and digital control logic.

Fig. 3 shows the block diagram of the proposed ten-bit SAR ADC with capacitance splitting. It consists of a pair of bootstrapped sampling switches, a differential splitting capacitor array, a dynamic comparator based on the strong ARM latch structure, and a logic module. To achieve low power consumption, the comparator operates in subthreshold conduction mode.

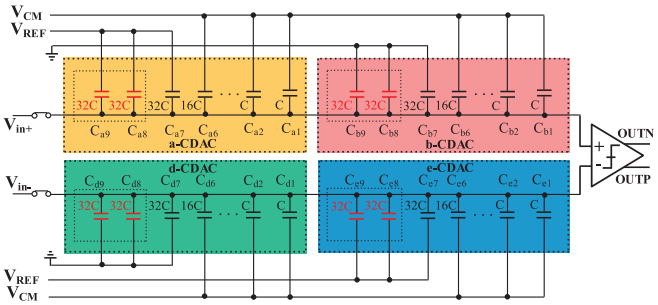



Fig. 4. Diagram of capacitor array connections during the sampling process.

## III. Design Principles and Circuit Implementation of the Proposed SAR ADC

In this section, the proposed SAR ADC is described in detail, including the voltage switching scheme of bypass windows, the quantization of 12-lead ECG signals, analysis of power consumption, and the design of logic control circuits.

### A. Voltage Switching Scheme and Bypass Window Design

As shown in Fig. 4, during the sampling process, the input signals are connected to the top plates of the capacitor array, i.e., $V_p = V_{in+}$ and $V_n = V_{in-}$. At the same time, the bottom plates of $C_{a9}, C_{a8}, C_{a7}, C_{e9}, C_{e8}$, and $C_{e7}$ are connected to $V_{REF}$, and the bottom plates of $C_{b9}, C_{b8}, C_{b7}, C_{d9}, C_{d8}$, and $C_{d7}$ are connected to GND. The bottom plates of the rest capacitors connected to $V_{CM}$. Thus, during the quantization process, for the first three voltage transitions, only a single capacitor's bottom-plate voltage switch is needed on each side of the DAC capacitor array. The entire quantization process consists of three stages: 1) bypass window switching operation; 2) $V_{CM}$-based switching operation; and 3) monotonic switching operation, as shown in Fig. 5.

1) The sampled $V_p$ and $V_n$ are directly compared. If $V_p > V_n$, then D [9] =1, the bottom plates of $C_{a9}$ and $C_{d9}$ are connected to GND and $V_{REF}$, respectively. Conversely, if $V_p < V_n$, D [9] =0, the bottom plates of $C_{b9}$ and $C_{e9}$ are connected to $V_{REF}$ and GND, respectively. Then, a second voltage comparison is performed. Since D [8]

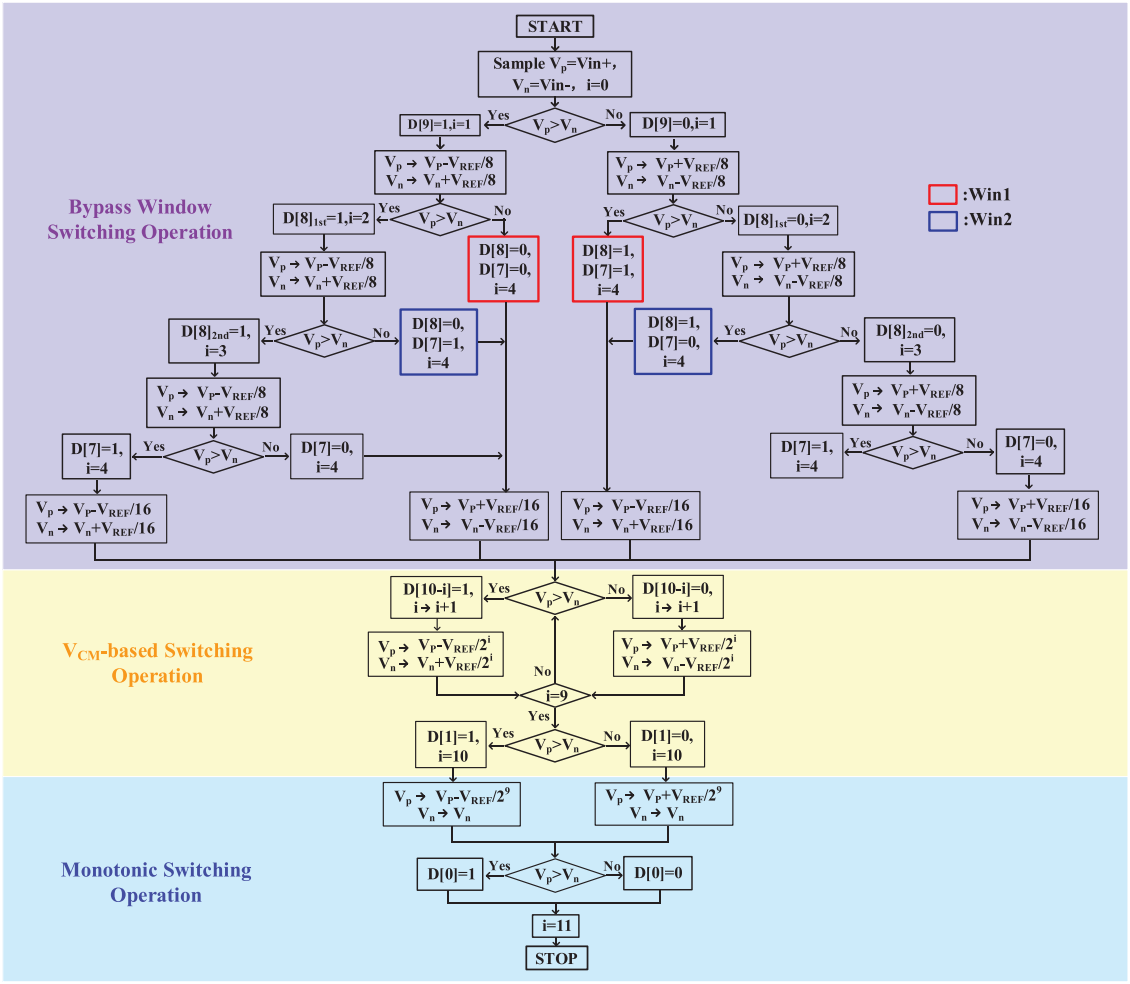



Fig. 5. Quantization process of the proposed SAR ADC.

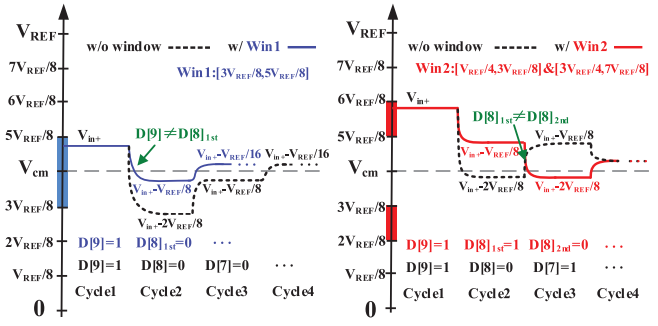



Fig. 6. Operating principles of the bypass window. (a) Operating principle of Win1. (b) Operating principle of Win2.

is quantized by the voltage flipping of 64C, which is "32 + 32C," we define the 1st 32 C quantization value as D [8]$_{1st}$ and the 2nd 32C quantization value as D [8]$_{2nd}$. So, D [8] is formed by combining D [8]$_{1st}$ and D [8]$_{2nd}$.

2) As shown in Fig. 6(a), if D [9] =1 and D [8]$_{1st}$ = 0, the XOR logic of D [9] and D [8]$_{1st}$ is 1. It means that the polarity of $V_p$ has changed after the voltage switching of the 1st 32C. It can be determined that the range of $V_{in+}$ is [$V_{CM}$, 5$V_{REF}$/8], within Win1. At this point, the conventional $V_{CM}$-based SAR ADC quantizes $V_{in+}$ to obtain the following values: D [9] =1, D [8] =0, and D [7] =0. Therefore, the voltage switching for $C_{a8}$, $C_{a7}$, $C_{b8}$, $C_{b7}$, $C_{d8}$, $C_{d7}$, $C_{e8}$, and $C_{e7}$ can be skipped, and D [8] =0, D [7] =0. Then, $C_{a6}$ and $C_{b6}$ are connected to $V_{REF}$ and $C_{d6}$ and $C_{e6}$ are connected to GND. After that, the quantization is performed according to the normal SAR logic, as shown by the diagram of Fig. 7(a).

Similarly, if D [9] =0 and D [8]$_{1st}$ =1, the XOR logic of them is 1, it can be determined that the range of $V_{in+}$ is [3$V_{REF}$/8, $V_{CM}$], within Win1. Therefore, the voltage switching for $C_{a8}$, $C_{a7}$, $C_{b8}$, $C_{b7}$, $C_{d8}$, $C_{d7}$, $C_{e8}$, and $C_{e7}$ can be skipped, and so, D [8] =1, D [7] =1. Then, $C_{a6}$ and $C_{b6}$ are connected to GND, and $C_{d6}$ and $C_{e6}$ are connected to $V_{REF}$. After that, the quantization is as shown in the timing diagram in Fig. 7(b).

3) As shown in Fig. 6(b), if D [9] =1 and D [8]$_{1st}$ =1, connect $C_{a8}$ to GND and $C_{d8}$ to $V_{REF}$, then perform voltage comparison to obtain D [8]$_{2nd}$. If D [8]$_{2nd}$ =0 and the XOR logic of D [8]$_{2nd}$ and D [8]$_{1st}$ is 1, it indicates that $V_{in+}$ falls within the range of [5$V_{REF}$/8, 6$V_{REF}$/8], which is within Win2. At this point, the conventional

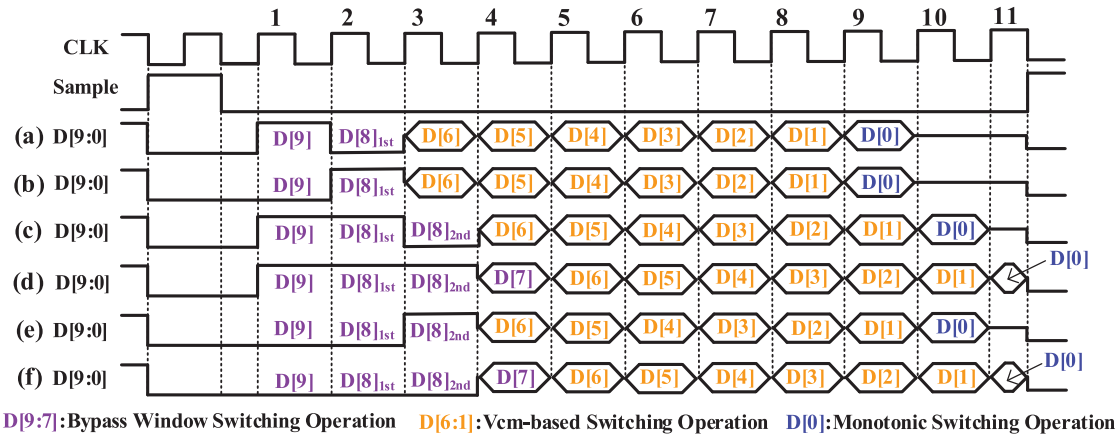



Fig. 7. Timing diagrams of the proposed ADC quantization process. (a) Quantization of $V_{in+}$ within the range [$V_{CM}$, $5V_{REF}/8$]. (b) Quantization of $V_{in+}$ within the range [$3V_{REF}/8$, $V_{CM}$]. (c) Quantization of $V_{in+}$ within the range [$5V_{REF}/8$, $6V_{REF}/8$]. (d) Quantization of $V_{in+}$ outside the ranges of Win1 and Win2. (e) Quantization of $V_{in+}$ within the range [$2V_{REF}/8$, $3V_{REF}/8$]. (f) Quantization of $V_{in+}$ outside the ranges of Win1 and Win2.

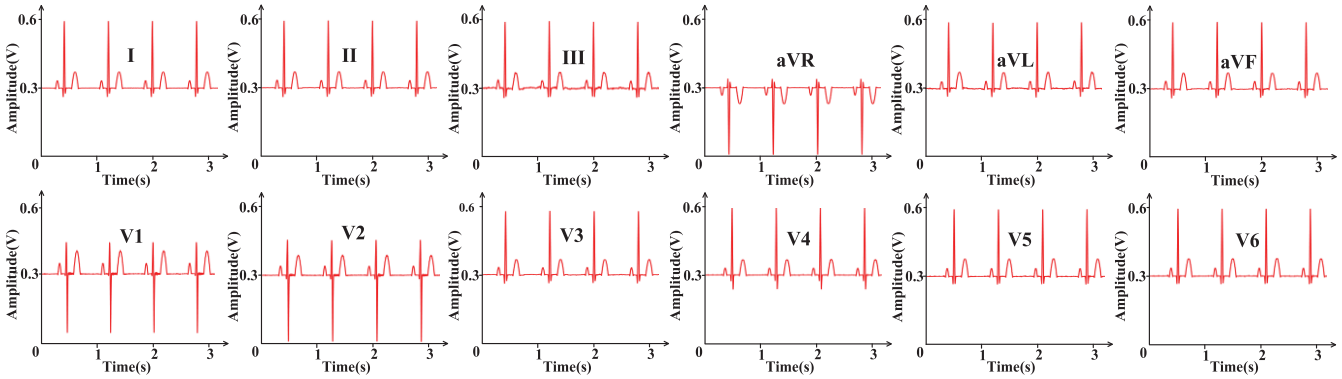



Fig. 8. 12-lead ECG signals generated by the ECG simulator.

$V_{CM}$-based SAR ADC quantizes $V_{in+}$ to obtain the following values: D [9] =1, D [8] =0, and D [7]=1.

Therefore, the voltage switching for $C_{a7}, C_{b7}, C_{d7}$, and $C_{e7}$ can be skipped with D [8] =0 and D [7] =1. Instead, $C_{a6}$ and $C_{b6}$ are connected to $V_{REF}$, and $C_{d6}$ and $C_{e6}$ are connected to GND. After that, the quantization is shown in the timing diagram Fig. 7(c). If D $[8]_{2nd}$ =1, D [8] is set to 1, and the voltage is quantized as shown in the timing diagram Fig. 7(d).

1) [4] If D [9] =0 and D $[8]_{1st}$ =0, connect $C_{b8}$ to $V_{REF}$ and $C_{e8}$ to GND, then perform voltage comparison to obtain D $[8]_{2nd}$. If D $[8]_{2nd}$ =1 and the XOR logic of D $[8]_{2nd}$ and D $[8]_{1st}$ is 1, it indicates that $V_{in+}$ falls within the range of [$2V_{REF}/8$, $3V_{REF}/8$], which is within Win2. Therefore, the voltage switching for $C_{a7}, C_{b7}, C_{d7}$, and $C_{e7}$ can be skipped with D [8] =1 and D [7] =0. Instead, $C_{a6}$ and $C_{b6}$ are connected to GND, and $C_{d6}$ and $C_{e6}$ are connected to $V_{REF}$. Then, the quantization is shown in the timing diagram Fig. 7(e). If D $[8]_{2nd}$ =0, D [8] is set to 0, and the voltage is quantized as shown in the timing diagram Fig. 7(f).
2) [5] For the comparison result of the second LSB: if $V_p > V_n$, D [1] =1 and the bottom plate of $C_{b1}$ is connected to GND. Conversely, if $V_p < V_n$, D [1] =0 and the bottom plate of $C_{b1}$ is connected to $V_{REF}$. Then, the comparison between $V_p$ and $V_n$ is performed to obtain D[0] and complete the entire quantization cycle.

### B. Analysis of 12-Lead ECG Signals

The 12-lead ECG signals are generated by ECG simulator SKX-2000 C+. It mainly includes: I, II, III, aVR, aVL, aVF, V1, V2, V3, V4, V5, and V6, as shown in Fig. 8. Due to the different sources of each ECG signal, there are differences in waveform and amplitude. These signals are all transformed by the analog front-end module into differential signals with amplitudes and common-mode voltages that are tailored for the designed SAR ADC.

The statistics for each sampled ECG signal can be obtained by taking 40000 sampled points, including the number and probability of points falling into Win1, Win2, and outside the window (Out), as shown in Table I. For example, taking the quantization of the V1 signal with the proposed ten-bit ADC, 80.51% of the V1 signal falls within Win1, as shown in Fig. 9. In the quantization process, we can directly assign values to D [8] and D [7], and this eliminates the voltage switching power consumption associated with capacitors $C_{a8}, C_{a7}, C_{b8}, C_{b7}, C_{d8}, C_{d7}, C_{e8}$, and $C_{e7}$, and the comparator only needs to perform nine comparisons. For the V1 signal, 14.31% falls within the Win2. In this quantization step, we can

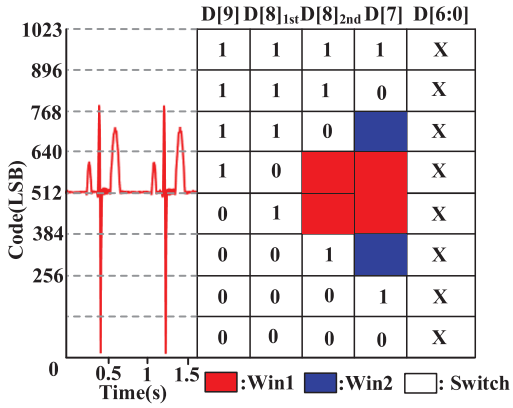



Fig. 9. Quantization of ECG signal V1 by the proposed SAR ADC.

TABLE I
STATISTICS FOR THE SAMPLING OF 12-LEAD ECG SIGNALS

| ECG | Win1(present) | Win2(present) | Out (present) |
|---|---|---|---|
| I | 36587(91.47%) | 1048(2.62%) | 2365(5.91%) |
| II | 36628(91.57%) | 1041(2.6%) | 2331(5.83%) |
| III | 36689(91.72%) | 996(2.49%) | 2315(5.79%) |
| aVR | 36640(91.6%) | 1015(2.54%) | 2345(5.86%) |
| aVL | 36501(91.25%) | 1159(2.9%) | 2340(5.85%) |
| aVF | 36521(91.3%) | 1118(2.8%) | 2361(5.9%) |
| V1 | 32205(80.51%) | 5724(14.31%) | 2071(5.18%) |
| V2 | 32638(81.6%) | 5360(13.4%) | 2002(5%) |
| V3 | 36520(91.3%) | 1161(2.9%) | 2319(5.8%) |
| V4 | 36744(91.86%) | 953(2.38%) | 2303(5.76%) |
| V5 | 36317(90.79%) | 1278(3.2%) | 2405(6.01%) |
| V6 | 36287(90.72%) | 1212(3.03%) | 2501(6.25%) |

directly assign a value to D [7], which eliminates the voltage switching power consumption for capacitors $C_{a7}, C_{b7}, C_{d7}$, and $C_{e7}$, and the comparator performs ten comparisons, and 5.18% falls outside the windows. In this quantization step, the comparator needs to perform 11 comparisons.

According to the statistics, it is found that the probability of the sampled 12-lead signals falling into the "Win1+ Win2" range is over 93.75%. This means that the proposed bypass window SAR ADC can effectively reduce the power consumption for the quantization of 12-lead ECG signals.

### C. Analysis of Power Consumption

For an N-bit SAR ADC, if the code values are uniformly distributed, the average power consumption for the capacitor array monotonic switching scheme [23] and the $V_{CM}$-based switching scheme [24] during the quantization process can be derived as follows, respectively

$$E_{\text{Monotonic}} = \sum_{i=1}^{N-1} \left(2^{N-i-2}\right) \text{CV}_{\text{REF}}^2 \tag{1}$$

$$E_{V_{\text{CM}}-\text{based}} = \sum_{i=1}^{N-1} \left(2^{N-2i-2}\right) \left(2^{i}-1\right) \text{CV}_{\text{REF}}^2. \tag{2}$$

For the proposed quantization scheme, the power consumption of the capacitor array can be mainly categorized into three cases.

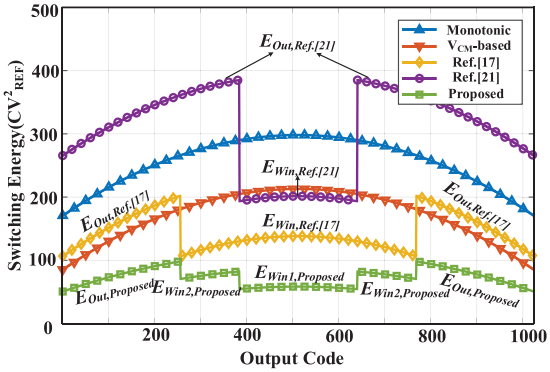



Fig. 10. Average switching power of ten-bit DACs.

1) When the signals fall outside the windows, that is in the range of [0, $2V_{\text{REF}}/8$] and [$6V_{\text{REF}}/8$, $V_{\text{REF}}$], the average power consumption of the DAC for quantization can be formulated as

$$E_{\text{Out,Proposed}} = \sum_{i=1}^{N} \left(2^{N-2i-1}\right) \left(2^{i-1}-1\right) \text{CV}_{\text{REF}}^2 - \left(2^{-N-1}+2^{N-7}\right) \text{CV}_{\text{REF}}^2. \tag{3}$$

2) When the signals fall within the Win1, that is in the range of [$3V_{\text{REF}}/8$, $5V_{\text{REF}}/8$], the average power consumption of the DAC for quantization can be formulated as

$$E_{\text{Win1,Proposed}} = \sum_{i=3}^{N} \left(2^{N-2i-1}\right) \left(2^{i-1}-1\right) \text{CV}_{\text{REF}}^2 - \left(2^{-N-1}-2^{N-8}\right) \text{CV}_{\text{REF}}^2. \tag{4}$$

3) When the signals fall within the Win2, that is in the range of [$2V_{\text{REF}}/8$, $3V_{\text{REF}}/8$] and [$5V_{\text{REF}}/8$, $6V_{\text{REF}}/8$], the average power consumption of the DAC for quantization can be formulated as

$$E_{\text{Win2,Proposed}} = \sum_{i=1}^{N} \left(2^{N-2i-1}\right) \left(2^{i-1}-1\right) \text{CV}_{\text{REF}}^2 - \left(2^{-N-1}+2^{N-7}\right) \text{CV}_{\text{REF}}^2. \tag{5}$$

When $N = 10$, the power consumption of DAC quantization is shown in Fig. 10. Specifically, $E_{\text{Win1,Proposed}}$ = 57.083 CV2 REF, $E_{\text{Win2,Proposed}}$ = 77.083 CV2 REF, and $E_{\text{Out,Proposed}}$ = 77.083 CV2 REF. To facilitate a power consumption comparison, the original voltage switching schemes in [17] and [21] are retained. Specifically, the range of bypass window in [17] is set to [$V_{\text{REF}}/4$, $3V_{\text{REF}}/4$], while the range of bypass window in [21] is set to [$3V_{\text{REF}}/8$, $5V_{\text{REF}}/8$]. For [17], the power consumption within the bypass window is $E_{\text{Win,Ref.[17]}}$ = 127.5 CV2 REF, and the outside is $E_{\text{Out,Ref.[17]}}$ = 159.5 CV2 REF. Similarly, for [21], the power consumption within the bypass window is $E_{\text{Win,Ref.[21]}}$ = 198.752 CV2 REF, and the outside is $E_{\text{Out,Ref.[21]}}$ = 337.169 CV2 REF.

To more precisely assess the power consumption of different bypass window switching schemes when quantizing 12-lead ECG signals, the weighted average power consumption $E_{\text{avg}}$

TABLE II

DAC POWER CONSUMPTION STATISTICS FOR THE BYPASS WINDOW QUANTIZATION SCHEMES PROPOSED IN [17] AND [21], AND THIS ARTICLE WHEN QUANTIZING 12-LEAD ECG SIGNALS; COMPARISON COUNT AND MEASURED POWER CONSUMPTION STATISTICS FOR THE PROPOSED BYPASS WINDOW SCHEME WHEN QUANTIZING 12-LEAD ECG SIGNALS

| ECG | I | II | III | aVR | aVL | aVF | V1 | V2 | V3 | V4 | V5 | V6 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $E_{avg,Ref.[17]}$ ($CV^2_{REF}$) | 129.4 | 129.4 | 129.4 | 129.4 | 129.4 | 129.4 | 129.2 | 129.1 | 129.4 | 129.3 | 129.4 | 129.5 |
| $E_{avg,Ref.[21]}$ ($CV^2_{REF}$) | 210.6 | 210.4 | 210.2 | 210.4 | 210.9 | 210.8 | 225.8 | 224.2 | 210.8 | 210 | 211.5 | 211.6 |
| $E_{avg,Proposed}$ ($CV^2_{REF}$) | 58.8 | 58.8 | 58.7 | 58.8 | 58.8 | 58.8 | 61 | 60.8 | 58.8 | 58.7 | 58.9 | 58.9 |
| $M_{avg,Proposed}$ | 9.14 | 9.14 | 9.14 | 9.14 | 9.15 | 9.15 | 9.25 | 9.23 | 9.15 | 9.14 | 9.15 | 9.16 |
| $P_{measured,Proposed}$ (nW) | 12.68 | 12.61 | 12.64 | 12.82 | 12.88 | 12.61 | 12.72 | 12.66 | 12.61 | 12.52 | 12.6 | 12.57 |

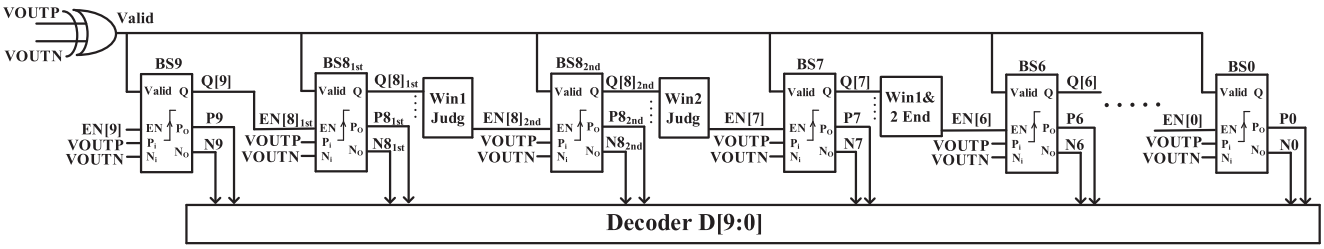



Fig. 11. Logic circuit diagram of the proposed SAR ADC.

is deemed a more appropriate metric. For the proposed bypass window, the weighted average power consumption $E_{\text{avg,Proposed}}$ is calculated as follows:

$$E_{\text{avg,Proposed}} = \alpha_1 E_{\text{Win1,Proposed}} + \alpha_2 E_{\text{Win2,Proposed}} + \alpha_3 E_{\text{Out,Proposed}} \quad (6)$$

where $\alpha_1, \alpha_2$, and $\alpha_3$ represent the probabilities of the signal falling into Win1, Win2, and Out, respectively, and $\alpha_1 + \alpha_2 + \alpha_3 = 1$.

For [17], the bypass window range is the aggregate of Win1 and Win2. Consequently, the weighted average power consumption $E_{\text{avg,Ref.[17]}}$ is expressed as

$$E_{\text{avg,Ref[17]}} = (\alpha_1 + \alpha_2) E_{\text{Win,Ref[17]}} + \alpha_3 E_{\text{Out,Ref[17]}}. \quad (7)$$

For [21], the bypass window range coincides with Win1. Hence, the weighted average power consumption $E_{\text{avg,Ref.[21]}}$ is formulated as

$$E_{\text{avg,Ref[21]}} = \alpha_1 E_{\text{Win,Ref[21]}} + (\alpha_2 + \alpha_3) E_{\text{Out,Ref[21]}}. \quad (8)$$

Similarly, despite the fact that the proposed bypass window scheme necessitates an additional comparison cycle, the weighted average number of comparisons $M_{\text{avg,Proposed}}$ when processing 12-lead ECG signals can be represented as

$$M_{\text{avg,Proposed}} = \alpha_1 M_{\text{Win1,Proposed}} + \alpha_2 M_{\text{Win2,Proposed}} + \alpha_3 M_{\text{Out,Proposed}}. \quad (9)$$

For the proposed quantization scheme, $M_{\text{Win1,Proposed}} = 9$, $M_{\text{Win2,Proposed}} = 10$, and $M_{\text{Out,Proposed}} = 11$.

As indicated in Table II, based on the weighted calculations and the statistical distribution of 12-lead ECG signals, $E_{\text{avg,Proposed}}$ is lower than both $E_{\text{avg,Ref.[17]}}$ and $E_{\text{avg,Ref.[21]}}$.

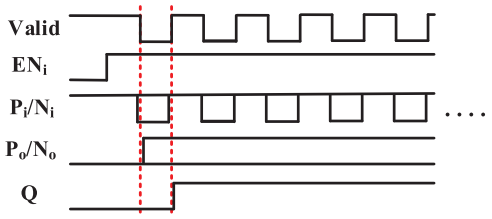



Fig. 12. Timing waveform diagram for the BS module.

Similarly, the weighted average number of comparisons $M_{\text{avg,Proposed}}$ remains around 9, thereby saving approximately one comparison cycle. It can be determined that the proposed bypass window quantization scheme offers a significant low-power advantage when quantifying 12-lead ECG signals.

### D. Design of Logic Control Circuits

For the proposed SAR ADC structure, the logic circuit diagram is shown in Fig. 11 and it mainly consists of the SAR logic and the encoding module. The SAR logic utilizes the XOR logic of the comparator outputs VOUTP and VOUTN to generate the control signal Valid. The sampling clock is inverted and used as EN [9]. Then, each bit-slice (BS) module is sequentially enabled by Q[N] = EN[N −1] to latch the outputs of the comparator [25].

In Fig. 12, the timing diagram of the BS module is depicted: when $EN_i = 1$, if valid =0, then $P_O = P_i$, $N_O = N_i$, and $Q = 0$; when valid transitions from 0 to 1, both $P_O$ and $N_O$ retain their previous states, while $Q$ is set to 1. When $EN_i = 0$, $Q$, $P_O$, and $N_O$ are all reset to 0. As shown in Fig. 13, the circuit of the BS is composed entirely of MOS transistors with a unit width-to-length ratio. Due to the leakage current, the drain

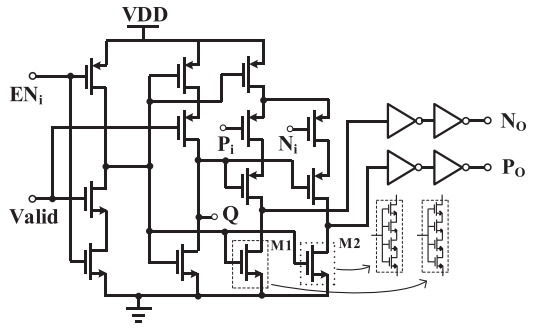



Fig. 13. Schematic circuit of BS module.

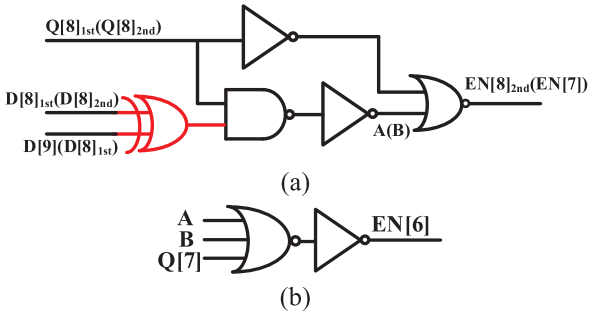



Fig. 14. (a) Circuitry of the Win1(2) judge module. (b) Circuitry of the Win1&2 end module.

voltages of M1 and M2 may change from high level to low level during the entire SAR ADC conversion cycle, resulting in logic errors. In order to achieve correct logic functions of BS module under the three process corners (ff, tt, and ss), M1 and M2 transistors use four-stacked nMOS with unit size to reduce leakage current effect.

Based on bypass window switching operation during the quantization process, in the Win1 judge module, if D $[8]_{1st}$ differs from D [9], the SAR logic should bypass the BS8$_{2nd}$ module, meaning that EN $[8]_{2nd}$ should remain constantly at 0. If the XOR result of D $[8]_{1st}$ and D [9] is directly used as EN $[8]_{2nd}$, when the BS8$_{1st}$ module outputs D $[8]_{1st}$, and the XOR result of D $[8]_{1st}$ and D [9] is 1, then EN $[8]_{2nd}$ will be set to 1. This will directly activate the BS8$_{2nd}$ module, resulting in a logical error. Therefore, $Q$ $[8]_{1st}$ is introduced as the control signal for EN $[8]_{2nd}$. When $Q$ $[8]_{1st}$ =0, EN $[8]_{2nd}$ must be held at 0. When $Q$ $[8]_{1st}$ =1, if the XOR result of D $[8]_{1st}$ and D [9] is 1, EN $[8]_{2nd}$ =0; if the XOR result is 0, EN $[8]_{2nd}$ =1. Thus, based on the relationship between the input variables $Q$ $[8]_{1st}$, D $[8]_{1st}$, and D [9], and the output result EN $[8]_{2nd}$, the expression for Win1 Judge can be derived using a Karnaugh map, resulting in the following expression:

$$\mathrm{EN}\,[8]_{2nd} = \overline{(D\,[9] \oplus D\,[8]_{1st}) \cdot Q\,[8]_{1st} + \overline{Q\,[8]_{1st}}}. \qquad (10)$$

Similarly, the input variables for the Win2 judge module are $Q$ $[8]_{2nd}$, D $[8]_{2nd}$, and D $[8]_{1st}$, and the output result is EN [7]. The circuit structure of the Win1(2) judge module is depicted in Fig. 14(a). There are three inputs for the Win1&2 end module and they are A, B, and $Q$ [7], as illustrated in Fig. 14(b). When any one of these inputs is 1, the output EN [6] is set to 1.

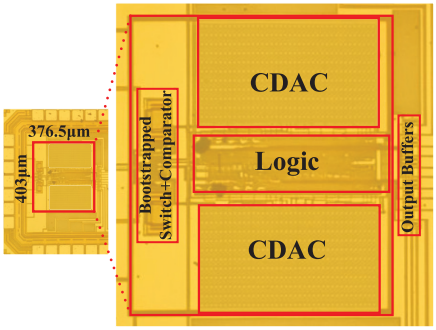



Fig. 15. Microphotography of the proposed SAR ADC.

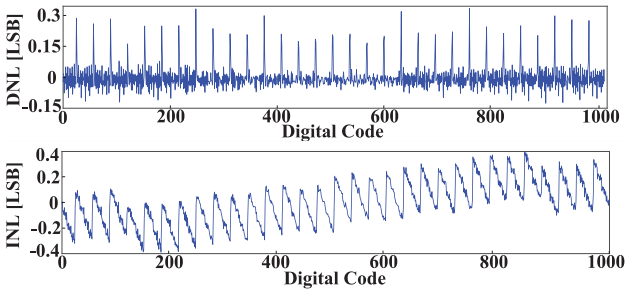



Fig. 16. Measurement results of DNL and INL.

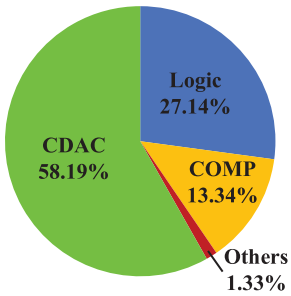



Fig. 17. Power consumption distribution of each block.

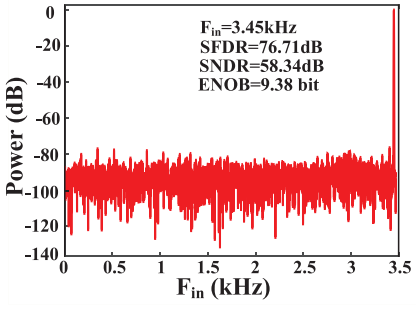
## IV. Measurement Results and Discussion

The proposed ten-bit bypass window SAR ADC is designed based on a standard 180-nm 1P6M CMOS process. Considering the limitations of quantizer power consumption, switching noise, and unit capacitor mismatch, this work employs a unit MIM capacitor array with a unit capacitance of approximately 19 fF. In the layout design, a common-centroid structure is employed, and dummy capacitors are introduced to reduce the impact of mismatch errors and minimize mismatch. Fig. 15 shows the microphotograph of the proposed ADC and the core area is 403 × 376.5 $\mu m^2$. In Fig. 16, the measurement results show that the differential nonlinearity (DNL) is −0.12/+0.33 LSB and integral nonlinearity (INL) is −0.39/+0.39 LSB.

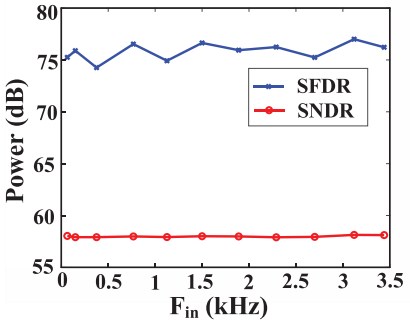
When the power supply is 0.6 V, the sampling rate $F_S$ reaches 6.94 kHz. If the input signal is a 1.17-$V_{PP}$ 3.45-kHz sine wave, the total power consumption of the ADC is 15.61 nW. As depicted in Fig. 17, the CDAC, logic circuits, comparator, and others constitute 58.19%, 27.14%, 13.34%, and 1.33% of the total power consumption, respectively.

TABLE III
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE-OF-THE-ART WORKS

| | TVLSI' 22[26] | TBCAS' 24[27] | TCAS-I' 20[28] | SJ' 20[29] | TCAS-II' 23[21] | TCAS-I' 19[30] | VLSI Circuits' 15[11] | **This work** | |
|---|---|---|---|---|---|---|---|---|---|
| Process | 130nm | 55nm | 180nm | 180nm | 180nm | 180nm | 180nm | **180nm** | |
| Supply (V) | 0.6 | 1.2 | 0.7 | 1 | 0.6 | 0.6 | 0.6 | **0.6** | |
| ADC Type | SAR | LC+SAR | SAR | NS-SAR | SAR | SAR | SAR | **SAR** | |
| Bypass Window | Yes | Yes | Yes | No | Yes | No | Yes | **Yes** | |
| Fs (kHz) | 10 | - | 100 | 10 | 50 | 200 | 100 | **6.94** | |
| Unit Capacitor(fF) | 65 | - | 6 | - | 20.28 | 31.1 | - | **19** | |
| C-2C | Yes | No | No | No | No | No | No | **No** | |
| Resolution (bit) | 10 | 4+4 | 12 | - | 12 | 10 | 8 | **10** | |
| ENOB (bit) | 9.38 | - | - | 10.5 | 10.12 | 9.16 | 7.5 | **9.38** | |
| SNDR(dB) | - | 51.2 @0.2kHz | 60.9 | 65 | 62.7 | 56.91 | 46.9 | **58.24** | |
| SFDR(dB) | - | - | 80 | - | 82.4 | 68.56 | 63.8 | **76.71** | |
| Power (nW) | 40-380 | 440 | 1500 | 90 | 1540 | 68.12 | 120 | **15.61 (sin)** | **12.66 (ECG)** |
| FoM(fJ/Conv.-step) | 6-56.6 | 29.7 | 16.6 | 50 | 27.7 | 15.38 | 6.6 | **3.38 (sin)** | **2.74 (ECG)** |




(a)




(b)

Fig. 18. Measurement results of the proposed SAR ADC. (a) FFT spectrum at $F_{in}$ = 3.45 kHz. (b) Dynamic performance versus $F_{in}$ within the Nyquist input range.

Fig. 18(a) displays the fast Fourier transform (FFT) spectrum plot of the ADC output with 16384 points when $F_{in}$ = 3.45 kHz, with an effective number of bit (ENOB) of 9.38 bits. Additionally, the signal-to-noise and distortion ratio (SNDR) and the spurious-free dynamic range (SFDR) can achieve 58.34 and 76.71 dB, respectively. Fig. 18(b) presents the statistical results of SNDR and SFDR within the Nyquist input range, showing no significant variations. According to the FoM defined as Power/($2^{ENOB*}$ $F_S$), the FoM of the proposed SAR ADC is approximately 3.38 fJ/Conv.-step.

For 12-lead ECG signals, the quantization power consumption of each ECG signal, denoted as $P_{measured,Proposed}$, can be measured, with a summary provided in the last row of Table II. Given that ECG signals are predominantly concentrated within the Win1 and Win2 ranges, it is possible to bypass some of the DAC's voltage switching, comparison operations, and digital circuit operations during quantization, thereby resulting in lower power consumption. The average power consumption is 12.66 nW. Subsequently, the FoM is calculated to be 2.74 fJ/Conv.-step.

Table III provides a performance comparison between the proposed work and state-of-the-art ADC circuits for ECG applications. It can be observed that the proposed ADC exhibits greater power efficiency advantages during the quantization process compared to other SAR ADCs, particularly when quantifying 12-lead ECG signals, with a more pronounced advantage in the FoM. For the noise-shaping (NS) SAR ADCs that rely on oversampling, although noise shaping can enhance quantization accuracy, the standard Nyquist SAR ADCs are more advantageous for achieving ten-bit quantization precision. For the level-crossing (LC) ADCs that can dynamically adjust the quantization rate in response to ECG signal activity, they can reduce power consumption by compressing quantization data, thereby lowering the power usage of the entire ECG acquisition system. However, compared with the LC ADCs, the proposed SAR ADC still demonstrates a significant power consumption advantage.

## V. CONCLUSION

In this article, a bypass window SAR ADC structure based on multiple splits of the MSB capacitor is proposed for

the characteristics of 12-lead ECG signals to minimize the power consumption. By introducing redundant capacitors for quantization, the total capacitor array is reduced by half. Two bypass windows and simple XOR judgment module can skip some intermediate quantization steps for the signals within Win1 or Win2 range, achieving low power consumption. The proposed structure is implemented using a standard 180-nm CMOS technology. The measurement results can achieve an ENOB of 9.38 bits and an SFDR of 76.71 dB with a 0.6-V supply at 6.94 kS/s. For a sine wave input, the quantization power consumption is 15.61 nW, and the FoM is 3.38 fJ/Conv.-step. However, for 12-lead ECG signals, the average power consumption is 12.66 nW, with an FoM of only 2.74. fJ/Conv.-step. This indicates that the proposed SAR ADC is highly suitable as a data converter for the low-power wearable 12-lead ECG acquisition systems.

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