A Low-Voltage Wide Swing Image Sensor with Simultaneous Energy Harvesting and Imaging Modes

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***Abstract*—This paper proposes a CMOS image sensor that can achieves imaging and energy harvesting simultaneously without introducing additional P-N junctions in the pixel array. The proposed pixel utilizes the vertical N+/P-well/DNW/P-sub structures as photodiodes based on a standard 180nm CMOS mixed-signal process. The N+/P-well is used for imaging, while the P-well/DNW and DNW/P-sub are used for energy harvesting with shorting P-well and P-sub together. Moreover, the traditional 4T pixel has been improved by using CMOS pairs as the switches and zero-threshold NMOS as the source follower. The rail-to-rail pixel output swing can be achieved. Simulation results show that the dynamic range is increased by 13.4dB compared with the traditional 4T pixel. Single pixel occupies an area of 11×13 μm^2 with a fill factor of 72%. An image sensor with 32×32 proposed pixel array and a dual-channel PWM quantizer is designed. Simulation results show that the average power consumption of the image sensor is approximately 6.7μW@2MHz.**

Key words*——*image sensor, energy harvesting, wide swing, low voltage, PWM

I. INTRODUCTION

In IoT applications, sensors are required to be low power or even self-powered in order to increase their life time. Pixels with energy harvesting (EH) capability is an important research direction for low-power image sensors. In recent years, for image sensors with EH capability, energy harvesting mode and imaging mode cannot be realized simultaneously [1-4]. Therefore, most energy harvesting imagers switch from imaging mode to energy harvesting mode in a time-sharing manner, which reduces energy harvesting time. Cevik placed an additional PN junction in parallel with the existing imaging diode to achieve simultaneous energy harvesting and imaging [5]. However, this method inevitably leads to a decrease in the pixel fill factor, resulting in low utilization of the pixel area. The pixel in [6] can work simultaneously in energy harvesting and imaging modes. However, this structure uses the substrate as the energy harvesting output terminal, meaning that all NMOS in the circuit system need to use DNW NMOS to isolate from the substrate. This brings more challenges to the design of subsequent circuits.

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In the low power techniques of image sensors, reducing the power supply voltage is an important method to reduce power consumption. However, after reducing the voltage supply, the output voltage swing decreases significantly due to the threshold voltage of the transistors, therefore the dynamic range is reduced. Weng uses two Schmitt triggers to detect the V_{PD} of the photodiode and control the P7 and P6 current sources when V_{PD} is low, thereby improving the dynamic range [7]. However, this structure does not fundamentally solve the decrease in output swing caused by the threshold voltage of N7 MOS, and eventually achieves only a 42dB dynamic range. The complementary pixel structure proposed in [8] achieves rail-to-rail pixel output swing, but the structure is complicated and the fill factor is only 40%. Many low-voltage image sensors adopt PWM digital pixels [9]. But the PWM pixel structure reduces the fill factor due to the use of in-pixel comparators and the static power consumption is increased.

This paper proposes an image sensor that can work simultaneously in energy harvesting and imaging modes and achieve higher output swing under 1V supply. The paper is structured as follows: Section II discusses the circuit structure and operating principles. Section III provides the simulation verification results. and Section IV concludes the paper.

II. DESIGN OF THE PROPOSED IMAGE SENSOR

The proposed low voltage image sensor system structure is shown in Fig. 1. The pixel array adopts a 32×32 and the shutter mode is a rolling shutter. The pixel array is exposed row by row by the controller. The change of light intensity is turned into the change of pixel output voltage. The pixel outputs are divided into odd and even column readouts, which are sent to two channels of the PWM quantizer respectively under the control of the transmission units. The upper channel of the PWM quantizer works at a high RST level, and the lower channel works at a low RST level. The PWM quantizer converts the analog voltage signal output from the pixel array into a pulse width signal. The two channel outputs of the PWM quantizer are alternately output under the control of the transmission gates, forming the final PWM output.

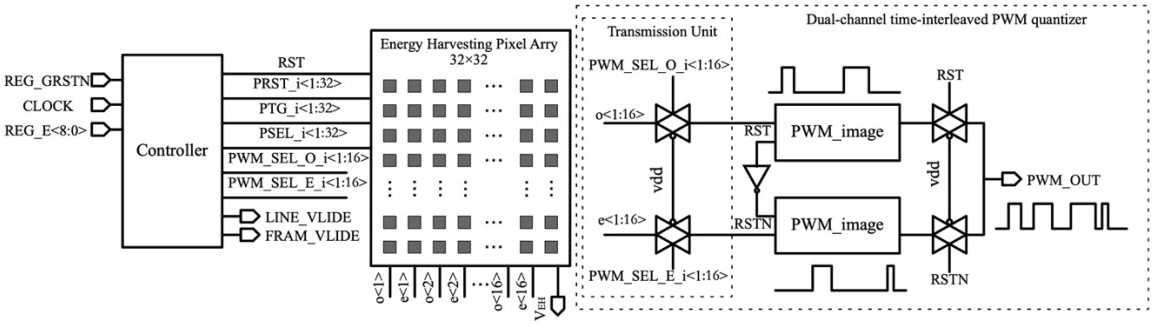

Fig.1 The proposed low voltage image sensor system architecture.

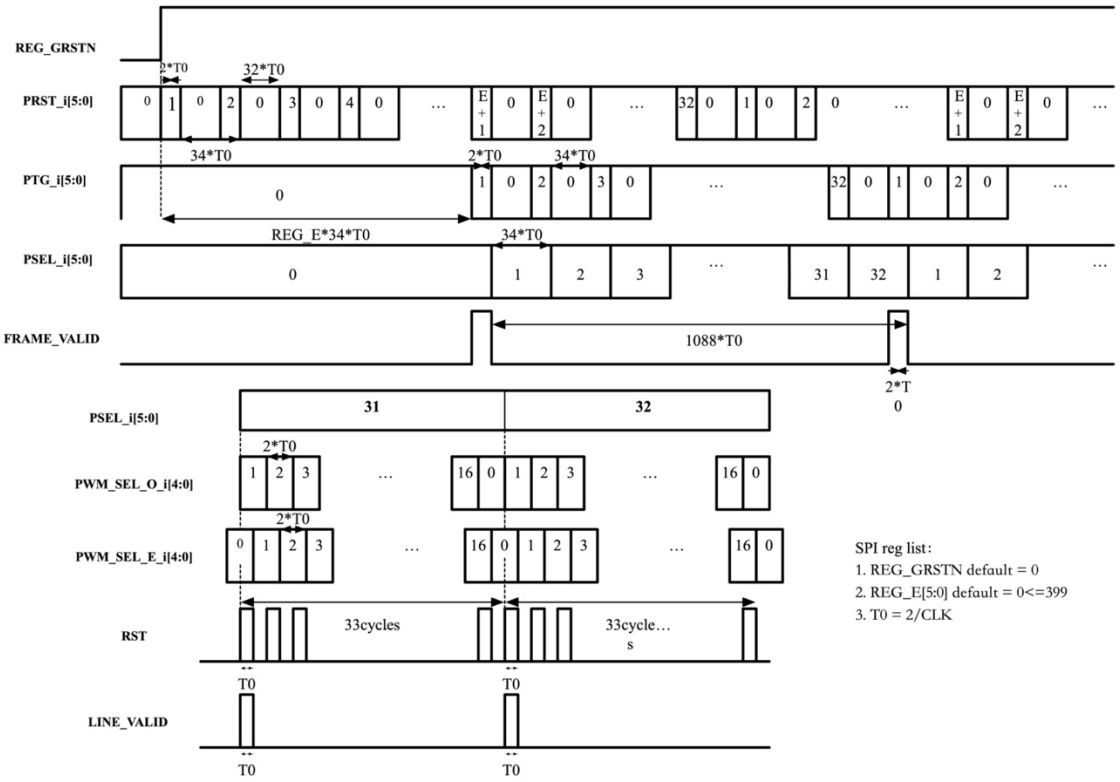

Fig .2 Image sensor timing diagram.

A. Architecture of the proposed image sensor

Fig. 2 shows the timing control diagram of the proposed image sensor. REG_GRSTN is the system reset signal, which resets all registers at low level and allows the controller to work normally at high level. PRST_i[5:0] are the row reset signals of the pixel array. For a 32×32 pixel array, 32 row reset signals are needed, which can be generated by a decoder using the 6-bit binary input PRST_i[5:0]. PTG_i[5:0] are the row exposure control signals of the pixel array, with 34×T0 being the minimum unit. The exposure time can be adjusted according to the control input REG_E[5:0], with a maximum of 1088×T0. The rising edges of PTG_i[5:0] are aligned with those of PRST_i[5:0]. PSEL_i[5:0] are the row output signals of the pixel array. Their rising edges are aligned with the falling edges of PTG_i[5:0]. PWM_SEL_O_i[4:0] and PWM_SEL_E_i[4:0] control the transmission of the pixel array signals, sending odd and even column signals to the PWM quantizer respectively. RST is the control clock of the PWM_image and exists only during PESE's high levels. LINE_VALID is the line sync signal, indicating the start of a row data readout when high. FRAM_VALID is the frame synchronization signal. Its rising edge indicates the start of a frame.

B. The proposed pixel circuit

Fig. 3 shows the proposed pixel structure for wide-swing simultaneous energy and imaging modes. The proposed photodiodes in the pixel utilizes the vertical N+/P-well/DNW/P-sub structure by connecting P-well and P-substrate to the ground. N+ and P-well form a photodiode for imaging. P-well and P-substrate form the second photodiode with DNW for energy harvesting [10]. Compared with the time-sharing photodiode in [1-4], it can work in energy harvesting and imaging modes at the same time. Due to the use of vertically stacked dual photodiodes, no additional area is required, which helps to improve the fill factor. The vertically stacked dual photodiodes share the P-well layer, which is grounded. DNW is used as the energy harvesting output terminal, which can generate a negative voltage respect to the ground. This negative voltage could be converted to a positive stable voltage supply through energy harvesting circuits. Compared with [6] using P-substrate as the energy harvesting terminal, this work does not DNW NMOS for the circuit system, providing more free space for circuit design.

The photodiode is responsible for transforming photon energy into electron potential energy, causing electrons to move in a specific direction and generate an electric current.

As a result, the short-circuit current I_{sc} serves as an indicator of the photodiode's ability to convert light into electricity. The

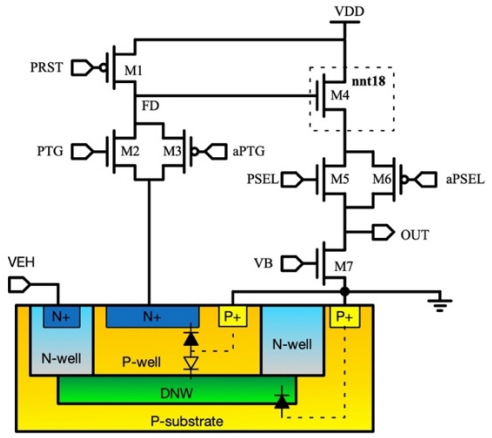

Fig. 3 The proposed pixel architecture for wide-swing simultaneous energy and imaging modes.

short-circuit current density per unit area J_{sc} can be expressed as (1).

$$J_{SC} = e\int_0^{\infty} QE\,(\lambda, d)\Phi_{inc}(\lambda)d\lambda \qquad (1)$$

where e represents the electron charge, λ is wavelength and d is the penetration depth. Φ_{inc} (λ) is the incident light intensity per unit area and QE (λ, d) represents the quantum efficiency.

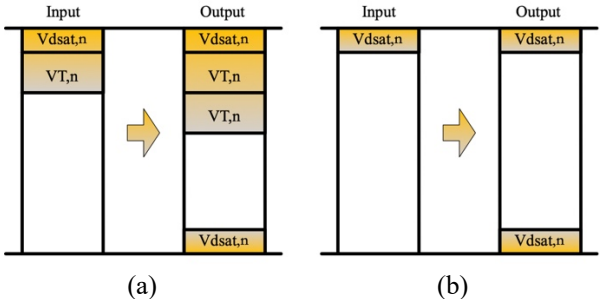

Fig.4 Traditional 4T pixel input and output swings. (b) The pixel input and output swings of this work.

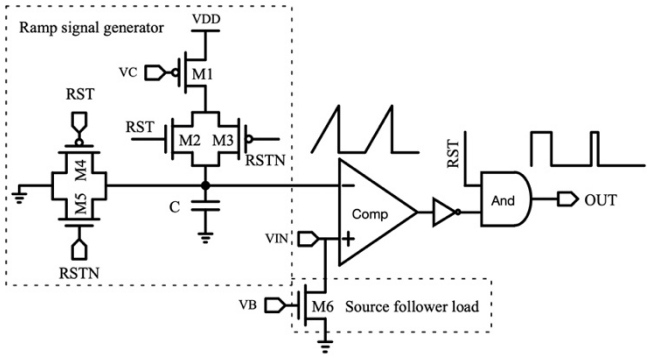

Fig. 5 The schematic of PWM_image

The proposed pixel circuit is based on a 4T pixel, with reset transistor M1 implemented using a PMOS transistor. The M4 in the source follower adopts a low threshold voltage nnt18 transistor. Meanwhile, the MOS pair M2/M3 is used to be transistor switches, reducing the voltage drop to 0V approximately. This allows the reset voltage of the photodiode to reach VDD. The SFA uses nnt18 transistors with a threshold voltage close to 0V. The row output switch uses the M5/M6 pair, which can effectively increase the output signal swing. Fig. 4 shows the traditional 4T pixel output swing and the rail-to-rail output swing proposed in this work.

C. Dual-channel time-interleaved PWM quantizer

The circuit diagram of PWM quantizer (PWM_image) is shown in Fig. 5. Transistors M1-5 and capacitor C constitute a ramp signal generator. M6 is the load current source for the pixel source follower. Through row synchronization signals, all odd columns share one load current source M6. When RST is low, M2/M3 are off and M4/M5 are on, and the capacitor voltage is 0V, so the comparator output is high. When RST is high, M2/M3 are on and M4/M5 are off. By adjusting VC to an appropriate value, suitable current is generated to charge capacitor C and generate a ramp signal. The ramp signal is compared with the pixel array voltage VIN. When the ramp signal is greater than VIN, the comparator output goes to low. After inversion, it becomes a high level pulse width signal after AND logic with the RST clock signal.

III. Simulation Results and Discussions

A. The proposed pixel circuit

The layout of the photodiode is shown in Fig. 6(a) with an area of 10μm×10μm. Parasitic parameter extraction gives a capacitance of 9.27fF for N+/P-well and 18.28fF for P-well/DNW/P-sub. The energy harvesting photodiode P-well/DNW/P-sub is simulated with a model of a capacitor and current source in parallel, sweeping the current source from 0 to 400pA. The resulting I-V curve is shown in Fig. 6(b). It means that the proposed pixel can harvest energy and generate a voltage between -350mV and -460mV.

With a 1V supply voltage, a comparative simulation is

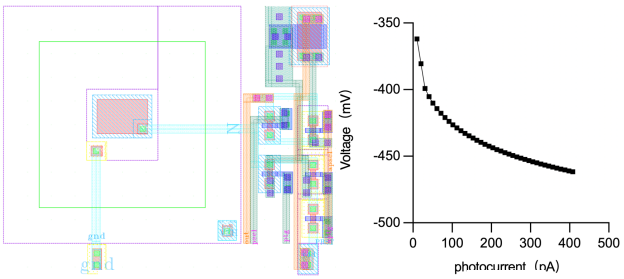

Fig.6 (a) Layout of the proposed pixel. (b) Volt-ampere response curve of the energy harvesting photodiode.

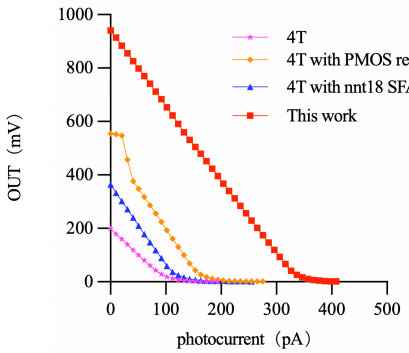

Fig.7 The output voltage swings for different 4T pixel circuits and the proposed work.

performed on the output swing of the conventional 4T pixel and the proposed pixel structure, as shown in Fig. 7. The bluecurve shows the output voltage swing of the conventional 4T pixel, with a maximum output voltage of 200mV. The purple curve is the result of a 4T pixel with an NMOS reset transistor and an nnt18 transistor for the source follower, and it has a maximum output voltage of 364mV. The orange curve is the result of a 4T pixel with a PMOS reset transistor and an nnt18 transistor for the source follower. Its output swing is improved and the maximum is 544mV. The red curve shows the output voltage swing of the wide swing pixel proposed in this work, with a maximum output voltage of 940mV. Compared to the three cases of the 4T pixel, the dynamic range is improved by 13.4dB, 8.24dB and 4.75dB, respectively.

B. Dual-channel time-interleaved PWM quantizer

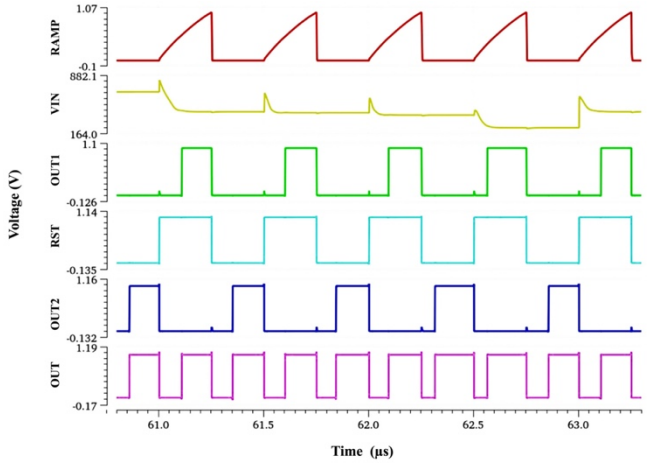

Fig.8 Simulation results of PWM quantizer.

TABLE I. SIMULATION RESULTS OF IMAGE SENSOR FOR TYPICAL PHOTOCURRENT.

Pixel out	o<3>	o<4>	o<5>	o<6>	o<7>
Photocurrent (pA)	100	200	300	500	100
VIN (mV)	445.4	420.8	392.8	390.3	436
OUT1 (ns)	142.1	150	157.2	186.9	145.3

TABLE II. PERFORMANCE SUNMMARY AND COMPARISON WITH OTHER WORKS

	[2]	[4]	[6]	This work
Process[µm]	0.18	0.35	0.18	0.18
Pixel type	APS	APS	APS	APS
Pixel size[µm2]	21×18.75	15×15	5×5	11×13
Pixel array	32×32	32×32	100×90	32×32
FF[%]	—	21	94	72
Supply[V]	1.8	1.5	0.6	1
FoM[pJ/pixel] Power Consumption	16.43µW	15.8µW	57.8 pJ/pixel	6.7µW

The simulation results of the dual-channel PWM quantizer are shown in Fig. 8. RAMP is the waveform generated by the ramp signal generator in Fig. 6. VIN is the waveform of the odd columns o<3-7> in the second row of the pixel array. The voltage values of VIN and their corresponding photocurrent are listed in Table I. Clock is the 2MHz clock signal. OUT1 is the PWM quantized output of a single channel. OUT2 is the output of the other channel. OUT is the final output after time-interleaving OUT1 and OUT2. It can be seen that VIN voltage is inversely proportional to the photocurrent, and the pulse width of OUT1 is proportional to the photocurrent. Table I lists the values of VIN, OUT1 in Fig. 8 and the corresponding configured photocurrent values. The data shows that the larger the photocurrent, the smaller the VIN, and the larger the pulse width of the PWM quantizer output signal. Table II summaries the performance of the Proposed image sensor and compares with the other recent state-of-the-art works.

IV. CONCLUSION

This paper proposes an image sensor with wide voltage swing that can work in energy harvesting and imaging modes simultaneously. The pixel architecture is optimized based on the conventional 4T pixel to effectively increase the output swing. Simulation results show an improvement of 13.4dB in dynamic range compared to the 4T pixel. The photodiode in the pixel uses vertically stacked N+/P-well and P-well/DNW/P-sub, with N+/P-well for imaging and P-well/DNW/P-sub for energy harvesting. An image sensor with 32×32 proposed pixel array and a dual-channel PWM quantizer is designed. The exposure time can be controlled through the input ports. The image sensor consumes 6.7µW power at 2MHz frequency. The power consumption could be further reduced if the harvested energy is collected to supply the system.

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