A 1.02 ppm/°C Precision Bandgap Reference with High-order Curvature Compensation for Fluorescence Detection

Bingjun Xiong, Feng Yan, Wenji Mo, Jian Guan, Yuxuan Huang, Jingjing Liu
School of Electronics and Communication Engineering, Sun Yat-Sen University, Shenzhen 518107, China
Email: liujj77@mail.sysu.edu.cn

2024 IEEE International Symposium on Circuits and Systems (ISCAS) | 979-8-3503-3099-1/24/$31.00 ©2024 IEEE | DOI: 10.1109/ISCAS58744.2024.10557967

***Abstract*—This paper presents a high precision bandgap reference using high-order curvature compensation to achieve good temperature coefficients over a wide operating range. The proposed compensation circuit employs currents with optimized temperature coefficients to minimize the temperature drift of the output voltage. The proposed bandgap reference is designed using a standard 0.18μm CMOS process. The simulation results demonstrate that the proposed bandgap reference achieved a 1.02ppm/°C from -40°C to 125°C with a supply voltage of 3.3V. With the proposed high-order curvature compensation schemes, the bandgap reference circuit can achieve a start-up time of 7μs and a 85.5dB PSRR at 100Hz. The reference voltage is 1.066V with the precision line sensitivity (LS) of 0.011%/V for supply voltages between 2V and 5V.**

Keywords—Bandgap reference, High-order curvature compensation, Temperature coefficient, Line sensitivity.

I. INTRODUCTION

The demand for precise temperature monitoring has risen, leading to great interest in fluorescent optical fiber sensors across industries. Their insulating properties and resistance to interference offer advantages over other temperature sensors [1]. However, the fluorescent optical fiber sensors require robust, accurate power supplies to ensure precision. Bandgap reference sources (BGR) are critical components in analog integrated circuits, providing a reference voltage to all other modules [2-4]. The accuracy of the reference directly affects power precision, which then impacts sensor measurement accuracy. Minimizing temperature coefficient (TC) in the bandgap reference circuits is therefore critical for research. Jiang et al. developed an all-MOS voltage reference. They minimized zero-TC sensitivity by analyzing secondary effects and using drain-source voltages [5]. They achieved a 5.6ppm/°C from -40°C to 125°C. Liu et al. developed a five-piece linear compensated voltage reference in 0.35μm CMOS process [6]. It uses mismatch/noise suppression and an adaptive current loop, which effectively minimize the temperature coefficient. Measurements demonstrate the reference provides 30μA load current and achieves an average temperature coefficient of 3ppm/°C from -45°C to 125°C. Li et al. proposed a V-shaped curvature compensation reference source circuit to reduce the temperature drift of the output reference voltage [7]. The voltage reference achieved an optimal temperature coefficient of 1.9ppm/°C when measured over a -45°C to 125°C temperature range. Li et al. proposed a curvature compensation circuit comprising current model fine-tuning circuits [8]. The fine-tuning circuits enabled the voltage reference circuit to achieve an ultra-low temperature coefficient of 1.64ppm/°C. Previous studies have proposed various compensation techniques to improve the temperature characteristics of voltage reference source circuits. This paper proposes a high-order curvature compensation circuit with a simple structure and good process portability. The rest of this paper is organized as follows: Section II discusses the circuit principles and implementation; Section III presents the simulation results; Finally, Section IV provides concluding remarks.

II. DESIGN OF THE PROPOSED BANDGAP REFERENCE CIRCUIT

A. Principle of basic bandgap reference

The base-emitter voltage (V_{BE}) of a bipolar junction transistor (BJT) varies with absolute temperature (T). The partial derivative can be expressed as (1).

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - E_g/q - (m+4)V_T}{T} = -1.5\, mV/°C \tag{1}$$

where $m \approx$ -1.5, V_T is the thermal voltage and E_g is the bandgap energy of silicon. They are equal to kT/q and 1.12eV respectively. The $\partial V_{BE}/\partial T$ generates a complementary-to-absolute-temperature voltage V_{CTAT} and has a negative TC of -1.5mV/°C when V_{BE} is 750mV and T is 300K. By utilizing BJTs of unequal sizes, the difference between the base-emitter voltages ΔV_{BE} of the two BJTs can be expressed as $V_T \cdot \ln(n)$ [9-11], which is proportional to absolute temperature. The V_{PTAT} exhibits a positive TC described by (2).

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} In(n) = \left[0.086 \cdot In(n)\right] mV/°C \tag{2}$$

Combining V_{PTAT} and V_{CTAT} with opposite temperature coefficients and assigning proper weights, the ideal zero temperature coefficient voltage V_R can be generated, as shown in Fig. 1.

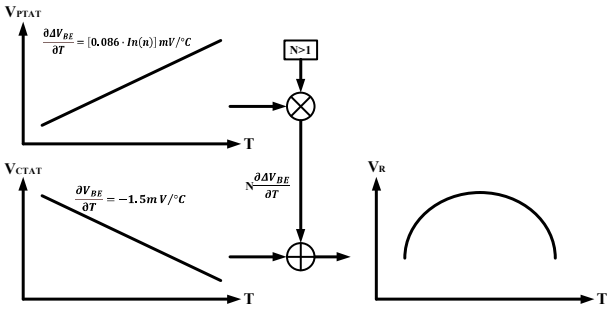


Fig. 1. Illustration of bandgap reference voltage generation.

This work is supported by National Natural Science Foundation of China with project no. 62174181.

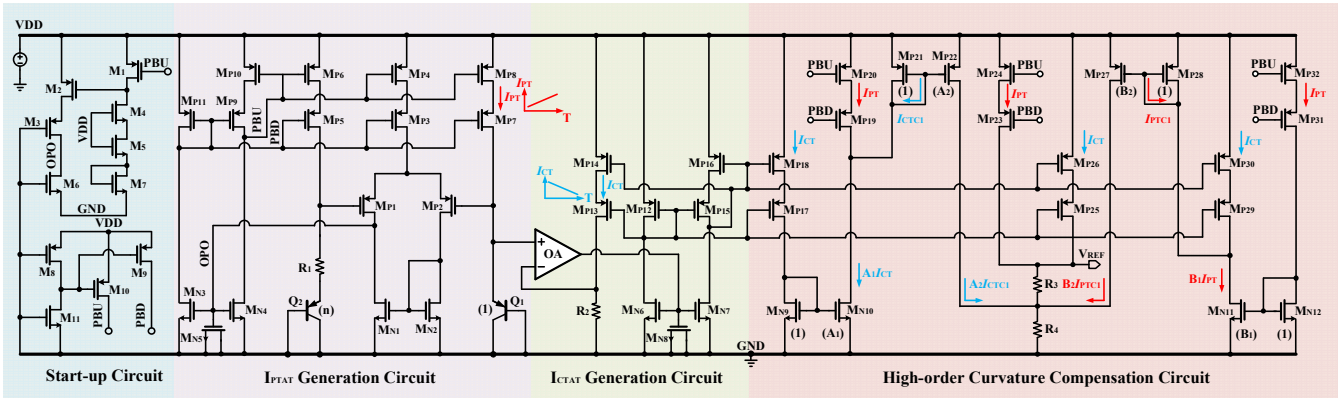
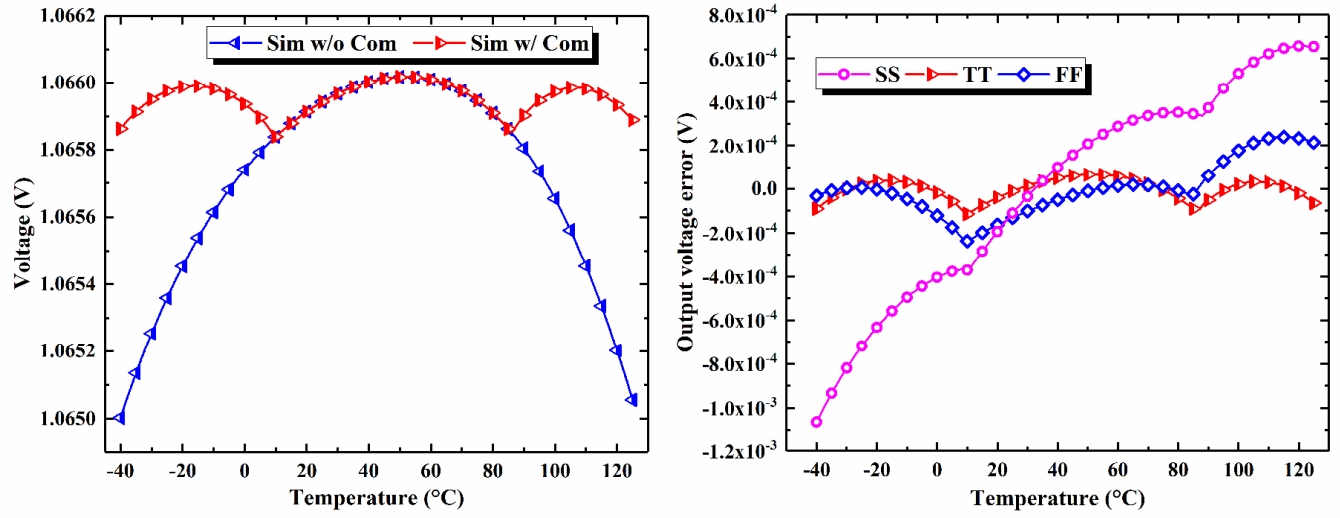


Fig. 2. Proposed high-order curvature compensation bandgap reference circuit.



(a) (b)

Fig. 3. (a) Simulation results of temperature coefficients for the proposed bandgap voltage reference V_{REF} and conventional bandgap voltage reference VR without curvature compensation. (b) Simulation results of the proposed bandgap voltage reference V_{REF} over process corners.

B. Proposed curvature compensation bandgap reference

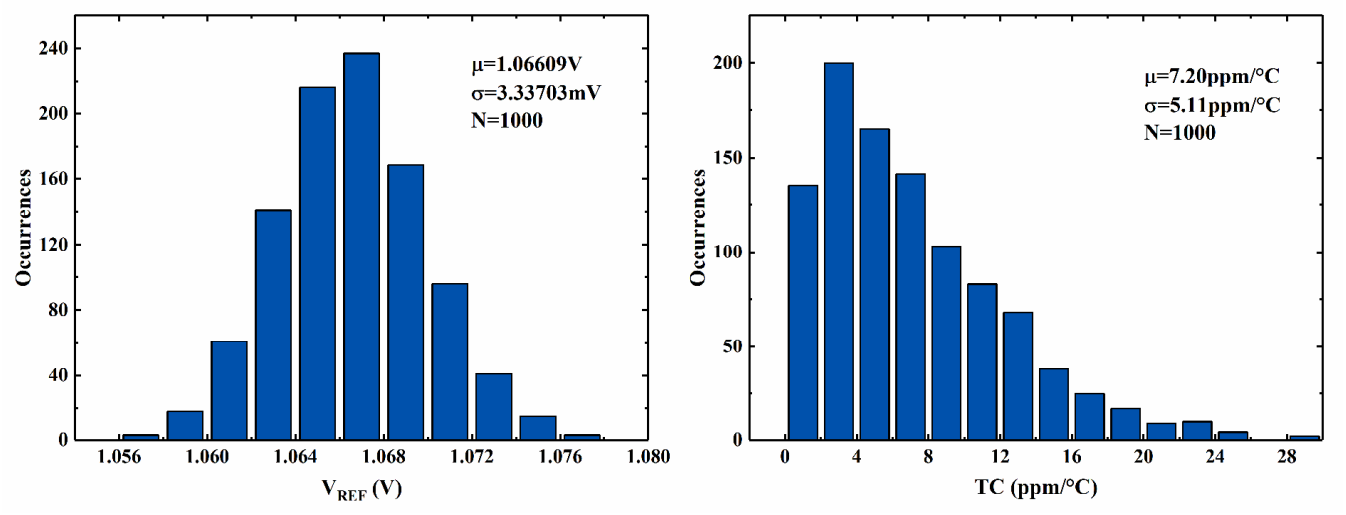
The proposed bandgap reference source circuit diagram with high-order curvature compensation is depicted in Fig. 2. It comprises a start-up circuit, a proportional-to-absolute-temperature (PTAT) current generation circuit, a complementary-to-absolute-temperature (CTAT) current generation circuit, and a high-order curvature compensation circuit.

The I_{PTAT} generation circuit comprises CMOS transistors M_{P1}-M_{P11}, M_{N1}-M_{N5}, bipolar transistors Q_1-Q_2, and poly-resistor R_1. M_{P1}-M_{P4} and M_{N1}-M_{N2} form a transconductance amplifier whose differential inputs connect to the emitter of Q_1 and R_1, respectively. This connection establishes the V_{BE} difference between Q_1 and Q_2 across R_1, therefore generating a current I_{PT}. Similarly, the deep negative feedback from the operational amplifier (OA) applied on Q_1 and R_2 produces a current I_{CT} across R_2. Transistors M_1-M_{11} constitute the start-up circuit, while transistors M_{N5} and M_{N8} act as MOS capacitors to stabilize the static operating point and ensure a smooth start-up process. By combining I_{PT} and I_{CT} with opposite temperature coefficients, and assigning proper weights, the ideal zero temperature coefficient voltage V_R can be expressed as (3).

$$V_R = (I_{PT} + I_{CT}) \cdot (R_3 + R_4) \tag{3}$$

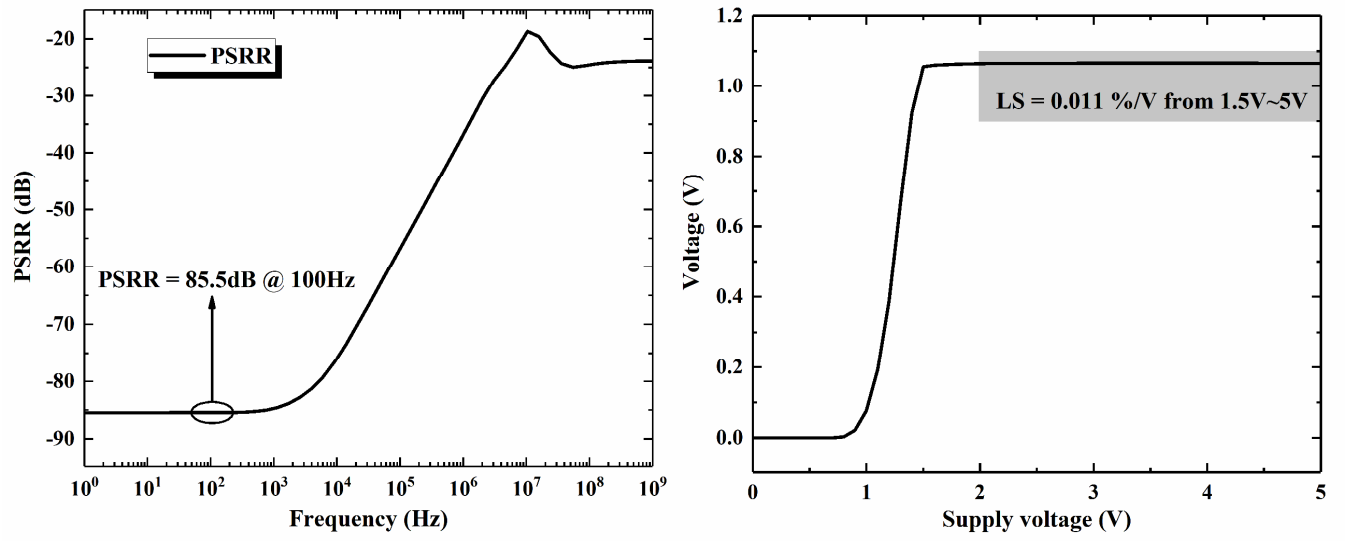
The high-order curvature compensation circuit is composed of CMOS transistors M_{P17}-M_{P32}, M_{N9}-M_{N12} and resistors R_3-R_4, and produces compensation currents I_{CTC1} and I_{PTC1} with negative TC at low temperature and positive TC at high temperature respectively. When $I_{PT} > A_1 I_{CT}$, transistors M_{P21} and M_{P22} are cut off, so no current flows through transistor M_{P22}. When $I_{PT} < A_1 I_{CT}$, transistors M_{P21} and M_{P22} turn on, and the negative temperature compensation current $A_2 I_{CTC1}$ is generated and flows into R_4. Similarly, the positive temperature compensation current $B_2 I_{PTC1}$ is generated and flows into R_4. By incorporating the compensation currents I_{CTC1} and I_{PTC1}, curvature compensation can be applied to V_R at low and high temperatures, respectively. This substantially suppresses the temperature drift of V_R. Thus, V_{REF} of the high-order curvature compensated bandgap reference can be expressed as (4).

$$V_{REF} = V_R + (A_2 I_{CTC1} + B_2 I_{PTC1}) \cdot R_4 \tag{4}$$



(a) (b)

Fig. 4. (a) The Monte Carlo simulation results of the proposed bandgap voltage reference V_{REF}. (b) The Monte Carlo simulation results of temperature coefficient for the proposed bandgap voltage reference.



(a) (b)

Fig. 5. (a) Simulation results of the power supply rejection ratio of the proposed bandgap voltage reference. (b) Simulation results of the line sensitivity of the proposed bandgap voltage reference.

III. Simulation Results of the Proposed Bandgap Reference Circuit

Fig. 3(a) shows the simulated output voltage before and after applying the curvature compensation. Specifically, the red curve indicates the compensated output voltage V_{REF}, while the blue curve corresponds to the uncompensated VR. The results show that both output voltages are approximately 1.066V. Within the wide temperature range of -45°C to 125°C, the temperature coefficient of the proposed high-order compensated reference is 1.02ppm/°C, which is 5.66 times smaller than the 5.77ppm/°C of the uncompensated traditional reference. By compensating at high and low temperatures, the curvature technique can significantly reduce output voltage drift and achieve a high-precision voltage reference.

Fig. 3(b) shows the process corner simulation results of the high-order curvature-compensated voltage reference. The output voltage values of the BGR were recorded at each temperature and the average value is obtained. The difference between each value and the average is plotted in Fig. 3(b). The simulation results indicate that under the FF process corner, the temperature coefficient of the output voltage is 2.72ppm/°C from the temperature range of -45°C to 125°C. For the SS process corner, the temperature coefficient is 9.73ppm/°C, which is still good enough.

As shown in (4), the output voltage V_{REF} is highly sensitive to the characteristics of the bipolar transistor, MOSFET, and resistor. Deviations and mismatches in these components can significantly deteriorate the voltage reference performance. Fig. 4(a) and (b) present the Monte Carlo simulation results for the proposed V_{REF} and TC, respectively. The mean output voltage is 1.066V with a standard deviation of 3.33mV over 1000 simulation runs. The average temperature coefficient is 7.2ppm/°C with a standard deviation of 5.11 ppm/°C.

TABLE I. PERFORMANCE OF THIS WORK COMPARED WITH OTHER REFERENCES

	This work[a]	[2][a] TCAS II 2020	[3][b] JSSC 2021	[4][b] TCAS I 2021	[9][a] ICTA 2021	[10][b] TCAS I 2022	[11][b] TIM 2022
Tech. (nm)	**180**	45	130	65	180	180	180
Type	**CMOS**	CMOS	CMOS	CMOS	BCD	CMOS	CMOS
Min VDD (V)	**1.5**	1.05	3.3	2.5	3	3.2	3.3
V_{REF} (V)	**1.066**	0.5	1.16	1.1458	2.048	2.141	0.275
LS (%/V)	**0.011**	0.15	0.03	N/A	N/A	0.0146	N/A
PSRR (dB) @100Hz	**85.5**	60	75	N/A	N/A	63.4	N/A
Temp. Range (°C)	**-40°C~125°C**	-40°C~120°C	-40°C~150°C	0°C~80°C	-40°C~125°C	-25°C~125°C	-20°C~110°C
Power (μW)	**866**	7.56	396	132	923	1350	1716
TC	**1.03**	24.4	5.78	0.87	42	1.183	2.9

[a] Simulation results. [b] Measured results.

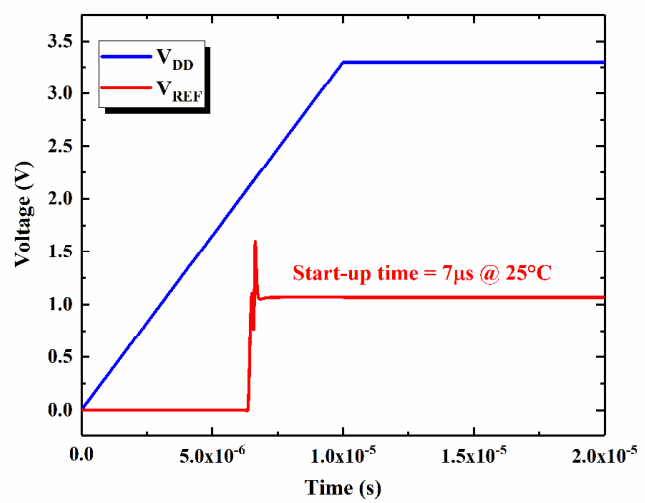


Fig. 6. Simulation results of the start-up circuit.

Fig. 5(a) presents the simulated power supply rejection ratio (PSRR) of the proposed bandgap reference. The PSRR is 85.5dB at 100Hz and decreases gradually with increasing frequency, reaching 76dB at 10kHz. Fig. 5(b) presents the simulated line sensitivity performance. The minimum operating voltage is 1.5V, and the LS is 0.011%/V over the 2V to 5V supply voltage range.

The bandgap reference uses an unexcited circuit topology. At start-up, operating point degeneracy may lead to zero current operation. To break this condition, a startup circuit (M_1-M_{11}) is implemented to establish normal operation. During startup, as the power supply voltage increases gradually, the differential PMOS pair M_{P1}-M_{P2} output OPO rises. When it exceeds the threshold voltage V_{THN} of transistors M_{N3} and M_{N4}, and turning them on. This pulls down nodes PBD and PBU, enabling reference startup. As the reference circuit starts up normally, the gate voltage of transistor M_2 increases gradually. Once the gate voltage exceeds VDD-$|V_{THP}|$, transistor M_1 cuts off. After M_1 cuts off, the start-up circuit shuts down. Fig. 6 presents the simulation results of the start-up circuit, validating the smooth start-up of the reference circuit within 7μs. Table I summarizes the performance comparison between this work and other reference designs. In comparison with other proposed designs, this work demonstrates superior temperature coefficient and reduced circuit complexity.

IV. CONCLUTION

This paper proposed a high-order curvature compensation bandgap voltage reference circuit implemented in 0.18μm CMOS process. The designed reference circuit exhibits an output voltage of 1.066V over a wide temperature range from -40°C to 125°C, along with a low temperature coefficient of 1.02ppm/°C. The accuracy is improved by 5.66 times compared to a conventional uncompensated reference circuit. The reference circuit also achieves a high PSRR of 85.5dB at 100Hz and a low LS of 0.011%/V. With these superior performance characteristics, the proposed high-order curvature compensation technique offers new solutions for power management integrated circuits (ICs). These ICs can then provide accurate high-precision power supplies required by fluorescent optical fiber temperature sensors for scientific temperature measurements in harsh environments.

REFERENCES

[1] S Ma, Y Xu, Y Pang, et al., "Optical fiber sensors for high-temperature monitoring: a review," Sensors, 2022, 22(15): 5722.

[2] R. Nagulapalli, R. K. Palani and S. Bhagavatula, "A 24.4 ppm/°C Voltage Mode Bandgap Reference With a 1.05V Supply," *IEEE Trans. Circuits Syst. II, Exp. Bri*, vol. 68, no. 4, pp. 1088-1092, April 2021.

[3] K. Chen, L. Petruzzi, R. Hulfachor and M. Onabajo, "A 1.16-V 5.8-to-13.5-ppm/°C Curvature-Compensated CMOS Bandgap Reference Circuit With a Shared Offset-Cancellation Method for Internal Amplifiers," *IEEE J. Solid-State Circuits*, vol. 56, no. 1, pp. 267-276, Jan. 2021.

[4] N. Liu, R. L. Geiger and D. Chen, "Sub-ppm/°C Bandgap References With Natural Basis Expansion for Curvature Cancellation," *IEEE Trans. Circuits Syst. I, Reg. Pap*, vol. 68, no. 9, pp. 3551-3561, Sept. 2021.

[5] J. Jiang, W. Shu and J. S. Chang, "A 5.6 ppm/°C Temperature Coefficient, 87-dB PSRR, Sub-1-V Voltage Reference in 65-nm CMOS Exploiting the Zero-Temperature-Coefficient Point," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 623-633, March 2017.

[6] L. Liu, X. Liao and J. Mu, "A 3.6 μVrms Noise, 3ppm/°C TC Bandgap Reference With Offset/Noise Suppression and Five-Piece Linear Compensation," *IEEE Trans. Circuits Syst. I, Reg. Pap*, vol. 66, no. 10, pp. 3786-3796, Oct. 2019.

[7] C. C. Lee, H. M. Chen, C. C. Lu, et al., "A High-Precision Bandgap Reference With a V-Curve Correction Circuit," *IEEE Access*, vol. 8, pp. 62632-62638, 2020.

[8] Y. Ji, J. Lee, B. Kim, H. J. Park and J. Y. Sim, "A 192-pW Voltage Reference Generating Bandgap–Vth With Process and Temperature Dependence Compensation," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3281-3291, Dec. 2019.

[9] Y. Shen, L. Cheng; D. Li, et al., "A 1.2 ppm/°C TC, 0.094% Inaccuracy 3-18V Supply-Range Bandgap Reference with Self-Compensation," *2021 IEEE ICTA*, Zhuhai, China, 2021, pp. 139-140.

[10] S. Huang, Li. M, Li. H, et al., "A Sub-1 ppm/°C Bandgap Voltage Reference With High-Order Temperature Compensation in 0.18-μm CMOS Process," *IEEE Trans. Circuits Syst. I, Reg*, vol. 69, no. 4, pp. 1408-1416, April 2022.

[11] M. Seung, W. Choi, S. Hur and I. Kwon, "Cold Junction Compensation Technique of Thermocouple Thermometer Using Radiation-Hardened-by-Design Voltage Reference for Harsh Radiation Environment," *IEEE Trans. Instrum. Meas*, vol. 71, pp. 1-7, 2022, Art no. 2005807.