# A Resistor-Free Grounded High-Frequency Memristor Emulator

Xinying Su, Bingjun Xiong, Junjie Yu and Jingjing Liu*

School of Electronics and Communication Engineering, Sun Yat-Sen University, Shenzhen, China

* suxy55@mail2.sysu.edu.cn, liujj77@mail.sysu.edu.cn

2024 IEEE 17th International Conference on Solid-State & Integrated Circuit Technology (ICSICT) | 979-8-3503-6183-4/24/$31.00 ©2024 IEEE | DOI: 10.1109/ICSICT62049.2024.10831028

***Abstract*—The memristor emulator circuit is an economical and effective tool that can simulate various circuit characteristics of the corresponding solid-state memristor. This paper proposes a resistor-free high frequency grounded incremental/decremental memristor emulators (MRE). It consists of a voltage-current conversion (VCC) module, an OTA and a grounded capacitor. The theoretical analysis of the proposed memristor emulator is conducted. The memristor emulator is designed using a standard 180nm CMOS technology. The simulation results show that the proposed memristor emulator demonstrate pinched hysteresis loops for the voltage-current curves with a power supply voltage of ± 0.9V and prove its memristor characteristics. The proposed design exhibits nonlinearity over a wide input voltage range and performs well at frequencies of up to 50MHz.**

***Keywords—operational transconductance amplifier* (*OTA*), *memristor emulator* (*MRE*), *pinched hysteresis loop* (*PHL*)**

## I. INTRODUCTION

The memristor is a nonlinear resistor with charge memory function, whose resistance value can change according to the history of the input current or voltage, enabling it to memorize the charge or magnetic flux by changing its resistance. Utilizing the above properties, memristors can be applied in various application fields, including high-speed memory arrays such as RRAM [1], analog and digital circuits [2], neuromorphic circuits [3], etc.

Due to the high manufacturing cost and structural complexity, physical memristors have not yet been commercialized. Therefore, simple and accurate memristor simulation circuits are needed to mimic the characteristics of real memristors. Currently, most memristor simulators consist of active modules (CFTA [4], VDTA[5], VDCC[6], etc.) and passive components such as capacitors. However, most existing memristor simulators have a maximum operating frequency of up to 1MHz and relatively complex circuit structures [4], [6].

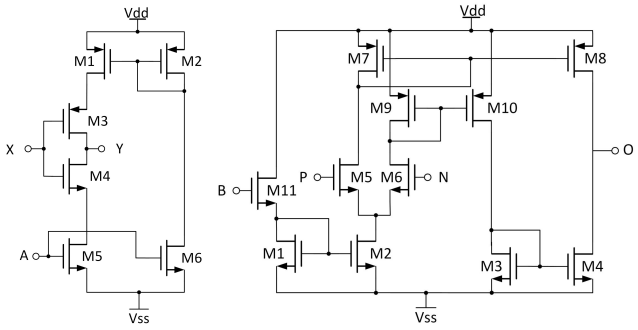
This paper proposes a resistsor-free high frequency memristor emulator with a voltage-current conversion (VCC) module. The VCC is connected with an operational transconductance amplifier (OTA) active module and a grounded passive capacitor to form a complete high-performance memristor emulator (MRE) circuit based on a standard 180nm CMOS technology. The simulation results verify the pinched hysteresis loop of the proposed memristor emulator circuit. The structure of this paper is as follows: Section II gives the design and mathematical derivation principles of the proposed MRE circuit. Section III contains the simulation results and discussion, and finally Section IV concludes the paper.

This work is supported by National Natural Science Foundation of China with project number 62174181.

## II. THE PROPOSED MEMRISTOR EMULATOR

### A. The VCC and OTA Modules

The circuit structure of the VCC module is shown in Fig. 1(a). The transconductance of the VCC module $G_{m1}$ can be derived from (1)-(3).




(a) (b)

Fig. 1. The circuit structures of (a) VCC, (b) OTA.

$$G_{m1} = \frac{g_{M3} + g_{M4}}{2} \tag{1}$$

$$g_{M3/4} = \sqrt{2 I_D K_{M3/4}} \tag{2}$$

$$K_{M3/4} = \mu C_{ox} \left( \frac{W}{L} \right)_{M3/4} \tag{3}$$

where $g_{M3}$ and $g_{M4}$ are the transconductance of M3 and M4 respectively, $I_D$ is drain current, $\mu$ is the mobility of carriers, $C_{OX}$ is the gate oxide capacitance per unit area and $W/L$ is the aspect ratio of transistors. Transistors M5 and M6 operate in the saturation region, and according to (1)-(3), and the drain current formula in the saturation region, (4) can be derived.

$$G_{m1} = k_1 \left( V_A - V_{ss} - V_{th} \right) \tag{4}$$

where $V_{th}$ is the threshold voltage of the transistor, and $k_1 = \left( \sqrt{K_{M3}} + \sqrt{K_{M4}} \right) \sqrt{K_{M5,6}} / 2\sqrt{2}$ . The relationship between the input voltage $V_X$ and the output current $I_Y$ is given by

$$I_Y = G_{m1} V_X \tag{5}$$

The schematic circuit of the OTA module is shown in Fig. 1(b), and the output current of the OTA can be obtained from (6).

$$I_O = G_{m2}(V_P - V_N) \tag{6}$$

where the transconductance of the OTA is $G_{m2} = \frac{k}{\sqrt{2}}(V_B - V_{ss} - V_{th})$. When the input voltage $V_{in}$ is connected to the P terminal, the N terminal is grounded, and vice versa. So the output current of the OTA can be written as follows:

$$I_O = \pm G_{m2} V_{in} \tag{7}$$

### B. The Proposed Memristor Emulator Circuit

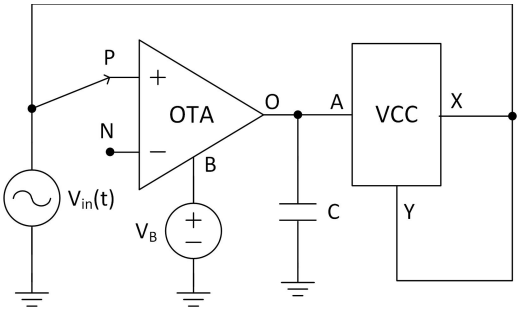



Fig. 2. Structure of the proposed memristor emulator.

The structure of the memristor emulator is shown in Fig. 2. A capacitor C is connected between the OTA and VCC module, leading to the following equation:

$$V_C = V_A = V_O = \pm\frac{1}{C}\int G_{m2} V_{in} dt = \pm\frac{G_{m2} A_m \cos \omega t}{\omega C} \tag{8}$$

where input voltage $V_{in}$ is a sinusoidal signal $V_{in} = A_m \sin \omega t$. Substituting (8) into (4), we obtain (9).

$$G_{m1} = k_1\left(\frac{\pm G_{m2} A_m \cos \omega t}{\omega C} - V_{ss} - V_{th}\right) \tag{9}$$

The X port is connected to the Y port and the input voltage $V_{in}$, and the Y port outputs current $I_Y$. Therefore, $I_Y = I_X = I_{in}$, $V_X = V_{in}$. The missing element memristor relates the charge and flux, as $dq = Wd\Phi$, which defines memductance $W$ for flux-controlled memristor.

$$W(\Phi_{in}) = \frac{I_{in}}{V_{in}} = \frac{I_Y}{V_X} = G_{m1} \tag{10}$$

Substituting (9) into (10), we obtain

$$W(\Phi_{in}) = k_1(-V_{ss} - V_{th}) \pm \frac{k_1 G_{m2} A_m \cos \omega t}{\omega C} \tag{11}$$

## III. Simulation Results and Discussion

To verify the performance of the proposed grounded memristor emulator, simulations were carried out based on a standard 180nm CMOS process. In the simulation DC supply voltages $V_{dd} = -V_{ss} = 0.9\text{V}$, bias voltage $V_B = 0.5\text{V}$, and input voltage $V_{in} = 0.25\sin \omega t$. The transistor sizes in the memristor emulator circuit are shown in Table I.Fig. 3 shows the transient response with an input voltage frequency of 2 MHz and a capacitance of 50pF.

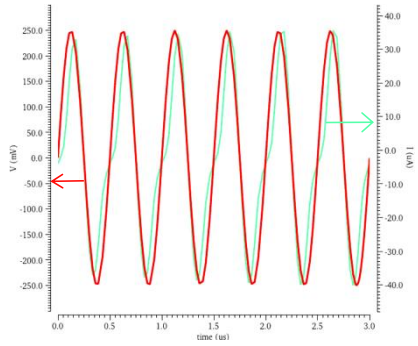


Fig. 3. Transient analysis at 2MHz with 50pF capacitor.

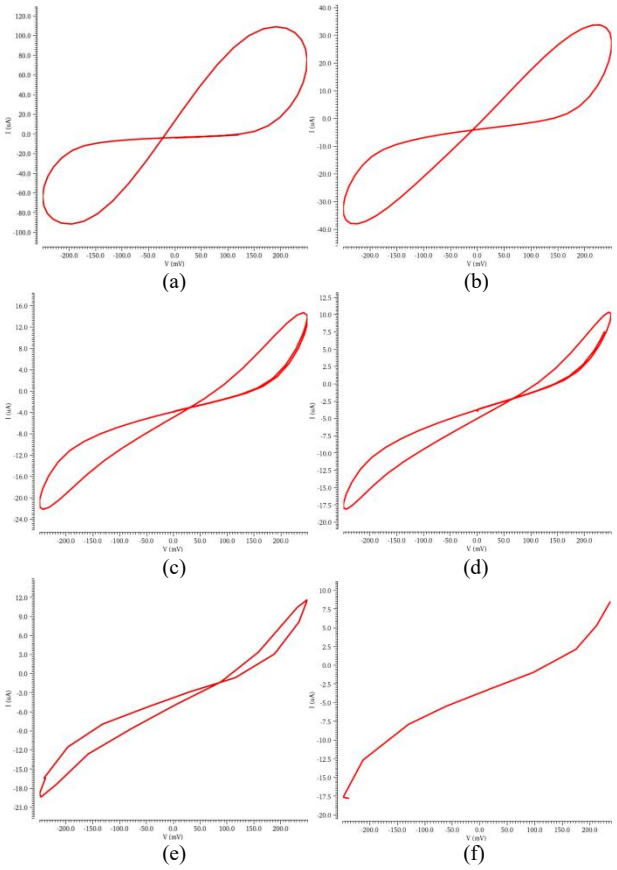



Fig. 4. Simulation results of the pinched hysteresis loops for the proposed memristor emulator circuit with different frequencies, (a) 900KHz, (b) 2MHz, (c) 4MHz, (d) 6MHz, (e) 8MHz, (f) 10MHz.

By plotting the input current versus the input voltage, the pinched hysteresis loop (PHL) characteristic of a memristor

was obtained. To determine the effect of the input voltage frequency on the memristor, a 50pF capacitor was connected, and only the input signal frequency was varied, resulting in pinched hysteresis loops at different frequencies. As shown in Fig.4 , as the frequency increases, the area of the PHL gradually decreases, and when the frequency reaches 10MHz, the memristor behaves like a linear resistor.

TABLE I. ASPECT RATIO OF ALL MOS TRANSISTORS

| | Transistors | W/L |
|---|---|---|
| **OTA** | M1-M6 | 1.44μm/180nm |
| | M7-M10 | 4.5μm/180nm |
| | M11 | 1.8μm/180nm |
| **VCC** | M1、M2 | 6.5μm/180nm |
| | M3 | 3.25μm/180nm |
| | M4 | 4μm/180nm |
| | M5、M6 | 2μm/180nm |

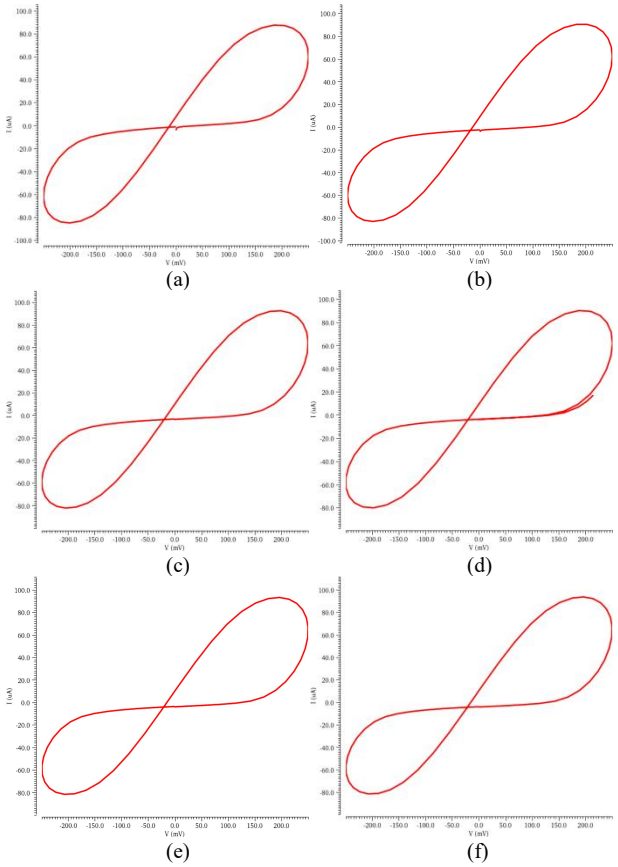



Fig. 5. Current-voltage curve of the proposed memristor emulator, at (a) 1MHz, 50pF, (b) 2MHz, 25pF, (c) 5MHz, 10pF, (d) 7.14MHz, 7.14pF, (e) 10MHz, 5pF, (f) 50MHz, 1pF.

Fig. 5 shows the simulation results of the memristor emulator when the capacitance frequency product is constant. It can be seen that the capacitance and frequency are inversely proportional, and when their product is a constant, the PHL remains essentially the same.

In Fig. 6, the maximum value of PHL at 25MHz with 2pF capacitor for the two memristor in parallel is approximately 300μA, while for the single memristor it is around 90μA. Similarly, PHL at 5MHz with 10pF capacitor for the parallel memristors is approximately 530μm, while for the single memristor it is around 90μm. This clearly indicates that the parallel memristors has a larger PHL area.

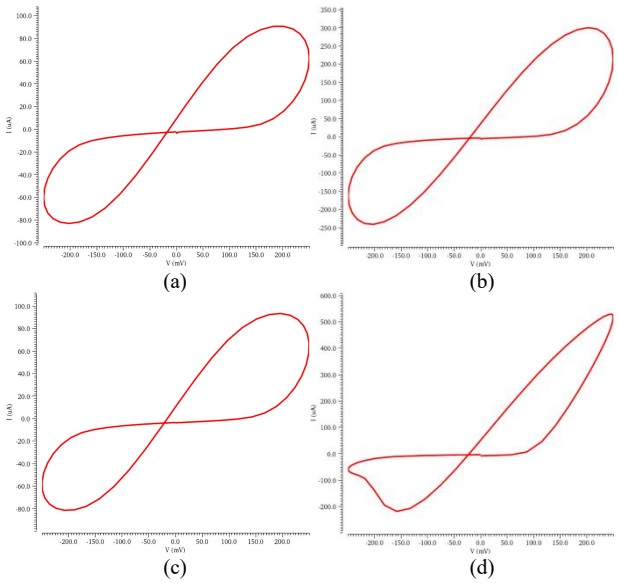



Fig. 6. Current-voltage curves for (a) single memristor emulator at 25MHz with 2pF capacitor, (b) two memristor emulators in parallel at 25MHz with 2pF capacitor, (c) single memristor emulator at 5MHz with 10pF capacitor, (d) two memristor emulators in parallel at 5MHz with 10pF capacitor.

## IV. CONCLUSION

This paper proposes a resistor-free grounded incrementing/decrementing memristor emulator based on OTA and VCC modules. Through simulations results, the mathematical analysis of the proposed memristor model is validated. Various parameter analysis, such as large changes in frequency and capacitance, are conducted to demonstrate the circuit's robustness. The proposed memristor's advantages include: i) electronic tunability, ii) resistor-free structure, iii) incrementing/decrementing modes, and iv) an operating range of up to 50 MHz. These observations confirm that the proposed MRE design is easy to implement and can be a good circuit model for the memristors.

## REFERENCES

[1] R. M. Claure, T. Tan Nguyen and B. Cambou, "Low Complexity Memristor-based RRAM Design for IoT Applications," 2023 7th International Conference on I-SMAC (IoT in Social, Mobile, Analytics and Cloud) (I-SMAC), Kirtipur, Nepal, 2023, pp. 42-45.

[2] S. Kirilov and V. Mladenov, "Application of New Metal-Oxide Memristor Models in Digital and Analog Electronic Circuits," 2023 19th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Funchal, Portugal, 2023, pp. 1-4.

[3] P. Nune and S. Mandal, "TaOx based memristor model and its emulator design for future neuromorphic computing," 2021 13th International Conference on Electronics, Computers and Artificial Intelligence (ECAI), Pitesti, Romania, 2021, pp. 1-5.

[4] S. S. Prasad, P. Kumar and R. K. Ranjan, "Resistorless memristor emulator using CFTA and its experimental verification", IEEE Access, vol. 9, pp. 64065-64075, 2021.

[5] J. Vista and A. Ranjan, "Flux controlled floating memristor employing VDTA: Incremental or decremental operation", IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 40, no. 2, pp. 364-372, Feb. 2021.

[6] K. Bhardwaj and M. Srivastava, "Floating memristor and inverse memristor emulation igurations with electronic/resistance controllability", IET Circuits Devices Syst., vol. 14, pp. 1065-1076, Oct. 2020.