A Second-Order Noise-Shaping SAR ADC for Biomedical Sensor Applications

Haoning Sun
School of Electronics and Communication Engineering
Sun Yat-Sen University
Shenzhen, China
sunhn3@mail2.sysu.edu.cn

Kangkang Sun
School of Electronics and Communication Engineering
Sun Yat-Sen University
Shenzhen, China
sunkk3@mail2.sysu.edu.cn

Yuchen Wang
School of Electronics and Communication Engineering
Sun Yat-Sen University
Shenzhen, China
wangych79@mail2.sysu.edu.cn

Wenji Mo
School of Electronics and Communication Engineering
Sun Yat-Sen University
Shenzhen, China
mowj28@mail2.sysu.edu.cn

Feng Yan
School of Electronics and Communication Engineering
Sun Yat-Sen University
Shenzhen, China
yanf9@mail2.sysu.edu.cn

Jingjing Liu*
School of Electronics and Communication Engineering
Sun Yat-sen University
Shenzhen, China
liujj77@mail.sysu.edu.cn

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***Abstract*—This paper proposes a low-power, area-efficient, and high-precision fully passive second-order noise-shaping (NS) successive approximation register (SAR) analog-to-digital converter (ADC) for a portable multi-channel biosignal recorder to detect abnormal action potentials in epilepsy. The proposed fully passive noise-shaping technique achieves a second-order noise transfer function (NTF) using only switched-capacitor and a single-input-pair comparator, resulting in significant benefits in power consumption and accuracy. The power consumption is further reduced and the circuit area is minimized by employing a split-segmented capacitor digital-to-analog converter (CDAC) array. The proposed second-order NS SAR ADC is implemented using a 180nm CMOS process with an area of 0.3×0.28mm^2. Simulation results show that the circuit consumes 86μW at a 1.2V supply voltage when the sampling rate is 10MS/s. It achieves a signal-to-noise and distortion ratio (SNDR) of 92.66dB, an effective number of bits (ENOB) of 15.1bits, a bandwidth of 80kHz, a Schreier figure of merit (FoM$_S$) of 182.3dB, and a Walden figure of merit (FoM$_W$) of 15fJ/conv.-step.**

Keywords—biosensor system, noise-shaping, SAR ADC, split-segmented capacitor array

I. Introduction

Epilepsy is a chronic disease characterized by recurrent behavioral seizures caused by abnormal discharges of human brain neurons. Electrophysiological examination is one of the important methods for diagnosing epilepsy, including Electroencephalography (EEG) and video EEG (vEEG) [1]. Different types of epilepsy may be accompanied by action potentials of different frequencies, but some severe epileptic seizures can cause action potential frequencies as high as several tens of kHz [2]. Portable multi-channel biosignal recorders typically contain multiple channels that can simultaneously record action potential signals from multiple locations or multiple neurons. In the front-end readout system, the action potential signals are acquired and preprocessed by the sensor electrodes and analog front-end blocks [3], [4]. An ADC digitizes the signals and transmits them to the digital signal processor (DSP) for further processing, as shown in Fig. 1. To accommodate the requirements of portability and multi-channel operation, the ADC needs to adopt a miniaturized and low-power design. In order to accurately capture the full range of action potentials, the ADC needs to have a relatively high bandwidth and precision.

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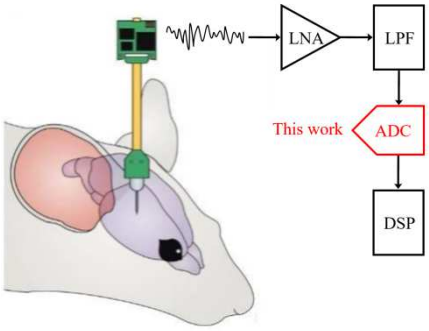

Fig. 1. Simplified readout front-end block diagram of an action-potential acquisition system.

NS-SAR ADC is one of the most promising hybrid ADC architectures. Similar to the SAR ADC, it features low power and low cost [5], while its high signal-to-noise ratio is comparable to that of the Δ-Σ ADC. The first modern NS-SAR ADC is implemented using a cascaded integrator feed-forward (CIFF) structure [6]. A loop filter used in the circuit consumes relatively high power, which cannot meet the low-power requirement. Passive gain technique is introduced into NS-SAR ADC [7], realizing second-order passive noise-shaping through charge redistribution. However, it uses an additional capacitor as large as the DAC capacitor array for the passive integration part, resulting in a large area consumption. Zhuang utilizes switches and capacitors to construct passive integrators instead of power-consuming operational amplifiers for noise-shaping [8]. But the multi-input comparator generates larger thermal noise. Moreover, since the kickback noise of the comparator is proportional to the total size of the input transistors, the multi-input comparator produces additional kick-back noise, affecting the accuracy of the ADC.

This paper presents a low-power, small-area, high-precision second-order noise-shaping SAR ADC suitable for a portable multi-channel biomedical signal recorder for epilepsy patients. First, a fully passive noise-shaping structure is employed, utilizing passive residue voltage summation and ping-pong residue capacitors switching techniques to achieve the second-order noise-shaping functionality. Second, a single-input-pair comparator structure is adopted to realize passive noise-shaping, which avoids the additional noise introduced by multi-input-pair comparators in the traditional

design and enhances the noise-shaping effect. This approach eliminates the need for additional active amplifiers, thereby reducing the ADC power consumption. Furthermore, a split-segmented capacitor array is utilized to reduce the total capacitance of the CDAC, minimizing the capacitor area. The structure of this paper is as follows. Section II presents the proposed noise-shaping SAR ADC architecture and principles. The ADC simulation results are shown in Section III. The final section concludes the paper.

II. The Proposed Second-Order NS SAR ADC Design

In this section, the structure and working principles of the fully passive second-order NS SAR ADC will be described. It utilizes passive residue voltage summation technique to achieve the integration process of noise-shaping. And ping-pong residue capacitors switching technique is used to enhance the sampling rate. In addition, a major advantage of the proposed NS SAR ADC is the use of a single-input-pair comparator. Moreover, this section also describes the design of split-segmented CDAC array.

A. Fully Passive Second-order Nosie-Shaping

A multi-input-pair comparator induces more thermal noise than a single-input-pair comparator. Moreover, the kick-back noise of a comparator is proportional to the total input transistor size, so the residue pair generates extra kick-back noise [9]. Thus, conventional NS-SAR ADCs need to balance the noise reduction brought by noise shaping with the noise increase caused by using multi-input-pair comparators. Based on this, the proposed NS-SAR ADC employs a fully passive signal residue summation technique, which enables second-order noise shaping without requiring multi-input-pair comparators. Thus, it can avoid this trade-off.

The proposed single-input-pair comparator-based second-order NS-SAR ADC architecture and its timing diagram are illustrated in Fig. 2. There are two continuous periods to clearly illustrate the operation principle. CLK_S denotes the

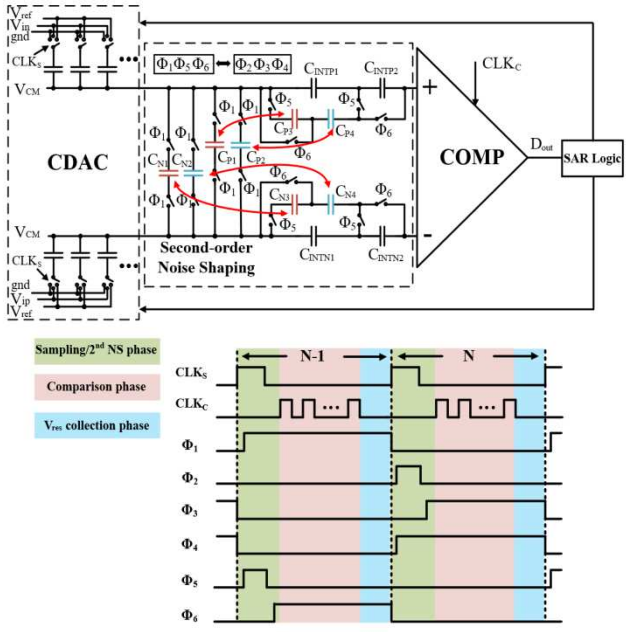

Fig. 2. The architecture of the proposed single-input comparator-based second-order NS SAR ADC and timing diagram for two conversion cycles.

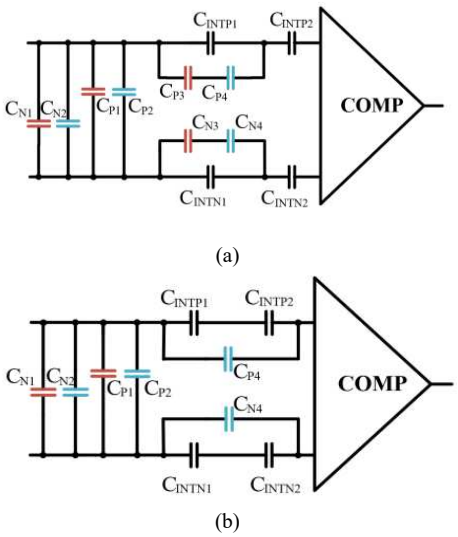

Fig. 3. Switched-capacitor switching diagram of the noise-shaping structure within one sampling cycle, (a) when Φ2 (or Φ5) is at a high level, (b) when Φ3 (or Φ6) is at a high level.

ADC sampling clock and CLK_C represents the control clock for the ADC comparator. During one sampling period, the ADC undergoes three phases, including the sampling and second-order noise-shaping phase, comparison phase and residue V_{res} collection phase. Φ_1 and Φ_4 are alternately switched on in a periodic manner. Φ_2 alternates with Φ_5, and Φ_3 alternates with Φ_6. The non-overlapping time between the switching of each switch (Φ_1 to Φ_6) is 25ps. It doesn't need extra time slots to process residue switching and charge sharing. Hence, the noise shaping function does not affect the sampling and comparison timing.

The circuit adopts a differential-input structure. $C_{P1\text{-}4}$ and $C_{INTP1,2}$ perform noise-shaping structure at the signal positive input, while $C_{N1\text{-}4}$ and $C_{INTN1,2}$ perform the same function at the negative input. This structure employs a residue voltage summation and ping-pong residue capacitors switching techniques to achieve fully passive second-order noise-shaping. $C_{N1,2}$ and $C_{N3,4}$ form one group of alternating switching capacitors ($C_{P1,2}$ and $C_{P3,4}$ constitute the other group). When $C_{N1,2}$ function as the residue voltage sampling capacitors, $C_{N3,4}$ serve as the integration capacitors and engage in charge redistribution with $C_{INTN1,2}$. The roles of $C_{N1,2}$ and $C_{N3,4}$ interchange in the subsequent cycle, as marked by red double head arrows. The same principle applies to $C_{P1\text{-}4}$ and $C_{INTP1,2}$. In this design, $C_{P1\text{-}4} = C_{N1\text{-}4} = C_{INTP1,2} = C_{INTN1,2} = C_{DACN,P}/4$. At the end of the comparison stage in one cycle (V_{res} collevtion phase), the residue V_{res} is collected by the back-to-back residue voltage collection capacitors of the current cycle connected across the top plates of the DAC arrays. When V_{res} collection mode finishes, $C_{N1,2}$ (or $C_{N3,4}$) and $C_{P1,2}$ (or $C_{P3,4}$) obtain the final residue with the same quantity but opposite polarity. The collected residual voltage is utilized as the integration voltage for noise shaping in the next sampling cycle.

The proposed fully-passive second-order noise-shaping process is illustrated in detail in Fig. 3. Consider the sampling cycle when Φ_1 is at a high level as an example. During this cycle, $C_{N1,2}$ and $C_{P1,2}$ serve as residue voltage collection capacitors. $C_{N3,4}$ and $C_{P3,4}$ participate in the noise-shaping integration process. When Φ_5 is at a high level, as shown in Fig. 3(a), C_{N3} and C_{N4}, as well as C_{P3} and C_{P4}, are connected in series to form charge pumps. Then, they are respectively

connected in parallel with C_{INTN1} and C_{INTP1} to realize charge sharing for voltage integration. Due to the charge sharing and the law of conservation of charges, the following equation can be derived:

$$V_{res}(z)(C_{N3}+C_{N4})z^{-1}+V_{int1}(z)C_{INTN1}z^{-1} = V_{int1}(z)\left(C_{INTN1}+\frac{C_{N3}C_{N4}}{C_{N3}+C_{N4}}\right) \quad (1)$$

where V_{int1} is the first-order integration voltage on C_{INTN1}.

Subsequently, when Φ_6 is at a high level, as shown in Fig. 3(b), C_{N4} (C_{P4}) is connected in parallel with the capacitance of $C_{INTN1,2}$ ($C_{INTP1,2}$) in series to realize second time of charge sharing for voltage integration. The following equation can be derived:

$$\frac{1}{2}V_{int1}(z)C_{N4}+V_{int1}(z)C_{INTN1}+\frac{1}{2}V_{int2}(z)C_{INTN2}z^{-1} = V_{int2}(z)\left(C_{N4}+\frac{C_{INTN1}C_{INTN2}}{C_{INTN1}+C_{INTN2}}\right) \quad (2)$$

where V_{int2} is the second-order integration voltage on C_{INTN1} and C_{INTP1} in series.

When Φ_4 is at a high level in the next sampling cycle, $C_{N3,4}$ and $C_{P3,4}$ serve as residue voltage collecting capacitors. $C_{N1,2}$ and $C_{P1,2}$ participate in the noise-shaping integration process, which is identical to the operation of capacitors $C_{N3,4}$ and $C_{P3,4}$ in the previous cycle.

After noise shaping, V_{int2} and the input voltage V_{in} are summed together and fed into the comparator input. Due to the quantization noise Q introduced during the comparator quantization phase, the ADC output D_{out} can be expressed as follows:

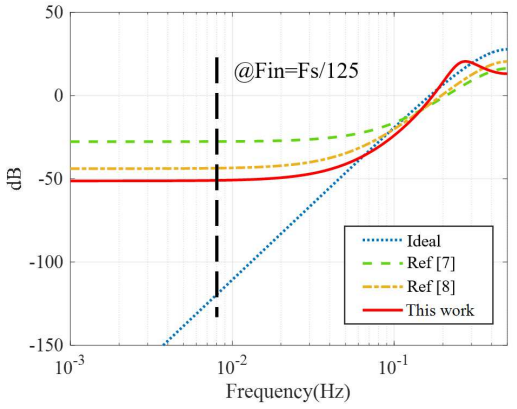

Fig. 4. NTF characteristics of the proposed and previously reported NS techniques.

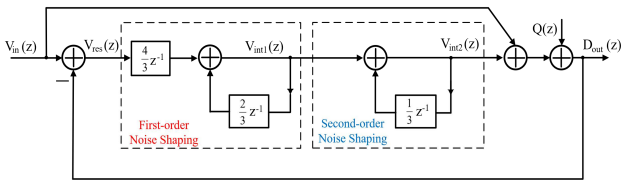

Fig. 5. Signal flow diagram of the proposed NS-SAR ADC.

$$D_{out}(z)=V_{int2}(z)+V_{in}(z)+Q(z) \quad (3)$$

Based on (1), (2) and (3), the following relationship can be derived:

$$D_{out}(z)=V_{in}(z)+\frac{(1-\frac{2}{3}z^{-1})^2}{1+\frac{4}{9}z^{-2}}Q(z) \quad (4)$$

It can be observed that this fully passive noise-shaping SAR ADC achieves a second-order noise-shaping function. The NTF is given by $(1-\frac{2}{3}z^{-1})^2 \Big/ (1+\frac{4}{9}z^{-2})$.

Fig. 4 shows the NTF characteristics of the proposed noise-shaping technique. The structure suppresses in-band quantization noise by up to −52dB. It improves the suppression of in-band quantization noise by 8dB compared to $(1-\frac{2}{3}z^{-1})^2$ in [8]. Fig. 5 shows the signal flow diagram of the proposed NS-SAR ADC.

B. Split-segmented CDAC Array

As the resolution of the ADC increases, the total capacitance value in the capacitor array grows exponentially. The capacitance of the most-significant-bit (MSB) is 2^N times that of the least-significant-bit (LSB). Segmenting the capacitor array can alleviate the issue of large capacitor ratios and reduce the total capacitance. Fig. 6 illustrates a two-segment CDAC array.

In this design, the CDAC is set to 8 bits, with a 4-bit main array and a 4-bit subarray. In the segmented architecture, the size of the bridge capacitor is a fraction of the unit capacitance, ensuring that the subarray collectively match the LSB capacitance in the main array. The total capacitance value of the segmented array is significantly smaller than that of the non-segmented array, which helps reduce the overall capacitance and lower power consumption. The area of the segmented capacitor array is only 18.86% of the conventional 8-bit CADC array.

The monotonic switching sequence differs from the traditional capacitor switching sequence. It employs a "compare-first, set-later" approach, which avoids ineffective switch transitions and reduces the number of comparisons and setting operations. It improves the overall ADC conversion speed and reducing power consumption. The split capacitor array replaces each single capacitor with two parallel

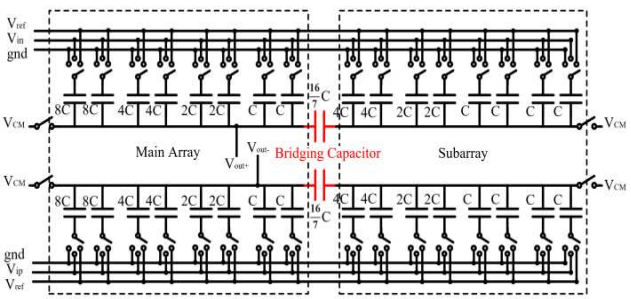

Fig. 6. The proposed split-segmented CDAC array.

capacitors, as shown in Fig. 6. By changing the switch connections of the two capacitors to different voltage levels while maintaining the same capacitance value, the monotonic switching sequence effect is achieved. Moreover, the split CDAC can effectively improve the dynamic range of the ADC. By dividing the array into two parts, a smaller unit capacitor sizes can be obtained, which reduces thermal noise and improves the signal-to-noise ratio (SNR) [10]. The proposed split-segmented CDAC also adopts the bottom-plate sampling technique, which eliminates the nonlinear sampling error caused by the charge injection effect.

III. Simulation Results and Discussion

The proposed second-order noise-shaping SAR ADC is implemented using a 180nm CMOS process, and the layout area is $0.3 \times 0.28\text{mm}^2$. This ADC consumes 86µW at a supply voltage of 1.2V. The power consumption breakdown of each block is illustrated in Fig. 7.

As shown in Fig. 8, when the input signal is a sine signal of 38kHz, the sampling rate of ADC is 10MS/s, the output spectrum density shows that SNDR is 92.66dB, corresponding to an ENOB of 15.1bit. This result is obtained through simulations based on the FFT analysis method with the application of the Blackman window. The number of FFT points is 4096. It validates the effectiveness of the proposed technique.

The performance comparison with previous noise-shaping ADCs is given in Table I. Due to its specific application, the bandwidth and power consumption of the proposed design are significantly lower than [3], [4]. Compared to the NS-SAR ADCs used for the biomedical applications in [7], [9], the proposed design demonstrates a superior SNDR performance while occupying a smaller area. The proposed design achieves a better FoM_s compared to these noise-shaping ADCs. However, our FoM_w is inferior to [9], because it employs an excellent 14nm FinFET process.

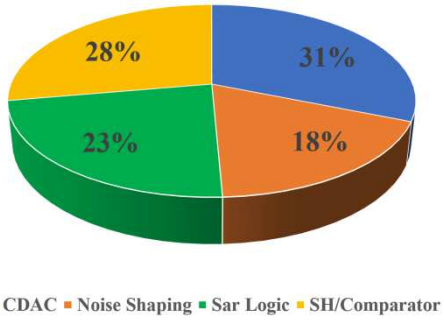

Fig. 7. Breakdown of simulated power consumption for each block.

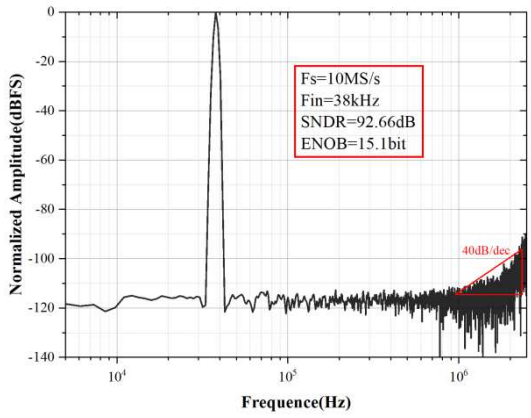

Fig. 8. Simulated spectral density of the proposed ADC for a 38kHz input signal sampled at 10MS/s.

TABLE I. Performance Summary and Comparison

Specifications	*[3]	**[4]	*[7]	*[9]	*[11]	**This work
Technology (nm)	180	65	40	14	28	**180**
Supply (V)	1	1	1.1	0.9	1	**1.2**
Sampling rate (S/s)	10k	10k	8.4M	320M	2M	**10M**
Bandwidth (kHz)	0.625	0.2	262	40000	100	**80**
Original bit	7	8	8	10	8	**8**
SNDR(dB)	65	74.8	80	66.6	87.6	**92.66**
ENOB(bit)	10.5	12.1	13	10.8	14.3	**15.1**
Power(µW)	0.09	0.1	143	1250	120	**86**
Area(mm^2)	0.12	0.13	0.04	0.002	0.02	**0.084**
FoM_s(dB)	163.5	168	173	171.6	177	**182.3**
FoM_w (fJ/conv.-step)	50	56	33	8.9	30	**15**

*Measurement Result **Simulation Result

IV. Conclusion

This paper proposes a fully passive second-order NS-SAR ADC. By using an 8-bit V_{CM}-based SAR ADC, a 15.1-bit ADC suitable for action potential signal detection is realized. To achieve high energy efficiency and minimal area consumption, the proposed design employs passive residue voltage summation and ping-pong residue voltage switching techniques to implement the noise-shaping functionality. The utilization of a split-segmented CDAC further reduces circuit power consumption and area overhead. The FoM_s and FoM_w of the proposed second-order NS-SAR ADC are 182.3dB and 15fJ/conv.-step respectively. It consumes 86µW from a 1.2V supply at 10MS/s. The SNDR is 92.66dB, corresponding to an ENOB of 15.1bit. Simulation results demonstrate that the proposed NS-SAR ADC achieves a favorable trade-off between conversion accuracy and power consumption.

References

[1] K. Sun, H. Wu, and J. Liu, "Modeling for Low Power Bypass Window SAR ADC Based on Highest Weight Capacitor Splitting," in *IEEE 2023 International Conference on Electronics, Circuits and Systems (ICECS)*, Dec. 2023, pp. 1-4.

[2] F. Yan and J. Liu, "Analog Front-End Input-Impedance Boosting Techniques for Bio-Potential Monitoring—A Review," *IEEE Transactions on Instrumentation and Measurement*, vol. 73, no. 2002214, pp. 1-14, Feb. 2024.

[3] J. Hu, D. Li, M. Liu and Z. Zhu, "A 10-kS/s 625-Hz-Bandwidth 65-dB SNDR Second-Order Noise-Shaping SAR ADC for Biomedical Sensor Applications," *IEEE Sensors Journal*, vol. 20, no. 23, pp. 13881-13891, Dec. 2020.

[4] Y. Tian and J. Yin, "An Area-Efficient Dynamic-Comparator-Reuse Noise-Shaping SAR ADC for Biosensor System," *IEEE Sensors Journal*, vol. 7, no. 11, pp. 1-4, Nov. 2023.

[5] K. Sun, F. Yan, and J. Liu, "A 0.6V 10-bit 20kHz Capacitor Splitting Bypass Window SAR ADC for Biomedical Applications," in *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, Nov. 2023, pp. 256-260.

[6] J. A. Fredenburg and M. P. Flynn, "A 90-MS/s 11-MHz-bandwidth 62-dB SNDR noise-shaping SAR ADC," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2898-2904, Dec. 2012.

[7] W. Guo, H. Zhuang, and N. Sun, "A 13b-ENOB 173dB-FoM 2nd-order NS SAR ADC with passive integrators," in *IEEE 2017 Symposium on VLSI Circuits*, Jun. 2017, pp. 236-237.

[8] H. Zhuang, W. Guo and J. Liu, "A Second-Order Noise-Shaping SAR ADC With Passive Integrator and Tri-Level Voting," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 6, pp. 1636-1647, Jun. 2019.

[9] Y. Lin and C. Lin, "A 40MHz-BW 320MS/s Passive Noise-Shaping SAR ADC with Passive Signal-Residue Summation in 14nm FinFET," in *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2019, pp. 330-332.

[10] Y. Shu, L. Kuo and T. Lo, "An Oversampling SAR ADC With DAC Mismatch Error Shaping Achieving 105 dB SFDR and 101 dB SNDR Over 1 kHz BW in 55 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 2928-2940, Sep. 2016.

[11] L. Jie and B. Zheng, "A 4th-Order Cascaded-Noise-Shaping SAR ADC with 88dB SNDR Over 100kHz Bandwidth," in *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2020, pp. 160-162.