Novel Structure of Dynamic CMOS Comparator with High Energy Efficiency

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***Abstract*—This article presents an energy-efficient dynamic CMOS comparator. By incorporating two additional NMOS transistors into the conventional Strong ARM (SA) structure, this design significantly reduces energy consumption as the differential voltage increases. Furthermore, it markedly improves key technical parameters such as precision, offset, and noise. Manufactured using a 180 nm CMOS process, the proposed comparator achieves 84 μV input-referred noise while consuming only 4.683-nW per comparison under a 1.2-V supply. This results in a figure of merit (FoM) of 0.033 nJ·μV², representing a 53.36% reduction in power consumption compared to the conventional SA latch. These improvements are essential for energy-sensitive applications, enhancing system performance and minimizing power usage.**

Keywords—strong ARM (SA), dynamic comparator, low-noise, low-power, high-precision, energy efficient, ADC.

I. INTRODUCTION

Comparators, as the core modules of analog-to-digital converters (ADCs), are used to convert the comparison results between analog signals and reference signals into digital signal outputs. With the increasing demand for low-power and low-noise ADCs, researchers have turned their attention to the dynamic comparator to meet these requirements [1-4]. This comparator primarily uses positive feedback to achieve the comparison of differential input signals, and it features short transmission times, rapid comparison speeds, and low power consumption [5-8]. These attributes are crucial for reducing the power consumption of ADCs and improving their performance. The SA comparator, a classic dynamic comparator structure, is characterized by its zero static power consumption, high comparison speed, and rail-to-rail output capabilities [7]. It is widely employed in low-power designs with moderate noise requirements. However, the energy efficiency of this comparator is somewhat limited due to the large internal voltage swing that occurs during the comparison process, which is attributed to significant parasitic capacitance.

Currently, some studies have improved the energy efficiency of the dynamic comparators by refining the conventional SA structure. L. Filippini demonstrates that the power consumption of the proposed adiabatic-driven SA (ADSA) comparator is only 28% to 55% compared to the conventional SA [9]. However, ADSA cannot resolve voltages as small as SA, making it only suitable for low-resolution ADCs. Another technique for enhancing energy efficiency is dynamic biasing, which can reduce the power consumption of the pre-amplifier under a given signal-to-noise ratio requirement, achieving a 2.5-fold improvement in energy efficiency [10]. Yet, due to the longer operating time under subthreshold conditions, comparators with dynamic biasing tend to have higher delay. A floating inverter amplifier (FIA)-based design is proposed in [11]. Through current reuse, it achieves output common-mode voltage insensitivity, improving energy efficiency by a factor of 7 compared to conventional SA comparators. R. Chen presents a gain-boosted dynamic comparator structure that, compared to the conventional two-stage comparator, achieves a 19% reduction in noise, 35% reduction in power, and 75% reduction in internal capacitance [12]. A. T. Ramkaj introduced the TLFF (Triple-Latch Feed-Forward) structure in [13]. By avoiding stacked latches and leveraging the multi-stage characteristics of cascaded latches, the TLFF structure achieves high gain while reducing delay and improving speed through parallel feed-forward paths. Nonetheless, compared to single-stage comparators, the structures designed in [11-13] increase the complexity and area occupation of the circuit. Furthermore, comparators are required to have extremely low noise levels to ensure high resolution [14]. S. K. Dey optimizes noise performance while maintaining the same area and power consumption by distributing additional capacitors between the integration and regeneration nodes, thereby enhancing the energy efficiency and noise reduction [15]. Additionally, M. Venkatesh opts to use programmable reservoir capacitors [16], dynamically adjusting the input-referred noise and power during the conversion cycle to reduce noise bandwidth and input-referred noise voltage. However, a longer integration time would inevitably lead to a certain degree of speed degradation.

This paper, based on the conventional SA structure, proposes a comparator that achieves a simple dynamic CMOS structure by adding only two NMOS transistors. At a power supply voltage of 0.6 V, the power consumption per comparison is 4.683-nW. The proposed comparator demonstrates significant improvements compared to the conventional SA comparator. Specifically, it consumes 53.36% less power and has 22.76% lower input-referred noise. Additionally, the comparator precision is improved by 75.69%, and the calculated energy efficiency is increased by 72.03%. As the input differential voltage increases, the power consumption advantage of the proposed comparator becomes

more pronounced. The dual optimization of power consumption and performance makes this comparator highly suitable for low-power, high-performance ADC applications. The rest of this paper is organized as follows. Section II presents the architecture and working principles of the conventional SA comparator and the proposed comparator. Section III analyzes the comparator performance from the perspectives of technical parameters. Section IV presents the simulation results, and section V provides a conclusion.

II. Dynamic Comparator Principle

A. Conventional SA Comparator

The conventional SA latch consists of a tail current transistor, input differential pair, positive feedback latch structure, and reset transistors [7]. Its operation can be divided into four phases: reset phase, amplification phase, comparison phase, and latch phase. To further reduce the power consumption of the CMOS dynamic comparator architecture, Z. Zhu has made optimizations to the conventional SA structure, as illustrated in Fig. 1 [3]. This structure is considered a derivative of the conventional SA comparator. In this circuit, the clock controls the tail current transistor M0 and PMOS transistors M9 and M10, while transistors M1 and M2 act as a common-source amplifier, capable of amplifying the input signals V_{IN} and V_{IP}, respectively. The NMOS transistors M3, M4, M7, and M8 form a back-to-back inverter structure within the circuit, and PMOS transistors M9 and M10 perform the reset operation.

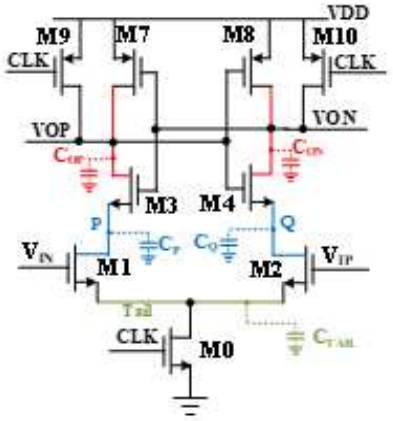


Fig. 1. Conventional SA Circuit

B. Proposed Comparator

Fig. 2 shows the schematic diagram of the proposed comparator. During the reset phase, the CLK is at a low level. At this point, the NMOS transistor M0' is off, resulting in almost no current flowing through the tail current transistor M0' to ground; the PMOS transistors M9' and M10' are on, causing the output terminals V_{OP} and V_{ON} to approach the power supply voltage V_{DD}; M5' and M6' are off. When the CLK is high, the comparator enters the amplification phase, with M0' being activated and M9' and M10' being turned off. The differential voltage is input to the NMOS transistors M1' and M2', under the assumption that V_{IN} is greater than V_{IP}. Based on the subthreshold voltage-current relationship pointed out in Eq. (1) [3], it can be deduced that the discharge rate at point P' is greater than that at point Q'. When V_P drops to V_{DD} - V_{THN} (where V_{THN} is the threshold voltage of M3' and M4'), M3' turns on first, followed by M4', entering the comparison phase. After M3' and M4' are both conducting, the node voltage V_{OP} drops faster than V_{ON}. When V_{OP} drops to V_{DD} - V_{THP} (where V_{THP} is the threshold voltage of M7' and M8'), M8' turns on before M7', entering the latch phase. Finally, similar to the conventional SA comparator, the proposed comparator completes a working cycle by the positive feedback of the latch, pulling the output voltage V_{ON} up to V_{DD} and V_{OP} down to 0.

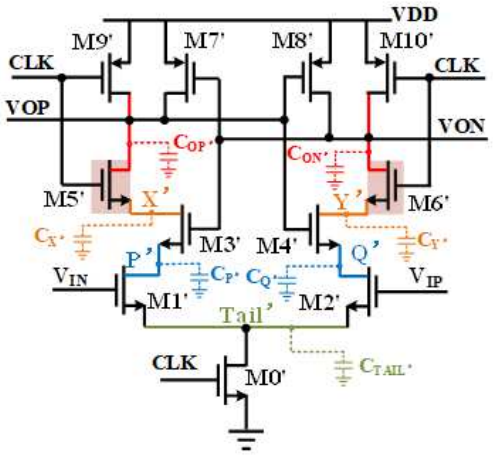


Fig. 2. Proposed Comparator Circuit

$$I_{M1',2'} = \frac{W_{1',2'}}{L_{1',2'}} I_0 \cdot e^{\frac{(V_{GS1',2'} - V_{TH1',2'})}{nV_{T1',2'}}} \left[1 - e^{-\frac{V_{DS1',2'}}{V_{T1',2'}}}\right] \approx \frac{W_{1',2'}}{L_{1',2'}} I_0 \cdot e^{\frac{(V_{GS1',2'} - V_{TH1',2'})}{nV_{T1',2'}}} \left(V_{DS1',2'} \geq V_{T1',2'}\right) \quad (1)$$

The difference is that, during the reset phase, in the conventional SA comparator, C_P, C_Q, C_{OP}, and C_{ON} all charge, whereas in the proposed circuit, due to the low-level clock controlling the NMOS transistors M5' and M6', only $C_{OP'}$ and $C_{ON'}$ are charging during this phase. When the clock goes high, during the amplification phase, the input signal enters M1' and M2', and the parasitic capacitors $C_{P'}$ and $C_{Q'}$ have a brief charging process. At the same time, $C_{OP'}$ and $C_{ON'}$ in the circuit also briefly charge $C_{X'}$ and $C_{Y'}$, while $C_{TAIL'}$ charges and discharges rapidly. In the next phase, when M3' and M4' conduct, $C_{P'}$ and $C_{Q'}$ both discharge. If M3' turns on relatively faster than M4', then $C_{X'}$ discharges while $C_{Y'}$ continues to charge, and vice versa.

III. Technical Parameters Analysis

A. Power Consumption

The power consumption is influenced by the node capacitance, power supply voltage, and clock cycle [7]. Combining the changes in node voltages ΔV_P, ΔV_Q, ΔV_{OP}, ΔV_{OQ}, as well as the change in voltage ΔV_{TAIL} across the tail current transistor and the parasitic capacitance C_{TAIL} at that node, the energy consumption of the conventional SA circuit can be expressed as Eq. (2).

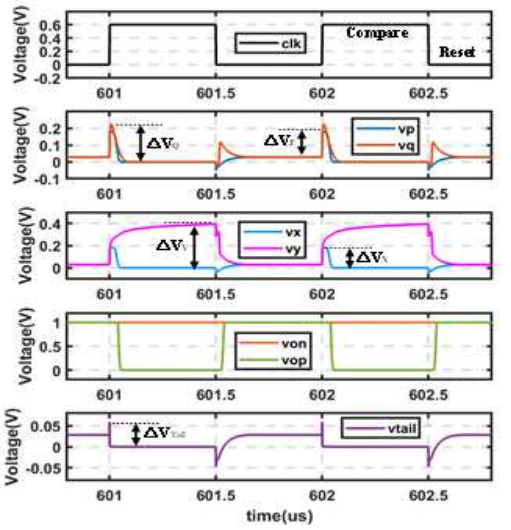
$$E_{SA} = C_P \Delta V_P^2 + C_Q \Delta V_Q^2 + C_{OP} \Delta V_{OP}^2 + C_{ON} \Delta V_{ON}^2 + C_{TAIL} \Delta V_{TAIL}^2 \quad (2)$$

$$E_{PRO} = C_{P'} \Delta V_{P'}^2 + C_{Q'} \Delta V_{Q'}^2 + C_{X'} \Delta V_{X'}^2 + C_{Y'} \Delta V_{Y'}^2 + C_{OP'} \Delta V_{OP'}^2 + C_{ON'} \Delta V_{ON'}^2 + C_{TAIL'} \Delta V_{TAIL'}^2 \quad (3)$$

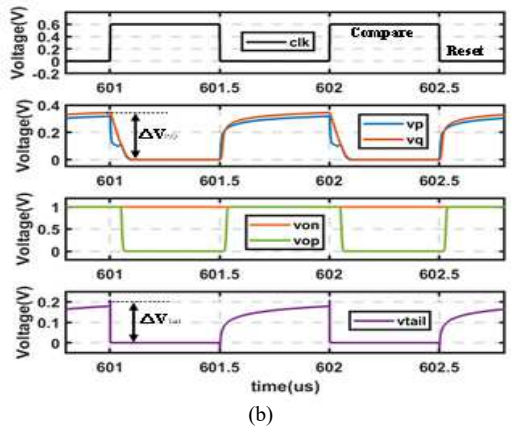
In the proposed circuit, the two NMOS transistors M5' and M6' introduce parasitic capacitances $C_{X'}$ and $C_{Y'}$ at nodes X'

and Y', respectively. The energy consumption can be expressed as Eq. (3). In Eq. (3), the power consumption of the proposed comparator is composed of the sum of the power dissipated by the parasitic capacitance charging and discharging at nodes P', Q', OP', OQ', X', and Y', as well as at the tail current node. During the reset and comparison processes, the voltage changes at points X', Y', P', and Q' in the proposed comparator are $\Delta V_{X'}$, $\Delta V_{Y'}$, $\Delta V_{P'}$, $\Delta V_{Q'}$, respectively.

Fig. 3 shows the simulated node voltage results when the input signal is a full differential input of 0 to 600 mV. Under the same differential input signal and comparison speed, the power consumption of the conventional SA comparator is mainly due to the charging and discharging at nodes P, Q, OP, ON, and the tail current node. In contrast, in the proposed circuit, only nodes ON', OP', and one of the nodes X' or Y' undergo a complete charging and discharging process, similar to the conventional SA circuit. The remaining nodes P', Q', the tail current and the other nodes X' or Y' only undergo a rapid charging and discharging process with a relatively small change in value, consuming much less power than a complete charge-discharge cycle. As a result, the power consumption of the proposed comparator is significantly reduced.



(a)



(b)

Fig. 3. Voltage at Various Nodes: (a) Proposed Circuit (b) Conventional SA Circuit

Additionally, Eq. (4) is another method for power consumption analysis in simulations. Fig. 4 shows the simulation results of the current when the differential voltage is 100 mV. The average current of the proposed comparator is lower than that of the conventional SA comparator. The power consumption calculated using this method will also be smaller, thus reflecting the energy efficiency advantage of the proposed comparator.

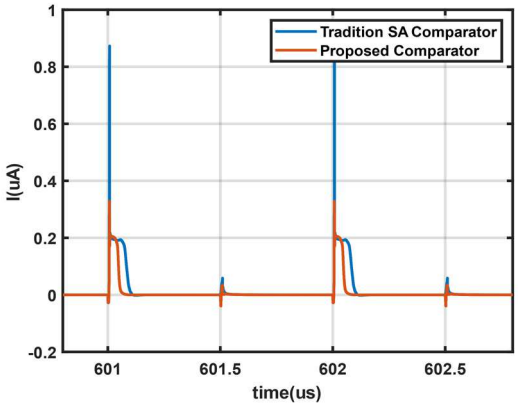


Fig. 4. Variation of Tail Current I_D

$$P_{pro} = V_{DD} \cdot average(I_D) \tag{4}$$

B. Noises

Considering the detailed analysis and derivation from [17], a noise analysis model for the comparator in the subthreshold state of each transistor in the proposed circuit can be established. The total input noise can be expressed as the sum of the noise contributions from each transistor is shown in Eq. (5).

$$\overline{v_{\text{pro},in}^2} = \overline{v_{M1,2}^2} + \overline{v_{M3,4,7,8}^2} + \overline{v_{M9,10}^2} + \overline{v_{M5,6}^2} \tag{5}$$

The above groups the MOS transistors to obtain four main noise contributions. More specifically, based on the comprehensive noise modeling process described in [17], the output noise of the working process in Section II.B of this paper is derived and then divided by the equivalent gain of the entire circuit. In input-referred noise expressions Eq. (6)-(9), the structure of KT/C is present. This term represents the thermal noise component in capacitive circuits, where K is the Boltzmann constant, T is the absolute temperature, and C is the capacitance.

$$\overline{v_{M1,2}^2} = \frac{2kT\gamma \cdot V_{ov1,2}}{C_{P,Q} \cdot \Delta V_{P,Q}} \tag{6}$$

$$\overline{v_{M5,6}^2} = \frac{kT}{2C_{X,Y}} \left(\frac{V_{ov1,2}}{\Delta V_{P,Q}}\right)^2 \tag{7}$$

$$\overline{v_{M3,4,7,8}^2} = \frac{kT\gamma V_{ov3,4} \cdot \Delta I_{P,Q}}{2C_{P,Q} I_{D3} \cdot \Delta V_{OP,OQ}} \cdot \left(\frac{V_{ov1,2}}{\Delta V_{P,Q}}\right)^2 + \frac{kT\gamma C_{OP,OQ}}{8C_{P,Q}} \cdot \left(\frac{V_{ov1,2} V_{ov3,4} \cdot \Delta I_{P,Q}}{I_{D3} \cdot \Delta V_{OP,OQ}}\right)^2 \tag{8}$$

$$\overline{v_{M9,10}^2} = \frac{kT}{2C_{OP,OQ}} \left(\frac{V_{ov1,2}}{\Delta V_{P,Q}}\right)^2 + \frac{kTV_{ov3,4} \cdot \Delta I_{P,Q}}{2C_{P,Q} I_{D3} \cdot \Delta V_{OP,OQ}} \cdot \left(\frac{V_{ov1,2}}{\Delta V_{P,Q}}\right)^2 + \frac{kTC_{OP,OQ}}{8C_{P,Q}} \cdot \left(\frac{V_{ov1,2} V_{ov3,4} \cdot \Delta I_{P,Q}}{I_{D3} \cdot \Delta V_{OP,OQ}}\right)^2 \tag{9}$$

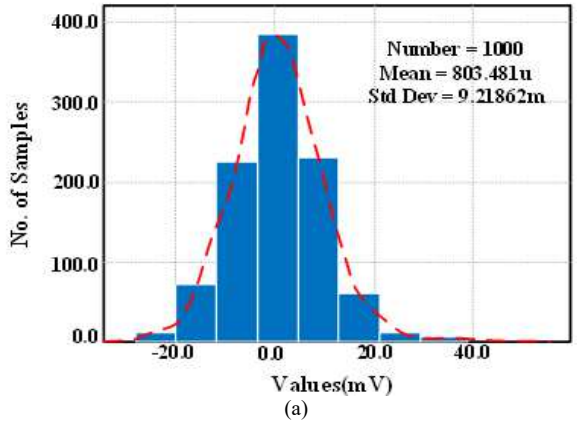
Where $V_{OV1,2} = V_{GS1,2} - V_{TH1,2}$ is the overdrive voltage of M1' and M2', and $V_{OV3,4} = V_{GS3,4} - V_{TH3,4}$ is the overdrive voltage of M3' and M4'. I_{D1} and I_{D3} are the current magnitudes flowing through M1' and M3' in the subthreshold state, respectively. $\Delta V_{P,Q}$ is the change in voltage at nodes P' and Q', and $\Delta I_{P,Q} = I_{D3} - I_{D1}$ is the current flowing into the parasitic capacitance $C_{p'}, Q'$.

Based on the input-referred noise expression, it is observed that although transistors M5' and M6' are added in the proposed circuit, the total noise is actually reduced. This is because, by examining the voltage and current changes as shown in Fig. 3 and Fig. 4, the magnitude of voltage changes is on the order of the first decimal place, while the current changes in the proposed circuit have been reduced from the microampere level to the nanoampere level compared to the conventional SA circuit. In the expression for input-referred noise, the noise magnitude of transistors M3', M4' and M7' to M10' is strongly correlated with the current changes. Therefore, despite the addition of noise from transistors M5' and M6', the overall noise contribution from the M3', M4' and M7' to M10' transistors is significantly reduced. This allows the proposed circuit to achieve a trade-off between low noise and low power consumption.

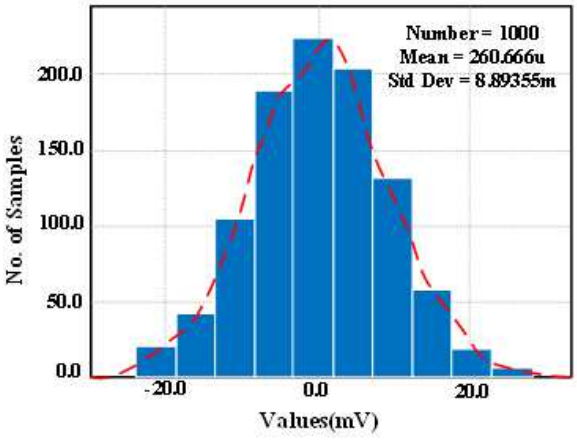
C. Accuracy and Offset

Enhancing the comparator's precision means it can more accurately discern subtle changes in input differential voltage, thereby outputting more precise comparison results. Since the gain of the input signal is inversely proportional to the size of the tail current [7], and combining the simulation results obtained from Fig. 4, it can be seen that the tail current of the proposed comparator is much smaller than that of the conventional SA comparator. Therefore, the gain of the proposed comparator is much greater than that of the conventional SA comparator. As a result, the proposed comparator can further amplify small input signals, achieving an improvement in precision. The proposed dynamic comparator reduces tail current without compromising speed. Unlike conventional SA comparators, where voltage changes on both sides lead to higher current and power consumption (as shown in Fig. 3), the proposed design involves voltage changes on only one side, thereby significantly lowering the tail current. The comparator's speed remains unaffected due to its reliance on the input signal amplitude and positive feedback mechanism.

Based on the analysis in [3], for input differential pairs where the offset voltage is independent of the common-mode voltage V_{CM}, it is advisable to increase their size. For transistors M3'-M8', which are closely related to V_{CM}, reducing the ratio W/L effectively can minimize comparator offset. Moreover, to realize interdigitated symmetry, parameter "M" of M1'-M2' is set to 2. Since M9'-M10' are inactive during the comparison phase and M0' does not participate in the differential branch, their influence on the offset voltage is negligible. By examining the 1000-point Monte Carlo simulation results in Fig. 5, it can be seen that the mean value of the proposed comparator is smaller than that of the conventional SA circuit, indicating that the offset of the proposed comparator is smaller, making the system more stable and the performance better.



(a)



(b)

Fig. 5. 1000-point Monte Carlo Simulation of (a) Conventional SA Circuit (b) Proposed Circuit

IV. Simulation Results

In the circuits shown in Fig. 1 and Fig. 2, the supply voltage V_{DD} is 0.6 V. By adjusting the length-to-width ratio of the MOS transistors at the input and latch of the circuit, the precision of both circuits is optimized to the best. Fig. 6 presents the results of the transistor-level simulation of power consumption, which shows that when comparing differential voltages of the same magnitude, the proposed comparator consumes less power than the conventional SA comparator, whether at low or high differential voltages. Moreover, at high differential voltages, the power consumption of the proposed comparator decreases more significantly, demonstrating a more pronounced advantage. The output noise curve of the comparator is shown in Fig. 7. The input-referred noise (IRN) can define the minimum value of the input signal. By considering the amplification factor of the circuit for the input signal, the input-referred noise result for the comparator can be obtained.

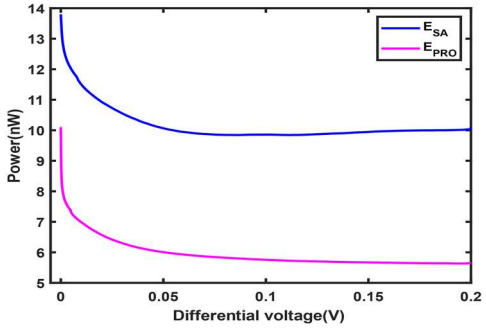


Fig. 6. Power Consumption Variation with Differential Voltage

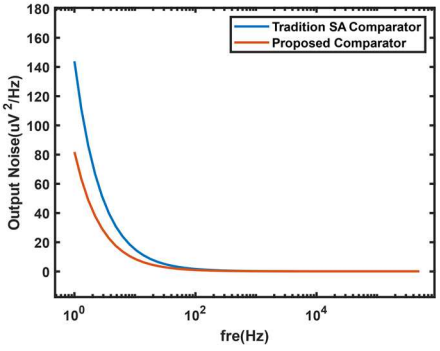


Fig. 7. Output Noise Curve

TABLE I. Comparison of Key Parameters Between Proposed and Conventional Designs

Parameters	Proposed	SA
Precision(μV)	6.915	28.45
Noise (μVrms)	84	108.75
Power(nW)	4.683	10.04
Energy(pJ /comparison)	0.0047	0.01
FoM (nJ•μV²)	0.033	0.118

TABLE II. Comparison of Parameters with Other Papers

	This work		[11]	[18]
Architecture	Proposed	SA	FIA	SA
Process(nm)	180	180	180	180
Supply(V)	0.6	0.6	1.2	1.2
Noise (μVrms)	84	108.75	46	62
Energy(pJ /comparison)	0.0047	0.01	1	4.1
Clock (MHz)	1	1	-	-
FoM (nJ•μV²)	0.033	0.118	2.07	15.8

$$FoM(nJ \cdot \mu V^2) = Energy(pJ/comparison) \cdot Noise\_power(\mu V^2) \cdot 10^{-3} \quad (10)$$

Table I summarizes the key differences in parameters between the proposed and conventional designs. Table Ⅱ presents a comparison of the performance of the proposed comparator with other dynamic comparators. (10) is the calculation for the FoM [11]. Although the noise of the comparator proposed in this paper and the conventional SA comparator is slightly higher than the two circuits presented in [11], the circuit proposed in this paper significantly reduces energy consumption and enhances precision, achieving a balance among the three parameters. Furthermore, the power consumption results of this paper are similar to those in [18], but with significantly reduced noise, thus achieving the optimal FoM result.

V. Conclusion

This paper proposes a novel structure of dynamic CMOS comparator with high energy efficiency. It achieves high precision and low power consumption while meeting the requirement of low input-referred noise. Compared to the conventional SA comparator, this dynamic comparator can achieve a 53.36% reduction in power consumption, a 22.76% decrease in input-referred noise, a 75.69% improvement in comparator precision, and a 72.03% enhancement in FoM. The proposed comparator can improve the overall energy efficiency of ADCs. This comparator can be further applied to high performance and low power ADC systems to improve the efficiency of devices such as wearable medical devices or IoT sensors.

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