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Optical receiver front end for optically powered smart dust‡

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SUMMARY

The ability to create and direct beams of light means that optical communications potentially offer a large power advantage over RF communications for sensor networks. This paper presents an optically powered receiver front end for wireless optical communications. A complete optical receiver front end including a photodetector, clock and Manchester data recovery circuits has been fabricated using the UMC 180 nm CMOS process. A novel modulation scheme is described that has been devised so that this front end can recover the clock and Manchester data from an optical beam. Experimental results show that the total current consumption of the optical receiver front end is as low as 18.8 nA for a 0.5 V supply when a 1 kbps Manchester data and 8 kHz clock signal are successfully recovered. This means that photodiodes on the same substrate as the front end circuits extract enough power from the communications beam to allow the front end to work at distances of up to 10 m from the transmitter. Copyright © 2013 John Wiley & Sons, Ltd.

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KEY WORDS: Manchester codes; optical receiver; photodiodes; smart dust; weak inversion; wireless sensor network

1. INTRODUCTION

WIRELESS microsensor networks have been recognized as one of the most important technologies in the 21st century [1]. These networks consist of a large number of small self-powered sensor nodes, which are able to collect information or detect certain events and communicate with other similar nodes, a base station (BS) or an external network. Microsensors have broad applications, such as environment and habitat monitoring, agriculture monitoring, security, education and micro-surgery. Wireless sensors therefore can have very wide applications in different fields, but they share some common characteristics. First, the sensors should be as small as possible. Second, the sensors must be inexpensive, because large numbers of nodes in the wireless sensor network are required to ensure coverage and connectivity. Third, the wireless sensors need to have their own power source. Power can be either from the pre-charged batteries, or the energy harvested from the environment. This means that energy consumption should be small.

Most sensor networks use radio communication between nodes [2–8]. However, radio communications are inefficient due to the high path loss and low efficiency of the small antennas.

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Moreover, RF transceivers have high power consumption, due to the typically used complicated transceiver designs [9]. In the passive RFID system, the architecture of transponder is simpler than conventional RF receivers. Moreover, the power consumption of transponder chips can be as low as 5 μW [10]. In order to achieve the power at the transponder chip, the reader's transmission power should be as high as 0.5 W EIRP (Effective Isotropic Radiated Power) with the consideration of 40 dB path loss and 10% rectifier efficiency. With the 40 dB path loss, the communication distance is only 3 m for 868 MHz or 1 m for 2.45 GHz [11]. Using optical communications for sensor networks offers a potentially large power advantage over RF because of the ability to direct beams of light. In this case, a 40 dB path loss corresponds to a communication distance of approximately 20 m [12]. A smart dust (SD) element is a self-contained sensing and communication system that can be integrated into cubic-millimetre motes that create massively distributed sensor networks [13–15]. Furthermore, due to the small size of the SD, there is no enough space for an efficient RF antenna. It has to be noted that for some terrestrial applications, the optical communication has some limiting factors, such as line of sight, beam dispersion and atmospheric absorption. These factors may cause an attenuated receiver signal and lead to higher bit error ratio. Some solutions have been found to overcome these issues, including multi-beam or multi-path architectures, which use more than one transmitter and more than one receiver. Although optical wireless communications has these disadvantages, it is still a promising alternative technique for sensor networks.

Our previous work has shown an optically powered photodetector in [16] and SD system results in [17, 18]. This paper focuses on the SD front end and is organized as follows. Section 2 gives the design and measurement results of power photodiodes. In Section 3, the analysis and design of a logarithmic adaptive photodetector are discussed and measurement results are presented. Furthermore, a novel modulation scheme is introduced. Section 4 describes the design of the rest of analog circuits in the front end. The measurement results of the complete optical receiver front end are shown in Section 5. Conclusions are given in Section 6.

2. POWER PHOTODIODES FOR THE SD

The SD has been fabricated using a 180 nm CMOS process available from UMC. This process starts with a p-type substrate (known as P-sub) in which a well of n-type material (the N-well) is formed. If a diode formed from the N-well and P-sub is illuminated, the open circuit voltage on a contact to the N-well will be a few hundred millivolts below the voltage of the P-sub contact. With this process, it is also possible to create a T-well, which is a well of p-type silicon inside an N-well. Hence, if a diode formed using a T-well and an N-well is illuminated, the open-circuit voltage of the T-well will be a few hundred millivolts higher than the voltage of the N-well. When this N-well is connected to the substrate, the T-well inside the N-well will generate a voltage higher than the substrate. By connecting a T-well/N-well diode in series with an N-well/P-sub diode, it is possible to generate a voltage difference that is approximately twice the voltage difference across a single diode.

To compensate for the different quantum efficiencies of the two different photodiodes, the SD is designed with a 0.2 mm^2 N-well/P-sub diode and a 1.3 mm^2 T-well/N-well diode. These two photodiodes sizes were chosen to generate enough power to support SD. Figure 1 shows the measured load lines of these two diodes illuminated with an 830 nm laser. For each of the illumination levels, the approximate maximum power point is labeled for each load line. The maximum illumination intensity, which is limited by the human eye safety, is approximately 79.45 $\mu W/mm^2$. Assuming that there is no ambient light available, the voltages at the maximum power points in Figure 1 will determine the most efficient operating voltages for the corresponding illumination intensities.

Since ambient light will only increase the available voltages, these voltages, listed in Table I, are applied when testing different circuits required for an optical receiver for a SD.

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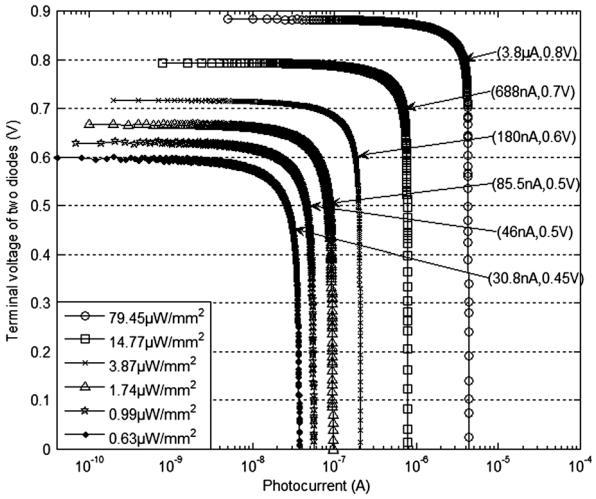

Figure 1. Measured load lines of the two series diodes in the 0.18 μm process.

Table I. Illumination intensities and the corresponding voltages and available photocurrents of the 0.18 μM process power diodes.

Illumination (μW/mm^2)	79.45	14.77	3.87	0.99	0.63
Voltage (V)	0.8	0.7	0.6	0.5	0.45
Photocurrent (nA)	3800	688	180	46	30.8

3. THE ADAPTIVE PHOTODETECTOR

To be robust to variations in the distance between the transmitter and the receiver, the photodetector that forms the first part of the optical receiver must be able to deal with large changes in the intensity of the incident light. The ideal design should also amplify the modulation in the incident laser beam that is used to form the down-link from the BS to the SD. A photodetector circuit that fulfils both these requirements is the logarithmic detector circuit. This circuit which has been used in the SD, which was originally proposed by Mahowald [19] and then studied further by Delbrück [20], is depicted in Figure 2.

In Figure 2, the current generated by M6 is mirrored to M3 by a current mirror composed of M3 and M5. This means that the bias current in M3 is not influenced by variations in the voltage supply. A buffer made from a simple PMOS source follower is used to drive the integrated circuit bond pad and measurement equipment when the photodetector circuit is tested. In this circuit, the photodiode is illuminated by an optical beam that generates such a small photocurrent that M_1 stays in the subthreshold region of operation. When the optical beam power is constant, transistor M_1 sources the constant photocurrent flowing through the photodiode and the circuit output V_2 is equal to the gate voltage required by M_1. If the beam intensity is modulated, the generated photocurrent includes a dc component I_{ph} and an ac small signal i_{ph}. The negative feedback loop in the circuit means that any small change in photocurrent could result in a large change in the output voltage V_2. Equally importantly because the load transistor M_1 is operating in the subthreshold region, any change in output voltage is proportional to the fractional change in the photocurrent.

The complete transfer function of the photodetector [16] is

$$H(s) = \frac{v_2/V_T}{i_{ph}/I_{ph}}(s) = \frac{(1+s/\omega_4)/k}{1+s/\omega_3+(1+s/\omega_1)(1+s/\omega_2)(1+s/\omega_4)/\left(k\,G_{forward}\right)} \quad (1)$$

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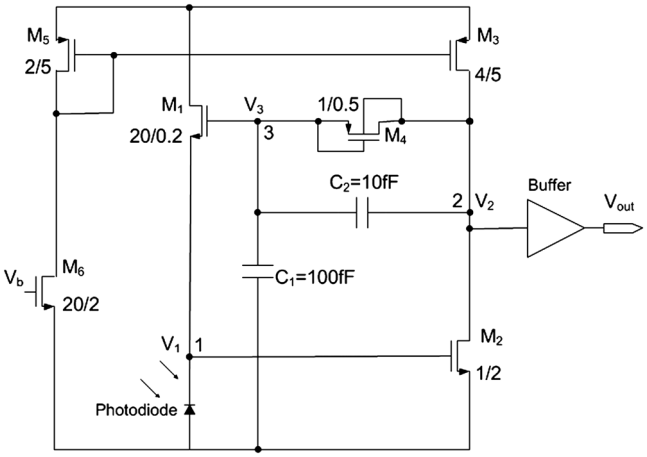

Figure 2. The photodetector circuit used as the first stage of the analog front end showing the device sizes used.

where V_T is thermal voltage, k is the capacitive coupling ratio from gate to channel of transistors and $G_{forward}$ is the gain of the amplifier formed by M_2 and M_3. ω_1 and ω_2 are two dominant poles at node 1 and node 2, respectively. The pole 1 is a function of photocurrent and so it moves as the average photocurrent varies. ω_3 and ω_4 are a pole and a zero at low frequencies caused by M_4, C_1 and C_2, and ω_3 is higher than ω_4. Eq. (1) shows that at very low frequency the gain of the photodetector is $1/\kappa$. At frequencies such that $\omega_3 < 2\pi f < \omega_2$ the third term in the denominator is small due to the large value of $\kappa_n G_{forward}$ and therefore it be ignored. Moreover, s/ω_3 and s/ω_4 are much larger than 1. Therefore, in this frequency range, the transfer function can be reduced to

$$G_{\text{detector}} = \frac{v_2/V_T}{i_{ph}/I_{ph}} = \frac{1}{\kappa} \times \frac{C_1 + C_2}{C_2} \tag{2}$$

In this case, the gain of the circuit is larger than the low frequency gain. The photodetector is therefore designed to work in this frequency range. At higher frequencies each pole causes the gain to drop by 20 dB/dec. The Bode plot of the transfer function is shown in Figure 3. To obtain a large bandwidth, the zero and pole 3 should be at very low frequencies and poles 1 and 2 should be at higher frequencies.

When the circuit in Figure 2 is manufactured, all the NMOS transistors must be T-well NMOS transistors, which are formed in T-wells rather than P-sub. The circuit was designed to operate with

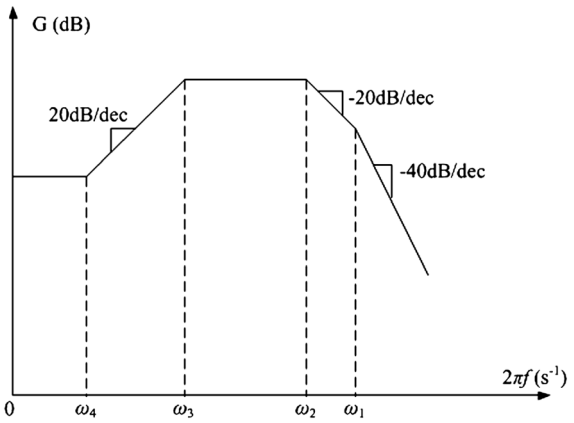

Figure 3. Bode plot of the transfer function of the photodetector.

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a bias voltage V_b of 90 mV. This voltage can generate a bias current which ensures all the transistors work in the subthreshold region. The bias current in M_3 is not influenced by variations in the voltage supply so that the frequency of pole 2 is fixed. The transistor sizes mean that the current through M_3 is set at approximately 2.6 nA and the frequency of pole 2 is at around 10 kHz. When determining the sizes of various devices, M_3 and M_5 were made large enough to improve the performance of the current mirror. The size of M_2 was chosen to ensure that M_3 and M_2 both operate in the subthreshold region for the whole range of incident photocurrents. The size of M_1 is 20 μm/0.2 μm and the ratio of width to length was kept large to make sure that M_1 operates in subthreshold. To ensure that the frequency of pole 2 is not too low, a 10 fF capacitance is used for C_2. To achieve a gain of 10 capacitance of C_1 was 100 fF. Simulation results suggest when the modulation depth of the incident light is 20% the output signal will be 65.8 mV.

The final key component of the photodetector circuit is the photodiode. The P-side of the photodiode needs to be connected to the lowest voltage of the circuit. This means that the photodiode must be made using the T-well/N-well/P-sub structure shown in Figure 4. Theoretically, there is no lower limit for the size of the photodiode. However, Delbrück found that larger diodes can give a better performance because the large photocurrent can overcome the electrical noise in the circuit [16]. However, this photodiode cannot be too large otherwise it will consume too much current from the power diodes. The photodiode in the photodetector is therefore designed to have an area of 0.015 mm^2, so that it consumes approximately 10% current of the power diodes.

Figure 5 shows a simplified experiment setup diagram. Voltage sources are not shown. A waveform representing the modulation of the laser is generated by a Matlab program and then loaded into a waveform generator (HP 33120A). The generator is used to output a voltage signal with this waveform. The minimum peak to peak value of the signal is 100 mV. This is used to modulate a laser driver (Newport 5005), which drives the 830 nm laser source. A 40 dB voltage attenuator is used between the waveform generator and laser driver in order to obtain a smaller voltage signal.

The used laser diode has a linear working range from 35 mA to 90 mA, and the modulated current through the laser diode is kept within this range. A piece of metal with a 2.5 mm diameter aperture in the centre is placed in front of the laser diode, so that a point light source is created. Two lenses are used to collimate the laser beam and focus the light. Neutral density (ND) filters are placed between the two lenses to attenuate the beam power so that the effect of different ranges on the beam can be simulated. The focused beam is directed to the IC chip by a beam splitter. There is also a microscope above the beam splitter. Through the microscope, the position of the IC chip can be adjusted so that the beam can illuminate the desired part of the chip. Before the optical test of the chip, the focused beam power is measured by an optical power meter (Newport 1830-C). Then, the optical power density can be obtained by dividing the optical power by the illumination area on the chip, which can be approximately calculated by measuring the radius of the spot magnified by a microscope and shown on a monitor.

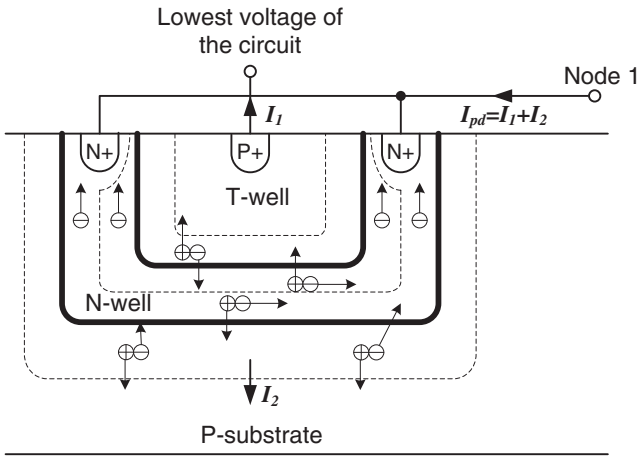

Figure 4. The photodiode in the photodetector.

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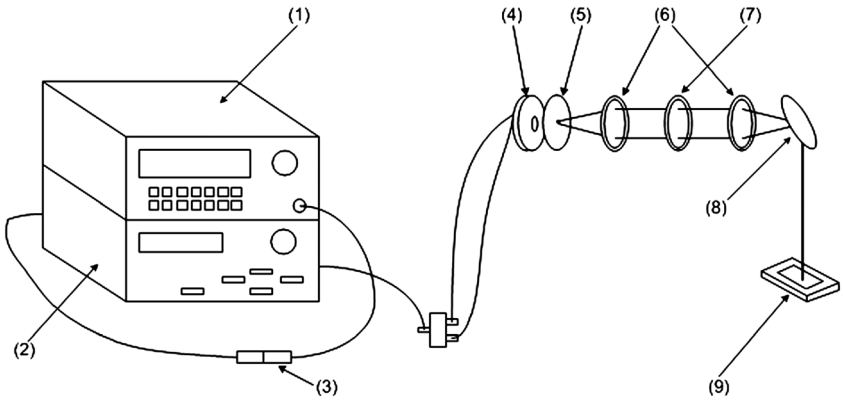

Figure 5. Simplified diagram showing the experiment setup, (1) HP 33120A arbitrary waveform generator, (2) Newport 5005 laser diode driver, (3) 40 dB attenuators, (4) laser diode, (5) metal slice with a 2.5 mm diameter aperture in the centre, (6) lenses, (7) ND filter, (8) beam splitter, (9) IC chip.

The photodetector circuit was tested at various supply voltage levels when illuminated with an 830 nm laser beam with a modulation depth of 20%. Some typical measured responses to modulated inputs for different illumination intensities are shown in Figures 6–7. Figure 6 shows the detector output at 10 kHz for an illumination intensity of 79.45 $\mu W/mm^2$. There are three signals in the figure. Trace (1) is the input signal modulated on the laser and trace (2) is the detector output. Trace (3) is the signal at node 3 in Figure 2, which is approximately 10 times smaller than the photodetecotor output. In this case, the peak-to-peak output amplitude is approximately 120 mV, which is consistent with the theoretical result. Figure 7 illustrates the detector output with the minimum illumination intensity 0.63 $\mu W/mm^2$. In this case, the moving pole is below 10 kHz, which reduces the amplitude of the output and attenuates the higher harmonics thus creating a sinusoidal output.

The results in Figure 8 demonstrate that the detector successfully works from supply voltages ranging from 0.45 V to 0.8 V. The small difference in the mid-band output is caused by the inaccuracy of the optical power density and modulation depth measurement. When the illumination is 79.45 $\mu W/mm^2$, pole 1, which depends on the photocurrent, is above 50 kHz. Under this condition, the detector has the largest bandwidth. The pole 2 which depends on the bias current is at approximately 50 kHz. When the illumination intensity decreases, pole 1 moves closer to the pole 2 which causes overshoot and the ringing effect. When the illumination is 0.63 $\mu W/mm^2$, the pole 1 moves just below 10 kHz and far away from pole 2. There is no longer any overshoot and ringing in the detector output. The detector is also tested with 0.3 V voltage supply. The results indicate that the circuit fails at this supply voltage.

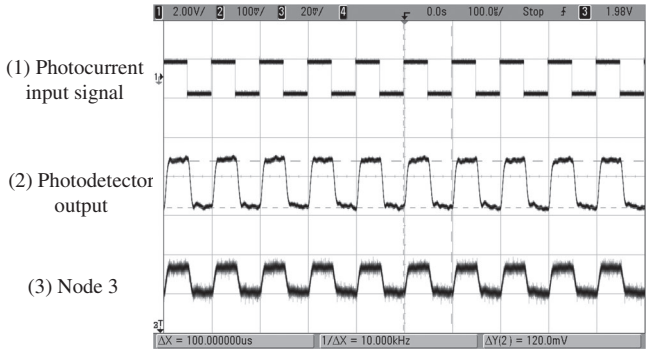

Figure 6. Measured photodetector output with 79.45 $\mu W/mm^2$ illumination intensity. The voltage scales for the three signals from top to bottom are 2 V/grid, 100 mV/grid and 20 mV/grid, respectively.

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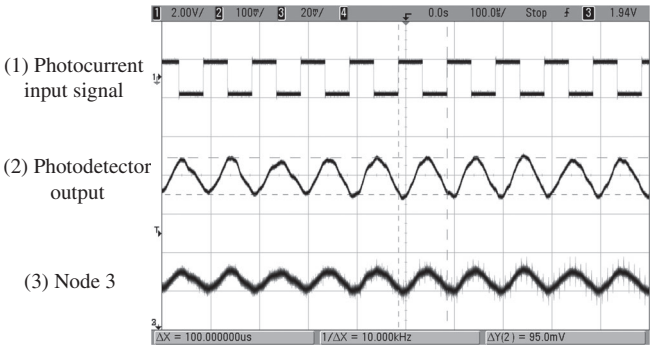

Figure 7. Measured photodetector output with 0.63 μW/mm^2 illumination intensity. The voltage scales for the three signals from top to bottom are 2 V/grid, 100 mV/grid and 20 mV/grid, respectively.

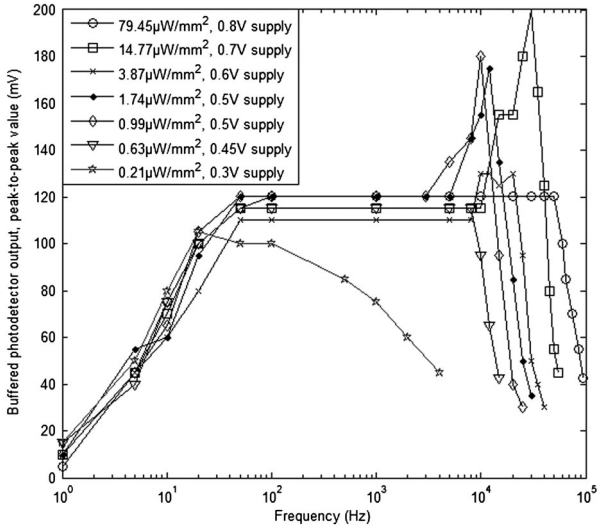

Figure 8. Measured 180 nm photodetector circuit output.

The optical downlink from the BS must be modulated by a data stream. If the data is represented by a conventional binary code, it may include a long stream of '1' s or '0' s, which would create a low frequency component to the modulation that would be difficult to be detected. The solution to this problem that has been adopted is to encode the data using a Manchester code which encodes data using transitions at a particular time. Since the transitions of Manchester codes occur at a specific time, the system needs a clock signal to ensure that the data is sampled at the correct time. An approach to create a clock on the SD is to send a clock signal from the BS on the same optical beam as that for the data. In order to easily separate the clock from the data using a first-order filter, their frequencies need to be approximately one decade apart. After filtering, the transmitted clock must be used to generate a clock at the frequency of the data. This process can be achieved easily using a divide-by-8 circuit, if the transmitted clock frequency is 8 times of the data frequency. The bandwidth of the photodetector must cover the frequencies of both the data and the transmitted clock. Since the cut-off frequency of the photodetector is approximately 10 kHz, the frequencies used for the data and transmitted clock were chosen to be 1 kHz and 8 kHz.

The illumination is modulated by a signal, which is a clock with its amplitude modulated by the Manchester encoded data, as shown in Figure 9. The modulated illumination intensity is the sum of three components, a dc component with the intensity of x, a Manchester encoded data with the intensity of y (peak to peak) and a clock with the intensity of z (peak-to-peak). The x, y and z are optical power illumination intensities and their unit is μW/mm^2.

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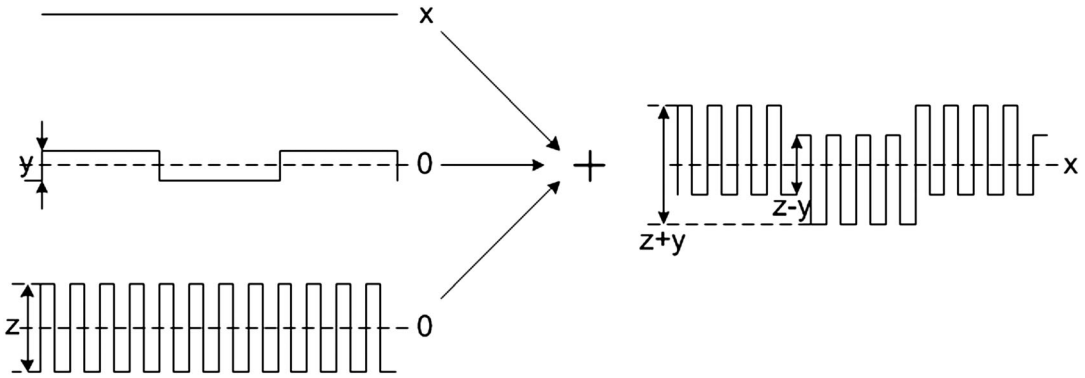

Figure 9. Illustration of modulation on the illumination intensity.

Two parameters, α and β, are used to characterize the modulation depths. α is the ratio of the peak to peak amplitudes of the clock and data. β is the ratio of modulated signal amplitude to the dc component, as shown in Eq. (3),

$$\alpha = \frac{z}{y}, \qquad and \quad \beta = \frac{y+z}{2x} \tag{3}$$

The photodetector was tested with a laser modulated to represent data at 1 kbps and a clock at 8 kHz, when α is 3 and β is 40%. These two parameter values ensure the data and clock can be recovered successfully by the circuits described in Section 4. Figure 10 shows a typical measurement result for 14.77 μW/mm^2 illumination intensity. Trace (1) is the photocurrent input signal and trace (2) is the photodetector output. As expected under these conditions, ringing occurs on the output. However, this will be filtered by the circuits that will be used to separate the data and the transmitted clock. The important result from this data is the peak-to-peak detector output amplitude. This is controlled by the modulation parameter β. When the modulation depth is 20%, the detector output is 120 mV and as expected when the modulation depth was doubled, the output also approximately doubled. This trend was reproduced at other illumination intensities. The only change that was observed was that as expected from the results in Figures 5–7, the detector output is a square wave for large illumination intensities and sinusoidal for small illumination intensities.

4. ANALOG CIRCUITS OF SD SYSTEM

The chosen modulation scheme means that each SD requires filters to separate the data and the transmitted clock. The clock can be recovered from the photodetector output using an integrator, a

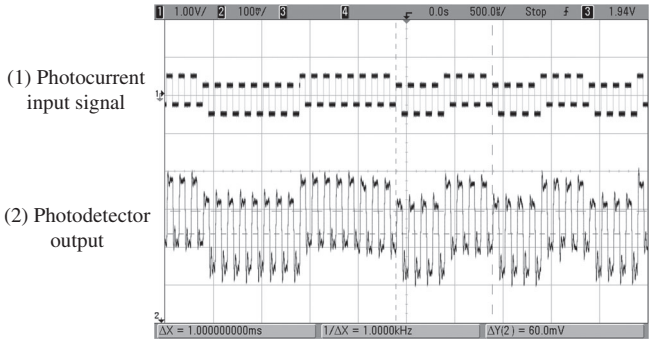

Figure 10. Modified detector output with the novel modulation scheme for 14.77 μW/mm^2 and 0.7 V voltage supply. The voltage scales for the two signals from top to bottom are 1 V/grid and 100 mV/grid, respectively.

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comparator and two inverters connected in series, as shown in Figure 11. Integrator1 is used to obtain the dc average of the detector output. This dc average is then compared to the detector output by the comparator and then the clock information is extracted. Two inverters are used to convert the comparator output to a digital signal and increase the driving ability at the same time. A buffer is necessary to drive the output pads and equipment for measurement purposes.

The schematic circuit diagram of Integrator1 is shown in Figure 12. The circuit is designed assuming that the bias voltage V_{int} is 90 mV above V_{ss}. To reduce the current consumption, the tail current is set to approximately 100 pA. This current is obtained by applying the bias voltage to a 3 μm wide and 1 μm long T-well NMOS transistor. The sizes of M_2 – M_5 were determined by the system requirement to ensure that all these devices operate in the subthreshold regime, the need to limit the load capacitance on the photodetector and the need to limit the dc offset of the integrator to less than 5 mV.

The capacitor C_1 in Figure 12 determines the corner frequency of the integrator and hence the ripple on the dc output level. The ripple amplitude is

$$v_{ripple} = \frac{I_{out} t_{\max}}{2C_1} = \frac{I_b \kappa_n (V_{in} - V_{out}) t_{\max}}{4 V_T C_1} \tag{4}$$

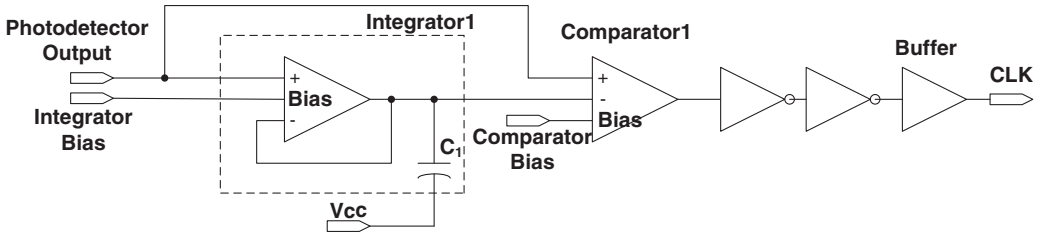

Figure 11. Clock recovery circuits.

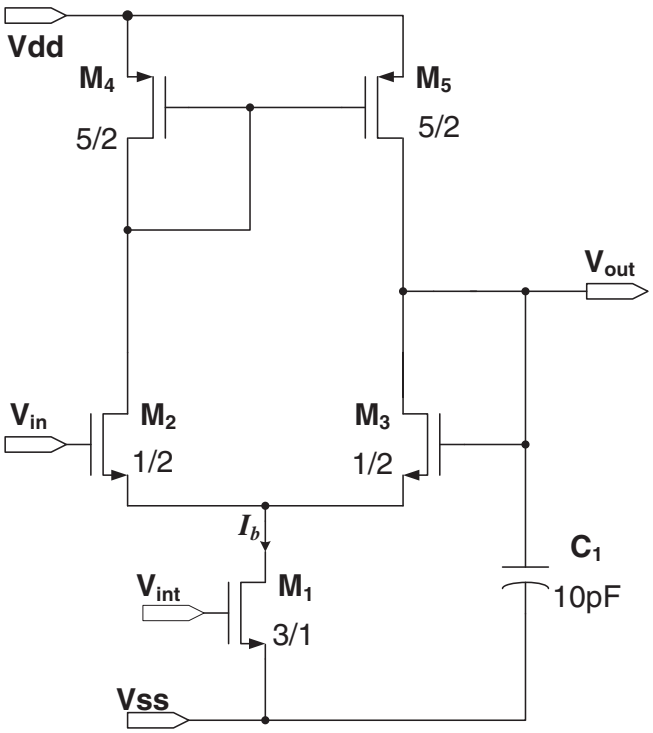

Figure 12. Circuit diagram of Integrator1.

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where t_{max} is the maximum charging/discharging time for C_1 and is 62.5 μs. The integrator output will be compared to its input for clock recovery. It is therefore better to consider the amplitude ratio η of the ripple to the input signal. The value of C_1 can be determined by setting η to 0.5%

$$C_1 = \frac{I_b \kappa_n t_{\max}}{4 V_T \eta} \approx 10\,pF \tag{5}$$

where $I_b = 115$ pA and $\kappa_n = 0.88$.

The schematic circuit diagram of Comparator1 in Figure 11 is shown in Figure 13. One of the inputs of this circuit is directly connected to the photodetector output, which is sensitive to the load capacitance. This means that the input pair of Comparator1 should be relatively small and these devices are therefore 1 μm wide and 2 μm long. In order to achieve a small dc offset and simplify the design, M_4 and M_5 are chosen to the same size as the equivalent devices in Integrator1. If the input differential voltage is large enough, most of tail current charges or discharges the output load. The tail current must be able to charge or discharge the comparators load capacitance in a small fraction of the clock period. To achieve this, a tail current of 4.5 nA is required.

The 90 mV bias voltage used in the integrator could also be used to bias this comparator. However, a large transistor would be required to obtain the required current. The comparator has therefore been biased; the voltage at the node 1 in Figure 2 is

$$V_1 = \frac{V_T}{\kappa_n} \ln\left(\frac{I_{bias} L_2}{I_{0n} W_2}\right) \tag{6}$$

V_1 is independent to the voltage supply and photocurrent. I_{bias} is fixed and then V_1 is also fixed and can be used to bias the comparator. The value of V_1 is approximately 210 mV obtained from simulations.

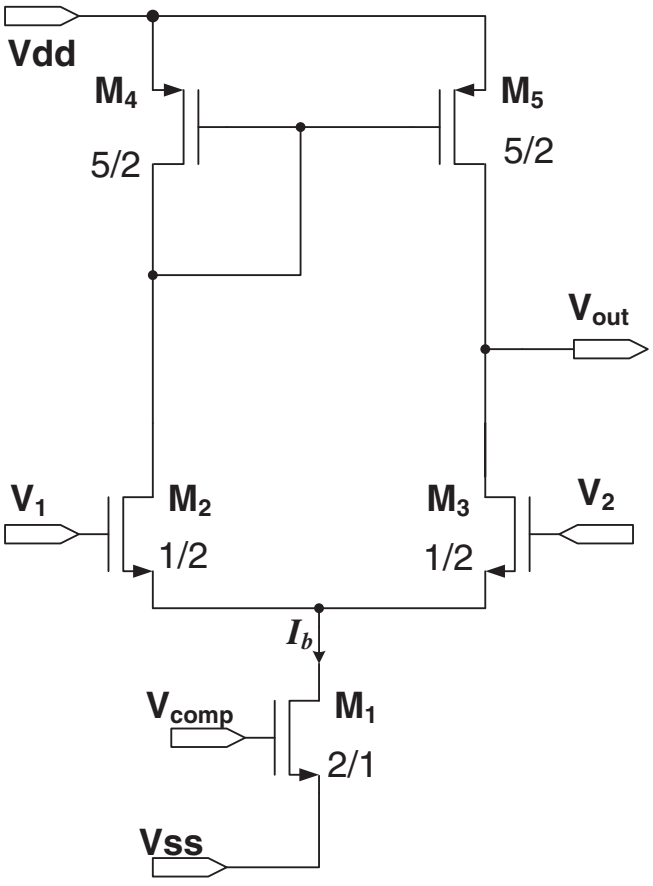

Figure 13. Circuit diagram of Comparator1.

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There is a small voltage ripple at the node 1 and it is caused by the photocurrent. But this ripple amplitude is as small as a few millivolts and does not affect the comparator performance. With this bias voltage, the size of M_1 in the comparator is 2 μm/1 μm and the actual designed tail current is 4.9 nA.

A schematic circuit diagram for the data recovery circuits is shown in Figure 14. In this scheme, Integrator2 and Integrator3 are used to remove the 8 kHz clock signal while retaining the 1 kbps Manchester data. This can be realized by putting the dominant poles of the two integrators at approximate 1 kHz. The dc average of Integrator3 output is obtained by Integrator4 and then compared with the Integrator3 output. The Manchester data is extracted by Comparator2. After that, two inverters are used to generate a digital output. A buffer is necessary to drive the output pads and test equipment.

Integrator2 is similar to Integrator1 and also directly connected to the photodetector output. To simplify the design, the same sizes of transistors as Integrator1 are used. However, the capacitance of C_2 must be carefully chosen. To avoid attenuation, the pole has been placed slightly above 1 kHz by using a 200 fF capacitance as C_2. Simulation results showed that Integrator2 does not remove the 8 kHz signal completely. Integrator3 is therefore needed to filter out these remaining 8 kHz ripples. The circuit for this integrator is the same as the other integrators. However, the input of Integrator3 is not connected to a capacitance sensitive node and so its input devices can be made larger (1 μm by 4 μm) to limit the offset voltage of this integrator. In order to reduce the loss of gain in Integrator3, the dominant pole of Integrator3 is set to 3 kHz by using a 100 fF capacitor as C_3. Integrator4 is needed to obtain the average output from Integrator3 so that a comparator can be used to obtain the 1 kbps Manchester data. Similar to Integrator3, Integrator4 is not connected to the node which is sensitive to the load capacitance. Therefore the same sizes of transistors are used as used in Integrator3. The load capacitance, C_4, needed to extract the data is approximately 5 pF.

The inputs of Comparator2 are connected to nodes which are insensitive to capacitive loads. Hence, the input transistors M_2 and M_3 were made 1 μm wide and 4 μm long. M_4 and M_5 are kept the same as in Comparator1. The tail current of Comparator2 can be smaller than that of Comparator1. In order to save power, the tail current is therefore reduced to approximately 2.5 nA, generated using a 1 μm wide and 2 μm long transistor.

5. MEASUREMENT RESULTS OF OPTICAL RECEIVER FRONT END

A complete optical receiver front end including a photodetector, clock and Manchester data recovery circuits has been fabricated as part of a 5×5 mm^2 chip, such as the one shown in Figure 15. The power photodiodes and other SD circuits have an area of 1×1.7 mm^2 and are marked by a rectangle. All the circuits are covered by a layer of top metal, which can shield the circuits from the illumination.

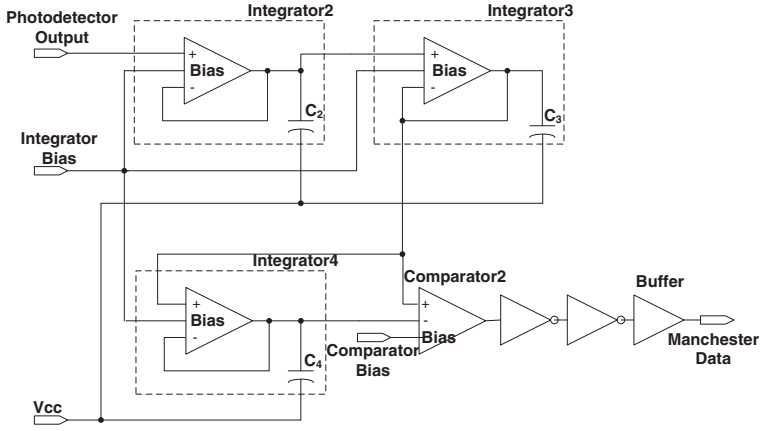

Figure 14. Manchester data recovery circuit.

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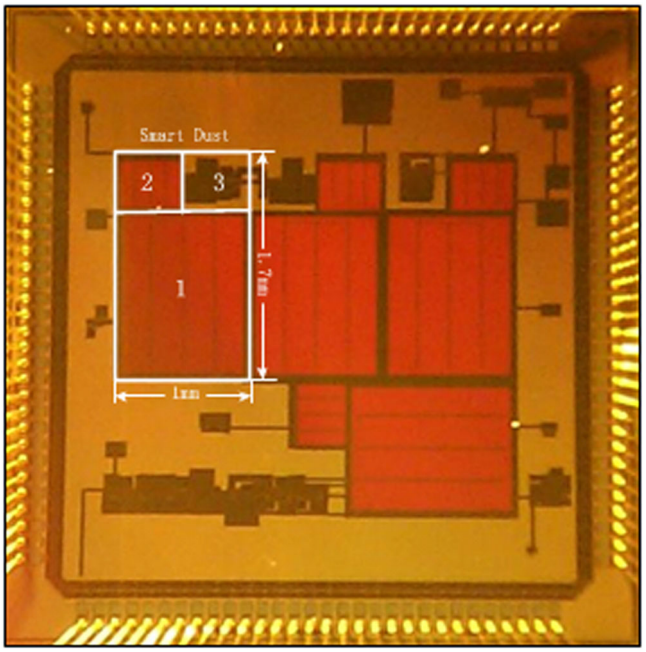
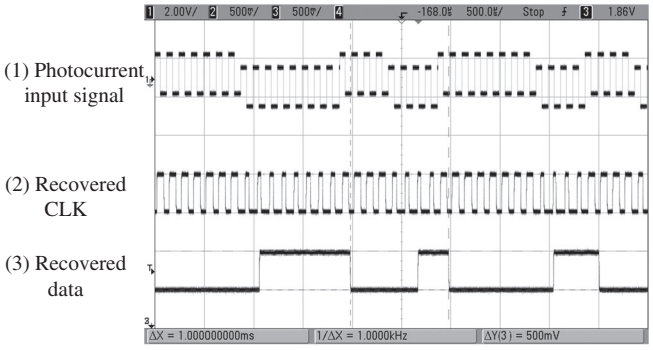
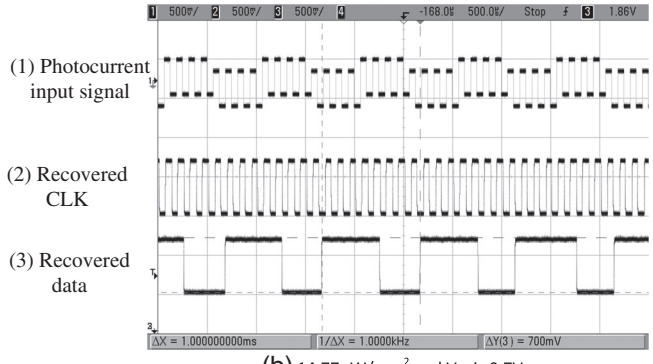


Figure 15. Picture of the fabricated chip. Part 1 is T-well/N-well diode, part 2 is N-well/P-sub diode and part 3 is the smart dust circuit system.



(a) 0.99μW/mm2 and Vdd is 0.5V,



(b) 14.77μW/mm^2 and V_{dd} is 0.7V

Figure 16. Measurement results with conditions of 1 kbps Manchester data rate, $\alpha = 3$ and $\beta = 40\%$. (a) The voltage scales for the three signals from top to bottom are 2 V/grid, 500 mV/grid and 500 mV/grid, respectively. (b) The voltage scales for the three signals are 500 mV/grid.

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The whole system has two outputs, the recovered clock and Manchester data. For testing, the system has three bias voltage connections, the photodetector bias, integrator bias and comparator bias. The bias voltage for the photodetector and integrator used in the measurement is 110 mV and the comparator bias is 210 mV as designed. A typical measurement result in Figure 16 (a) shows that the clock and Manchester data are successfully recovered for 0.5 V supply and 0.99 $\mu W/mm^2$. The voltage supply and its corresponding illumination intensity are obtained from power diode measurement results shown in Table I. Trace (1) in Figure 16 (a) shows the modulation on the laser beam. Trace (2) and trace (3) are the successfully recovered 8 kHz clock and 1 kbps Manchester data, which is inverted, compared to the original data. The clock does not have a 50% duty cycle and the Manchester data does not switch in the middle of the bit. These characteristics were expected from the simulation results; however, they will not affect the whole system because the following digital block can be designed to use edge-triggered sampling. As a result, the sensitivity of the front end is approximately 1 $\mu W/mm^2$ for 8 kHz clock and 1 kbps Manchester data transmission. Figure 16 (b) shows measured results when the illumination intensity is 14.77 $\mu W/mm^2$. In this case, the detector output has overshoot and ringing phenomena as shown in Figure 10. However, the system still successfully recovers both the clock and the Manchester encoded data.

The complete data and clock recovery system has been tested under all the conditions described in Table I. When the illumination intensity is 79.45 $\mu W/mm^2$, the total current consumption is approximately 135 nA. The total current consumption drops to 18.8 nA when the illumination intensity is 0.99 $\mu W/mm^2$. In this case, the total available photocurrent is 46 nA and there is therefore enough power available from the power diodes. The system is therefore tested powered from the photodiodes on the same substrate. To do this, the V_{dd} of the system is connected to the T-well terminal of the T-well/N-well and the V_{ss} of the system is connected to the N-well terminal of the N-well/P-sub. The bias voltages were obtained from external voltage sources with the ground terminals of equipment connected to the V_{ss} of the system. In summary, the front end successfully works powered by the photodiodes and similar measurement results can be obtained. The self-powered SD system can work at least in a 10 m distance to the BS.

6. CONCLUSION

In this paper, the design and measurement results of an optically powered, optical receiver are provided. T-well/N-well and N-well/P-sub are selected for the power photodiodes. The areas of these devices were chosen to compensate for the different quantum efficiencies at wavelengths around 830 nm. With the illumination intensities expected to be available from the BS, the power diodes can generate a voltage between 0.45 V and 0.8 V, and a current of between 30.8 nA and 3800 nA corresponding to 10 m and 1 m distance, respectively.

An adaptive logarithmic photodetector has been designed to act as the first stage of an optical receiver. In this circuit, all the NMOS transistors are T-well NMOS transistors so that the complete circuit is in an N-well. The detector successfully works for voltage supply range from 0.5 V to 0.8 V and the corresponding illumination intensities. The bandwidth of the detector varies as the illumination intensity varies because one dominant pole depends upon the photocurrent. The maximum bandwidth is above 50 kHz under the maximum illumination intensity. The minimum bandwidth is about 10 kHz as designed and this ensures the complete system works successfully.

A novel modulation scheme has been developed in order to transmit both Manchester encoded data and a clock from the BS to the SD. The circuits needed to recover the Manchester data and clock have been described and shown to work successfully. The sensitivity of the front end is approximately 1 $\mu W/mm^2$ for 8 kHz clock and 1 kbps Manchester data transmission. The complete system worked successfully when it is powered by the two power diodes integrated on the same substrate as the optical receiver front end circuits. The results presented therefore show that it is possible to design an optically powered, optical receiver for an SD operating at data rates of 1 kbps. In the future, other functions can be added to the smart dust.

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