An 8-Channel Wearable EEG Acquisition Front-End IC with Integrated Multi-Functions

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***Abstract*—This paper presents a single chip integrated 8-channel biomedical signal readout front-end circuit for wearable EEG acquisition system following a low power and high dynamic range (DR) strategy. The proposed 8-channel hybrid sigma-delta analog-to-digital convertor (HSD-ADC) contains a programmable-gain input interface in the first stage to allow the users to optimize their system with different ranges of input level. The time-interleaving technique is used on the second channel-shared stage for low power dissipation. The prototype chip is designed with 65 nm CMOS technology. Post-layout simulation results show a SNDR of 83.7 dB and 98.5 dB dynamic range with 85 μW power dissipation per channel at 1.2 V operation.**

Keywords—EEG, biomedical, integrated circuit, front-end interface, analog-to-digital converter

I. INTRODUCTION

Modern wearable technology was developing rapidly thanks to the recent advances in integrate circuits (ICs), biomedical engineering technologies, sensors, power management technologies, wireless communication for the personal healthcare and telehealth application. Low-power biomedical ICs are widely applied in wearable wellness and health monitor to continuously sense biomedical signal and transfer health information in people's daily life. Electroencephalography (EEG) is one of the most significant noninvasive and radiation-free way to monitor bioelectric signal of brain and provide the important reference for the diagnosis of brain diseases, like Alzheimer's disease, Parkinson's disease, epileptic seizures and so on [1]. Also, EEGs play an important part in brain-computer interface (BCI) and other cognitive research [2].

The analog front-end circuit plays a vital role in the wearable EEG acquisition system and dominates its overall performance. The conventional front-end circuit applied in EEG recording systems is based on multiple separated printed circuit boards (PCBs), which is very bulky and occupy a large space that is not suitable for wearable electronic device. Besides, the implementation with discrete PCB level lead to systemic delay which will affect the stability and accuracy for continuous EEG monitoring system. Therefore, a novel front-end circuit for EEG acquisition system with high integration, high resolution signal processing and gain programmability must be developed in order to extend the operational dynamic range and enhance the performances of wearable EEG acquisition system.

This paper presents a novel energy-efficient EEG signal acquisition front-end IC, which is typically the core of wearable EEG monitor. The proposed circuit is realized with 8-channel hybrid channel-shared SD-ADC. Gain programmability function is embedded inside the first stage to extent the performance of dynamic range. The inherent anti-aliasing filter of the hybrid SD-ADC can remove the conventional low pass filter. Time-interleaving technique is used for the channel-shared design. This proposed EEG acquisition front-end circuit achieves low power consumption and miniaturization of area, and also reduces the complexity.

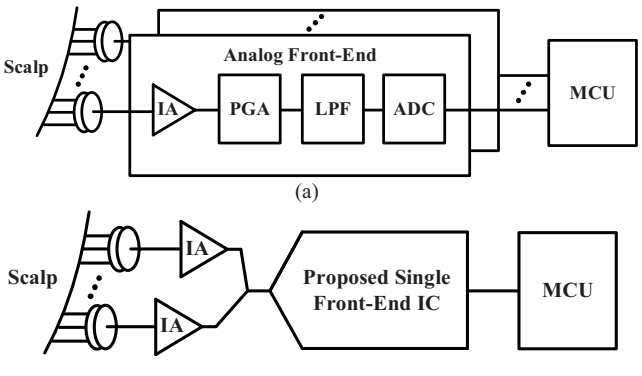

Fig. 1 (a) Conventional EEG signal acquisition chain block diagram (b) System-level of proposed EEG acquisition front-end IC

II. SYSTEM-LEVEL EEG ACQUISITION STRUCTURE

Fig. 1(a) shows the EEG signal acquisition chain block diagram which include the wet/dry electrode, instrumental amplifier, signal conditioning circuit with gain programmability and low pass filter (LPF) and analog-to-digital conversion, and microcontroller unit (MCU) as the digital processing part. Multi-channel wet/dry electrodes are interfaces between the scalp and front-end circuit to sense the biomedical signal of brain with μV level. Each electrode is connected to an instrumental amplifier (IA) to amplify the weak biopotential signal. The traditional front-end signal conditioning circuit is realized with many discrete components in PCB level, which are quite bulky [3][4]. In this work, a mixed-signal single front-end IC is proposed in Fig. 1(b) and designed with an 8-channel HSD-ADC as described below. Combining both advantages of analog and digital system, the proposed mixed-signal front-end circuit achieve several special features as follows. Firstly, adaptive signal conditioning with front-end input gain programmability is provided in the EEG acquisition system for higher flexibility and better dynamic range. Secondly, the integrated front-end circuit can be operated in parallel with 8-channel capability. Thirdly, low-power signal processing, higher resolution and faster response time can be achieved by a mixed-signal platform.

The system-level working principle of the proposed mixed-signal integrated EEG acquisition front-end circuit shown in Fig. 1(b) can be simply described as: the electrodes detect EEG signals from the scalp, then the instrumental amplifiers is necessary to amplify and process the output signals of electrodes on the order of microvolts, and then the

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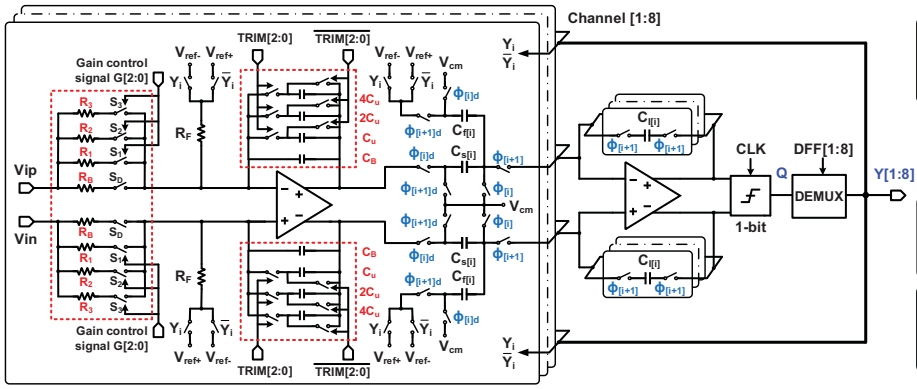

Fig. 2 The proposed integrated 8-channel HSD-ADC

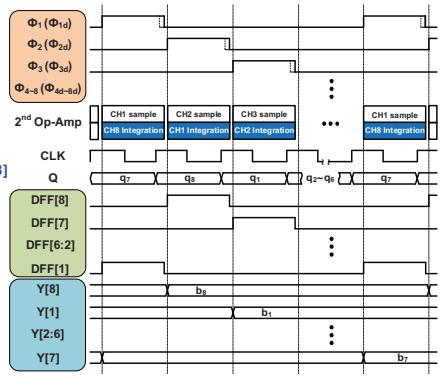

Fig. 3 Timing diagram of the proposed circuit

front-end mixed signal IC transform IA's output signal to digital code. In analog part of the mixed signal IC, the programmable gain amplifier (PGA) is applied to amplify a better matchup with the ADC range for enhancing the signal resolution and dynamic range. After analog-to-digital conversion, the digital signals are transmitted into MCU for digital processing. In digital processing part, the decimation block, adaptive gain control block, reference compensating block, resolution compensation block, and other EEG signal analysis algorithm blocks are implemented in MCU. Mixed signal front-end IC is under control of MCU and allows to be dynamically gain reconfigured through a 3-bit gain control bus G[2:0]. The mixed signal front-end provides an effective way to processing and convert EEG signal to digital code for further analysis algorithm.

III. Proposed Circuit Design

A. Proposed Integrated 8-Channel Hybrid ADC

Most of the brain signal observed in a scalp EEG falls in the range of 0.5–100 Hz, but in some cases which are caused by artifacts, the frequency is around 1000Hz under standard clinical recording conditions [5][6]. Overall EEG acquisition system model is built and simulated in MATLAB® simulink platform. As a result, a 16-bit ADC dynamic range with 1KHz bandwidth can satisfy the common international standards in EEG acquisition system. ADC requirements are specified and a suitable topology is selected to meet the design requirements. SD-ADC is one of the most energy-efficient ADCs when high resolution with low/medium signal bandwidth need to be achieved. So an integrated 8-channel HSD-ADC as the EEG acquisition front-end circuit is proposed as shown in Fig. 2, which consists of 8 channels of continuous-time (CT) integrators, a channel-shared discrete-time (DT) integrator, quantizer, demultiplexer and an 8-phase clock generator. Fully differential structure can improve the power supply rejection and noise performance and reduce the crosstalk effect as well. The first stage parallel 8 channels of CT integrators which contain two capacitor banks on the differential pair at each channel to trim RC time constant for process and temperature variations and two resister banks for the gain programmability function (from 1x to 8x). Plus, the first CT stage can provide the inherent anti-aliasing function as a low pass filter at the front-end [7]. A single-bit DAC with good linearity is used to feedback the quantized digital signal to the input of the 1st and 2nd integrator, which build an 8-channel HSD-ADC loop. In the second DT integrator, 8 sampling capacitors and 8 integration capacitors are processed for time interleaving. Fig.3 shows the timing diagram. An 8-phase clock generator provide eight 400 KHz clock phases with 12.5% duty cycle as a clock control signal for the channel-shared DT integrator. The proposed multi-channel HSD-ADC convert 8-channel signals to a serial 1-bit streams that include information about all channels and are transmitted into demultiplexer. The demultiplexed 8-channel outputs send to off-chip for digital signal processing and EEG analysis algorithm in MCU and feedback to the input of the ADC at the same time.

B. Design Consideration of Gain Programmability

The programmable gain amplifier function is realized by two switchable resistor banks which are controlled by a 3-bit digital code G[2:0] shown in Fig.2. The gain is switched from 1 to 8 times according to the amplitude of the input signal. The merged PGA–filter–HSDADC design provides the same functionality as the conventional cascade of PGA and filter stages.

It is possible that the gain of the active RC integrator is affected because of the ON-resistances of the switches, which cause a gain error for the whole EEG acquisition system. The transfer function of the active RC integrator is expressed in Equation 1.

$$H(s)=\left(\frac{G[2]}{R_3+R_{S3}}+\frac{G[1]}{R_2+R_{S2}}+\frac{G[0]}{R_1+R_{S1}}+\frac{1}{R_B+R_{SD}}\right)\cdot\frac{1}{C\cdot s} \quad (1)$$

The gain control signals G[2:0] equal to value '1' when the switches S_1 to S_3 are turned on. On the contrary, G[2:0] equal to value '0' when the switches are turned off. It can be seen from Equation 1 that, the resistors R_1 to R_3 need to have higher resistances than the ON-resistances of switches in order to minimize the gain error. Besides, when a resistance ratio of the base resistor R_B to the resistors R_1 to R_3 is set to be equal to the ratio of the dummy switch ON-resistance R_{SD} to the switches ON-resistance R_{S1} to R_{S3}, the gain variation is controlled irrespective of the ON-resistances of the switches. In this case, the resistance ratio is set as follows: $R_B = R_1 = R_2/2 = R_3/4$; $R_{SD} = R_{S1} = R_{S2}/2 = R_{S3}/4$, where the ON-resistances of the switches is determined by the size of transistor. The new transfer function can be expressed below.

$$H(s)=\frac{1}{(R_B+R_{SD})\cdot C\cdot s}\cdot\left(4\cdot G[2]+2\cdot G[1]+G[0]+1\right) \quad (2)$$

It can be seen from Equation 2 that, When the resistance ratios are controlled to be the same, the gain of the active RC

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integrator can be controlled from 1 to 8 times $1/(C_S \cdot (R_B+R_{SD}))$ in response to the 3-bit G[2:0].

Additionally, when the small input signal needs to be amplified by the PGA, the related switches turn on, which means decrease the resistance value of input path by parallel extra resistors. Thereby, the thermal noise generated by the resistor is reduced. The input signal and thermal noise that have already reduced are amplified together, which do not generate bad effect for signal to noise ratio (SNR).

C. Time-Interleaving Technique

Traditional designs of switched-capacitor integrator require op-amp outputs to change during one phase of a two-phase non-overlapping clock and hold constant during the other phase. The output of each Op-Amp is constant when its sampling capacitor samples the input and changes when the sampling capacitor charges to integrating capacitor. To overcome this limitation, for this case, 8 sampling capacitors can be used for time interleaving to each integrating capacitor. The timing diagram is shown in Fig. 3. For the channel-shared second stage of HSD-ADC, when one channel is sampling, simultaneously, another channel is integrating, thereby the quantizer can update the new code in each phase. The clock generator generates eight 400 KHz clock phases with 12.5% duty cycle to control the shared DT integrator of proposed HSD-ADC.

IV. Post-Simulation Results

The proposed 8-channel EEG acquisition front-end circuit embedded PGA, LPF and ADC function is designed in CMOS 65nm process. The layout is shown in Fig. 4. The active chip area is 0.026 mm^2 per channel. After the post-layout simulation, the output streams from each channel and the clock signal are analyzed through MATLAB®. This proposed circuit achieves 83.7 dB peak SNDR shown in Fig.6 and 98.5 dB (16-bit) DR which is boosted by the programmable gain function (Fig.5). The crosstalk was simulated by putting a full-scale sinusoidal input at 220 Hz to one channel, a 480 Hz input to another channels, and then observing the 480 Hz component at the output of the former channel and the 220 Hz component at the output of the later channel at the same time. The crosstalk was simulated to be around -101 dB (Fig.7). This front-end circuit only consumes 85 µW power per channel with 1.2 V power supply.

V. Conclusions

This paper presented an integrated multi-channel EEG acquisition front-end circuit with embedded PGA, LPF and ADC function. This IC design opens the door for the miniaturization and low power dissipation of the wearable EEG monitor with signal processing delay reduction and performance improvement.

Acknowledgment

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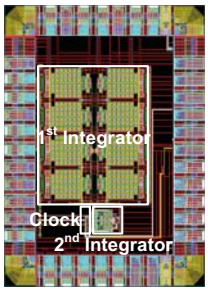

Fig. 4 Chip layout

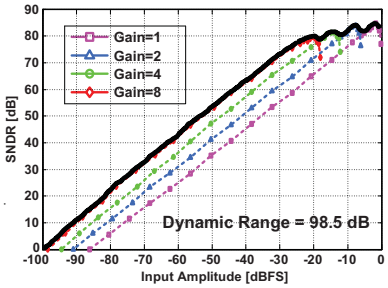

Fig. 5 SNDR vs. input with PGA settings

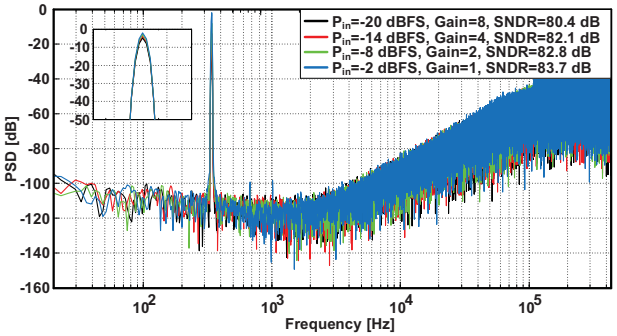

Fig. 6 Simulated results in different input level with PGA (1x to 8x)

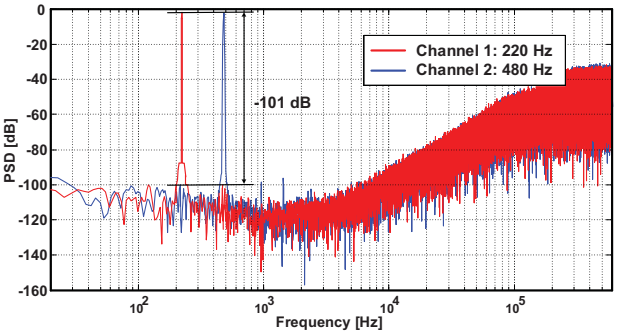

Fig. 7 The crosstalk simulation result

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