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A 1.65-nW 11.14-ppm/°C self-biased subthreshold CMOS voltage reference with temperature compensation circuit

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Summary

This paper presents a subthreshold CMOS voltage reference (VR) that utilizes self-biased circuits. This voltage reference includes temperature compensation circuits to expand its operating temperature range and reduce its temperature coefficient. The proposed CMOS voltage reference is designed using a standard 0.18-μm CMOS process and has a small area of only 0.005 mm^2. Post-layout simulation results demonstrate that the power consumption of the circuit at room temperature (25°C) is only 1.65 nW at a power supply voltage of 1 V. In this case, the voltage reference output is 316.56 mV, with an average temperature coefficient (TC) of 11.14 ppm/°C in a wide temperature range from −40°C to 140°C. Furthermore, the line sensitivity (LS) of the circuit is 0.024%/V, and the power supply rejection ratio (PSRR) of the circuit is −86.5 dB at 10 Hz. In summary, the subthreshold CMOS voltage reference structure proposed in this paper demonstrates excellent performance characteristics, such as low power consumption, a small area, and high-temperature stability. These features make it a promising candidate for voltage reference for low-power applications with significant changes in environmental temperature.

KEYWORDS

CMOS voltage reference, line sensitivity, low area, low power, low supply voltage, power supply rejection ratio, self-biased, subthreshold, temperature coefficient

1 | INTRODUCTION

There has been an increasing need for low-power solutions to sustain the operation of ultra-low-power Internet of Things (IoT) nodes, such as unattended sensors and smart household appliances, that need to run for a long time with low-capacity batteries or energy-harvesting platforms.[1] The rapid development of IoT systems has resulted in the widespread use of low-supply voltage and low-power sensors. However, for self-powered IoT sensor applications, the power supply harvested from ambient energy is often unstable, leading to the need for VR designs with low power consumption, small areas, fast activation, and trimming free.

To ensure a stable voltage that is independent of process, supply voltage, and temperature (PVT) variations, a well-designed VR circuit is essential. Many VR circuit designs have been proposed to address the challenges of low power consumption and low-temperature variation. One design utilized a two-transistor VR circuit to achieve ultra-low power consumption and low supply voltage.[2] However, the circuit suffered from significant leakage current and large performance variations between chips even after using a trimming circuit. Then, stable low-power reference circuits

with better performance of power supply rejection ratio (PSRR) and line sensitivity (LS) can be built by an operational amplifier (OPA) operating in the subthreshold region.[3-7] However, due to the introduction of OPA, the circuit structure becomes more complex. In low-power and low-voltage applications, these VRs have no advantage in power consumption and chip area. The sub-bandgap voltage reference (sub-BGR) that combined with the bipolar junction transistors (BJT) and MOS transistors working in the subthreshold region has emerged as a promising alternative to due to its low power consumption.[8-13] Although it offers good temperature performance and power supply rejection ratio (PSRR), the minimum supply voltage is limited by the base–emitter voltage of the BJT, and in terms of power consumption, sub-BGRs are basically higher than pure subthreshold CMOS VR circuits. The latter has been shown to have simplified bias circuits.[14-17] These self-biased circuits greatly reduce the complexity of the VR circuits. This can greatly reduce the overall power consumption and circuit area. Among subthreshold CMOS VR circuit designs, the stacked diode-connected MOS transistors (SDMTs) are effective in achieving PVT immunity for reference voltage through two NMOS transistors with different threshold voltages, making it suitable for low voltage and low power applications.[17-21] However, further improvement is required in terms of temperature coefficients. Aminzadeh develops a nano-power voltage reference using curvature compensation without amplifiers.22 The proposed circuit uses NMOS transistors with different threshold voltages and has an average TC as low as 9.79 ppm/°C. Ebrahimi presents a new PVT-compensated BGR by using the switched-capacitor (S.C.) technique. Simulation results show that the average temperature coefficient of the S.C. BGR is 17 ppm/°C with a power consumption of 28 μW.[23] But in low-supply voltage and low-power sensor applications, ultra-low power consumption, small minimum power supply voltage, and silicon area are required. To solve the mentioned problems, a modified SDMT voltage reference circuit without an operational amplifier is proposed, which features a self-biased circuit design that reduces the circuit's complexity. The paper is structured as follows: Section 2 discusses the SDMT and the modified SDMT with temperature compensation. Section 3 provides the design details of the proposed CMOS VR and Section 4 presents the post-layout simulation results. Finally, Section 5 concludes the paper.

2 | SDMT WITH TEMPERATURE COMPENSATION

The use of MOS transistors operating in the subthreshold region enables the generation of complementary-to-absolute-temperature (CTAT) voltage and adjustable proportional-to-absolute-temperature (PTAT) voltage. By using an SDMT structure, the first-order temperature coefficient of the output voltage can be eliminated. This SDMT circuit offers lower power consumption and a lower supply voltage compared to the traditional BGR.

Figure 1 shows the comparison of the traditional SDMT VR and the proposed SDMT VR with temperature compensation. M_1, M_3, and M_6 are thin-oxide NOMS transistors, and the rest transistors are thick-oxide NMOS transistors, which have a higher threshold voltage. All MOS transistors operating in the subthreshold region are biased by ideal current sources I, I_1, and I_2. The drain current (I_D) of these transistors can be expressed as Equation (1).

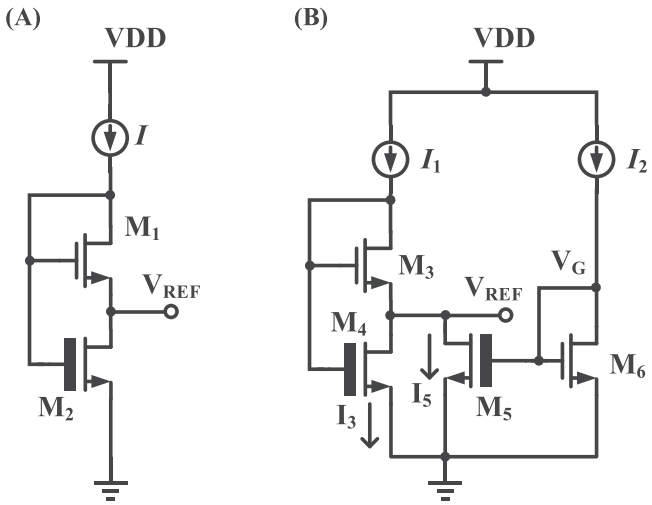

FIGURE 1 Conceptual diagrams of (A) SDMT architecture[17] and (B) modified SDMT with temperature compensation circuit.

$$I_D = \mu_n C_{OX}(m-1)KV_T^2 \exp\left(\frac{V_{GS}-V_{TH}}{mV_T}\right)\left(1-\exp\left(\frac{-V_{DS}}{V_T}\right)\right) \quad (1)$$

where μ_n is the mobility of electrons, C_{OX} is the gate oxide capacitance per unit area, V_{TH} is the threshold voltage of the transistor, K is the aspect ratio ($=W/L$) of the transistor, $V_T = k_B T/q$ is the thermal voltage, k_B is the Boltzmann constant, and T is absolute temperature, q is the elementary charge, and $m = 1 + C_{OX}/C_d$ is the subthreshold slope factor, where C_d is the depletion capacitance per unit area.[12] The body effect can change the threshold voltage of MOSFET V_{TH}.

$$V_{TH} = V_{TH0} + \gamma\left[\sqrt{|2\phi_F + V_{SB}|} - \sqrt{2\phi_F}\right] \quad (2)$$

where V_{TH0} is the threshold voltage of MOSFET when the source-bulk potential difference $V_{SB} = 0$, $\phi_F = (kT/q)\ln(N_{sub}/n_i)$, N_{sub} is the doping density of the substrate, n_i is the density of electrons in undoped silicon, and γ is the body-effect coefficient of the MOSFET. In Equation (2), both V_{TH0} and ϕ_F have temperature dependence. However, when making a difference in the threshold voltage of the same type of transistor in the temperature performance analysis, the influence of the body effect on different transistors can be ignored.[24] In a simple analysis, it can be approximated that the C_{OX} and V_{TH} of the same type of NMOS transistors are equal. Neglecting body effects and assuming that different types of NMOS transistors have the same subthreshold slope factor m (in the CMOS process used, m is 1.03 and 1.13 for thick-oxide NMOS transistors and thin-oxide NOMS transistors, respectively). When $V_{DS} \geq 3V_T$, the drain current of the transistor in the subthreshold region can be approximated as:

$$I_D = \mu_n C_{OX}(m-1)KV_T^2 \exp\left(\frac{V_{GS}-V_{TH}}{mV_T}\right) \quad (3)$$

For the traditional SDMT circuit, the same drain current flows through M_1 and M_2. The output voltage is the difference between the gate-source voltage of the two transistors with different gate oxide thicknesses. Therefore, when the subthreshold slope factors m of M_1 and M_2 are the same, the V_{REF} can be represented as (4).

$$V_{REF} = (V_{TH2} - V_{TH1}) + mV_T \ln\left(\frac{\mu_1 C_{OX1} K_1}{\mu_2 C_{OX2} K_2}\right) \quad (4)$$

It can be seen that the output voltage of the SDMT is insensitive to the bias current. Due to the use of NMOS transistors with different gate oxide thicknesses, there is a threshold voltage difference ΔV_{TH} between them, and the difference in threshold voltage generates a CTAT voltage[17]:

$$\Delta V_{TH} = \Delta V_{TH0} + (\alpha_2 - \alpha_1)(T - T_0) \quad (5)$$

where α is the first-order derivative of the threshold voltage with respect to the temperature, ΔV_{TH0} is the threshold voltage difference at normal temperature T_0 (300 K). V_{TH} has a negative temperature coefficient and the term $(\alpha_2 - \alpha_1)$ is negative due to the thick gate MOS M_2. The second term in Equation (5) is a PTAT voltage. However, it is only first-order coefficient compensation. As the temperature gradually increases, the voltage output of the traditional SDMT is dominated by high-order positive temperature coefficients, which cause the TC of the SDMT to increase. To solve this problem, a current with positive TC at a high-temperature range is required and used to sink the SDMT output node. So small TC could be achieved at a high temperature range. Therefore, this paper proposes an improved SDMT circuit to compensate for the temperature coefficient of VR, as shown in Figure 1B. The threshold voltages of $M_3 \sim M_6$, and the threshold voltage difference between M_4 and M_3, M_6 and M_5 are shown in Figure 2. Except for V_{TH6} - V_{TH5}, all others are complementary to temperature. The gate voltage V_G of M_5 in Figure 1 can be expressed as:

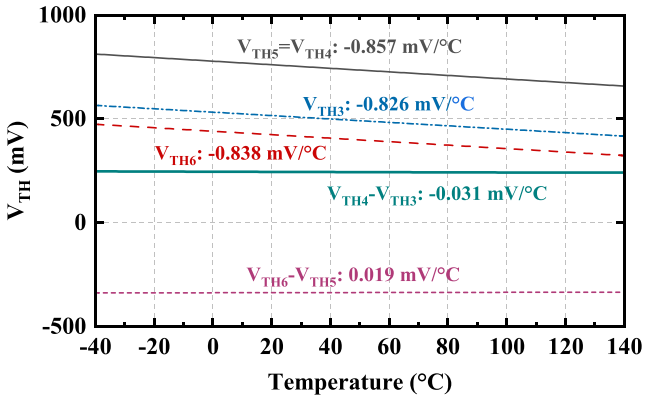

FIGURE 2 Simulation results of V_{TH} of M3 ~ M6, and the difference threshold V_{TH4} - V_{TH3}, V_{TH6} - V_{TH5}.

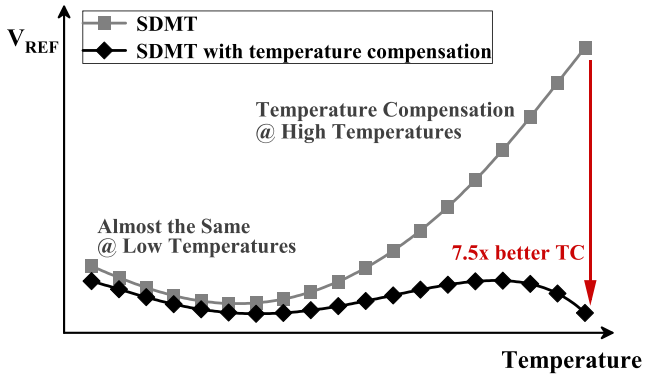

FIGURE 3 Conceptual diagrams of SDMT architecture[17] and modified SDMT with temperature compensation circuit over temperature.

$$V_G = mV_T \ln \frac{I_2}{\mu_6 C_{OX6}(m-1)K_6 {V_T}^2} + V_{TH6} \tag{6}$$

According to (3) and (7), the drain current of the M_5 can be written as:

$$I_5 = I_2 \times \frac{\mu_5 C_{OX5} K_5}{\mu_6 C_{OX6} K_6} \exp\left(\frac{V_{TH6} - V_{TH5}}{mV_T}\right) \tag{7}$$

Because V_{TH6} is smaller than V_{TH5} and V_T is proportional to temperature, the M_5 drain current I_5 is almost zero at low temperatures based on the characteristics of exponential functions. As the temperature increases, I_5 can be no longer ignored. Therefore, the temperature performance of the circuit at high temperature is compensated. The output voltage of the SDMT with temperature compensation can be expressed as:

$$V_{REF} = (V_{TH4} - V_{TH3}) + mV_T \ln\left(\frac{I_3}{I_3 + I_5} \times \frac{\mu_3 C_{OX3} K_3}{\mu_4 C_{OX4} K_4}\right) \tag{8}$$

The modified SDMT output voltage is insensitive to the bias current at low temperatures, similar to the traditional SDMT in this case. The proposed SDMT with temperature compensation shows a decrease in the PTAT voltage (second term in Equation 8) coefficient as the temperature increases due to the increase of I_5, leading to temperature compensation at high temperatures. The conceptual diagrams of the SDMT circuit and modified SDMT circuit with a temperature compensation structure are shown in Figure 3. It can be seen that the proposed SDMT circuit with a temperature compensation structure can enhance the temperature coefficient (TC) performance and operating temperature range of the circuit compared with the traditional SDMT architecture.

3 | DESIGN OF THE PROPOSED CMOS VR CIRCUIT

3.1 | Temperature coefficient

Figure 4 shows the schematic of the proposed CMOS VR circuit, which is composed of an improved SDMT with temperature compensation, a self-biased circuit, and a start-up circuit. All MOS transistors operate in the subthreshold region except M_{S1}, M_{S2} and M_{S3}. M_{N2} and M_{N3} are thick-oxide NMOS transistors that have higher threshold voltage. The branch currents I_{P1} and I_{P3} are mirrored from the bias current I_{bias} through cascode current mirrors. The final output reference voltage can be expressed as:

$$V_{REF} = (V_{THN2} - V_{THN1}) + mV_T \ln\left(\frac{I_{N2}}{I_{P1}} \times \frac{\mu_{N1} C_{OXN1} K_{N1}}{\mu_{N2} C_{OXN2} K_{N2}}\right) \tag{9}$$

$$I_{N2} + I_{N3} = I_{P1} \tag{10}$$

$$I_{N3} = I_{P3} \times \frac{\mu_{N3} C_{OXN3} K_{N3}}{\mu_{N4} C_{OXN4} K_{N4}} \exp\left(\frac{V_{THN4} - V_{THN3}}{mV_T}\right) \tag{11}$$

Based on Equations (9) to (11), by carefully adjusting the transistors' size of $M_{N1} \sim M_{N4}$ and the current ratio of I_{P1}, I_{P3}, and I_{bias}, it is possible to create CTAT voltage and PTAT voltage. Its temperature performance is also well compensated at high temperatures so that the proposed CMOS VR can extend the operational temperature range and have good TC performance. The design parameters are summarized in Table 1.

3.2 | Process variation

From (9), the temperature-independent V_{REF} is not only affected by the bias current but also affected by the threshold voltage V_{TH} of the MOS transistors. In low-power applications, the impact of process deviation is often greater due to

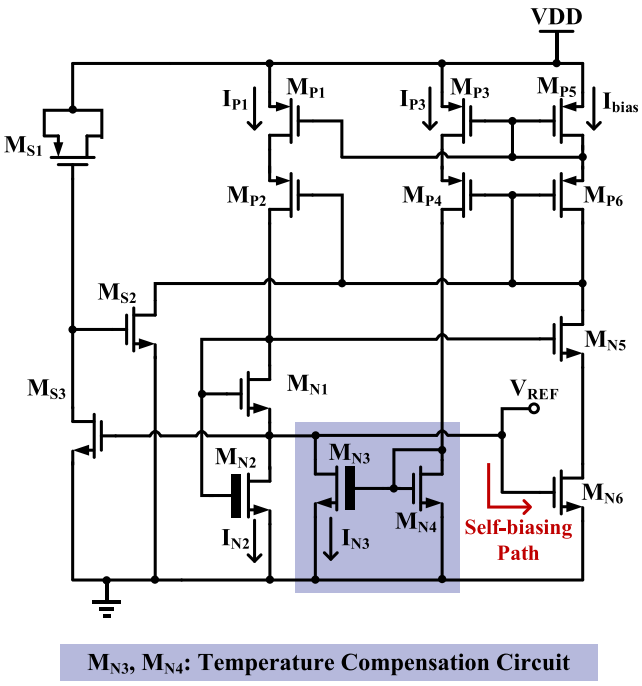

FIGURE 4 Schematic of the proposed CMOS VR circuit.

TABLE 1 Component parameters in the proposed VR circuit.

Components	W/L (μm/μm)	Components	W/L (μm/μm)
M_{S1}	4*5/5	M_{P6}	2*4/3
M_{S2}	4/20	M_{N1}	4*12.8/10
M_{S3}	4/20	M_{N2}	2/10
M_{P1}	12/3	M_{N3}	2/10
M_{P2}	4/3	M_{N4}	2/10
M_{P3}	3/3	M_{N5}	1/1
M_{P4}	1/3	M_{N6}	0.22/20
M_{P5}	2*12/3		

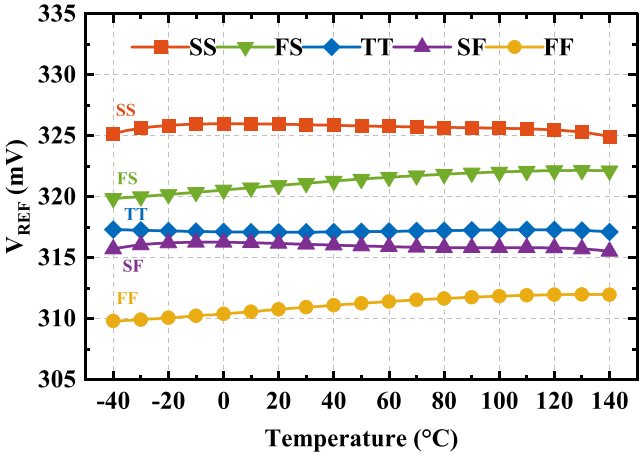

FIGURE 5 Simulation results of the proposed V_{REF} over process corners.

TABLE 2 Summary of the proposed VR over process corners simulation results.

Corner	SS	FS	TT	SF	FF
V_{REF} @ 25°C (mV)	325.9	321.0	317.1	316.1	310.9
TC- V_{REF} (ppm/°C)	18.3	37.7	2.1	13.4	37.9

the exponential characteristics of subthreshold currents. Due to the use of the SDMT structure as the core structure for generating a temperature-independent voltage in the proposed VR, it reduces its dependency on process variations, and increasing the number of SDMT stages can further reduce process dependence and increase the output voltage,[17] but it would result in increased power consumption, area, and minimum operating voltage. So, the proposed voltage reference adopts a single-stage SDMT structure. Figure 5 shows the output voltage of the proposed CMOS VR at different temperatures under different process corners when the supply voltage is 1 V. The simulated TCs are 2 ∼ 38 ppm/°C from −40°C to 140°C among five different corners without any trimming circuits. Table 2 presents the V_{REF} at room temperature and the TCs of the proposed CMOS VR at different process corners. From (11), the sinking current of the temperature compensation circuit is affected by the branch current I_{P3} and is also affected by process deviations. So, the TC of the proposed VR is slightly affected by process deviation. If further reduction in process deviation is required, the 5-bit trimming circuit mentioned by Kelam M et al[21] can be employed. This circuit implements current sourcing action when the reference is less than the desired value and current sinking action when the reference is greater than the desired value. However, considering the area and the fact that the deviation is not significantly large compared to the same type of other circuits, this work ultimately does not use a trimming circuit.

3.3 | Self-biased circuit

The proposed design generates its bias current through M_{N6} via a self-biased feedback path derived from the output reference voltage, V_{REF}. The bias voltage of M_{N6} originates from the output voltage V_{REF}. The self-biased feedback loop produces a bias current of 1.08 nA, subsequently mirrored by the cascode current mirror structure to other branches, forming a stable bias loop, as depicted in Figure 4. Since the self-biased structure has a feedback loop, it is important to discuss the stability of the circuit. Assuming some noise causes V_{REF} to rise, this means the bias current I_{bias} increases. Through the current mirror, an increase in current I_{P1} will cause an increase in V_{GSN2}. When considering the different subthreshold slope factors m for different types of NMOS transistors, Equation (9) can be expressed as:

$$V_{REF} = \left(\frac{m_1}{m_2}V_{TH2} - V_{TH1}\right) + m_1 V_T \ln\left[\frac{I_{N2}}{I_{N2}+I_{N3}}\frac{\mu_1 C_{ox1} K_1 (m_1 - 1)}{\mu_2 C_{ox2} K_2 (m_2 - 1)}\right] + \left(1 - \frac{m_1}{m_2}\right) V_{GSN2} \tag{12}$$

The first two terms are constant for the same temperature. In the CMOS process used, m_1 is larger than m_2. Therefore, the increase of V_{GSN2} will cause V_{REF} to decrease. As a result, the proposed VR circuit has negative feedback and it is stable. The currents of the core voltage reference circuit's two branches, namely I_{P1} and I_{P3}, are determined by the ratio of their current mirror transistors. This ratio must be carefully adjusted to obtain a balance between loop stability, TC performance, and power consumption. The feedback loop additionally introduces a substantial equivalent impedance from the gate of M_{P6} to the ground, thereby diminishing the circuit's sensitivity to the power supply voltage fluctuations and enhancing the LS performance of the circuit. According to (9), considering the constant ratio between I_{N2} and I_{P1} (when the temperature is determined), the output of the VR is independent of the branch current or the gate voltage of the M_{N1} and M_{N2}, which also improves the stability of the VR circuit. In comparison to employing distinct biasing circuits and reference circuits utilizing operational amplifiers, the self-biasing feedback design enhances the LS performance of the circuit without introducing the augmented circuit complexity and elevated power consumption associated with a separate biasing circuit design.

3.4 | Start-up circuit

Because the low-power reference circuit dissipates quite a low amount of power, it will suffer from a slow start-up time. Although the self-biased structure guarantees the normal operation of the circuit, the startup speed is limited to hundreds of milliseconds due to the low power consumption. The low power consumption limits the start-up time of the circuit, so the start-up circuit can get the circuit off the zero-start-up point, which can greatly improve the start-up time of the circuit. The start-up circuit which is also used by Wang L et al[3] comprises three MOS transistors, $M_{S1} \sim M_{S3}$. M_{S1} acts as a MOS capacitor. When the supply voltage is zero, M_{S3} and M_{S2} are both turned off. Upon powering on the circuit, the start-up circuit starts to work. The gate of M_{S2} charges continuously through the MOS capacitor, causing the gate voltage of M_{S2} to increase until it turns on. The gate voltages of M_{P2}, M_{P4}, and M_{P6} are pulled down, leading to the circuit breaking away from the zero point and gradually entering a normal operating state. Once the output voltage reaches a steady state, M_{S3} turns on. This, in turn, pulls down the gate voltage of M_{S2} and turns it off. At this point, the start-up circuit completes its task and the power consumption is close to zero. The start-up circuit improves the starting speed and will close after the circuit is working properly, no longer consuming additional current.

3.5 | Line sensitivity and PSRR analysis

To improve the LS of the design, the cascode current mirror structure is used to replace the traditional single PMOS current mirror to increase the output impedance. To evaluate the dependence of V_{REF} on the change of direct current (DC) voltage, the LS is defined as:

$$LS = \frac{\Delta V_{REF}}{V_{REF} \times \Delta VDD} \times 100\% \tag{13}$$

Although the bias current and output voltage of the proposed self-biased voltage reference theoretically remain unaffected by power supply voltage fluctuations, the non-ideal current mirror will still lead to some influence of power supply disturbance on the bias current and output voltage. From (12), it is clear that the key to improving the performance of LS is to reduce $\Delta V_{REF}/\Delta VDD$ or increase the output voltage V_{REF}. To reduce this influence, the equivalent impedance from VDD to V_{REF} can be increased by the cascode current mirror. Using more stages of SDMT structures can increase the output voltage, but multi-stage SDMT can cause an increase in the minimum power supply voltage and power consumption. Therefore, this design uses a single-stage SDMT structure with temperature compensation and a cascode current mirror structure to achieve a good balance between performance and power consumption. A simplified model of the circuit is shown in Figure 6, where R_1 and R_2 represent the resistances of the cascode current sources. R_3 and R_4 represent the equivalent impedance from the gate of M_{P6} to VDD and to ground, respectively. The output current i_1 and i_2 of the current source are determined by the difference between the gate voltage of M_{P6} and ΔVDD, where the gate voltage of M_{P6} can be expressed as $R_4\Delta VDD/(R_3 + R_4)$. The output value of a current source can be equivalent to the multiplication of its MOSFET gate-source voltage V_{GS} and equivalent transconductance. Therefore, the expressions of i_1 and i_2 are shown in Equation (13) and Equation (14), respectively.

$$i_1 = \frac{G_{m1}R_3\Delta VDD}{R_3 + R_4} \tag{14}$$

$$i_2 = \frac{G_{m2}R_3\Delta VDD}{R_3 + R_4} \tag{15}$$

where G_{m1} and G_{m2} represent the equivalent transconductance of the current sources. R_3 is equal to two diode-connected transistors in series and much smaller than R_4. So, when there is a certain change in the power supply voltage, i_1 and i_2 are extremely small, which is also the reason why the circuit has good LS performance. The expression of $\Delta V_{REF}/\Delta VDD$ is shown in Equation (15).

$$\frac{\Delta V_{REF}}{\Delta VDD} = \frac{(g_{mn1} - g_{mn2})\left(Ag_{m1} + \frac{1}{R_1}\right) - \frac{g_{mn3}(Ag_{m2}R_2+1)}{g_{mn4}R_2+1}}{g_{mn1}\left(\frac{1}{R_1} + g_{mn2}\right)} \tag{16}$$

where $A = R_3/(R_3 + R_4)$. g_{mn1}, g_{mn2}, g_{mn3}, and g_{mn4} represent the equivalent transconductance of M_{N1}, M_{N2}, M_{N3}, and M_{N4}, respectively. The transconductance of a transistor can be changed by its size. In this design, the transistors' sizes should be designed by considering the balance between temperature performance and LS performance, and ultimately the optimum sizes are determined. Due to the improved LS performance of the circuit, the low-frequency PSRR performance is also improved. The simulation results of PSRR performance are shown in Figure 7. It can be seen that the

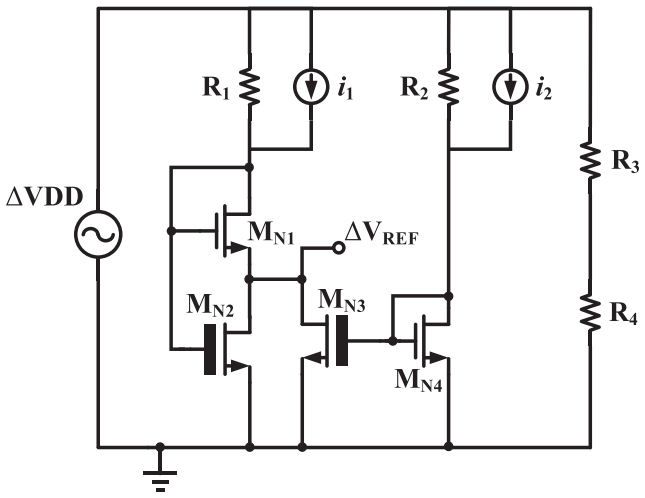

FIGURE 6 Simplified model of the proposed CMOS VR.

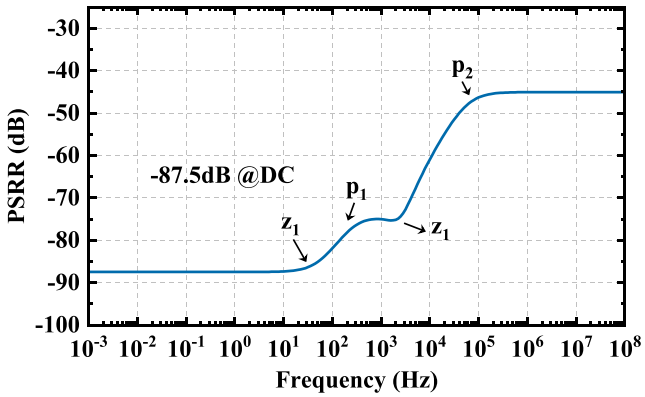

FIGURE 7 The simulated PSRR results of the proposed CMOS VR.

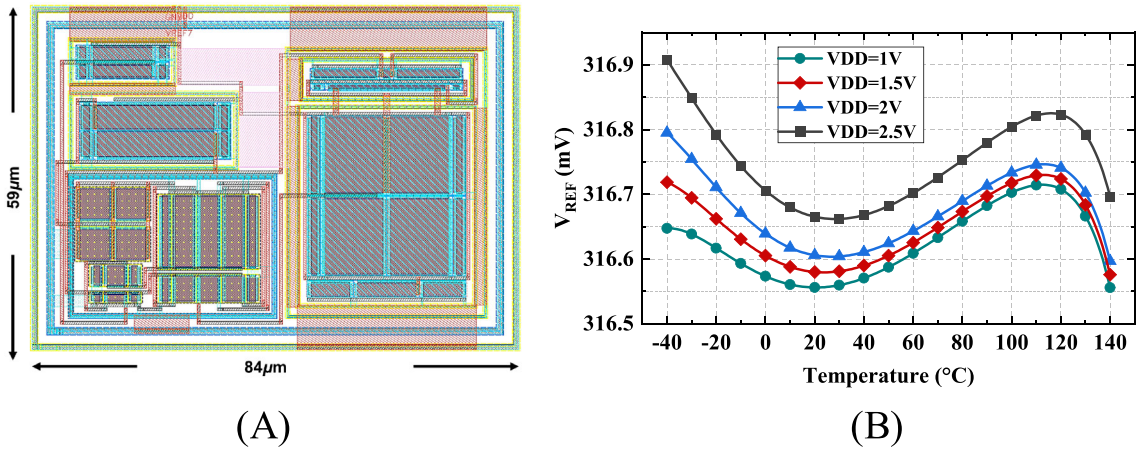

FIGURE 8 (A) Layout of the proposed CMOS VR, (B) post-layout simulation results of the VR from −40°C to 140°C at different *VDD*.

proposed CMOS VR achieves −85 dB @DC. An on-chip decoupling capacitor will reduce noise.[9] At the same time, some on-chip capacitors can also optimize the PSRR performance of the circuit. However, it may degrade start-up time and significantly increase the silicon area. Due to the considerations of ultra-low area and startup speed, the proposed VR circuit does not use on-chip capacitors. Because of the lack of capacitance, the zeros and poles are all generated by the parasitic parameters of the circuit. How to reduce the parasitic parameters effectively should also be considered in the layout design.

4 | POST-LAYOUT SIMULATION RESULTS

The proposed voltage reference circuit is implemented by all MOSFET, and designed using a standard 0.18-μm CMOS process. Figure 8A shows the circuit layout and it occupies an area of 0.005 mm^2. Figure 8B shows the V_{REF} of the proposed CMOS VR at different temperatures under different supply voltages. Due to the use of an improved SDMT structure, the operating temperature range, and TC performance have been significantly enhanced. As a result, the achieved TC is 2.79 ppm/°C within a wide temperature range of −40°C to 140°C when the supply voltage is 1 V. The highest TC is 4.3 ppm/°C over a supply voltage range of 1 V to 2.5 V.

Figure 9A presents the LS of the proposed design at room temperature. The LS is improved by the cascode current mirror structure. Moreover, there is a weak correlation between the output voltage and current. When the power supply voltage reaches above 0.7 V, the circuit outputs a stable reference voltage. The LS of the circuit over a wide power supply voltage range (0.7 V ∼ 2.5 V) is only 0.024%/V. Figure 9B shows a comparison of the pre-layout PSRR and the post-layout PSRR under a power supply voltage of 1 V at room temperature. The parasitic parameters have shifted the circuit's zeros and poles in the PSRR analysis, which results in some degradation of the circuit's PSRR performance in the

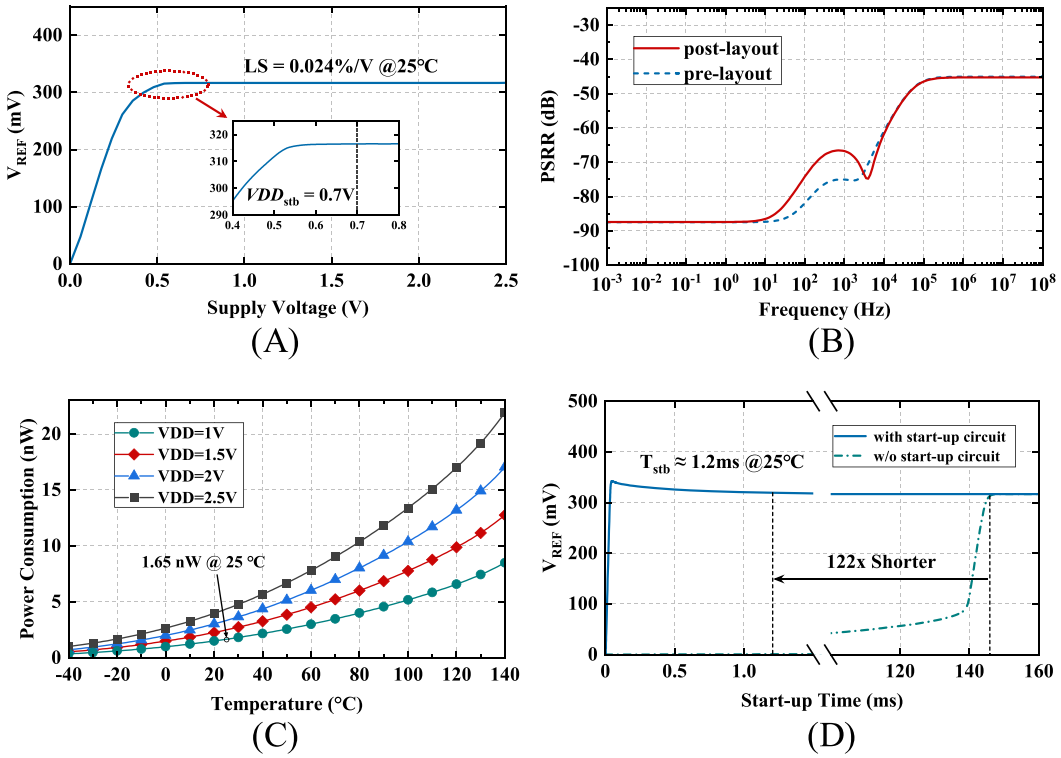

FIGURE 9 (A) Post-layout simulation results of the proposed CMOS VR line sensitivity, (B) post-layout and pre-layout PSRR of the proposed CMOS VR, (C) post-layout simulation results of the proposed CMOS VR power consumption at different temperatures under different supply voltages, (D) post-layout simulation results of start-up time with and without the start-up circuit at room temperature.

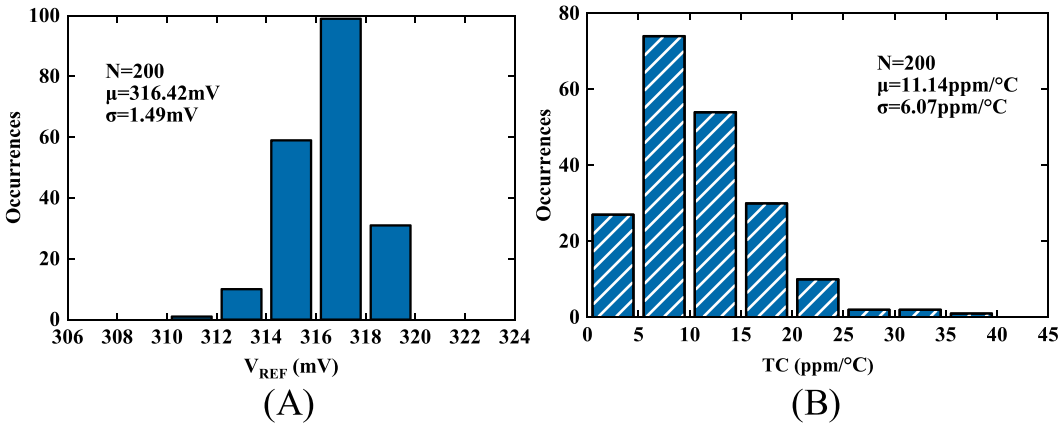

FIGURE 10 (A) Monte-Carlo simulation results of $V_{REF,}$ (B) Monte-Carlo simulation results of TC of V_{REF}.

10 Hz to 10 kHz frequency band. Figure 9C illustrates the power consumption at different temperatures under different supply voltages. When the *VDD* is 1 V, the circuit's power consumption at room temperature is only 1.65 nW. Figure 9D shows the start-up time of the circuit at room temperature. After powering on, the M_{S2} turns on and pulls down the gate of the current mirrors to the ground. The 1% settling time is approximately 1.2 ms with the simple start-up circuit, which is approximately 122 times shorter compared to the one without the start-up circuit. The Monte Carlo simulation results of TC performance and output voltage of the proposed design under a power supply voltage of 1 V are shown in Figure 10A and Figure 10B, respectively. In 200 runs, the average output voltage (μ) is 316.42 mV and its standard deviation (σ) is 1.49 mV, which shows a 0.47% variation (σ/μ). The average TC is 11.14 ppm/°C and its standard deviation is 6.07 ppm/°C. The CMOS VRs usually require trimming to achieve a TC of less than 100 ppm/°C.[17] This work can maintain a good temperature coefficient within a wide temperature range under process variations without trimming.

TABLE 3 Performance summary and comparison with other works.

	[a]This work	[a]Aminzadeh H et al[7]	[a]Shetty D et al[10]	[b]Qiao H et al[15]	[b]Shao C-Z et al[17]	[a]Thomas Abraham N et al[24]
Year	2024	2020	2022	2021	2021	2023
Technology (nm)	**180**	180	180	180	180	180
Type	**CMOS**	Digital CMOS	Sub-BGR	CMOS	CMOS	CMOS
Supply Voltage (V)	**0.7–2.5**	0.7–2.0	0.9	0.25–1.8	0.9–1.8	0.8–2
Power (nW)	**1.65**	21	30	0.113	1.8	15.6
V_{REF} (mV)	**316.56**	147	474	118.1	261	332.85
Temp. Range (°C)	**−40 ∼ 140**	−40 ∼ 125	−20 ∼ 80	−40 ∼ 140	−40 ∼ 130	0 ∼ 120
TC (ppm/°C)	**11.14**	66.38 @ $VDD = 1.0$ V	19	73.5	62	77.425
LS (%/V)	**0.024**	0.031 @ $VDD = 1.3$–1.8 V	0.1	0.3	0.013	0.5
PSRR (dB)	**−86.5@10 Hz**	−90@10 Hz				−48@10 Hz
	−66.7@1 kHz	N/A	N/A	−65@100 Hz	−73.5@1 kHz	−31@1 kHz
	−45.3@1 MHz	−64@1 MHz				−9@1 MHz
Area (mm^2)	**0.005**	0.01	0.04	0.0009	0.005	N/A
Self-biased	**Yes**	Yes	No	Yes	Yes	No
V_{REF}-σ/μ (%)	**0.47 @ 1.0 V**	1.7 @ 1.0 V	0.95 @ 0.9 V	1.1 @ 1.8 V	0.43 @ 0.9 V	0.22 @ 1.0 V

[a]Simulation results.
[b]Measurement results.

Table 3 presents a performance comparison of low-power reference circuits reported in recent years. The comparison shows that the TC performance of Sub-BGR is generally better than that of CMOS VR, the latter is more power-efficient. Achieving stable TC performance in a wide temperature range at the nW level is challenging. This work achieves a wider temperature range of 180°C (−40°C to 140°C) with better TC performance compared to other works because of the proposed temperature compensation circuit. Additionally, due to the use of cascode devices and self-biased circuits, this work achieves good LS and PSRR performance and has a favorable area.

5 | CONCLUSION

In this paper, an ultra-low power subthreshold CMOS voltage reference with a self-biased circuit based on SDMT structure with temperature compensation has been proposed. Without the use of operational amplifiers and capacitors, the proposed voltage reference achieves an average temperature coefficient of 11.14 ppm/°C in a wide temperature range of −40°C ∼ 140°C, using a standard 0.18-μm CMOS process. Self-biased structure and cascode devices are added to suppress the power supply voltage fluctuations. The self-biased structure also reduces circuit consumption and silicon area, which has an advantage in comparison with similar circuits. The temperature compensation circuit enhances the temperature performance of the proposed circuit. Post-layout simulation results demonstrate the circuit's ability to maintain a stable output voltage V_{REF}, even when supply voltage or temperature changes significantly. Overall, the proposed reference voltage can operate at lower power supply voltages, with good temperature performance and power supply rejection performance, as well as ultra-low power consumption and small silicon area. These advantages make this design a good solution for low-voltage and low-power sensor applications even in environments with significant temperature changes.

DATA AVAILABILITY STATEMENT

Data sharing is not applicable to this article as no new data were created or analyzed in this study.

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