A 0.816nW 12.3pS Tunable Low-G_m Transconductor for Bio-electrical Signal Acquisition

Feng Yan, Bingjun Xiong, Wenji Mo, Kangkang Sun, Jian Guan, and Jingjing Liu

School of Electronics and Communication Engineering, Sun Yat-sen University, Shenzhen 518107, China
E-mail: liujj77@mail.sysu.edu.cn

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***Abstract*—A transconductance amplifier with low-G_m is indispensable for applications that acquire low-frequency bio-electric signals. This paper proposes a subthreshold bootstrapped low-G_m transconductor based on body-input. The input topology of the transconductor consists of two transistors with body inputs and a source degeneration resistor. The outputs of the two transistors are connected to the resistor to bootstrap the voltages at these terminals and increase the equivalent resistance. An area-efficient serial-parallel current division network is further adopted to reduce the G_m of the transconductor. Meanwhile, programming the bias voltage can tune the G_m value. The circuit is designed using a standard 0.18 µm CMOS process. Simulations verify the characteristics of the proposed transconductor. The post-layout simulation results show that the transconductor's G_m value is tunable within a range of a few hundred pS. The minimum achievable G_m is 12.3 pS, and the linear input range is ±150 mV. The input referred noise power spectral density (PSD) of the transconductor is 13.7 µV/√Hz. It consumes 0.816 nW of power with 0.8 V supply voltage and occupies an area of 0.0057 mm².**

Keywords—transconductance amplifier, bio-electric signals, body-input, bootstrap

I. Introduction

The primary detection targets of medical electronic devices are low-frequency, low-amplitude bio-electric signals, where the signals of interest have a frequency distribution in the range below 1 Hz (typically less than 0.5 Hz for electroencephalogram (EEG) [1]). The acquisition of low-frequency bio-electrical signals requires active filters with a large time constant. While large capacitors can achieve such low cutoff frequencies, their significant on-chip area is undesirable in implantable acquisition chips. Switched-capacitor [2] and switched-resistor [3] techniques offer an area-efficient solution. However, their linearity is limited to 8 bits [4] due to the variations in voltage on both sides, and they are highly sensitive to the process, voltage, and temperature (PVT) variations. A popular approach is to utilize transconductors with exceptionally low-G_m values. If considering an on-chip capacitance of 10 pF, and designing an active low-pass filter with a cutoff frequency below 0.5 Hz, the G_m of the transconductor should be less than 30 pS.

Traditional linear transconductors are designed based on transistors operating in the strong inversion region [5]. The conversion from voltage to current is accomplished through the input differential pairs, while the other transistors simply replicate the current to the output. It becomes challenging to achieve G_m below nanosiemens with this approach. The current distribution scheme [6] allocates a portion of the signal current in the strong inversion region to the output current in order to reduce the transconductance. However, this technique results in significant power consumption due to the waste of operating current. Transistors operating in the sub-threshold region can take advantage of the large G_m/I_D ratio to achieve low transconductance while operating with a significantly small current [7]. Unfortunately, this technique leads to non-linear transfer characteristics of the transconductor, thereby limiting the input linear range within 100 mVpp. Another option is to utilize an active voltage attenuator at the input of the operational transconductance amplifier (OTA) to decrease its transconductance [8]. The main disadvantages of this technique are the presence of DC offset and the increased noise contribution from the OTA. Furthermore, the current cancellation technique reduces the equivalent transconductance of the OTA by dividing each transistor of the differential pair into two parallel transistors [9]. Moreover, this technique is constrained by device mismatch and noise, consequently limiting the reduction factor of G_m to 20 times.

In recent years, the concept of body-driving technique has emerged [10], as body transconductance (g_{mb}) is typically smaller than gate transconductance (g_m). This paper proposes a novel tunable transconductor with body-input to achieve an exceptionally low-G_m. The topology is realized based on body-input bootstrapping technique and series-parallel current mirrors. Compared to the bootstrap-based pseudo-differential transconductor [11], the proposed solution offers lower transconductance and a smaller on-chip area.

The remaining parts of this paper are organized as follows. Section II introduces the proposed technique for reducing transconductance. The circuit structure of the proposed low-G_m transconductor is presented in Section III. Section IV analyzes the post-layout simulation results and considerations for mismatch. Finally, the conclusions are given in Section V.

II. Proposed G_M Reduction Technique

Bootstrap, as a voltage feedback technique, is commonly used to increase the input impedance of amplifiers [12]. As

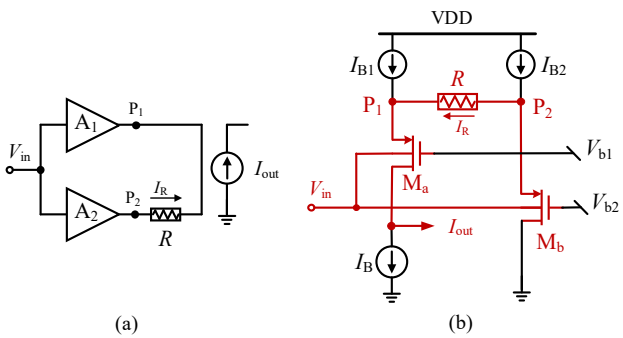

Fig.1 (a) The concept of bootstrapping technique. (b) Implementation of the proposed body-input boosting technique.

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shown in Fig. 1(a), the outputs of two voltage amplifiers, A_1 and A_2, are connected to the terminals of resistor R. In this scenario, the current through the resistor is given by $I_R = V_{in}$ (A_2-A_1) / R. By copying the current I_R through a current mirror to the output, the conversion from input voltage V_{in} to output current I_{out} is achieved. If the gains of A_1 and A_2 are similar, it means that the voltages applied to both ends of resistor R at points P_1 and P_2 are similar. In this case, only a very small current flows through R, thus achieving a remarkably low-G_m value [11]. The transconductance value of this bootstrapping technique is given by $G_m = (A_2\text{-}A_1) / R$.

The proposed body-input boosting technique is shown in Fig. 1(b). Two voltage amplifiers A_1 and A_2 are implemented using transistors M_a and M_b with the same dimensions. They are designed to have similar gains, allowing the transconductor to achieve a remarkably low value of G_m. The input voltage V_{in} is applied to the bodies of both transistors, and the operating current is routed through the M_a pathway to the output. The use of PMOS configuration allows its body to be the input due to N-well fabrication technology.

In contrast to conventional gate-driven circuits, the input terminals of body-driven transistors are comprised of PN junctions, and the gate terminals of these devices are biased to suitable levels to establish conductive channels. In the standard CMOS process, the g_{mb} is typically 2 to 5 times smaller than g_m, and the drain current of MOS transistors is determined by the value of threshold voltage. The threshold voltage for P-channel devices can be represented as (1) [13].

$$|V_{TH}| = |V_{TH0}| + |V_{OFF}| + \Delta V_{TH} \tag{1}$$

where V_{TH0} is the value of the threshold voltage V_{TH} when the body-to-source voltage is zero, V_{OFF} is the offset threshold voltage of a transistor operating in the sub-threshold region, ΔV_{TH} is the change in threshold voltage caused by body effect and it can be expressed by (2).

$$\Delta V_{TH} = |\gamma| \cdot \left[\sqrt{2|\phi_F + V_{BS}|} - \sqrt{2|\phi_F|} \right] \tag{2}$$

where γ is the body effect parameter, ϕ_F is Fermi potential, and V_{BS} is body-to-source voltage. The operation of body-driven devices is based on the body effect, that is the dependence of V_{TH} on V_{BS}. The drain current I_D varies with V_{BS}, thus achieving the transconductance function between the body voltage and drain current. Since the transistor is biased in weak inversion, the voltages at nodes P_1 and P_2 are given by (3) and (4) respectively.

$$V_{P1} = V_{in} - nV_t \cdot \ln\left[\frac{I_{B1} + I_R}{I_{S0}} \right] \tag{3}$$

$$V_{P2} = V_{in} - nV_t \cdot \ln\left[\frac{I_{B2} - I_R}{I_{S0}} \right] \tag{4}$$

where V_t is the thermal voltage, n is the slope factor and I_{S0} is the operating current. When $I_R << I_{B1}$, I_{B2}, the current I_R can be approximated by the Taylor expansion as (5).

$$I_R \approx -nV_t \frac{I_{B1} I_{B2}}{R I_{B1} I_{B2} + nV_t (I_{B1} + I_{B2})} \cdot \ln\left[\frac{I_{B1}}{I_{B2}} \right] \tag{5}$$

From (5), it can be observed that the bias currents I_{B1} and I_{B2} establish a direct current through resistor R. In the case of ideal current sources, the gains of the two amplifiers are $A_1 = A_2$, which implies that the transconductance of the proposed body-input circuit is zero.

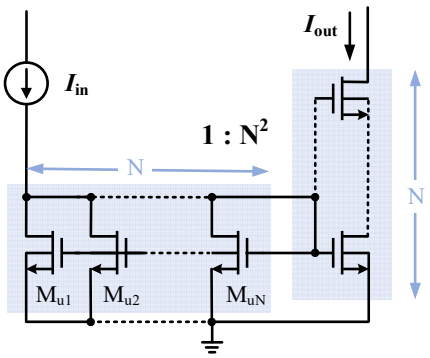

Fig. 2 Current mirrors with a series-parallel current division to reduce transconductance without loss in the linear range.

Additionally, the design of the current mirror which copies the current I_R to the output needs to be considered. By employing series-parallel current splitting in the OTA, the area-efficiency can be improved. The technique of series-parallel current distribution is particularly suitable for designing transconductors with low G_m [14]. For the NMOS current mirror depicted in Fig. 2, N unit transistors M_{uN} are placed in series and parallel to reduce an effective output transconductance, which can be expressed as (6).

$$G_m = \frac{g_{m1}}{N^2} \tag{6}$$

where g_{m1} represents the transconductance of transistor M_{uN}, and N^2 can be expressed as the transconductance attenuation factor. The current mirrors of in Fig. 2 are not only area-efficient because their area is proportional to the square root of the copy factor, but also mismatch-efficient because they benefit from the layout matching of the common centroid geometry and the same surroundings.

III. Proposed Tunable Low-G_M Transconductor

The proposed low-G_m transconductor, as shown in Fig. 3, is composed of a bias current source, differential G_m-reduction block, and series-parallel current mirror. As mentioned earlier, the G_m-reduction block is implemented by body-input PMOS transistors M_1 to M_4. Source-degeneration resistors are realized by M_5 to M_8 and they are connected to

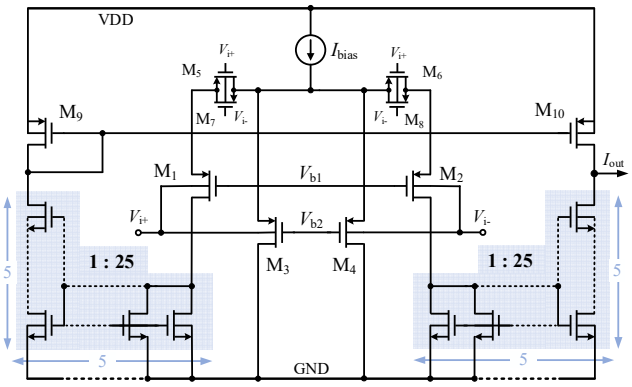

Fig. 3 Proposed tunable low-G_m transconductor circuit.

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the outputs of the four body-input transistors. Benefiting from the source degeneration effect, the effective G_m of the input differential pair is reduced. The input pair and source degeneration resistor MOSFETs with equal dimensions are all biased in the deep sub-threshold region. Here, the body of the source degeneration resistor MOS is biased by VDD to modulate the transistor and provide additional degrees of freedom [7]. The output current of each module is replicated to the output branch through series-parallel current mirrors to cancel the DC component. These current mirrors have an equal gain and they include five transistors in parallel and five transistors in series, dividing the input current by a factor of 25 to further reduce G_m. The proposed circuit achieves low transconductance in this manner, and it can be adjusted through bias voltages V_{b1} and V_{b2}.

The proposed transconductor circuit is designed using a standard 0.18 μm CMOS process, and the chip layout is depicted in Fig. 4. To minimize the impact of layout mismatch, a common centroid arrangement is employed in the layout along with the utilization of dummy transistors. The proposed transconductor has an effective area of only 0.0057 mm^2, resulting in approximately half area reduction compared to the recent work of self-bootstrapped pseudo-differential OTA [11].

The relationship between the analog output current of the proposed transconductor and the differential input voltage is illustrated in Fig. 5. When V_{b1} = 450 mV and V_{b2} = 360 mV, the results demonstrate that the transconductor exhibits a minimum G_m value as low as 12.3 pS, with a linear range exceeding ± 150 mV. The proposed transconductor circuit demonstrates exceptional robustness. The transmission characteristics have been evaluated through 1000 Monte Carlo simulations, and the results are depicted in Fig. 6. The average G_m value is 12.3 pS, with a standard deviation of only 0.6 pS.

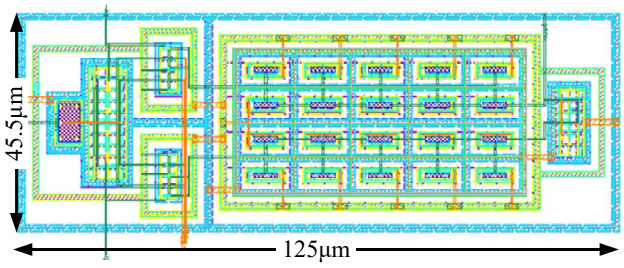

Fig. 4 Layout of the proposed tunable low-G_m transconductor.

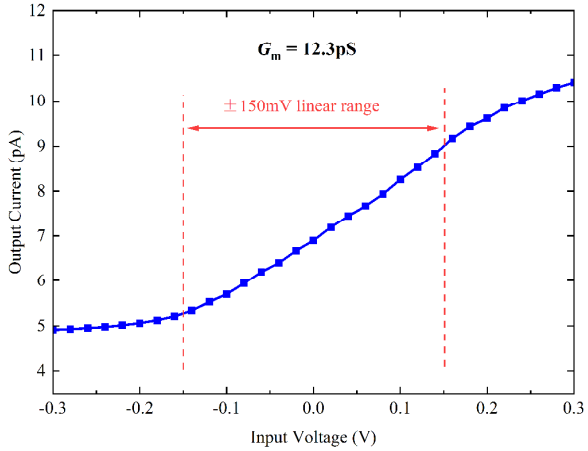

Fig. 5 Post-layout simulation results of the output current of the proposed transconductor versus the input voltage.

IV. Simulation Results and Mismatch Considerations

In order to gain an in-depth understanding of the proposed transconductor operation, some simulations are provided for the tunable characteristics and mismatch considerations of the transconductor.

As shown in Fig. 7, the tunable transconductor can provide a variable G_m value by programmatically bias voltages V_{b1} and V_{b2}. When V_{b1} = 450 mV and V_{b2} = 490 mV, the transconductor achieves its maximum G_m value of 225.5 pS. Undoubtedly, it can be employed within the instrumentation amplifier of medical electronic devices. The proposed transconductor allows for adjustable cutoff frequencies within the range of 0.19 to 3.6 Hz by utilizing a 10 pF load capacitor. Alternatively, a cutoff frequency of 0.5 Hz can be achieved by utilizing a mere 4 pF capacitor, resulting in a smaller capacitor area and noise contribution. In other words, the bias voltage can be adjusted to ensure the desired G_m value even in the presence of process and temperature variations. The input referred noise of the transconductor within the range of 0.1 Hz to 10 MHz is shown in Fig. 8. The transconductor exhibits an input-referenced thermal noise of 13.7 μV/√Hz.

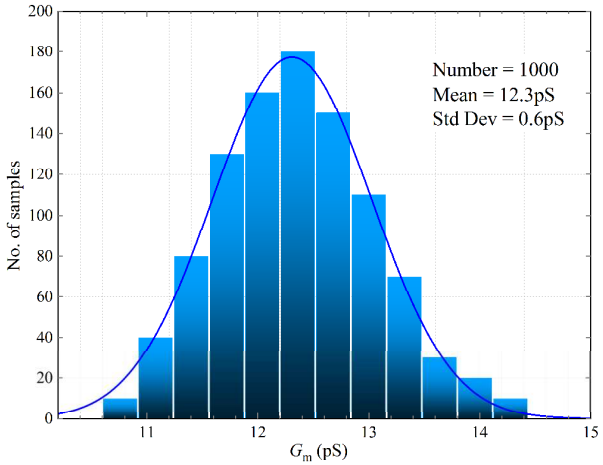

Fig. 6 Monte Carlo simulation of the proposed transconductor with 1000 runs at V_{b1} = 450 mV and V_{b2} = 360 mV.

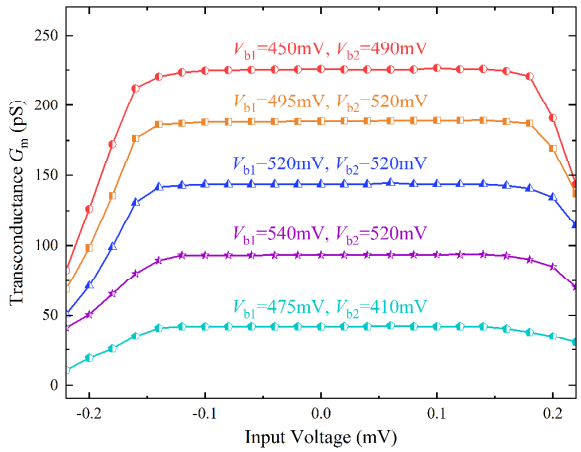

Fig. 7 G_m value of the proposed transconductor at different bias voltages.

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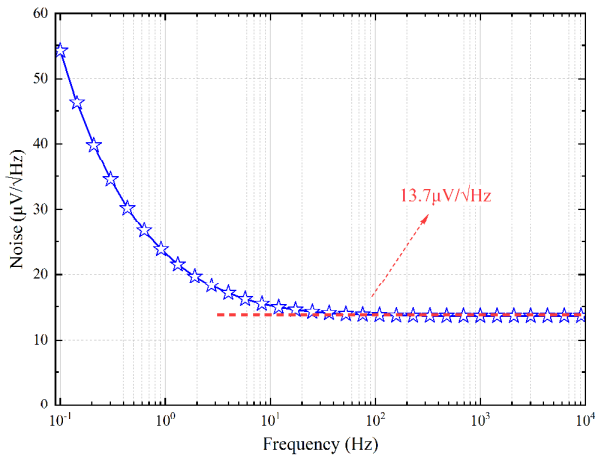

Fig. 8 Input-referenced noise PSD of the proposed transconductor.

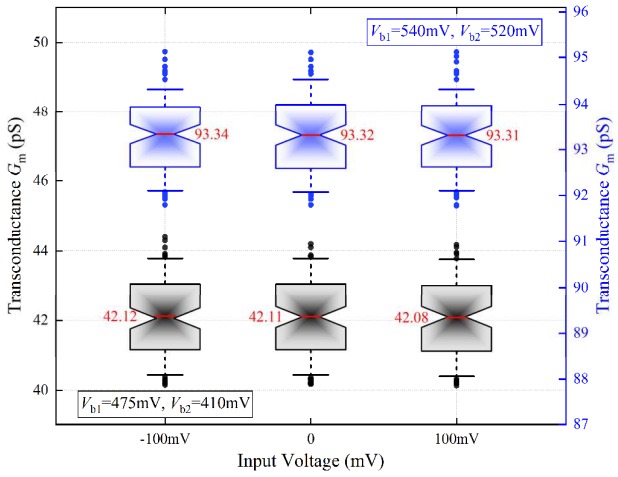

Fig. 9 Box plot of the transconductor at two bias voltages.

TABLE I
PERFORMANCE COMPARISON WITH OTHER LOW-G_M TRANSCONDUCTORS

Parameter	[16]'14* *MJ*	[17]'19 *Sensors*	[18]'19 *CSSP*	[15]'20 *Sensors*	[11]'22 *TCASII*	**This Work****
Process (μm)	0.35	0.18	0.18	0.18	0.18	**0.18**
Supply (V)	5	1.8	0.3	1	1.8	**0.8**
Power (μW)	160	5.4	0.05	0.27	4	**0.000816**
Technique	Full Differential	Current Attenuation	Bulk Driven	Bulk Driven	Bootstrapping	**Body-Input Boosting**
Area (mm^2)	0.006	0.014	0.035	0.027	0.0099	**0.0057**
Gm (nS)	39.5–367.2	0.5–5000	68–460	0.062–6.28	15–18.5	**0.012–0.225**
Input-Referred Noise	104.7 μV_{rms} (10–300k Hz)	1.63 μV_{rms}* (0.06–5 Hz)	1.33 μV/√Hz* @10 Hz	760 μV_{rms}* (1–100 Hz)	70.3 μV/√Hz @100 Hz	**13.7 μV/√Hz @100 Hz**
CMRR (dB)	44.8	N/A	57	56	N/A	**45**

*Simulation results ** Post-layout simulation results

To assess the impact of device mismatch on the G_m, random sampling simulations (100 runs each) of the proposed transconductor are conducted with three different input voltage amplitudes (-100 mV, 0 mV, and 100 mV). Fig. 9 displays the box plots of the impact of mismatch on G_m under two different bias voltage conditions. The red line in the box plot represents the average value of G_m. When V_{b1} = 475 mV and V_{b2} = 410 mV, the G_m is 42.1 pS under all three cases, and V_{b1} = 540 mV and V_{b2} = 520 mV, the G_m is 93.3 pS. It can be seen that the distribution is symmetric. The boxes cover the interquartile range of the distribution, i.e., 50% of the measurement would lie in the range, from 41.2 to 43.0 pS and 92.5 to 94.1 pS, respectively.

Table I summarizes the comparison of the proposed work with the latest designs in the literature. Compared to bulk-driven-based transconductance amplifiers [15], the proposed solution offers lower transconductance values and a smaller on-chip area. As a result, the proposed transconductor exhibits tunable low-G_m with low power consumption, low noise contribution, and low area consumption.

V. CONCLUSION

In this paper, a tunable low-G_m, low-power, and low-noise transconductor with body-input bootstrapping topology is proposed for bio-electrical signal acquisition. The bootstrapping technique based on sub-threshold operation and a series-parallel current mirror with a 25-fold attenuation factor is employed to achieve a low cutoff frequency. Compared to conventional transconductors, the proposed body-input stage exhibits a wider adjustable range and superior linearity. The utilization of attenuation factor in the series-parallel current mirror can further reduce the transconductance. The proposed circuit is designed using 0.18 μm CMOS technology, with a supply voltage of 0.8 V and a current consumption of 1.02 nA. The post-layout simulation results indicate that for a 10 mVpp differential input signal at 100 Hz, the tunable range of the G_m is 12.3 to 225.5 pS, with a standard deviation of 0.6 pS. The input reference thermal noise PSD is 13.7 μV/√Hz. As a conclusion, the proposed transconductor achieves a tunable low-G_m with a good trade-off between input linearity, noise, and power consumption. In practical scenarios, programmable voltage can be used to adjust the desired G_m value for measuring different biological signals.

REFERENCES

[1] M. Guermandi, R. Cardu, E. Franchi and R. Guerrieri, "Active electrode IC combining EEG, electrical impedance tomography,

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continuous contact impedance measurement and power supply on a single wire," *2011 Proceedings of the ESSCIRC (ESSCIRC)*, Helsinki, Finland, 2011, pp. 335–338.

[2] N. Verma, A. Shoeb, J. Bohorquez, J. Dawson, J. Guttag and A. P. Chandrakasan, "A micro-power EEG acquisition SoC with integrated feature extraction processor for a chronic seizure detection system," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 804–816, Apr. 2010.

[3] T. Y. Wang, M. R. Lai, C. M. Twigg, and S. Y. Peng, "A fully reconfigurable low-noise biopotential sensing amplifier with 1.96 noise efficiency factor," *IEEE Trans. Biomed. Circuits Syst*., vol. 8, no. 3, pp. 411–422, Jun. 2014.

[4] V. Majidzadeh, A. Schmid, and Y. Leblebici, "Energy efficient low-noise neural recording amplifier with enhanced noise efficiency factor," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 3, pp. 262–271, Jun. 2011.

[5] Z. Wang *et. al.*, "A voltage-controllable linear MOS transconductor using bias offset technique," *IEEE J. Solid-State Circuits.*, vol. 25, pp. 315–317, 1990.

[6] A. Veeravalli *et. al.*, "A CMOS transconductor amplifier architecture with tuning range for very low frequency applications," *IEEE J. Solid-State Circuits*, Vol. 37, pp. 776–781, 2002.

[7] D. Luo, M. Zhang, and Z. Wang, "A low-noise chopper amplifier designed for multi-channel neural signal acquisition," *IEEE J. Solid-State Circuits*, vol. 54, no. 8, pp. 2255–2265, Aug. 2019.

[8] C. D. Salthouse and R. Sarpeshkar, "A practical micropower programmable bandpass filter for use in bionic ears," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 63–70, Jan. 2003.

[9] J. Silva-Martinez and J. Salcedo-Suñer, "IC voltage to current transducers with very small transconductance," *Analog Integr. Circuits Signal Process.*, vol. 13, pp. 285–293, Jul. 1997.

[10] Khateb, F., Kulej, T. & Vlassis, S. "Extremely low-voltage bulk-driven tunable transconductor," *Circuits Syst. Signal Process*, vol. 36, pp. 511–524, 2017.

[11] O. J. Cinco-Izquierdo, C. A. de la Cruz-Blas, and M. T. Sanz-Pascual, "High-linearity tunable low-G_m transconductor based on bootstrapping," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 69, no. 2, pp. 259–263, Feb. 2022.

[12] Y. M. Chi, C. Maier, and G. Cauwenberghs, "Ultra-high input impedance, low noise integrated amplifier for noncontact biopotential sensing," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 1, no. 4, pp. 526–535, Dec. 2011.

[13] J. M. Carrillo, J. F. Duque-Carrillo and G. Torelli, "Design considerations on CMOS bulk-driven differential input stages," *2012 International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)*, Seville, Spain, 2012, pp. 85–88.

[14] A. Arnaud, R. Fiorelli, and C. Galup-Montoro, "Nanowatt, sub-nS OTAs, with sub-10-mV input offset, using series-parallel current mirrors," *IEEE J. Solid-State Circuits*, vol. 41, no. 9, pp. 2009–2018, Sept. 2006.

[15] J. Jakusz, W. Jendernalik, G. Blakiewicz, M. Kłosowski, and S. Szczepanski, "A 1-nS 1-V Sub-1-μW linear CMOS OTA with rail-to-rail input for Hz-band sensory interfaces," *Sensors*, vol. 20, no. 11, p. 3303, Jun. 2020.

[16] C.F.T. Soares, G. S. Moraes, A. Petraglia, "A low-transconductance OTA with improved linearity suitable for low-frequency Gm-C filters," *Microelectron. J.* vol. 45, pp. 1499–1507, 2014.

[17] J. Pérez-Bailón, B. Calvo, and N. Medrano, "A CMOS low pass filter for SoC lock-in-based measurement devices," *Sensors*, vol. 19, no. 23, p. 5173, Nov. 2019.

[18] F. Khateb, T. Kulej, M. Akbari, and P. Steffan, "0.3-V bulk-driven Nanopower OTA-C integrator in 0.18 μm CMOS," *Circuits Syst. Signal Process.*, vol. 38, pp. 1333–1341, Jul. 2019.

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