A 0.88nW Ultra-Low G_m Tunable Transconductor Based on Bootstrap-Body-Input for Biomedical Sensors

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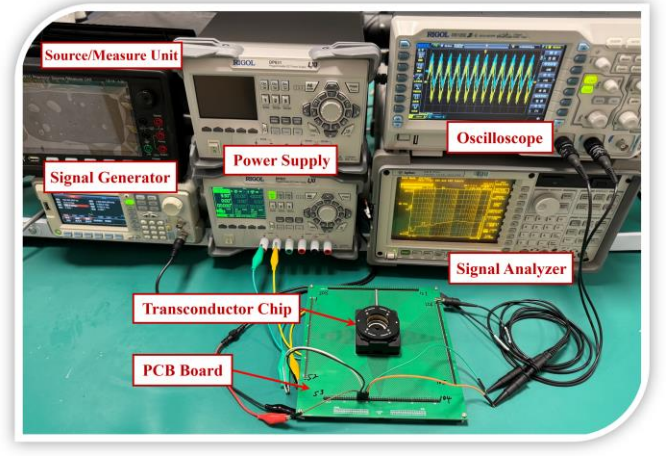
***Abstract*—Low-transconductance (G_m) amplifiers are essential for implementing low-frequency continuous-time filters, a critical aspect for biomedical sensors. This paper proposes a low-power, low-G_m amplifier based on the bootstrap-body-input technique. The input topology of the transconductor consists of two transistors with body-inputs and a source degeneration resistor. The source of the two transistors connected to the resistor, which bootstraps the terminal voltages and expands the input range. To further reduce the G_m value of the transconductor, an area-efficient series-parallel current mirror is adopted. The transconductor was fabricated in a 0.18 μm CMOS process. Measurement results show that the bootstrap-body-input transconductor achieves a reduction in G_m value of more than 1200 times over conventional body-input transconductor. The proposed transconductor features a tuning range of 27 to 581 pA/V at 0.8 V supply voltage, with a power consumption of only 0.88 nW. The input-referred noise is measured at 25.4 μV/√Hz at 100 Hz and the power supply rejection ratio exceeds 56 dB. Tuning tests reveal that the proposed transconductor allows for programming the control voltage of the remaining gate terminals to adjust the G_m value, compensating for variations in process, voltage, and temperature.**



***Index Terms*—Biomedical sensors, bulk-driven, low transconductance value, programmable voltage, transconductor.**

I. Introduction

With the advancement of medical technology, and biomedical sensors are being intensively researched in the wearable [1], [2] and implantable direction [3], [4]. The main detection targets of these devices are low-amplitude bioelectrical signals, where the frequencies of interest are usually in the range of DC to 10 kHz [5], [6]. Fig. 1 illustrates a typical analog front-end block diagram for the bioelectric signal acquisition channel, which includes a pre-amplifier, a low-pass filter (LPF), a programmable post-amplifier, and an analog-to-digital converter (ADC). In this system, the pre-amplifier performs 20 to 40 dB amplification of weak bioelectric signals (e.g. EEG, ECG, and EMG) [7]. Behind the pre-amplifier, an ultra-low power filter with a low-cutoff frequency is required to reject the out-of-band noise [8]. The post-amplifier is a programmable amplifier that not only relaxes the design of the pre-amplifier but also amplifies the filtered output signal to reduce the influence of switch-induced noise from the sampling behavior of the ADC [9].

The continuous-time LPF have become a key component in various biosensors. Area and power budgets in wearable or implantable acquisition systems can be very tight due to limited form factors and power resources [10]. In order to reduce the chip cost and extend the operating time of the system, an LPF with small areas and low power consumption are necessary. A popular method to achieve such a low-cutoff frequency filter on a small chip area is to use an extremely low transconductance amplifier [11]. Unfortunately, it is difficult to achieve low G_m values with ordinary linear transconductor designed based on transistors operating in the strong inversion region [12]. This is primarily because the input differential pair only performs voltage-to-current conversion, and the other transistors simply replicate the current to the output. The current cancellation technique reduces the equivalent G_m of the operational transconductance amplifier (OTA) by splitting the input transistor into two parallel transistors [13]. However, this technique

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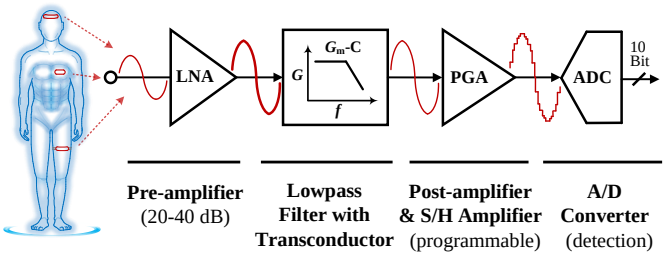

Fig. 1. A typical analog front-end circuit block diagram with a low-pass filter for biomedical sensors.

suffers from device mismatch and noise, resulting in the G_m reduction factor being limited to 20 times. Simply partitioning the output current of a differential pair at a high ratio is widely regarded as an area-expensive technique [14]. Furthermore, transistors operating in the subthreshold region can obtain small transconductances (45 pS) with the application of very low operating currents [15]. However, this technique degrades the linear transfer characteristics of the transconductor, resulting in a linear input range limited to 100 mV_{pp}. The multi-input MOS-transistor technique can expand the input voltage range and reduces the DC voltage gain of the OTA [16]. While this approach decreases the G_m, the additional input capacitance divider significantly increases the area of the chip [17], [18].

Without applying any enhancement technique, body driving becomes an attractive solution for designing low-G_m OTA circuits due to the inherent property that the body-transconductance (g_{mb}) is smaller than gate-transconductance (g_m) [19]. The conduction of body-driven input transistors is controlled by the body terminal voltage, with the body threshold voltage typically being lower than the gate threshold voltage. This characteristic enables body-input transconductor to process input signals at lower levels, rendering them particularly well-suited for applications involving weak bioelectrical signals. The circuit of a conventional body-input transconductor is shown in Fig. 2. Unfortunately, the G_m values realized by this circuit are not sufficient to meet the requirements of low-cutoff frequencies of filters in biosensors. This paper proposes a bootstrap-body-input transconductor to overcome the above limitations. It shows low area, low power consumption, high linear input range, and tunable low G_m values. The proposed topology is realized based on the single current source bootstrap body terminal and series-parallel current mirrors technique. The proposed transconductor achieves a reduction in G_m value of more than 1200 times over conventional transconductor. Additionally, compared to the state-of-the-art G_m values reported in [15], the proposed transconductor offers a twofold improvement and possesses programmable characteristics.

This work was first introduced in [20]. The complete study and measurement results with additional details is presented here. Section II explains the proposed bootstrap-body-input topology and the tunable G_m technique. Section III describes the circuit of the proposed bootstrap-body-input transconductor and compares it with conventional transconductors. Detailed characterization results of the transconductors are given in Section IV. Finally, conclusions are drawn in Section V.

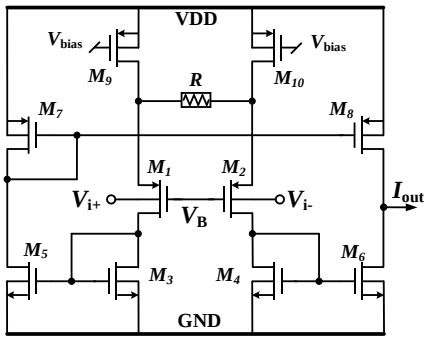

Fig. 2. The conventional body-input transconductor.

II. Proposed Bootstrap-Body-Input Technique

Body-drive, as a low voltage technique, is typically used in low-power biosensors. Compared to the gate driving [21], body driving offers superior signal sensitivity and allows more precise threshold voltage control. In Fig. 2, the input signal is applied to the body terminals of the input pair M_1 / M_2 to modulate the drain-source current I_{DS}. The I_{DS} of the MOS transistor operating in a subthreshold region can be given by (1).

$$I_{DS} = I_S\left(\frac{W}{L}\right)\exp\left(q\frac{V_{GS}-V_{TH}}{nkT}\right)\left[1-\exp\left(-q\frac{V_{DS}}{kT}\right)\right] \quad (1)$$

where k is the boltzmann constant, T is the absolute temperature, q is the elementary charge, I_S is the characteristic current and n is the slope factor in the sub-threshold region. The g_m can be presented as a function of current I_{DS} only. Similarly, the g_{mb} exists in a body-driven transistor [22]. The ratio of g_{mb} to g_m can be described by η, which can be expressed as (2).

$$\frac{g_{mb}}{g_m} = \frac{g_{mb}}{q\cdot I_{DS}/nkT} = \frac{\gamma}{2\sqrt{2\phi_F + V_{BS}}} = \eta \quad (2)$$

where γ is the body effect parameter, ϕ_F is Fermi potential, and V_{BS} is body-to-source voltage. It is evident that the ratio η depends on the specific process parameters. In the 0.18 μm CMOS technology, the g_{mb} is typically 2 to 5 times smaller than the g_m.

Bootstrap, as a voltage feedback method, is commonly used to reduce the current in a specific path or increase the input impedance of the amplifiers [23]. One application of this technique involves using a resistor R connected between the input and output of a gain amplifier A, as depicted in Fig. 3(a). The equivalent input resistance of the circuit is $R_{eq}=R/(1-A)$. If the amplifier's gain approaches unity, meaning similar voltages are applied across the two terminals of the resistor, this equivalent resistance becomes very high. The circuit depicted in Fig. 3(b) operates on a similar principle, employing two voltage amplifiers, A_1 and A_2, to ensure that the voltages at both terminals of the resistor are nearly identical. In this scenario, the current through the R can be rewritten as (3).

$$I_R = \frac{V_{in}(A_2 - A_1)}{R} \quad (3)$$

By copying the current I_R through a current mirror to the output, the conversion from input voltage V_{in} to output current I_{out} is achieved. If the gains of A_1 and A_2 are similar, it means

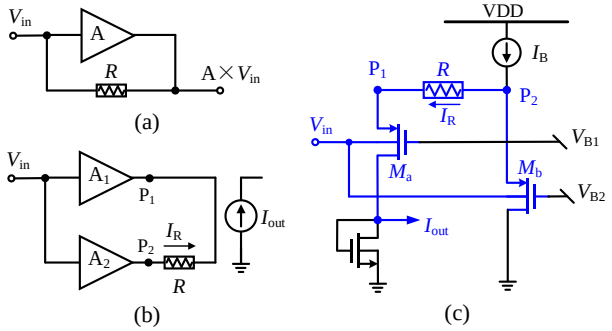

Fig. 3. (a) The concept of bootstrapping. (b) The principle of bootstrapping technique. (c) The proposed bootstrap-body-input circuit.

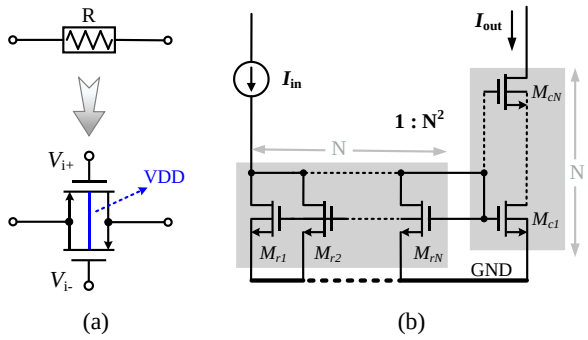

Fig. 4. (a) The source degeneration resistor. (b) Current mirrors with a series-parallel current division to reduce transconductance.

that the voltages applied to the two ends of resistor R at points P_1 and P_2 are similar. The current flowing through R is very small, resulting in a greatly reduced I_{out}. The small I_{out} indicates that the transconductor implements low G_m values.

The principle of the proposed bootstrap-body-input technique is shown in Fig. 3(c). The PMOS transistors are selected as input pairs since the body of the N-Well can be used as an input terminal. Two voltage amplifiers A_1 and A_2 are implemented using transistors M_a and M_b with body-driven and the same dimensions. The body input is used to reduce the voltage-to-current conversion to obtain a smaller G_m value than the gate input. Since the amplifiers M_a and M_b are designed to have similar gains, the current flowing through the resistor R is extremely small. This operating current I_{out} is mirrored to the output, allowing the transconductor to achieve a very low G_m value. The G_m value of this bootstrapping technique is given by (4).

$$G_m = \frac{A_2 - A_1}{\mathrm{R}} \tag{4}$$

The bootstrap-body-drive technique allows the transistors of the input pair to conduct at low voltages, which effectively extends the input common-mode voltage range and enables them to operate at very low supply voltages. Unlike conventional gate-drive circuits, the common-mode voltage behavior of the input transistor needs to be carefully considered since the input terminals of the body-drive transistor consist of PN junctions. When a common-mode signal V_{incm} equal to the supply voltage is applied to the body input differential pair, the voltages at nodes P_1 and P_2 are significantly lower than this level, causing the $M_{a,b}$'s source-body PN junctions are operating in the reverse bias region. As V_{incm} decreases, the voltages V_{P1} and V_{P2} decrease correspondingly. Once V_{incm} becomes less than V_{P1} and V_{P1}, the $M_{a,b}$'s source-body PN junctions begin to operate in the forward bias region. Due to the implementation of a single current source, the voltage at node P_1 will not exceed that at node P_2. Therefore, even with V_{B1}=V_{B2}, there is no concern about polarity reversal as in [24]. The gate terminals of these input transistors are biased at appropriate levels to establish conductive channels. The drain current of a PMOS transistor depends on the value of the threshold voltage, which can be expressed as (5).

$$\left|V_{TH}\right| = \left|V_{TH0}\right| + \gamma \cdot \left[\sqrt{2\left|\phi_F + V_{BS}\right|} - \sqrt{2\left|\phi_F\right|}\right] \tag{5}$$

where V_{TH0} is the value of the threshold voltage V_{TH} when the body-to-source voltage is zero. It can be seen that $|V_{TH}|$ increases with the increase of V_{BS}. The operation of body-driven devices is based on the body effect, that is the dependence of V_{TH} on V_{BS}. By modulating the body terminal voltage V_B, the conduction state of the transistor can be effectively controlled. A lower threshold voltage implies that the transistor can enter the conduction state more easily under the same gate-source voltage V_{GS}, thereby increasing the drain current I_D. The I_D varies with V_{BS}, thus achieving the transconductance function between the body voltage and drain current. Related work has demonstrated that the reduction of $|V_{TH}|$ results in an increase of the effective G_m values of the differential pair [25].

The resistor R is realized through the source degradation resistor and the circuit is shown in Fig. 4(a). The substrate of the source degenerate transistor is biased to VDD, which allows the body effect to be utilized to produce an equivalent bias offset voltage to extend the linear input range of the amplifiers M_a and M_b [15]. Additionally, to avoid current mirrors that simply replicate the operating current to the output, series-parallel current mirrors are used to further reduce the G_m value of the transconductor. Series-parallel current mirrors permit the diversion of the current by a large attenuation factor without degrading noise and matching performance [14]. The circuit is shown in Fig. 4(b). The transistors designated as M_{r1} to M_{rN} are reference transistors, and M_{c1} to M_{cN} are replica transistors. If the body of an NMOS transistor is connected to GND, a potential difference could be established between the substrate and the source terminals. This body effect causes the threshold voltage V_{TH} to increase, leading to inconsistent conductivity of replica transistors with the same gate voltage. For low-G_m transconductor circuits, the body effect has the potential to significantly decrease the accuracy of the current mirror due to a mismatch in the characteristics of the transistors. Therefore, the body of the NMOS transistor in the series-parallel current mirror is connected to the source terminals to eliminate the body effects. This provides a stable threshold voltage to ensure that the current I_{in} is accurately diversion. By arranging N NMOS transistor units with deep N-well structures in series and parallel configuration, an effective ultra-low G_m is achieved, as expressed G_m=g_{m1}/N^2. where g_{m1} represents the transconductance of transistor M_{r1}, and N^2 is the transconductance attenuation factor. The current mirrors are not only area-

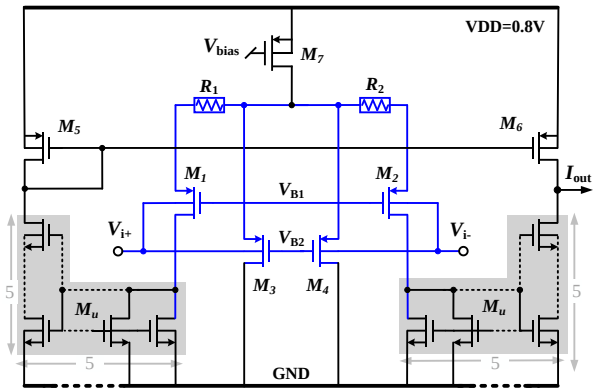

Fig. 5. The proposed tunable low-G_m transconductor circuit.

efficient because their area is proportional to the square root of the copy factor, but also match-efficient because they benefit from the layout matching of the common centroid geometry and the same surroundings.

III. Proposed Low-G_M Transconductor Based on Bootstrap-Body-Input

Due to the input core of the transconductor in [24] only consists of a source follower, its minimum G_m value is limited by the output resistance of the biased current source. To address this issue, this work employs a differential pair based on a single current source. The proposed transconductor, shown in Fig. 5, operates under a 0.8 V supply and consists of a bias current source, a differential G_m-reduction block, and series-parallel current mirrors. The G_m-reduction block is implemented by the body-input PMOS transistors M_1 to M_4. Among these transistors, the bodies of M_1 and M_3 are connected to the positive input terminal V_{i+}, and the bodies of M_2 and M_4 are connected to the negative input terminal V_{i-}. The source terminals of M_1 and M_3, as well as those of M_2 and M_4, are connected to source degeneration resistors R_1 and R_2 respectively. The voltages V_{B1} and V_{B2} are set such that M_1 and M_3, along with M_2 and M_4, exhibit similar gains. Analysis of the small-signal model of the forward input stage of the transconductor reveals that the small-signal current i_R through resistor R can be expressed as (6).

$$i_R = \frac{(g_{m1}g_{mb3} - g_{mb1}g_{m3}) \cdot V_{in}}{(g_{m1} + g_{mb1} + g_{m3} + g_{mb3}) + R(g_{mb3} + g_{m3})(g_{mb1} + g_{m1})} \quad (6)$$

where r_b is the output resistance of the bias current source. Assuming r_bR>>1 and g_mr_b>>1, the circuit transconductance G_m can be approximated as (7).

$$G_m \approx \frac{g_{m1}g_{mb3} - g_{m3}g_{mb1}}{g_{m1} + g_{m3} + R \cdot g_{m1} \cdot g_{m3}} \quad (7)$$

The effective transconductance of the input differential pair is reduced owing to the source degeneration effect. Ideally, the voltage values across the source degeneration resistors R are equal, $A_{M1} = A_{M3}$, $A_{M2} = A_{M4}$, and the G_m values equals zero. However, since the actual gain is determined by mismatches, it is impossible to achieve infinitesimally small currents flowing through R in practice. The current flowing through R_1 and R_2 is usually a few pA. From the differential input characteristics, it can be seen that the equivalent G_m of the transconductor

TABLE I
Bias Current and Transistor W/L in Transconductor Circuits

Transistor	M_1–M_4	M_5, M_6	M_7	M_u	I_{bias}
W/L (μm/μm)	4×1/1	2×1/1	4/8	1/5	1 nA

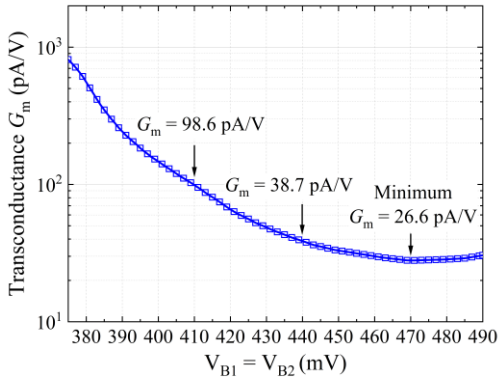

Fig. 6. The simulation results of the relationship between the transconductor's G_m values and the control voltage $V_{B1} = V_{B2}$.

constructed with transistors M_1 to M_4 is twice that presented in Equation (7). The proposed transconductor achieves a gain of more than 31.7 dB, and the dimensions of its transistors are shown in Table I.

To verify the programmable function in the proposed bootstrap-body-input technique, Fig. 6 presents the simulation results of the relationship between the transconductor's G_m values and the control voltage V_{B1} and V_{B2}. The V_{B1} is set equal to V_{B2} to ensure a similar voltage across the source degradation resistor with a minimal current flow. The proposed transconductor achieves a G_m of 98.6 pA/V at a control voltage of 410 mV. As the gate voltage increases, the channel of the PMOS transistor in the differential G_m-reduction block decreases, resulting in a reduction in current. As a result, the G_m value continuously decreases. The minimum G_m value of 26.6 pA/V is achieved when $V_{B1} = V_{B2} = 470$ mV. Thereafter, the channel becomes pinched-off with the increase in voltage, and the low transconductor begins to fail.

Monte Carlo analysis was conducted to deeply assess the potential mismatch of the transconductor. Fig. 7 presents the 200 Monte Carlo results for four different bias voltages. When the bias is set to $V_{B1} = V_{B2} = 470$ mV, the standard deviation of the best average G_m value is only 0.67 pA/V. At 440 mV, the standard deviation changes little, as the channel current is still small (tens of pA). As the bias voltage decreases, the G_m value and current deviation gradually increase. At a bias voltage of 410 mV, the standard deviation increases by 0.34 pA/V compared to the standard deviation at the optimal G_m value. When $V_{B1} = V_{B2} = 390$ mV, the standard deviation reaches 1.22 pA/V. Clearly, the mismatch of the transconductor increases significantly as the gate voltage decreases. This is primarily due to the current deviation of the input-stage PMOS transistors, which is influenced by the high current in the channel.

Using the body terminal of a PMOS transistor as a signal input still allows for control of its quiescent current with the remaining gate terminal. Voltage V_{B1} and V_{B2} effectively regulate the operating state of the transconductor to achieve

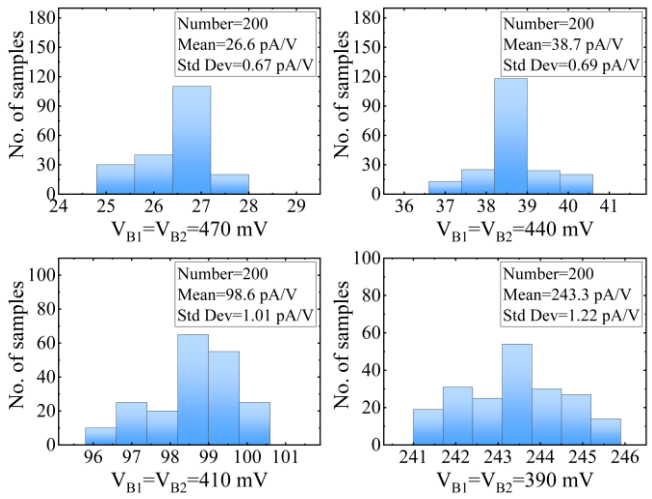

Fig. 7. Monte Carlo analysis of the transconductor at four bias voltages considering PVT variations (V_{B1} =V_{B2} = 470 / 440 / 410 / 390 mV).

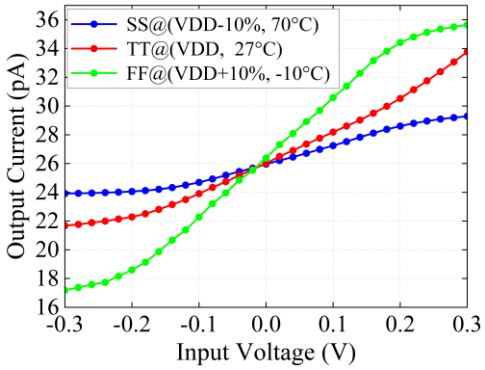

Fig. 8. The post-layout simulation results of the output current of the proposed transconductor at V_{B1} = V_{B2} = 470 mV in the worst case.

programmable G_m values. In other words, the two control voltages allow the transconductor to modulate each other's mismatch due to the process, voltage, and temperature (PVT) variations. Additionally, the sensitivity of the area-advantaged MOS transistor-based source degradation resistor to PVT is suppressed. Both the source degeneration transistor and the input pair are designed with identical dimensions and biased in the deep subthreshold region. The output current of the differential G_m-reduction block is replicated to the output branch through series-parallel current mirrors, which form the single-end output of the transconductor. These current mirrors have the same gain, and a large attenuation factor allows for a low G_m value. The proposed transconductance amplifier's current mirror comprises five parallel transistors and five series transistors, which replicate the current of the G_m-reduction block with an attenuation factor of 25. In fact, it is possible to achieve lower transconductance values by employing a higher attenuation factor [15].

To analyze the robustness of the proposed transconductor against PVT variations, Fig. 8 illustrates the post-layout simulation results of the output current for the proposed transconductor. Under the typical-typical (TT) process corner, a G_m value of 26.1 pA/V is obtained with a linear input range exceeding 0.3 V, while the input pair transistors' gate terminals

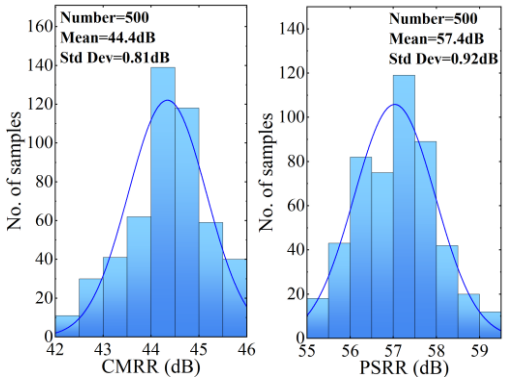

Fig. 9. Results of 500 Monte Carlo analysis for CMRR and PSRR.

TABLE II
PERFORMANCE SUMMARY OF THE POST-LAYOUT SIMULATION RESULTS OF THE PROPOSED TRANSCONDUCTOR

Parameter	Typical	Process		Voltage (V)		Temperature	
		FF	SS	0.72	0.88	-10°C	70°C
I_D (nA)	1.1	1.25	0.98	1.17	1.11	1.06	1.19
Power (nW)	0.88	1	0.78	0.84	0.98	0.85	0.95
G_m (pA/V)	26.1	39.4	16.9	28.5	27.7	27.4	24.8
Linear Input Range (V)	0.3	0.32	0.24	0.28	0.34	0.29	0.31
CMRR (dB)	44.4	45.9	41.2	45.4	42.2	44.2	46.6
PSRR (dB)	57.4	59.9	51.0	47.1	59.2	56.2	57.5
IRN@100 Hz (μV/√Hz)	24.2	25.7	30.1	24.0	28.5	24.1	33.4

V_{B1} and V_{B2} are both biased at 470 mV. Based on this bias voltage, the proposed transconductor is operated under extreme conditions for the high-temperature slow-slow (SS) process corner and the low-temperature fast-fast (FF) process corner. The results demonstrate that despite the transconductor's G_m value and linear range are slightly change, the output current remains at the pA level. Table II summarizes the performance metrics of the proposed bootstrap-body-input transconductor under PVT variations obtained from the post-layout simulations. The higher supply voltage promotes the conduction of the input pair transistors in the G_m-reduction block, resulting in an increased output current of the transconductor under the FF corner. Nevertheless, the proposed transconductor allows for the restoration of the desired operating current by tuning the gate terminals V_{B1} and V_{B2}.

Fig. 9 presents the results of 500 Monte Carlo simulations for the common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR). Benefiting from the design of the core circuit and the optimization of the centroid layout (particularly, the transistors $M_{1\sim4}$ are symmetrically drawn to increase the matching of the input stage), the transconductor achieves an average CMRR and PSRR of 44.4 and 57.4 dB, respectively.

IV. MEASUREMENT RESULTS

Both the conventional body-input transconductor in Fig. 2 and the proposed transconductor in Fig. 5 are designed and fabricated using a 0.18 μm CMOS process, and the chip micro-

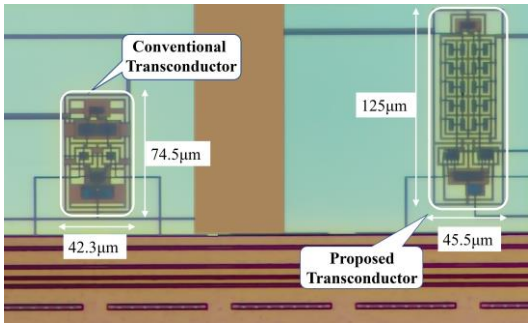

Fig. 10. Micrographs of chips with conventional transconductor and proposed transconductor.

graph is shown in Fig. 10. Despite the utilization of dummy transistors, the proposed bootstrap-body-input transconductor occupies a chip area of merely 0.0057 mm², which is approximately half the area consumption compared to state-of-the-art bootstrapped pseudo-differential OTAs [24].

Fig. 11 shows the measurement setup for the transconductor. The input of the transconductor is connected to an active balun formed by two auxiliary OTAs to achieve a fully differential input signal. A high-precision transimpedance amplifier (TIA) is connected to the output of the transconductor to measure the G_m value. This TIA converts the output current I_{out} to the output voltage V_{out}, facilitating precise measurement of the current variation. The measurement method for the transconductance involves applying a 100 Hz triangular wave from 0 to VDD at the input and using an oscilloscope to obtain the derivative of the output voltage relative to the input voltage [26]. Therefore, the G_m value is expressed as (8).

$$G_m = \frac{dV_{out}}{R_F \cdot dV_{id}} \tag{8}$$

where R_F is the feedback resistor in the TIA and V_{id} is the input voltage. The G_m measurement results as a function of the differential input voltage is shown in Fig. 12. The G_m value of conventional transconductor decreases with increasing bias voltage V_B. This indicates that body driving can adjust the G_m value of the transconductor via the gate terminal. The minimum G_m value achieved by a conventional body-input transconductor is approximately 34 nA/V (V_B=480 mV), whereas the proposed transconductor consistently achieves G_m values below 27 pA/V with five samples. Compared to traditional body-input transconductor, the proposed transconductor exhibits an enhancement in transconductance performance by over 1200 times. The measurement results reveal that the bootstrap-body-input technique allows the transconductor to generate small currents to achieve extremely low G_m value.

The G_m value of the bootstrap-body-input transconductor at different bias voltages is shown in Fig. 13. The proposed transconductor achieves a maximum G_m of about 581 pA/V at V_{B1} = 380 mV and V_{B2} = 375 mV. When V_{B1} = 465 mV and V_{B2} = 465 mV, the G_m value of the transconductor is reduced to 30 pA/V. The transconductor provides a G_m value tuning range from 27 pA/V to 581 pA/V and consumes 0.88 nW. The linear input range of the transconductor exceeds 300 mV and remains stable over a large bias voltage range.

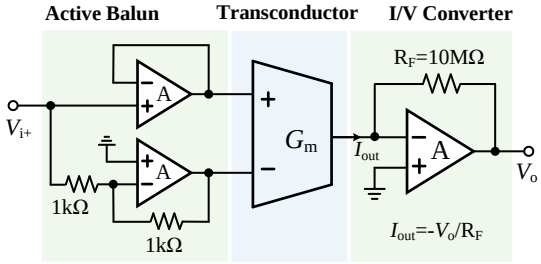

Fig. 11. Measurement setup of the DC transfer characteristics of the transconductor.

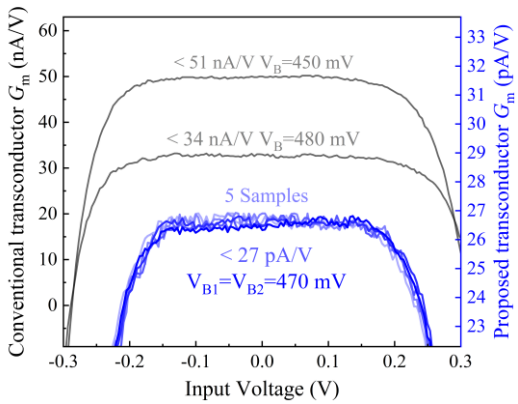

Fig. 12. Measured transconductance as a function of differential input voltage. The conventional transconductor exhibits a minimum G_m value of approximately 34 nA/V, whereas the proposed transconductor achieves around 27 pA/V across five samples. This is a 1200-fold improvement over the conventional transconductor.

It is noteworthy that the two control voltages are not always identical. The mismatch of the branch is compensated by tuning V_{B2} to achieve the optimal G_m value. As mentioned in the Monte Carlo analysis in Section III, the G_m value experiences mismatch due to the reduction of the gate voltage. This mismatch is observed in practice as an adjustment of the bias voltage. To further investigate the mismatch behavior of the proposed transconductor, tuning tests were conducted to observe the trend of changes in G_m. The results of the tuning characteristics for four different bias voltage settings of the transconductor are shown in Fig. 14. It is evident that at higher gate voltages (V_{B1}=440, 465 mV), the transconductor accurately achieves the expected G_m value when V_{B1} = V_{B2}. This is because the drain current of the input transistor pair is insensitive to the small difference in V_{TH} and the current levels are closely matched. However, as the gate voltage decreases (V_{B1}= 380, 410 mV), this small difference is amplified exponentially, and the absolute deviation increases significantly due to the larger current, causing a noticeable current mismatch between the two transistors. When V_{B2} is set equal to V_{B1}, the channel current through M_3 and M_4 exceeds that of M_1 and M_2, leading to a G_m value that exceeds the expected range. By properly lowering V_{B2}, the optimal G_m value can be achieved. With excessive reduction of V_{B2}, the voltage difference across the resistors in the transconductor increases again, resulting in accelerated degradation of the G_m value. The measurement results indicate that the tuning of the proposed transconductor with respect to the bias voltage exhibits a non-monotonic behavior. Fortunately, at lower gate voltages, the G_m value

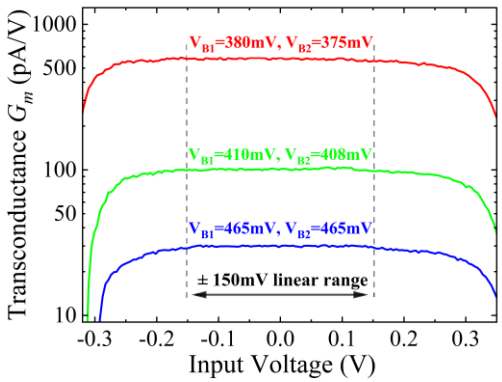

Fig. 13. Measurement results of the tunable characteristics for the proposed transconductor. The control voltage is provided by a verified off-chip source. The G_m values from high to low are about 581 pA/V, 99 pA/V, and 30 pA/V, respectively.

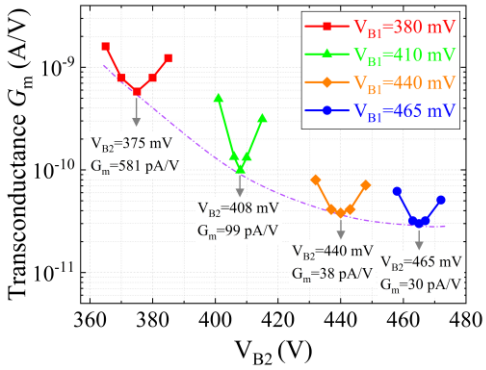

Fig. 14. Measurement results of the tuning characteristics of the transconductor. Tuning V_{B1} to cope with the mismatch results in optimal G_m values at specific V_{B2}, and the trend of these optimal values is consistent with the simulation analysis.

remains at an excellent level, although the mismatch may cause the G_m to exceed the expected value. The proposed transconductor demonstrates excellent adjustment capability in compensating for gain mismatches caused by process variations, voltage changes, and temperature drifts.

Thanks to the careful design of the layout, as shown in Fig. 15, the proposed transconductor achieves a CMRR greater than 44 dB and a PSRR greater than 56 dB. Fig. 16 illustrates the total harmonic distortion (THD) measurement results for the proposed transconductor. At V_{B1} =V_{B2} = 470 mV, THD is -42 dB for a 300 mV_{pp} sinusoidal input signal at 100 Hz. THD improves to -48.8 dB when the input voltage drops to 150 mV_{pp}. In particular, the proposed transconductor achieves the best THD at 100 mV_{pp} sinusoidal input when V_{B1} = 461 mV, V_{B2} = 460 mV, and the distortion of the signal is reduced to 0.35 %. It is possible to achieve an even lower THD by replacing the simple current mirrors in the topology with cascade configurations.

Table III compares the proposed transconductor with state-of-the-art designs in the literature. While some previous work [27], [19] achieved higher input range, this usually occurred at the cost of high supply voltages and high-power consumption. Low noise contribution was demonstrated in [26], [28], and [29], but these are simulation results, and achieving extremely low G_m values was challenging using only body-driven technique. Despite the fact that both the transconductor in [24] and the

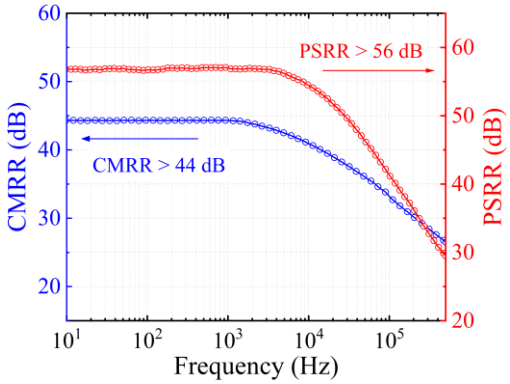

Fig. 15. Measurement results of the CMRR and PSRR.

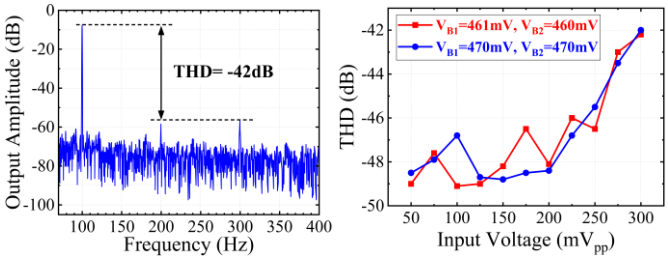

Fig. 16. (a) Measured THD of the proposed transconductor for a 300 mV_{pp} input at 100 Hz. (b) Measured results of THD versus input voltage at different bias voltages.

proposed design employ bootstrapping techniques, the latter exhibits significantly lower G_m values and power consumption. This improvement is attributed to the optimization of the core circuitry, the implementation of series-parallel current mirrors, and the utilization of the body-input technique. In summary, the proposed transconductor realizes tunable low G_m with a small area and low power, and achieves a good balance between linearity, input range and noise. This is particularly appealing for bioelectric signal acquisition systems with limited size and power resources.

V. Conclusion

In this paper, a low power, low G_m transconductor with bootstrap-body-input topology is proposed for biomedical sensors. The bootstrapping technique based on sub-threshold operation and a series-parallel current mirror technique with a 25-fold attenuation factor combine to achieve extremely low and tunable G_m values. The source degeneration resistor further extends the linear input range of the transconductor with the benefit of the body effect. The proposed transconductor is fabricated using a 0.18 μm CMOS process, which only consumes 0.0057 mm^2 chip area and 0.88 nW total power. The proposed transconductor achieves more than 1200 times lower G_m values compared to conventional body-input transconductors. The measurements showed that the transconductor's G_m value is tunable within a range of a few hundred pA/V. The minimum achievable G_m is below 27 pA/V and the linear input range exceeds 300 mV. THD is -42 dB at 300 mV_{pp}@100 Hz sinusoidal input signal. In practical scenarios, programmable voltages can be employed to adjust the required G_m values, facilitating adaptability to various small-size and low-power sensor applications.

TABLE III
PERFORMANCE AND COMPARISON OF THE PROPOSED LOW-G_M TRANSCONDUCTORS

Parameter	[27]2019	[19]2020	[21]2020	[24]2022	[26]2022	[28]2022	[29]2023*	This Work
Process (µm)	0.18	0.18	0.13	0.18	0.18	0.13	0.18	**0.18**
Supply (V)	1.8	1	±0.2	1.8	0.5	0.3	0.6	**0.8**
Power (µW)	5.4	0.27	0.36	4	0.0247	0.7	0.462	**0.00088**
BW (Hz)	5.2 k	100	1.1 M	15 k	224.5	N/A	95.5 k	**1.7 k**
Area (mm^2)	0.014	0.027	0.0264	0.0099	0.011	0.00094	0.0037	**0.0057**
Minimum G_m (nA/V)	0.5	0.62	760	15	24.5	1410	1800	**0.027**
Linear Input Range (V)	0.43	2	0.2	0.28	63.4 dB	rail-to-rail	±0.6	**0.3**
CMRR (dB)	N/A	56	70 *	N/A	84	63	73	**44**
PSRR (dB)	N/A	47	52 *	N/A	52	46	42	**56**
Input-referred Noise	1.63 μV_{rms} * (0.06–5 Hz)	760 μV_{rms} * (1–100 Hz)	0.99 µV/√Hz *	70.3 µV/√Hz @100 Hz	5.32 µV/√Hz * @1k Hz	0.72 µV/√Hz * @1k Hz	0.1 µV/√Hz @10 Hz	**25.4 µV/√Hz @100 Hz**
THD (dB) (V_{pp}@Hz)	-40 0.16@5	-42 1@1k	-41.61 0.3@10k	-40 0.35@1k	-51 @0.5 V	-54 @0.1 V	-40 @0.18 V	**-42 0.3@100**
Technique	Current Attenuation	Bulk-driven	Gate-driven	Bootstrapping	Multiple-input Bulk-driven	Bulk-driven non-tailed OTA	Bootstrapped bulk-driven	**Bootstrap-body-input**

* Simulation results

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