A 1-V Wide Swing Image Sensor With Simultaneous Energy Harvesting and Imaging Modes for IoT Applications

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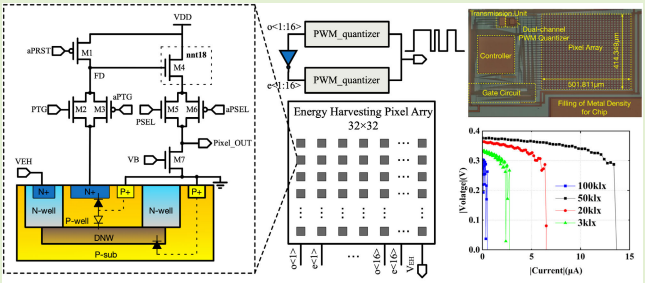
***Abstract*—Image sensors with energy-harvesting capabilities aid in the development of self-powered Internet of Things (IoT) nodes. By achieving simultaneous energy harvesting and imaging, these image sensors make it possible to eliminate batteries and directly achieve self-powered operation. The article proposes a 1-V wide swing image sensor with simultaneous energy harvesting and imaging modes. The proposed pixel utilizes a vertical n+/p-well/DNW/P-sub structures as the photodiode based on a standard 180-nm CMOS mixed-signal process. The n+/p-well is used for imaging, while the p-well/DNW and DNW/P-sub are used for energy harvesting with p-well and P-sub shorted together. Moreover, a traditional 4T pixel has been improved by using CMOS pairs as the switches and zero-threshold NMOS as the source follower. The rail-to-rail pixel output swing can be achieved. An image sensor with simultaneous energy harvesting and imaging modes, which consists of a 32 × 32 pixel array, a controller, and a dual-channel PWM quantizer, has been designed and fabricated. Measurement results show that the average power consumption of the image sensor is approximately 899.6 nW with 25 fps at 3 klx. The proposed image sensor has a DR of 47.3 dB under a 1-V supply. The measured power generated by energy harvesting while maintaining imaging functionality is 194 pW/lx/mm^2.**



***Index Terms*— CMOS image sensor (CIS), dynamic range (DR), energy-harvesting imager (EHI), simultaneous imaging and energy harvesting.**

I. Introduction

IN THE Internet of Things (IoT), image sensors and their networks are essential for the acquisition, processing, and transmission of visual data. These sensors empower IoT nodes with visual capabilities, enabling tasks such as facial recognition, scene understanding, and real-time monitoring [1], [2]. As the number of IoT devices continues to rise, the design of low-power image sensors becomes increasingly critical. Low-power sensors can extend the battery life of devices and reduce energy consumption, which in turn lowers maintenance costs and enhances the overall efficiency of systems [3], [4]. In fields such as environmental monitoring, health surveillance, and urban infrastructure management, efficient energy use not only improves device performance but also contributes to achieving sustainability goals. Consequently, the development of low-power image sensors is vital for the widespread application of IoT technology.

Energy harvesting plays a crucial role in the implementation of low-power image sensors. By effectively harnessing ambient energy, these sensors can reduce their dependence on external power sources, thereby extending device lifespan and enhancing flexibility across various applications. In recent years, several studies have focused on developing image sensors with energy-harvesting capabilities. However, many energy-harvesting image sensors are unable to operate in both energy-harvesting and imaging modes simultaneously, which limits their energy utilization efficiency. For instance, the works cited in [5], [6], [7], and [8] indicate that most energy-harvesting imagers (EHIs) employ a time-division mode, alternating between imaging and energy-harvesting

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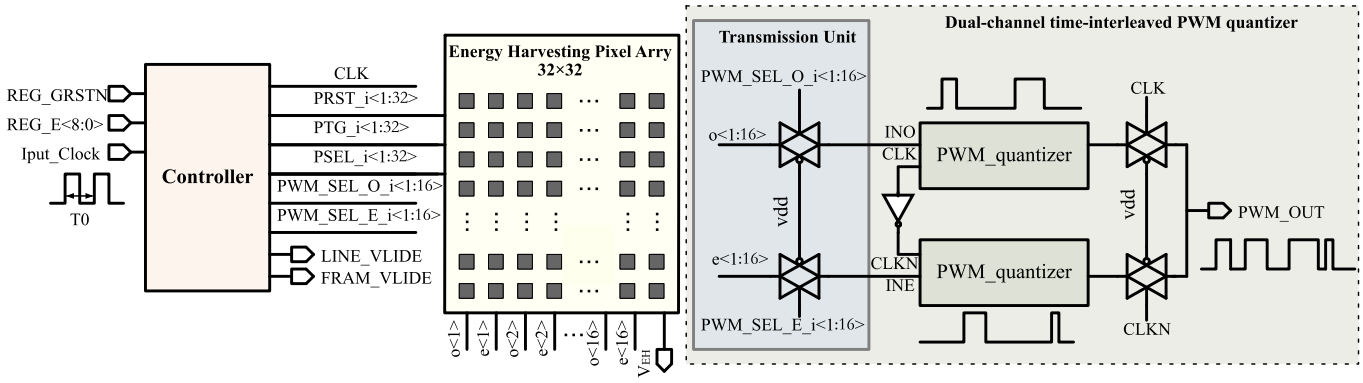


Fig. 1. System architecture of the proposed image sensor with simultaneous energy harvesting and imaging modes.

modes. This switching reduces the time available for energy collection and consequently impacts overall device performance. Some research efforts have sought to address this limitation. Fish proposed a method to enable simultaneous energy harvesting and imaging by incorporating a p-n junction alongside the imaging diodes [9], [10]. However, this approach inevitably reduces the pixel fill factor and decreases the utilization rate of the pixel area, subsequently affecting imaging quality and efficiency. In addition, Park introduced a novel pixel structure capable of concurrent energy harvesting and imaging [11]. This structure utilizes the substrate as the output terminal for energy harvesting, which necessitates deep trench isolation for all NMOS (DNW NMOS) in the circuit system to isolate them from the substrate. While this design successfully addresses the challenge of simultaneous energy harvesting and imaging, it also introduces complexity and challenges in subsequent circuit design.

In the realm of low-power techniques for image sensors, reducing the supply voltage is a crucial method for decreasing power consumption. However, a reduction in supply voltage results in a significant decrease in pixel output voltage swing, which, in turn, diminishes the dynamic range (DR). The complementary pixel structure achieves a rail-to-rail pixel output swing [12], but this structure is complex and has a fill factor of only 40%. Many low-voltage image sensors employ pulsewidth modulation (PWM) digital pixels [13]. However, the PWM pixel structure reduces the fill factor due to the incorporation of in-pixel comparators, which also increases static power consumption.

This article proposes an image sensor capable of operating simultaneously in energy-harvesting and imaging modes while achieving a higher output swing with a supply voltage under 1 V. In comparison to the previous conference paper [14], this article presents measurement results from the testing of the fabricated chip. It also explores three aspects in greater depth. Specifically, this article enhances the discussion of the proposed pixel by providing a detailed explanation of its working principles, thereby facilitating a deeper understanding for readers. Building upon the theoretical analysis presented in the conference paper, a comparative analysis of recent articles is included. Furthermore, the energy-harvesting functionality of the pixel array is validated through tape-out testing, thereby bolstering the credibility of the proposed solution. In addition, based on the simulation validation of the dual-channel PWM quantization discussed in the conference paper, tape-out validation is performed. The article is organized as follows: Section II discusses the proposed image sensor circuit structure and operating principles, Section III presents the tape-out verification results, and Section IV concludes the article.

II. Proposed Image Sensor Design

A. Architecture of the Proposed Image Sensor

The proposed architecture of the image sensor system is depicted in Fig. 1. It consists of a controller, a 32 × 32 energy-harvesting pixel array, and a dual-channel PWM quantizer. These pixels can operate concurrently in both imaging and energy-harvesting modes. While converting light intensity signals into voltage signals, the pixel array simultaneously performs energy harvesting. The output from the pixel array is divided into odd and even columns, with the signals from each column directed to the two-channel PWM quantizer. Under the control of the CLK clock signal, the two channels alternately process the pixel output signals, converting them into PWM-modulated signals. The pulsewidth of the PWM signals is proportional to the light intensity. Finally, the PWM signals are time-interleaved to produce the final output of the entire image sensor, controlled by transmission gates.

Fig. 2 illustrates the timing control diagram for the proposed image sensor. The system reset signal, REG_GRSTN, resets all registers when low and allows the controller to function normally when high. PRST_i[1:32] represents the row reset signals for the pixel array. For a 32 × 32 pixel array, 32-row reset signals are required, which can be generated by a decoder using the 6-bit binary input PRST_i[1:32]. PTG_i[1:32] are the row exposure control signals for the pixel array, with a minimum unit of 34 × T0. The exposure time is adjustable based on the control input REG_E[1:32], with a maximum duration of 1088 × T0. The rising edges of PTG_i[1:32] are synchronized with those of PRST_i[1:32]. PSEL_i[1:32] are the row output signals for the pixel array, with their rising edges aligned with the falling edges of PTG_i[1:32]. FRAME_VALID are frame synchronization signals, which

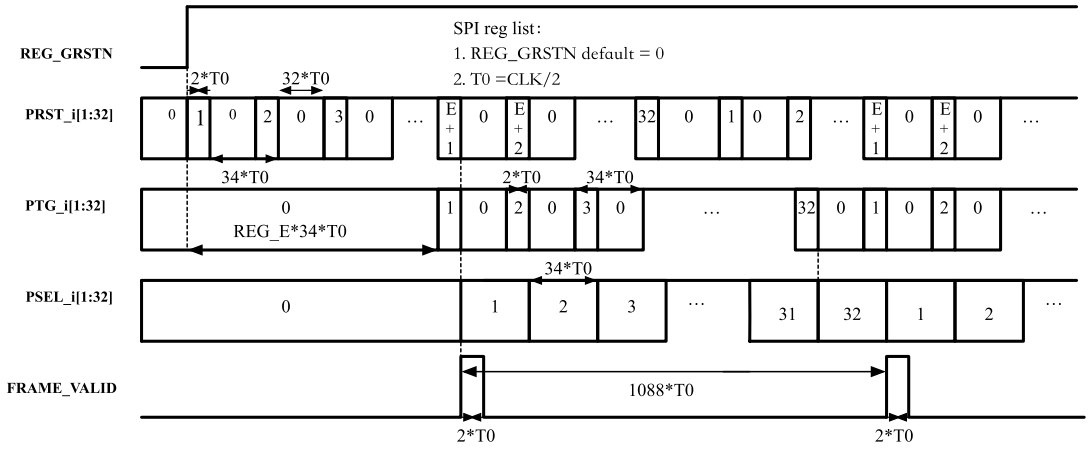


Fig. 2. Timing diagram of the controller.

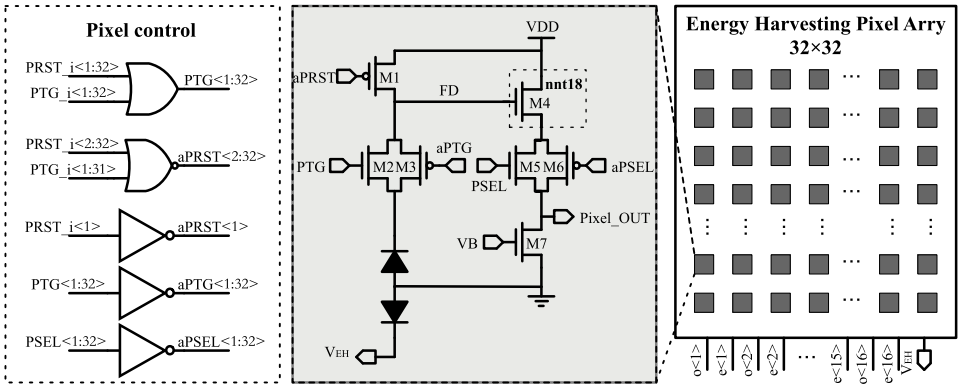


Fig. 3. Proposed pixel of the image sensors.

indicate the beginning of a frame signal with each arrival of a high level.

B. Proposed Pixel Circuit

In the present CMOS image sensor (CIS) technology, the four-transistor (4T) pixel structure is well-recognized for its high efficiency and low noise performance. However, during the low-voltage operations, its output voltage swing often fails to meet the required DR. Based on the traditional 4T pixel architecture, a new pixel circuit is proposed shown in Fig. 3. This advancement not only extends the output voltage swing but also integrates a novel photodiode design. As a result, it enables the pixel to collect energy more effectively during imaging tasks, thereby further reducing overall power consumption. Fig. 4 illustrates the control sequence of the proposed pixel, and the specific working principle is as follows.

1) *Reset Phase for PD:* During this phase, aPRST is low, and PTG/aPTG are high/low, respectively. Both the reset transistor (M1) and the transfer gate (M2/M3) are activated, resetting the voltages of the floating diffusion V_{FD} and the photodiode (V_{PD}) to predefined reference levels.
2) *Charge Accumulation Phase:* In this phase, the photodiode of the pixel captures light, converting it into an electrical charge. When PTG/aPTG are low/high, the transfer gate (M2/M3) is turned off, and the photodiode remains isolated from the rest of the circuit. V_{PD} gradually decreases, with the rate of reduction depending on the light intensity.
3) *Reset Phase for FD:* Before the charge transfer, aPRST is low, and the reset transistor (M1) resets the V_{FD} to a known reference level, preparing the FD to receive the charge from the photodiode.
4) *Charge Transfer Phase:* Once enough charge has been accumulated, PTG/aPTG are high/low, and M2/M3 is turned on. This action allows the charge to migrate from the photodiode to the FD.

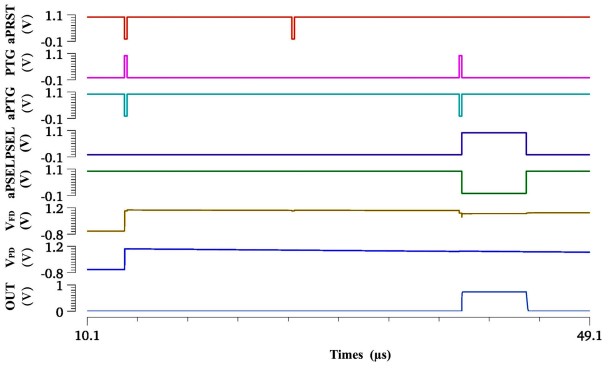


Fig. 4. Diagram displays the control timing for a single cycle of the proposed pixel, along with the voltage signals at critical nodes.

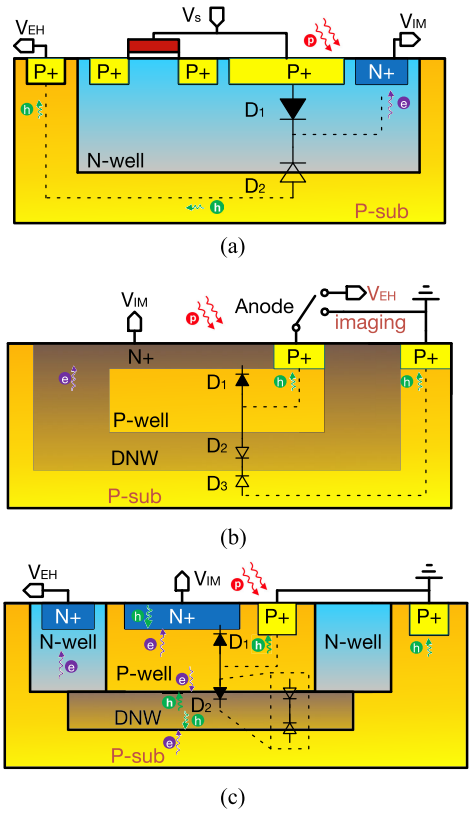


Fig. 5. (a) Pixel structure using a P-substrate as the energy-harvesting port. (b) Time-division multiplexed pixel structure requiring switching between energy-harvesting and imaging modes. (c) Proposed pixel structure for simultaneous imaging and energy harvesting. V_{IM} is the imaging signal terminal, and V_{EH} is the energy-harvesting output terminal.

5) *Readout Phase:* In this phase, the source follower (M4/M7) transistors function as a buffer, converting the charge in the FD into a voltage signal. This conversion process preserves the charge integrity, ensuring the accurate readout. Concurrently, PSEL/aPSEL are high/low, and the row select (M5/M6) transistors are engaged, enabling the readout of this pixel's signal onto the image sensor's output line (OUT), where the actual image data from the pixel is captured.
6) *Cycle Repeat:* After the readout, the pixel undergoes a reset, initiating a new cycle for the subsequent image capture.

C. Simultaneous Imaging and Energy-Harvesting Technologies

Fig. 5(a) illustrates a pixel structure utilizing a P-sub as the energy-harvesting output terminal [11]. This configuration employs P+/N-well (D1) and N-well/P-sub (D2) junctions to facilitate simultaneous imaging and energy harvesting. However, because the substrate functions as the energy-harvesting output terminal, traditional NMOS transistors with a grounded body cannot be integrated into the design, necessitating the use of DNW NMOS transistors. This requirement significantly increases the circuit area. In addition, the P-sub typically exhibits a low doping concentration, leading to high resistivity, which is detrimental to effective energy harvesting.

Fig. 5(b) presents an alternative time-division multiplexing pixel structure [7]. In this arrangement, three distinct diodes are connected in parallel: n+/p-well junction D1, p-well/Deep N-well junction D2, and Deep N-well/P-sub junction D3. These diodes share a common cathode. During imaging mode, the anodes of D1 and D2 are interconnected and grounded. In energy-harvesting mode, the anodes of D1 and D2 are connected to the energy-harvesting output terminal (V_{EH}). Due to the grounding of D3's anode, D3 cannot contribute to energy harvesting. Consequently, this structure cannot operate in both energy harvesting and imaging modes simultaneously; it can only alternate between the two modes. To achieve a self-powered image sensor, this configuration necessitates a supercapacitor for energy storage, which further increases the area required.

Fig. 5(c) illustrates the proposed photodiode structure designed for simultaneous imaging and energy harvesting. This structure employs photodiodes with a vertical n+/p-well/DNW/P-sub configuration, where the p-well and P-substrate are connected to the ground. In this arrangement, photodiode D1 is formed between the n+ and p-well for imaging applications, while photodiode D2, consisting of the p-well/DNW and DNW/P-sub, is designated for energy harvesting. When the parasitic capacitance of D1 is reset under the timing control of the pixel circuit, the voltage VD1 is reset to VDD. Exposure then commences as incident photons illuminate the photodiodes. The photons with the energy over the silicon's bandgap can be absorbed by electrons in the valence band, generating electron–hole pairs that are subsequently separated by the built-in electric field in the p-n junction. The electrons in the n+/p-well are driven toward the n+ region, while the holes are directed to the p-well, thereby forming the photocurrent of D1. As a result, VD1 gradually decreases. After the exposure, the signal value of D1 is transmitted to the pixel circuit via the V_{IM} terminal. For the D2, during the exposure, the electrons in the p-well/DNW and DNW/P-sub are collected by the NNW and go out through V_{EH}, while the holes go to the ground through p-well and P-sub. D2 operates independently of pixel timing control, allowing it to continuously function in the energy-harvesting mode. The relationship between the current and voltage of the illuminated photodiode is described by the following equation:

$$I = I_s\left(e^{\frac{qV}{kT}} - 1\right) - I_{\text{ph}} \tag{1}$$

where I is the total current (positive direction from the P region to the N region), I_s is the reverse saturation current of the diode (dark current), q is the electron charge (1.602×10^{-19} C), V is the voltage across the diode (the P region relative to the N region), k is the Boltzmann constant (1.381×10^{-23} J/K), T is the absolute temperature (in K), and I_{ph} is the photogenerated current, proportional to light intensity and can be expressed as

$$I_{\text{ph}} = k' I_{\text{opt}} \tag{2}$$

where k' is the proportionality coefficient and I_{opt} is the intensity of the incident light. After derivation, the open-circuit

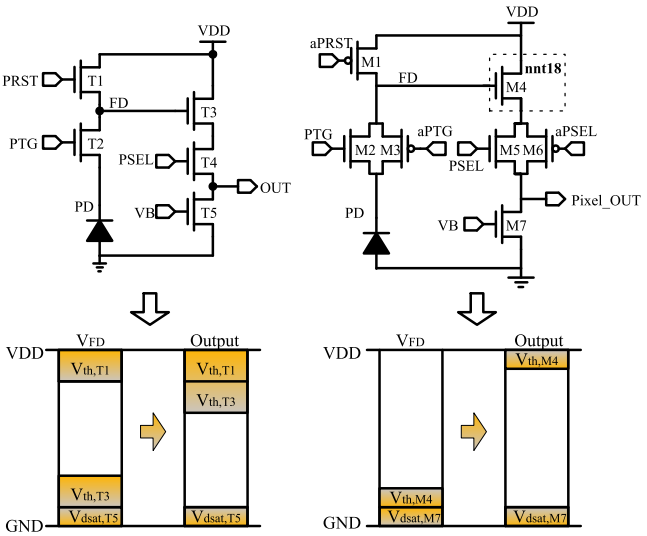


Fig. 6. Pixel circuits and output voltage swing. (a) Traditional 4T. (b) Proposed pixel.

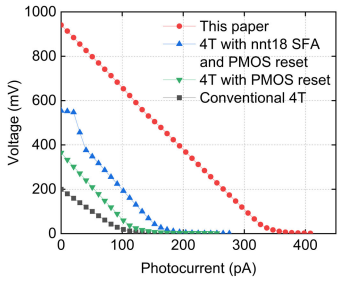


Fig. 7. Simulation results of the pixel output voltage swing for different pixel architectures.

voltage can be obtained as

$$V = \frac{kT}{q} \ln\left(\frac{k' I_{\text{opt}}}{I_s} + 1\right). \tag{3}$$

It can be seen that the open-circuit voltage is proportional to the logarithm of the light intensity.

D. Wide Output Swing Design for the Pixel

The pixel output range of image sensors is a crucial parameter that relates to the DR. The reduction in DR becomes particularly pronounced in low-voltage designs. Fig. 6(a) illustrates a typical 4T pixel and its output swing. The maximum voltage of V_{FD} is (VDD $-$ $V_{\text{th,T1}}$) due to the NMOS reset transistor, M1. To ensure that M3 and M5 both operate in the saturation region, the minimum voltage of V_{FD} is ($V_{\text{dsat,T5}} + V_{\text{th,T3}}$). Therefore, the effective voltage range of V_{FD} is [$V_{\text{dsat,T5}} + V_{\text{th,T3}}$, VDD $-$ $V_{\text{th,T1}}$]. After the source follower amplifier (SFA) M3, the output voltage swing range is [$V_{\text{dsat,T5}}$, VDD $-$ $V_{\text{th,T1}} - V_{\text{th,T3}}$].

To enhance the output swing, the proposed pixel structure replaces the original NMOS with a PMOS for M1, allowing V_{FD} voltage to reach up to VDD. The original single-transistor T2 is substituted with a complementary transmission gate M2/M3, which demonstrates an almost negligible voltage drop when in the "on" state. The source follower utilizes an nnt18 transistor for M4, effectively reducing its threshold voltage within 100 mV. This adjustment means that the maximum voltage of the M4 source voltage is (VDD $-$ 100 mV). In the traditional 4T pixel, the single transistor T4 can transmit a maximum voltage of (VDD $-$ $V_{\text{th,T4}}$), which is less than (VDD $-$ 100 mV). Therefore, this single-tube configuration does not meet the transmission requirements of the proposed pixel. By implementing M5/M6 in the place of the original single transistor T4, this issue can be resolved. As a result, these modifications contribute to an increased output swing range, as depicted in Fig. 6(b).

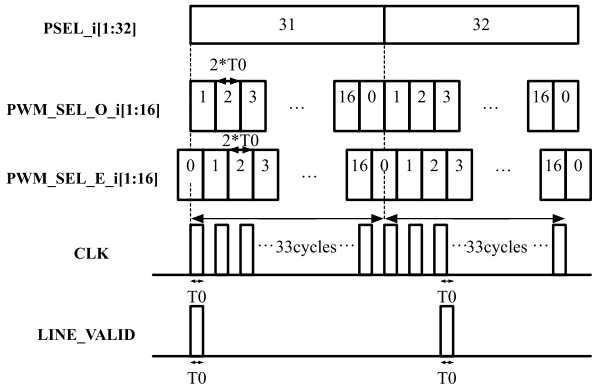


Fig. 8. Timing diagram of the dual-channel time-interleaved PWM quantizer.

The output swing simulation results for the traditional 4T pixel, 4T (PMOS reset), 4T (nnt18 SFA and PMOS reset), and the proposed pixel under a 1-V supply voltage are presented in Fig. 7. The black curve with square markers illustrates the output voltage swing of the conventional 4T pixel, which reaches a maximum output voltage of only 200 mV. In contrast, the red curve with circle markers represents the output voltage swing of the proposed wide swing pixel, achieving a maximum output voltage of 940 mV. Consequently, the DR of the proposed pixel is enhanced by 13.4 dB compared to the conventional 4T pixel.

E. Dual-Channel Time-Interleaved PWM Quantizer

Time-interleaving technology enhances sampling rates and bandwidth by enabling the parallel operation of multiple channels. This approach improves data-processing speed and efficiency, making it particularly suitable for high-performance applications. The design incorporates a dual-channel time-interleaved PWM quantizer, which increases data sampling rates and processing speeds through the use of two parallel channels. These channels alternately process data during the high and low phases of the clock, subsequently interleaving the output signals to achieve a higher overall sampling rate and speed. In contrast to traditional single-slope ADCs, this design directly outputs PWM image signals, leading to reduced power consumption.

Fig. 8 illustrates the control timing of the dual-channel PWM time-interleaved controller. The signals PWM_SEL_O_i[1:16] and PWM_SEL_E_i[1:16] manage the transmission of pixel array signals, directing odd and even column signals to the PWM quantizer, respectively.

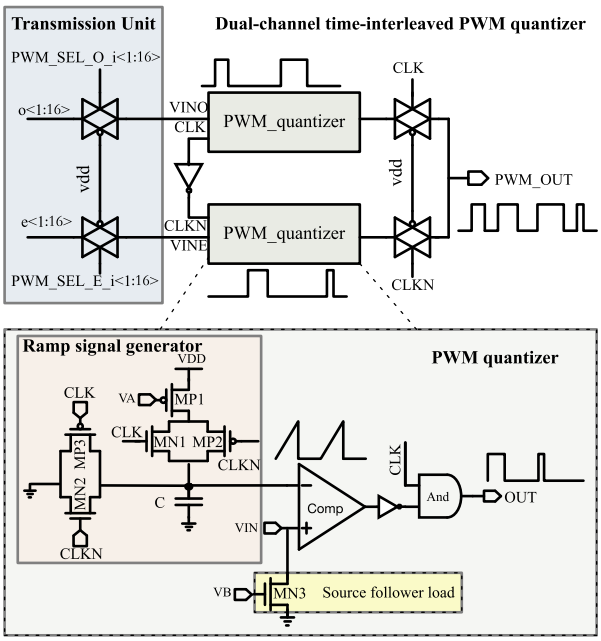


Fig. 9. Schematic of the dual-channel time-interleaved PWM quantizer.

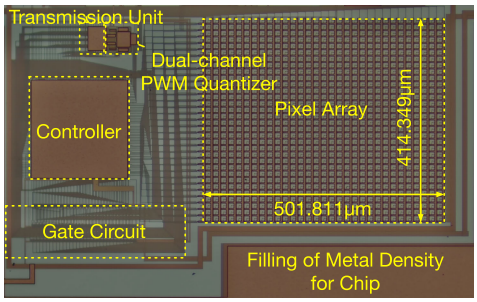


Fig. 10. Schematic of the dual-channel time-interleaved PWM quantizer.

CLK serves as the control clock for the PWM quantizer and is active only during the high levels of PSEL_i[1:32]. LINE_VALID is the line synchronization signal that indicates the commencement of a row data readout when it is high.

The circuit diagram of the PWM quantizer is depicted in Fig. 9. Transistors MN1–MN2 and MP1–MP3, along with capacitor C, form a ramp signal generator. MN3 serves as the load current source for the pixel source follower. When the CLK is in the low state, transistors MN1 and MP2 are deactivated, while MN2 and MP3 are activated, resulting in the capacitor voltage dropping to 0 V, which keeps the comparator output high. Conversely, when CLK is high, MN1 and MP2 are activated, and MN2 and MP3 are deactivated. Consequently, M1 charges capacitor C, generating a ramp signal. This ramp signal is then compared against the pixel array output voltage connected to VIN. When the ramp signal exceeds VIN, the comparator's output transitions to low. This output is inverted to create a high-level pulsewidth signal, which is subsequently processed through an AND operation with the CLK to yield the final output of the PWM quantizer.

III. Experimental Results and Discussion

The proposed image sensor was fabricated using a standard 180-nm CMOS process, with each pixel occupying an area

Fig. 11. Experimental setup and measurement results for testing the proposed image sensor.

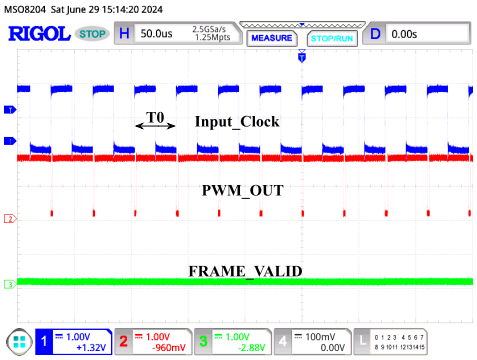


Fig. 12. Proposed image sensor output with 25 fps under 3 klx illumination.

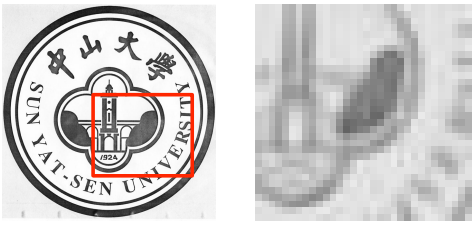
of 12.959 × 15.682 μm and a fill factor of 49.2%. Fig. 10 presents a microscopic photograph of the chip. To minimize the interference of illumination on the transistors, top metal layers are strategically utilized to cover all the transistors. This design choice ensures that the electrical characteristics of the transistors remain stable and unaffected by external light sources.

Fig. 11 illustrates the measurement environment for the chip. A Keysight B2910BL source meter provides a stable supply voltage of 1 V, while a Rigol DP831 voltage supply delivers multiple bias voltages to the image sensor chip. These bias settings facilitate the subthreshold operation of the tail current transistors, thereby significantly reducing power consumption. The signal timing is controlled using a Tektronix AFG31000 series signal generator, with the input clock period T0 set to 36.7 μs. Based on the FRAME_VALID timing in the diagram presented in Fig. 2, the duration of one frame is calculated as 1088 T0, resulting in a frame rate of 25 fps. Illumination is provided by a Princess PL-X500D xenon lamp, which is measured using a Delixi DLY-1801C lx meter. Signal observation and recording are conducted with a RIGOL8204 oscilloscope. In addition, a Keithley DMM6500 multimeter is employed to assess the open-circuit voltage (V_{EH}) of the energy harvesting output terminal, which is recorded at −289.3 mV.

Under a lighting condition of 3 klx, the PWM output of the image sensor reaches its maximum value of 36.7 μs T0, as illustrated in Fig. 12. Consequently, the maximum detectable signal is defined as T0, and the sensitivity is calculated to be 12.23 ns/lx. The image sensor output (red

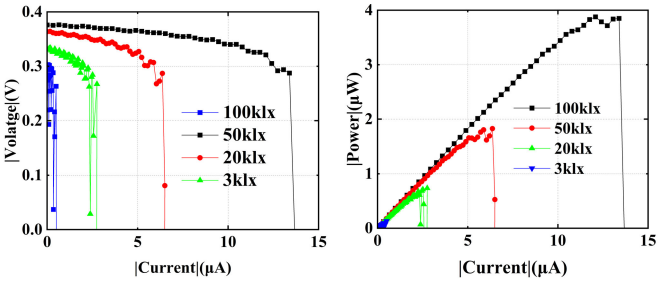
TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER WORKS

Reference	Gomez-Merchan 2023 [7]	Nazhamaiti 2021 [8]	Park 2018 [11]	Wu 2022 [25]	Shah 2019 [26]	This work
Process (μm)	0.18	0.18	0.18	0.18	0.13	**0.18**
Pixel complexity	54T	5T	3T	4T	4T	**6T**
Pixel size (μm^2)	–	21×18.75	5×5	–	–	**12.959×15.682**
Pixel array	128×128	32×32	100×90	128×128	320×240	**32×32**
Fill factor (%)	30.65	–	94	27	60.4	**49.2**
Supply Voltage	0.7V	1.8V	0.6V	1.2V	1.8V	**1V**
Sensitivity	–	–	–	–	–	**12.23ns/lx**
Frame Rate (fps)	51.5	1894	15	15	–	**25**
Readout Noise	5.34%	–	3.80%	0.80%	–	**0.43%**
Power Consumption	1.14μW	16.43μW	10.08μW	17.4μW	–	**899.6nW**
FoM [pJ/(pixel·frame)]	3.496	135.5	4.98	11.4	–	**35.1**
Dynamic Range (dB)	100	–	–	–	42.3	**47.3**
Simultaneous EH & Imaging	No	No	Yes	Yes	No	**Yes**
P. generation (pW/lx/mm^2)	–	31.25	998	267	940	**194**



(a) (b)

Fig. 13. (a) Image from the scanner. (b) Image sample from the proposed image sensor.



(a) (b)

Fig. 14. (a) Image from the scanner. (b) Image sample from the proposed image sensor.

waveform in Fig. 12) is recorded over 1000 consecutive clock cycles to analyze sensor mismatches. During these cycles, the standard deviation of the high pulsewidth of the sensor output is measured to be 1.5779×10^{-7} seconds, resulting in a readout noise of 0.43%. By defining this noise as the minimum detectable signal, the DR can be calculated as follows:

$$\mathrm{DR} = 20\log\left(\frac{T_0}{1.5779 \times 10^{-7}}\right) = 47.3 \text{ dB}. \tag{4}$$

The DR of the proposed image sensor is measured to be 47.3 dB, achieved through the application of wide-swing technology. In contrast, employing traditional 4T pixels under the same 1-V supply voltage conditions would yield a pulsewidth range of approximately one-fifth of the current value, resulting in a DR of only 33.35 dB. Meanwhile, the total current measured by the source meter is 899.6 nA, and the FoM calculated is 35.1 pJ/(pixel · frame).

To verify the imaging functionality of the proposed image sensor, we captured the Sun Yat-sen University logo printed on an A4 sheet. Fig. 13(a) presents the image of the A4 sheet with the logo obtained from a scanner, while Fig. 13(b) shows the captured sample image, focusing on a portion of the lower right corner of Fig. 13(a). Although the 32 × 32 resolution is low and leads to a noticeable pixelation, the imaging functionality can still be considered normal. To characterize the energy-harvesting characteristics, while ensuring that the imaging function operates normally, we adjusted the intensity of the xenon light source (PL-X500D) and scanned the load of the solar cell to measure the output current. Fig. 14 illustrates the measured I–V and I–P curves under varying illuminance levels. The short-circuit current, open-circuit voltage, and maximum output power were determined. At illuminance levels of 3, 20, 50, and 100 klx, the measured maximum output power was approximately 0.3, 0.57, 1.8, and 3.88 μW, respectively. Given the pixel array area of 0.2 mm^2, the corresponding normalized power generation capability is approximately 194 pW/lx/mm^2. It is noteworthy that this energy-harvesting power was obtained while the imaging mode was operational. If the imaging mode is inactive, the energy-harvesting capability can be measured at 224 pW/lx/mm^2. Table I summarizes the performance of

the proposed image sensor and compares it with other recent state-of-the-art works.

IV. Conclusion

This work proposes a CIS capable of simultaneous imaging and energy harvesting without the need for additional p-n junctions in the pixel array. The proposed pixel employs a vertical n+/p-well/DNW/P-sub structure as the photodiode, which efficiently separates the functions of imaging and energy harvesting. The n+/p-well structure is dedicated to the imaging function, while the p-well/DNW and DNW/P-sub structures are allocated for energy harvesting. To validate the proposed design, an image sensor featuring a 32 × 32 pixel array and a dual-channel PWM quantizer was designed and fabricated. Experimental results indicate that the image sensor achieves a DR of 47.3 dB under a 1-V supply and consumes 899.6 nW of power at 25 fps under 3 klx illumination. Furthermore, the measured power generated through energy harvesting, while maintaining imaging functionality, is 194 pW/lx/mm^2.

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