Modeling for Low Power Bypass Window SAR ADC Based on Highest Weight Capacitor Splitting

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***Abstract*—A 10-bit low power successive approximation register (SAR) analog-to-digital converter (ADC) with bypass window timing based on highest weight capacitor splitting is proposed. Different splitting schemes are analyzed and compared. By establishing a behavioral model in MATLAB, the power consumption of quantizing uniformly distributed signals for each splitting scheme is simulated. The results show that the lowest power consumption is 79.08CV$^2_{REF}$, which saves 94.7% and 53.5% compared with the conventional switching timing and V_{CM}-based timing respectively. The proposed bypass window quantization scheme has more obvious advantages of low power consumption to quantize physiological signals like electrocardiogram (ECG) . It can also improve the accuracy and linearity of the ADC. The paper also analyzes the influence of capacitor mismatch, comparator offset and input noise on the performance of the ADC, and evaluates their impact under different splitting schemes through MATLAB. The simulation results show that with 1% capacitor mismatch error, the "64+64" scheme can achieve an effective number of bits (ENOB) of 9.9 bit.**

Keywords—SAR ADC; low power; highest weight capacitor splitting; bypass window; ECG; biomedical electronics

I. INTRODUCTION

Cardiovascular diseases and stroke are the leading causes of death worldwide, accounting for approximately 17.9 million deaths in 2019 [1]. ECG signals are important medical diagnostic indicators for heart disease, and a simplified ECG signal acquisition and processing system is shown in Fig. 1. It is known that 90% of the ECG signal frequency is concentrated in the range of 0.25~35Hz [2], and it only has occasional large variations in a short period of time. The SAR ADC, due to its binary quantization characteristic and low power advantage, is very suitable for long-term monitoring of ECG systems. In the traditional SAR ADC switching scheme, since all signals need to be quantized according to a fixed steps, a large amount of redundant steps and power consumption will be created when quantizing signals within certain amplitude ranges. Therefore, the concept of bypass window

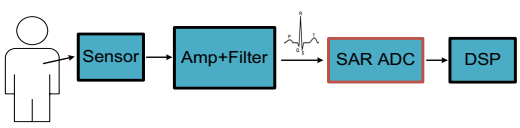

Fig.1. ECG signal acquisition and processing system.

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was proposed in literature to achieve power reduction by skipping some quantization steps [3]. After that, the bypass window SAR ADC has undergone a series of development [4-8], but since most bypass windows require the design of dedicated judgment module circuits, this increases the complexity of circuit design and limits the effect of bypass windows in reducing power consumption.

This paper proposes a bypass window quantization method based on the highest weight capacitor splitting to reduce the quantization power consumption of the 10-bit SAR ADC. Firstly, by monotonically quantizing the redundant unit capacitance of the capacitor array, the most significant capacitance of the array can be reduced from 256C to 128C. Then, the 128C is split into two capacitors, 2^NC and (128-2^N)C, where N is a natural number less than 7. As shown in Fig. 2, the proposed SAR ADC architecture (using a 64C+64C splitting scheme as an example) mainly includes a sampling circuit, digital-to-analog converter (DAC), comparator, and SAR logic circuit. This paper is arranged as follows. Section II describes the DAC switching scheme. Section III discusses the details of simulation results. Section IV concludes this paper.

II. DAC SWITCHING SCHEME

The operation of the SAR ADC mainly consists of two parts: the sampling process and the quantization process. In the sampling process, the bottom plate is connected to V_{CM} uniformly, and the top plate is used for sampling, where V_p=V_{in+} and V_n=V_{in-}. The quantization of SAR ADC mainly consists of three parts: bypass window quantization, traditional V_{CM}-based quantization and monotonic quantization, with the following specific steps:

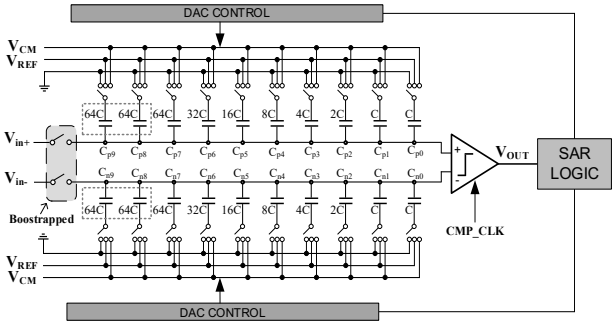


Fig.2. The proposed SAR ADC architecture

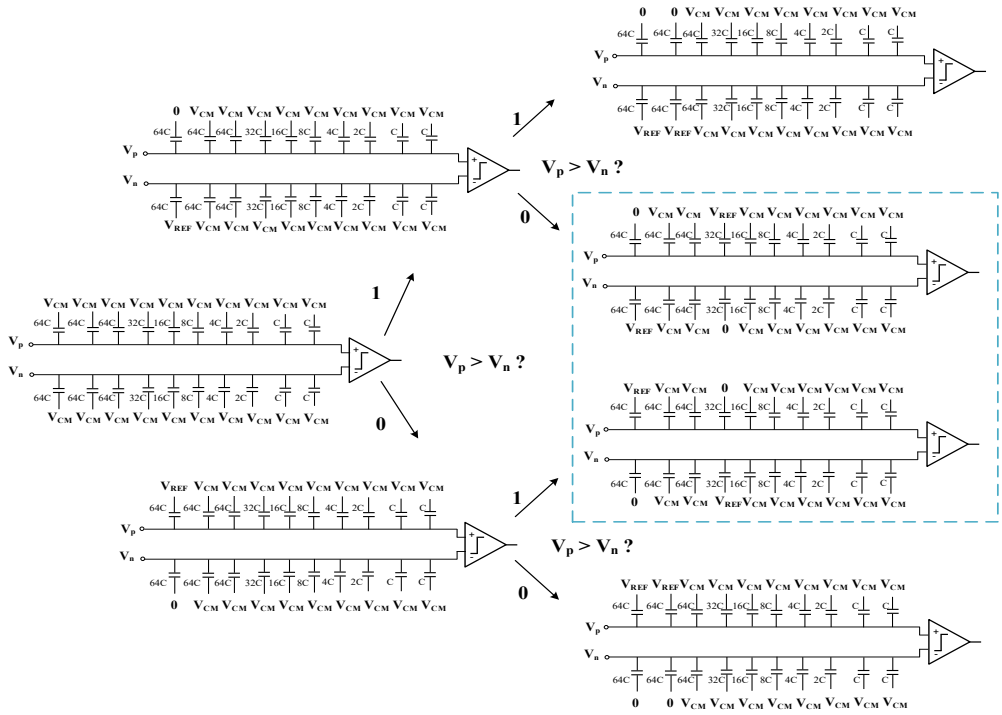


Fig.3. Proposed Switching Scheme for 10-bit SAR ADC.

1) For the first comparison, if $V_p > V_n$, the most significant bit (MSB) D[9] = 1 and the bottom plate of C_{p9} is connected to GND, while the bottom plate of C_{n9} is connected to V_{REF}. If $V_p < V_n$, the MSB D[9] = 0 and the bottom plate of C_{p9} is connected to V_{REF}, while the bottom plate of C_{n9} is connected to GND.

2) For the second comparison, there are two possible cases as shown in Fig. 3.

Case 1: If D[9] is different from the second comparison result, it means that the polarities of V_p and V_n have changed before and after voltage switching, i.e. it falls within the bypass window. The dashed box indicates the bypass window quantization process. In this case, the voltage switching can skip the next two 64C capacitors and directly switch the 32C.

If D[9] = 0 and the second comparison result is $V_p > V_n$, the bottom plates of C_{p8}, C_{p7}, C_{n8}, C_{n7} remain unchanged. The bottom plate of C_{p6} is connected to GND and the bottom plate of C_{n6} is connected to V_{REF}, and D[8] = 1, D[7] = 1.

If D[9] = 1 and the second comparison result is $V_p < V_n$, the bottom plates of C_{p8}, C_{p7}, C_{n8}, C_{n7} remain unchanged. The bottom plate of C_{p6} is connected to V_{REF} and the bottom plate of C_{n6} is connected to GND, and D[8] = 0, D[7] = 0.

Then continue to quantify according to the V_{CM}-based timing.

Case 2: If D[9] is the same as the second comparison result, it means the signal falls outside the bypass window. Then continue to quantify according to the V_{CM}-based timing.

3) For the second least significant bit (LSB), if $V_p > V_n$, D[1] = 1 and the bottom plate of C_{p1} is connected to GND. Conversely, if $V_p < V_n$, D[1] = 0 and the bottom plate of C_{p1} is connected to V_{REF}. After the voltage changes, if $V_p > V_n$, D[0] is 1; if $V_p < V_n$, D[0] is 0.

In fact, there are multiple ways to perform capacitor splitting based on the highest weight in addition to splitting 128C into "64C+64C". Capacitors can also be split into different combinations such as "32C+96C", "16C+112C", "8C+120C", "4C+124C", "2C+126C", and "1C+127C". The smaller the bypass window capacitor, the more capacitors in the array are skipped during quantization of the input signal within the window. However, the probability of the signal falling into the window is lower. Detailed analysis and explanations of different splitting schemes will be provided in Section III.

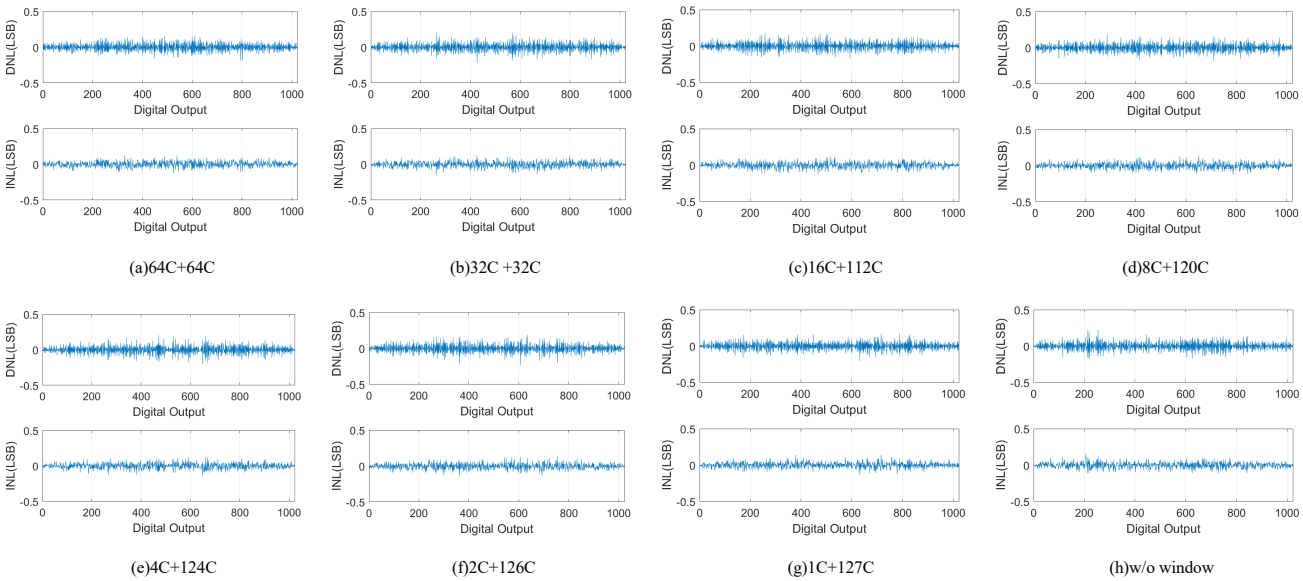
III. Analysis of Different Quantization Splitting Schemes

A. Error Analysis

Assume the mismatch error of the unit capacitor C due to semiconductor fabrication process follows a normal distribution with a mean value of Co and a standard deviation of σ_C. Fig. 4 shows the simulation results of integral nonlinearity (INL) and differential nonlinearity (DNL) when σ_C = 1%. These results of different splitting schemes are statistically analyzed to obtain Table I. Similarly, by simulating and analyzing INL and DNL when σ_C = 3%, Table II can be obtained.

It can be seen that when σ_C increases from 1% to 3%, both INL and DNL increase across almost all levels, which indicates that the larger the standard deviation of the unit capacitor caused by manufacturing process, the worse the linearity of the ADC. Due to the randomness of a single simulation, it is difficult to observe the impact of unit capacitor mismatch error on the performance of the proposed SAR ADC architecture. Therefore, for each capacitive splitting scheme, 20 simulations were performed. The minimum ENOB of the 20 simulations was taken as the reference value of the ADC, finally obtaining the relationship between $ENOB_{min}$ and the size of bypass window as shown in Fig. 6.

The input signals falling within the window will skip some quantization steps, which can avoid the negative impact of some capacitor mismatch on conversion accuracy. Therefore, under the same capacitor mismatch error, the ENOB of the



(a)64C+64C (b)32C +32C (c)16C+112C (d)8C+120C

(e)4C+124C (f)2C+126C (g)1C+127C (h)w/o window

Fig.4. The INL and DNL of different splitting schemes when σ_C = 1%.

TABLE I. INL AND DNL PEAK VALUES WITH Σ_C=1%.

Splitting Schemes	INL peak values (LSB)	DNL peak values (LSB)
64C+64C	0.13/-0.13	0.23/-0.20
32C+96C	0.13/-0.16	0.33/-0.31
16C+112C	0.13/-0.13	0.25/-0.28
8C+120C	0.14/-0.13	0.23/-0.28
4C+124C	0.13/-0.14	0.33/-0.36
2C+126C	0.14/-0.14	0.36/-0.22
1C+127C	0.14/-0.14	0.23/-0.27
w/o window	0.16/-0.11	0.20/-0.23

TABLE II. INL AND DNL PEAK VALUES WITH Σ_C = 3%.

Splitting Schemes	INL peak values (LSB)	DNL peak values (LSB)
64C+64C	0.16/-0.19	0.30/-0.27
32C+96C	0.20/-0.22	0.30/-0.30
16C+112C	0.19/-0.17	0.34/-0.34
8C+120C	0.19/-0.19	0.33/-0.38
4C+124C	0.20/-0.20	0.28/-0.31
2C+126C	0.19/-0.23	0.31/-0.34
1C+127C	0.17/-0.20	0.36/-0.31
w/o window	0.22/-0.17	0.30/-0.28

bypass window scheme is higher than that of the w/o window scheme. Moreover, the probability of the signal falling into the 64C size bypass window is the largest, so the chances of skipping some conversion steps are also the most, and the ENOB and linearity are the best.

The effect of Gaussian white noise in the input signal on the ENOB under different capacitor splitting schemes is also analyzed. In MATLAB, the "awgn" function is used to add specified signal-to-noise ratio (SNR) Gaussian white noise to simulate external interference, and a 70dB SNR is adopted in this paper. The simulation results in Fig. 7 show that the effect of white noise on ENOB is almost the same for different capacitor splitting schemes. At the same time, Fig. 7 shows the effect of different splitting schemes on ENOB when the comparator offset error is 1.5 LSBs. It can be seen that the splitting scheme has almost no effect on ENOB.

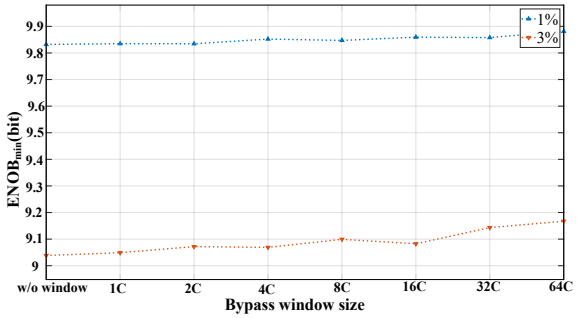


Fig.6. The relationship between ENOB and bypass window size.

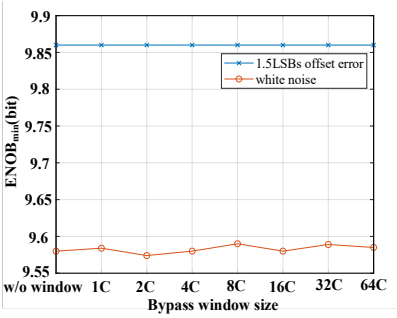


Fig.7. The effect of white noise and 1.5LSBs offset error on ENOB for different splitting schemes.

B. *Power Consumption Analysis*

Fig. 8 shows the quantization power consumption curves of the conventional timing [9], V_{CM}-based timing [10] and w/o window timing DAC for a resolution of 10 bits. On the basis of the w/o window timing, the highest weight capacitance is decomposed into different combinations. For each splitting scheme, MATLAB modeling and power consumption simulations were performed. For uniformly distributed signals, the average power consumptions of different splitting schemes are shown in Fig. 9. It can be seen that the average quantization power consumption of all splitting schemes is lower than that of the w/o window scheme. More importantly, when the bypass window size is 64C, the average power consumption is the lowest, only $79.08CV^2_{REF}$, which saves 94.7% and 53.5% compared with the conventional switching timing and V_{CM}-based timing respectively.

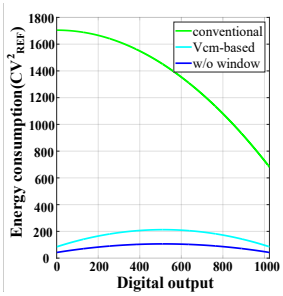


Fig.8 The power consumption curves for some traditional methods.

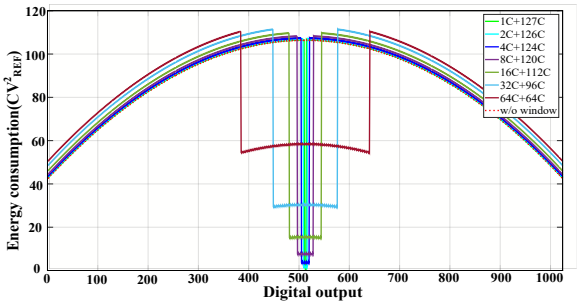


Fig.9 The power consumption curves of different capacitor splitting schemes.

TABLE III. POWER CONSUMPTION AND NUMBER OF COMPARISON CYCLES FOR DIFFERENT QUANTIZATION SCHEMES.

Splitting Scheme		*Average Power Consumption*	*Average Number of Comparison Cycles*
Conventional		1363.33	10
V_{CM}-based		170.17	10
w/o Window		85.08	10
Splitting Schemes	1C+127C	84.92	10.97
	2C+126C	84.75	10.95
	4C+124C	84.43	10.91
	8C+120C	83.81	10.84
	16C+112C	82.68	10.75
	32C+96C	80.83	10.63
	64C+64C	79.08	10.50

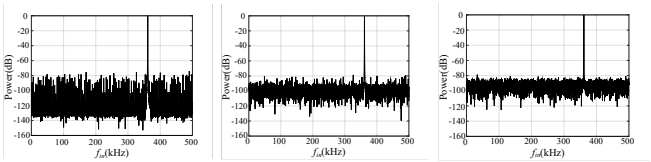
Table III summarizes the average capacitive array power consumption and average comparison counts for uniformly distributed inputs under different quantization schemes. It can be seen that the "64C+64C" splitting scheme has both the lowest quantization power and the average number of comparisons, at 79.08 CV^2_{REF} and 10.5, respectively. However, for quantizing specific signals, especially physiological signals with obvious concentrated distributions, the splitting scheme can be selected according to the distribution characteristics of the signals to achieve a better match.

C. *Spectral Analysis*

Taking the "64C+64C" splitting scheme as an example, the quantization results are analyzed by Fast Fourier Transform (FFT) spectrum. Assuming the ADC power supply is 0.6V and the sampling rate is 1MHz. When the input is a 0.6V, 361.3kHz sinusoidal signal, quantization is performed under unit capacitor standard deviations of 0, 1% and 3%. The spectra are shown in the Fig.10. The dynamic performance statistics of the proposed ADC are summarized in Table IV.

IV. CONCLUSION

This paper proposed a bypass window SAR ADC based on highest weight capacitor splitting. For different splitting schemes, MATLAB behavioral modeling is performed



(a)σ_C = 0 (b)σ_C = 1% (c)σ_C = 3%

Fig.10. FFT spectrum of the "64C+64C" splitting scheme.

TABLE IV. THE DYNAMIC PERFORMANCE OF THE PROPOSED ADC WITH BYPASS WINDOW.

Capacitor Standard Deviation	**SNDR(dB)**	**SNR(dB)**	**SFDR(dB)**	**ENOB(bit)**
0	62.16	63.74	73.89	10.0
1%	61.16	61.6	77.46	9.9
3%	56.95	57.05	81.38	9.2

respectively. The impact of Gaussian white noise, unit capacitor mismatch error and comparator offset error on the linearity and dynamic performance of the ADC under different splitting schemes were analyzed. The average quantization power consumption of the capacitor array and the average number of comparisons were statistically analyzed for different schemes. According to the characteristics of physiological signals and the power characteristics of each splitting scheme, a matching low-power splitting scheme can be selected. For uniformly distributed signals, the "64C+64C" splitting scheme has the lowest power and best performance. This work has certain reference significance for the improvement of SAR ADC performance and power reduction, especially in the field of physiological signals such as ECG.

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