A 3.7-nW 248-ppm/°C Subthreshold Self-Biased CMOS Current Reference

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***Abstract*—A modified self-biased β-multiplier-based current reference (CR) circuit is proposed for ultralow-power Internet of Things (IoT) application and is realized without any resistors, bipolar junction transistors (BJTs), or operational amplifiers (OPAs). The proposed CR circuit directly generates the reference current from a modified β-multiplier, which is biased by a stacked diode-connected MOS transistor (SDMT)-based compensated through a complementary-to-absolute temperature (CTAT) voltage. The proposed CR is implemented in a standard 0.18-μm CMOS process with an active area of 0.0069 mm^2 and almost all transistors operate in the subthreshold region. Measurement results show that the temperature coefficient (TC) of the CR is 248 ppm/°C in a temperature range from −40 °C to 125 °C. The proposed CR exhibits a line sensitivity (LS) of 0.33%/V within the supply voltage range of 0.8–1.4 V. The output of the CR at room temperature (25 °C) is 1.84 nA with a power consumption of 3.7 nW.**

***Index Terms*—CMOS, current reference (CR), line sensitivity (LS), low power, self-biased, stacked diode-connected MOS transistor (SDMT), subthreshold, temperature coefficient (TC).**

I. Introduction

In recent years, there has been an increasing need for ultralow-power solutions to sustain the operation of the Internet of Things (IoT) nodes. They need to run for a long time with low-capacity batteries or energy-harvesting platforms [1]. A reference circuit needs to generate stable currents or voltages that are independent of process variations, power supply voltages, and temperature fluctuations (PVT). To achieve performance optimization and low power consumption, the difference between gate-source voltages (ΔV_{GS}) is used to obtain a voltage reference [2].

Current references (CRs) are also fundamental components in the IoT devices, used to set the operating points of analog/mixed-signal blocks, such as amplifiers and oscillators [3]. Microsensors with self-powered capabilities have substantial potential in Internet of Everything applications, as they are small and can operate independently by harvesting energy from the ambient environment [4], [5]. This requires the sensors to work in the nanowatt levels [6]. Numerous low-power CRs have been proposed [7], [8], [9], [10], [11], [12], [13], [14], [15]. Among them, the low-power CRs using resistors have been discussed to generate stable CRs [7], [8]. However, to produce a nanoampere current, GΩ-level resistors are typically required, leading to a significant increase in the circuit area. The smallest area among them [7] is 0.023 mm^2. A voltage-controlled CR is proposed in [9], but it needs an external bias voltage to improve accuracy. Reference circuits that do not use resistors can greatly save the circuit area [10], [11]. They employ different methods for temperature compensation of CRs, but even the widest temperature range in these works [11] was relatively limited from −10 °C to 100 °C. Operational amplifiers (OPAs) were used in [12] and [13]. The CR circuits use bipolar junction transistors (BJTs) in [12] and [13], which not only result in a large circuit area but also increase the minimum operating voltage. The CR based on the modified β-multiplier is also applied in [14] to generate the reference voltage. A level shift is proposed in [15] and used for isolating the N-channel/P-sub diode leakage current, which decreases the temperature coefficient (TC).

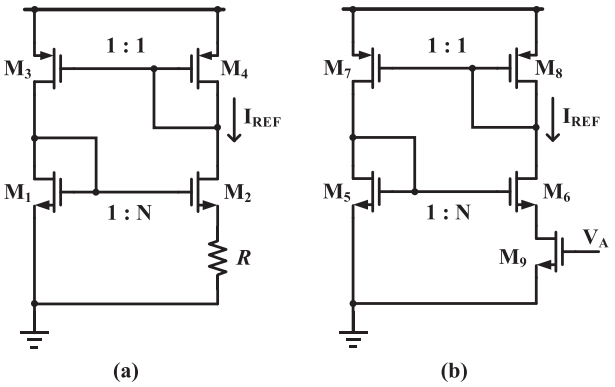

Fig. 1. Conceptual diagrams of (a) conventional β-multiplier and (b) modified β-multiplier.

To solve the problems mentioned above, this brief proposes a new circuit configuration for a temperature-independent CR based on a single modified self-biased β-multiplier with a small silicon area. The TC of the output current is compensated through a complementary-to-absolute temperature (CTAT) voltage generator using different types of nMOS and a simple self-biasing path. Section II describes the traditional self-biased β-multiplier and the modified self-biased β-multiplier. Section III discusses the circuit description and analysis of the proposed CR circuit. Section IV presents the measurement results and a performance comparison between some recent works and the proposed CR circuit. Finally, Section V concludes this brief.

II. Self-Biased β-Multiplier

Fig. 1 shows the conceptual diagram of the traditional self-biased β-multiplier and the modified self-biased β-multiplier [18]. When the drain-source voltage (V_{DS}) is greater than three times the thermal voltage ($3V_T$), the drain current of the MOSFET in the weak inversion can be approximated as

$$I_D \approx \mu_n C_{OX} K V_T^2 \exp\left(\frac{V_{GS} - V_{TH}}{mV_T}\right) \tag{1}$$

where μ_n represents the mobility of electrons; C_{OX} is the gate oxide capacitance; V_{TH} is the threshold voltage of the transistor, which is inversely proportional to temperature; K is the aspect ratio (= W/L) of the transistor; $V_T = k_B T/q$ is the thermal voltage, exhibiting a positive TC; k_B is Boltzmann's constant; T is the absolute temperature; q is the elementary charge; and m is the subthreshold slope factor.

The aspect ratio of M_1–M_2 (M_5–M_6) is 1:N. This results in a gate-source voltage difference ΔV_{GS} of M_1 and M_2 (M_5 and M_6) when they carry the same current. ΔV_{GS} is applied to the resistor R and the current flowing through R is defined as a proportional-to-absolute temperature (PTAT) current generated by the conventional

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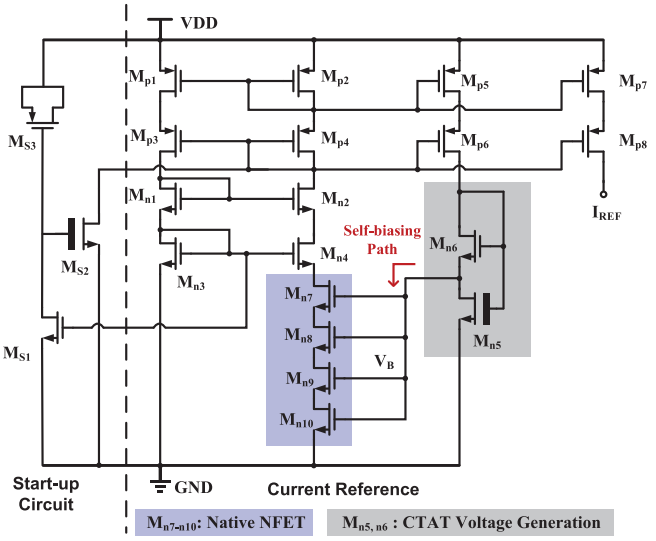


Fig. 2. Circuit diagram of the proposed CR circuit.

TABLE I
COMPONENTS PARAMETERS USED IN THE PROPOSED CIRCUIT

Components	W/L (μm/μm)	Components	W/L (μm/μm)
M_{S1}	0.22/0.18	M_{p11}	3*12/3
M_{S2}	2/4	M_{p12}	3*4/3
M_{S3}	4*5/5	M_{n1}	2/3
M_{p1}	2*12/3	M_{n2}	4/3
M_{p2}	3*12/3	M_{n3}	10/3
M_{p3}	2*4/3	M_{n4}	20/3
M_{p4}	3*4/3	M_{n5}	6*12/19
M_{p5}	12/3	M_{n6}	2/19
M_{p6}	4/3	M_{n7}-M_{n10}	0.5/19

β-multiplier. Assuming that the subthreshold slope factors $m_1 = m_2 = m_5 = m_6 = m$, the expression for the generated PTAT current I_{REF} in this circuit can be expressed as follows:

$$I_{REF} = \frac{1}{R} m V_T \ln N. \tag{2}$$

GΩ-level resistors occupy a large area of silicon. Therefore, an MOS transistor operating in the deep triode region can be used to replace the resistor, as shown in Fig. 1(b). According to the strong-inversion triode equation of nMOS, the equivalent resistance R_{eff} of M_9 can be expressed as

$$R_{eff} \approx \frac{1}{\mu_{n9} C_{OX9} K_9 (V_A - V_{TH9})}. \tag{3}$$

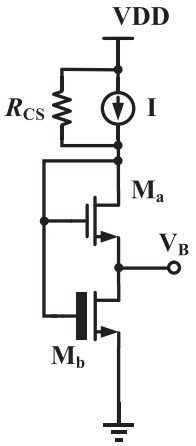
I_{REF} in Fig. 1(b) is modified as follows:

$$I_{REF} = \mu_{n9} C_{OX9} K_9 (V_A - V_{TH9}) m V_T \ln N. \tag{4}$$

Without using resistors, it can be observed that the modified β-multiplier is allowed to output nanoampere-level current with a smaller area.

III. DESIGN OF THE PROPOSED CR CIRCUIT

The circuit diagram is shown in Fig. 2, and the transistor sizes are given in Table I. The start-up circuit consists of M_{S1}, M_{S2}, and M_{S3}, and can make the CR circuit deviate from the original zero bias point into the normal operation state, wherein M_{S1} acts as a capacitor. The CR is generated by a self-biased β-multiplier circuit and a CTAT voltage generation, producing a temperature-independent current. To meet the requirements of low-voltage low-power IoT sensor applications, native NFETs (M_{n7}–M_{n10}) are used and biased in the deep triode region to act as a large resistor with adjustable resistance, while all other transistors operate in the subthreshold region.



Output Voltage:

$$V_B = \left(\frac{m_a}{m_b} V_{THb} - V_{THa}\right) + m_a V_T \ln\left(\frac{\mu_a C_{oxa} W_a L_b}{\mu_b C_{oxb} W_b L_a}\right) + (m_b - m_a) V_T \ln\left(\frac{L_a I}{\mu_b C_{oxb} W_b V_T}\right)$$

LS:

$$\frac{V_B}{VDD} \approx \frac{\frac{1}{g_{mb}} - \frac{1}{g_{ma}}}{R_{CS} + \frac{1}{g_{mb}}}$$

Fig. 3. Conceptual diagram of the SDMT structure.

A. CTAT Voltage Generation

The stacked diode-connected MOS transistor (SDMT) structure is known as a simple voltage reference [2]. The schematic of the SDMT is shown in Fig. 3. The output voltage $V_B = V_{GSb} - V_{GSa}$. Since both M_a and M_b are operated in the subthreshold region, the drain current of M_a and M_b has been given in (1). Therefore, V_B can be approximated as

$$V_B = \left(\frac{m_a}{m_b} V_{THb} - V_{THa}\right) + m_a V_T \ln\left(\frac{\mu_a C_{oxa} W_a L_b}{\mu_b C_{oxb} W_b L_a}\right) + (m_b - m_a) V_T \ln\left(\frac{L_a I}{\mu_b C_{oxb} W_b V_T}\right). \tag{5}$$

M_b is a thick-oxide nMOS transistor and M_a is a thin-oxide nMOS transistor. In the CMOS process used, m is 1.13 and 1.03 for thin-oxide nMOS transistors and thick-oxide nMOS transistors, respectively. It can be seen that the first term in (5) is the threshold voltage difference generating a CTAT voltage

$$\Delta V_{TH} \approx \Delta V_{TH0} + (\alpha_b - \alpha_a)(T - T_0) \tag{6}$$

where α is the first-order derivative of threshold voltage with respect to temperature, $\alpha_a < \alpha_b < 0$, ΔV_{TH0} is the threshold voltage difference at room temperature, and T_0 is the room temperature (25 °C). As shown in (6), ΔV_{TH} exhibits a CTAT characteristic, while the second term in (5) represents a tunable PTAT voltage by sizing M_a and M_b. Therefore, V_B can be designed to be a tunable CTAT voltage with the desired TC.

Line sensitivity (LS) is generally defined as $\Delta V_{OUT}/\Delta VDD$, it is a crucial parameter that represents the dependence of the circuit's output on variations of the supply voltage under dc conditions. It is obvious that if $m_a = m_b$, the output voltage will not be related to the bias current I. In fact, due to the different subthreshold slope factors m between M_a and M_b, the stability of the bias current also affects the stability of the output voltage [2]. From (4), the LS performance of CTAT voltage V_B will also affect the LS performance of the CR. Ignoring the short-channel length modulation effect, the LS for the SDMT can be approximated as

$$\frac{V_B}{VDD} \approx \frac{\frac{1}{g_{mb}} - \frac{1}{g_{ma}}}{R_{CS} + \frac{1}{g_{mb}}}. \tag{7}$$

If the bias current of M_a and M_b transistors are equal, g_{ma} is equal to g_{mb}, indicating that the circuit is independent of the power

supply voltage. However, in practical applications, the transconductance g_m of transistors operating at subthreshold is influenced by the subthreshold slope factor m. A cascode current mirror circuit is used to improve the output impedance of the current mirror. In addition, although increasing the number of SDMT stages can increase the output voltage and reduce process dependency, this also leads to higher power consumption, a larger circuit area, and a higher minimum supply voltage [2]. Based on these considerations, a single-stage SDMT circuit is used for the CTAT voltage generation to achieve a simple and small silicon area circuit. The weak correlation between the output voltage and current of SDMT can realize low current consumption of SDMT structure, further reducing the power consumption of the circuit.

B. CR Circuit

Based on the self-biased β-multiplier, a cascode current mirror circuit is used to reduce the influence of power supply voltage disturbances on the generated reference current. Due to the small CTAT voltage V_B, to ensure the working state of the MOSFET that replaces the resistor is in the deep triode region, four identical native transistors M_{n7}–M_{n10} with small width and long length are biased by the one-stage SDMT circuit. The series connection of four native transistors results in a larger equivalent R, with the aim of reducing power consumption. V_{DS} of M_{n7}–M_{n10} is only several millivolts and so their gate-source voltage V_{GS} is approximately equal. These four identical transistors in series are equivalent to one with a 1/4 aspect ratio of each. Assuming that the subthreshold slope factors $m_{n1} = m_{n2}$ and $m_{n5} = m_{n6}$. This gate bias voltage is given in (5). Substituting it into (4) yields the final output of the proposed CR, as shown in the following equation:

$$I_{REF} = \frac{1}{4}\mu_{n7}C_{OXn7}K_{n7}m_{n4}V_T \ln\left(\frac{\mu_{n4}C_{OXn4}K_{n4}}{\mu_{n3}C_{OXn3}K_{n3}}\right) \times \left[(V_{THn5}-V_{THn6}-V_{THn7})+m_{n6}V_T \ln\left(\frac{\mu_{n6}C_{OXn6}K_{n6}}{\mu_{n5}C_{OXn5}K_{n5}}\right)\right]. \quad (8)$$

Due to the negative TC exhibited by the threshold voltage difference ΔV_{TH} and the positive TC exhibited by the thermal voltage V_T, the equation can be simplified as follows:

$$I_{REF} = (\Delta V_{TH1} + B(T - T_0) + A_1 T)A_2 T \quad (9)$$

$$B = \alpha_{n5} - \alpha_{n6} - \alpha_{n7} \quad (9\text{-a})$$

$$A_1 = \frac{\partial V_T}{\partial T} m_{n6} \ln\left(\frac{\mu_{n6}C_{OXn6}K_{n6}}{\mu_{n5}C_{OXn5}K_{n5}}\right) \quad (9\text{-b})$$

$$A_2 = \frac{\partial V_T}{\partial T} m_{n4} \frac{1}{4}\mu_{n7}C_{OXn7}K_{n7} \ln\left(\frac{\mu_{n4}C_{OXn4}K_{n4}}{\mu_{n3}C_{OXn3}K_{n3}}\right) \quad (9\text{-c})$$

where ΔV_{TH1} is the threshold voltage difference of M_{n5}, M_{n6} and M_{n7} at room temperature; and the coefficients $B < 0$, $A_1 > 0$, and $A_2 > 0$. Take the partial derivative for the temperature

$$\frac{\partial I_{REF}}{\partial T} = 2(B + A_1)A_2 T + A_2(\Delta V_{TH1} - BT_0). \quad (10)$$

By adjusting the transistors' sizes, it is possible to achieve better TC performance for the output of the reference current within the overall temperature range by setting $\partial I_{REF}/\partial T = 0$ at 40 °C. The 40 °C is approximately the center of the temperature range that is targeted in this brief.

C. Influence of Process Variations

The reference output I_{REF} is influenced by process parameters such as V_{TH}. The variation of the threshold voltage is generally larger than that of the mobility [10]. From (8), it can be seen that the impact of threshold voltage variation on I_{ref} has not been effectively eliminated. This indicates that the TC variations are dominated by the process variations of the threshold voltage of M_{n5}–M_{n10}. Monte Carlo simulations for the proposed CR circuit are made and the results are shown in Fig. 4. Over 1000 runs, the average CR output value is 2.05 nA with a standard deviation of 0.59 nA. The median TC is 380 ppm/°C and the TC of 60% chips is in the range of 220 ppm/°C and 520 ppm/°C. According to (5), the difference in subthreshold slope factors ma and mb leads to a weak correlation between the CTAT voltage and bias current output by SDMT. At the same time, due to the reference current being output through the current mirror, the mismatch has a certain impact on I_{ref}, but the dominant reason is still the process deviations. The output current may have certain process variations, which can lead to slight performance and power consumption impacts on application circuits such as ADCs.

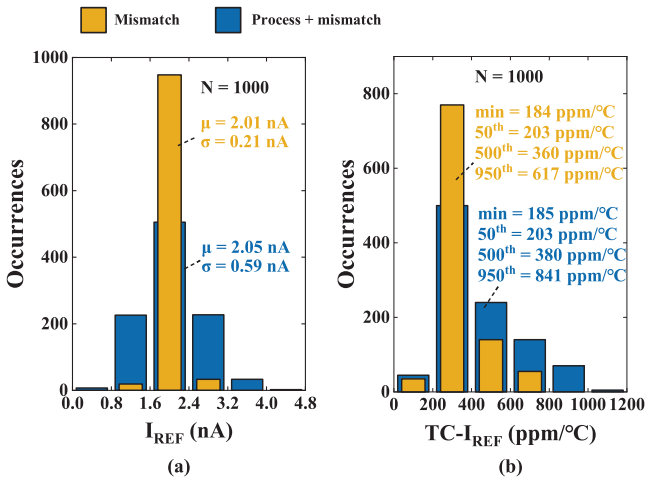


Fig. 4. Results of Monte Carlo simulations with both local mismatch and process variations considered for the proposed CR circuit at 1 V. (a) I_{REF} at 25 °C and (b) TC-I_{REF}.

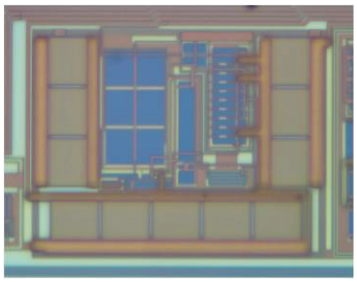


Fig. 5. Micrograph of the proposed CR.

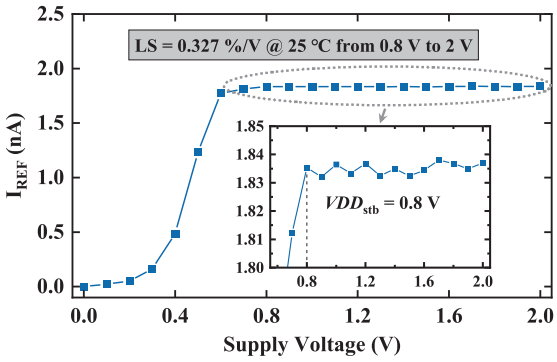


Fig. 6. Measured LS of the proposed CR at room temperature.

IV. Measurement Results

The proposed CR circuit is fabricated using a standard 0.18-μm CMOS process. Fig. 5 shows the micrograph of the proposed CMOS CR, occupying an area of 0.0069 mm^2. Fig. 6 illustrates the

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER WORKS

	This work [Δ]	TCASI'2019 [3] [Δ]	VLSI-DAT'2019 [11] [Δ]	ISSCC'2017 [12] [Δ]	ISCAS'2022 [13] [*]	AEU'2023 [16] [*]	JSSC'2024 [17] [Δ]
Technology(nm)	**180**	180	180	180	130	180	110
Type	**CMOS**	CMOS	CMOS	CMOS	Sub-BGR	CMOS	CMOS
Supply Voltage(V)	**0.8-1.4**	0.7-2	0.85	1.3-1.8	0.9	0.55-1.8	0.8-1.2
Power (nW)	**3.7**	28	15.8	9.3	30	9.6	16.8
I_{REF}(nA)	**1.84**	10	6.3	6.64	2	1.96	2.3
Temp. Range(°C)	**-40~125**	-40~125	-10~100	0~110	-20~80	0~100	-40~85
TC-I_{REF}(ppm/°C)	**248**	150	138	283	474	96.17	176
LS-I_{REF}(%/V)	**0.33**	0.6	4.15	1.16	N/A	0.2	2.23
Area(mm^2)	**0.0069**	0.055	0.062	0.055	0.04	0.003	0.0106
FoM($°C^3$/%×nW×ppm×mm^2)	**150**	74	27	71	2	2021	142

[*] Simulation results, [Δ] Measurement results.

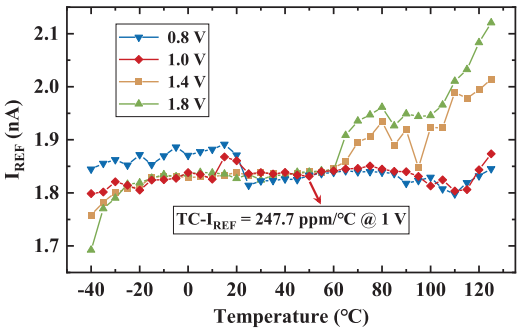


Fig. 7. Measured TC of I_{REF} at different power supply voltages.

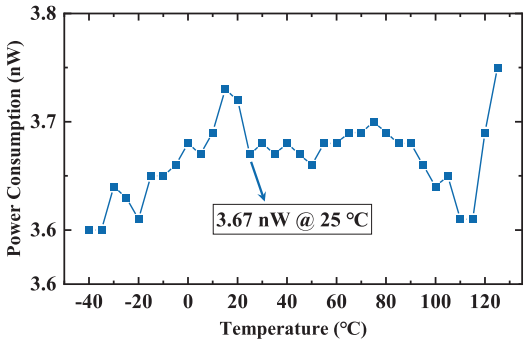


Fig. 8. Measured power consumption of the proposed CR circuit at a 1-V power supply voltage.

measurement results of LS characteristics at room temperature. The LS of the CR output within a supply voltage range of 0.8–2.0 V is 0.33%/V.

Fig. 7 presents the TC measurement results of the CR circuit. Without any trimming adjustments, the TC of the CR is 248 ppm/°C over a wide temperature range from −40 °C to 125 °C. At room temperature (25 °C), the CR output is 1.84 nA. The measurement results also show the TCs under different power supply voltages. When the power supply voltage is higher than 1 V, I_{ref} shows an increase in high-temperature conditions. The reason is that V_{DS} of M_{n7}–M_{n10} will rise when the power supply voltage increases, resulting in a worse TC. Fig. 8 shows the power consumption variations with the temperature under a 1-V power supply voltage. The power consumption of the circuit is only 3.67 nW at room temperature. Due to the bias current of the entire circuit generated by the CR, the power consumption remains stable at around 3.7 nW within a wide temperature range from −40 °C to 125 °C.

Table II provides a comparison between the performance of low-power CR circuits in recent years and the proposed work. In order for a fair comparison in more complete dimensions, we suggest a figure of merit (FoM)

$$\text{FoM} = \frac{(T_{\text{MAX}} - T_{\text{MIN}})^2 \times \mu}{\text{TC} \times \text{Power} \times \text{Area} \times \sigma \times 100} \tag{11}$$

which is based on [19]. Achieving a low TC for the CR over a wide temperature range, while operating at the nanowatt level is challenging due to the significant influence of temperature and process factors on the current. This work achieves a TC of 248 ppm/°C at ultralow power consumption for the CR within a wide temperature range from −40 °C to 125 °C. Moreover, this work achieves favorable LS performances and also exhibits advantages in terms of circuit area, while having the best FoM performance except for [16], which has a relatively small temperature range and only shows the simulation results.

V. CONCLUSION

This brief proposes a subthreshold CMOS CR circuit based on a modified self-biased β-multiplier implemented in a standard 0.18-μm CMOS process for ultralow-power applications. Measurement results demonstrate that the proposed circuit achieves a TC of 248 ppm/°C for CR over a temperature range from −40 °C to 125 °C while occupying a small chip area of 0.0069 mm^2. The circuit can provide stable output current under the 0.8–2.0-V supply voltage range. The power consumption is only 3.7 nW at room temperature and remains stable from −40 °C to 125 °C. Therefore, it represents a simple and small silicon area solution for ultralow-voltage, ultralow-power IoT sensor applications.

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