A Dual-Direction SCR Featuring Shallow Snapback and High-Temperature Robustness for ESD Protection of Industrial Communication Buses

Yang Wang, *Member, IEEE*, Ke Zhang, Yujie Liu, Wei Liu, Bingjun Xiong, *Graduate Student Member, IEEE*, Qifeng Fu, Jingjing Liu, and Yuqin Dou

***Abstract*— The reliability standards for on-chip electrostatic discharge (ESD) protection in high-voltage industrial communication buses are stringent, and traditional ESD solutions cannot effectively meet the requirements for high holding voltage (V_h) and high-temperature tolerance in these applications. Therefore, this article presents a dual-direction silicon-controlled rectifier (DDSCR) featuring shallow snapback and high-temperature robustness. At the same size, V_h (38.4 V) of the parallel NPN-enhanced SCR (NPNE_DDSCR), which employs a metal short and no shallow trench isolation (STI), is significantly higher than that of the traditional structure (T_DDSCR) and the parallel NPN structure (NPN_DDSCR). Under high-temperature conditions ranging from 50 °C to 125 °C, the structure maintains nanoampere-level leakage current, and the device's ESD characteristics show no significant degradation. The electrostatic properties of three types of structures were verified based on the 0.18-μm bipolar-CMOS–DMOS (BCD) process, and their operating mechanisms were further analyzed using technology computer-aided design (TCAD) simulations. The results show that the NPNE_DDSCR exhibits superior performance, with a human body model (HBM) level exceeding 8 kV, and is suitable for efficient on-chip ESD protection of industrial communication buses.**

***Index Terms*— Electrostatic discharge (ESD), integrated circuit reliability, semiconductor device reliability.**

Received 4 June 2025; revised 10 July 2025 and 2 September 2025; accepted 8 September 2025. This work was supported in part by the National Natural Science Foundation of China under Grant 62304007 and Grant 62174181 and in part by the Natural Science Research Start-Up Foundation of Recruiting Talents of Nanjing University of Posts and Telecommunications under Grant NY224101. The review of this article was arranged by Editor C. Duvvury. *(Corresponding authors: Jingjing Liu; Yuqin Dou.)*

Yang Wang, Qifeng Fu, and Yuqin Dou are with the College of Integrated Circuit Science and Engineering, Nanjing University of Posts and Telecommunications, Nanjing 210023, China (e-mail: douyuqin@njupt.edu.cn).

Ke Zhang, Yujie Liu, and Wei Liu are with the Key Laboratory of Physics and Devices in Post-Moore Era, College of Hunan Province, Hunan Normal University, Changsha 410081, China.

Bingjun Xiong and Jingjing Liu are with the School of Electronics and Communication Engineering, Sun Yat-sen University, Nanjing 210023, China (e-mail: liujj77@mail.sysu.edu.cn).

Digital Object Identifier 10.1109/TED.2025.3608742

I. Introduction

INDUSTRIAL control and automotive electronic systems are commonly exposed to severe environments characterized by intense electrostatic stress and elevated temperatures. Depending on the application domain, the bus ports of a controller area network (CAN) are required to withstand different voltage levels, such as ±14, ±16, ±36, ±58, and ±70 V. This is to ensure the high robustness of the CAN bus during operation and to prevent chip damage caused by power short circuits, transient disturbances, and other anomalies. Therefore, to meet the application requirements of industrial automation or automotive electronics, CAN bus ports commonly employ high-voltage LDMOS devices to satisfy the 70-V breakdown voltage (BV) standard. In addition, the bus port defines a minimum holding voltage (V_h) of ±36 V for its on-chip bidirectional electrostatic discharge (ESD) protection device to prevent false triggering or destructive latch-up caused by high transient voltages. Currently, traditional high-voltage ESD protection solutions include stacked diodes [1], [2], PNP [3], [4], GGNMOS [5], [6], and SCR [7], [8]. Both diodes and PNP rely on a snapback-free characteristic to prevent latch-up. GGNMOS exhibits shallow snapback behavior due to the presence of a parasitic NPN path, but its high-temperature tolerance is poor. SCR benefits from the positive feedback mechanism of parasitic NPN and PNP transistors. Although it can achieve high discharge efficiency per unit area, its deep snapback characteristic results in a low V_h, which makes it difficult to adapt to the ESD window of high-voltage buses and leads to a high risk of latch-up [9], [10], [11]. Enhancing V_h of SCR devices is an effective method to extend their application range. Works [12], [13], [14], [15], [16], [17] introduced multiple parallel paths to suppress the positive feedback of SCR, thereby increasing V_h. Bourgeat et al. [18] and Wang et al. [19] use stacking of unit SCRs to achieve high V_h characteristics. However, this solution comes at the cost of increased area. Deng et al. [20] proposed a traditional symmetrical dual-direction silicon-controlled rectifier (DDSCR) structure based

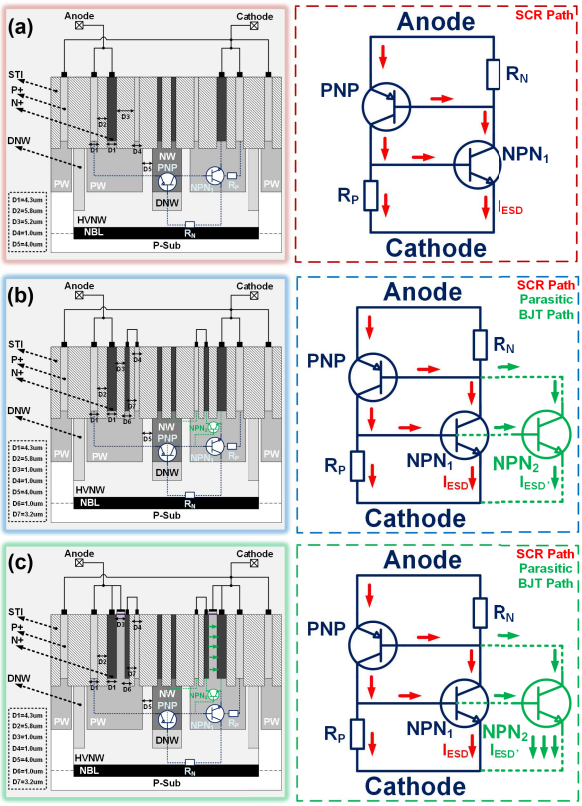

Fig. 1. Device structure and equivalent circuit of DDSCRs. (a) T_DDSCR. (b) NPN_DDSCR. (c) NPNE_DDSCR.

on the standard bipolar-CMOS–DMOS (BCD) process. The introduction of a floating P^+ injection region reduced the contribution of the parasitic NPN discharge path, thereby achieving a higher V_h. [21] verified that the DDSCR without N-type buried layer (NBL) has a slight degradation of V_h at high temperature. This is because the reverse-biased p-n junction formed by the low-doping concentration high-voltage N-well (HVNW) and the P-Sub is relatively more affected by the intrinsic excitation at high temperature. The asymmetric DDSCR (ADDSCR) proposed in [22] still faces challenges such as increased leakage and degradation of holding characteristics at high temperature. This is a common problem in SCRs dominated by the NPN path under high-temperature conditions [23], [24], [25]. Therefore, the development of high-performance DDSCRs is considered the preferred approach for efficient ESD protection of industrial communication buses [26], [27].

In response to the urgent need for efficient on-chip ESD protection in industrial communication buses, this article presents a parallel NPN-enhanced DDSCR employing metal shorting and without shallow trench isolation (STI) isolation. This structure can improve the inherently low holding characteristics of SCRs by combining a parallel shunt design with a parasitic NPN path enhancement strategy. This approach significantly suppresses the device's positive feedback effect and leads to a notable increase in both forward and reverse V_h. Under the premise that V_h of T_DDSCR and NPN_DDSCR cannot meet the holding window of the target chip, the NPNE_DDSCR device achieves a trigger voltage (V_{t1}) of 41.4 V and the snapback is only 3 V (38.4 V). In addition, NPNE_DDSCR can maintain leakage current at the nanoampere level even at high temperatures ranging from 50 °C to 125 °C, with no significant degradation in ESD characteristics. Its human body model (HBM) withstand voltage exceeds 8 kV, making it fully suitable for on-chip ESD protection in industrial communication buses.

II. Principle and Simulation of SCR

The cross section and critical dimensions of the traditional DDSCR are shown in Fig. 1(a). The T_DDSCR employs an HVNW and an NBL to enclose the active area and suppress the formation of substrate leakage paths. The floating P^+ (D4) regions at the anode and cathode are used to increase the P-well (PW) doping concentration (which serves as the base of the parasitic NPN_1). This reduces the emission efficiency of the parasitic NPN_1, thereby increasing V_h [20], [21]. The turn-on of T_DDSCR relies on the avalanche effect occurring at the PW/HVNW, deep N-well (DNW), and N-well (NW) junctions, which determines its dc BV and V_{t1}. When the ESD pulse reaches the anode of T_DDSCR, the avalanche carriers generate a voltage drop on the parasitic resistance R_N of the cathode N-type well region, which then turns on the parasitic PNP and starts to discharge the ESD current. The ESD current density distribution of the device was simulated using Sentaurus under a 5-mA injection condition. As shown in Fig. 2(a), the initial PNP discharge path is clearly observed. As the initial PNP path discharges ESD current gradually, a voltage drop is generated on the parasitic resistance R_P of Cathode PW, which then turns on parasitic NPN_1. At this time, T_DDSCR is fully turned on, forming a low-resistance PNPN path from Anode P^+ to Cathode N^+. Fig. 2(d) shows the complete SCR path and equivalent circuit of the device under a 2-A transmission line pulse (TLP) stress.

Under the premise of the same size, we introduced N^+ (D6) in the STI (D3) region of T_DDSCR and shortened it to P^+ (D4), that is, introduced the NPN_DDSCR with a parallel shunt path [Fig. 1(b)]. The conduction mechanism and initial PNP path of NPN_DDSCR [Fig. 2(b)] are exactly the same as those of T_DDSCR, but there are obvious differences in the complete SCR path and equivalent circuit of the two types of devices [Fig. 2(e)]. When the NPN_DDSCR is fully triggered, in addition to conduction through the main SCR path, the ESD current also flows to the N^+ (D6) via the metal short P^+ (D4). At this time, as the voltage drop of the parasitic resistance R_P of the Cathode PW is generated, the parasitic NPN_1 and NPN_2 in parallel will be turned on at the same time. The turning on of NPN_2 gradually shunts the main SCR path, thereby suppressing the positive feedback effect and increasing V_h. However, the ESD current of the parasitic NPN_2 in NPN_DDSCR still needs to bypass STI (D3) to be transmitted to Cathode N^+, which limits the shunting capability of the parasitic NPN_2. Therefore, to further improve V_h of the NPN_DDSCR, we enhance the shunting capability of the parasitic NPN_2 [Fig. 1(c)]. The NPNE_DDSCR replaces the STI (D3), which blocks parallel shunting, with a polysilicon

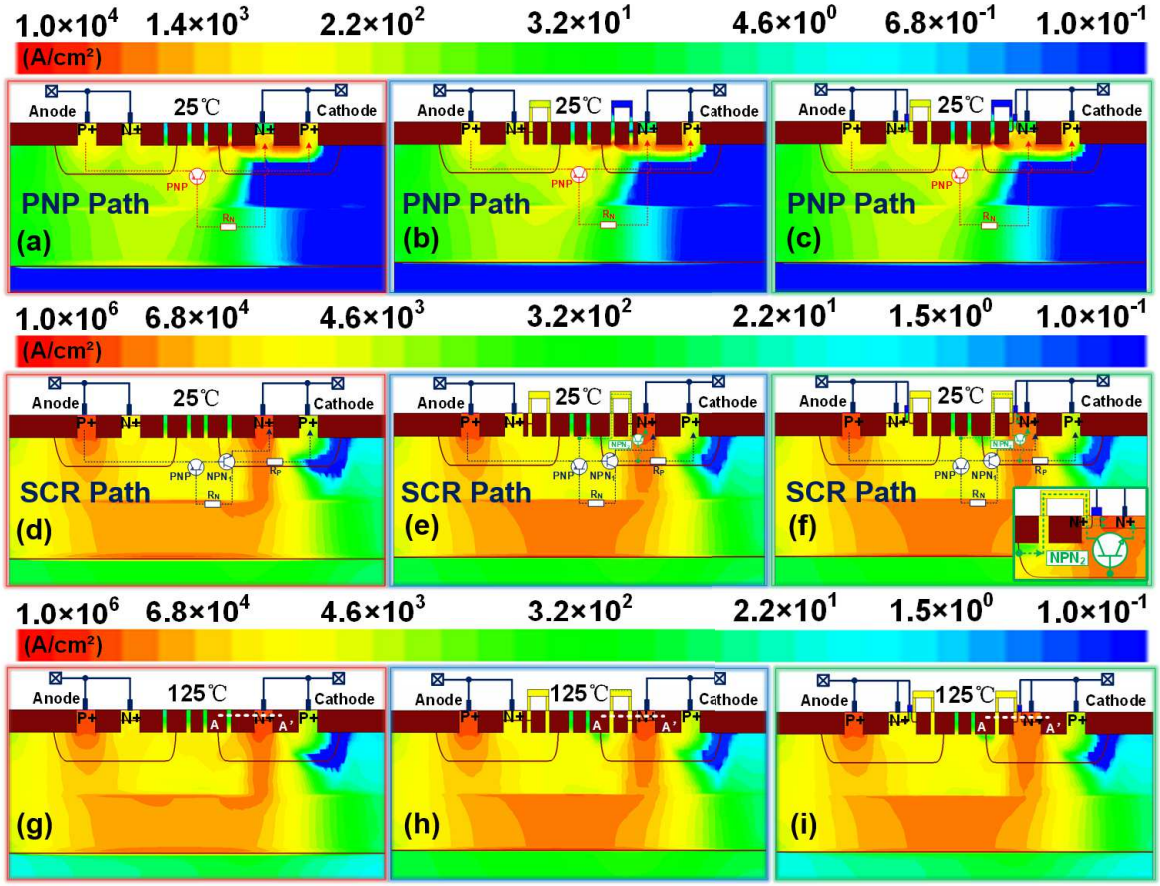

Fig. 2. TCAD simulations of DDSCRs. (a) PNP path of T_DDSCR (25 °C). (b) PNP path of NPN_DDSCR (25 °C). (c) PNP path of NPNE_DDSCR (25 °C). (d) SCR path of T_DDSCR (25 °C). (e) SCR path of NPN_DDSCR (25 °C). (f) SCR path of NPNE_DDSCR (25 °C). (g) SCR path of T_DDSCR (125 °C). (h) SCR path of NPN_DDSCR (125 °C). (i) SCR path of NPNE_DDSCR (125 °C).

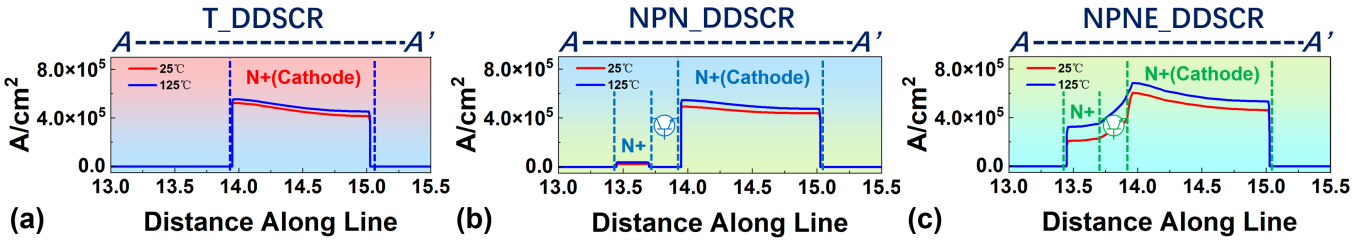

Fig. 3. One-dimensional tangential distribution of current density in SCR paths of DDSCRs at 25 °C and 125 °C along A-A'. (a) T_DDSCR. (b) NPN_DDSCR. (c) NPNE_DDSCR.

gate that is shorted to either the anode or cathode. Although the initial PNP path of the improved structure remains essentially unchanged [Fig. 2(c)], this approach significantly reduces the sheet resistance of the parasitic NPN_2 conduction path. The ESD current can flow directly from N^+ (D6) through the well region beneath the gate to the cathode N^+ [Fig. 2(f)]. Based on the above conduction mechanism, when the main SCR path and the parallel shunt NPN path coexist, the NPNE_DDSCR enhances the ESD current sharing through the parallel path and reduces the current density in the main SCR path, thereby maximizing V_h.

In addition, in order to further verify the high-temperature ESD characteristics of the above SCR structure, the 2-A TLP simulation results of T_DDSCR, NPN_DDSCR, and NPNE_DDSCR at 125 °C are shown in Fig. 2(g), (h), and (i), respectively. Through the 1-D tangent of the 2-D current density simulation results, it can be clearly found that the current density of T_DDSCR at 125 °C is slightly higher than that at 25 °C [Fig. 3(a)], which is consistent with the basic physical principle of intrinsic excitation enhancement at high temperatures. The current density of the parasitic NPN_2 path of NPN_DDSCR and NPNE_DDSCR also increased significantly at 125 °C, indicating that the parasitic parallel shunt effect of the two types of devices was also enhanced at high temperature [Fig. 3(b) and (c)]. Specifically, as the temperature increases, the intrinsic carrier concentration of the device increases, resulting in a decrease in the p-n junction barrier voltage, that is, the built-in potential of the emitter junction of the

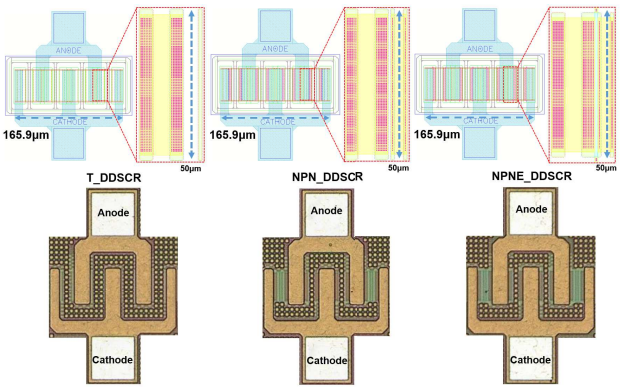

Fig. 4. Layout designs and microscope images of DDSCRs.

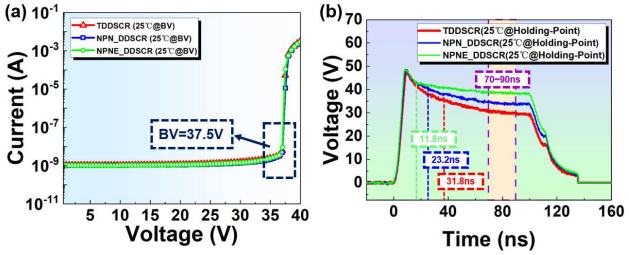

Fig. 5. Test results of DDSCRs at 25 °C. (a) DC curves. (b) Transient voltage curves.

parasitic NPN_2 decreases, and the emitter injection efficiency increases, thereby increasing the current share of the shunt path. The strengthening of the parasitic parallel shunt paths of NPN_DDSCR and NPNE_DDSCR can suppress the effect of high-temperature conditions on V_h degradation to a certain extent.

III. Results and Discussion

This article implements T_DDSCR, NPN_DDSCR, and NPNE_DDSCR devices of identical size (50-μm finger length with four fingers) based on a 0.18-μm BCD process. The layout designs and microscope images of the three types of DDSCR structures are shown in Fig. 4. We used the standard Thermo Scientific Celestron TLP test system to verify the dc, transient, and *I*–*V* characteristics of the three device types at temperatures of 25 °C, 50 °C, 75 °C, 100 °C, and 125 °C.

At room temperature (25 °C), the three structures have the same trigger surface and exhibit BVs of 37.5 V [Fig. 5(a)]. By extracting the transient voltage–time curve at the holding point, it is observed that T_DDSCR forms a single PNPN path, resulting in a relatively long clamping time of 31.8 ns (the clamping time is defined as the time difference between the voltage overshoot point and 1.1 times the average voltage from 70 to 90 ns). By introducing a parallel shunt path through the parasitic NPN_2, NPN_DDSCR accelerates the establishment of the SCR conduction loop and significantly reduces the clamping time to 23.2 ns. NPNE_DDSCR further enhances the current injection through the parasitic NPN_2, resulting in a shorter clamping time (11.8 ns) compared to that of the NPN_DDSCR [Fig. 5(b)]. The TLP *I*–*V* curves of T_DDSCR, NPN_DDSCR, and NPNE_DDSCR are shown in

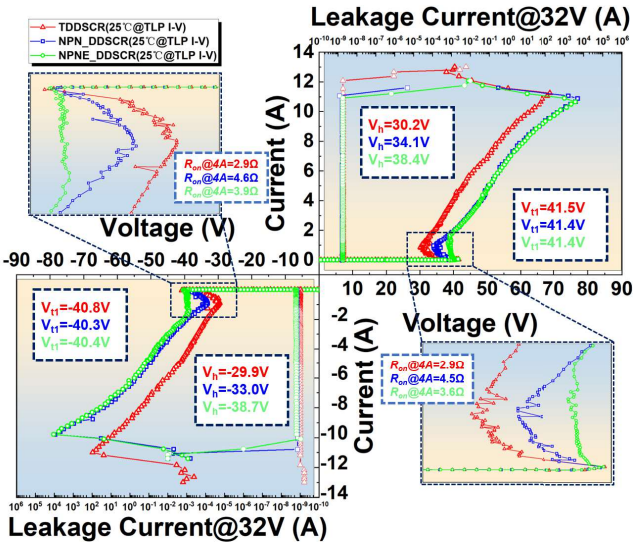

Fig. 6. TLP *I*–*V* curves of DDSCRs at 25 °C.

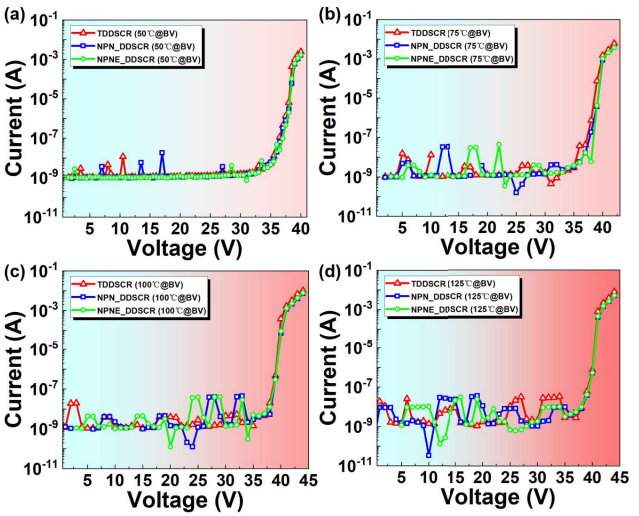

Fig. 7. DC curves of DDSCRs at (a) 50 °C, (b) 75 °C, (c) 100 °C, and (d) 125 °C.

Fig. 6. Clearly, the forward and reverse ESD characteristics of the three devices are symmetrical, and their trigger characteristics are consistent. However, differences exist in V_h and ON-resistance (R_{on}). Benefiting from the enhanced parasitic NPN_2 path, V_h of the NPNE_DDSCR is 38.4 V, which is 8.2 V higher than that of the T_DDSCR (30.2 V) and 4.3 V higher than that of the NPN_DDSCR (34.1 V). Since the increase in V_h for both NPN_DDSCR and NPNE_DDSCR relies on a parallel shunt path to suppress the positive feedback of the main SCR path, their R_{on} is slightly higher than that of the T_DDSCR. Based on the figure of merit (FoM) calculation formula [FoM = $(V_h \times I_{t2})/(V_{t1} \times S)$] [28], the FoMs for T_DDSCR, NPN_DDSCR, and NPNE_DDSCR are 1.06, 1.10, and 1.25 mA/μm^2, respectively. These results preliminarily confirm that NPNE_DDSCR offers superior ESD protection performance.

Figs. 7–9 show the dc characteristic curves, transient voltage curves, and TLP *I*–*V* curves of the three structures under a

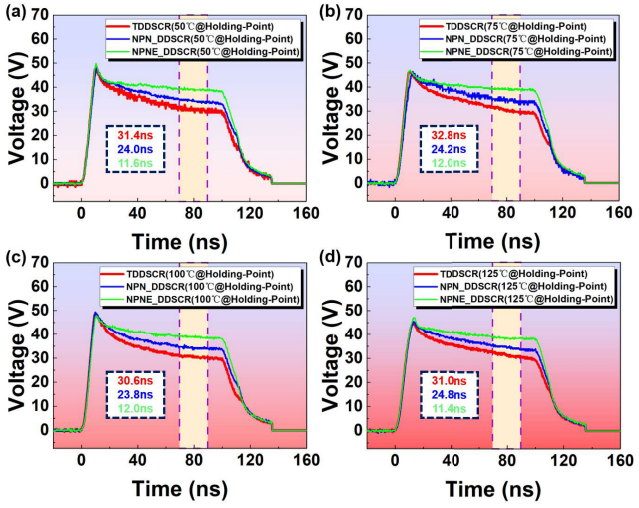

Fig. 8. Transient voltage curves of DDSCRs at (a) 50 °C, (b) 75 °C, (c) 100 °C, and (d) 125 °C.

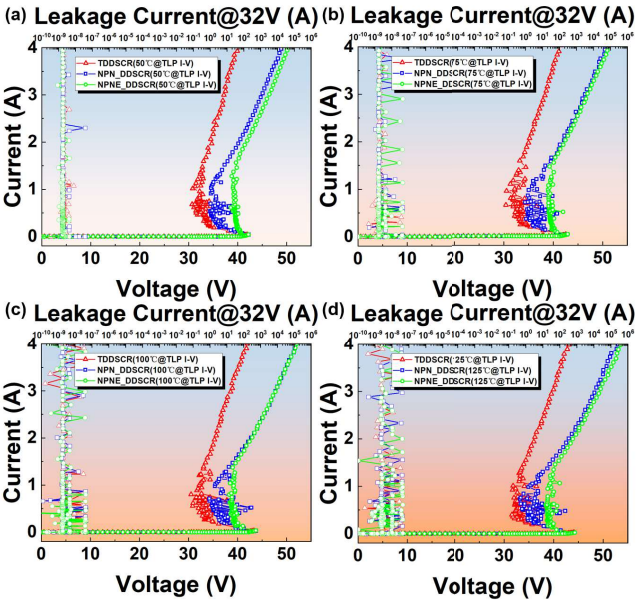

Fig. 9. TLP *I–V* curves of DDSCRs at (a) 50 °C, (b) 75 °C, (c) 100 °C, and (d) 125 °C.

TABLE I
PERFORMANCE COMPARISON OF T_DDSCR, NPN_DDSCR, AND NPNE_DDSCR (25 °C)

Device Name	BV (V)	V_{t1} (V)	V_h (V)	R_{on}@4A (Ω)	FoM (mA/μm²)
T_DDSCR	37.5	41.5	30.2	2.9	1.06
NPN_DDSCR	37.5	41.4	34.1	4.5	1.10
NPNE_DDSCR	37.5	41.4	38.4	3.6	1.25

current-limited condition of 4 A, across a temperature range from 50 °C to 125 °C. Fig. 10(a), (c), and (d) summarizes all the experimental data for the devices. The results show that the three types of DDSCRs exhibit nanoampere-level leakage current, stable transient voltage, and ESD characteristics without significant degradation at high temperature (the sample error is less than 1.5 V, which has little impact on

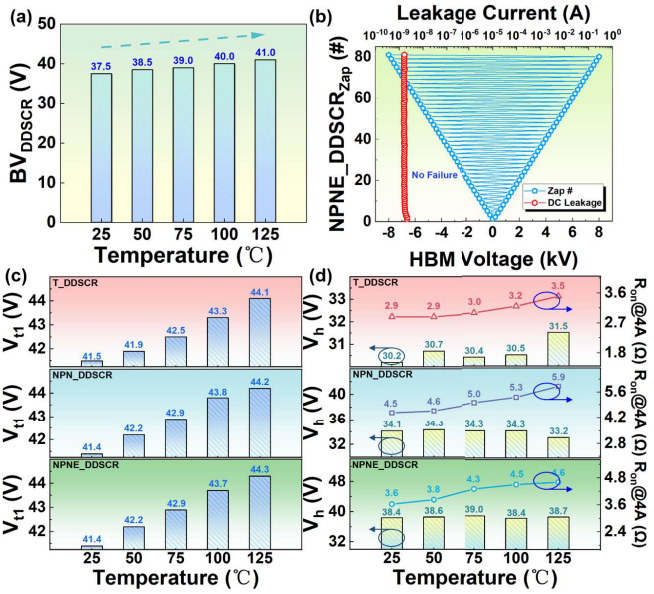

Fig. 10. Summary of data and HBM test results. (a) BV. (b) HBM test of NPNE_DDSCR. (c) Trigger voltage. (d) Holding voltage and ON-resistance.

TABLE II
PERFORMANCE COMPARISON OF T_DDSCR, NPN_DDSCR, AND NPNE_DDSCR (50 °C~125 °C)

Device Name	BV (V)	V_{t1} (V)	V_h (V)	R_{on}@4A (Ω)	Temp. (°C)
T_DDSCR	38.5	41.9	30.7	2.9	
NPN_DDSCR	38.5	42.2	34.3	4.6	50
NPNE_DDSCR	38.5	42.2	38.6	3.8	
T_DDSCR	39.0	42.5	30.4	3.0	
NPN_DDSCR	39.0	42.9	34.3	5.0	75
NPNE_DDSCR	39.0	42.9	39.0	4.3	
T_DDSCR	40.0	43.3	30.5	3.2	
NPN_DDSCR	40.0	43.8	34.3	5.3	100
NPNE_DDSCR	40.0	43.7	38.4	4.5	
T_DDSCR	41.0	44.1	31.5	3.5	
NPN_DDSCR	41.0	44.2	33.2	5.9	125
NPNE_DDSCR	41.0	44.3	38.7	4.6	

TABLE III
PERFORMANCE COMPARISON OF NPNE_DDSCR AND REFERENCE HIGH-VOLTAGE SCR

Device Name	BV (V)	V_{t1} (V)	V_h (V)	I_{t2} (A)	FoM (mA/μm²)
LDMOS-SCR [8]	-	42.3	8.3	10.7	0.32
HVSCR [14]	48.0	50.5	21.7	8.1	0.38
LRSCR [16]	-	9.8	5.9	5.7	1.09
DDSCR [17]	-	11.1	4.1	3.6	0.66
SDDSCR [19]	59.5	31.1	17.1	18.5	0.36
NPNE_DDSCR	37.5	41.4	38.4	11.2	1.25

the ESD protection evaluation of core chips for high-voltage and high-temperature applications). This is consistent with the technology computer-aided design (TCAD) simulation results under high-temperature conditions. Since the devices all have NBL with high doping concentration, their ESD characteristics are relatively less affected by intrinsic excitation at high temperature and can effectively block the leakage path and voltage clamp drift caused by thermal stress of the p-n junction between the well region and the substrate. Moreover, elevated temperatures increase lattice scattering in ESD

devices, which reduces carrier mobility and slightly raises both the BV, V_{t1}, and R_{on} [29]. Finally, the HBM test results of the NPNE_DDSCR are shown in Fig. 10(b). The device exhibits an HBM level exceeding 8 kV (no failure) while maintaining shallow snapback and high-temperature robustness at 125 °C, making it suitable for efficient on-chip ESD protection of industrial communication buses. Tables I and II summarize the data for T_DDSCR, NPN_DDSCR, and NPNE_DDSCR, while Table III compares the performance of NPNE_DDSCR with other SCR-based high-voltage ESD protection devices.

IV. Conclusion

This article presents a DDSCR with shallow snapback and high-temperature robustness, featuring a trigger voltage of 41.4 V, a holding voltage of 38.4 V, an ON-resistance of 3.6 Ω, and a figure of merit of 1.25 mA/μm^2. Under high-temperature conditions ranging from 50 °C to 125 °C, the device consistently maintains nanoampere-level leakage current, and its ESD characteristics exhibit no significant degradation. In summary, this structure offers an effective on-chip ESD protection solution for the reliability design of high-voltage industrial communication buses.

References

[1] Z. Qi et al., "Novel multifunctional transient voltage suppressor technology for modular EOS/ESD protection circuit designs," in *Proc. 35th Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, May 2023, pp. 72–75, doi: 10.1109/ISPSD57135.2023.10147403.

[2] J. Jeong, H. Kim, J. Park, J. Shin, and J. Jeong, "Compact and broadband ESD protection I/O pad using pad-stacked inductor," *IEEE Access*, vol. 11, pp. 11422–11429, 2023, doi: 10.1109/ACCESS.2023.3238323.

[3] M Monishmurali, N. K. Kranthi, G. Boselli, and M. Shrivastava, "Impact of thin-oxide gate on the ON-resistance of HV-PNP under ESD stress," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Mar. 2023, pp. 1–5, doi: 10.1109/IRPS48203.2023.10117638.

[4] L. Qian, H. Wang, Z. Dai, H. Yang, M. Li, and S. Hu, "Optimized PNP ESD protection device with adjustable trigger and holding voltages for high-voltage applications," *IEEE Trans. Electron Devices*, vol. 71, no. 6, pp. 3540–3545, Jun. 2024, doi: 10.1109/TED.2024.3392551.

[5] C.-Y. Ke and M.-D. Ker, "Investigation on ESD robustness of 20-V GGNMOS and GDPMOS in 4H-SiC process with 100-ns TLP pulse," in *Proc. IEEE 10th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Dec. 2023, pp. 1–5, doi: 10.1109/WIPDA58524.2023.10382191.

[6] P. Mahajan, S. Suresh, X. M. E. Low, K. J. Hwang, and R. Gauthier, "A robust scalable ESD protection device integrating drain side floating P+ diffusion with tunable ESD design window and effective latch-up immunity for high-voltage power clamp applications," in *Proc. 44th Annu. EOS/ESD Symp. (EOS/ESD)*, Sep. 2022, pp. 1–8, doi: 10.23919/EOS/ESD54763.2022.9928482.

[7] U. Y. Seo, S. W. Kwon, J. S. Gu, J. M. Lee, K. Y. Lee, and Y. S. Koo, "Development of diode triggering SCR-based ESD protection circuit with improved trigger voltage for low voltage application," in *Proc. Int. Conf. Electron., Inf., Commun. (ICEIC)*, Jan. 2024, pp. 1–3, doi: 10.1109/ICEIC61013.2024.10457205.

[8] M. Wu et al., "A radiation-hardened dual-direction SCR based on LDMOS for ESD protection in the extreme radiation environment," *IEEE Trans. Nucl. Sci.*, vol. 67, no. 4, pp. 708–715, Apr. 2020, doi: 10.1109/TNS.2020.2978766.

[9] X.-Y. Yang, S.-L. Chen, T.-E. Lin, H.-W. Chen, and Y.-M. Lee, "ESD/latch-up immunities enhancements of HV NLDMOSs by the embedded discrete SCR/Schottky alternating arrangement design at the drain side," in *Proc. Int. Conf. Consum. Electron.-Taiwan*, Jul. 2024, pp. 783–784, doi: 10.1109/ICCE-TAIWAN62264.2024.10674520.

[10] X.-Y. Yang, S.-L. Chen, T.-E. Lin, H.-W. Chen, and Y.-M. Lee, "ESD/Latch-up reliability enhancements of HV nLDMOSs by drain-end horizontally embedding different discrete P+ SCRs," in *Proc. 10th Int. Conf. Appl. Syst. Innov. (ICASI)*, Apr. 2024, pp. 1–2, doi: 10.1109/ICASI60819.2024.10547995.

[11] M. Goyal, M. Chaturvedi, H. Nath, M. Vaidya, and M. Shrivastava, "Novel trigger circuit & SCR device co-engineering based local (I/O-VSS & I/O-VDD) ESD clamp concepts with improved latch-up susceptibility, lower leakage and lower capacitance for ultra high speed I/Os," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Mar. 2025, pp. 1–8, doi: 10.1109/IRPS48204.2025.10983375.

[12] R. Chen et al., "Gate-controlled LVTSCR for high-voltage ESD protections in advanced CMOS processes," *IEEE Trans. Electron Devices*, vol. 70, no. 4, pp. 1566–1573, Apr. 2023, doi: 10.1109/TED.2023.3244765.

[13] W. Song et al., "Robust silicon-controlled rectifier with high-holding voltage for on-chip electrostatic protection," *IEEE Trans. Electron Devices*, vol. 69, no. 2, pp. 696–703, Feb. 2022, doi: 10.1109/TED.2021.3131536.

[14] C.-T. Dai and M.-D. Ker, "Comparison between high-holding-voltage SCR and stacked low-voltage devices for ESD protection in high-voltage applications," *IEEE Trans. Electron Devices*, vol. 65, no. 2, pp. 798–802, Feb. 2018, doi: 10.1109/TED.2017.2785121.

[15] C.-T. Dai and M.-D. Ker, "ESD protection design with stacked high-holding-voltage SCR for high-voltage pins in a battery-monitoring IC," *IEEE Trans. Electron Devices*, vol. 63, no. 5, pp. 1996–2002, May 2016, doi: 10.1109/TED.2016.2544382.

[16] K.-I. Do and Y.-S. Koo, "A new SCR structure with high holding voltage and low ON-resistance for 5-V applications," *IEEE Trans. Electron Devices*, vol. 67, no. 3, pp. 1052–1058, Mar. 2020, doi: 10.1109/TED.2020.2963994.

[17] H. Liang et al., "A novel dual-direction SCR embedded with segmental and cross-bridge topology for high-voltage ESD protection," *IEEE Trans. Electron Devices*, vol. 70, no. 8, pp. 4036–4042, Aug. 2023, doi: 10.1109/TED.2023.3284416.

[18] J. Bourgeat, Y. Solaro, and N. Guitard, "ESD protection based on stacked SCRs with adjustable triggering voltage for CMOS high-voltage application," in *Proc. 44th Annu. EOS/ESD Symp. (EOS/ESD)*, vol. 44, Sep. 2022, pp. 1–6, doi: 10.23919/EOS/ESD54763.2022.9928468.

[19] Y. Wang, Z. Zhong, X. Jin, and Y. Wang, "A high-voltage dual direction silicon-controlled rectifier based on flexible stacking strategy," *IEEE Trans. Electron Devices*, vol. 72, no. 4, pp. 2086–2089, Apr. 2025, doi: 10.1109/TED.2025.3544975.

[20] Z. Deng, Y. Wang, Y. Zhang, B. Yu, W. Guan, and H. Yang, "ESD characteristics improving for DDSCR with NBL by adding high voltage N-type well isolation in 0.18-μm BCD technology," in *Proc. 10th Int. Symp. Next-Gener. Electron. (ISNE)*, May 2023, pp. 1–3, doi: 10.1109/isne56211.2023.10221621.

[21] X. Bao, Y. Wang, Y. Liu, and X. Jin, "Design and manufacture of dual-gate DDSCR with high failure current and holding voltage," *Chin. J. Electr. Eng.*, vol. 10, no. 2, pp. 116–125, Jun. 2024, doi: 10.23919/cjee.2024.000061.

[22] X. Chen, Y. Wang, X. Jin, Z. Zhou, J. Lu, and D. Jia, "An ESD robust high holding voltage dual-direction SCR with symmetrical I-V curve by inserting a floating P+ in PWell," *Solid-State Electron.*, vol. 160, Oct. 2019, Art. no. 107627, doi: 10.1016/j.sse.2019.107627.

[23] W. Liang et al., "Characteristics of ESD protection devices operated under elevated temperatures," in *Proc. IEEE Int. Nanoelectronics Conf. (INEC)*, May 2016, pp. 1–2, doi: 10.1109/INEC.2016.7589442.

[24] Z. Yu, H. Jin, S. Dong, H. Wong, J. Zeng, and W. Wang, "Comparative study of reliability degradation behaviors of LDMOS and LDMOS-SCR ESD protection devices," *Microelectron. Rel.*, vol. 61, pp. 111–114, Jun. 2016, doi: 10.1016/j.microrel.2015.12.024.

[25] M. Shrivastava and H. Gossner, "A review on the ESD robustness of drain-extended MOS devices," *IEEE Trans. Device Mater. Rel.*, vol. 12, no. 4, pp. 615–625, Dec. 2012, doi: 10.1109/TDMR.2012.2220358.

[26] F. B. Du et al., "Layout optimization of dual-directional scr for holding voltage equilibrium in ESD applications," *IEEE Trans. Electron Devices*, vol. 72, no. 6, pp. 2783–2788, Jun. 2025, doi: 10.1109/TED.2025.3558487.

[27] L. Qian et al., "A novel segmented LDMOS-SCR structure with 8-kV HBM ESD robustness in CMOS analog multiplexer," *IEEE Trans. Electron Devices*, vol. 69, no. 12, pp. 6904–6909, Dec. 2022, doi: 10.1109/TED.2022.3211913.

[28] A. Amerasekera and C. Duvvury, *SD in Silicon Integrated Circuits*, 2nd ed., Hoboken, NJ, USA: Wiley, 2002, doi: 10.1002/0470846054.

[29] K.-I. Do, J.-W. Jung, J. Song, and C.-H. Jeon, "Design of dual-directional SCR structure with high holding voltage and low dynamic resistance for high voltage ESD protection," *IEEE Trans. Electron Devices*, vol. 70, no. 9, pp. 4509–4517, Sep. 2023, doi: 10.1109/TED.2023.3294351.