

Analog Front-End Input-Impedance Boosting Techniques for Bio-Potential Monitoring—A Review

Feng Yan[✉], *Graduate Student Member, IEEE*, and Jingjing Liu[✉], *Member, IEEE*

Abstract—Physiological information provided by bio-potential signals is essential and pivotal for biomedical sensors. As the first stage in the signal chain of the sensor, impedance matching of the analog front-end (AFE) is critical for determining signal integrity. AFEs require high input impedance to minimize the effects of electrode impedance mismatch. A significant problem is that the input impedance is affected by parasitic capacitances from the integrated circuit (IC) package, electrode cables, and internal chips. This article aims to summarize the development of AFE impedance-boosting techniques for bio-potential monitoring. The scope of this work includes a review of common architectures for instrumentation amplifiers (IA), mechanisms for input impedance reduction, and a comparison of impedance boosting factors (IBF) employed to evaluate the efficiency of impedance enhancement. Techniques schemes for boosting input impedance in architectures are then surveyed and the contributions and drawbacks of these techniques are discussed. Finally, the state-of-the-art designs of AFE are compared and summarized, along with an analysis of the trend toward enhanced input impedance in bio-electrical signal acquisition. These provide useful references for AFE designers.

Index Terms—Analog front-end (AFE), bio-electrical signal acquisition, impedance boosting factors (IBF), impedance matching, instrumentation amplifiers (IA).

I. INTRODUCTION

LOW-FREQUENCY (about dc–10 kHz) and low-amplitude (about 0–10 mV) bio-potential signals contain a lot of valuable physiological information [1], which can be used in many applications such as biomedical sensors, wearable electronics, and neural signal monitoring. Analog front ends (AFEs) that detect and record bio-potentials in the form of electrocardiography (ECG) [2], [3], electroencephalography (EEG) [4], electromyography (EMG) [5], electroretinography (ERG) [6], and neurostimulation [7], are indispensable and vitals tools in the field of medical and research. Fig. 1 illustrates the concept of instrumentation amplifiers (IAs) acquiring bio-potential signals from the human body. Table I shows the

Manuscript received 3 September 2023; revised 5 December 2023; accepted 11 January 2024. Date of publication 27 February 2024; date of current version 7 March 2024. This work was supported in part by the National Natural Science Foundation of China under Project 62174181. The Associate Editor coordinating the review process was Dr. Anoop Chandrika Sreekantan. (*Corresponding author: Jingjing Liu*)

The authors are with the School of Electronics and Communication Engineering, Sun Yat-sen University, Shenzhen 518107, China (e-mail: yanf9@mail2.sysu.edu.cn; liujj77@mail.sysu.edu.cn).

Digital Object Identifier 10.1109/TIM.2024.3370766

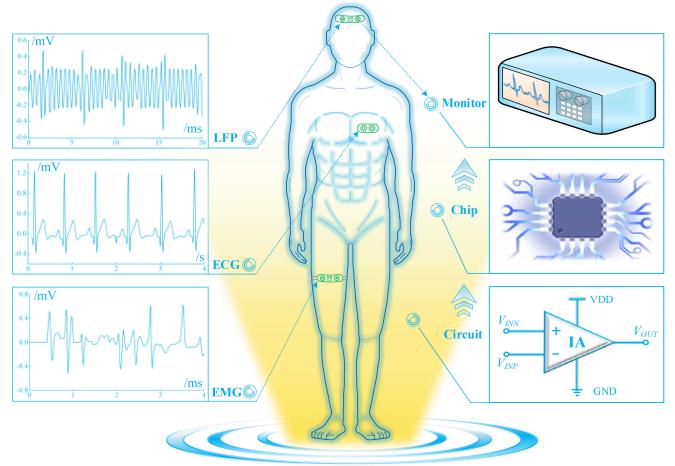


Fig. 1. Concept of IAs acquiring bio-electrical signals from the human body. The green graphics on the body represent wearable devices. The left is common local field potentials, ECG, and EMG, and the right is a bio-potential monitor composed of an IA chip.

TABLE I
TYPICAL BIO-SIGNAL CHARACTERISTICS

Bio-potential signals	Frequencies (Hz)	Amplitudes (mV)
Electrocardiography (ECG)	0.05–100	0.5–5
Electroencephalography (EEG)	0.5–100	0.01–0.1
Electromyography (EMG)	DC–500	< 10
Electrooculography (EOG)	0.1–50	0.05–3.5
Action Potential (AP)	300–7500	0.005–0.05
Local Field Potentials (LFP)	0.025–100	1–10

frequency and amplitude of typical bioelectric signals [8]. To a great extent, the input impedance of AFE determines the signal quality by distributing the voltage from the signal source. In pursuit of procuring high-fidelity physiological signals, the AFE demands a large and stable input impedance.

With the growing awareness of wearable health monitoring [9], [10], bio-signal acquisition integrated circuits (ICs) for ExG (i.e., ECG, EEG, EMG, ERG, and EOG) have gained much interest over the past decade [11], [12], [13]. The brief lifespan of the conductive gel utilized in wet electrodes and

them unsuitable for everyday wearable applications. Most of the wearable devices developed to employ dry electrodes [14], [15] as the interface between sensors and the human body [16], as they can provide a better user experience than wet electrodes in terms of convenience and durability. Generally, the contact impedance characteristics of dry electrodes can be represented by an impedance model of $1 \text{ M}\Omega||10 \text{ nF}$ [17], with the dc impedance being one order of magnitude higher compared to wet electrodes. Dry electrode technology can acquire bioelectrical signals without the need for gels, adhesives, and even direct skin contact [18], [19]. However, this complicates the measurement of bio-potentials, since IAs with dry electrodes require very high input impedance. Dry electrodes clearly include some design challenges for the development of AFE circuits. One of the most important points is that dry electrodes have higher skin/electrode impedance [20], [21], [22], and the input impedance of the readout circuit needs to be increased to match dry electrodes to achieve high common-mode rejection ratio (CMRR), noise immunity, and contact change resilience.

Undoubtedly, recording the electrical activity of neurons has been a crucial step for decoding brain function [23]. These recordings are indispensable for understanding and diagnosing neurological disorders like epileptic seizures [24], in the creation of brain-machine interfaces [25] and for neuromodulatory technologies to aid paralyzed patients [26], [27]. Within neural recording systems, the AFE forms the critical element for signal detection and preprocessing. The neural recording amplifier in the system has stringent area and power constraints due to the large number of recording channels required [28]. With that in mind, many micro-electrodes form a voltage divider at the input of the IA, which necessarily attenuates the received neural signals. Graphene FET active electrode (AE) arrays have a slight advantage in wire count limitation [29], [30]. Yet, the input impedance of various types of microelectrodes is usually limited to the range of $100 \text{ k}\Omega\text{--}6 \text{ M}\Omega$ at 1 kHz [31]. The resulting input attenuation can significantly degrade the output signal accuracy. At the same time, due to the problem of tissue fibrosis [32], the input impedance of the amplifier is further attenuated, and the effective CMRR is reduced, which limits the performance of subsequent modules.

These challenges and limitations have encouraged research of technique schemes that can increase the total input impedance. In order to acquire high-quality bioelectrical signals by AFE, a variety of solutions ranging from AE design [33], [34], [35], [36] to the subsequent IA design [37], [38], [39], [40], [41] have been proposed. It has become a hot topic in recent years. A few design schemes are mentioned in [42], however, the main challenges in impedance boosting techniques, such as the underlying factors causing impedance attenuation, trade-offs in performance parameters, and techniques for enhancing common-mode (CM) input impedance, have not been fully summarized. This article specifically reviews and summarizes various enhancement techniques of input impedance in AFE.

The rest of the section is organized as follows. Section II briefly introduces the commonly used IA architectures in AFEs and discusses their input impedance characteristics. Section III

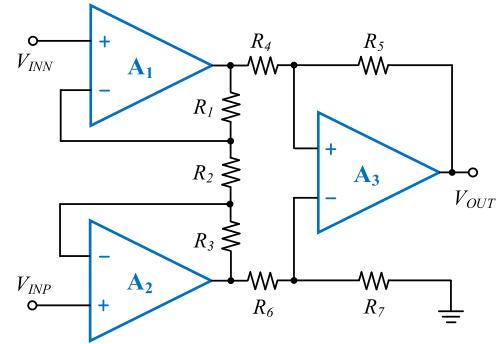


Fig. 2. Traditional three-op-amp AFE architecture.

presents a generic contact model of the bio-potential sensor, which helps analyze the cause of input impedance attenuation at the AFE. Interesting technique solutions for increasing the input impedance are discussed in Section IV, including differential-mode input impedance and CM input impedance. The article concludes with a discussion of the latest developments in boosting input impedance along with future research directions and challenges.

II. OVERVIEW OF IA ARCHITECTURE

In past research, there have been a large number of publications on the bioelectrical signal recording front-end circuits. As shown in Fig. 2, the traditional three-op-amp AFE architecture usually consists of two stages, and the gain can be adjusted through external resistors [43]. Proper design of the first-stage amplifier can achieve high input impedance [44], [45] and satisfactory CMRR. The CM rejection of the second stage is determined by the mismatch of the resistor network. In fact, the load driven by the three-op-amp structure is resistive, which brings an intuitive impact that the required power consumption is increased. Since the bioelectrical signal is dc-coupled to the amplifier, its gain needs to be set low to prevent electrode offset from saturating the IA output [46]. Current feedback IA (CFIA) architecture consumes less power by sharing the output stage and also has the advantage of high input impedance [47], [48], [49], [50]. The CFIA uses two identical converters to convert the input and feedback voltages, respectively [51]. Its gain is related to the ratio of the transconductance of the two converters. Inevitably, the mismatch between the two transconductances affects the gain accuracy of the IA. A current balanced IA (CBIA) architecture consists of an input stage transconductance and an output stage transconductance, and does not suffer from this problem [52], [53]. Although power regulation can enhance the CMRR of CBIA [54], additional supply regulators are required and less efficient for systems with small channel counts.

Capacitively coupled IA (CCIA) architecture [55], [56], [57], [58] is a commonly used topology in AFE, which consists of an operational transconductance amplifier (OTA) and a passive resistor-capacitor network. The capacitively coupled topology ensures high input impedance and rail-to-rail electrode dc offset (EDO) rejection [59] with negligible signal attenuation at the electrodes when the input capacitance

is set to less than 100 pF. However, the impact of the way passive filters are added to the OTA inputs is not negligible. High-quality capacitors that are low-noise, low-parasitic, and stable must be selected to avoid introducing new noise and errors and adding undesired impedance variations. It is well known that many bioelectrical signals have distributions in the frequency range below 1 Hz, therefore, IA needs to achieve a low high-pass corner frequency F_{HPF} (for EEG signals, it is usually 0.5 Hz). The size of the capacitor in the passive resistor–capacitor network does not occupy too much on-chip area due to the limitation of full-chip integration [60]. From the published works, it seems that their capacitance is generally in the order of several fF to tens of pF. Using a pseudo-resistor with a very large resistance value is an area-effective way to achieve an extremely low F_{HPF} , which can be realized through a MOS transistor topology [11], [61], switched capacitors [62], or switched resistors [26], [63]. It is worth noting that the nonlinearity of pseudo-resistors limits the linearity of the sensor front-end to 8 bits [64] while being very sensitive to process and temperature. Any bulk leakage current in the pseudo-resistor can cause huge dc bias shifts, leading to poor control of bias points in the AFE.

Auto-zeroing (AZ) and chopping techniques are used to improve the trade-off between high input impedance and low noise [65]. The AZ technique samples the amplifier offset periodically rather than applying it continuously to the input signal. Although this sampling operation has a negligible effect on the overall input impedance due to the slight load generated, the sample-and-hold principle makes the AZ amplifier susceptible to noise aliasing. A chopper-stabilized (CS)-CCIA architecture with a chopper added to a CCIA is another popular AFE topology for bio-potential signal acquisition applications [66], [67], [68], [69]. Based on the time domain analysis, it can be concluded that the chopping modulation is actually the operation of multiplying the input by the square wave signal. Low-frequency errors including low-frequency drift and flicker noise are modulated and filtered out along with the input offset. Adding a chopper is an effective way to achieve low noise and low offset of the amplifier at the same time. It can improve the system's total CMRR (TCMRR) [40], noise efficiency factor (NEF) [70], [71], and power efficiency factor (PEF) [72], [73]. Since chopping modulation essentially separates the low-frequency noise from the input signal on the spectrum and then filters it out, it cannot absolutely eliminate the noise and inevitably introduce output ripple. The IA architectures that employ chopping require various ripple reduction loops (RRL) to mitigate the effects of ripple [67], [74], [75], [76]. What is more, the passive mixer at the input combined with the input capacitance forms a switched-capacitor resistance, which is inversely proportional to the chopping frequency and results in a lower input impedance and a significant attenuation of the signal amplitude.

Each type of IA architecture possesses unique advantages and limitations due to its inherent topology. Without adding any enhancement techniques, dc-coupled IA architectures have higher input impedance than capacitively coupled IAs. The dc-coupled IA utilizes transistors as input stages instead of

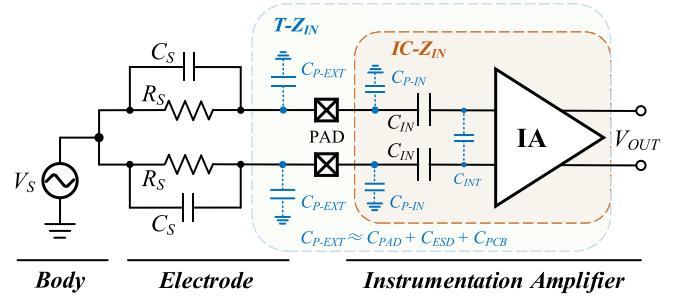


Fig. 3. Circuit model of the contact impedance between the electrode interface and the IA of AFE, including parasitic capacitance.

capacitors [77], thereby enabling a more intuitive realization of high input impedance, especially with a thick-oxide input transistor. However, this IA architecture requires paying attention to amplifier saturation caused by electrode offset. The ac-coupled IA [78], [79] can achieve higher input impedance through various topologies, albeit at the cost of introducing additional circuitry, which inevitably increases noise, power consumption, and design complexity. Designers of AFEs need to achieve an excellent trade-off between input impedance, EDO rejection, noise, power consumption, and chip area.

III. ANALYSIS OF AFE INPUT IMPEDANCE

Before delving into the details of circuit techniques for boosting the input impedance, it is necessary to address the design considerations for bioelectrical signal sensors. One of the difficulties is constructing the measurement of the impedance interface in the AFE [33]. Fig. 3 depicts a general circuit model of the bioelectric signal sensor front-end. The electrical signal from the body is modeled as a voltage source V_S and it is coupled to the sensor front-end through a parallel coupling resistor R_S (typically ranging from 1 GΩ to infinity, depending on the material of the interface and whether there exists an air gap) and coupling capacitor C_S (typically ranging from 10 pF to 200 nF) [38]. R_S and C_S form a variable electrode contact impedance up to the GΩ range for bio-signals <10 Hz [80], [81]. Due to the large electrode contact impedance, too small an AFE input impedance can cause a serious mismatch of electrode impedance, reduced CMRR, and increased power supply interference to the signal acquisition system [82]. Therefore, the input impedance in the chip ($IC-Z_{IN}$) is often designed to be much larger than the electrode contact impedance [39].

The parasitics before the IA chip absorb the bioelectrical signals generated by the body and so attenuates the useful information collected by the AFE [83]. As seen in Fig. 3, the total input impedance ($T-Z_{IN}$) of the AFE is limited by off-chip parasitics, chip I/O parasitics, on-chip parasitics, and the input impedance of the core circuit. Off-chip parasitics consist mainly of the signal lines from the chip pins to the electrodes. The size of parasitic capacitance depends on the length of the chip's external traces and the distance of the nearby metals, and its value typically ranges from a few hundred fF to tens of pF [37]. Chip I/O parasitics usually come from the parasitic capacitance of PCB, PAD, and on-chip electrostatic discharge (ESD). On-chip parasitics include the parasitic capacitance

(C_{IN}) [84] of the amplifier input nodes and other node parasitics in the chip. These parasitics may cause signal loss, phase shift, and circuit instability, which is also the reason for the narrowing of the operating frequency band of the amplifier, especially in the case of high frequency and large gain.

It should be particularly concerned that although the chopper stabilization technique can alleviate the flicker noise of AFE [85], the charge injection introduced by the chopper leads to measurement errors and performance degradation of IA. Since the chopper is placed before the input capacitor, the low input impedance of the CS-CCIA structure is primarily due to the chopper periodically charging and discharging the input capacitor. The average value of transient currents at this moment manifests as the input current that limits the equivalent $T - Z_{IN}$ of the IA. The total input impedance of CS-CCIA can be expressed as follows:

$$T - Z_{IN} = \frac{1}{s(C_{IN} + C_P)} \approx \frac{1}{2 \cdot F_{CH} \cdot (C_{IN} + C_P)} \quad (1)$$

where C_P is the total parasitic capacitance at the input of the front-end amplifier and F_{CH} is the operating frequency of the chopper. Equation (1) describes a switched-capacitor equivalent resistance. It manifests that the input impedance exhibits an inverse relationship with the magnitude of the input capacitance as well as the frequency of the chopping signal. The input impedance given by (1) can be increased by decreasing the chopper frequency [85] or the area of the input device, i.e., C_{IN} or C_P . In fact, C_{IN} should be large enough to minimize the overall system noise and closed-loop gain error arising from parasitic capacitance. However, an excessively large C_{IN} would decrease the input impedance [66], [86]. Also, F_{CH} should be much higher than the corner frequency F_{HPF} (i.e., the intersection of flicker noise and thermal noise) to mitigate residual flicker noise, which further reduces the input impedance [87]. For typical input capacitance values and chopper frequency, Z_{IN} could be reduced to below 1 MΩ. This would accelerate electrode aging and attenuate the bio-potential signal, thus degrading the signal-noise ratio (SNR), which counteracts the initial effort for improved performance.

Due to the characteristics of various IA architectures and technical schemes, the absolute value of the obtained enhanced impedance varies greatly [88]. In order to estimate the effective input impedance, it is necessary to establish an input impedance boost factor (IBF) [89]. This technical indicator shows the improvement capability of impedance enhancement schemes on the original IA architecture. IBF can be expressed as follows:

$$IBF = \frac{T - Z'_{IN}}{T - Z_{IN}} \quad (2)$$

where $T - Z'_{IN}$ is the total input impedance with impedance boost and $T - Z_{IN}$ is the total input impedance without impedance boost. The next section will discuss the detailed techniques for enhancing the input impedance.

IV. TECHNICAL SCHEMES OF INPUT IMPEDANCE BOOSTING

The large input impedance allows the input of the IA to obtain a large signal voltage from the signal source, which

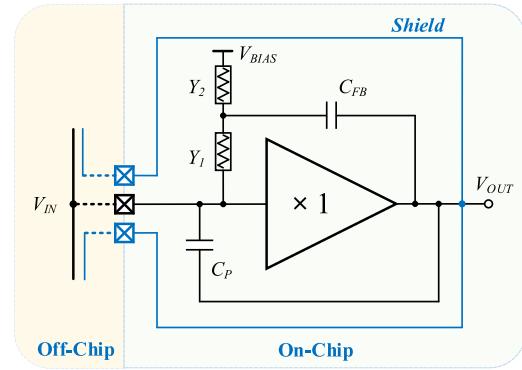


Fig. 4. Classic structure of AS technique [33].

means less attenuation of the bioelectric signal [90]. The entirely discrete component-built IA in [91] has >10 GΩ input impedance, which meets the relevant standards set forth by the International Electrotechnical Commission (IEC) 60601 [92]. The AFE built using a PCB prototype is merely an attempt and full-chip integration is an inevitable trend. The utilization of off-chip coupling capacitors could be employed to augment the dc input impedance [93]. Nevertheless, it is impractical for highly miniaturized implants encompassing a vast number of recording channels. Therefore, a fully chip-integrated technique scheme for impedance enhancement has become a major design requirement.

A. Active Shield Technique

Active shield (AS) constitutes an efficient technique for mitigating trace parasitics at the PCB board. This technique reduces signal-to-ground parasitics by protecting the signal lines by encompassing them in a shield [94]. The input of the sensor front-end is a MOS transistor, i.e., its input impedance is capacitive [33]. The block diagram of a dc-coupled sensor front-end using AS is shown in Fig. 4. The principle of this technique is that the unity-gain amplifier uses virtual short ($V_{OUT} \approx V_{IN}$) of the op-amp to bootstraps the parasitic input capacitance C_P and keeps a constant voltage. The output of the unity-gain amplifier V_{OUT} drives a shield to achieve the active shielding, which encompasses the input leads on the silicon chip, pads, and bonding wires from the sensor electrodes to the IC on the PCB. To minimize the unshielded bonding wire capacitance as much as possible, the V_{IN} PAD is surrounded on both sides by V_{OUT} PADs. Concurrently, the dc operating point of the circuit is established by connecting MOS pseudo-resistors Y_1 and Y_2 in series between V_{IN} and bias voltage V_{BIAS} .

Conventionally, the unit gain buffer is used to neutralize the input parasitic capacitance at differential nodes and the external parasitic capacitance at electrodes through the AS [34], [35]. Based on the AS technique, the work in [36] reduces the load applied to the input by adding a local source follower in the chopper, which can keep the voltage across the parasitic capacitor at the input differential pair constant. In this way, the input impedance is maximized to 6.7 GΩ at 50 Hz with an equivalent input capacitance of 0.47 pF. Active shielding techniques can mitigate the external

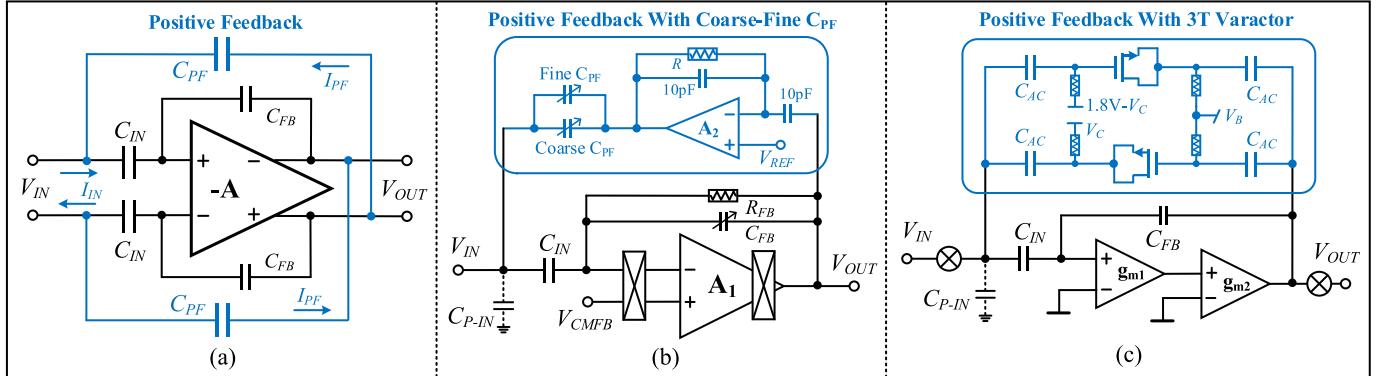


Fig. 5. Positive feedback technique of (a) traditional structure [67], (b) coarse and fine adjustment capacitor array [89], and (c) three-terminal variable capacitor [6].

parasitic capacitance and achieve a $T - Z_{IN}$ over $T\Omega$ (at the high-pass corner frequency) [33]. A dc-coupled AE [95] and an elaborately devised two-stage ESD are jointly employed to boost the input impedance of IA at lower frequencies only [96]. The reason for this is that any noise picked up by the shield is amplified at higher frequencies, reducing the signal-to-noise ratio. While this achieves rail-to-rail EDO rejection, unfortunately, the intrinsic input parasitic capacitance of the OTA itself could not be dispelled and the robustness of the ESD is compromised.

B. Positive Feedback Technique

For reducing on-chip parasitics, one of the feasible methods is the positive feedback loop (PFL) technique. Fig. 5(a) demonstrates the PFL technique for boosting the input impedance. The PFL is driven by the output V_{OUT} , and the capacitor C_{PF} can be regarded as a negative capacitor [97] C_{NEG} at the input node of the amplifier by the Miller Theorem. C_{NEG} is expressed as follows:

$$C_{NEG} = (1 - A)C_{PF} \quad (3)$$

where A is the gain of the amplifier and it is much larger than 1. The summation of the negative capacitance C_{NEG} at the input node diminishes the input parasitic capacitance and ultimately enhances the input impedance of the IA [67]. Analyzed from the perspective of current flow, the PFL uses the current I_{PF} from the output to charge/discharge C_P , thus reducing the draw from the current I_{IN} and increasing the $IC_{Z_{IN}}$.

This technique scheme requires an accurate design of both the amplifier gain and the capacitance C_{PF} so that C_{NEG} can be close to the parasitic capacitance of the actual chip as much as possible [98]. High impedance can be obtained over a wide range by precise capacitance matching [99]. Precise matching can be achieved by fine-tuning, and a number of excellent methods have been proposed. In [18], the positive feedback path for input impedance boosting is implemented through a 4-bit fine-impedance boosting loop (FIBL) to avoid the capacitive mismatch caused by the chip fabrication. In [89], the partial PFL is implemented as an ac-coupled inverting amplifier in series with a parallel array of coarse-fine tuning capacitors, as shown in Fig. 5(b). The coarse C_{PF} loop is

trimmed according to the variable C_{FB} to compensate for C_{IN} , while the fine C_{PF} loop is adjusted to eliminate C_{P-IN} . The input impedance is reported as over 2 GΩ at 1 Hz after two-step manual calibration. Scaling down C_{IN} and C_{PF} proportionally can achieve a higher input impedance without sacrificing the mid-band gain of IA. One feasible approach is to replace the C_{FB} in the feedback path of the chopper amplifier with the intrinsic parasitic gate-drain capacitance C_{gd} of the amplifier input transistor. Therefore, scaling down the input capacitance can directly achieve an input impedance boosting [31], [100]. An interesting scheme to improve the calibration resolution of C_{FB} and eventually the IBF is presented in [6], which introduces three-terminal (3T) varactors as a trimming capacitor in the PFL. As depicted in Fig. 5(c), two varactors controlled by the external voltages V_C and V_B , are inversely connected in parallel to provide tiny capacitance for trimming. A large IBF of 370 is achieved and the measured input impedance from 0.1 to 10 Hz is 1.5 GΩ with the F_{CH} of 10 kHz.

Another appealing approach is to make the input impedance independent of the voltage gain of IA. Conventional PFLs require reconfiguration of the positive feedback capacitor C_{PF} to accommodate different gains. The work in [101] implemented a local PFL (LPFL) which decouples its loop gain from the voltage gain of IA, thereby providing another degree of freedom to compensate C_{P-IN} . This work utilizes an inherently low-capacitance current-balanced architecture [102] as the input stage of the IA. LPFL is used to eliminate the C_{gd} of the input pair transistors and the layout parasitic capacitances in CFIA. Ultimately, the chopper CFIA exhibits the minimal input impedance of 1.8 GΩ at 5 Hz. Admittedly, the prototype IC is implemented in a 0.18 μm CMOS process and consumes 5.35 mW of energy. It is of interest to designers that LPFL-based impedance enhancement techniques in CFIA can also be applied to CS op-amps. However, it should not be overlooked that positive feedback for high input impedance may result in excessive phase shift at high frequencies, potentially causing oscillation or ringing.

C. Dynamic Element Matching Technique

From the perspective of the input electrodes, in order to make the chopper-coupled capacitive amplifier have an extremely high input impedance, one way is to boost the

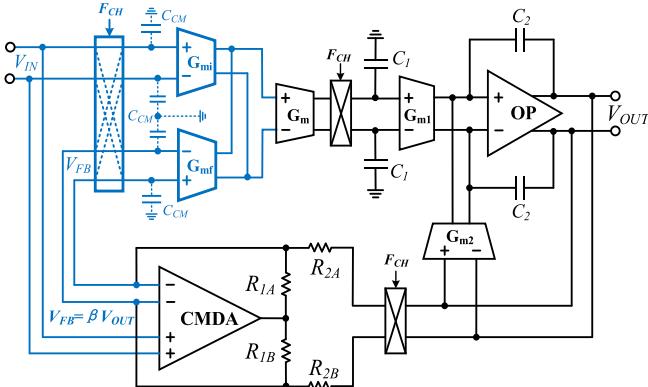


Fig. 6. DEM technique in CFIA architecture [105].

input impedance by simply switching the positions of the chopper and the input capacitor [62]. Chopper modulation of the input signal is performed at the virtual ground of the main op-amp, which allows the dc offset of the electrodes to be decoupled through the bias resistor. However, due to input capacitance mismatch, CMRR has to be sacrificed for high input impedance. Exchanging input and feedback signals is equivalent to exchanging input transconductances, which is a synchronous dynamic element matching (DEM) technique. That was initially developed as a method to reduce the effect of transconductance mismatch on the gain accuracy [103], [104].

In the designs aimed at minimizing mismatch, the frequency of DEM F_{DEM} is typically an integer multiple of the chopping frequency F_{CH} (e.g., $F_{\text{DEM}} = F_{\text{CH}}/4$ [103]). This can effectively attenuate the transconductance mismatch. However, the parasitic capacitances continue to transfer charge during the intervals of no DEM switching, which results in little improvement in input impedance.

Synchronizing and merging each chopper frequency to the DEM switching (i.e., $F_{\text{DEM}} = F_{\text{CH}}$) can achieve a large improvement in input impedance. This synchronous input exchange mechanism implemented in CFIA is illustrated in Fig. 6 [105]. When F_{CH} transitions from low to high, the signals V_{IN} and V_{FB} (that is βV_{OUT}) are exchanged, while the inverting and non-inverting terminals are also exchanged, resulting in chopper modulation of the two signals. The transfer charge generated at the V_{IN} terminal can be expressed as $C_P(V_{\text{IN}} - \beta V_{\text{OUT}})$. The periodic exchange of the input (G_{mi}) and feedback (G_{mf}) converters implements modulation of the input signal without charging the parasitic capacitances. This achieves a high input impedance of more than $1 \text{ G}\Omega$. Designers need to be aware that this DEM technique only applies to CFIA rather than other IA architectures.

In this scenario, a high chopping frequency enhances flicker noise rejection and allows a wide amplifier bandwidth. However, it is important to note that it also leads to an increase in power consumption. The IA chip reported in [105] consumes $561 \mu\text{W}$ at a chopping frequency of 20 kHz . Low-chopper frequencies reduce power consumption and result in lower residual offset. The CBIA with the embedded input stage consumes $3.96 \mu\text{W}$ at a chopping frequency of 1 kHz [106].

This IA with a simple design still provides acceptable input impedance and EDO rejection.

D. Precharge Assistance Technique

Another popular technique to increase the input impedance is to precharge the input capacitor [107]. For the CS-CCIA structure, the auxiliary path at the chopper input node includes a set of auxiliary buffers [108]. The auxiliary charge storage can supply charges to the input capacitance during the switch closure. So that less current is drawn from V_{IN} and the input impedance is increased significantly. The enhancement principle is essentially the same as that of PFL, but the advantage of this technique over PFL is that it is insensitive to the size of parasitic capacitances and can effectively increase the input impedance around dc.

As shown in Fig. 7(a) [109], before the main chopper F_{CH} starts to operate (i.e., the precharging stage), the auxiliary path buffer precharges the input capacitance C_{IN} . After precharging is completed, the auxiliary path stops operations to reduce power consumption while the input capacitance C_{IN} is reconnected to the input terminal of the main amplifier. Since C_{IN} has been precharged to V_{IN} , the main amplifier does not need to provide the charging current. The bypass chopper is driven by a buffer with an extremely high input impedance. As a result, the input capacitance C_{IN} does not draw current from V_{IN} throughout the signal acquisition process, which effectively increases the input impedance. It is worth noting that since the auxiliary path is added directly to the input of the IA [26], the dc offset and flicker noise of the auxiliary buffer will be amplified and degrade the performance of the front-end. An additional frequency clock is added in [109] to drive the passive mixer, M_1 and M_2 , in the auxiliary path to overcome this problem. The measurement results show that the input impedance is $1.6 \text{ G}\Omega$ from 0.1 Hz to 20 Hz , with an equivalent input capacitance of about 1 pF . It is suitable for closed-loop neural recording applications. Fortunately, the addition of C_{AUX} , a storage capacitor with a larger capacity than C_{IN} , reduces the error in the precharge stage and improves the total impedance boosting from 28.6 to 76.2 times [110].

To avoid the use of chopping in the precharge path, an AZ [111], [112] based precharging path is proposed to increase the input impedance [113], as shown in Fig. 7(b). Compared with the structure in Fig. 7(a), the auxiliary amplifier in G_{m1} has two differential input pairs, the auxiliary input pair with the AZ capacitor C_Z is used to store the mismatch voltage. The precharging path performs the AZ in Phase $\varphi 1$ and stores the offset voltage on capacitor C_Z . Similar to [109], two MOS capacitors are subsequently connected at the auxiliary amplifiers' outputs to share the charge with C_{IN} to speed up the precharging/discharge process. Interestingly, the AZ directly reduces the mismatch voltage between G_{m1} and G_{m2} . This not only greatly reduces the offset on the electrodes caused by the precharge path, but also reduces the setup error of the auxiliary amplifier, thus further boosting $T - Z_{\text{IN}}$. For a 10 kHz chopper with a parasitic input capacitance of 200 fF , the $T - Z_{\text{IN}}$ is boosted to $2.2 \text{ G}\Omega$ using an AZ auxiliary amplifier. However, it cannot be neglected that the

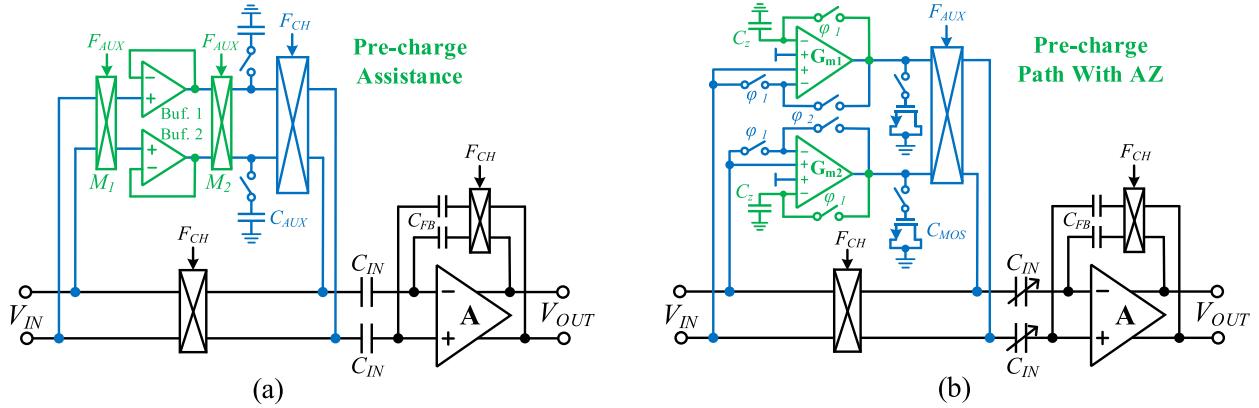


Fig. 7. Precharge technique for enhanced input impedance in CS-CCIA (a) auxiliary path [109] and (b) based on AZ [113].

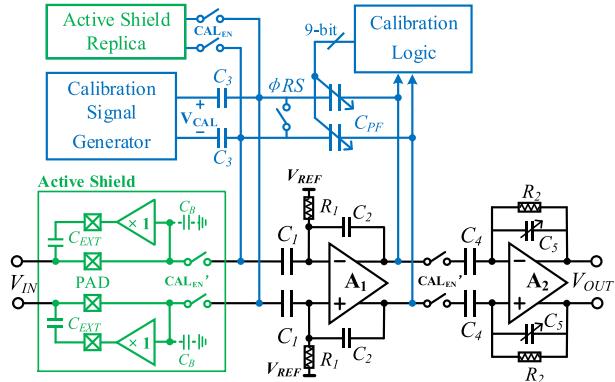


Fig. 8. Hybrid structure using AS replicas and self-calibrating positive feedback [37].

improvement efficiency of the precharge assistance technique is limited by the bandwidth of the buffer and its offset, and it is only applicable to the CS-CCIA architecture.

It is worth mentioning that the structure in Fig. 7(a) can be simplified. The passive mixer and precharging switch are not required if the buffers are redesigned [114] for self-compensation through periodic reconfiguration, reducing deterministic offsets [115]. According to the measurement results, although the input impedance of the self-compensating buffer is slightly inferior to the work in [109], it gains in low noise and a simple circuit configuration. The IBF is 30, which is comparable to that achieved using precharge-based methods.

E. High-Impedance Hybrid Structures

In addition to the above methods, hybrid structures that combine positive feedback with other techniques have also been proven to be an effective approach. A hybrid technique of self-calibrating positive feedback with AS replica to boost impedance is shown in Fig. 8 [37]. The AS replica consists of a virtual pad and a virtual shield buffer. During acquisition mode, an AS replica is connected for accurate modeling of internal parasitics. The scheme is set in calibration mode at the boundary between the steady state and the unstable state. During the calibration mode, CAL_{EN} is high and the calibration signal generator and calibration logic are turned on. The calibration signal generator provides a differential test

signal (V_{CAL}) through the coupling capacitor C_3 . An inverter-based comparator in the calibration logic block is used to check the stability of the system, monitor the output state of A_1 , and update the 9-bit positive feedback control word (PFCW). By detecting the stability boundary of the AFE, the capacitance values of the positive feedback capacitor array are adjusted automatically to maximize the cancellation of internal parasitic capacitances [116]. The reported IA benefits from the hybrid structure and achieves an input impedance of 50 G Ω at 50 Hz, which is equivalent to 60 fF capacitance [37]. Regrettably, it leads to an integrated noise on the signal bandwidth of up to 8.26 μ V_{rms}, in the absence of electrode firm contact.

The parasitic leakage current associated with the MOS pseudo-resistors employed in this architecture can engender large input mismatch voltages, and the leakage of the input ESD cells may constrain the dc input impedance. This problem was solved by using back-to-back diodes biased by V_{REF} [38]. Minimum-sized diodes are adopted to reduce the leakage which may limit the dc input impedance. Compared with linear resistive biasing, the back-to-back diodes enable faster recovery from the disturbances caused by input artifacts. This method is worth considering for enhancing the input impedance. On the other hand, to avoid the signal buffer for the shield consuming extra power and bringing noise to the system, one approach is to add an external PFL that compensates for external parasitic capacitance to the traditional internal PFL architecture [39]. This hybrid enhancement technique is known as an auto-calibrating double PFL (DPFL). It consists of two positive feedbacks. One added an attenuator A_{PF} [117] on the conventional PFL, and the other used an off-chip feedback capacitor C_{EPF} to effectively compensate for C_{P-EXT} . In other words, the two PFLs are designed to cancel out the $C_{IN} + C_{P-IN}$ and the C_{P-EXT} . The DPFL scheme also automatically controls the size of feedback capacitors to counteract undetermined parasitic components of the C_{P-IN} and C_{P-EXT} by the on-chip calibration logic. In order to relieve the tuning resolution limitation of C_{PF} in [38], an attenuator is used to compensate $C_{IN} + C_{P-IN}$ and reduce the resolution, which enhances the calibration capability of C_{PF} and further boosts IC-Z_{IN}. The reported AFE in [39] achieves 15 G Ω at 10 Hz and 2 G Ω at 50 Hz with the additional C_{P-EXT}

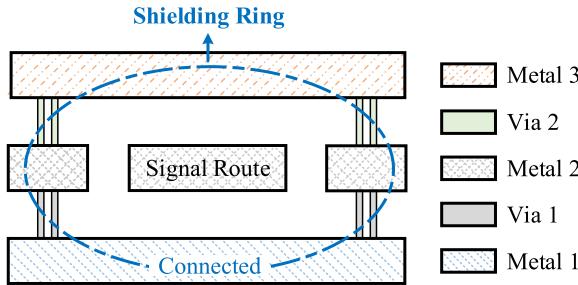


Fig. 9. Vertical cross section view of layout shielding technique.

of 82 pF. Dual-automatic calibration has a better NFE metric than detection boundary stability calibration [37] because the signal buffers for shielding unavoidably consume additional power and contribute noise to the AEF.

In an IA implementation, a neutralization technique with a fixed-value capacitor [118] is not sufficient in practice, owing to the intrinsic differences in IC manufacturing and variations in process, voltage, and temperature (PVT). To break through this limitation, hybrid approaches combining neutralization loops with bootstrapping architecture have been proposed in [8]. Bootstrapping [33] is a voltage feedback loop technique to address current into the bias network, and neutralization is a current feedback technique to address the leakage current of the amplifier. The effective compensation of leakage current allows an IA to suppress noise while maintaining high input impedance in a compact IC form [119]. In addition, layout shielding is an effective guarding technique that is implemented for the entire input stage. The physical layout realization is illustrated in Fig. 9. In this case, parasitic capacitance between the signal route and its environment draws no current from the driving signal. Upon introducing the shielding technique, the IA with the bootstrapping voltage feedback loop provides an input impedance of about 3.2 G Ω , while the bootstrapping voltage feedback loop and the neutralization current loop work together to achieve about 42 G Ω input impedance at 1 kHz [8].

Apart from the classic circuit-hybrid-based IAs, the dc-coupled differential-difference amplifier (DDA) [120] is an important building block for implementing a high $T - Z_{IN}$ AFE for bioelectric recording [44], [121]. Based on DDA's dual differential input pair structure, the input pair GM₂ is connected to the output to form a fully differential buffer [122], as shown in Fig. 10. The DDA-based buffer is added between the chopper and the input capacitor C_{IN} . The input signal V_{IN} reaches the input pair transistor of the GM₁ after passing through the chopper. Therefore, the equivalent capacitance is mainly determined by the parasitic capacitances of the GM₁'s input pair, which can be reduced to the order of fF by using the small size of the input transistors. According to (1), the capacitance charged by the chopper is reduced, thus significantly increasing the input impedance. The reported chip achieves an input impedance of 1.29 G Ω at 60 Hz for a 1 mV peak-to-peak input signal. This approach can be understood as adding a buffer to the dc-coupled input stage, which increases the input impedance but also introduces additional power consumption. Each channel of IA in [44] consumes 2.48 μ W

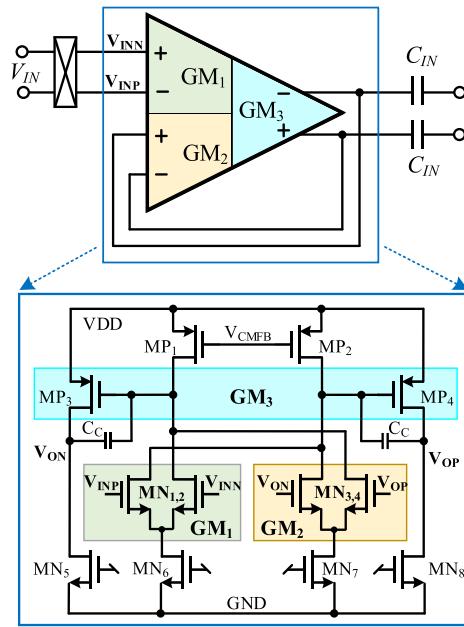


Fig. 10. DDA-based input impedance boosting chopper [122].

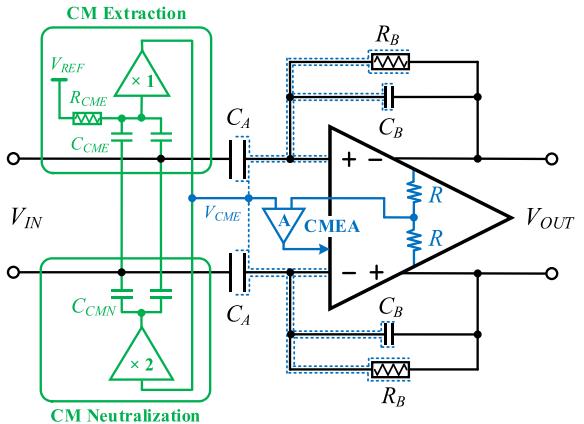


Fig. 11. CM-REP technique to enhance the CM input impedance in [129].

of power and contributes an input-referred noise of 1.74 μ V_{rms}. Furthermore, in [45], DDA was optimized to use only one current source, two nMOS, and two pMOS devices. This further reduces the power consumption and circuit complexity of the IA.

Despite the improvements in power consumption achieved by impedance boosting schemes, these chips still occupy a large area. In neural recording ICs, high channel counts are required to read out as many neurons as possible via implanted electrodes. Correspondingly, dramatic area reduction has been achieved by using direct $\Delta\Sigma$ conversion at the expense of noise [123]. The input impedance of this topology is further increased by mixing bootstrapping and chopping schemes onto a small-area dc-coupled $\Delta - \Delta\Sigma$ architecture. The chip reported in [124] achieves an input impedance of 283 M Ω at 10 Hz with an area of merely 0.0077 mm² per channel. The trade-off in technical indicators of this work is that the EDO rejection is limited to ± 70 mV.

TABLE II
PERFORMANCE SUMMARY OF INPUT IMPEDANCE BOOSTING TECHNIQUES

Parameter	Technology (nm)	Power /channel (μW)	Architecture ^(A)	Impedance Boosting Type	Input Impedance	IBF	Equivalent Input Capacitance (pF) ^(B)	Input Referred Noise ^(C)	Application
[101] JSSC'23	180	5350	CFIA	LPFL	1.8 G Ω @5 Hz	3.6	17.7	39 nV/ $\sqrt{\text{Hz}}$	Sensor Node
[106] TBCS'23	350	1.19	CBIA	Embedded Input Stage	496 M Ω @50 Hz	N/A	6.4	0.91 μV_{rms}	ECG
		3.96			463 M Ω @50 Hz		6.9	0.6 μV_{rms}	EEG
[91] TIM'23	N/A ^(D)	130	Op-amp	Power Bootstrapping	>10 G Ω (0.1–150 Hz)	N/A	N/A	32 μV_{pp} (@250 Hz)	ECG
[39] JSSC'22	110	3.83	CS-CCIA	DPFL	15 G Ω @10 Hz 2 G Ω @50 Hz	10.7 ^(E)	1.1	0.36 μV_{rms} (0.5–300 Hz)	Wearable Devices
[129] JSSC'22	180	3.35	IA+PGA	CM-REP	1.6 G Ω (@50 Hz ^(F))		N/A	3.14 μV_{rms} (0.5–5k Hz)	Wearable Devices
[6] JSSC'22	180	4.5	CS-CCIA	3-T Varactor	>1 G Ω	370	N/A	13 nV/ $\sqrt{\text{Hz}}$	ECG/ERG
[45] TBCS'21	350	0.67	Three-opamp	DDA	336 M Ω @50 Hz	N/A	9.5	1.54 μV_{rms} (0.1–300 Hz)	ECG
[124] VLSIC'21	55	61.2	DC-coupled	Bootstrapping + Chopping	283 M Ω @10 Hz	N/A	56	5.53 μV_{rms} (0.3–10k Hz)	Neural Recording
[38] TBCS'19	180	90	CCIA	Two Diodes + PFL	5 G Ω @50 Hz	4	0.64	3.7 μV_{rms} (0.5–100 Hz)	ECG
[100] ASSCC'19	180	0.78	CS-CCIA	Scaled Cap + PFL	1.5 G Ω @50 Hz	N/A	1.1	1.62 μV_{rms} (0.5–800 Hz)	ECG
[37] JSSC'18	180	0.29	IA+PGA	AS + Self-calibrated PFL	50 G Ω @50 Hz	50	0.06	8.26 μV_{rms} (1–400 Hz)	Wearable Devices
[105] TCASI'17	320	561	CFIA	DEM	> 1 G Ω	22.4	N/A	18 nV/ $\sqrt{\text{Hz}}$	Sensor Node
[109] JSSC'17	40	2.8	CS-CCIA	Pre-charge Assist	1.6 G Ω @DC	76.2	~1	1.8 μV_{rms} (1–200 Hz)	Neural Recording
[97] TCASI'17	130	42	IA+VGA	NCGFB ^(G)	570 M Ω @50 Hz 1.42 G Ω @20 Hz	12.5	5.6	3.75 μV_{rms} (0.5–45.5 Hz)	EEG
[36] VLSI'16	180	108	CS-CCIA		Active Electrode		6.7 G Ω @50 Hz	N/A	0.67 μV_{rms} (0.5–100 Hz)
[8] TBCS'16	350	3.1	Op-amp	BNS ^(H)	42 G Ω @1 kHz	13.3	0.0038	18.2 nV/ $\sqrt{\text{Hz}}$	Neural Monitoring
[67] JSSC'11	65	1.8	CS-CCIA	Traditional PFL	> 30 M Ω	5	N/A	60 nV/ $\sqrt{\text{Hz}}$	Sensor Node
[33] JESTES'11	500	4.95	Op-amp	AS	> 50 T Ω ^(I)	N/A	N/A	200 nV/ $\sqrt{\text{Hz}}$ @1 Hz	ECG/EEG

^(A) PGA=programmable gain amplifier, VGA=variable gain amplifier.

^(B) Calculated from $(2\pi f_{IN} \times Z_{IN})^{-1}$.

^(C) Considering the noise contributions brought by different techniques, input reference noise spectral density is added as a reference in the table.

^(D) This amplifier prototype was built using commercially available off-the-shelf discrete components.

^(E) With an additional C_{P-EXT} of 82 pF.

^(F) This is the differential-mode input impedance, the common-mode input impedance is 50 G Ω @50 Hz.

^(G) NCGFB=negative capacitance generation feedback.

^(H) BNS=bootstrapping, neutralisation with shielding.

^(I) This is the estimated value in [33].

F. CM Replication Technique

The above technique schemes are usually used to boost the differential mode input impedance. Bio-electric signals are vulnerable to the CM interference from the 50/60 Hz mains supply [125]. It is obvious that increasing the CM input impedance is beneficial for the IA to obtain high CMRR [126], [127], [128]. Recently, a novel idea of CM input impedance boosting has been proposed in [129]. Replicating the input CM signal to the output causes the CM voltage on the amplifier to

be zero, eliminating the CM current and achieving an infinite CM input impedance. This approach is known as the CM replication (CM-REP) technique.

The CM-REP technique implemented in IA is shown in Fig. 11. Two capacitors, C_{CME} , are used to extract the input CM voltage and transfer it to the input of the CM error amplifier (CMEA). The other input of the CMEA is the output CM of the OTA. Thus, this is similar to a conventional amplifier with dc CM bias. The high-gain common

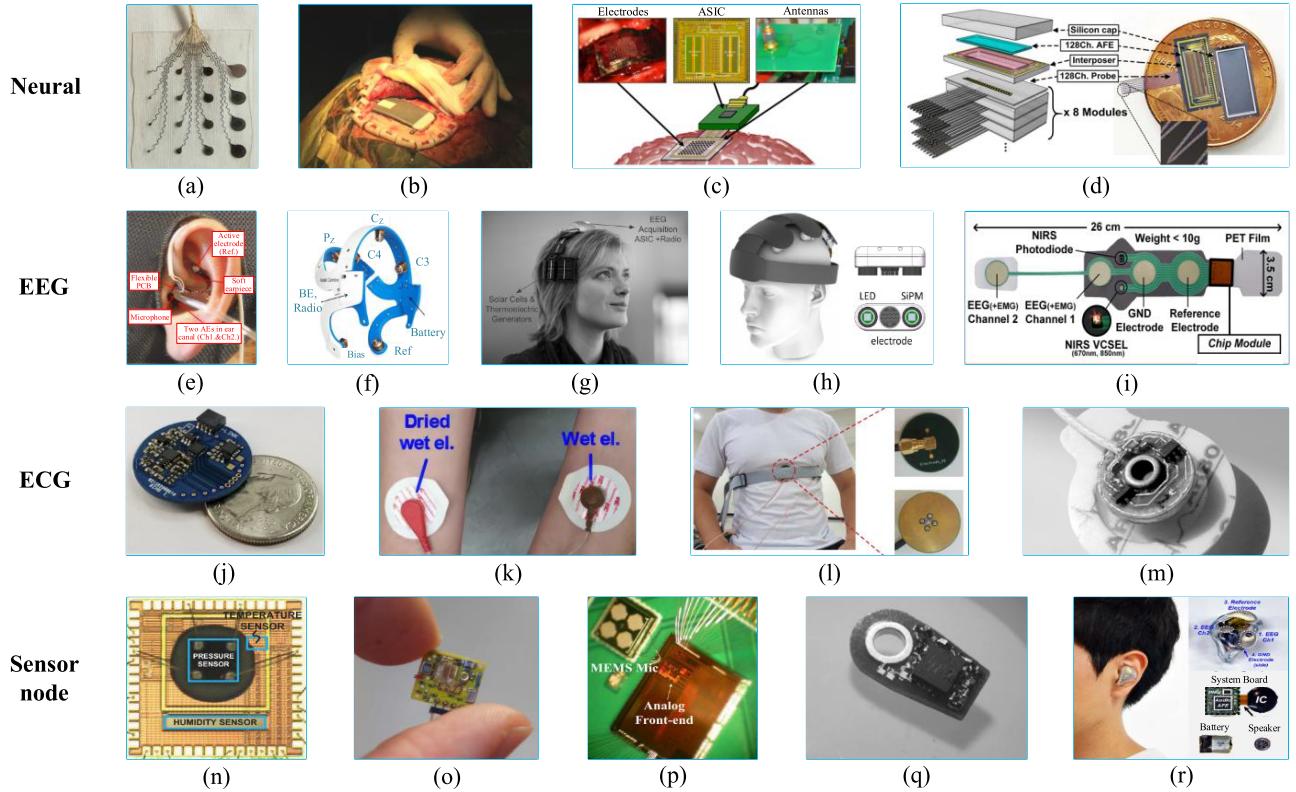


Fig. 12. Biomedical applications of high input impedance systems. Neural: (a) 16-channel PtIr-electrode array [114], (b) closed-loop neurostimulator [113], (c) 64-channel wireless electrocorticography [32], and (d) 1024-channel 3-D neural recording microsystems [28]. EEG: (e) wearable ear-EEG [36], (f) wireless EEG headset [35], (g) ambulatory EEG systems [12], (h) multimodal brain monitoring [94], and (i) anesthesia depth monitoring system [81]. ECG: (j) multimodal recording link device [133], (k) contacts for two-electrode ECG [132], (l) custom non-contact electrodes [37], and (m) AE on button [134]. Sensor node: (n) multifunction environmental sensor [1], (o) sensing/recording system: “Bumblebee” [58], (p) acoustic AFE [59], (q) AE for EEG and electrical impedance tomography [119], and (r) in-ear controller IC [135].

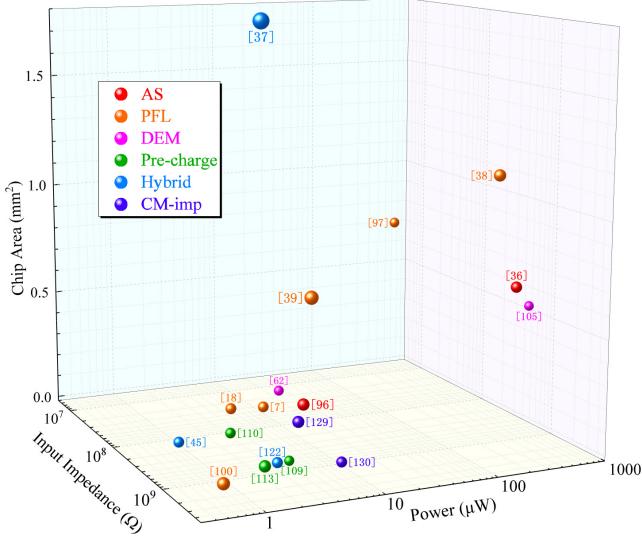


Fig. 13. Three-dimensional comparison of input impedance, power, and chip area. Red: AS technique, Orange: positive feedback technique, Magenta: DEM technique, Green: precharge assistance technique, Blue: hybrid technique, and Purple: CM impedance boosting technique. Visually, there is a perceptible effect of diminishing size with distance, whereby a larger sphere signifies a higher input impedance.

mode feedback (CMFB) loop [130] clamps the voltage V_{CME} extracted by C_{CME} and the OTA output CM, establishing the IA's output CM voltage to achieve CM-REP. Meantime,

the same shield-metal technique shown in Fig. 9 is used, and the shielding ring is driven through a CM buffer. The CM neutralization circuit and the shielding circuit reduce the parasitic capacitance of critical nodes to further eliminate the flow of CM current through the nodes. The reported IA demonstrates 130 dB CMRR with $1 \text{ M}\Omega||10 \text{ nF}$ mismatch of source impedance and $50 \text{ G}\Omega$ input CM impedance at 50/60 Hz simultaneously.

The CM-REP technique reuses the CMFB loop of traditional amplifiers, offering a more streamlined implementation while avoiding chopping. In practical applications, the AFE mentioned in [129] can provide a significant CMRR to combat CM interference. Even so, the chip's differential input impedance at 50 Hz is only $1.6 \text{ G}\Omega$, which is lower than the value of the CM input impedance, posing a potential risk of attenuation for bioelectric signals. The precharging technique in [26] and [109] also enhances the CM input impedance. However, current noise is introduced in this structure due to the chopping involved. This scheme requires further optimization to achieve low noise and high input impedance.

V. CONCLUSION AND TREND

From the design methodology perspective, architectural ideas for boosting input impedance in bioelectrical signal acquisition systems are well described in this article, from achieving high IBF to building technical circuitry. Examples of

these high input impedance systems in biomedical applications for neural, ECG, EEG, and sensor nodes are illustrated in Fig. 12. A summary and comparison of the technique solutions for AFE input impedance enhancement are shown in Table II. With the assistance of boosting techniques, the ac-coupled IA architecture has achieved significant improvement in IBF (for example [6], [8], [37], [97], [105], [109]). This can be regarded as indicative of its greater potential for improvement compared to the dc-coupled architecture. The equivalent input capacitance serves as a metric that mitigates the differences between architectures, as it takes into account the effect of frequency on the final input impedance value after employing enhanced techniques. These IA architectures using various impedance boosting techniques achieve input impedances exceeding the $G\Omega$ range at 50 Hz (for example [8], [36], [37], [38], [39], [91], [100], [129]). We interestingly find that [39] and [100], employing the same architecture, exhibit similar impedance characteristics, yet each possesses distinct advantages in terms of power consumption and input-referred noise. That is to say, boosting Z_{IN} requires additional chip area and power. Fig. 13 provides a data comparison between the power, chip area, and input impedance of the above boosting techniques. There exists a phenomenon of spheres appearing smaller in the distance and larger up close in 3-D space. In fact, the AFE chip in [39], [96], [100], [109], [113], [122], [129], and [130] has a power of less than 10 μW , an area of less than 0.5 mm^2 and an input impedance of greater than 1 $G\Omega$. In conclusion, the AS and positive feedback technique is a promising candidate for high input impedance AFE designs ($G\Omega$ level). For applications that prioritize small areas and low power consumption, precharge and hybrid techniques with moderate input impedance (sub- $G\Omega$ level) are good choices.

In bioelectrical signal monitoring sensor systems, the total input impedance should be as high as possible to avoid signal attenuation. It remains an unsolved challenge. As CMOS technology continues scaling down, the decreased power supply voltages and aggravated parasitics exacerbate this problem. New techniques are required to solve this issue. In the future, a possible trend is that technique schemes will become more hybrid to achieve higher input impedance characteristics. With the emergence of AS + LPF and DPFL, compensating for internal and external parasitics respectively is a promising scheme. Meanwhile, it is worth further optimizing the feedback capacitance and calibration method of the PFL to jointly achieve low power consumption, high tuning resolution, and bandwidth. Another trend that may become more important in the future is to increase CM interference tolerance [128], [131] to weaken the impact of contact impedance mismatch, even in the dry electrode or non-contact acquisition mode [38], [132]. Overall, AFEs with high input impedance characteristics are needed to provide high-quality signals for biomedical sensor nodes. Efforts in this research area are expected to achieve significant returns for the field of bio-electric monitoring.

REFERENCES

- [1] M. Maruyama, S. Taguchi, M. Yamanoue, and K. Iizuka, “An analog front-end for a multifunction sensor employing a weak-inversion biasing technique with 26 nV_{rms}, 25 aC_{rms}, and 19 fA_{rms} input-referred noise,” *IEEE J. Solid-State Circuits*, vol. 51, no. 10, pp. 2252–2261, Oct. 2016.
- [2] Y.-P. Chen et al., “An injectable 64 nW ECG mixed-signal SoC in 65 nm for arrhythmia monitoring,” *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 375–390, Jan. 2015.
- [3] S. Song et al., “A low-voltage chopper-stabilized amplifier for fetal ECG monitoring with a 1.41 power efficiency factor,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 9, no. 2, pp. 237–247, Apr. 2015.
- [4] M. Guermandi, R. Cardu, E. Franchi, and R. Guerrieri, “Active electrode IC combining EEG, electrical impedance tomography, continuous contact impedance measurement and power supply on a single wire,” in *Proc. ESSCIRC (ESSCIRC)*, Helsinki, Finland, Sep. 2011, pp. 335–338.
- [5] Y.-P. Hsu, Z. Liu, and M. M. Hella, “A –68 dB THD, 0.6 mm² active area biosignal acquisition system with a 40–320 Hz duty-cycle controlled filter,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 1, pp. 48–59, Jan. 2020.
- [6] L. Fang and P. Gui, “A low-noise low-power chopper instrumentation amplifier with robust technique for mitigating chopping ripples,” *IEEE J. Solid-State Circuits*, vol. 57, no. 6, pp. 1800–1811, Jun. 2022.
- [7] D. Luo, M. Zhang, and Z. Wang, “A low-noise chopper amplifier designed for multi-channel neural signal acquisition,” *IEEE J. Solid-State Circuits*, vol. 54, no. 8, pp. 2255–2265, Aug. 2019.
- [8] Z. Zhou and P. A. Warr, “A high input impedance low noise integrated front-end amplifier for neural monitoring,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 6, pp. 1079–1086, Dec. 2016.
- [9] C. De Capua, A. Meduri, and R. Morello, “A smart ECG measurement system based on web-service-oriented architecture for telemedicine applications,” *IEEE Trans. Instrum. Meas.*, vol. 59, no. 10, pp. 2530–2538, Oct. 2010.
- [10] L. Fanucci et al., “Sensing devices and sensor signal processing for remote monitoring of vital signs in CHF patients,” *IEEE Trans. Instrum. Meas.*, vol. 62, no. 3, pp. 553–569, Mar. 2013.
- [11] X. Zou, X. Xu, L. Yao, and Y. Lian, “A 1-V 450-nW fully integrated programmable biomedical sensor interface chip,” *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1067–1077, Apr. 2009.
- [12] R. F. Yazicioglu, P. Merken, R. Puers, and C. Van Hoof, “A 200 μW eight-channel EEG acquisition ASIC for ambulatory EEG systems,” *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 3025–3038, Dec. 2008.
- [13] D. D. He, E. S. Winokur, and C. G. Sodini, “A continuous, wearable, and wireless heart monitor using head ballistocardiogram (BCG) and head electrocardiogram (ECG),” in *Proc. IEEE EMBC*, Aug. 2011, pp. 4729–4732.
- [14] A. Gruetzmann, S. Hansen, and J. Müller, “Novel dry electrodes for ECG monitoring,” *Physiolog. Meas.*, vol. 28, no. 11, pp. 1375–1390, Nov. 2007.
- [15] P. Laferriere, E. D. Lemaire, and A. D. C. Chan, “Surface electromyographic signals using dry electrodes,” *IEEE Trans. Instrum. Meas.*, vol. 60, no. 10, pp. 3259–3268, Oct. 2011.
- [16] F. Dell’Agnola, U. Pale, R. Marino, A. Arza, and D. Atienza, “MBioTracker: Multimodal self-aware bio-monitoring wearable system for online workload detection,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 15, no. 5, pp. 994–1007, Oct. 2021.
- [17] Y. M. Chi, T. P. Jung, and G. Cauwenberghs, “Dry-contact and noncontact biopotential electrodes: Methodological review,” *IEEE Rev. Biomed. Eng.*, vol. 3, pp. 106–119, 2010.
- [18] T. Tang, W. L. Goh, L. Yao, and Y. Gao, “A 16-channel TDM analog front-end with enhanced system CMRR for wearable dry EEG recording,” in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2017, pp. 33–36.
- [19] S. Novik et al., “A CMOS multi-electrode array for four-electrode bioimpedance measurements,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 16, no. 6, pp. 1276–1286, Dec. 2022.
- [20] F. N. Guerrero and E. M. Spinelli, “A two-wired ultra-high input impedance active electrode,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 2, pp. 437–445, Apr. 2018.
- [21] B. Taji, A. D. C. Chan, and S. Shirmohammadi, “Effect of pressure on skin-electrode impedance in wearable biomedical measurement devices,” *IEEE Trans. Instrum. Meas.*, vol. 67, no. 8, pp. 1900–1912, Aug. 2018.
- [22] E. Spinelli and M. Haberman, “Insulating electrodes: A review on biopotential front ends for dielectric skin-electrode interfaces,” *Physiolog. Meas.*, vol. 31, no. 10, pp. S183–S198, Oct. 2010.

- [23] A. K. Engel, C. K. E. Moll, I. Fried, and G. A. Ojemann, "Invasive recordings from the human brain: Clinical insights and beyond," *Nature Rev. Neurosci.*, vol. 6, no. 1, pp. 35–47, Jan. 2005.
- [24] W. Truccolo et al., "Single-neuron dynamics in human focal epilepsy," *Nature Neurosci.*, vol. 14, no. 5, pp. 635–641, May 2011.
- [25] A. B. Schwartz, X. T. Cui, D. J. Weber, and D. W. Moran, "Brain-controlled interfaces: Movement restoration with neural prosthetics," *Neuron*, vol. 52, no. 1, pp. 205–220, Oct. 2006.
- [26] H. Chandrakumar and D. Marković, "A high dynamic-range neural recording chopper amplifier for simultaneous neural recording and stimulation," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 645–656, Mar. 2017.
- [27] C. Qian, J. Parramon, and E. Sanchez-Sinencio, "A micropower low-noise neural recording front-end circuit for epileptic seizure detection," *IEEE J. Solid-State Circuits*, vol. 46, no. 6, pp. 1392–1405, Jun. 2011.
- [28] S.-Y. Park, J. Cho, K. Na, and E. Yoon, "Modular 128-channel Δ - $\Delta\Sigma$ analog front-end architecture using spectrum equalization scheme for 1024-channel 3-D neural recording microsystems," *IEEE J. Solid-State Circuits*, vol. 53, no. 2, pp. 501–514, Feb. 2018.
- [29] J. Kim, C. V. Fengel, S. Yu, E. D. Minot, and M. L. Johnston, "Frequency-division multiplexing with graphene active electrodes for neurosensor applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 5, pp. 1735–1739, May 2021.
- [30] Y.-H. Nien et al., "Application of non-enzymatic lactate sensor modified by graphitic carbon nitride/iron-platinum nanoparticles and combined with the low power consumption instrumentation amplifier and calibration readout circuit," *IEEE Trans. Instrum. Meas.*, vol. 72, pp. 1–8, 2023.
- [31] K. A. Ng and Y. P. Xu, "A compact, low input capacitance neural recording amplifier with C_{in}/gain of 20 fF/V/N," in *Proc. IEEE Biomed. Circuits Syst. Conf. (BioCAS)*, Nov. 2012, pp. 328–331.
- [32] R. Müller et al., "A minimally invasive 64-channel wireless μ ECoG implant," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 344–359, Jan. 2015.
- [33] Y. M. Chi, C. Maier, and G. Cauwenberghs, "Ultra-high input impedance, low noise integrated amplifier for noncontact biopotential sensing," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 1, no. 4, pp. 526–535, Dec. 2011.
- [34] J. Xu, B. Busze, C. Van Hoof, K. A. A. Makinwa, and R. F. Yazicioglu, "A 15-channel digital active electrode system for multi-parameter biopotential measurement," *IEEE J. Solid-State Circuits*, vol. 50, no. 9, pp. 2090–2100, Sep. 2015.
- [35] J. Xu et al., "A wearable 8-channel active-electrode EEG/ETI acquisition system for body area networks," *IEEE J. Solid-State Circuits*, vol. 49, no. 9, pp. 2005–2016, Sep. 2014.
- [36] X. Zhou, Q. Li, S. Kilsgaard, F. Moradi, S. L. Kappel, and P. Kidmose, "A wearable ear-EEG recording system based on dry-contact active electrodes," in *Proc. IEEE Symp. VLSI Circuits (VLSI-Circuits)*, Jun. 2016, pp. 1–2.
- [37] J. Lee, G. Lee, H. Kim, and S. Cho, "An ultra-high input impedance analog front end using self-calibrated positive feedback," *IEEE J. Solid-State Circuits*, vol. 53, no. 8, pp. 2252–2262, Aug. 2018.
- [38] M. Chen et al., "A 400 $\text{G}\Omega$ input-impedance active electrode for non-contact capacitively coupled ECG acquisition with large linear-input-range and high CM-interference-tolerance," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 2, pp. 376–386, Apr. 2019.
- [39] Y. Park, J.-H. Cha, S.-H. Han, J.-H. Park, and S.-J. Kim, "A 3.8- μ W 1.5-NEF 15- $\text{G}\Omega$ total input impedance chopper stabilized amplifier with auto-calibrated dual positive feedback in 110-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 57, no. 8, pp. 2449–2461, Aug. 2022.
- [40] S. Zhang, C. Gao, X. Zhou, and Q. Li, "A 130 dB CMRR instrumentation amplifier with common-mode replication," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 356–358.
- [41] M. R. Pazhouhandeh, M. Chang, T. A. Valiante, and R. Genov, "Track-and-zoom neural analog-to-digital converter with blind stimulation artifact rejection," *IEEE J. Solid-State Circuits*, vol. 55, no. 7, pp. 1984–1997, Jul. 2020.
- [42] S. Song, Y. Zhou, M. Li, and M. Zhao, "A review on recent development of input impedance boosting for bio-potential amplifiers," in *Proc. 18th Int. SoC Design Conf. (ISOCC)*, Oct. 2021, pp. 272–273.
- [43] C. Kitchin and L. Counts, *A Designer's Guide to Instrumentation Amplification*, 3rd ed. Norwood, MA, USA: Analog Devices, 2006.
- [44] Y. Zhao, Z. Shang, and Y. Lian, "A 2.55 NEF 76 dB CMRR DC-coupled fully differential difference amplifier based analog front end for wearable biomedical sensors," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 5, pp. 918–926, Oct. 2019.
- [45] C. Sawigun and S. Thanapitak, "A compact sub- μ W CMOS ECG amplifier with 57.5- $\text{M}\Omega$ Z_{in} , 2.02 NEF, 8.16 PEF and 83.24-dB CMRR," *IEEE Trans. Biomed. Circuits Syst.*, vol. 15, no. 3, pp. 549–558, Jun. 2021.
- [46] M. N. Hasan and K.-S. Lee, "A wide linear output range biopotential amplifier for physiological measurement frontend," *IEEE Trans. Instrum. Meas.*, vol. 64, no. 1, pp. 120–131, Jan. 2015.
- [47] B. J. van den Dool and J. K. Huijsing, "Indirect current feedback instrumentation amplifier with a common-mode input range that includes the negative roll," *IEEE J. Solid-State Circuits*, vol. 28, no. 7, pp. 743–749, Jul. 1993.
- [48] R. Wu, K. A. A. Makinwa, and J. H. Huijsing, "A chopper current-feedback instrumentation amplifier with a 1 mHz 1/f noise corner and an AC-coupled ripple reduction loop," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3232–3243, Dec. 2009.
- [49] A. Worapishet and A. Demosthenous, "Generalized analysis of random common-mode rejection performance of CMOS current feedback instrumentation amplifiers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 9, pp. 2137–2146, Sep. 2015.
- [50] A. Worapishet, A. Demosthenous, and X. Liu, "A CMOS instrumentation amplifier with 90-dB CMRR at 2-MHz using capacitive neutralization: Analysis, design considerations, and implementation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 4, pp. 699–710, Apr. 2011.
- [51] Z. Hoseini, M. Nazari, K.-S. Lee, and H. Chung, "Current feedback instrumentation amplifier with built-in differential electrode offset cancellation loop for ECG/EEG sensing frontend," *IEEE Trans. Instrum. Meas.*, vol. 70, pp. 1–11, 2021.
- [52] R. F. Yazicioglu, S. Kim, T. Torfs, H. Kim, and C. Van Hoof, "A 30 μ W analog signal processor ASIC for portable biopotential signal monitoring," *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp. 209–223, Jan. 2011.
- [53] R. F. Yazicioglu, P. Merken, R. Puers, and C. Van Hoof, "A 60 μ W 60 nV/ $\sqrt{\text{Hz}}$ readout front-end for portable biopotential acquisition systems," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1100–1110, May 2007.
- [54] S. Lee et al., "A 110 dB-CMRR 100 dB-PSRR multi-channel neural-recording amplifier system using differentially regulated rejection ratio enhancement in 0.18 μ m CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 472–474.
- [55] S. Zhang, X. Zhou, C. Gao, and Q. Li, "An AC-coupled instrumentation amplifier achieving 110-dB CMRR at 50 Hz with chopped pseudoresistors and successive-approximation-based capacitor trimming," *IEEE J. Solid-State Circuits*, vol. 56, no. 1, pp. 277–286, Jan. 2021.
- [56] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003.
- [57] K. A. Ng and Y. P. Xu, "A low-power, high CMRR neural amplifier system employing CMOS inverter-based OTAs with CMFB through supply rails," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 724–737, Mar. 2016.
- [58] F. Zhang, J. Holleman, and B. P. Otis, "Design of ultra-low power biopotential amplifiers for biosignal acquisition applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 4, pp. 344–355, Aug. 2012.
- [59] R. Rothe et al., "A delta sigma-modulated sample and average common-mode feedback technique for capacitively coupled amplifiers in a 192-nW acoustic analog front-end," *IEEE J. Solid-State Circuits*, vol. 57, no. 4, pp. 1138–1152, Apr. 2022.
- [60] P. Harpe, H. Gao, R. v. Dommele, E. Cantatore, and A. H. M. van Roermund, "A 0.20 mm² 3 nW signal acquisition IC for miniature sensor nodes in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 1, pp. 240–248, Jan. 2016.
- [61] E. Guglielmi et al., "High-value tunable pseudo-resistors design," *IEEE J. Solid-State Circuits*, vol. 55, no. 8, pp. 2094–2105, Aug. 2020.
- [62] N. Verma, A. Shoeb, J. Bohorquez, J. Dawson, J. Guttag, and A. P. Chandrakasan, "A micro-power EEG acquisition SoC with integrated feature extraction processor for a chronic seizure detection system," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 804–816, Apr. 2010.

- [63] T.-Y. Wang, M.-R. Lai, C. M. Twigg, and S.-Y. Peng, "A fully reconfigurable low-noise biopotential sensing amplifier with 1.96 noise efficiency factor," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 3, pp. 411–422, Jun. 2014.
- [64] V. Majidzadeh, A. Schmid, and Y. Leblebici, "Energy efficient low-noise neural recording amplifier with enhanced noise efficiency factor," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 3, pp. 262–271, Jun. 2011.
- [65] T. Rooijers, J. H. Huijsing, and K. A. A. Makinwa, "An auto-zero-stabilized voltage buffer with a quiet chopping scheme and constant sub-pA input current," *IEEE J. Solid-State Circuits*, vol. 57, no. 8, pp. 2438–2448, Aug. 2022.
- [66] T. Denison, K. Consoer, W. Santa, A.-T. Avestruz, J. Cooley, and A. Kelly, "A 2 μ W 100 nV/ $\sqrt{\text{Hz}}$ chopper-stabilized instrumentation amplifier for chronic measurement of neural field potentials," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2934–2945, Dec. 2007.
- [67] Q. Fan, F. Sebastian, J. H. Huijsing, and K. A. A. Makinwa, "A 1.8 μ W 60 nV/ $\sqrt{\text{Hz}}$ capacitively-coupled chopper instrumentation amplifier in 65 nm CMOS for wireless sensor nodes," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1534–1543, Jul. 2011.
- [68] R. Müller et al., "A miniaturized 64-channel 225 μ W wireless electrocorticographic neural sensor," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 412–413.
- [69] G. T. Ong and P. K. Chan, "A power-aware chopper-stabilized instrumentation amplifier for resistive wheatstone bridge sensors," *IEEE Trans. Instrum. Meas.*, vol. 63, no. 9, pp. 2253–2263, Sep. 2014.
- [70] M. S. J. Steyaert and W. M. C. Sansen, "A micropower low-noise monolithic instrumentation amplifier for medical purposes," *IEEE J. Solid-State Circuits*, vol. SSC-22, no. 6, pp. 1163–1168, Dec. 1987.
- [71] S. Mondal and D. A. Hall, "A 13.9-nA ECG amplifier achieving 0.86/0.99 NEF/PEF using AC-coupled OTA-stacking," *IEEE J. Solid-State Circuits*, vol. 55, no. 2, pp. 414–425, Feb. 2020.
- [72] R. Müller, S. Gambini, and J. M. Rabaey, "A 0.013 mm², 5 μ W, DC-coupled neural signal acquisition IC with 0.5 V supply," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 232–243, Jan. 2012.
- [73] F. M. Yaul and A. P. Chandrakasan, "A noise-efficient 36 nV/ $\sqrt{\text{Hz}}$ chopper amplifier using an inverter-based 0.2-V supply input stage," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 3032–3042, Nov. 2017.
- [74] J. Zheng, W.-H. Ki, and C.-Y. Tsui, "Analysis and design of a ripple reduction chopper bandpass amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 4, pp. 1185–1195, Apr. 2018.
- [75] H. Chandrakumar and D. Markovic, "A simple area-efficient ripple-rejection technique for chopped biosignal amplifiers," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 2, pp. 189–193, Feb. 2015.
- [76] T. N. Lin, B. Wang, and A. Bermak, "Ripple suppression in capacitive-gain chopper instrumentation amplifier using amplifier slicing," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 10, pp. 3991–4000, Oct. 2021.
- [77] R. van Wegberg et al., "A 5-Channel unipolar fetal-ECG readout IC for patch-based fetal monitoring," *IEEE Solid-State Circuits Lett.*, vol. 2, no. 9, pp. 71–74, Sep. 2019.
- [78] O. Casas, E. M. Spinelli, and R. Pallas-Areny, "Fully differential AC-coupling networks: A comparative study," *IEEE Trans. Instrum. Meas.*, vol. 58, no. 1, pp. 94–98, Jan. 2009.
- [79] E. Serrano-Finetti and R. Pallas-Areny, "Noise reduction in AC-coupled amplifiers," *IEEE Trans. Instrum. Meas.*, vol. 63, no. 7, pp. 1834–1841, Jul. 2014.
- [80] S. Mitra, J. Xu, A. Matsumoto, K. A. A. Makinwa, C. Van Hoof, and R. F. Yazicioglu, "A 700 μ W 8-channel EEG/contact-impedance acquisition system for dry-electrodes," in *Proc. Symp. VLSI Circuits (VLSIC)*, Jun. 2012, pp. 68–69.
- [81] U. Ha, J. Lee, M. Kim, T. Roh, S. Choi, and H. Yoo, "An EEG-NIRS multimodal SoC for accurate anesthesia depth monitoring," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1830–1843, Jun. 2018.
- [82] A. C. Metting van Rijn, A. Peper, and C. A. Grimbergen, "High-quality recording of bioelectric events: Part 1 interference reduction, theory and practice," *Med. Biol. Eng. Comput.*, vol. 28, no. 5, pp. 389–397, Sep. 1990.
- [83] Y. Li, C. C. Y. Poon, and Y.-T. Zhang, "Analog integrated circuits design for processing physiological signals," *IEEE Rev. Biomed. Eng.*, vol. 3, pp. 93–105, 2010.
- [84] N. Van Helleputte, S. Kim, H. Kim, J. P. Kim, C. Van Hoof, and R. F. Yazicioglu, "A 160 μ A biopotential acquisition IC with fully integrated IA and motion artifact suppression," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 6, pp. 552–561, Dec. 2012.
- [85] J. Xu, Q. Fan, J. H. Huijsing, C. Van Hoof, R. F. Yazicioglu, and K. A. A. Makinwa, "Measurement and analysis of current noise in chopper amplifiers," *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1575–1584, Jul. 2013.
- [86] L. Fang and P. Gui, "A 14 nV/ $\sqrt{\text{Hz}}$ 14 μ W chopper instrumentation amplifier with dynamic offset zeroing (DOZ) technique for ripple reduction," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2019, pp. 1–4.
- [87] C. C. Enz, E. A. Vittoz, and F. Krummenacher, "A CMOS chopper amplifier," *IEEE J. Solid-State Circuits*, vol. SSC-22, no. 3, pp. 335–342, Jun. 1987.
- [88] S. Maji and M. J. Burke, "Establishing the input impedance requirements of ECG recording amplifiers," *IEEE Trans. Instrum. Meas.*, vol. 69, no. 3, pp. 825–835, Mar. 2020.
- [89] J. Xu, R. F. Yazicioglu, B. Grundlehner, P. Harpe, K. A. A. Makinwa, and C. Van Hoof, "A 160 μ W 8-channel active electrode system for EEG monitoring," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 6, pp. 555–567, Dec. 2011.
- [90] S. Hadri and B. Leung, "Impedance boosting techniques based on BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 28, no. 2, pp. 157–161, Feb. 1993.
- [91] S. Maji and M. J. Burke, "A micropower high-performance ECG recording amplifier," *IEEE Trans. Instrum. Meas.*, vol. 72, pp. 1–12, 2023.
- [92] *Medical Electrical Equipment. Part 2–27, Particular Requirements for the Basic Safety and Essential Performance of Electrocardiographic Monitoring Equipment*, Standard IEC 60601-2-27:2011, Int. Electrotechnical Standard (IEC), Int. Electrotech. Commission, Geneva, Switzerland, 2011. [Online]. Available: <https://webstore.iec.ch/publication/2638>
- [93] S. Stanslaski et al., "Design and validation of a fully implantable, chronic, closed-loop neuromodulation device with concurrent sensing and stimulation," *IEEE Trans. Neural Syst. Rehabil. Eng.*, vol. 20, no. 4, pp. 410–421, Jul. 2012.
- [94] J. Xu et al., "A 665 μ W silicon photomultiplier-based NIRS/EEG/EIT monitoring ASIC for wearable functional brain imaging," *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 6, pp. 1267–1277, Dec. 2018.
- [95] J. Xu, S. Mitra, C. Van Hoof, R. F. Yazicioglu, and K. A. A. Makinwa, "Active electrodes for wearable EEG acquisition: Review and electronics design methodology," *IEEE Rev. Biomed. Eng.*, vol. 10, pp. 187–198, 2017.
- [96] M. Tohidi, J. Kargaard Madsen, and F. Moradi, "Low-power high-input-impedance EEG signal acquisition SoC with fully integrated IA and signal-specific ADC for wearable applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 6, pp. 1437–1450, Dec. 2019.
- [97] C. Chang, S. A. Zahrai, K. Wang, L. Xu, I. Farah, and M. Onabajo, "An analog front-end chip with self-calibrated input impedance for monitoring of biosignals via dry electrode-skin interfaces," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 10, pp. 2666–2678, Oct. 2017.
- [98] I. Akita and M. Ishida, "A 0.06 mm² 14 nV/ $\sqrt{\text{Hz}}$ chopper instrumentation amplifier with automatic differential-pair matching," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 178–179.
- [99] M. A. Bin Altaf, C. Zhang, and J. Yoo, "A 16-channel patient-specific seizure onset and termination detection SoC with impedance-adaptive transcranial electrical stimulator," *IEEE J. Solid-State Circuits*, vol. 50, no. 11, pp. 2728–2740, Nov. 2015.
- [100] L. Zhang, T. Tang, J. H. Park, and J. Yoo, "A 0.012 mm², 1.5G Ω Z_{IN} intrinsic feedback capacitor instrumentation amplifier for bio-potential recording and respiratory monitoring," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2019, pp. 301–304.
- [101] T. Qu, Q. Pan, L. Liu, X. Zeng, Z. Hong, and J. Xu, "A 1.8–G Ω input-impedance 0.15– μ V input-referred-ripple chopper amplifier with local positive feedback and SAR-assisted ripple reduction," *IEEE J. Solid-State Circuits*, vol. 58, no. 3, pp. 796–805, Mar. 2023.
- [102] R. G. H. Eschauzier, R. Hogervorst, and J. H. Huijsing, "A programmable 1.5 V CMOS class-AB operational amplifier with hybrid nested Miller compensation for 120 dB gain and 6 MHz UGF," *IEEE J. Solid-State Circuits*, vol. 29, no. 12, pp. 1497–1504, Dec. 1994.
- [103] R. Wu, J. H. Huijsing, and K. A. A. Makinwa, "A current-feedback instrumentation amplifier with a gain error reduction loop and 0.06% untrimmed gain error," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2794–2806, Dec. 2011.

- [104] F. Butti, P. Bruschi, M. Dei, and M. Piotto, "A compact instrumentation amplifier for MEMS thermal sensor interfacing," *Anal. Integr. Circuits Signal Process.*, vol. 72, no. 3, pp. 585–594, Sep. 2012.
- [105] F. Butti, M. Piotto, and P. Bruschi, "A chopper instrumentation amplifier with input resistance boosting by means of synchronous dynamic element matching," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 4, pp. 753–764, Apr. 2017.
- [106] S. Thanapitak, W. Surakampontorn, and C. Sawigun, "A micropower chopper CBIA using DSL-embedded input stage with 0.4 V EO tolerance for dry-electrode biopotential recording," *IEEE Trans. Biomed. Circuits Syst.*, vol. 17, no. 3, pp. 458–469, Jun. 2023.
- [107] Q. Pan, T. Qu, B. Tang, F. Shan, Z. Hong, and J. Xu, "A $0.5\text{m}\Omega/\sqrt{\text{Hz}}$ 106 dB SNR 0.45 cm^2 dry-electrode bioimpedance interface with current mismatch cancellation and boosted input impedance of $100\text{ M}\Omega$ at 50 kHz," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 65, Feb. 2022, pp. 332–334.
- [108] A. Prasad, A. Chokhawala, K. Thompson, and J. Melanson, "A 120 dB 300 mW stereo audio A/D converter with 110 dB THD+N," in *Proc. 30th Eur. Solid-State Circuits Conf.*, Sep. 2004, pp. 191–194.
- [109] H. Chandrakumar and D. Marković, "An 80-mV_{pp} linear-Input range, $1.6\text{-G}\Omega$ input impedance, low-power chopper amplifier for closed-loop neural recording that is tolerant to $650\text{-mV}_{\text{pp}}$ common-mode interference," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 2811–2828, Nov. 2017.
- [110] H. Chandrakumar and D. Marković, "A $2.8\text{ }\mu\text{W}$ 80 mV_{pp} -linear input range 1.6-G input impedance bio-signal chopper amplifier tolerant to common-mode interference up to $650\text{ mV}_{\text{pp}}$," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb., Feb. 2017, pp. 448–449.
- [111] K. A. Makinwa, M. A. P. Pertijis, J. C. V. D. Meer, and J. H. Huijsing, "Smart sensor design: The art of compensation and cancellation," in *Proc. 37th Eur. Solid State Device Res. Conf.*, Sep. 2007, pp. 76–82.
- [112] M. A. P. Pertijis and W. J. Kindt, "A 140 dB-CMRR current-feedback instrumentation amplifier employing ping-pong auto-zeroing and chopping," *IEEE J. Solid-State Circuits*, vol. 45, no. 10, pp. 2044–2056, Oct. 2010.
- [113] Y. Wang et al., "A closed-loop neuromodulation chipset with 2-level classification achieving 1.5-V_{pp} CM interference tolerance, 35-dB stimulation artifact rejection in 0.5 ms and 97.8%-sensitivity seizure detection," *IEEE Trans. Biomed. Circuits Syst.*, vol. 15, no. 4, pp. 802–819, Aug. 2021.
- [114] S. Reich, M. Sporer, and M. Ortmanns, "A chopped neural front-end featuring input impedance boosting with suppressed offset-induced charge transfer," *IEEE Trans. Biomed. Circuits Syst.*, vol. 15, no. 3, pp. 402–411, Jun. 2021.
- [115] S. Reich, M. Sporer, and M. Ortmanns, "A self-compensated, low-offset voltage buffer for input impedance boosting in chopped neural front-ends," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Oct. 2020, pp. 1–5.
- [116] J. Lee, H. Kim, and S. Cho, "A 255 nW ultra-high input impedance analog front-end for non-contact ECG monitoring," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2017, pp. 1–4.
- [117] S.-I. Chang, S.-Y. Park, and E. Yoon, "Low-power low-noise pseudo-open-loop preamplifier for neural interfaces," *IEEE Sensors J.*, vol. 17, no. 15, pp. 4843–4852, Aug. 2017.
- [118] A. Demosthenous, I. Pachnis, D. Jiang, and N. Donaldson, "An integrated amplifier with passive neutralization of myoelectric interference from neural recording tripole," *IEEE Sensors J.*, vol. 13, no. 9, pp. 3236–3248, Sep. 2013.
- [119] M. Guermandi, R. Cardu, E. F. Scarselli, and R. Guerrieri, "Active electrode IC for EEG and electrical impedance tomography with continuous monitoring of contact impedance," *IEEE Trans. Biomed. Circuits Syst.*, vol. 9, no. 1, pp. 21–33, Feb. 2015.
- [120] E. Sackinger and W. Guggenbuhl, "A versatile building block: The CMOS differential difference amplifier," *IEEE J. Solid-State Circuits*, vol. SSC-22, no. 2, pp. 287–294, Apr. 1987.
- [121] J. Oreggioni, A. A. Caputi, and F. Silveira, "Current-efficient preamplifier architecture for CMRR sensitive neural recording applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 3, pp. 689–699, Jun. 2018.
- [122] L. Liu, D. Gao, Y. Tian, Y. Yu, and Z. Qin, "A low mismatch and high input impedance multi-channel time-division multiplexing analog front end for bio-sensors," *IEEE Sensors J.*, vol. 22, no. 7, pp. 6755–6763, Apr. 2022.
- [123] D. De Dorigo et al., "Fully immersible subcortical neural probes with modular architecture and a delta-sigma ADC integrated under each electrode for parallel readout of 144 recording sites," *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3111–3125, Nov. 2018.
- [124] S. Wang et al., "A 77-dB DR 16-Ch 2nd-order $\Delta-\Delta\Sigma$ neural recording chip with $0.0077\text{ mm}^2/\text{Ch}$," in *Proc. Symp. VLSI Circuits*, Jun. 2021, pp. 1–2.
- [125] K. A. Ng and P. K. Chan, "A CMOS analog front-end IC for portable EEG/ECG monitoring applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 11, pp. 2335–2347, Nov. 2005.
- [126] N. Tadic, D. Petric, M. Erceg, and A. Dervic, "CMRR enhancement in instrumentation amplifiers using an algorithmic approach with dynamic analog signal processing," *IEEE Trans. Instrum. Meas.*, vol. 70, pp. 1–17, 2021.
- [127] Y. H. Ghallab, W. Badawy, K. V. I. S. Kaler, and B. J. Maundy, "A novel current-mode instrumentation amplifier based on operational floating current conveyor," *IEEE Trans. Instrum. Meas.*, vol. 54, no. 5, pp. 1941–1949, Oct. 2005.
- [128] N. Koo and S. Cho, "A $24.8\text{-}\mu\text{W}$ biopotential amplifier tolerant to 15-V_{pp} common-mode interference for two-electrode ECG recording in 180-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 56, no. 2, pp. 591–600, Feb. 2021.
- [129] S. Zhang, X. Zhou, C. Gao, and Q. Li, "A 130-dB CMRR instrumentation amplifier with common-mode replication," *IEEE J. Solid-State Circuits*, vol. 57, no. 1, pp. 278–289, Jan. 2022.
- [130] Z. Zhou et al., "A high CMRR instrumentation amplifier employing pseudo-differential inverter for neural signal sensing," *IEEE Sensors J.*, vol. 22, no. 1, pp. 419–427, Jan. 2022.
- [131] N. Koo, H. Kim, and S. Cho, "A $43.3\text{-}\mu\text{W}$ biopotential amplifier with tolerance to common-mode interference of 18 V_{pp} and T-CMRR of 105 dB in 180-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 58, no. 2, pp. 508–519, Feb. 2023.
- [132] J. Li et al., "Non-contact electrocardiogram measuring method based on capacitance coupling electrodes with ultra-high input impedance," *Rev. Sci. Instrum.*, vol. 93, no. 3, Mar. 2022, Art. no. 034101.
- [133] R. Mandal, N. Babaria, J. Cao, and Z. Liu, "Adaptive and wireless recordings of electrophysiological signals during concurrent magnetic resonance imaging," *IEEE Trans. Biomed. Eng.*, vol. 66, no. 6, pp. 1649–1657, Jun. 2019.
- [134] T. Degen and H. Jackel, "A pseudodifferential amplifier for biologic events with DC-offset compensation using two-wired amplifying electrodes," *IEEE Trans. Biomed. Eng.*, vol. 53, no. 2, pp. 300–310, Feb. 2006.
- [135] J. Lee et al., "A 0.8-V $82.9\text{-}\mu\text{W}$ in-ear BCI controller IC with 8.8 PEF EEG instrumentation amplifier and wireless BAN transceiver," *IEEE J. Solid-State Circuits*, vol. 54, no. 4, pp. 1185–1195, Apr. 2019.



Feng Yan (Graduate Student Member, IEEE) received the B.Sc. degree in physics of electronic engineering from Yuncheng University, Shanxi, China, in 2018, and the M.Sc. degree in physics and electronics from Hunan Normal University, Hunan, China, in 2021. He is currently pursuing the Ph.D. degree with Sun Yat-sen University, Shenzhen, China.

His current research interests include circuit design of analog front end for biomedical applications and sensor interfaces.



Jingjing Liu (Member, IEEE) received the B.Eng. (Hons.) and M.Eng. degrees from the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, in 2003 and 2005, respectively, and the D.Phil. degree from the Department of Engineering Science, University of Oxford, Oxford, U.K., in 2009.

From 2009 to 2010, he was a Postdoctoral Research with the University of Oxford. He was a Researcher with Peking University Shenzhen Research Institution for a few years. He is currently an Associate Professor with Sun Yat-sen University, Shenzhen, China. His research interests include low-power smart micro-sensor integrated circuit design, image sensors, biomedical sensors, and energy harvesting circuits.