# A Second-Order Dual-Charge-Pump Passive Noise-Shaping SAR ADC for Medical Implant Devices

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***Abstract*—A 14.14bit 2MS/s Second-Order Passive Noise-Shaping Successive Approximation Register Analog-to-Digital Converter (NS SAR ADC) is proposed in this paper. The structure utilizes techniques such as charge pumps and multi-input comparator with a gain to compensate for the signal loss during the noise shaping process. It incorporates two zero points at 0.8 in the noise transfer function (NTF), which enhances the noise shaping capability. This ADC is designed using a standard 180nm CMOS process. The simulation results show that the ADC consumes 56.8 μ W, achieving a signal-to-noise-and-distortion ratio (SNDR) of 86.75 dB and a spurious-free dynamic range (SFDR) of 97.16 dB with an oversampling ratio (OSR) of 8 at 2MS/s, resulting in an Schreier figure of merit (FoMs) of 180.18dB.**

***Keywords—SAR ADC, Noise-Shaping, charge pump, multi-input comparator.***

## I. INTRODUCTION

Recently, Electrocardiogram (ECG) devices with low power consumption, high resolution, and portability have gradually been reported. However, the power consumption of the front-end module, the ADC module, and the DSP module greatly limits the application of the portable ECG devices for the long-term heart monitoring [1]. As shown in Fig. 1, the ADC is a fundamental and critical component between the sensor and the analog front-end circuit in biomedical applications. Its power consumption and accuracy greatly determine the application scenarios and scope of the entire system.

Due to the inherent low power consumption advantage of SAR ADCs, their precision is difficult to achieve beyond 10 bits, and even if it does exceed 10 bits, the energy efficiency becomes very poor [2]. To improve accuracy, researchers have proposed a noise-shaping SAR ADC structure based on sigma-delta modulation. Therefore, noise-shaping SAR ADCs inherently possess the advantages of low power consumption and high precision. In the NS-SAR ADC structure, an active integrator filter based on the amplifier structure effectively constructs a clear noise transfer function, bringing more significant low-frequency suppression effects for the design of NTF, thereby enhancing the performance of noise shaping and the precision of the ADC. However, the amplifier circuit increases the complexity of the entire system design and additional power consumption. At the same time, the amplifier is more sensitive to process variations, and the changes of the gain could reduce the stability of the circuit.

To solve the mentioned issues, this paper proposes a second-order passive noise-shaping structure utilizing a charge pump, achieving 14.12 bits at a 2MS/s sampling rate. The rest of the paper is structured as follows: Section II analyzes the challenges faced by the passive noise shaping. Section III describes the proposed second-order dual-charge-pump passive Cascade of Integrators with Feed-Forward (CIFF) NS-SAR ADC. Section IV gives the simulation results, and Section V concludes the paper.

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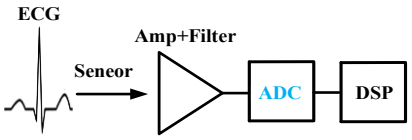


**Fig. 1** The ECG signal acquisition and processing system.

## II. ANALYSIS OF CHALLENGES FACED BY PASSIVE NOISE SHAPING

In the passive noise shaping circuits, the sharing and transfer of charges inevitably result in signal loss, causing the non-ideal behavior of the passive integrators and affecting the noise shaping effect, which ultimately impacts the accuracy of the ADC. As shown in Fig. 2, Guo presents a classic design of a first-order passive loop filter [3], which employs a multi-input comparator with a gain to compensate for the signal loss during the transfer of residual voltage between capacitors. Assuming the comparator provides a relative gain of $g$, $C_1 = C_3 = C$, $C_2 = a/(1-a)C$, where $C$ is the total capacitance of the DAC and $a$ is capacitance ratio. The expression for the integrated voltage $V_{\text{int}}$ after charge sharing between the sampling capacitor and the integration capacitor in the z-domain for the residual voltage $V_{\text{RES}}$ can be derived as follows:

$$V_{\text{int}}(z) = \frac{(1-a)a}{1-(1-a)z^{-1}} V_{RES}(z) \cdot \tag{1}$$

So the noise transfer function NTF is

$$\text{NTF} = \frac{1-(1-a)z^{-1}}{1-(1-a)(1-ga)z^{-1}} \cdot \tag{2}$$

The NTF reveals a zero at $z$=1−$a$ and a pole at $z$=(1−$a$)(1−$ga$).

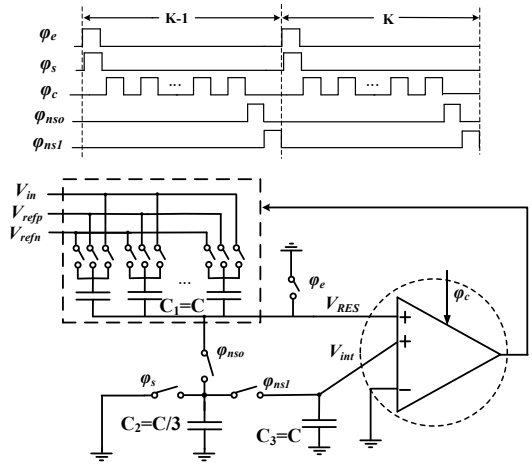


**Fig. 2** First-Order Passive NS-SAR ADC Structure.

With the gain $g$ set to $g$=1/$a$, and given $a$=1/4, the first-order NTF can be simplified to be $(1-0.75z^{-1})$. The presence of a zero at 0.75 leads to a -12 dB suppression at direct current (DC).

To improve noise shaping, the second-order passive NS-SAR ADC incorporates an additional set of integrator capacitors $C_{int2}$ and upgrades the comparator to a six-input design [4]. This configuration creates two zeros at 0.75 in the NTF, enabling second-order noise shaping with -24 dB suppression at DC. However, it necessitates precise aspect ratios of 1:4:16 for the comparator's input pairs. The large input pairs increase power consumption and introduce parasitic capacitance, potentially degrading the ADC accuracy and comparator speed, representing a key limitation in passive noise shaping.

## III. The Proposed Second-Order Dual-Charge-Pump Passive NS-SAR ADC

This paper proposes a second-order passive noise-shaping structure using the charge pump principle, which achieves high quantization precision by creating two zeros at 0.8 with a comparator gain ratio of 1:2.5:6.25.

### A. Modulator Structure

Fig. 3 illustrates the proposed second-order dual-charge-pump passive CIFF NS-SAR ADC structure introduced. For simplicity of description, the single-ended configuration is shown here, whereas the actual circuit is a fully differential 10-bit SAR ADC. Compared to the architecture proposed in [4], this work has two improvements. First, a charge pump with 2× gain is integrated at both the sampling capacitor $C_{RES}$ and the second-order integrator capacitor $C_{INT2}$. The relative gain for the passive integrators is supplied by the two charge pumps in conjunction with the multi-input comparator. The charge pump at the sampling capacitor provides a 2× gain to compensate for the signal loss, and the second charge pump on $C_{INT2}$ offers a 2× gain to compensate for the integration loss. As depicted in Fig. 4, this results in a reduced aspect ratio of 1:2.5:6.25 for the input pairs of the strong ARM latch comparator, thereby eliminating the large size of the input pairs. Second, to enhance the noise shaping effect, the capacitance values are set to $C_{RES}$ = $C_{INT1}$ = $C_{INT2}$ = 1/4$C$, with $C$ being the total capacitance of the CDAC array. The proposed second-order NS-SAR ADC architecture adds only an additional 0.75$C$ compared to the fundamental SAR ADC without NS, and this modest increase in capacitance

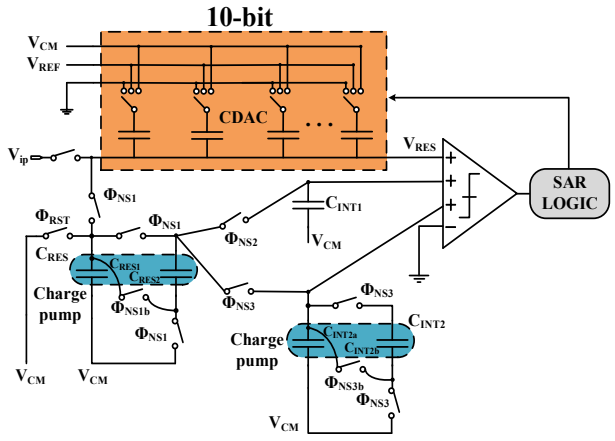


**Fig. 3** The proposed second-order dual-charge-pump passive NS-SAR ADC.

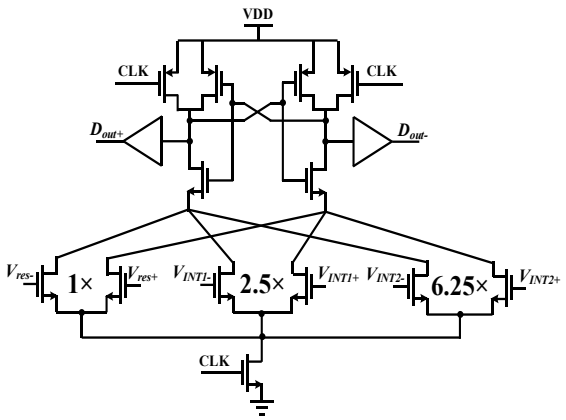


**Fig. 4** The comparator with the aspect ratio of 1:2.5:6.25 for the three input pairs.

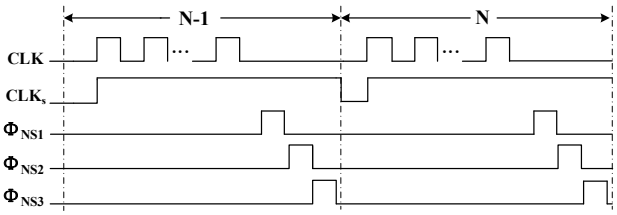


**Fig. 5** The timing diagram of the proposed second-order NS-SAR ADC.

contributes to power consumption reduction and less chip footprint compared to [4].

Fig. 5 illustrates the operational timing of this structure. During the ($N$-1)th quantization cycle, the ADC first performs a standard 10-bit SAR ADC conversion process. After the DAC completes the final voltage flip, $\Phi_{NS1}$ is activated, allowing $C_{RES}$ to sample the residual voltage. $\Phi_{NS1}$ then turns off, and the charge pump initiates the boosting operation. $\Phi_{NS2}$ and $\Phi_{NS3}$ are sequentially activated, enabling the sampling capacitor $C_{RES}$ to perform the integration with $C_{INT1}$ and $C_{INT2}$. In the $N$th quantization cycle, the residual integration voltage from the ($N$-1)th cycle is engaged in the entire SAR ADC quantization process.

### B. Transfer Function Analysis

Assuming $2C_{RES1}$ = $2C_{RES2}$ = $C_{INT1}$ = $2C_{INT2a}$ =$2C_{INT2b}$ =$a/(1-a)C$, with $C$ being the DAC's total capacitance, and given the first-order integration path's relative gain is $g_1$ and the second-order's is $g_2$, the corresponding signal flow graph for this structure is depicted in Fig. 6. The NTF's general expression can be derived as follows:

$$\mathrm{NTF}=\frac{[1-(1-a)z^{-1}]^2}{1+(1-a)(4g_2a^2+2g_1a-2)z^{-1}+(1-a)^2(1-2g_1a)z^{-2}}. \quad (3)$$

With $g_1$=2.5, $g_2$=6.25, and $a$=0.2, these values are substituted into (3) and it can be simplified to be (4).

$$\mathrm{NTF}=(1-0.8z^{-1})^2 \quad (4)$$

According to (4), the NTF of this design has two zeros located at 0.8, leading to a more significant reduction in low-frequency noise. The position of these zeros is entirely determined by the ratio of the capacitors, making this NTF minimally affected by PVT (Process, Voltage, Temperature) variations and highly robust. Compared to the first-order NS-SAR ADC architecture in [3], this structure's NTF does not have poles, thus offering greater system stability. Compared to [4], this design has larger zeros, indicating better noise

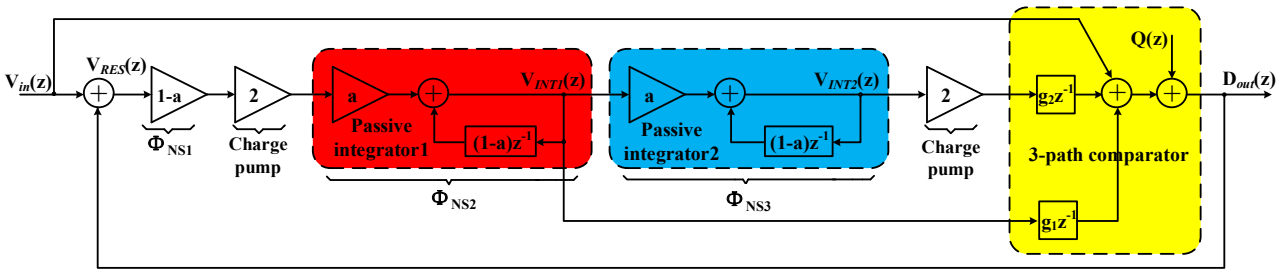


**Fig. 6** The signal flow diagram of the proposed second-order NS-SAR ADC.

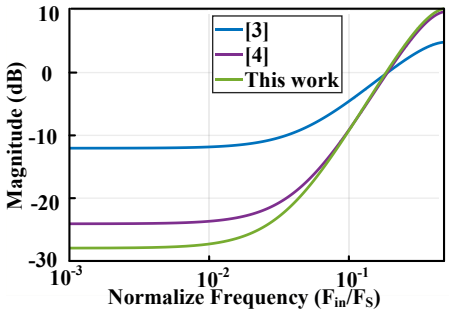


**Fig. 7** The NTF frequency responses of different architectures.

shaping. Fig. 7 compares the NTF frequency responses, showing the proposed structure's NTF provides a more pronounced high-pass filtering effect, with approximate -28 dB suppression at DC.

## IV. Simulation Results of the Proposed ADC

This paper presents a noise-shaping SAR ADC architecture designed in a 180nm process. The ADC is simulated with a 1.2V power supply, a sampling frequency of 2MHz, and an OSR of 8, Fig. 8 displays the ADC's output spectrum for a 93.75kHz sine wave input with -0.06dBFS. The output spectrum clearly demonstrates the second-order noise shaping, pushing low-frequency quantization noise to the high-frequency range. Within the target bandwidth (125kHz), the ADC achieves an SNDR of 86.75dB, an effective bit resolution (ENOB) of 14.12 bits, and an SFDR of 97.16dB. The total power consumption of the proposed ADC is 56.8µW. According to the FoM definition, the Walden FoM for the NS-SAR ADC is calculated to be 3.19 fJ/Conv.-step, and the corresponding Schreier FoM is 180.18dB. Table I lists and compares the simulation results with previous works, indicating that the proposed second-order dual-charge-pump passive NS-SAR ADC not only achieves higher precision but also exhibits superior energy efficiency, which is particularly advantageous for bio-medical electronic applications.

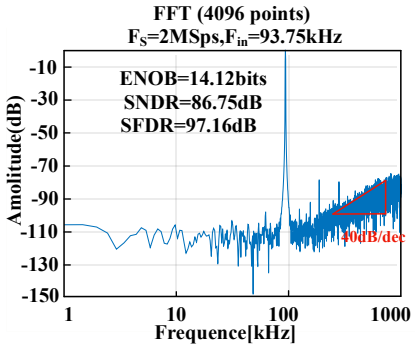


**Fig. 8** The output spectrum of the proposed NS-SAR ADC.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON.

| Specifications | [4] | [5] | [6][a] | **This work[a]** |
|---|---|---|---|---|
| Process | 40nm | 65nm | 180nm | **180nm** |
| Supply (V) | 1.1 | 1 | 0.8 | **1.2** |
| ADC Type | NS-SAR | SAR | Time | **NS-SAR** |
| Fs (MHz/s) | 8.4 | 0.5 | 0.004 | **2** |
| BW(kHz) | 262 | - | - | **125** |
| ENOB (bit) | 12.7 | - | 10.9 | **14.12** |
| SNDR (dB) | 78.4 | 71.8 | 67.4 | **86.75** |
| SFDR (dB) | - | 101.2 | - | **97.16** |
| Power (µW) | 143 | 9.14 | 0.06812 | **56.8** |
| $FoM_W$ (fJ/Conv.-step) | - | 5.7 | 8.91 | **3.19** |
| $FoM_S$ (dB) | 171 | 176.2 | - | **180.18** |

[a.] Simulation Results

## V. Conclusion

This paper presents a 14.12-bit 2MS/s NS SAR ADC in 180nm CMOS technology. The proposed structure utilizes a charge pump and a multi-input comparator with a gain to compensate for signal loss during the noise shaping process, thereby enhancing the noise shaping capability and improving the quantization accuracy. The simulation result shows that the proposed ADC achieves a Schreier FoM of 180.18dB, which is highly suitable for medical electronic applications.

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