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An Ultra-Low Power Time-Domain Temperature Sensor for IoT Applications

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***Abstract*—This paper proposed an ultra-low power time-domain temperature sensor circuit for IoT applications. It uses 2-T structures to generate reference voltage and complementary-to-absolute-temperature (CTAT) voltage. The reference voltage produces reference current by using current mirror to charge the capacitor. Then the voltage of capacitor is compared with the CTAT voltage to generate a temperature-dependent pulse. The pulse width is then digitized to represent the temperature. The temperature sensor is designed using 0.18μm CMOS process. The simulation results show that it measures temperature from -10°C to 60°C from 1V supply voltage. The power it costs is 570nW at a conversion speed of 100 Sa/s.**

Keywords—temperature sensor, ultra-low power, TDC

I. INTRODUCTION

IoT sensors develop towards ultra-low power, because it will extend the sensor life, or even can be self-powered by the energy harvested from environment. Traditional temperature sensor utilizes bipolar junction transistor (BJTs) as temperature sensing devices [1]-[2]. As for BJT, V_{BE} is complementary to absolute temperature, and the difference between V_{BE1} and V_{BE2}, is proportional to absolute temperature. Then ADC is used to convert the voltage to digital output. This kind of temperature sensor could achieve high accuracy at the cost of power consumption, and therefore it is not suitable for low power applications of IoT sensors.

MOSFETs could also be used as temperature sensing. It generates reference voltage V_{ref} and V_{PTAT} / V_{CTAT}, then the two voltages are fed into time to digital converter (TDC) [3], or frequency to digital converter (FDC) [4]. This topology decreases power consumption, but it is not as accurate as BJT-based temperature sensors. This work proposed a time domain ultra-low power temperature sensor. Two simple 2-T structures are employed to generate temperature-independent voltage and temperature-dependent voltage respectively. Then the two voltages are converted to digital output through TDC. In this paper. Section II describes temperature sensor circuit implementation. Section III describes the digital circuit. Section IV shows the simulation results. Section V shows the conclusion.

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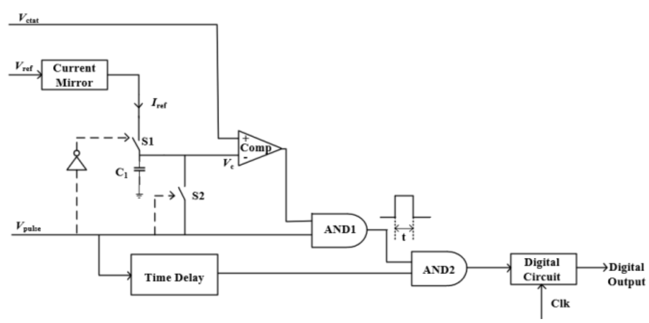

Fig. 1. The block diagram of the proposed temperature sensor.

II. TEMPERATURE SENSOR CIRCUIT IMPLEMENTATION

Fig. 1 shows the block diagram of the proposed temperature sensor. Firstly, voltage generator block produces reference voltage V_{ref} and CTAT voltage V_{ctat}. V_{ref} is converted to a charging current I_{ref} and V_{pulse} controls whether the capacitor C1 is charged or discharged. When V_{pulse} is high, switch S1 is closed and switch S2 is open, C1 is charged through charge current I_{ref}. When V_{pulse} is low, switch S1 is open and switch S2 is closed, C_1 is discharged rapidly. During the charging process, if $V_c<V_{ctat}$, the comparator output is high. If $V_c>V_{ctat}$, the comparator output is low. The AND1 gate outputs the required time t when V_c is charged to be equal to V_{ctat}. Because of the temperature dependence of V_{ctat}, the time is proportional to absolute temperature.

A. Voltage Reference Generator

The voltage reference generator circuit is shown in Fig. 2 [5]. M1 is a native NMOS with smaller threshold voltage and M2 is a normal NMOS. The two transistors M1 and M2 operate in the subthreshold region. The circuit formula of subthreshold region transistor can be expressed as

$$I_{\mathrm{sub}} = \mu C_{\mathrm{ox}} \frac{W}{L}(m-1)V_T^{\,2} \exp\left(\frac{V_{\mathrm{gs}}-V_{\mathrm{th}}}{mV_T}\right)\left[1-\exp\left(\frac{-V_{\mathrm{ds}}}{V_T}\right)\right] \tag{1}$$

where m is subthreshold slope factor, V_{th} is threshold voltage. V_T is thermal voltage. u is mobility, C_{ox} is oxide capacitance. W is the transistor width, L is the transistor length. V_{gs} is the gate-source voltage of MOS, and V_{ds} is the drain-source voltage of MOS.

When $V_{\mathrm{ds}}>>3V_{\mathrm{T}}$, the term $\exp\left(\frac{-V_{ds}}{V_T}\right)$ could be ignored. In Fig. 2, M1 and M2 current can be expressed by (2) and (3) respectively.

$$I_1 = \mu_1 C_{\mathrm{ox1}} \frac{W_1}{L_1}(m_1-1)V_T^{\,2} \exp\left(\frac{0-V_{\mathrm{ref}}-V_{\mathrm{th1}}}{m_1 V_T}\right) \tag{2}$$

$$I_2 = \mu_2 C_{\mathrm{ox2}} \frac{W_2}{L_2}(m_2-1)V_T^{\,2} \exp\left(\frac{V_{\mathrm{ref}}-V_{\mathrm{th2}}}{m_2 V_T}\right) \tag{3}$$

Since I_1 is equal to I_2, we can get

$$V_{\mathrm{ref}} = \frac{m_1 m_2}{m_1+m_2}\left(V_{\mathrm{th2}}-V_{\mathrm{th1}}\right)+\frac{m_1 m_2}{m_1+m_2}V_T \ln\left(\frac{\mu_1 C_{\mathrm{ox1}} W_1 L_2}{\mu_2 C_{\mathrm{ox2}} W_2 L_1}\right) \tag{4}$$

According to (4), we can see that the slope of (V_{th2}-V_{th1}) with respect to temperature is positive or negative. The slope of V_{T} with respect to temperature is positive, but we can adjust W_1, W_2, L_1, L_2 to make the slope of the second term in (4) with respect to temperature is negative or positive. Then it can be obtained that V_{ref} does not depend on temperature by adjusting W_1, W_2, L_1, L_2, as shown in Fig. 3.

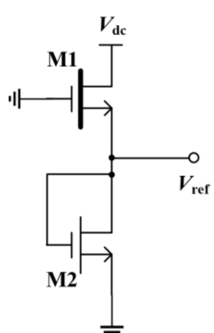

Fig. 2. Reference volage circuit.

The result is shown in Fig. 3, we can see that the temperature changes by 70°C, and the voltage changes by 0.474mV.

B. CTAT Voltage V_{ctat} Generator

The CTAT voltage is generated by 2-T structure as shown in Fig. 4 [4]. But, there is some difference from [4] that M1 is native NMOS, and with temperature increasing, its operating region transitions from the subthreshold region to the saturation region. M2 works in subthreshold region. The result is shown in Fig. 5. We can see that the linearity of voltage with respect to temperature is good.

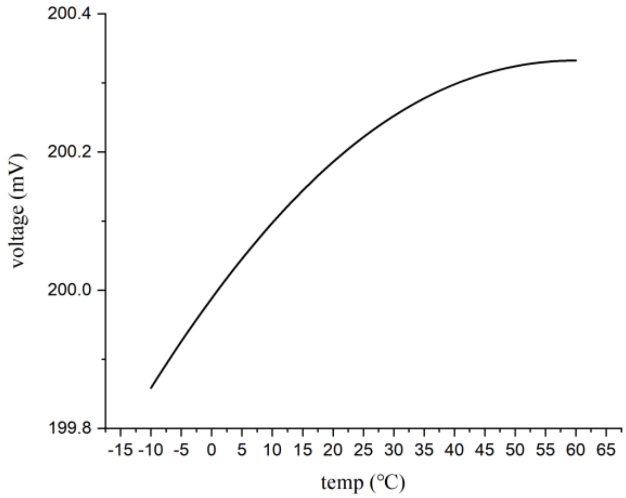

Fig. 3. The simulation result of reference voltage.

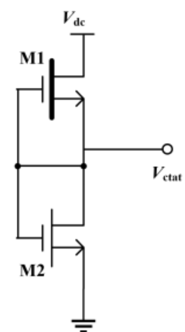

Fig. 4. CTAT voltage generator circuit.

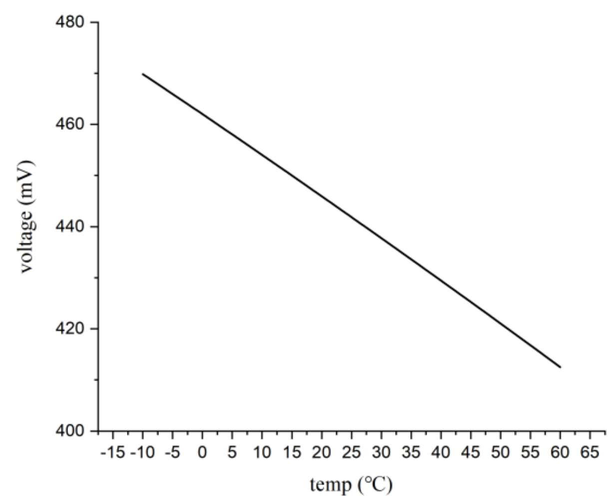

Fig. 5. The simulation result of CTAT voltage.

C. Charging Current Generator and Comparator

Fig. 6 shows the charging and discharging circuit. The reference voltage V_{ref} is used to drive M1 and generates a current. It must be noticed that M1 works in triode region, so the supply voltage should be stable and low-noise. Current mirrors are used to reduce the value of current. And this current is reduced by many times and minimized to M7 in order to save power and reduce the size of C1. Among the charging phase, the voltage of V_c increases, and as mentioned before, V_c and V_{ctat} will be compared through a comparator [6] shown in Fig. 7. During the discharging phase, the capacitor C1 will be discharged through S2, and the discharging speed should be as fast as possible.

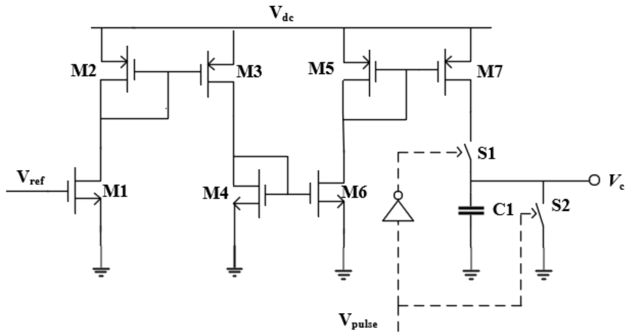

Fig. 6. Charging and discharging circuit.

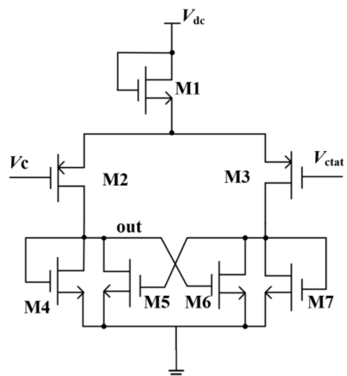

Fig. 7. The schematic of comparator circuit.

D. Time Delay Circuit

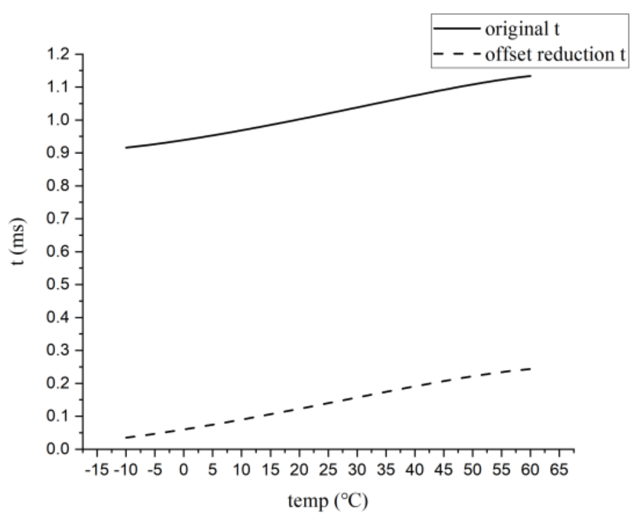

Fig. 8. Width offset reduction achieved by time delay circuit. The upper line is original t, and the lower line is offset reduction t.

As mentioned before, the time t is proportional to absolute temperature, but there is a big DC offset which will cause the considerable waste of the counter bit resources. As shown in Fig. 8, when the temperature is -10℃, the width of pulse is not zero. So we utilizes time delay circuit that can delay about 800us or 900us to eliminate the extra time. The delay time is not very exact, but it won't affect its effect. The time delay circuit is shown in Fig. 9. M1~M3 are current mirrors, which copy the current from the charging current generator. In Fig. 9, M3 and M7 have the same current, which are used to charge and discharge C2. Therefore the rising time and falling time of V_A voltage are the same as shown in Fig.10. With time delay circuit, the DC offset time is decreased obviously as shown in Fig. 8.

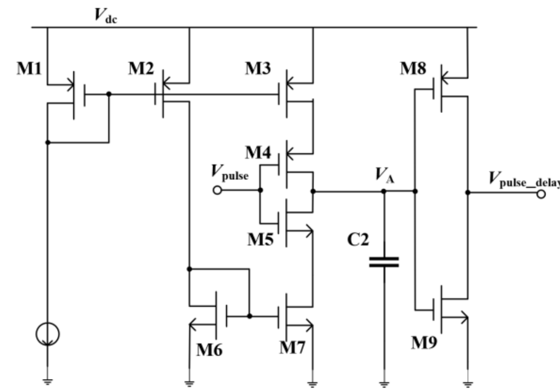

Fig. 9. The schematic of time delay Circuit.

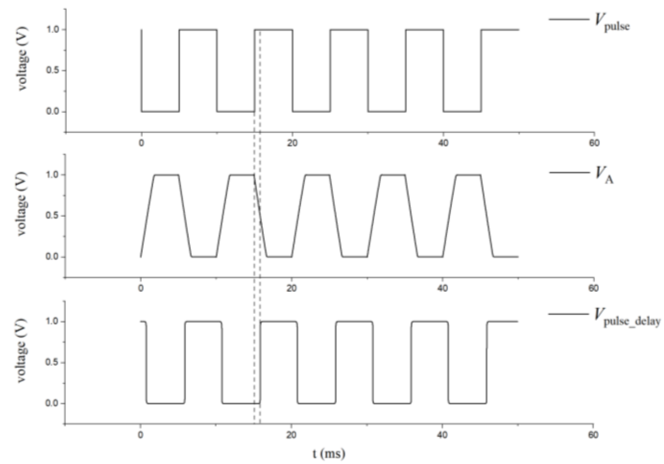

Fig. 10. The waves of time delay circuit.

III. Digital Circuit

The digital circuit consisting of counter and DFF is shown in Fig. 11.

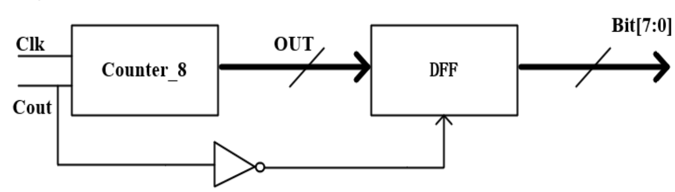

Fig. 11. The digital circuit.

Cout is the pulse whose width can be used to digitize temperature, and clk is the off-chip clock. Counter_8 is used to digitize the width of Cout, and DFF is used to storage the output of Counter_8.

IV. Simulation Results of Temperature Sensor

Fig. 12 is the simulation of the voltage of capacitor. In Fig. 12, there are 71 simulation lines about charging and discharging process for the temperature from -10~60℃.

We can see that when the pulse is high, capacitor will be charged, and when the pulse is low, capacitor will be discharged. We only take the charge part into consideration, and the transitions of lines don't affect the linearity of pulse width. According to simulation, the slope stays constant, but the points where the capacitor starts to be charged are different as shown in Fig. 12. However, the voltage value of the point and temperature are linearly related, so the linearity with respect to temperature of charging time is not influenced.

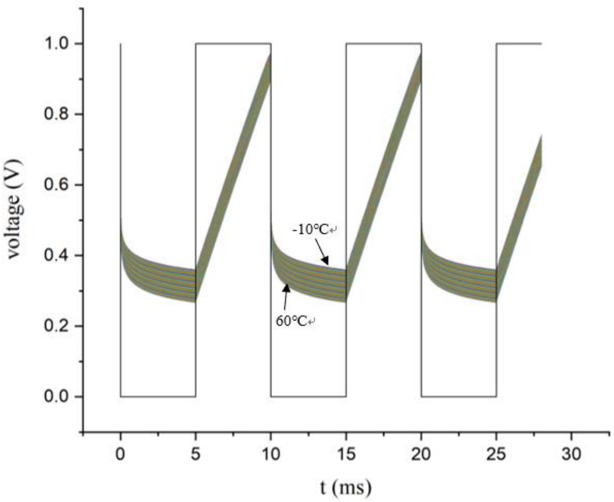

Fig. 12. The simulation results of Vc during charging and discharging phase.

And according to simulation, the digital output with respect to different temperature from -10℃~60℃ is shown in Fig. 13. Table I compares this work with other designs.

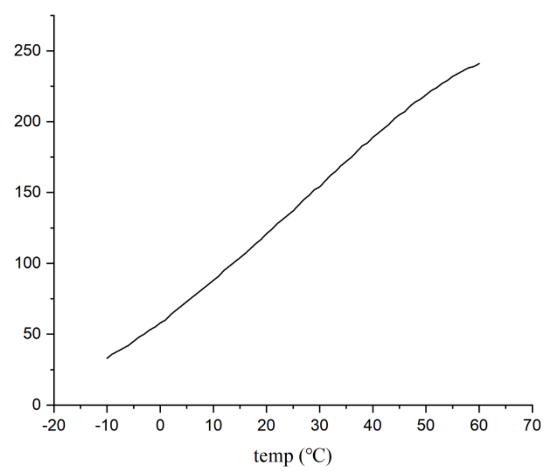

Fig. 13. The output of the digital circuit.

TABLE I. Comparison with other Designs

Parameters	This Work	[4]	[7]	[8]	[9]
Technology (μm)	0.18	0.18	0.18	0.18	0.18
Supply Voltage	1V	1.2V	1.6V,1.8V	1.8V	0.6V
Temperature Range(℃)	-10~60	0~100	-20~80	-20~80	0~100
Power	570nW	71nW	820nW@1.8V 480nW@1.6V	1.99μW[1]	75nW
Conversion Speed	100Sa/s	/	1.25Sa/s	/	/

1. Power of the on-chip clock is included.

V. Conclusion

This paper proposed an ultra-low power Time-Domain temperature sensor using 0.18μm CMOS technology. V_{ref} and V_{ctat} are converted by TDC consisting of capacitor charging and discharging circuit, comparator, time delay circuit. Then a pulse whose width is linear with temperature is sent to the digital circuit where there are counter and DFF. The output of the digital circuit is 8bits. And according to the simulation result, this temperature sensor could measure temperature from -10℃ ~60℃, and it can achieve ultra-low power operation. It costs 570nW at a conversion speed of 100 Sa/s.

References

[1] M. Law, S. Lu, T. Wu, A. Bermak, P. Mak and R. P. Martins, "A 1.1 uW CMOS Smart Temperature Sensor With an Inaccuracy of ±0.2 ℃ (3σ) for Clinical Temperature Monitoring," in *IEEE Sensors Journal,* vol. 16, no. 8, pp. 2272-2281, April15, 2016.

[2] A. Bakker and J. H. Huijsing, "Micropower CMOS temperature sensor with digital output," in *IEEE Journal of Solid-State Circuits,* vol. 31, no. 7, pp. 933-937, July 1996.

[3] Poki Chen, Chun-Chi Chen, Chin-Chung Tsai and Wen-Fu Lu, "A time-to-digital-converter-based CMOS smart temperature sensor," in *IEEE Journal of Solid-State Circuits,* vol. 40, no. 8, pp. 1642-1648, Aug. 2005.

[4] S. Jeong, Z. Foo, Y. Lee, J. Sim, D. Blaauw and D. Sylvester, "A Fully-Integrated 71 nW CMOS Temperature Sensor for Low Power Wireless Sensor Nodes," in *IEEE Journal of Solid-State Circuits,* vol. 49, no. 8, pp. 1682-1693, Aug. 2014.

[5] M. Seok, G. Kim, D. Blaauw and D. Sylvester, "A Portable 2-Transistor Picowatt Temperature-Compensated Voltage Reference Operating at 0.5 V," in *IEEE Journal of Solid-State Circuits,* vol. 47, no. 10, pp. 2534-2545, Oct. 2012.

[6] A. Azam, Z. Bai and J. S. Walling, "An Ultra-Low Power CMOS Integrated Pulse-Width Modulated Temperature Sensor," in *IEEE Sensors Journal,* vol. 21, no. 2, pp. 1294-1304, 15 Jan.15, 2021.

[7] W. Song, J. Lee, N. Cho and J. Burm, "An Ultralow Power Time-Domain Temperature Sensor With Time-Domain Delta–Sigma TDC," in *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 64, no. 10, pp. 1117-1121, Oct. 2017.

[8] Y. Chen et al., "A +0.66/−0.73 ℃ Inaccuracy, 1.99-μW Time-Domain CMOS Temperature Sensor With Second-Order ΔΣ Modulator and On-Chip Reference Clock," in *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 67, no. 11, pp. 3815-3827, Nov. 2020.

[9] X. Wang, P. -H. P. Wang, Y. Cao and P. P. Mercier, "A 0.6V 75nW All-CMOS Temperature Sensor With 1.67m℃/mV Supply Sensitivity," in *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 64, no. 9, pp. 2274-2283, Sept. 2017.