A Sub-0.9-ps Static Phase Offset 500 MHz Delay-Locked Loop With a Large Gain Phase Detector

Jingjing Liu, *Member, IEEE*, Ruihuang Wu, Haoning Sun, Bingjun Xiong, Feng Yan, Kangkang Sun, Zhipeng Li, and Jian Guan

***Abstract*—This article presents an analog delay-locked loop (DLL) designed for high-precision measurement applications, featuring low static phase offset (SPO) and fast locking speed, such as time-to-digital converters (TDCs) and analog-to-digital converters (ADCs). A large gain and dead-zone free phase detector (PD) is proposed. When the DLL reaches the locked state, the phase error between the two input signals of the PD can be reduced to 0.53 ps (0.095°), which has an 18-time improvement compared to the conventional DLL. Therefore, the SPO of the entire DLL can be effectively reduced to be less than 0.87 ps. Furthermore, the auxiliary circuit, consisting of a large phase difference detector (LPDD) and fast-adjusting branches (FABs), accelerates the DLL's locking process to 42 clock cycles and improves the locking speed by 4.1 times. Designed by a standard 180 nm CMOS technology, the DLL occupies an area of 106.1 × 93.3 μm. It achieves low power consumption of 1.89 mW at 500 MHz, and the root mean square (rms) jitter and P-P jitter are 1.01 and 6.26 ps, respectively.**

***Index Terms*—Delay-locked loop (DLL), fast-locking, low jitter, low power, low static phase offset (SPO), phase detector (PD).**

I. Introduction

DELAY-LOCKED loop (DLL) is commonly employed in time-to-digital converters (TDCs) [1], [2] and analog-to-digital converters (ADCs) [3]. In these applications, the DLLs need to possess low static phase offset (SPO) and low jitter, thus ensuring high accuracy of the system. Additionally, the DLLs find extensive applications in clock generators [4], [5], [6] and clock data recovery (CDR) circuits [7], [8]. In these applications, the DLL needs to possess fast locking speed and low power consumption, thus the system can rapidly make a transition from a low-power sleep state to an active state, thereby conserving power during idle periods and facilitating efficient operation. Therefore, SPO, locking speed, power, and jitter are all important performance metrics for evaluating a DLL. The DLLs can be categorized into digital DLLs and analog DLLs. The digital DLLs utilize digital-controlled delay lines (DCDLs) to introduce discrete delays to the input reference clock. The minimum delay of the DCDL depends on the number of bits in its control sequence. On the other hand, the analog DLLs employ voltage-controlled delay lines (VCDLs), and a continuous analog control voltage enables the VCDL to generate a continuous delay. So VCDLs have a typically exhibit smaller SPO than digital DLLs, possibility of fine-tuning the delay. As a result, analog DLLs which make them more suitable for applications requiring high phase accuracy.

SPO of DLLs refers to a fixed phase error between the final stage's output clock and the input reference clock when the circuit is locked. It typically arises from non-ideal factors such as charge pump (CP) current mismatch and different switching times between charging and discharging branches. Therefore, two operational amplifiers are used to clamp the drains of the MOS transistors in the current mirror, ensuring a high matching of charging and discharging currents of the CP [9]. However, the use of operational amplifiers increases the power consumption and circuit complexity. Chopped PFD technique [10] and auto-zero technique [11] can also reduce SPO. However, the chopped PFD has limited improvement on SPO, and further reduction of SPO still requires a highly matched CP. And the auto-zero technique needs a μs-level calibration time to achieve a sub-ps SPO. In this article, a large gain and dead-zone free phase detector (PD) is proposed. The proposed PD exhibits a gain larger than two when approaching the locked state and effectively reduces the SPO. Additionally, the auxiliary circuit, consisting of a large phase difference detector (LPDD) and fast-adjusting branches (FABs), is proposed to increase the DLL's locking speed. These techniques work together and make the proposed DLL more suitable for low-power and high-precision applications. This article is organized as follows. Section II introduces the architecture of the proposed DLL. Section III discusses the detailed principles of each module. Section IV discusses the impact of the proposed large gain PD on the jitter of the proposed DLL. Section V presents the post-layout simulation results, while Section VI provides a summary.

II. Architecture of the Proposed DLL

Fig. 1 illustrates the system structure of the proposed DLL. The key blocks of the DLL include the control voltage regulation circuitry, VCDL, and bias circuit. The control voltage regulation circuitry is used to adjust the control voltage V_C. To expedite system lock-in, this structure incorporates

Received 31 October 2024; revised 19 February 2025 and 23 April 2025; accepted 27 April 2025. This work was supported by the National Natural Science Foundation of China under Project 62174181. *(Corresponding author: Jingjing Liu.)*

The authors are with the School of Electronics and Communication Engineering, Sun Yat-sen University, Shenzhen 518107, China (e-mail: liujj77@mail.sysu.edu.cn).

Digital Object Identifier 10.1109/TVLSI.2025.3566739

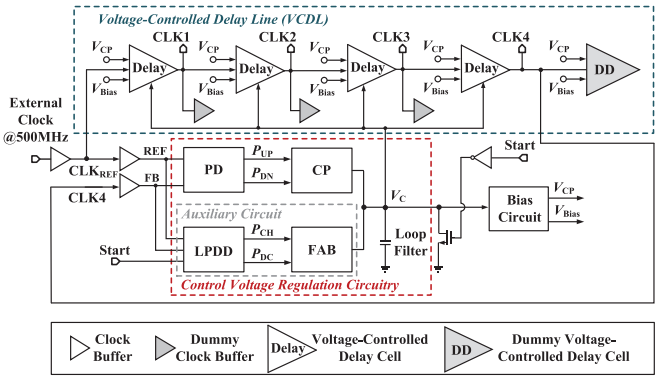

Fig. 1. Structure diagram of the proposed DLL.

additional components beyond the PD, CP, and loop filter (LF). A LPDD and FABs are proposed, which constitute the proposed auxiliary circuit. During power-on or reset, the start signal remains at a low level for a certain period before transitioning back to a high level, resetting the control voltage and establishing the appropriate starting conditions for DLL operation. When there is a significant phase error between the REF and FB, the LPDD generates pulse signals P_{CH} and P_{DC} to activate the FAB and allows V_C to be rapidly adjusted. As the system approaches the locked state, the LPDD and FAB stop operating. Only the PD detects the phase difference and controls the CP to either charge or discharge the LF, fine-tuning the V_C. The LF and bias circuit work together to generate the necessary control signals (V_C, V_{CP}, and V_{Bias}) for the VCDL. The VCDL consists of four identical delay cells. In order to overcome the additional phase error introduced by the slope mismatch, the dummy clock buffers and a dummy voltage-controlled delay cell are utilized to achieve output load matching of each delay cell. The proposed DLL is designed for high-precision measurement applications, such as TDCs and ADCs, where a clean and stable external reference clock is crucial. To achieve this, CLK_{REF} is obtained from an external clock passing through a clock buffer, and its slope is adjusted to closely align with the slope of the four outputs of the VCDL. These measures contribute to achieving a more precise phase output for the proposed DLL. The external input clock frequency of the proposed DLL is fixed at 500 MHz.

III. Design of the Proposed DLL

A. Voltage-Controlled Delay Line

The proposed voltage-controlled delay cell and its bias circuit are shown in Fig. 2. In the voltage-controlled delay cell, the input clock signal is divided into two paths. One is the falling edge delay inverter consisting of M_1–M_4, the other is the rising edge delay inverter consisting of M_5–M_7. The paths formed by M_2–M_4 have lower conduction capability compared to the path formed by M_7; similarly, the paths formed by M_5 and M_6 have lower conduction capability compared to the path formed by M_1. This design ensures that the rising edge of A is sharper than that of B, while the falling edge of A is gentler than that of B. Therefore, the simultaneous conduction time of M_8 and M_9 can be reduced effectively, consequently decreasing the power consumption of the delay

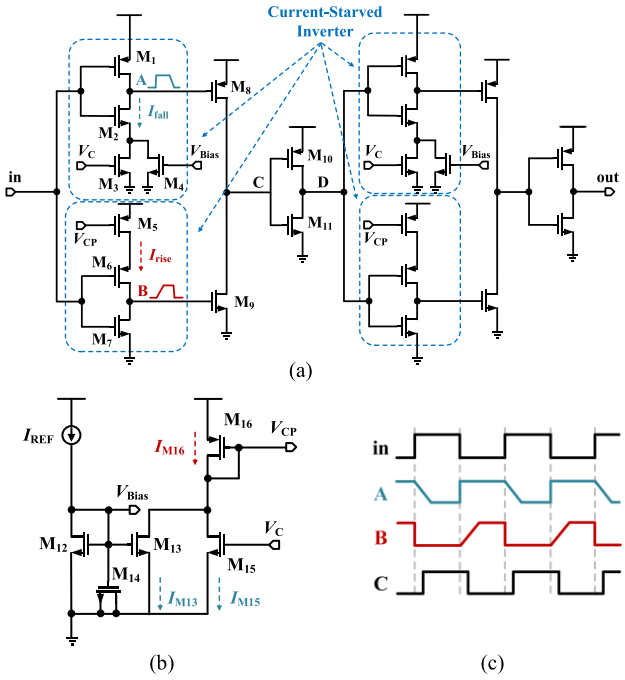

Fig. 2. (a) Circuit diagram of the proposed voltage-controlled delay cell, (b) its bias circuit, and (c) signal waveforms at important node in the proposed voltage-controlled delay cell.

cell. The delays caused by the two paths may not be the same. So the signal at node C is inverted and fed into the same circuit structure that matches M_1–M_{11} completely. This ensures that each voltage-controlled delay cell has the same delay for both the rising and falling edges of the input clock signal and thereby mitigating duty cycle distortion. The bias circuit in Fig. 2(b) is used to generate the voltage at the nodes V_{CP} and V_{Bias}. These output nodes are connected to the proposed voltage-controlled delay cell, facilitating the replication of the bias circuit's currents I_{M13} and I_{M16} to the proposed falling and rising edge delay inverters of the VCDL. Since the currents in M_3 and M_4 are equal to those in M_{15} and M_{13}, respectively, the discharge current of the proposed falling edge delay inverter is

$$I_{fall} = I_{M3} + I_{M4} = I_{M13} + I_{M15} \tag{1}$$

and the charging current of the proposed rising edge delay inverter is

$$I_{rise} = I_{M16} = I_{M13} + I_{M15}. \tag{2}$$

Therefore, V_C regulates current I_{M15}, consequently controlling the delay of the proposed voltage-controlled delay cell. The constant current I_{M13} can prevent the voltage-controlled delay cell from turning off when V_C is low.

As shown in Fig. 1, the proposed VCDL is composed of four cascaded voltage-controlled delay cells. During power-on or reset, the "Start" signal resets the control voltage V_C to a low level and the VCDL has the maximum delay. In order to avoid harmonic locking during locking process, the proposed VCDL need to satisfy

$$T_{REF} < T_{VCDL,max} < 1.5T_{REF} \tag{3}$$

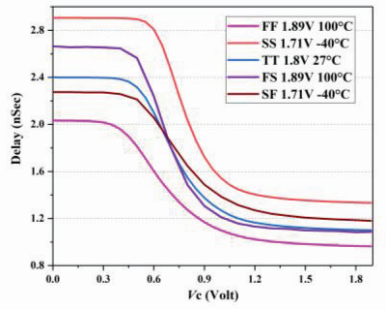

Fig. 3. Relationship between the control voltage V_C and the delay of proposed VCDL under different PVT conditions.

where T_{REF} represents the period of the reference clock and $T_{VCDL,max}$ represents the maximum delay time of the VCDL. The relationship between the control voltage V_C and the delay of proposed VCDL is simulated under various PVT conditions, as shown in Fig. 3. For the proposed DLL, T_{REF} is 2 ns and the delay of the proposed VCDL always less than 3 ns. Therefore, the proposed VCDL meets the requirement of (3).

B. PD and CP

The gain of PD can be expressed as

$$K_{PD} = \frac{\Delta t_{out}}{\Delta t_{in}} \tag{4}$$

where Δt_{in} and Δt_{out} represent the phase difference between the two input signals and the effective width difference between the two output pulses of the PD, respectively.

In conventional PDs [12], [13], Δt_{out} is equal to Δt_{in}, leading to the neglect of K_{PD}. Taking K_{PD} into consideration, the SPO φ_e caused by CP current mismatch Δi can be expressed as

$$\varphi_e = 2\pi \cdot \frac{\Delta t_{on}}{K_{PD} \cdot T_{REF}} \cdot \frac{\Delta i}{I_{CP}} \tag{5}$$

where T_{REF} is the reference clock period, Δt_{on} is the turn-on time and I_{CP} is the CP current [12].

It can be observed from (5) that increasing K_{PD} can also reduce the SPO in the DLLs. Therefore, a PD with a larger gain is proposed, as shown in Fig. 4. The proposed PD has two identical modified true-single-phase clock (TSPC) blocks, which consists of a falling edge delay inverter and a phase detection circuit, as shown in Fig. 4(b). The working mechanism of the modified TSPC block is described below.

1) Clk1 Lags Behind Clk2: As shown in Fig. 5(a), at the time t_{clk2}, the rising edge of CLK2 arrives and opens M_5, and M_6 is still open because node A is at logic high. So node B is discharged to logic low, and node Q rises to a high logic level. At the time t_{clk1}, CLK1's rising edge arrives and opens M_3, node A is discharged to a low logic level after a delay of $t_{delay,M3}$ and closes M_6. Since the falling edge of CLK1_D is delayed by a time of t_{delay} due to the falling edge delay inverter, the falling edge of Q will not arrive until time $t_{clk1} + t_{delay}$. Thus, it can be assumed that the pulse Q begins at t_{clk2} and ends at $t_{clk1} + t_{delay}$. Define $\Delta t = t_{clk1} - t_{clk2}$, then the estimated pulsewidth of Q can be expressed as

$$t_{pulse} = \Delta t + t_{delay}. \tag{6}$$

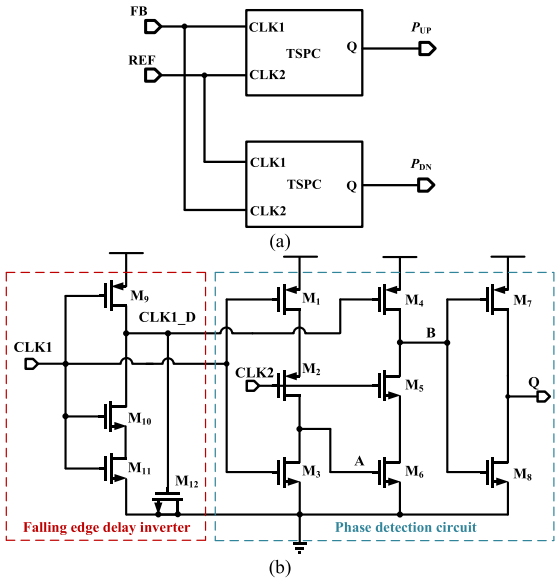

Fig. 4. Proposed PD circuit, (a) block diagram and (b) circuit diagram of the modified TSPC block.

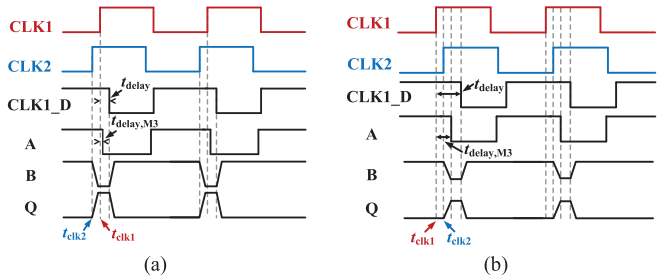

Fig. 5. Timing diagram of modified TSPC block, (a) CLK1 lags behind CLK2 and (b) CLK1 leads CLK2, when $t_{clk2} < t_{clk1} + t_{delay,M3}$.

Therefore, even when Δt is extremely small, due to the presence of t_{delay}, the generated pulse is wide enough to turn on the CP and eliminate the dead zone. Furthermore, this method only delays the charging of node B, so the dead-zone elimination technique does not sacrifice the phase detection range of the proposed TSPC PD.

After t_{clk2}, the discharge path of node B remains open for the duration of time $t_{delay,M3} + \Delta t$. Suppose nodes B and Q have the same amplitude and width of pulse. So the actual pulse amplitude of Q can be expressed as

$$V_{pulse} = \min\left(\frac{\overline{i_{B,DC}} \times \left(t_{delay,M3} + |\Delta t|\right)}{C_B}, V_{DD}\right) \tag{7}$$

where $\overline{i_{B,DC}}$ and C_B are the average discharge current and parasitic capacitance at node B respectively.

2) Clk1 Leads Clk2: The high logic of CLK1 first arrives at the time t_{clk1} and node A is discharged by M_3 to low logic after a period of time $t_{delay,M3}$. So M_6 is shut down at the time $t_{clk1} + t_{delay,M3}$ and the discharging path of node B is closed. The rising edge of CLK2 arrives at time t_{clk2} and opens M_5. Let $t_{delay} \gg t_{delay,M3}$ by proper sizing of transistors. Then there are two cases. First, if $t_{clk2} < t_{clk1} + t_{delay,M3}$, as shown in Fig. 5(b), node B has a discharging time of $t_{delay,M3} - |\Delta t|$,

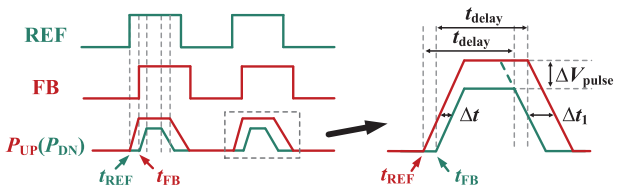

Fig. 6. Timing diagram of the proposed PD when REF leads FB by Δt.

the pulse amplitude of Q can be expressed as

$$V_{\text{pulse}} = \min\left(\frac{\overline{i_{\text{B,DC}}} \times \left(t_{\text{delay},M3} - |\Delta t|\right)}{C_{\text{B}}}, V_{\text{DD}}\right). \tag{8}$$

Notice that CLK1_D turns on M_4 at the time $t_{\text{clk1}} + t_{\text{delay}}$ and charges node B. It can be assumed that the pulse Q begins at t_{clk2} and ends at $t_{\text{clk1}} + t_{\text{delay}}$. So in this case, the estimated pulsewidth of Q can be expressed as

$$t_{\text{pulse}} = t_{\text{delay}} - \Delta t. \tag{9}$$

Conversely, if $t_{\text{clk2}} > t_{\text{clk1}} + t_{\text{delay},M3}$, M_6 is closed before M_5 is opened and node B cannot be discharged. The output Q cannot generate any pulses.

As shown in Fig. 4(a), the inputs of the two TSPC blocks are cross-connected to FB and REF respectively. Thus, if CLK1 leads CLK2 in one block, CLK1 will lag behind CLK2 in the other block. Taking REF leads FB by Δt ($\Delta t < t_{\text{delay},M3}$) as an example, the timing diagram of the proposed PD is shown in Fig. 6. Based on (7) and (8), it can be concluded that the two output pulses P_{UP} and P_{DN} of the proposed PD have a difference of ΔV_{pulse} in the pulse amplitude

$$\Delta V_{\text{pulse}} = \frac{2\overline{i_{\text{B,DC}}} \times |\Delta t|}{C_{\text{B}}}. \tag{10}$$

As shown in Fig. 6, the pulsewidth difference between P_{UP} and P_{DN} is

$$\Delta t_{\text{out}} = \Delta t + \Delta t_1. \tag{11}$$

The slope factor of the falling edges of the two output pulses is

$$k = \overline{i_{\text{B}}}/C_{\text{B}} \tag{12}$$

where $\overline{i_{\text{B}}}$ is the average charge current at node B in Fig. 4(b). Then Δt_1 can be estimated as follows:

$$\Delta t_1 = \Delta t + \Delta V_{\text{pulse}}/k = \left(1 + \overline{i_{\text{B,DC}}}/\overline{i_{\text{B}}}\right) \times \Delta t. \tag{13}$$

Combining (4), (11), and (13), the gain factor of proposed PD can be estimated as

$$K_{\text{PD}} = \left(2 + \overline{i_{\text{B,DC}}}/\overline{i_{\text{B}}}\right). \tag{14}$$

In the proposed design, the typical value for K_{PD} is approximately 14 when $\Delta t < t_{\text{delay},M3}$. Therefore, theoretically, the proposed PD can reduce the SPO of the DLL by a factor of 14. For large Δt values, only one pulse output exists with a width of $\Delta t + t_{\text{delay}}$ and an amplitude of V_{DD}.

Transient simulation results of the proposed PD are illustrated in Fig. 7. First, let FB lead REF by 200 ps, as shown in Fig. 7(a). P_{DN} is charged to logic high along with the arrival of the rising edge of FB signal. The falling edge of P_{DN} does

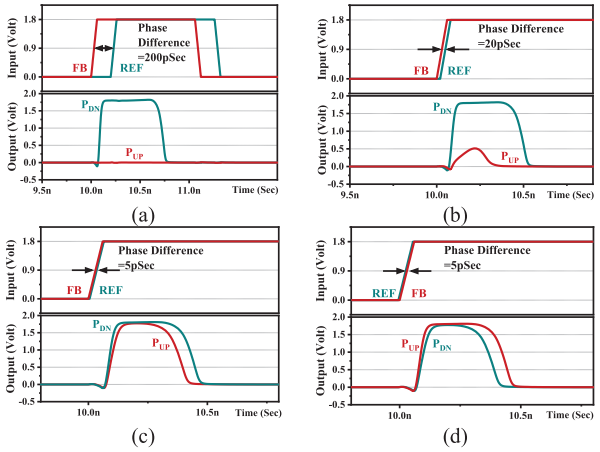

Fig. 7. Transient behaviors of the proposed PD when (a) FB leads REF by 200 ps, (b) FB leads REF by 20 ps, (c) FB leads REF by 5 ps, and (d) FB lags REF by 5 ps.

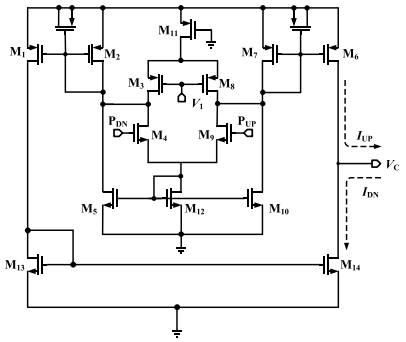

Fig. 8. Structure of the proposed CP.

not arrive immediately after the REF's rising edge, but arrives after a certain delay. And P_{UP} remains unchanged from the beginning to the end. When FB leads REF by 20 ps, the simulation result is shown in Fig. 6(b). The output pulses P_{UP} and P_{DN} still exhibit significant differences. Fig. 6(c) and (d) demonstrate that when the phase error is small, P_{UP} and P_{DN} differ in both height and width, validating the previous theoretical derivation.

Fig. 8 shows the CP similar to [14]. The input signals P_{UP} and P_{DN} come from the PD's output and control M_4 and M_9, respectively. When both P_{UP} and P_{DN} are at a low level, no current flows through M_{12}, therefore both M_5 and M_{10} are turned off. At this time, the CP's charging current I_{UP} and discharge current I_{DN} are both zero. When P_{DN} is high and P_{UP} is low, M_4 is turned on and M_9 is turned off. At this time, current flows through M_{12}, allowing M_5 and M_{10} to mirror the current from M_{12}. Since M_9 is off, the currents from M_7 and M_8 are directed into M_{10}. By selecting appropriate transistor sizes, it's able to ensure that the voltage at the drain of M_{10} is high enough to keep M_7 off and the current in M_{10} only comes from M_8. In this case, I_{UP} equal to zero. Since M_4 is turned on, the currents from M_2 and M_3 flow simultaneously through M_5 and M_{12}. As the current flowing through M_5 is less than that through M_{10}, the drain voltage of M_5 is lower. Consequently, M_2 is turned on and generates the discharge current I_{DN}. Conversely, when P_{DN} is at a low level and P_{UP} is

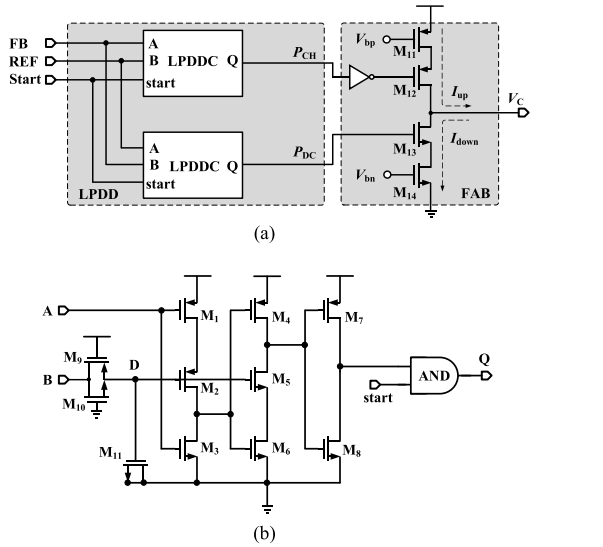

Fig. 9. Proposed auxiliary circuit, (a) block diagram and (b) schematic circuit of LPDDC.

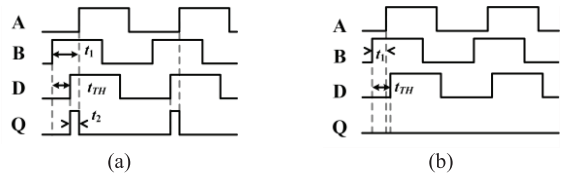

Fig. 10. Working mechanism of the proposed LPDDC, A and B have (a) large phase error and (b) small phase error.

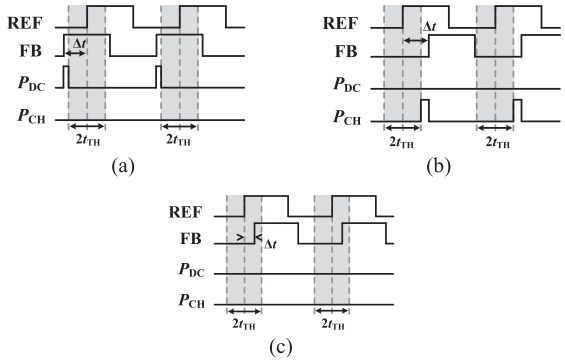

Fig. 11. Working mechanism of the proposed LPDD (a) FB leads REF by Δt ($\Delta t > t_{TH}$), (b) FB lags REF by Δt ($\Delta t > t_{TH}$), and (c) $|\Delta t| < t_{TH}$.

at a high level, the CP only generates the charging current I_{UP}. When both input signals are high, the CP can simultaneously generate currents I_{DN} and I_{UP}, and ideally, their magnitudes are equal. However, due to the short channel effect, there is an unavoidable mismatch between I_{UP} and I_{DN}. The proposed CP exhibits an approximate 6% mismatch in the charging and discharge current, but the proposed PD can greatly reduce the SPO caused by the current mismatch.

C. Proposed Auxiliary Circuit

The proposed LPDD and FAB constitute the proposed auxiliary circuit, as shown in Fig. 9. Fig. 9(b) shows the circuit diagram of the proposed LPDD cell (LPDDC), where M_1–M_8 form a conventional TSPC PD unit, and M_9–M_{11} constitute a

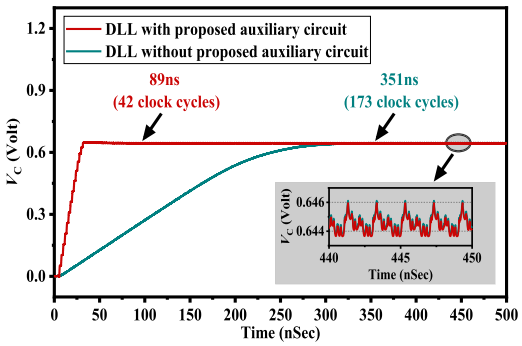

Fig. 12. V_C waveform during locking process of the DLLs with and without the proposed auxiliary circuit.

delay unit. After the DLL is reset, the "start" signal remains at a high level, and the output signal of the PD unit can be directly transmitted to node Q. The delay unit is designed to introduce a delay of t_{TH} to signal B and generate signal D. Consequently, a pulse signal Q is generated only if the time t_1 of signal B leading signal A exceeds t_{TH}, as shown in Fig. 10(a). If t_1 is less than t_{TH}, no pulse signals are generated. Thus, as shown in Fig. 11, the proposed LPDD only generates pulse signals P_{CH} or P_{DC} when the deviation Δt between REF and FB exceeds t_{TH}. The typical value of t_{TH} is 21 ps, and under extreme conditions, it is not less than 10 ps. Transistors M_{12}–M_{15} form the proposed FAB circuit. M_{12} and M_{15} are biased by V_{bp} and V_{bn}, respectively, and act as 150 μA current sources. The V_C node is connected to the LF capacitor and it can be adjusted rapidly when the FAB is activated by LPDD. As shown in Fig. 11(c), when $|\Delta t| < t_{TH}$, the proposed DLL is close to or in a locked state. No pulse signals output from P_{DC} and P_{CH}, and FAB is not activated. Therefore, the proposed auxiliary circuit does not affect the jitter of the DLL when it is near or in a locked state.

Fig. 12 compares the waveform of V_C during the locking process of the DLLs with and without proposed auxiliary circuit. At 5 ns, the "Start" signal in Fig. 1 makes a transition from a low level to a high level, indicating the beginning of the system's locking stage. During the initial stage of the DLL locking process, V_C deviates from the target value, leading to a large phase difference between REF and FB. Consequently, with the proposed auxiliary circuit, LPDD can activate the proposed FAB for rapid adjustment of V_C. Then V_C of the DLL with the proposed auxiliary circuit can be rapidly regulated to approach the target value and stabilize by 89 ns. The locking process of the proposed DLL only lasts for 42 clock cycles. On the contrary, the DLL without the proposed auxiliary circuit locks slowly and reaches the locked state by 351 ns (173 clock cycles). This means the auxiliary circuit improves the locking speed by 4.1 times. It can be observed that, when the system is in the locked state, the ripple amplitudes of the control voltage V_C are almost the same for the DLL with and without the proposed auxiliary circuit. This preliminarily verifies that the auxiliary circuit does not affect the DLL in the locked state.

Fig. 13 shows that there is no much difference in the energy spectrum of phase noise between the DLLs with

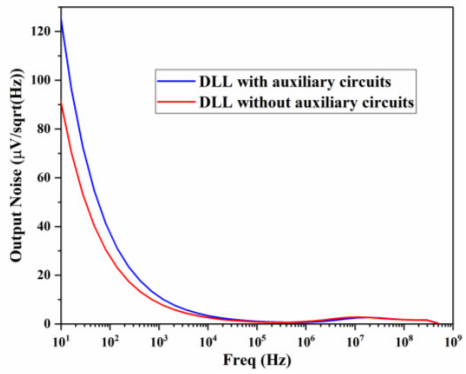

Fig. 13. Output phase noise with/without auxiliary circuit.

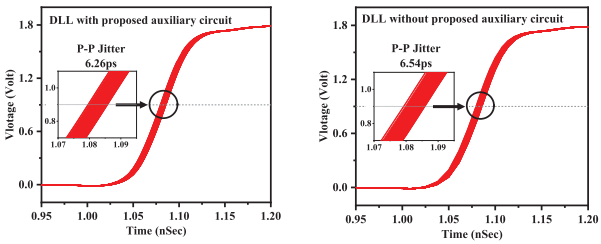

Fig. 14. P-P jitter obtained from 1000 cycles of the "CLK4" signal in locked state, (a) DLL with the proposed auxiliary circuit and (b) DLL without the proposed auxiliary circuit.

and without proposed auxiliary circuits. Due to the possibility of small leakage to the LF of the proposed auxiliary circuit, additional flicker noise may be introduced into the loop, resulting in a higher energy of low-frequency noise (10 Hz–10 kHz). However, the difference in noise energy spectral density between the two curves is relatively small at low frequencies. In the high-frequency band, the noise spectra of the two curves almost overlap. The contribution of the noise difference is almost negligible. Therefore, there is no much difference in the P-P jitter of DLL between the DLLs with and without the proposed auxiliary circuit.

The transient simulation taking the thermal noise and flicker noise of the devices into account is performed for the DLLs with and without auxiliary circuit. After the DLLs reached the locked state, 1000 clock cycles of CLK4 are captured and plotted together to obtain the P-P jitter, as shown in Fig. 14. It is evident that the difference in P-P jitter between the two DLLs is minimal. In addition, the root mean square (rms) jitter of the DLL is obtained using periodic steady state (PSS) and periodic noise (PNOISE) simulations. The rms jitter for the both DLLs is 1.01 ps. The simulation results above further demonstrate that the proposed auxiliary circuit does not affect the DLL under locked condition.

IV. Jitter Due to the Proposed Large Gain PD

A. Small-Signal and Noise Transportation Model of the Proposed DLL

The increased gain of the proposed PD can reduce the SPO. However, it may also influence the output noise of the proposed DLL. Therefore, it is necessary to analyze the

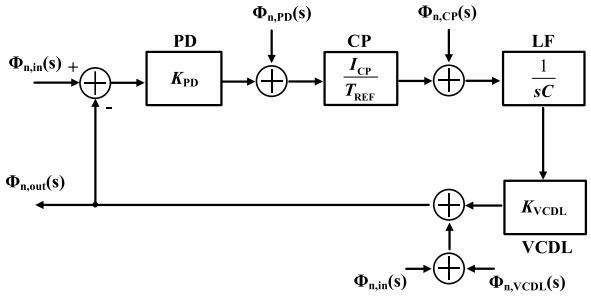

Fig. 15. Small-signal and noise transportation model of the proposed DLL.

relationship between K_{PD} and the DLL's output noise. The simulation results in Section III show that when the system is near or in the locked state, the impact of the proposed auxiliary circuit on DLL's output jitter is negligible. Therefore, the small-signal and noise transportation model of the proposed DLL can be depicted in Fig. 15. The subscript "n" represents noise in the components. I_{CP}, C, and K_{VCDL} specify the CP's current, LF capacitance, and the gain factors of the VCDL, respectively.

There are four primary noise sources influence the jitter of the DLL [15]: noise of the input reference clock [$(\Phi_{n,\mathrm{in}}(s)$], noise in the CP's output [$\Phi_{n,\mathrm{CP}}(s)$], and noise in the VCDL [$\Phi_{n,\mathrm{VCDL}}(s)$]. These noise sources can be assumed to be uncorrelated, and each can be analyzed separately to understand their individual contribution to the overall jitter of the DLL. First, consider the transmission characteristic of $\Phi_{n,\mathrm{in}}(s)$ to the output, while setting other noise sources to zero

$$\left(\Phi_{n,\mathrm{in}}(s)-\Phi_{n,\mathrm{out}}(s)\right)\frac{K_{\mathrm{PD}}I_{\mathrm{CP}}K_{\mathrm{VCDL}}}{T_{\mathrm{REF}}\times sC}+\Phi_{n,\mathrm{in}}(s)=\Phi_{n,\mathrm{out}}(s). \tag{15}$$

It can be determined from (15) that $\Phi_{n,\mathrm{in}}(s)=\Phi_{n,\mathrm{out}}(s)$, so the noise from the input reference clock is completely transmitted to the output clock and is independent of K_{PD}. In practical applications, it is advisable to use a low jitter clock signal as the input reference clock to minimize noise transmission to the output. Similarly, the transfer function from the PD's noise $\Phi_{n,\mathrm{PD}}(s)$ to the DLL's output can be derived

$$\frac{\Phi_{n,\mathrm{out}}(s)}{\Phi_{n,\mathrm{PD}}(s)}=\frac{1/K_{\mathrm{PD}}}{1+s/\omega_N} \tag{16}$$

where ω_N represents the −3 dB bandwidth of the loop, and

$$\omega_N=\frac{K_{\mathrm{PD}}\times I_{\mathrm{CP}}\times K_{\mathrm{VCDL}}}{T_{\mathrm{REF}}\times C}. \tag{17}$$

Similarly, the transfer function from $\Phi_{n,\mathrm{CP}}(s)$ to the output can be derived

$$\frac{\Phi_{n,\mathrm{out}}(s)}{\Phi_{n,\mathrm{CP}}(s)}=\frac{1/\left(K_{\mathrm{PD}}\times I_{\mathrm{CP}}/T_{\mathrm{REF}}\right)}{1+s/\omega_N} \tag{18}$$

and the transfer function from $\Phi_{n,\mathrm{VCDL}}(s)$ to the output can be derived

$$\frac{\Phi_{n,\mathrm{out}}(s)}{\Phi_{n,\mathrm{VCDL}}(s)}=\frac{1}{1+\omega_N/s}. \tag{19}$$

Therefore, according to (16) and (18), increasing K_{PD} under constant loop bandwidth ω_N and CP current I_{CP} can effectively reduce the contribution of PD and CP's noise to

the DLL's output. VCDL noise mainly results from supply fluctuation, inherent flicker, and thermal noise. Equation (19) shows that only higher frequency components of VCDL noise are transmitted to the DLL's output. If other parameters remain constant, a higher K_{PD} increases the loop bandwidth ω_N, as described in (17), enhancing the DLL's ability to suppress high frequency VCDL noise. For the proposed DLL, the loop bandwidth is about 45.14 MHz.

B. Jitter Due to Supply Fluctuation of the Proposed PD

Equation (16) demonstrates that increasing K_{PD} can suppress the contribution of PD's noise to the DLL's output. To further validate the reliability of the proposed PD, it is also necessary to analyze and simulate the effects of supply noise on its output noise. The output noise of PD manifests as fluctuation in the pulsewidth difference Δt_{out} between UP and DN. Fluctuation in Δt_{out} leads to the variations in the amount of charges injected by CP into the LF during each clock cycle, ultimately resulting in output clock jitter.

Assuming the reset pulse durations for UP and DN as $t_{\mathrm{rst,UP}}$ and $t_{\mathrm{rst,DN}}$, and the phase difference between the two input clocks of PD is Δt_{in}, the conventional PD produces a pulsewidth difference of

$$\Delta t_{\mathrm{out}} = \Delta t_{\mathrm{in}} + \left(t_{\mathrm{rst,UP}} - t_{\mathrm{rst,DN}}\right). \tag{20}$$

If the reset paths between UP and DN are mismatched, it leads to a difference between $t_{\mathrm{rst,UP}}$ and $t_{\mathrm{rst,DN}}$ (Δt_{rst}). Δt_{rst} is the sole factor related to the supply voltage, and the sensitivity of Δt_{out} to supply voltage can be defined as follows [16]:

$$S_{\mathrm{PD}} = \frac{d\left(\Delta t_{\mathrm{out}}\right)}{d\left(V_{\mathrm{DD}}\right)} = \frac{d\left(\Delta t_{\mathrm{rst}}\right)}{d\left(V_{\mathrm{DD}}\right)}. \tag{21}$$

For the proposed PD, the pulsewidth difference between UP and DN is given as

$$\Delta t_{\mathrm{out,proposed}} = K_{\mathrm{PD,proposed}} \Delta t_{\mathrm{in}} + \Delta t_{\mathrm{rst}}. \tag{22}$$

Both Δt_{rst} and K_{PD} are related to supply voltage. Therefore, the sensitivity of $\Delta t_{\mathrm{out,proposed}}$ to supply voltage can be defined as

$$S_{\mathrm{PD.proposed}} = \frac{d\left(K_{\mathrm{PD,proposed}}\right)}{d\left(V_{\mathrm{DD}}\right)} \times \Delta t_{\mathrm{in}} + \frac{d\left(\Delta t_{\mathrm{rst}}\right)}{d\left(V_{\mathrm{DD}}\right)}. \tag{23}$$

The sensitivity of $\Delta t_{\mathrm{out,proposed}}$ to supply voltage is also related to Δt_{in}.

The PAC simulations were performed for both the conventional PD and the proposed PD under varying Δt_{in} conditions. This aims to investigate the correlation between the amplitude of Δt_{out} and the 1 V supply fluctuation at different frequencies. The amplitude of Δt_{out} can be considered as the output noise of PD caused by supply fluctuation. As shown in Fig. 16(a), the simulation curves under different Δt_{in} conditions nearly overlap, aligning well with the analysis presented in (21). Higher frequency supply fluctuation increases PD output noise via the parasitic capacitances in MOS transistors. However, as indicated by (16), the low-pass characteristic between $\Phi_{n,\mathrm{PD}}(s)$ and $\Phi_{n,\mathrm{out}}(s)$ allows effective suppression of high frequency PD output noise by adjusting the loop bandwidth. The relationship between the output noise of the

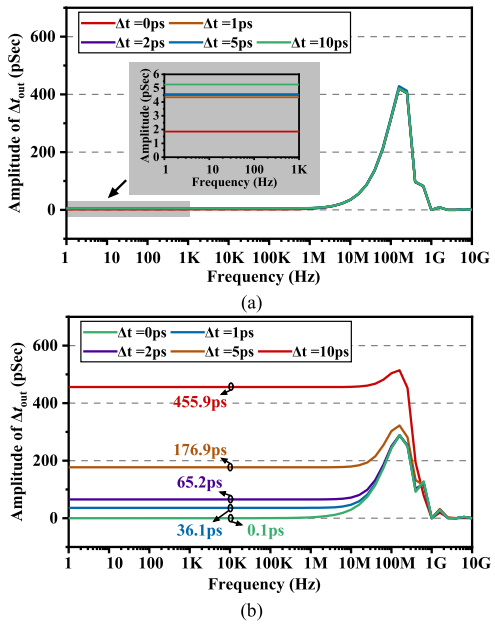

Fig. 16. Fluctuation amplitude of Δt_{out} caused by 1 V supply fluctuation at different frequencies (a) conventional PD and (b) proposed PD.

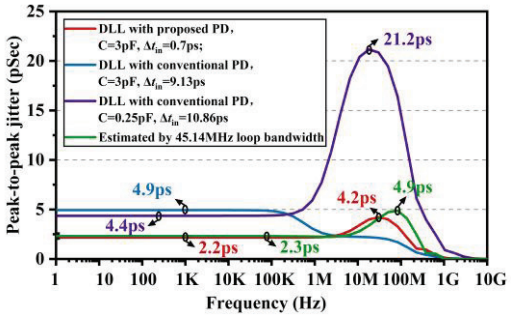

Fig. 17. P-P jitter of DLLs caused by 1 V supply fluctuation at different frequencies.

proposed PD and the supply noise has been simulated and depicted in Fig. 16(b). When Δt_{in} equal to 0, the output noise of the proposed PD is minimally affected by low frequency supply fluctuation. Since the gain factor K_{PD} of the proposed PD is sensitive to the supply voltage, as Δt_{in} increases, the impact of supply fluctuation on the PD's output noise also increases and is proportional to Δt_{in}, confirming the analysis in (23). However, the following two factors can both reduce the noise ultimately transmitted to the DLL output by the proposed PD. First, when the DLL is in a locked state, K_{PD} reduces Δt_{in} at the input of the proposed PD, thereby reducing the output noise of the proposed PD caused by supply fluctuation, as described by (23). Second, as described by (16), K_{PD} can also suppress the propagation of noise from the PD output to the DLL output. Therefore, the supply fluctuation of the proposed PD does not significantly interfere with the DLL output.

Under the locked condition, further simulations are performed to evaluate the impact of PDs' supply fluctuation on the DLL's output clock jitter, as shown in Fig. 17. The vertical axis shows the P-P jitter induced in the output clock by a normalized 1 V supply voltage fluctuation at different

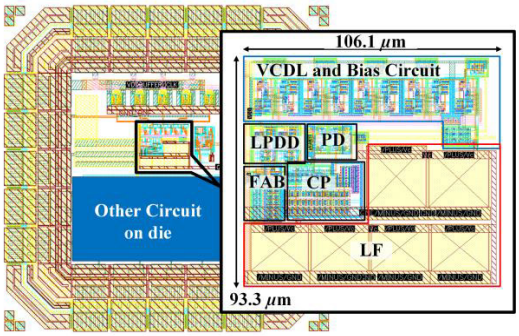

Fig. 18. Layout floorplan of the main core of the proposed DLL.

frequencies. Simulation results indicate that, under the locked condition, the phase error Δt_{in} between the two input clocks of the proposed PD is approximately 0.7 ps, and a 1 V low frequency supply fluctuation of proposed PD ultimately introduces a 2.2 ps P-P jitter at the DLL output. Owing to the low-pass characteristics described by (16), higher frequency noise at the proposed PD output is effectively suppressed. Consequently, the maximum output clock jitter induced by the supply noise of the proposed PD is 4.2 ps. To verify the accuracy of the loop bandwidth, we estimated the relationship between the output jitter of the proposed DLL and the PD supply noise based on (16). It can be seen from Fig. 17 that the estimated result is close to the simulation results, which validates the formula derivation and the accuracy of the loop bandwidth calculation.

Since the gain of the conventional PD is 1, replacing the proposed PD with the conventional PD results in a reduced loop bandwidth of the system, which more effectively suppresses high frequency noise at the PD output, as shown in Fig. 17. However, low frequency noise at the conventional PD output is transmitted to the DLL output with almost no attenuation. A 1 V low frequency supply fluctuation of conventional PD introduces a 4.9 ps P-P jitter at the DLL output. Reducing the LF capacitance C of the DLL with the conventional PD from 3 to 0.25 pF results in an increased loop bandwidth. As shown in Fig. 17, the DLL exhibits a significant reduction in its ability to suppress high-frequency noise from PD, confirming the analysis of (16).

As a result, considering the presence of noise in both the supply voltage and the input reference clock signal, it can be concluded that the proposed large gain PD itself does not introduce significant noise into the DLL output.

V. Post-Layout Simulation Results and Discussion

The proposed DLL is designed using a standard 0.18 μm CMOS process. The layout floorplan of the proposed DLL is depicted in Fig. 18, and the total area of the core circuit is 106.1 $\times$ 93.3 μm. The various metrics of the DLL are obtained through post-layout simulation. To compare the output phase accuracy of the DLL using the proposed PD and the conventional one, 200-time Monte Carlo simulations with process and mismatch variations are performed at a 1.8 V supply voltage and room temperature, as shown in Fig. 19. In the system's locked state, the phase error between CLK_{REF}

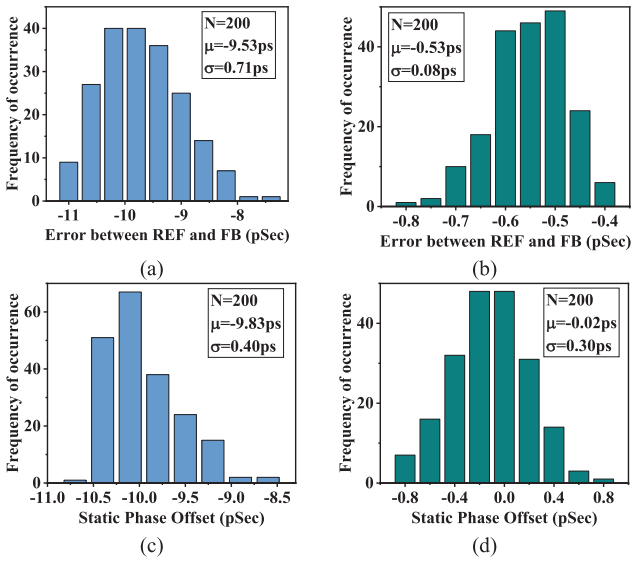

Fig. 19. Monte Carlo simulation results of DLLs' phase error and SPO (a) phase error of DLL using conventional PD, (b) phase error of DLL using proposed PD, (c) SPO of DLL using conventional PD, and (d) SPO of DLL using proposed PD.

and CLK4, denoted as SPO, is simulated. The phase error between REF and FB is also simulated, as they serve as direct input signals to the PD. From Fig. 19(a) and (b), it is evident that the proposed PD effectively reduces the mean phase error between REF and FB from 9.53 ps (1.71°) to 0.53 ps (0.095°) when the system is locked, representing an 18-fold improvement compared to the conventional DLL. The typical value of proposed K_{PD} is 14, as indicated by (5), it is theoretically capable of reducing the DLL's SPO by 14 times. Due to non-ideal factors in the CP switching process, there is a slight deviation between the theoretical analysis and the simulation results. Furthermore, the standard deviation of phase error using proposed PD is reduced to 0.08 ps, confirming its effectiveness in minimizing the phase error caused by the random current mismatch of CP. Therefore, the SPO of the proposed DLL can be effectively reduced to the mean value of 0.02 ps (0.0036°), as shown in Fig. 19(d). Due to slight slope differences between CLK4 and CLK_{REF}, there is a minor deviation between the SPO values and the phase error between REF and FB.

Further 200-time Monte Carlo simulations are conducted under different supply voltages and temperatures. The mean phase errors of the proposed DLL's outputs are summarized in Table I. The phase error of the Nth stage output can be calculated using the following method:

$$\text{PhaseError}_N = \left| t_{\text{delay},N} - N \times 500 \text{ ps} \right| \tag{24}$$

where 500 ps represents the ideal delay for each voltage-controlled delay cell, and $t_{\text{delay},N}$ is the phase deviation between CLKN and CLK_{REF}.

Due to the influence of parasitic capacitance, the delay of each stage of the VCDL is not exactly the same. Therefore, there still exists a phase error in the DLL outputs. Additionally, PVT variations can influence the phase error of the output signal. As shown in Table I, the proposed DLL exhibits

TABLE I

MONTE CARLO SIMULATION RESULTS FOR PHASE ERROR OF THE PROPOSED DLL FOUR-PHASE OUTPUTS

Supply (V)	Temperature (°C)	Phase Error relative to CLK_REF (pSec)				Phase Error Between REF and FB (pSec)
		CLK1	CLK2	CLK3	CLK4	
1.71	-40	2.42	0.56	3.67	0.17	0.75
	27	3.24	0.65	2.50	0.43	0.51
	100	3.60	1.21	1.70	0.68	0.39
1.8	-40	3.11	0.82	4.47	0.65	0.75
	27	4.00	0.60	3.18	0.02	0.53
	100	4.35	1.26	2.30	0.25	0.42
1.89	-40	3.92	0.99	5.00	0.87	0.65
	27	4.74	0.54	3.75	0.42	0.55
	100	5.07	1.33	2.83	0.18	0.45

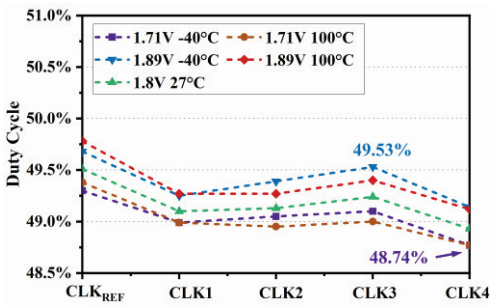

Fig. 20. Monte Carlo simulation results of the duty cycle of each clock signal.

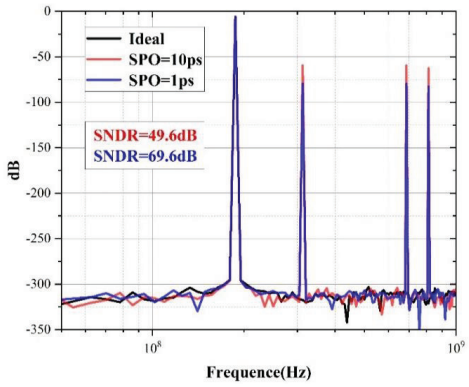

Fig. 21. ADC spectral density with using an ideal four-phase sampling clock, a four-phase-clock with SPO of 1 ps, and a four-phase-clock with SPO of 10 ps as the sampling clocks.

the maximum output phase error of 5.07 ps (0.91°) and maximum SPO of 0.87 ps (0.16°). Fig. 20 presents the Monte Carlo simulation results of the duty cycle of CLK_{REF} and CLK1–CLK4 under various supply voltages and temperature conditions. The duty cycle range for CLK1–CLK4 is between 48.74% and 49.45%.

Compared with traditional PD, using the proposed PD can decrease the SPO of DLL from nearly 10 ps to within 1 ps. The SPO of a DLL with multi-phase output will be evenly distributed to each output clock, introducing phase errors to each output clock. In order to analyze the expected benefits of SPO improvement for ADC applications, we used an ideal four-phase clock, a four-phase-clock with SPO of 1 ps, and a four-phase-clock with SPO of 10 ps as the sampling clocks for a four-channel TI-ADC. We sampled a sine wave signal with a frequency of 187.5 MHz, and the four-phase clock had a frequency of 500 MHz. We used 256 points for FFT analysis and simulated the spectral density of the ADC as shown in Fig. 21. It can be seen that compared with the four-phase-clock with SPO of 10 ps, using the four-phase-clock with SPO of 1 ps as the sampling clock for ADC results in lower harmonic noise, and signal-to-noise and distortion ratio (SNDR) can achieve a 20 dB improvement.

TABLE II

LOCKING DURATION (CLOCK CYCLES) UNDER DIFFERENT PVT CONDITIONS

Supply (V)	Temperature (°C)	Process Corner		
		TT	FF	SS
1.71	-40	13	20	25
	27	62	33	28
	100	57	38	61
1.8	-40	28	15	33
	27	42	36	47
	100	43	27	41
1.89	-40	33	23	23
	27	37	35	37
	100	23	37	51

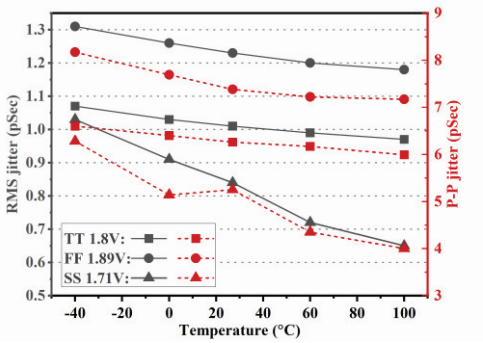

Fig. 22. P-P jitter and rms jitter under different PVT conditions.

The locking speed under different PVT conditions is summarized in Table II. The PVT variations impact the previously mentioned t_{TH} of the proposed LPDD and the delay characteristic of the proposed VCDL, consequently affect the locking speed of the proposed DLL.

Fig. 22 shows the P-P jitter and rms jitter under various process corners and temperature conditions. Under typical condition (TT process corner, 27 °C and supply voltage of 1.8 V), the P-P jitter and rms jitter of the proposed DLL are 6.26 and 1.01 ps, respectively. The worst case P-P jitter and rms jitter of the DLL do not exceed 7.69 and 1.26 ps, respectively. In addition to the simulated results for TT, FF, and SS process corners presented in Fig. 22, it is worth noting that the maximum P-P jitter remains below 22.4 ps even when considering the FS and SF process corners.

Table III summarizes the key performance metrics of the proposed DLL compared to other circuits. The comparative DLLs in [10] and [11] are designed to improve the SPO of DLLs without considering the locking time. In contrast, the

TABLE III
PERFORMANCE METRICS COMPARISON OF DIFFERENT WORKS

Parameter	This work [s]	ISCAS' 19 [10] [s]	TCAS-II' 21 [11] [s]	TCAS-II' 22 [14] [f]	Integration' 19 [17] [s]	TCAS-I' 18 [18] [f]
Process (nm)	180	130	130	180	180	130
Supply (V)	1.8	-	1.2	1.8	3.3	1.2
Frequency (MHz)	500	500	250	250	82.67~ 168	1500~ 3300
Area (mm^2)	0.0099	-	-	0.0092	0.017	0.0077
SPO (ps)	0.87[a]	1.16[b]	0.9[b]	-	4.72[c]	-
Locking Time (cycles)	42	-	-	-	54	16-32
RMS jitter (ps)	1.01[d]	-	0.42	-	1.36 @100MHz	1.629 @3.3GHz
P-P jitter (ps)	6.26	-	-	28.34 (13.76[s])	9.51 @100MHz	12 @3.3GHz
Power (mW)	1.89	-	2.89	2.28	3.54 @100MHz	7
FoM	-259	-	-	-248	-248	-250
Implement-ation	Analog	Analog	Analog	Analog	Analog	Digital

[s] Simulation results. [f] Measurement results. [a] Mean value based on 200 Monte Carlo runs, considering temperature and power supply variations. [b] Mean value based on 150 Monte Carlo runs, without considering temperature and power supply variations. [c] Transient simulation results. [d] Mean value based on pss + pnoise simulations and the integration range of jitter measurement is from 0.001 Hz to 250 MHz.

proposed DLL not only achieves lower SPO but also exhibits fast locking characteristic. Its locking speed is also comparable to that of other design with fast-locking characteristics [17]. The DLL presented in this article is an analog DLL. While existing digital DLL [18] can achieve faster locking speed compared to the proposed DLL, analog DLLs generally exhibit lower output clock jitter than their digital counterparts. In this table, the power and jitter performance of the proposed design are compared with existing designs using the following equation:

$$\text{FOM} = 10\log\left(\frac{\text{Power(mW)}}{\text{Frequency(MHz)} \times \text{Voltage}^2\,(\text{V}^2)}\right) + 10\log\left(\frac{\text{Area}\,(\text{mm}^2)}{\text{Process}^2\,(\mu\text{m}^2)} \times \left(\frac{\text{jitter}_{p-p}}{1s}\right)\right). \quad (25)$$

The proposed DLL achieves low SPO and fast locking while maintaining excellent power consumption, jitter, and area performance.

VI. CONCLUSION

This article proposes a DLL with a low SPO and maintains a fast locking speed. A large gain and dead-zone free PD is proposed to reduce the SPO of the DLL. As the system approaches lock-in, the proposed PD provides a typical gain of 14, thereby reducing the DLL's SPO to less than 0.87 ps. Furthermore, this work analyzes and simulates the potential impact of the proposed large gain PD on the jitter of the proposed DLL. The results indicate that the proposed large gain PD does not introduce significant noise into the DLL output. An auxiliary circuit is also proposed, reducing the locking time of the proposed DLL from 173 clock cycles to 42 clock cycles and improving the locking speed by 4.1 times. The proposed DLL operates with a 500 MHz input reference clock frequency and consumes a power of 1.89 mW. Additionally, it also exhibits rms jitter and P-P jitter values of 1.01 and 6.26 ps, respectively. Therefore, it can be a better choice for the applications such as TDCs and clock generators.

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