An 88.96 dB HDR CMOS Image Sensor Modeled on Visual Neuronal Response

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***Abstract*—This brief proposes a low-voltage low-power high dynamic range (HDR) CMOS image sensor (CIS) with visual neuronal responses (VNR) tailored for IoT applications, especially biomedical scenarios, which demand low power consumption and limited transmission bandwidth. The proposed CIS modeled on the nonlinear compression characteristics of illumination in the visual nervous system to enhance the dynamic range (DR). By employing a dynamic readout of pixel signals and comparing with a reference ramp voltage, the output of the proposed CIS conforms to the Naka-Rushton function, which describes the response features of visual neurons. The proposed CIS adopts a column-parallel architecture to enable simultaneous exposure, readout, and quantization of pixels in each row, combined with several low-power reset circuits to reduce image lag and inter-row crosstalk. A 126 × 64 HDR CIS with a 6.6 μm pixel pitch was fabricated using a 180 nm CMOS technology. Measurement results show a DR exceeding 88.96 dB, with a total power consumption of 18.62 μW at 60 fps and 0.8 V supply.**

***Index Terms*—CMOS image sensor (CIS), high dynamic range (HDR), Naka-Rushton function, visual neuronal response.**

I. Introduction

SINGLE-FRAME high dynamic range (HDR) techniques can be broadly divided into linear response synthesis and nonlinear response compression techniques. Linear synthesis HDR techniques mainly include dual conversion gain (DCG) [1], [2], triple conversion gain (TCG) [3], and lateral overflow integration capacitor (LOFIC) [4]. These methods typically require multiple readout to synthesize linear HDR images, which results in reduced frame rates and increased power consumption. Some studies adopt adaptive techniques to individually control each pixel's gain [5] or exposure time [6], enabling a single simultaneous readout of both signals and states. However, they still require external calculations to obtain HDR images. Due to the limitations of transmission bandwidth, storage formats, and the display devices, these high-bit-depth linear HDR data are typically tone-mapped or gamma-corrected within the image signal processor (ISP) to be compressed into low-bit-depth nonlinear HDR images. This synthesis-then-compress process results in the generation and transmission of numerous unused data, leading to increased power consumption and delay.

Nonlinear compression HDR technology compresses captured light intensity information within the sensor to mitigate pixel saturation under strong illumination, thus enhancing dynamic range (DR). This method requires no additional gain correction or image synthesis, making it more suitable for power-constrained IoT applications. Nonlinear techniques mainly include logarithmic pixel [7], nonlinear ADC [8], [9], [10], and piecewise linear (PWL) method [11]. Traditional logarithmic pixels, leveraging the subthreshold characteristics of MOSFETs, are suffered from significant fixed pattern noise (FPN), limited output swing, poor low-light signal-to-noise ratio (SNR), and image lag. Combining linear and logarithmic responses in pixels can mitigate some issues [12], [13], but the discontinuities and dips in the SNR curves are similar to those linear synthesis and PWL methods. Nonlinear ADCs generally exhibit higher power consumption due to their complex digital circuit architectures.

This brief presents a low-voltage low-power CIS with a nonlinear compression HDR technique. Unlike logarithmic or PWL methods, the response characteristics of the proposed CIS to illumination are modeled based on the Naka-Rushton function [14], which describes visual neuronal behavior. At the circuit level, each pixel is composed of only four MOSFETs and the CIS adopts a column-parallel architecture with a rolling shutter with exposure, readout, and quantization of each row occurring simultaneously. The output signal of each pixel is dynamically loaded onto the column bus and compared with a reference ramp voltage to conforms to the Naka-Rushton function. This brief is organized as follows: Section II describes the proposed CIS design. Section III discusses the analysis of visual neuronal response (VNR) for the proposed CIS. The measurement results and conclusion are given in Sections IV and V, respectively.

II. Design of the Proposed CIS

A. HDR Pixel Structure

The proposed pixel structure, shown in the left-side dashed box of Fig. 1, consists of a single photodiode (PD) and four MOSFETs, controlled by a pair of differential digital signals, sig and $\overline{\text{sig}}$. In conventional designs, pixels are limited by threshold voltages of MOSFETs, typically necessitating higher supply voltages to achieve the high signal swing required for maintaining noise performance. In the proposed design, the reset transistor M1, implemented as a PMOS device, hard-resets the PD node voltage (V_{pd}) to the supply voltage (V_{DD}), effectively eliminating residual charge-induced image lag and enhancing the pixel output signal swing. To further improve the output signal swing, a native NMOS M2 with near-zero threshold voltage (V_{th}) serves as the source follower amplifier, while M3 and M4 are configured as a transmission gate, enabling rail-to-rail transmission of pixel output signals. These signal swing enhancement methods enable a reduction in supply voltage to 0.8 V while maintaining adequate noise

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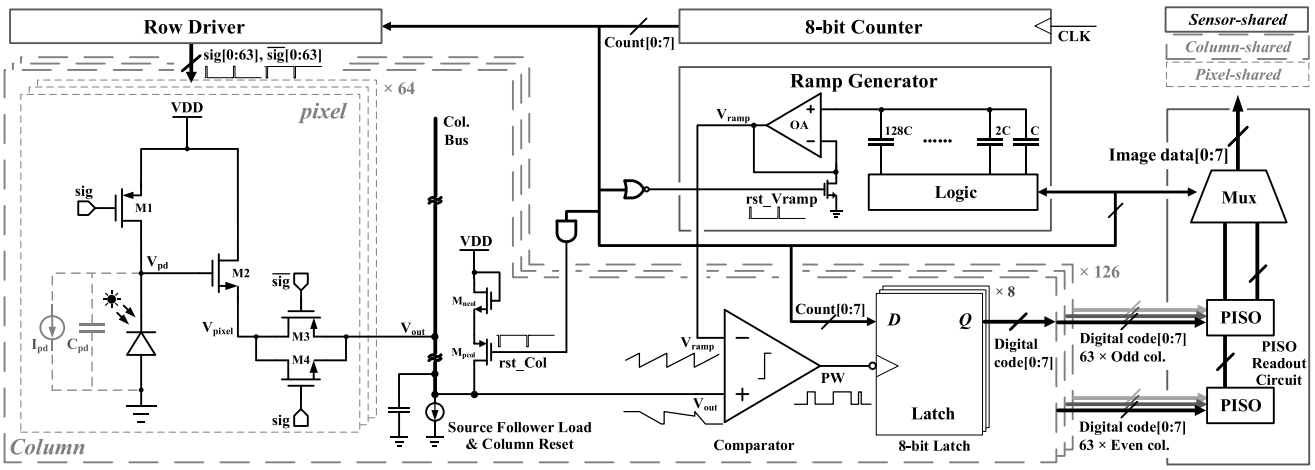

Fig. 1. Detailed circuit diagram of the proposed HDR CIS with VNR.

performance with peak SNR exceeding 55 dB and consequently reducing power consumption.

B. Overall Architecture and Circuit Implementation

The proposed HDR CIS with VNR, illustrated in Figs. 1 and 2, integrates a 126 × 64 pixel array, sensor-shared control circuits, column-shared parallel 8-bit quantization circuits, dual parallel-in-serial-out (PISO) readout circuits for both odd and even columns, and a multiplexer (MUX) for alternating output. By utilizing a rolling shutter architecture, all 126 pixels in a row simultaneously undergo exposure, readout, and digitization into 8-bit codes within a single row period (T). These 126 digital codes are then serialized and output sequentially through PISO and MUX in the subsequent period.

Fig. 3 illustrates the CIS' corresponding system operational timing. At the beginning of a row period (Count[0:7] = 0), the control signals sig[n] and $\overline{\text{sig}}$[n] of the n$^{\text{th}}$ row driver output a high-level pulse and a low-level pulse, respectively. During this time, M1 switches off, enabling PD to generate a photocurrent (I_{pd}) under illumination and discharges the PD parasitic capacitance (C_{pd}), resulting in a continuous decrease in V_{pd} over the row period. The source follower output voltage (V_{pixel}) is then passed through the conducting transmission gate and loaded onto the column bus as a dynamic voltage signal of pixel output (V_{out}). V_{out} is transmitted to the positive input of the column-shared comparator, and compared with the ramp voltage (V_{ramp}), which is generated by the ramp generator and rises in 256 steps from 0 to VDD. The comparator outputs a pulse-width modulated signal (PW), which contains the illumination information. The falling edge of PW is used to control the 8-bit latch to capture the quantized result of the pixel output. By this stage, the proposed CIS completes the conversion from photons to digital signal output. At the end of the row period (Count[0:7] = 255), the 126 8-bit latches transfer the captured digital codes in parallel to the two PISO shift registers. During the subsequent row period, these 126 digital codes will be shifted out and alternately serialized through the MUX, serving as the row-by-row readout of the digital image data.

C. Low-Power Implementation

Reset circuits are designed for both the column bus and the ramp generator. At the column bus, the dynamically varying

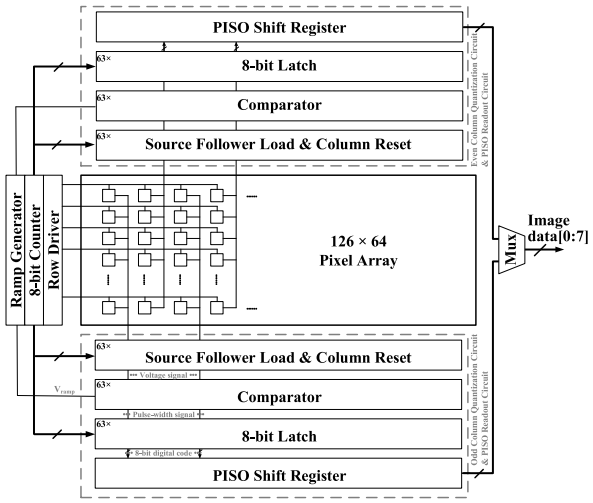

Fig. 2. Block diagram of the proposed CIS.

V_{out} undergoes a voltage jump to VDD − V_{th} during pixel switching. Without a reset circuit, the charging current for the voltage jump should be provided by a larger size of M2 to overcome the significant parasitic capacitance on the column bus, leading to a reduction in the pixel fill factor. To address this issue, a diode-connected NMOS M_{ncol} is used to provide a V_{th} drop, and a PMOS M_{pcol} is employed as a switch to reset the column bus. At the end of each row period (Count[0:7] = 255), V_{out} is rapidly pulled to VDD − V_{th}, thereby preventing the inter-row signal interference caused by residual charges from the previous row. Similarly at the ramp generator, V_{ramp} must transition from VDD to 0 rapidly at the beginning of each row period (Count[0:7] = 0) to prevent quantization errors, which may occur if V_{ramp} falls slower than V_{out}.

Notably, the high-current demand occurs exclusively during voltage jumps in both the column bus and ramp generator. The proposed reset circuit consequently reduces the quiescent current of M2 and relaxes the operational amplifier (OA) slew rate requirement in the ramp generator. Furthermore, the proposed CIS is solely driven by the 8-bit counter, utilizing simple shift registers as the row driver to generate pixel control signals, thereby eliminating the need for complex digital controllers. Combined with low-voltage pixels and subthreshold-designed analog circuits in the quantization circuits, the proposed HDR

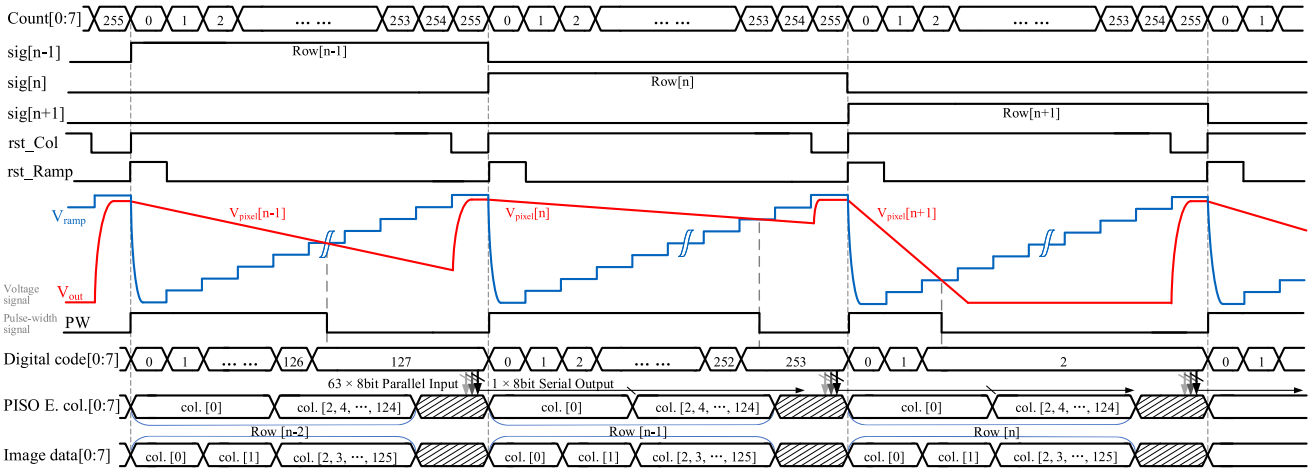

Fig. 3. Operational timing diagram of the proposed HDR CIS with VNR.

CIS with VNR achieves ultra-low-power consumption through these methods.

III. Analysis of VNR for the Proposed CIS

A. Features of VNR

In psychophysics, the Weber-Fechner Law [16], [17] describes the logarithmic relationship between stimulus intensity and perceived sensory response. To align imaging systems with human visual perception while efficiently storing and transmitting HDR images under limited bandwidth, engineers use log curves in ISPs to compress high-bit-depth data into standard 8 or 10 bits.

However, log curves derived from the Weber-Fechner Law are not the most accurate models for representing human visual perception [18]. In neuroscience and visual physiology, the Naka-Rushton function [14], exhibiting an S-shaped curve when plotted on logarithmic coordinates, is recognized as a more precise mathematical model for describing the features of VNR, which can be expressed as:

$$R_{Naka}(I) = R_{max} \cdot \frac{I^n}{I^n + R_{50}^n} \tag{1}$$

where $R_{Naka}(I)$ represents the magnitude of VNR under a stimulus intensity I, and the half-saturation parameter R_{50} indicates the stimulus intensity required to elicit 50% of the maximum saturated response R_{max}, while the Hill coefficient n determines the steepness of the response curve. Experimental studies on vertebrate rod cells [19] and the magnocellular lateral geniculate nucleus (LGN) of macaque monkeys [20] have demonstrated that the Hill coefficient n typically ranges between 0.7 and 1.2.

B. VNR of the Proposed CIS

Fig. 4 illustrates the voltage waveforms at the critical nodes within the pixel. V_{ramp} approximates the step ramp voltage signal generated by the ramp generator. During a single row period, the voltages at these nodes can be described as:

$$V_{ramp} = (VDD \cdot t)/T \tag{2}$$

$$V_{out} = V_{pd} - V_{th} = VDD - V_{th} - (I_{pd} \cdot t)/C_{pd}. \tag{3}$$

During the interval from 0 to T, V_{out} decreases from VDD − Vth, while V_{ramp} increases from 0 to VDD.

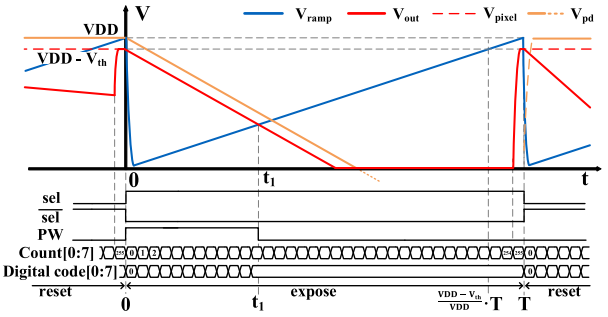

Fig. 4. Waveform and timing within a single row period.

Consequently, there is exactly one moment t_1 within the period when $V_{out} = V_{ramp}$, causing the comparator to toggle. By combining (2) and (3), the expression for the comparator's output pulse-width signal PW is derived as:

$$PW = t_1 - 0 = \frac{VDD - V_{th}}{VDD/T + I_{pd}/C_{pd}}. \tag{4}$$

When in the darkness, $I_{pd} = 0$, and $PW = \frac{VDD - V_{th}}{VDD} \cdot T$. When the illumination is strong, I_{pd} approaches infinity, causing PW to approach zero. To ensure that the output data from the CIS correlates with the intensity of the light, inverters are used in the MUX to invert the output digital codes. Therefore, the value of the digital image data is given by:

$$Dout = \left(2^8 - 1\right) - \left\lfloor 2^8 \times \frac{PW}{T} \right\rfloor = 255 - \left\lfloor 256 \times \frac{PW}{T} \right\rfloor \tag{5}$$

where the operator $\lfloor \cdot \rfloor$ denotes the floor function. The response characteristic of the proposed CIS can be nomalized as:

$$\begin{aligned} &R_{CIS}(I_{pd}) \\ &= 1 - \frac{PW}{T} = \frac{V_{th}}{VDD} + \frac{VDD - V_{th}}{VDD} - \frac{VDD - V_{th}}{VDD + T \cdot I_{pd}/C_{pd}} \\ &= \frac{V_{th}}{VDD} + (VDD - V_{th}) \cdot \frac{T \cdot I_{pd}/C_{pd}}{VDD^2 + VDD \cdot T \cdot I_{pd}/C_{pd}} \\ &= \frac{VDD - V_{th}}{VDD} \cdot \frac{I_{pd}}{I_{pd} + VDD \cdot C_{pd}/T} + \frac{V_{th}}{VDD}. \end{aligned} \tag{6}$$

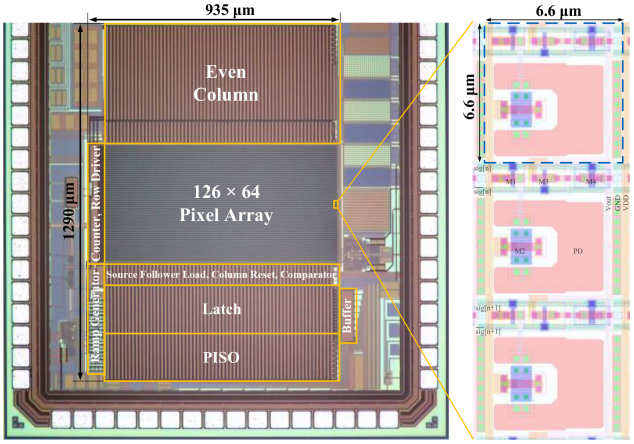

Fig. 5. Micrograph of the CIS and the layout of pixels.

Through the comparison of (1) and (6), it can be concluded that the output response of the proposed CIS is consistent with VNR, as it conforms to a linear transformation of the Naka-Rushton function with a Hill coefficient of $n = 1$.

In (6), $\mathrm{VDD} \cdot \mathrm{C_{pd}}/\mathrm{T}$ represents the value of $\mathrm{I_{pd}}$ when the effective response magnitude of the CIS reaches half-saturation. The scaling factor $\frac{\mathrm{VDD}-\mathrm{V_{th}}}{\mathrm{VDD}}$ represents the maximum output swing of the pixel normalized to the supply voltage, which corresponds to the maximum effective response magnitude of the CIS. It should be noted that the minimum output value cannot reach zero due to the presence of $\mathrm{V_{th}}$, with $\frac{\mathrm{V_{th}}}{\mathrm{VDD}}$ serving as the black level offset of the CIS in dark environments. However, this fixed offset does not affect the proposed CIS's ability to detect low light levels.

C. DR Analysis

The DR of a CIS can be defined as the ratio between the highest and lowest light intensities that can be distinguished within the same scene. In this brief, although (4) indicates that the pixel will not saturate under strong illumination, the luminance resolution of the digitized image is constrained by the bit depth of the quantization circuits, resulting in a finite DR. Assuming that $0 \sim \frac{\mathrm{VDD}-\mathrm{V_{th}}}{\mathrm{VDD}} \cdot \mathrm{T}$ contains N discrete digital codes ($\mathrm{N} = \lfloor 256 \times \frac{\mathrm{VDD}-\mathrm{V_{th}}}{\mathrm{VDD}} \rfloor$), The proposed CIS achieves distinguishable maximum and minimum values of $\mathrm{I_{pd}}$ at $\frac{\mathrm{T}}{256}$ and $\frac{(\mathrm{N}-1)\cdot\mathrm{T}}{256}$, respectively. By incorporating (4), the DR of the proposed HDR CIS with VNR can be calculated as

$$\mathrm{DR} = 20\log\left(\frac{\mathrm{I_{pd\ max}}}{\mathrm{I_{pd\ min}}}\right) = 20\log\left(\frac{\mathrm{I_{pd}}\big|_{\mathrm{PW}=\frac{\mathrm{T}}{256}}}{\mathrm{I_{pd}}\big|_{\mathrm{PW}=\frac{\mathrm{VDD}-\mathrm{V_{th}}}{\mathrm{VDD}}\cdot\mathrm{T}-\frac{\mathrm{T}}{256}}}\right)$$
$$= 20\log\left[\left(256 \times \frac{\mathrm{VDD}-\mathrm{V_{th}}}{\mathrm{VDD}} - 1\right)^2\right] = 20\log[(\mathrm{N}-1)^2] \tag{7}$$

IV. Measurement Results

In this brief, a low-voltage low-power HDR CIS modeled on VNR was fabricated using a standard 180 nm CMOS technology. Fig. 5 shows the CIS micrograph with a core size of 1290 μm × 935 μm and the layout of pixels. The effective pixel resolution is 126 × 64, with 6.6 μm pixel pitch and 37.6% fill factor.

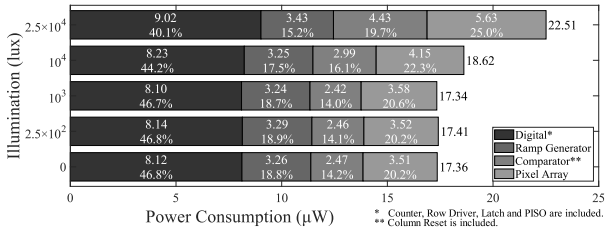

Fig. 6. Power break down of the CIS at 60 fps.

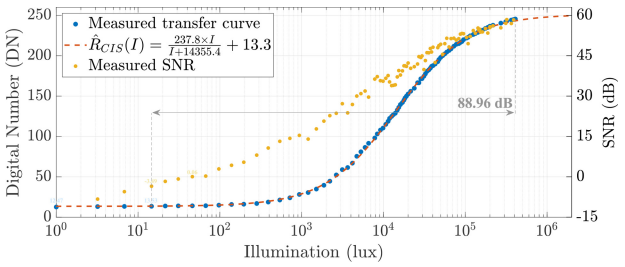

Fig. 7. Measured transfer curve, fitted curve, and SNR.

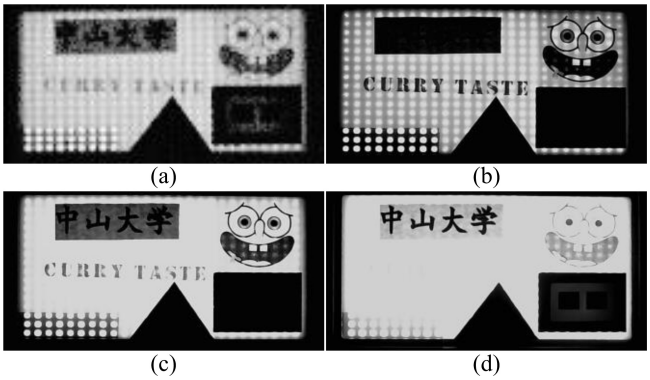

Fig. 8. Sample images captured by (a) the proposed HDR CIS with VNR, and by conventional camera with (b) short, (c) medium, (d) and long exposure time.

The proposed CIS operates at 0.8 V for both analog and digital circuits, consuming 18.62 μW at 60 fps under 10klux illumination. Fig. 6 shows the power breakdown under different illumination levels. Fig. 7 presents the measured transfer curve, the fitted curve, and the measured SNR. The fitted curve $\widehat{\mathrm{R}}_{\mathrm{CIS}}(\mathrm{I})$ conforms to the Naka-Rushton function and consists with (6). The measured transfer curve closely aligns with the Naka-Rushton function, and the measured SNR demonstrates smooth continuity without any dips. The proposed CIS achieves a DR exceeding 88.96 dB, defined as the ratio between the maximum resolvable luminance and the minimum luminance required to produce a one-code increment in the output digital value.

Fig. 8(a) presents the image captured using the proposed CIS, while Fig. 8(b), (c), and (d) depict the images captured by a conventional camera with different exposure time. In imaging tests, a logic analyzer captures the 8-bit digital signals output by the CIS, the first-row control signal sig[0] and the counter's MSB Count[7] serving as the frame and line synchronization signals, respectively. A MATLAB code is

TABLE I
COMPARISON TABLE WITH STATE-OF-THE-ART WORKS

	This Work	SSC-L '24 [10]	TCAS-II '21 [9]	JSSC '25 [5]	TED '23 [1]	TVLSI '23 [2]	TED '21 [4]	TCAS-I '20 [6]
Process	180nm CMOS	65/40 Stacked	110nm CIS	350nm CIS	180nm CIS	55nm CIS	180nm CIS	130nm CMOS
Pixel Pitch	6.6 μm	6.3 μm	3.2 μm	7.2 μm	10 μm	2.9 μm	16 μm	6.5 μm
Fill Factor	37.6%	86%	N/A	40.5%	> 70%	N/A	52.8%	54%
Pixel Array	126 × 64	640 × 480	640 × 480	512 × 320	512 × 512	1920 × 1080	128 × 128	256 × 256
Supply	0.8 V	1.8 V	3.3/1.5 V	3.3 V	3.3/1.8 V	3.3/1.2 V	3.3 V	1.5 V
Frame Rate	60 fps	30 fps	15 fps	60 fps	30 fps	30 fps	685 fps	100 fps
ADC	8-bit	10-bit	8-bit	10-bit	12-bit	12-bit	Off-chip	10-bit
DR (dB)	> 88.96	120	61.5	90.5	> 140	120	> 120	N/A
FPN (%)	0.99 (pix.) 0.46 (col.)	0.6	0.12	0.32 (pix.) 0.18 (col.)	N/A	0.01 (pix.) 0.04 (col.)	N/A	1.41
Power	18.62 μW	1330 μW	6 mW	97.6 mW	N/A	150 mW	N/A	7.31 mW
FoM*	38.5	144	1302.1	9900	N/A	2411.3	N/A	1115.4
HDR Tech.	Visual Neuronal Response (VNR)	Logarithmic counter & ramp	Bi-Gamma SS-ADC	Adaptive DCG	DCG & Logarithmic	DCG	Two-stage LOFIC	Pixel-wise exposure
Off-chip Processing**	No	No	No	Yes	Yes	Yes	Yes	Yes
Transfer Curve	Nonlinear	Nonlinear	Nonlinear	Linear	Nonlinear	Linear	Linear	Linear

* FoM (pJ/pixel/frame) = Power / (Pixel Array × Frame Rate)
** Off-chip processing (e.g., image synthesis, gain correction, or numerical calculations) requires additional power consumption.

used solely to convert the 8-bit binary data into decimal values and rearrange the serialized data into matrix format, without any additional numerical processing or data manipulation. The proposed CIS effectively captures and distinguishes the details across the entire scene, including the moderately bright Chinese characters in the upper-left, the low-brightness pattern within the black square in the lower-right, and the high-brightness light bulbs in the background, all within a single frame.

Table I compares the performance of the proposed CIS with state-of-the-art single-frame HDR techniques. By modeled on the VNR and implemented with low-voltage low-power circuits, the proposed CIS achieves an enhanced DR without requiring additional off-chip processing, while also demonstrating superior energy efficiency compared to the existing methods. However, the FPN of the proposed CIS remains relatively high due to the lack of compensation for pixel threshold variations.

V. CONCLUSION

This brief proposes a low-voltage low-power HDR CIS modeled on the nonlinear illumination compression of the visual nervous system. A novel quantization method utilizing dynamic readout of pixel signals for modeling VNR and a low-power circuit implementation are proposed. Fabricated in 180 nm CMOS technology, the proposed CIS operates at a supply voltage of 0.8 V and consumes only 18.62 μW while driving a 126 $\times$ 64 pixel array at 60 fps, achieving a DR of over 88.96 dB. The measured transfer curve closely aligns with the Naka-Rushton function, which characterizes the nonlinear response of visual neurons. By combining bio-inspired design with low-voltage low-power operation, the proposed HDR CIS with VNR is highly suitable for biomedical applications.

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