An Optical Transceiver Powered by On-Chip Solar Cells for IoT Smart Dusts With Optical Wireless Communications

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***Abstract*—Using optical communications for smart dust applications enables small size of transceivers and offers a potentially large power advantage over RF. This paper presents an optically powered transceiver, which consists of on-chip solar cells, an optical receiver, a storage capacitor, and a passive transmitter formed by a liquid crystal (*LC*) modulator and a modulated retro-reflector (MRR). The transceiver circuit system has been fabricated using a standard 0.18-μm CMOS process and the circuit area is 1×1.7 mm^2 excluding the MRR. Measurement results show that the complete transceiver can successfully work for 1-kb/s downlink and 10-b/s uplink under 0.5-V voltage supply and consume 53 nA totally. This indicates the transceiver can work at least in a 10-m range. It is successfully demonstrated that the transceiver scavenged the power from a 670-nm modulated laser beam sent by a base station (BS), extracted clock signal and the encoded data from the beam, decoded two designed instructions, switched the *LC* in the MRR and sent responses back to the BS. To the author's best knowledge, this is the first time to present that an on-chip solar-cell powered transceiver realizes the two-way optical wireless communications for Internet of Things applications.**

***Index Terms*—Energy harvesting, Internet of Things (IoT), optical transceivers, optical wireless communications, smart dusts.**

I. Introduction

THE INTERNET of Things (IoT) draws more and more attentions due to its broad applications, such as environment monitoring [1], agriculture monitoring [2], traffic control [3], healthcare [4], and logistics management [5]. The IoT will consist of billions of intelligent devices and networks, such as wireless sensor networks. The lifetime of the network is mainly determined by the sensor nodes and this leads the nodes to develop toward size reduction, low power and low voltage design, and the ability of energy harvesting. When a sensor node integrates self-contained sensing and communication system into a cubic-millimeter mote, it is called "smart dust" [6]–[8]. Most sensor networks use RF communications to transmit information [9]–[12]. In the smart dust applications, the antenna size is far smaller than the typical RF working wavelength and this causes the antenna efficiency very low. Optical wireless communications is a potentially attractive alternative to realize smart dusts due to the ability to create highly directed channels using small lenses or mirrors. There are quite few works to show hardware implementation of millimeter scale smart dusts in the literature. First smart dust was developed by Pister from UC Berkeley and it is made up of an optical receiver, a corner-cube retro-reflector transmitter, a solar cell, and a battery [8]. The power consumption of the smart dust is high up to 75 μW and the passive transmitter needs an 8-V voltage to actuate. Blaauw's team developed a 1-mm^3 smart dust with five layers of chip stacking structure including two ARM Cortex-M0 processors, temperature sensor, solar cells, and battery without communication platform [13]. It is a complicated system and consumes 40 μW in active mode. IoT requires large number of sensor nodes to ensure the network coverage, so low cost of the nodes is a key issue. A self-sustained cheap and relatively simple smart dust which can sense information and send it to a base station (BS) for further processing is needed. Oxford smart dust team developed an optical wireless communication network system including a BS and smart dust motes (SDMs) [14]–[22]. The SDM is an optical wireless communication platform for sensor nodes. It includes on-chip solar cells, an optical receiver, a storage capacitor, and a passive transmitter formed by a liquid crystal (*LC*) modulator and a modulated retro-reflector (MRR). This paper focuses on the SDM circuit design and is organized as follows. Section II shows an overview of the smart dust system and the detailed circuit designs are discussed in Section III. Measurement results of the SDM are presented in Section IV and Section V gives the conclusions of this paper.

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II. Overview of Oxford Smart Dust System

In the Oxford smart dust system, the BS can scan the space and position each SDM in its field of view and then communicate with them. The BS consists of a laser source, a beam steering system, and a camera [16]. The wavelength of the laser is 830 nm, as this wavelength is not visible and can

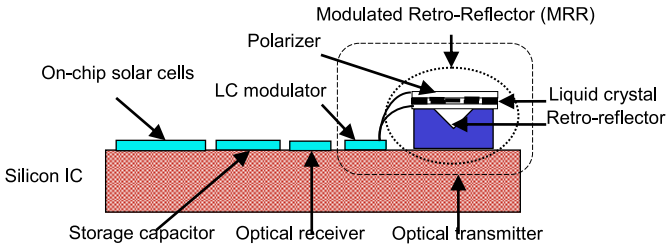

Fig. 1. Conceptual diagram of the proposed SDM.

be detected by silicon. The laser source illuminates an SDM through a beam steering system. The intensity of the laser source is modulated by a signal that is the information the BS sends to the SDM. To support a number of SDMs, the target downlink data rate is set as 10 kb/s. The maximum 830-nm laser source power is 0.5 mW due to the limitation of eye safety issue.

The structure of the SDM is shown in Fig. 1. It consists of on-chip solar cells, a storage capacitor, an optical receiver, an *LC* modulator, and an MRR. The solar cells scavenge energy from the laser illumination and environment to supply the power of the SDM. A storage capacitor is connected in parallel to the solar cells. The optical receiver can detect the optical signals modulated onto the downlink beam, recover the clock and data, decode instructions, and generate an output. Since sensors are not considered in this version of SDM, the receiver output directly drives the *LC* modulator of the transmitter. The MRR consists of a polarizer, an *LC* cell, and a retro-reflector. When the laser illuminates the SDMs, the MRR retro-reflects the beam modulated by the polarizer and *LC* cell back to the BS. Therefore, the MRR allows the transmission of information from SDM to the BS.

In the practical applications, sensors, such as temperature sensor, can be integrated on the SDM. The SDM can also work with an SDM reader through visible light communications. A good SDM reader can be smart phones, because their flashlight can be modulated to send optical signals and the digital camera can recognize optical signals by image processing techniques. These functions have been realized by some smart phone applications [23], [24].

III. SDM Circuit System Design

The block diagram of the smart dust circuit system is shown in Fig. 2. The on-chip solar cells are realized by a series connection of N-well/P-sub diode and T-well/N-well diode [14]. Under illuminations, a two-diode voltage is achieved on one chip. In order to compensate the different quantum efficiencies of the two diodes, the area of N-well/P-sub and T-well/N-well are 0.2 and 1.3 mm^2, respectively. The solar cells have been fabricated using a standard 0.18-μm CMOS process and the measurement results in Table I shows the available voltages and corresponding photocurrents under different illumination intensities. We assume in the worst condition there is no ambient light and the SDM is powered by the laser only. So these voltages and currents are the upper limits for the smart dust circuit system design. Due to the negative voltage rail below the substrate potential, all the MOS transistors in the SDM circuit system should be in an N-well, which is connected to the positive power rail. This requires that all the nMOS transistors are T-well nMOS transistors.

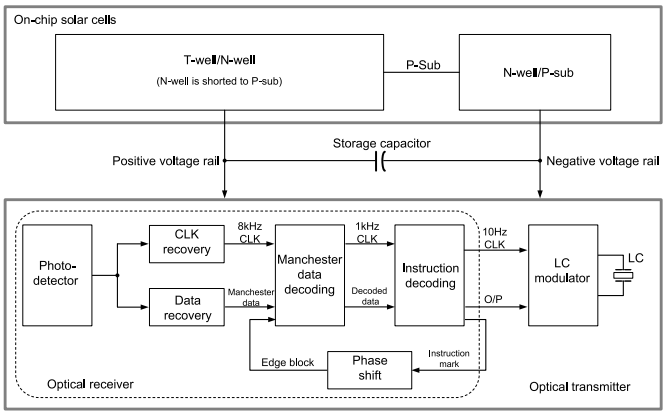

Fig. 2. Block diagram of the smart dust circuit system.

TABLE I
Illumination Intensities and the Corresponding Working Distance, Voltages, and Photocurrents Available in a 0.18-μm CMOS Process Solar Cells

Illumination ($\mu W/mm^2$)	79.45	14.77	3.87	0.99
Voltage (V)	0.8	0.7	0.6	0.5
Photocurrent (nA)	3800	688	180	46
Distance btw SDM and BS (m)	2	5	10	20

In order to eliminate the need for a power-demanding phase-lock-loop and an external frequency reference crystal for SDMs, clock and data are both modulated on the laser beam sent by the BS. The photodetector converts the received optical signal to an electrical analog signal. Based on this, clock is recovered and Manchester data is extracted. Then Manchester data is converted to a conventional binary data. This decoded data is fed into the instruction decoding block and instructions are identified. There are two instructions designed for demonstration purpose in this version. If there is an "up" instruction, the receiver output will become high. If there is a "down" instruction, the receiver output will become low. Sometimes the instructions cannot be detected successfully because Manchester data is decoded wrongly. This is caused by the decoding clock sampling at the wrong side of voltage transitions in the Manchester data bits. To fix this problem, a phase shift circuit is designed. The receiver output drives the *LC* modulator, which is used to switch the *LC* cell. A storage capacitor with ten times the *LC* capacitance is required to charge and discharge the *LC* so that the large instant current through the *LC* will not consume all the photocurrent.

A. Analog Front-End Block

The analog front-end block includes photodetector, clock recovery, and data recovery. In order to achieve a long working distance range for SDMs, the photodetector should have high dynamic range. A logarithmic photodetector is used, as shown in Fig. 3 [15]. All the transistors work in the subthreshold region. Its output depends on the modulation depth of the photocurrent and capacitance ratio. It is a three-pole one-zero

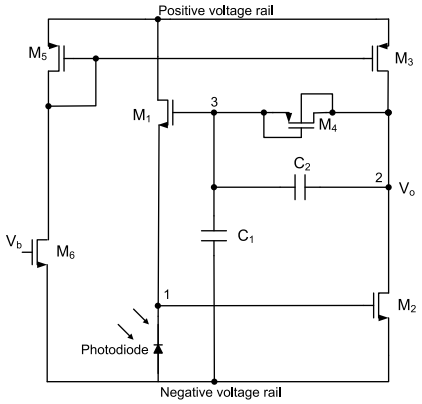

Fig. 3. Photodetector circuit used as the first stage of the analog front end.

circuit. The complete closed loop transfer function is

$$H(s) = \frac{(1 + s/\omega_4)/\kappa}{1 + s/\omega_3 + (1 + s/\omega_1)(1 + s/\omega_2)(1 + s/\omega_4)/(\kappa G_{\text{forward}})} \tag{1}$$

where κ is capacitive coupling ratio from gate to channel of transistors and G_{forward} is the gain of the amplifier formed by M_2 and M_3. ω_1 and ω_2 are two dominant poles at nodes 1 and 2, respectively. The pole 1 is a function of photocurrent and so it moves as the average photocurrent varies. ω_3 and ω_4 are a pole and a zero, respectively, at low frequencies. They are caused by M_4, C_1, and C_2. The Bode plot is shown in Fig. 4. The mid-band gain is

$$G_{\text{detector}} = \frac{v_o/V_T}{i_{\text{ph}}/I_{\text{ph}}} = \frac{1}{\kappa} \times \frac{C_1 + C_2}{C_2} \approx 14 \tag{2}$$

where V_T is thermal voltage, κ is 0.74 and the capacitance ratio (C_1 /C_2) is 10.

Manchester coding is selected for the data because conventional nonreturn-to-zero codes have a dc content, which is outside the bandwidth. The frequencies for the Manchester data and clock are chosen to be 1 kb/s and 8 kHz, respectively. If a low-pass filter is used to eliminate all the ac components, the dc average of the photodetector output is obtained, which is represented by the straight green line in Fig. 5. Then the clock can be recovered by using a comparator to compare the photodetector output with this average. If another low-pass filter is used to only remove the high frequency clock, the output is represented by the dashed red curve. Then comparing the red curve with its dc average will give the Manchester coded data. Fig. 6 shows the measurement result of the analog front-end block. The 1-kb/s Manchester data and 8-kHz clock are successfully recovered under 0.5-V supply.

B. Manchester Data Decoding Block

It is necessary to convert the Manchester data to a conventional nonreturn-to-zero signal, that is, a data "1" is represented by a high and a data "0" is represented by a low. A straightforward method is to sample the Manchester data with a *D* flip flop using the same frequency of clock, as shown in Fig. 7. When the laser turns on to illuminate the smart dust, the parasitic capacitance of the on-chip solar cells and the storage capacitor start to charge up and the voltage

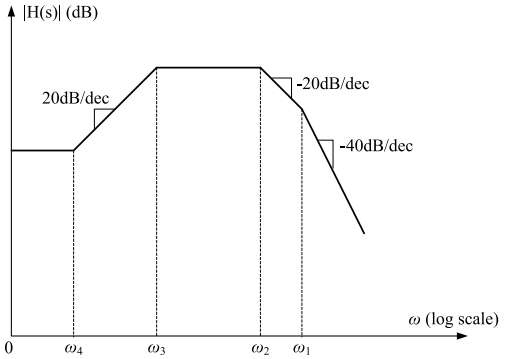

Fig. 4. Bode plot of the photodetector closed-loop transfer function.

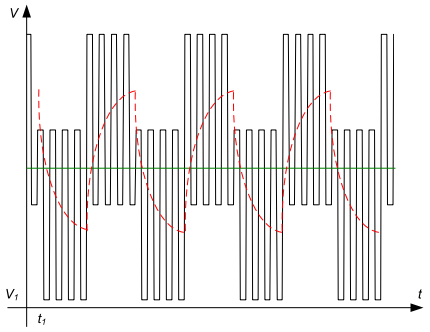

Fig. 5. Illustration of the recovery of the clock and data.

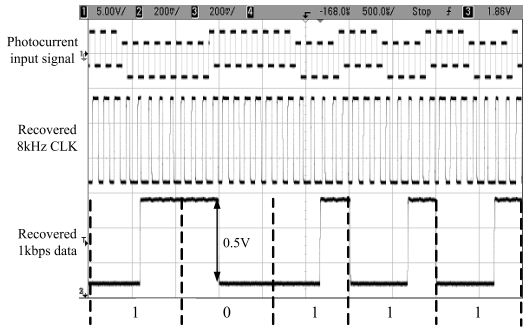

Fig. 6. Measurement result of analog front-end block. The test conditions are 0.5-V supply, 0.99-μW/mm^2 illumination intensity. The 8-kHz clock and 1-kb/s Manchester data are recovered.

across them rises. The time difference between the first successfully recovered clock and the first successfully recovered Manchester data varies for different illumination intensities. This means the phase difference between the clock and the Manchester data is a variable. If the clock has an 180° phase shift, the decoded data will be the complement of the desired data. This indicates that one of the two complementary outputs of the *D* flip flop is the true decoded data. But a selection must be made between them.

The decoded data includes the instructions sent from the BS. In the prototype of SDM, there are two instructions and each instruction is represented by 8-bit standard ASCII codes. For example, *d* and *u* representing down and up instructions, respectively, are implemented in the design. Two start bits "10" and two stop bits "11" are added and therefore one complete instruction has 12 bits. In the standby mode, Manchester data "1" is sent as a preamble and then the decoded data is

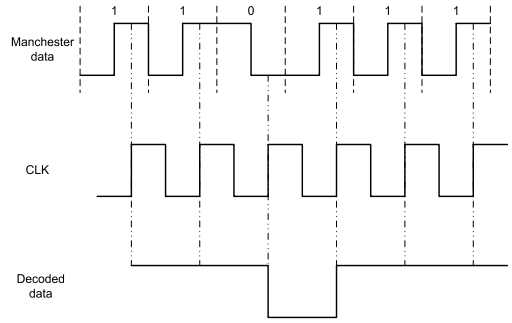

Fig. 7. Illustration of Manchester data decoding. A 180° phase shift of clock can cause the inversion of the decoded data.

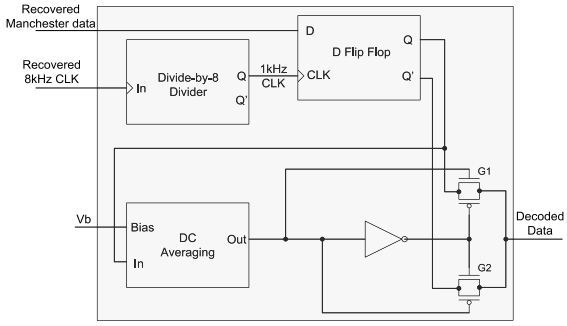

Fig. 8. Block diagram of Manchester data decoding.

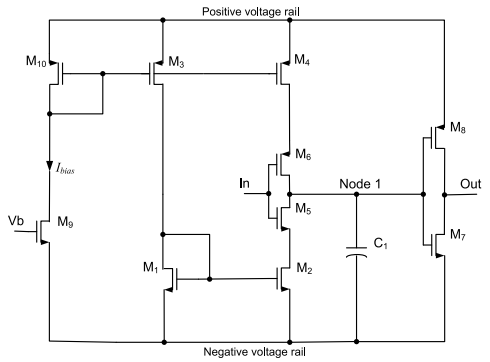

Fig. 9. Circuit diagram of dc averaging circuit.

expected to be "high" when there are no instructions. If the high in the standby mode is long enough comparing to the instructions, the dc average of one output of the D flip flop will be above a designed threshold voltage. Then this output is selected for the decoded data. The block diagram of Manchester data decoding is shown in Fig. 8. The Manchester data and CLK inputs are from the outputs of the analog front-end block. After the divide-by-8 divider, there is a 1-kHz clock and this clock samples the Manchester data. Suppose that Q of the D flip flop is the desired output and this means Q is high in the standby mode. Then the output of the dc averaging circuit is high. This will make $G1$ conducting and $G2$ open circuit and therefore the Q of the D flip flop will go to the decoded data output. If Q' is the desired output, the dc averaging circuit will output a "0" and this will make $G2$ conducting and $G1$ open circuit. So Q' will go to the decoded data output.

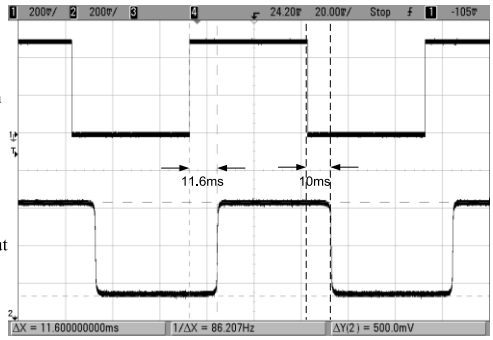

Fig. 10. Measurement results of dc averaging circuit with 0.5-V supply. The input is a square wave. The rising and falling edges of output have 11.6- and 10-ms delay, respectively.

Fig. 9 shows the schematic of the dc averaging circuit. The input "In" is connected to the D flip flop output. To save the limited power, low current consumption is the key point in the design. Moreover, small current leads to a small capacitor C_1. The bias current from M_9 is designed to be 20 pA and this current is halved and mirrored to M_3 and M_4. The current in M_4 is to limit the current flow from the high voltage rail to the inverter (M_6/M_5) and so as to control the charging time of C_1. The current in M_3 is mirrored to M_2 by M_1 to limit the current flow to the low voltage rail. Suppose that the input is high in the standby mode and then the node 1 is low. The decoded data could have nine bits of zeros in the worst case, which includes eight bits of instruction and one in the start bits. The nine bits of zeros mean a low for 9 ms at the input and the Node 1 is charged up during this time. The capacitor C_1 must ensure that the Node 1 voltage should not exceed the threshold voltage of the inverter formed by M_8 and M_7. Then the output will not be altered by the instructions and keep the value of the standby mode. The threshold voltage of the inverter (M_8/M_7) should be close to the middle of the two voltage rails so that the C_1 can have a similar voltage budget for the discharge if the input low in the standby mode. The C_1 should be at least 391 fF obtained from

$$C_1 = \frac{I_{\text{bias}}\Delta t}{2\Delta U} = \frac{20\ \text{pA} \times 9\ \text{ms}}{2 \times 0.23\ \text{V}} = 391\ \text{fF} \tag{3}$$

where ΔU is the threshold voltage of the M_8/M_7 inverter under 0.5-V supply. The actual value of C_1 used in the design is 406 fF, which is realized by a 20 μm $\times$ 20 μm MIMCAP.

The design criterion of the dc averaging circuit is that the output should be equal to the standby mode voltage when the instructions are sent. This means the instructions bits are removed from the data and therefore it can also be regarded as a delay circuit. For example, suppose the rising edge of the output is 9 ms later than the input rising edge, this indicates that a 9 ms of data "1" is removed when the input standby mode is low. A 9-ms falling edge delay indicates that a 9 ms of data "0" is removed when the input standby mode is high. Fig. 10 shows the measurement result of the dc averaging circuit. The delay time at the rising and falling edges of the output are slightly different and longer than 9 ms. This is caused by fabrication accuracy errors and mismatch of transistors. The longer delay time ensures the dc averaging circuit works.

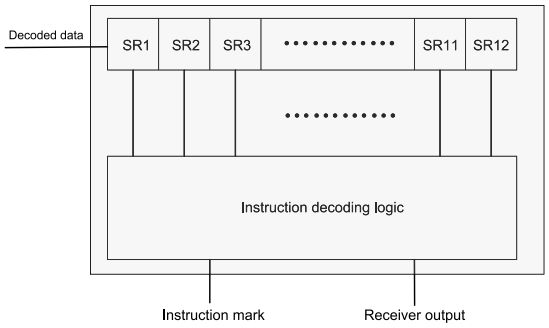

Fig. 11. Block diagram of instruction decoding.

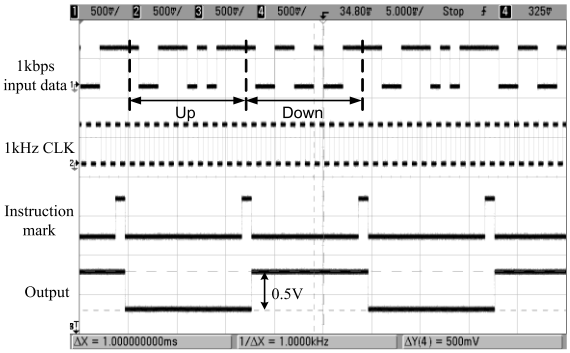

Fig. 12. Measurement result of the instruction decoding block with 0.5-V supply and 1-kb/s data rate.

C. Instruction Decoding Block

After the Manchester data decoding block, the decoded data includes two different instructions, up and down represented by ASCII codes *u* and *d*, respectively. These two instructions are simple examples and more instructions can be designed for more complicated systems. Including the start and stop bits, the complete instructions are shown

$$\text{“down”} = 10\ 01100100\ 11$$
$$\text{“up”} = 10\ 01110101\ 11. \tag{4}$$

Once an up instruction is detected, the output of the instruction decoding block will go high. The output will continue staying high till the first down instruction is detected. Then the output will go to high again when the next up instruction is found. In order to decode the instructions, a 12-bit shift register is required to temporarily save the data and logic circuits are needed to represent the instructions. The instruction decoding block diagram is shown in Fig. 11.

The “instruction mark” indicates whether there are instructions detected. Every instruction including up and down generates a pulse in the instruction mark and this will be an input of the phase shift block. In this prototype design, the output of the instruction decoding block is directly connected to the input of *LC* modulator block in the transmitter. Fig. 12 shows the measurement result of the instruction decoding block with a 0.5-V voltage supply. An input signal includes a series of up and down instructions and the output goes to high and low repeatedly. The instruction mark uses a high pulse to represent each successfully detected instruction. The pulse width is one time period of the clock.

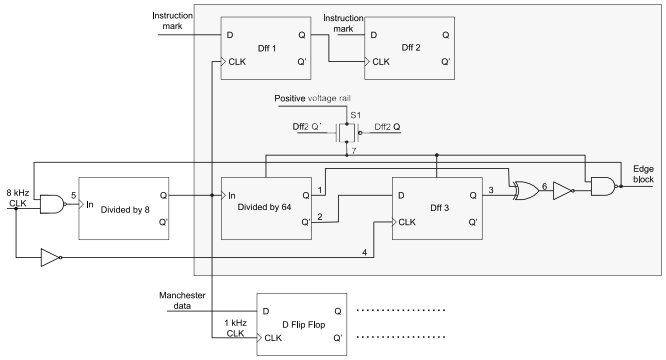

Fig. 13. Schematic of phase shift block.

D. Phase Shift Block

The phase difference between the clock and the Manchester data varies for different illumination intensities. When illumination intensity is low, the failure of Manchester decoding increases. This is because the voltage transitions of the recovered Manchester data bits are not in the middle as shown in Fig. 6 and the transition time is long. If the sampling edge of the clock is close to the transition edges, the clock will easily sample at the wrong side of the voltage transitions for some Manchester data bits. This causes some Manchester data is decoded wrongly and therefore no valid instructions will be detected. If no instructions are detected in a reasonably long time after startup, it is necessary to shift the clock phase. The phase shift block can effectively improve the accuracy of Manchester decoding for low illumination intensities and increase the SDM working distance.

Fig. 13 shows the diagram of the phase shift block in the highlighted rectangle. The basic idea of the phase shift block is to remove one sampling edge of the recovered 8-kHz clock and therefore shift the phase of the 1-kHz clock by 1/8 cycle. Once the first instruction is detected, the phase shift block will be shut down to save power. One NAND gate is placed before the divide-by-8 divider to allow the “edge block” signal to remove one edge of the 8-kHz clock. The decision to block an edge is based upon the detection of a valid instruction in a time that is longer than the time required to receive several instructions. Each instruction takes 12 clock cycles and for simplicity the detection time period is 64 clock cycles long. The phase problem will be apparent as soon as the system is powered up. In the startup period, the instruction mark is low and the power control circuit formed by Dff1 and Dff2 causes the switch *S*1 to conduct. The phase shift block starts to work. The divide-by-64 divider then counts 64 cycles of the 1-kHz clock and this means its output cannot change before the 32nd clock cycle, which is 32 ms and approximately 3-instructions long. If an instruction is not detected before this time, the output from the divide-by-64 divider will change. A problem is that every time the system is powered up the initial state of this output is unknown. However, the output from the edge block must be low to be effective. This can be solved by using an XOR gate. The timing diagram to generate the edge block signal is shown in Fig. 14(a). To ensure one sampling edge of the 8-kHz clock is blocked, one input to this XOR gate is via the Dff3 clocked at 8 kHz and this generates the

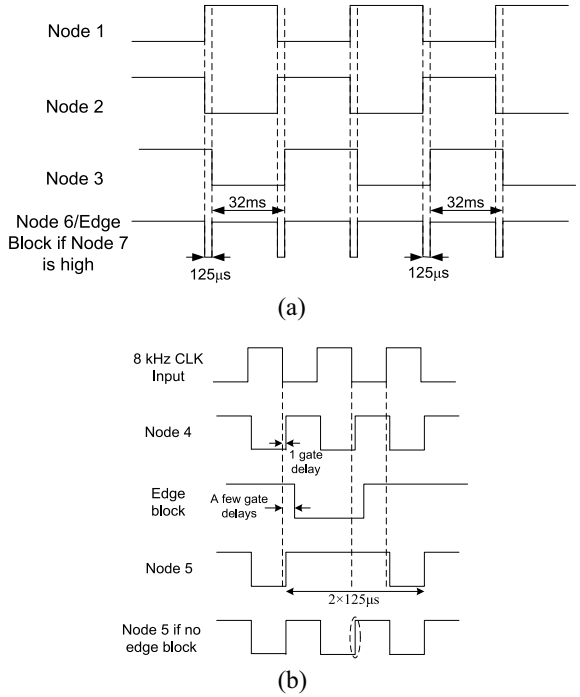

Fig. 14. Timing diagram of phase shift block. (a) Showing the generation of edge block signal. (b) Showing how the edge block signal to work.

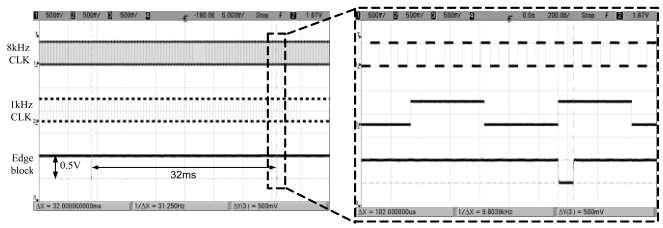

Fig. 15. Measurement result of the phase shift block with 0.5-V supply.

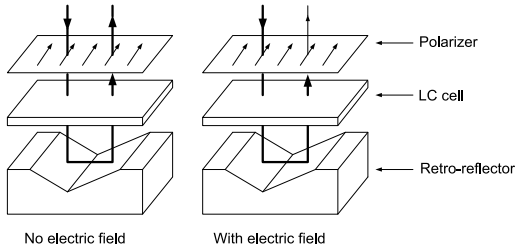

Fig. 16. MRR on the smart dust works with electric fields and without electric fields across the *LC* cell.

edge block signal with a pulse width of approximate 125 μs. Fig. 14(b) shows how the edge block signal to remove one sampling edge of the recovered 8-kHz clock. The delay is crucial in the phase shift block.

If an instruction is detected before 32 ms or after some phase shifts by phase shift block, there will be a high pulse in the instruction mark. The clock of the instruction decoding block is from the *Q*' of the divide-by-8 divider. Then the edges of the instruction mark will be close to the falling edges of the Dff1 clock. The *Q* of Dff1 will have an approximate half pulse width delay relative to its input. Then *Q* and *Q*' of Dff2 will become "1" and "0," respectively. Therefore, *S*1 is turned off and then the divide-by-64 divider and Dff3 are shut down. Node 7 becomes low and edge block will output a "1" to take out the effect of the feedback loop. The purpose of the half pulse width delay of Dff1 output *Q* comparing to the Instruction mark is to get rid of the wrong output of the Dff2 if there are glitches on the Instruction mark signal. In this prototype of SDM, we assume that there is no further phase shift required after the first instruction is successfully decoded. In this case, the SDM has to be restarted if the communication is lost. In the next version of SDM, we will consider the case that if instructions are missing for a certain long time, the phase shift block will be reactivated.

There is a feedback loop from the edge block signal and so it is crucial to ensure the feedback will not affect the system in the startup period. The CLK of Dff3 is from the recovered clock of the analog front-end block. Hence, Dff3 can work properly if the clock is successfully recovered and it is not affected by the feedback of the edge block. With the two complementary voltages as inputs, the XOR gate outputs a "1" and then inverted and fed into a NAND gate. As a result, edge block must be "1" when the SDM starts up and the feedback loop does not affect the system.

The phase shift block has three inputs and they are the instruction mark signal, an 8-kHz clock at node 4 and a 1-kHz clock. In the measurement, the instruction mark is low to represent a situation that no instructions have been decoded. Fig. 15 shows the measurement result of the phase shift block when the instruction mark is low. The output has a low pulse per 32 ms as expected from the design. The low pulse is magnified and shown in the figure. It will cover one rising edge of the divide-by-8 divider input due to gate delays, and the 1-kHz output phase will be shifted.

E. LC Modulator Block

The MRR is composed of a polarizer, an *LC* cell and a retro-reflector as shown in Fig. 16. The laser goes through the polarizer and a polarized light enters the *LC* cell. The light goes through the *LC* cell first, then is reflected back by the retro-reflector, and finally comes out of the *LC* cell. If there is no electric field across the *LC*, the light coming out of the *LC* cell passes through the polarizer and can be received by the BS. Data "1" is transmitted. If there is an electric field across the *LC*, the polarization of the light coming out of the *LC* cell is rotated and thus a big portion of light is blocked by the polarizer. Data "0" is transmitted. Ionic *LCs* (ILCs) are selected due to its high sensitivity to small voltages. However, ILCs should be driven by a signal whose dc component is small, because the dc offset will reduce its sensitivity. The *LC* modulator block has two outputs, which are connected to the *LC* cell. It needs to switch the *LC* into four stages sequentially, no electric field, positive field, no electric field, and negative field. Therefore, the dc offset is minimized. Fig. 17 shows the circuit of the *LC* modulator block. The flip flops need a clock signal, which can be obtained from the optical receiver. Fig. 18 shows the measurement results. The input signal frequency is 10 Hz and it is based on the response time of the *LC* cell made by our team. The difference of the

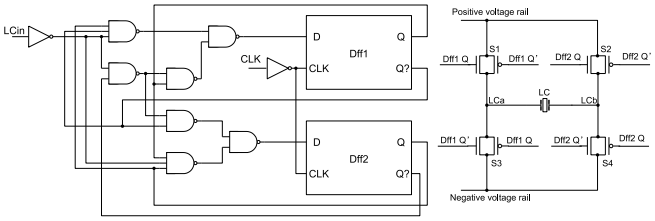

Fig. 17. Circuit diagram of the *LC* modulator block.

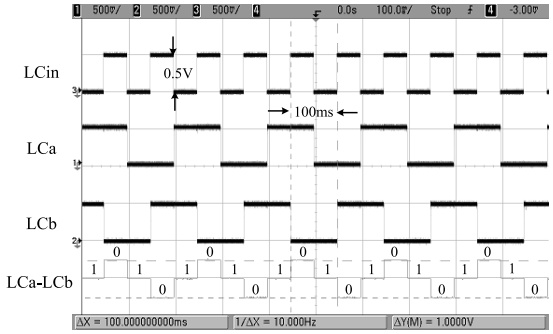

Fig. 18. Measurement result of the *LC* modulator block.

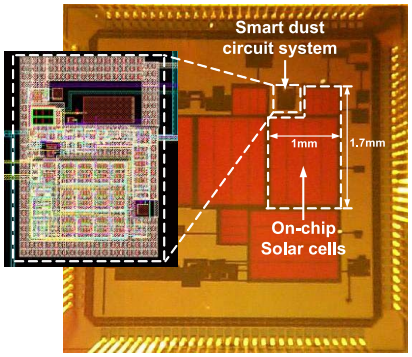

Fig. 19. Micrograph of the fabricated chip and smart dust circuit system layout.

two outputs is the voltage applied across the *LC* cell, which is a dc-balanced signal. The transmitted data by the MRR is marked on the "LCa-LCb" signal. When the voltage across the *LC* cell is 0 V, data "1" is transmitted. When the voltage is 0.5 V or −0.5 V, data "0" is transmitted. So in this case the BS will receive a repeated high-low signal.

IV. Measurement Results of Smart Dust System

Each individual functional block and SDM circuit system have been fabricated using a standard 0.18-μm CMOS process. Fig. 19 shows the micrograph of the chip and a complete SDM circuit system including solar cells occupies 1×1.7 mm^2. Since the circuit system part is covered by top metal to protect from illuminations, the layout of the circuit part is also shown. In this section, the measurement results of the electrically powered SDM will be described. Then the results of two-way optical wireless communication using optically powered SDM system will be presented.

A waveform representing the modulation of the laser is generated by a MATLAB program and then loaded into a waveform generator. The voltage signal from the generator is used to modulate a laser driver, which drives an 830-nm laser source. The laser is guided by lenses and focus on the chip. Neutral density filters are used to obtained different illumination intensities. The electrically powered SDM circuit system, including the optical receiver and *LC* modulator block, has been tested without the *LC* cell under the illumination and voltage conditions in Table I. The maximum Manchester data rate for each condition is summarized in Table II and it increases as the illumination and voltage supply increase. Although the illumination intensity varies almost in two decades and voltage supply varies from 0.8 to 0.5 V, the SDM circuit system works well under all these conditions.

TABLE II
Maximum Data Rates for Different Illumination Intensities

Illumination (μW/mm^2)	79.45	14.77	3.87	0.99
Voltage (V)	0.8	0.7	0.6	0.5
Max. data rate (kbps)	5.3	4.7	2.3	1.5

Table III shows the measured current consumptions of each functional block in the system for a 1-kb/s Manchester data rate under two illumination conditions. When the illumination intensity is 0.99 μW/mm^2, the clock recovery and data recovery in the analog front-end block consume approximately 9.5 nA, which is equivalent to the consumption of the photodetector. The digital block consumes a similar amount of power as the analog front-end block. When the receiver drives the *LC* modulator block, the total current is approximately 12 nA higher. This is because the *LC* modulator block needs a 1-kHz clock signal, which is generated from the receiver. This connection is made externally, so the clock signal switches the large capacitance of the connection. If the *LC* cell with 100-pF capacitance is switched at 10 Hz, it will consume 0.5 nA. As a result, the total current consumption of the fabricated SDM circuit system is approximately 53 nA. It is slightly smaller than the total available photocurrent 46 nA under this illumination. This means the smart dust cannot work in a 20-m distance, but at 10-m distance the illumination intensity increases approximately by four times and this will ensure the SDM can scavenge enough energy to work. When the illumination intensity is the maximum, the total current consumption of the SDM system is 188 nA and the total available photocurrent is 3800 nA, which is enough for the system to operate.

A typical result is shown in Fig. 20 and it is measured under 0.99-μW/mm^2 illumination intensity, 0.5-V voltage supply and 1-kb/s Manchester data rate. In this case, the up and down instructions shown in (4) are sent repeatedly. The smart dust circuit successfully recovered the clock and Manchester data, decoded the instructions and generated a dc-balanced signal for the *LC*.

A complete smart dust two-way optical wireless communication system is constructed and shown in Fig. 21. A visible 670-nm laser source is used for demonstration. The BS directs laser beams using a holographic beam-steering system. Multiple beams are generated due to higher diffraction orders and this significantly reduces the power density of the first

TABLE III
CURRENT CONSUMPTIONS OF EACH BLOCK AND COMPLETE SDM CIRCUIT SYSTEM FOR 1-kb/s DOWNLINK AND 10-b/s UPLINK

	2m distance (79.45 μW/mm^2)	20m distance (0.99 μW/mm^2)
Photodetector	46.9nA	9.3nA
Analog front-end block	135nA	18.8nA
Digital block	30.9nA	21.1nA
Optical receiver	174nA	40.6nA
LC modulator block	1.5nA	1.01nA
Optical receiver + LC modulator block	187nA	52.5nA
Switching 100pF at 10Hz	1nA	0.5nA
Total current consumption of SDM circuit system	188nA	53nA
Total available photocurrent	3800nA	46nA

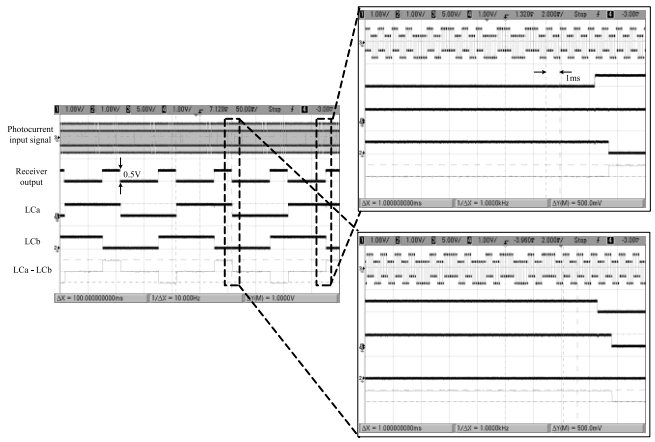

Fig. 20. Measurement results of the optical receiver with *LC* modulator under illumination 0.99-μW/mm^2, 0.5-V supply, and Manchester data rate is 1-kb/s.

order beam. The MRR is not miniaturized yet and placed beside the chip testing board. The SDM chip obtains the power from its on-chip solar cells. Although SDM contains bias generating circuits, but it did not operate as predicted due to process calibration issues, so bias voltages are externally generated. The chip has two *LC*-modulator output pins connected to the MRR. In order to monitor these two outputs, two unity-gain buffers using off-chip opamps are made on the testing board. The chip and MRR forms an optical transceiver and they are placed 1 m away from the BS. The first order of laser beam from the BS is used to illuminate the chip and a higher order of beam is used to illuminate the MRR. The laser is modulated by 8-kHz clock and 1-kb/s Manchester data including repeated up and down instructions.

The SDM chip powered by the illumination successfully decoded instructions. In Fig. 22(a), the top signal is the optical signal which modulated by 8-kHz CLK and 1-kb/s Manchester data. The bottom is the receiver output when an up instruction is received. It can be seen that the optically powered SDM can successfully work even under a 0.4 V. Fig. 22(b) shows the signal applied on the *LC* cell of MRR. The large noises caused by the off-chip buffers are removed by the subtraction of the

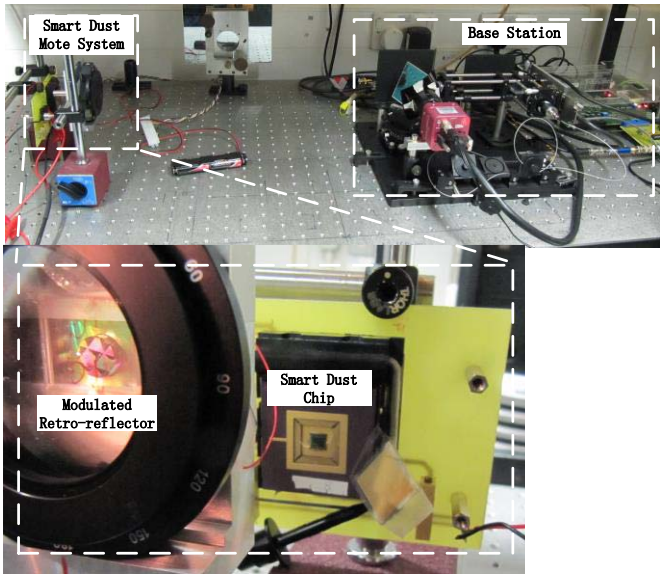

Fig. 21. Smart dust communication system. Smart dust testing chip is on the left and the BS is on the right, smart dust chip testing board, and off-chip MRR are also shown.

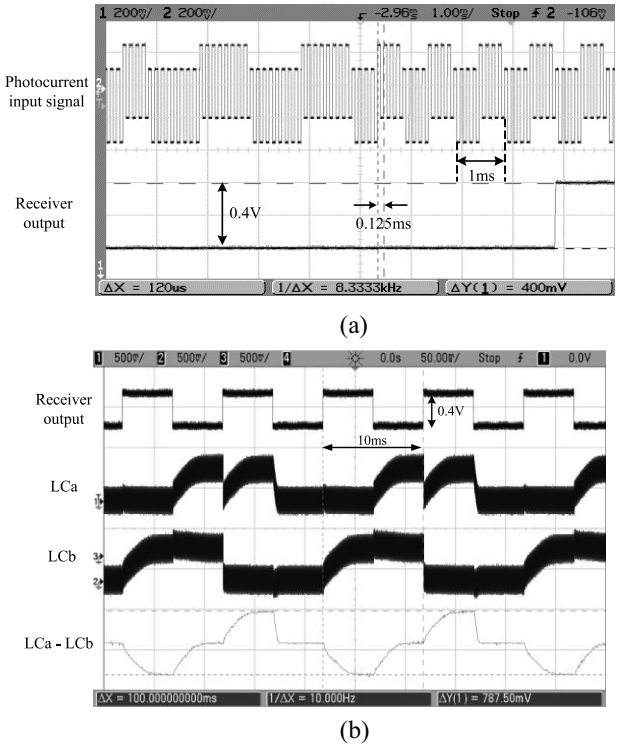

Fig. 22. Optically powered SDM measurement results. (a) Receiver output. (b) Voltage signal across the *LC* cell.

two *LC* modulator outputs, so have no effect on the *LC* cell. Compared to the measurement results of the electrically powered SDM in Fig. 20, the transition time of rising and falling edges is longer due to the limited power. The uplink received by the BS is a 10-b/s signal sent by the MRR, as shown in Fig. 23. Since the BS sends a series of repeated up and down instructions, the SDM receives them and outputs a repeated high-low signal. Then this signal turns on and off the *LC* cell through the modulator block and the MRR retro-reflects

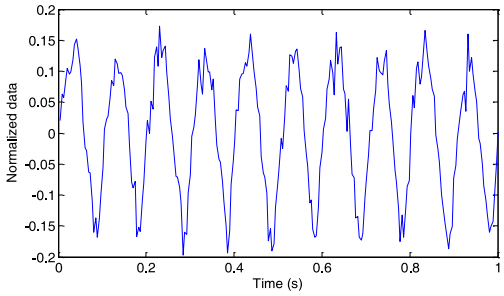

Fig. 23. Measurement results of the signals received by the BS, which are sent from the SDM. The *x*-axis is time in second and the *y*-axis is the normalized value.

back the laser. Therefore the BS receives a repeated high-low signal shown in Fig. 23. The high frequency glitches can be removed by a low-pass filter in the post signal processing. As a result, we successfully design and demonstrate the two-way optical wireless communications using on-chip solar cell powered transceiver for IoT smart dusts.

V. Conclusion

This paper reported the Oxford SDM prototype circuit system, which is an optical transceiver powered by on-chip solar cells for IoT smart dusts with two-way optical wireless communications. We assume there is no ambient light, the SDM is powered by the laser beam from the BS only. The solar cells generated a voltage from 0.5 to 0.8 V and very limited photocurrent under illuminations. Based on these conditions, SDM circuit system was designed. The analog front-end block recovered the 8-kHz clock and 1-kb/s Manchester data modulated on the beam. The Manchester data was then converted to a nonreturn-to-zero signal and instructions including up and down were decoded. The phase difference between the Manchester data and the 1-kHz clock varies with illumination intensities. This may cause Manchester data decoding to fail. This problem was solved by the phase shift block. The MRR has not been miniaturized onto the top of the SDM chip and the transceiver circuit including the solar cells is 1×1.7 mm^2. Electrically powered measurement results show that the transceiver can successfully work with 1-kb/s downlink and 10-b/s uplink under the voltage supply from 0.5 to 0.8 V. The total current consumption is 53 nA when the supply is 0.5 V. This current indicates the transceiver can work at least in a 10-m distance. The two-way optical wireless communication between the SDM and BS is also demonstrated. The transceiver was powered by the laser beam from the BS and received the optical signal, decoded the instructions and transmitted an optical signal. Then it was received by the BS successfully.

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