A Wide Linear Range Ultra-low Transconductance Amplifier for Biomedical Sensor Applications

Haoning Sun
School of Electronics and Communication Engineering
Sun Yat-Sen University
Shenzhen, China
sunhn3@mail2.sysu.edu.cn

Zhipeng Li
School of Electronics and Communication Engineering
Sun Yat-Sen University
Shenzhen, China
lizhip57@mail2.sysu.edu.cn

Ruihuang Wu
School of Electronics and Communication Engineering
Sun Yat-Sen University
Shenzhen, China
wurh29@mail2.sysu.edu.cn

Yan Feng
School of Electronics and Communication Engineering
Sun Yat-Sen University
Shenzhen, China
yanf9@mail2.sysu.edu.cn

Yuxuan Huang
School of Electronics and Communication Engineering
Sun Yat-Sen University
Shenzhen, China
huangyx295@mail2.sysu.edu.cn

Jingjing Liu*
School of Electronics and Communication Engineering
Sun Yat-Sen University
Shenzhen, China
liujj77@mail.sysu.edu.cn

Jin He*
Shenzhen SoC Key Laboratory
Peking University Shenzhen Institute and PKU-HKUST Shenzhen-Hong Kong Institution
Shenzhen, China
frankhe@pku.edu.cn

Yiqun Wei
Shenzhen SoC Key Laboratory
Peking University Shenzhen Institute
Shenzhen, China
Weiyq@ier.org.cn

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***Abstract*—In the field of biomedical sensors, active filters with very low cutoff frequencies are required because of the weak electrical signals from the human body. The Gm-C filters are more prominent among the filter designs, which consist of an operational transconductance amplifier (OTA) and a capacitor. The key design issues are transconductance and linearity. In this paper, a new ultra-low transconductance OTA structure is proposed. The basic idea is to extend the linear input range of the OTA using the source degeneration pseudo-resistor technique and the bulk-driven technique. The transconductance is reduced by using series-parallel current mirrors for the OTA. This ultra-low transconductance OTA has an extremely low bias current of 0.1nA and a shunt factor of 100, reducing the OTA transconductance to 0.4pS with 39.55μVrms noise. It also increases the linear input range from ±50mV to ±2.5V, extending it by a factor of 50.**

Keywords—operational transconductance amplifier, source degeneration, series–parallel current mirror, bulk-driven

I. INTRODUCTION

In recent years, the development of integrated transconductance amplifiers has attracted a large number of scholars for research, mainly because of their prominent applications in frontier industries such as biomedical circuits and neural networks. Among them, in the field of medical electronics, active filters with very low cutoff frequencies (a few Hz) are required due to the relatively low frequency of electrical signals in the human body [1].The Gm-C filter is prominent among the designs successfully applied to low frequency filters. It consists of OTAs and capacitors, where the key design issue is the degree of transconductance. Methods to improve the linearity of MOS transconductor are constantly being pursued. Currently the reduction of the OTA transconductance is a major drawback for many of the proposed linearization methods. However, for the implementation of a transconductance operational amplifier-capacitor (OTA-C) filter, such low frequencies imply large capacitance and very low transconductance [2]. That is, the design of Gm-C filters requires low transconductance OTA, which makes them particularly suitable for the application of linearization techniques.

A method to reduce the transconductance is current dividing technique. It only uses current mirrors with large divisions [3]. However, the current mirrors have a large area, making the low transconductance OTA occupy too much area. The use of series-parallel current mirrors in OTAs can greatly improve the area efficiency and achieve a very low transconductance 89pS and extend the linear input range to ±500mV [4]. T Kulej used a long-channel PMOS as the output transistor to reduce the overall circuit transconductance to 31.1nS [5]. Carlos F.T. Soares effectively reduced the circuit transconductance to 36nS using a shunt method [6]. Ali Namdari used subthreshold techniques in combination with substrate-driven transistor techniques to reduce power consumption and transconductance [7][8]. In this paper, the proposed CMOS OTA design is a source degeneration PMOS transistor pseudo-resistive, series-parallel shunt ultra-low transconductance OTA with extremely low bias current. The rest of this paper is organized as follows. Section II introduces the design of the proposed OTA. Section III discuss the simulations and analysis of the OTA. Section IV concludes this paper.

II. CIRCUIT DESIGN

In this section, we will describe the design of the source degeneration pseudo-resistor loaded OTA with series-parallel current mirrors, which realized an ultra-low transconductance. The circuit structure and working principles will be discussed.

A. Source Degeneration Pseudo-resistive

Compared to single-ended input methods, differential input methods make it easier to identify small signals and are less susceptible to environmental noise. So, it is possible to achieve

an ultra-low transconductance by using a very low tail current for the MOS transistors. In this case, a PMOS pair is biased in the subthreshold region. Although this results in a lower current and power consumption, the linear input range is limited to $100mV_{pp}$, which is a small linear input range [9]. So, a classical differential PMOS pair used as the input stage does not meet the needs of the ultra-low transconductance OTA. To improve the linearity of the differential PMOS pair, one of the simplest topologies is to add a source degeneration resistor to the circuit [10], as shown in Fig. 1(a).

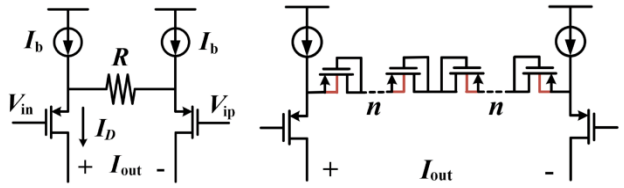


Fig. 1. (a) Source degeneration differential PMOS pair OTA input stage. (b) Differential PMOS pair OTA input stage with source degeneration transistor pseudo-resistor.

Neglecting body effects and channel length modulation effects, the voltage drop across resistor R increases as the input voltage increasing. This causes an increase in I_D. It means that a portion of the input voltage is distributed across the resistor R and not all the input is used as the overdrive voltage between the two gates and sources. Therefore, the change in I_D is smoother, thus extending the linear input range of the differential pair. Usually, it is difficult to make resistors with precisely controlled resistance or with reasonable physical dimensions due to CMOS process conditions. Therefore, it is better to use MOS transistors instead of resistors. By replacing the degeneration resistor with PMOS transistor pseudo-resistor [11], a differential PMOS pair OTA input stage with source degeneration transistors can be obtained, as shown in Fig. 1(b).

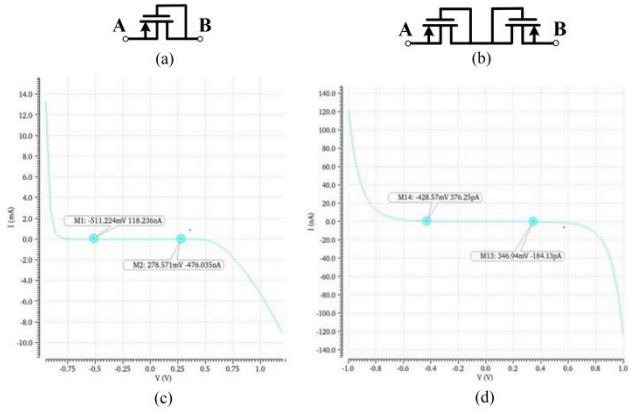


Fig. 2. (a) Delbrück resistor-like device. (b) Pseudo-resistor structure based on Delbrück resistor-like device. (c) Current-voltage relation of Delbrück resistor-like device. (d) Current-voltage relation of Pseudo-resistor structure.

This structure can achieve greater linearity and better linear input range. The pseudo-resistor structure is achieved by using the resistor-like device proposed by Delbrück [12], as shown in Fig. 2(a). In this structure, the gate of the PMOS transistor is connected to its drain and the substrate is connected to its source. The current flowing through the PMOS transistor increases exponentially with voltage, and the structure has an extremely high resistance region when the voltage across the PMOS transistor is small.

As shown in Fig. 2(a), if the voltage at point B is higher than point A, the structure will work as a PNP bipolar junction transistor. On the contrary, the structure will work as a PMOS transistor. It means that the pseudo-resistor is asymmetrical. Its current-voltage relation can be seen as Fig. 2(c). In order to eliminate this asymmetry, this paper uses the structure shown in Fig. 2(b) to implement the pseudo-resistor. In this case, the I-V relation of the pseudo-resistor is symmetrical. No matter which side has a higher voltage, the equivalent resistance is always caused by one PNP BJT and one PMOS transistors together.

Although the Delbrück device can some extent equivalently replace the resistor, its resistance is affected by the voltage range. If only the structure of Fig. 2(b) is used as a pseudo-resistor, the pseudo-resistance is limited due to the voltage range across them. Therefore, large resistance cannot be achieved merely by changing the width and length of MOS transistors. To increase the resistance of the pseudo-resistor, the structure in Fig. 1(b) allows multiple MOS transistors to be connected in series to form a pseudo-resistor. This structure can expand the voltage range across the pseudo-resistor. The equivalent resistance can be deduced as below.

$$R = \frac{nV_T}{2\mu_n C_{ox}\frac{W}{L}(e^{-V_{GS}}-1)} + \frac{n\zeta V_T}{2\mu_{\mathrm{n}} C_{ox}\frac{W}{L}e^{\frac{V_{GS}}{\zeta V_T}}} \quad (1)$$

where V_{t} is the total voltage range of the pseudo-resistor. n is the number of MOS transistors in the pseudo-resistor. R is the resistance value of the pseudo-resistor. μ_n and C_{ox} are process parameters. W/L is the width to length ratio. $V_T = kT/q$ is the thermal voltage. $\zeta > 1$ is a non-ideal factor.

B. OTA with Series-parallel Current Mirrors

An OTA using series-parallel current mirror technique is shown in Fig. 3 [5]. In this case, the current mirror uses a series and parallel current mirror structure. This allows the current to to be reduced by a factor of N^2 [13]. Effective output transconductance can be calculated as

$$G_m = \frac{g_m}{N^2} \quad (2)$$

where g_m is the transconductance of the input PMOS transistors.

C. The Proposed Ultra-low Transconductance OTA

The structure of the proposed ultra-low transconductance OTA is shown in Fig. 4. The module on the left is the bulk-driven input stage OTA with source degeneration feedback and series-parallel current mirrors. The small module on the top consisting of four MOS transistors is the common-mode feedback (CMFB) circuit of the OTA.

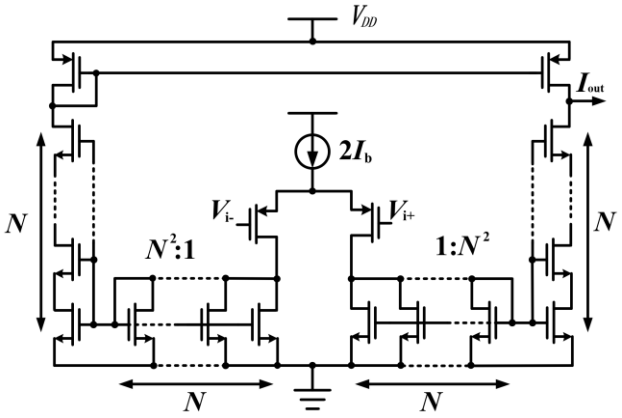


Fig. 3. The schematic of OTA with series-parallel current mirrors.

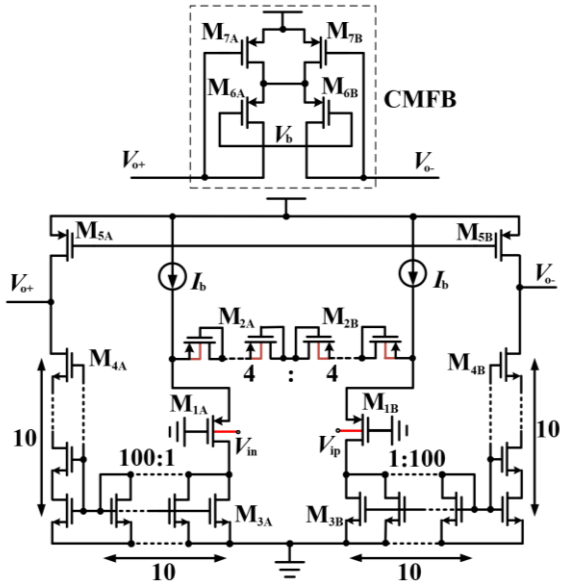


Fig. 4. The proposed ultra-low transconductance OTA structure.

The input stage of the OTA uses the source degeneration feedback technique and the bulk driven technique to extend the linear input range. The source degeneration feedback resistor is replaced by the proposed pseudo-resistor. V_{DD} is set to 1.8V. The bias current I_b is extremely low, which is set to 50pA. The resistance of pseudo-resistance can be calculated to be about 8GΩ from (1).

The bulk-driven OTA topology utilizes the transistor body terminals of the differential pair to achieve higher transconductance linearity and larger input range compared to the conventional gate-driven topology [14][15]. Another advantage of the body-driven topology over the gate-driven approach is the reduced minimum supply voltage required for operation [16]. The gate terminals of the differential pair transistor M_{1A} and M_{1B} is connected to ground instead of the input signal voltage, which normally has a typical common-mode voltage of half the supply voltage.

The common-mode feedback circuit is added to enable the OTA to accurately set the output common-mode voltage value and improve the linearity [17][18]. In this design, the common-mode output is designed to be 1V. The same size MOS transistors M_{7A} and M_{7B} operate in the deep linear region, which are used to sense the common mode voltage difference of V_{o+} and V_{o-}. The two transistors M_{6A} and M_{6B} biased by V_b work in the subthreshold region as large resistors. The common mode voltage difference is compensated through M_{6A} and M_{6B}.

The proposed ultra-low transconductance OTA circuit also utilizes series-parallel current mirrors. The current mirror shunt factor N is 100. In the output stage, the series NMOS transistor array can be equated to one NMOS transistor with N times its channel length. The current of the series NMOS is $1/N$ of each NMOS transistor in the parallel array. So we get (3).

$$\frac{V_{\text{in}} g_{\min}}{N} = N I_{\text{out}} \tag{3}$$

Therefore, the equivalent transconductance of the OTA can be expressed as

$$G_m = \frac{I_{\text{out}}}{V_{\text{in}}} = \frac{g_{\min}}{N^2} \tag{4}$$

$$g_{\min} = \frac{g_{m1}}{1 + \zeta g_{m1} R} \tag{5}$$

Where N is the number of MOS transistors in the array. $g_{\min}$ is the equivalent transconductance of the input transistors. g_{m1} is the transconductance of M1. R is the equivalent resistance of pseudo-resistor, which consists of 8 PMOS shown in Fig. 4.

III. Circuit Simulation and Analysis

The proposed ultra-low transconductance OTA is designed using a standard 0.18μm CMOS process. Using the classical differential PMOS pair as the input stage of the ultra-low transconductance OTA, the linear input range of the OTA is obtained as shown in Fig. 5. The linear input range is only about -50mV ~ 50mV.

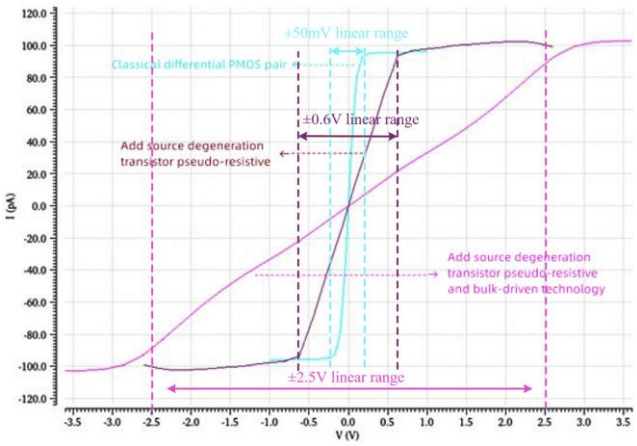
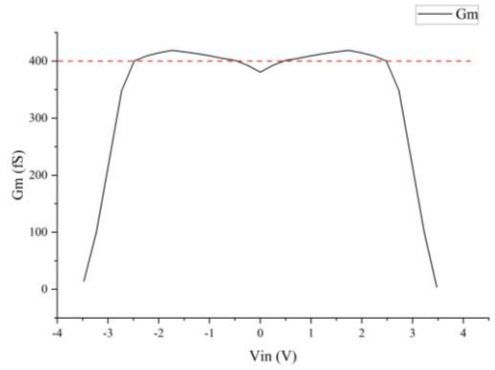


Fig. 5. Simulation results of OTA linear input range comparison for three different input pairs.

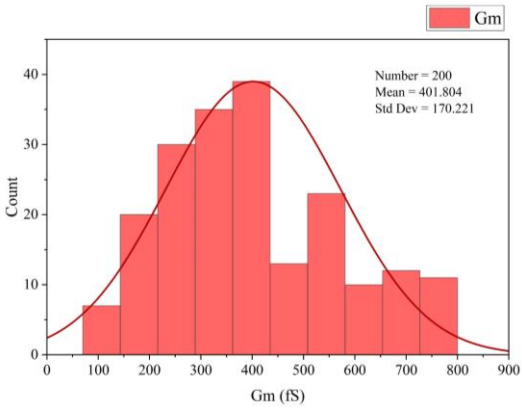
While using a source degeneration transistor pseudo-resistor, the linear input range is approximately -600mV ~ 600mV. Using a source degeneration pseudo-resistor and bulk-driven technology differential PMOS pair as the input stage, the OTA

linear input range is extended to -2.5V ~ 2.5V. So the proposed input pair increases the linear range of the OTA significantly.

In addition, the series-parallel current mirror is used to reduce the already extremely low bias current I_b of 100pA to 1pA. This technique reduces the transconductance of the OTA to be 0.4pS, as shown in Fig. 6(a). Transconductance varies with the process variations, as shown in Fig. 6(b).With 200 runs of Monte Carlo simulation, transconductance features a standard deviation of 170.221fS. The noise and CMRR simulation of the ultra-low transconductance OTA are shown in Fig. 7. The total voltage noise is calculated to be $39.55\mu V_{rms}$ and the CMRR is 74.137dB.



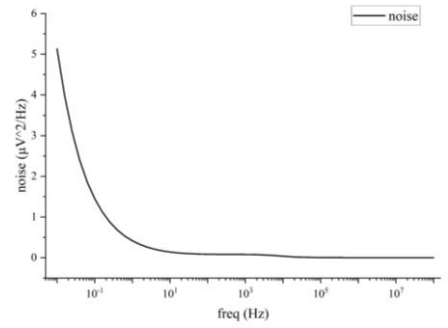
(a)



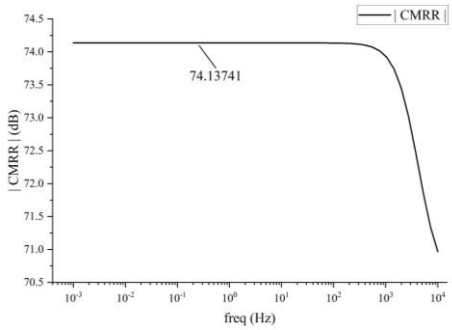
(b)

Fig. 6. (a)Transconductance of OTA. (b) Monte Carlo simulation results of transconductance.

The performance of the proposed ultra-low transconductance OTA is compared with other designs and the results are summarized in Table I. It can be seen that the proposed circuit structure significantly reduces the OTA transconductance. The transconductance value of 0.4pS is an order of magnitude lower than that of other low transconductance OTAs in the literature. The linear input range of the proposed ultra-low transconductance OTA is -2.5V ~ 2.5V, which is much larger than other designs. In addition, the table also shows that the ultra-low transconductance OTA has the advantages of low bias current and low noise.



(a)



(b)

Fig. 7. (a) The proposed OTA noise simulation results. (b) CMRR simulation results.

IV. Conclusion

In this paper, an ultra-low transconductance OTA structure is proposed. It consists of a source degeneration pseudo-resistor and bulk-driven technology input stage, a common-mode feedback circuit, and an input symmetrical OTA with series-parallel current mirrors. The linear input range and transconductance of the proposed ultra-low transconductance OTA are -2.5V ~ 2.5V and 0.4pS respectively. Compared with other designs, the proposed ultra-low transconductance OTA extends the linear range by a factor of 50. The noise achieves $39.55\mu V_{rms}$ and common mode rejection is 74.137dB. The proposed ultra-low transconductance OTA can be used in biomedical sensor applications.

TABLE I. Low Transconductance OTA Parameter Comparison with Literature

Parameters	[4]	[6]	[8]	[15]	[18]	This work
Supply Voltage (V)	1.8	2.5	0.5	0.3	0.9	**1.8**
CMOS Process (μm)	0.8	0.35	0.18	0.13	0.18	**0.18**
Linear Input Range (V)	−0.5 ~0.5	–	−0.25 ~0.25	−0.15 ~0.15	−0.25 ~0.25	**−2.5 ~2.5**
CMRR (dB)	–	44.8	–	54.88	–	**74.137**
Transconductance (nS)	69	36	20	–	5.5	**0.0004**
Bias Current (nA)	–	–	5	7.125	1	**0.1**
Noise (μV_{rms})	190	332	–	3.156	91.2	**39.55**

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