



A 10.16% Efficiency On-Chip Solar Cells With Analytical Model Based on a Standard Bulk CMOS Process for Self-Powered Microsensors

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Abstract—Energy harvesting systems can power microsensors by harvesting energy from the environment. On-chip solar cells made by photodiodes serve as crucial components for highly-integrated energy harvesting systems. To maximize the vertical photoactive area and achieve on-chip solar cells with enhanced photoelectric conversion capabilities, the photoactive area is increased by segmenting the doped region. With the assistance of an approximate model, an optimized segmented triple-well photodiode design is proposed and implemented in a standard $0.18\mu\text{m}$ bulk CMOS process. Measurement results demonstrate a photoelectric conversion efficiency of 10.16% for the proposed segmented triple-well on-chip solar cell, which represents a 39.94% improvement compared to traditional unsegmented triple-well on-chip solar cells. The short-circuit current is 26.51% higher than that of the traditional one.

Index Terms—On-chip solar cells, energy harvesting system, photodiode model, triple-well photodiodes, smart dust.

I. INTRODUCTION

SELF-POWERED microsensors are required for smart dust applications [1], [2]. TABLE I shows the power consumption required of some microsensors, and the demand for power consumption in the microwatt range or even lower makes the use of on-chip solar cells for powering microsensors have great development potential [2], [3]. The integration of on-chip solar cell energy harvesting system and functional circuits on the same chip has been achieved [4]. The on-chip solar cells based on standard bulk CMOS processes help to reduce manufacturing costs [5], [6]. However, due to the design rules of CMOS processes and the limitations of silicon materials, the photoelectric conversion efficiency of common single PN junction photodiodes, as shown in Fig. 1, is relatively low. The photovoltaic conversion efficiencies of single PN solar cells made from N+/P-sub and P+/N-well are only 5.73% and 2.1%, respectively [4], [5]. The low photoelectric conversion

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TABLE I
THE POWER CONSUMPTIONS OF MICROSENSORS

Sensors	Image sensor [7]	Temperature sensor [8]	Pressure & temperature sensor [9]	Temperature sensor [10]
CMOS Process	$0.18\mu\text{m}$	$0.18\mu\text{m}$	$0.13\mu\text{m}$	$0.15\mu\text{m}$
Power	$3.6\mu\text{W}$	75nW	$2.3\mu\text{W}$	2.5nW

efficiency of on-chip solar cells necessitates a larger area and stronger illumination to meet the power requirements of microsensors. Undoubtedly, this hinders the miniaturization and application of on-chip solar cells. Therefore, it is very important to improve the photovoltaic conversion efficiency of on-chip solar cells through structural optimization.

Previous studies have demonstrated that by changing the structure of the photodiodes, more photosensitive PN junctions can be obtained in the vertical edge area, thereby improving the power generation of the on-chip solar cell [11], [12], [13]. In addition, a triple-well structure was used in the design of on-chip solar cells [14]. In contrast to single-well on-chip solar cells, the triple-well on-chip solar cells feature an increased number of planar photosensitive PN junctions, and therefore have stronger photoelectric conversion capabilities. To maximize the photosensitive area in this work, segmented doping regions are employed to enhance the photoactive area along the vertical edges, and incorporate a triple-well structure to further increase the number of planar photosensitive PN junctions. Additionally, we propose an approximate model and formulas to optimize the segmentation method for triple-well on-chip solar cells.

II. BASIC THEORY AND MODEL OF PHOTODIODES

The short-circuit current I_{SC} serves as an indicator of the photodiode's ability to convert light into electricity. The short-circuit current density per unit area J_{SC} can be expressed as (1), in which e is the electron charge, λ is wavelength, and d

$$J_{SC} = e \int_0^{\infty} \text{QE}(\lambda, d) \cdot \Phi_{\text{inc}}(\lambda) d\lambda \quad (1)$$

is the penetration depth. $\Phi_{\text{inc}}(\lambda)$ is the incident light intensity per unit area and $\text{QE}(\lambda, d)$ is the quantum efficiency [15].

We divide the photoactive area of the photodiode into two parts, as shown in Fig. 1. One is parallel to the surface of the photodiode, formed by the bottom edge of the N+ region and the P-sub, which we call the bottom photoactive area

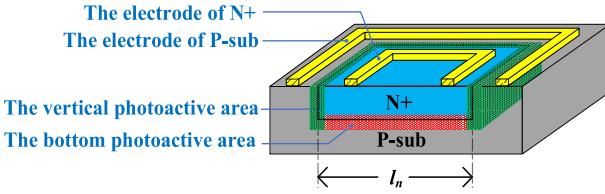


Fig. 1. The common single-well on-chip solar cell.

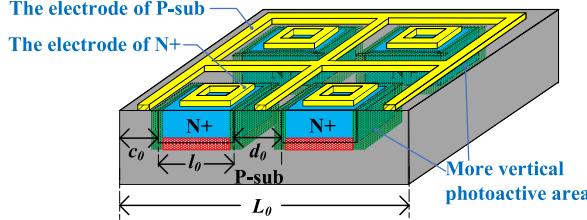


Fig. 2. Segmented N+/P-substrate on-chip solar cell.

(red region); the other is perpendicular to the surface of the photodiode, formed by the vertical edge of the N+ region and the P-sub, which we call the vertical photoactive area (green region). Their respective short-circuit current densities are J_b and J_v .

The photoactive area mentioned in the letter includes the depletion region of the PN junction and the nearby region outside the depletion region due to peripheral response. The peripheral response is caused by the diffusion movement of photogenerated carriers, which makes the actual photoactive area to be larger than the depletion region. W_{DN} and W_{DP} are the width of the N+ side depletion region and the P-sub side depletion region, respectively. To simplify the model while considering the peripheral response, the actual photoactive area is considered k times the depletion region width.

Considering the spatial distribution of bottom and vertical photoactive areas, by substituting parameters into (1), we get expressions for J_b and J_v shown in (2) and (3) respectively. The parameter a represents the photocurrent of bottom photoactive area as shown in (4) and b represents the photocurrent in the vertical photoactive area per unit length as shown in (5). The total short-circuit current I_{SC} of the photodiode in Fig. 1, is given by (6), where l_n is the side length of the N+ region.

$$J_b = e \int_0^\infty \Phi_{inc}(\lambda) \cdot \left[\frac{QE(\lambda, d + W_{DP} \cdot k)}{-QE(\lambda, d - W_{DN} \cdot k)} \right] d\lambda \quad (2)$$

$$J_v = e \int_0^\infty \Phi_{inc}(\lambda) \cdot QE(\lambda, d + W_{DP}) d\lambda \quad (3)$$

$$a = J_b \quad (4)$$

$$b = k \cdot (W_{DP} + W_{DN}) \cdot J_v \quad (5)$$

$$I_{SC} = a \cdot l_n^2 + 4 \cdot l_n \cdot b \quad (6)$$

III. DESIGN OF HIGH-EFFICIENCY ON-CHIP SOLAR CELL

A. Single-Well on-Chip Solar Cells

To increase the vertical photoactive area, we divide a large N+ doped segment into multiple smaller N+ doped regions. Fig. 2 shows a photodiode with an area of $L_0 \times L_0$. The distance d_0 between two adjacent N+ regions and the distance c_0 from N+ to the edge of P-sub are determined by the design rules and the layout traces of the metal electrodes.

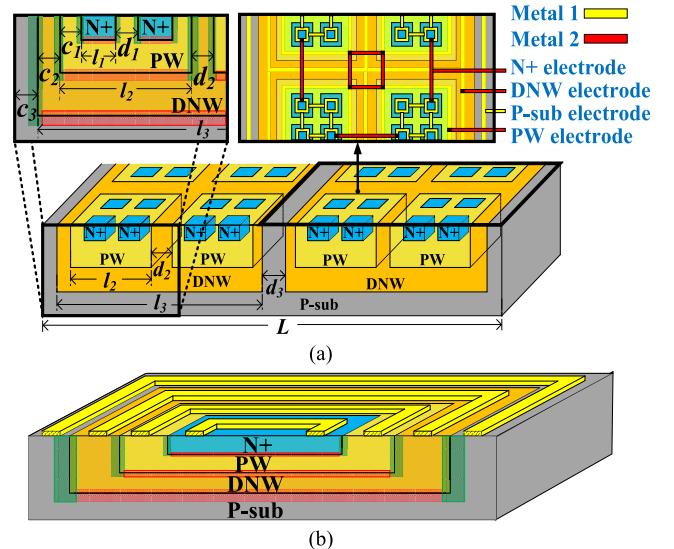


Fig. 3. (a) The illustration diagram of the proposed segmented triple-well on-chip solar cell. (b) The traditional triple-well on-chip solar cell.

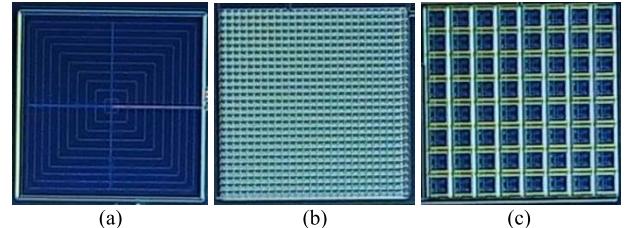


Fig. 4. The micrograph of the fabricated three on-chip solar cells, (a) 1 DNW, 1 PW, and 1 N+, (b) 729 DNWs, 1 PW in each DNW, and 1 N+ in each PW, (c) 64 DNWs, 1 PW in each DNW and 4 N+ in each PW.

l_0 represents the side length of each small N+ doped region, $n_0 \times n_0$ represents the number of small N+ doped regions, and n_0 can be calculated from (7). The electrode blocks the area of illumination with metal area S_0 . Considering that the majority of metal are located above the bottom photoactive area, the influence of metal on the vertical photoactive area is ignored. The I_{SC} of each small N+ region can be calculated by equation (6), and the total photocurrent I_{SC0} can be obtained by summing up the photocurrents of all small N+ regions, as shown in equation (8).

$$n_0 = (L_0 + d_0 - 2c_0) / (l_0 + d_0) \quad (7)$$

$$I_{SC0} = [a \cdot (l_0^2 - S_0) + 4 \cdot l_0 \cdot b] \cdot n_0^2 \quad (8)$$

In order to find the maximum short-circuit current, We take the derivative of l_0 in (8). The result shows that I_{SC0} reaches its maximum value when both (9) and (10) are satisfied simultaneously.

$$\frac{a}{b} \leq 2 \cdot \left(\frac{1}{d_0} - \frac{1}{L_0 - 2c_0} \right) / \left[1 + \frac{S_0}{d_0(L_0 - 2c_0)} \right] \quad (9)$$

If (9) is not satisfied, I_{SC0} increases as l_0 increases. This means that when l_0 reaches its maximum value, $l_0 = L_0 - 2c_0$ (that is undivided doping region), I_{SC0} reaches its maximum value.

$$l_0 = (1 + \frac{a \cdot S_0}{b \cdot 2}) / \left(\frac{1}{d_0} - \frac{a}{2b} \right) \quad (10)$$

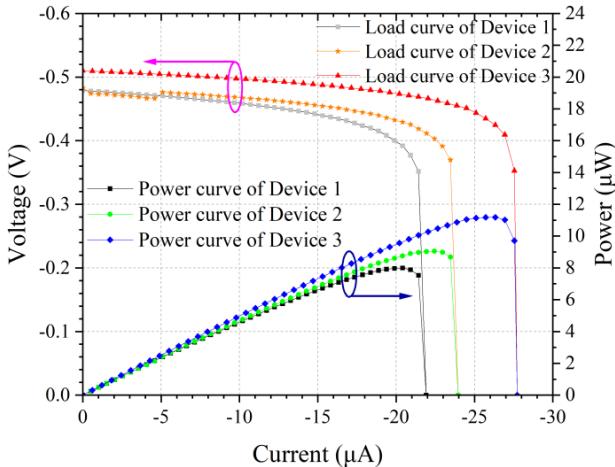


Fig. 5. Measurement results of short-circuit current and power of three types of 0.1mm^2 triple-well on-chip solar cells.

B. Triple-Well on-Chip Solar Cells

Fig. 3 (a) and (b) show the structures of the proposed segmented triple-well on-chip solar cell and the traditional triple-well on-chip solar cell, respectively. We connect PW and P-sub to ground and short-circuit DNW and N+ as output terminals of the solar cell. Using the same logic as above, we can derive the total short-circuit current I_{SC1} of the triple-well on-chip solar cell from (11). By taking the partial derivatives of l_1 , l_2 , and l_3 in (11), we can obtain the optimal values of l_1 , l_2 , and l_3 , thereby maximizing I_{SC1} of the proposed triple-well on-chip solar cell. Since the exact values of N+, PW, and DNW's doping concentration and doping depth cannot be determined, we can only use approximate orders of magnitude in the model. The orders of magnitude for N+, PW, and DNW's doping concentration are $10^{19}\text{n}/\text{cm}^3$, $10^{17}\text{n}/\text{cm}^3$, and $10^{16}\text{n}/\text{cm}^3$, respectively, while the orders of magnitude for the doping depth are $0.1\ \mu\text{m}$, $1\ \mu\text{m}$, and $10\ \mu\text{m}$, respectively.

$$\begin{aligned} I_{SC1} = & \left[a_3 \cdot (l_3^2 - S_3) + 4 \cdot b_3 \cdot l_3 \right] \cdot n_3^2 \\ & + \left[a_2 \cdot (l_2^2 - S_2) + 4 \cdot b_2 \cdot l_2 \right] \cdot n_2^2 \cdot n_3^2 \\ & + \left[a_1 \cdot (l_1^2 - S_1) + 4 \cdot b_1 \cdot l_1 \right] \cdot n_1^2 \cdot n_2^2 \cdot n_3^2 \quad (11) \end{aligned}$$

IV. MEASUREMENT RESULTS

Three 0.1mm^2 on-chip solar cells are designed by a standard $0.18\mu\text{m}$ bulk CMOS process. The micrograph of the fabricated three on-chip solar cells are shown in Fig. 4. Device 1 is a traditional triple-well on-chip solar cell. Device 2 is an excessively segmented triple-well on-chip solar cell. Device 3 is the proposed segmented triple-well on-chip solar cell which is optimized by (11). It consists of 64 DNWs, 1 PW in each DNW and 4 N+ in each PW. It should be noted that, due to inherent deviations between the model and actual fabrication, the optimized structure derived from our analysis serves as an approximation of the true optimal structure, though it may not represent the absolute fabrication optimum.

Under vertical illumination of a 110k lux solar simulator, we have measured three different structures of solar cells. The load lines and power curves corresponding to the three structures of triple-well solar cells are shown in Fig. 5. The

TABLE II
THE IMPORTANT INDICATORS OF ON-CHIP SOLAR CELLS

Device & Area	Light source	V_{open} (V)	I_{short} ($\mu\text{A}/\text{mm}^2$)	Power density ($\mu\text{W}/\text{mm}^2$)	η
#Ringo chip planarized & 0.16cm^2 [3]	AM 100k lux*	0.88	151.9	70.6*	7.1%
N+/P-sub Photodiode & 1cm^2 [4]	Solar simulator 100k lux	0.54	135	57.3	5.73%
P+/N-well Photodiode & 0.006mm^2 [5]	Halogen EKE	0.45	3.83	1.3	2.1%
NW/P-sub Photodiode & 0.75mm^2 [6]	830nm laser	0.5	142	N/A	7.45%
Device 1 & 0.1mm^2	Solar simulator 110k lux	0.47	219.2	79.9	7.26%
Device 2 & 0.1mm^2	Solar simulator 110k lux	0.48	239.5	90.4	8.22%
Device 3 & 0.1mm^2	Solar simulator 110k lux	0.51	277.3	111.8	10.16%

η is the photoelectric conversion efficiency

*Estimated from the corresponding literature

#Non-standard CMOS processes

key parameter values are summarized in TABLE II. Compared to the traditional triple-well on-chip solar cell (Device 1) and those with excessive segmentation (Device 2), the optimized triple-well on-chip solar cell (Device 3) exhibits higher short-circuit current, maximum power, and photoelectric conversion efficiency. In Fig. 4, the bright regions are caused by metal reflection. Apparently, under the same area, Device 2 has the largest metal coverage area due to the necessary electrode contacts and metal routing, causing light to be reflected by the metal. Therefore, Device 2 does not significantly improve its photoelectric conversion capability due to an inappropriate segmentation method. However, the performance of Device 2 is still better than Device 1. This means the segmentation is useful and necessary. The Device 3 is designed by the optimized segmentation method and achieved 10.16% of photoelectric conversion efficiency and $277.3\mu\text{A}/\text{mm}^2$ of I_{short} , which has a 39.94% and 26.51% improvement compared to Device 1.

V. CONCLUSION

In this work, the photoelectric conversion efficiency of on-chip solar cells is improved by optimizing the segmentation of triple-well solar cells. Under the guidance of the proposed approximate model, the photovoltaic conversion efficiency of the optimized triple-well on-chip solar cell is 10.16% and has an improvement of 39.94% compared to that of traditional triple-well one. The short-circuit current is also improved by 26.51%. The proposed segmentation model is proved to be effective in the on-chip solar cell design.

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