A High Dynamic Range Pixel with Inverse Proportional Response

Yuchen Wang, Wenji Mo, Haoning Sun, Jingjing Liu*

School of electronics and communication engineering, Sun Yat-sen University, Shenzhen 518107, China

* Email: wangych79@mail2.sysu.edu.cn, liujj77@mail.sysu.edu.cn

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***Abstract*—This paper proposes a high dynamic range (HDR) pixel that combines linear response and inverse proportional response. This pixel achieves nonlinear compression of light intensity under inverse proportional response to improve dynamic range (DR), suitable for CMOS image sensors (CIS) with rolling shutter operation. The proposed pixel is composed of only 4 MOSFET. In HDR mode, it loads the output signal with brightness information dynamically onto the column signal bus. This pixel does not rely on the I-V characteristics of the CMOS subthreshold region and adopts a hard reset structure, overcoming the problems of poor low light SNR performance and image lagging in the traditional logarithmic pixels. The use of low threshold NMOS transistors in the pixel circuit results in the swing of the pixel output close to the power supply voltage, improving the low-voltage performance of the pixel circuit and bringing higher DR. Under a standard CMOS process, the pixel pitch is 6.6μm with a fill factor of 37.6%. The post simulation results indicate that the proposed pixel has good linear and inverse proportional responses to photocurrent. Compared to the linear mode, this pixel has a DR improvement of at least 31.9dB in the HDR mode.**

Keywords—CMOS image sensors (CIS), high dynamic range (HDR), inverse proportional response

I. Introduction

Dynamic range (DR) of CMOS image sensors (CIS) is one of the important criteria for evaluating performance. Human eye can achieve a DR of about 130dB by adjusting the pupil size. However, the DR of current commercial cameras usually does not exceed 70dB. Many methods to expand the DR of CIS have been investigated.

The traditional HDR is achieved by imaging the same scene multiple times with different exposure times [1]. Other techniques that use linear pixels to extend DR include completing two different exposure times within one single frame [2], adding additional integration capacitors to the pixels, using high-resolution ADC for high supply voltages [3], and using pulse frequency pulse width modulation to obtain for digital pixel outputs for low supply voltages [4], etc.

In addition, logarithmic response pixels can also be used to improve the DR. The logarithmic pixels utilize the I-V characteristic of MOSFETs operating in the subthreshold region to achieve nonlinear compression of light intensity. However, operating in the subthreshold region makes them vulnerable to fixed pattern noise (FPN). Small pixel output swing, poor low light SNR performance, and image lagging are also issues with the logarithmic pixels [5-6].

This paper proposes a novel HDR pixel, which mimics the human eye and exhibits an inverse proportional response to light intensity. The pixel can also achieve the same linear response characteristics as traditional 3T pixels by reconfiguring the control signal. This pixel circuit consists of only 4 MOSFETs and is suitable for CIS with rolling shutter operation. Different from the traditional linear pixels that output stable voltage values, the proposed pixel dynamically loads the output signal with brightness information onto the column signal bus, thus obtaining larger DR. And unlike traditional logarithmic pixels, the proposed pixel does not have transistors operating in the subthreshold region, resulting in a smaller FPN due to the process variations. Hard reset structure is used in the pixel, so there is no image lagging. In addition, low threshold NMOS transistors are used within the pixel, achieving a swing of the pixel output close to the power supply voltage, resulting in better SNR performance for low supply voltages.

II. The Proposed Pixel Structure And Operations

The structure of the proposed HDR pixel circuit and quantization circuit are shown in figure 1, and the schematic of a single pixel is shown in the dashed box. One pixel consists of one photodiode and four MOSFETs, requiring three control signals including a reset signal rst, gating signal sel and $\overline{sel}$. Among them, M1 and M3 are nominal threshold voltage PMOS, M2 is a native NMOS, and M4 is a medium threshold voltage NMOS. M1 uses PMOS to hard reset the photodiode to VDD, which can avoid image lagging caused by charge residue and also improve the swing of the pixel output signal. The native NMOS as the source follower and the transmission gate can also improve the output swing. The use of medium threshold voltage NMOS in M4 is a compromise between the performance and layout of the transmission gate under low power supply voltage. A larger swing provides a better SNR performance. The pixel output signal swing is only limited by the threshold voltage of the native NMOS M2 and the voltage drop of the source follower load.

The proposed high dynamic range pixels can operate in linear mode or HDR mode by changing the control signal and quantization circuit transmission path. The comparator compares the pixel output with a rising slope signal to obtain a pulse width modulation (PWM) signal containing the pixel brightness information. Then, the counter converts the PWM signal into a digital code to complete the quantization process of the pixel output.

A. HDR Mode

When the pixel operates in HDR mode, the quantization circuit keeps the switch HDR on and the switch LIN off. The key node voltage and control signal waveforms in the HDR mode are shown in Fig. 2. The maximum exposure time for the pixel is set to T. Firstly, before the time 0, M1 keeps on

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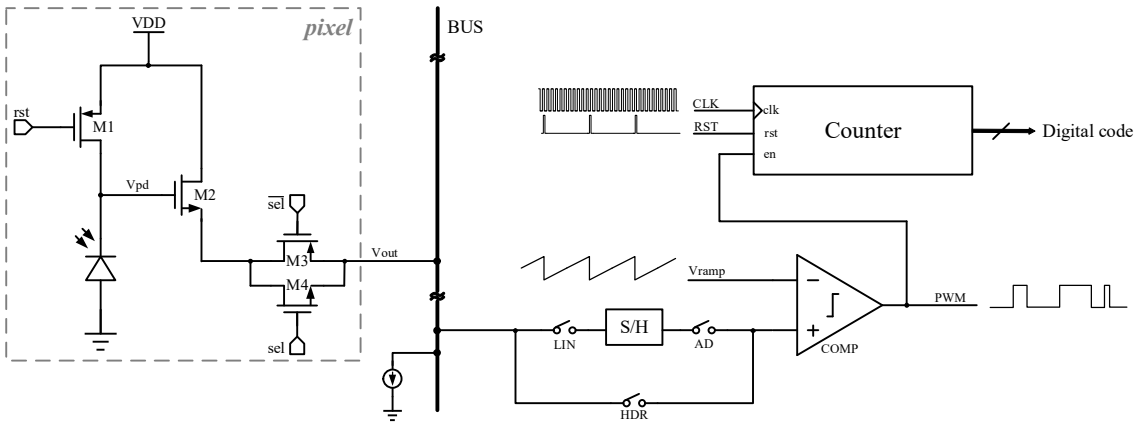

Fig. 1. The structure of the proposed HDR pixel circuit and quantization circuit.

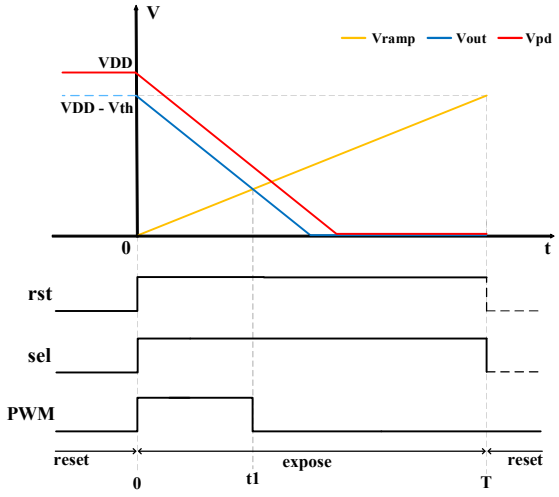

Fig. 2. Key node voltage and control signal waveforms in HDR mode.

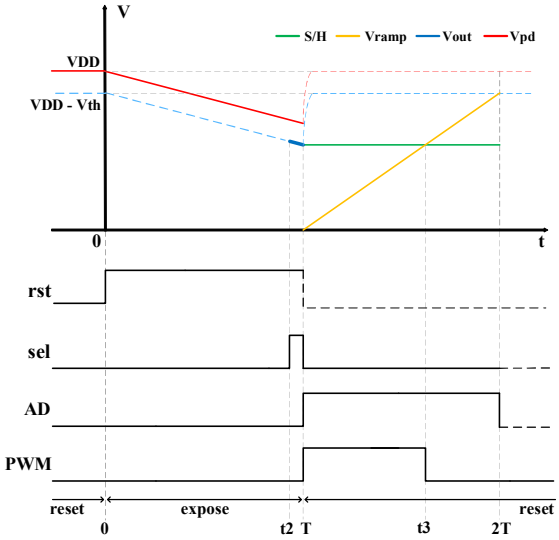

Fig. 3. Key node voltage and control signal waveforms in Linear mode.

and the photodiode node is reset to the power supply voltage VDD. At the time 0, M1 turns off and the cathode node voltage Vpd of the photodiode gradually decreases under the illumination. At the same time, the transmission gate composed of M3 and M4 turn on, and Vpd is amplified by M2 and transmitted to the column signal bus through the transmission gate as $Vout$. $Vout$ has a decrease of M2 threshold voltage compared to Vpd signals, which is given by (1):

$$Vout = Vpd - Vth = VDD - \frac{Ipd \cdot t}{C} - Vth \qquad (1)$$

where t denotes any time within the range of 0 to T. Ipd represents the photocurrent generated by the photodiode. C is the total parasitic capacitance of the photodiode, drain of M1, and gate of M2. Vth is the threshold voltage of M2. In HDR mode, pixel exposure, read out, and quantization are performed at the same time. The output of proposed pixel is a dynamic waveform rather than a stable voltage, which is different from the traditional pixels.

Within $0{\sim}T$, the negative input terminal voltage of the comparator has an expression for the ramp signal $Vramp$ that rises from 0 to $VDD - Vth$:

$$Vramp = \frac{VDD - Vth}{T} \cdot t \qquad (2)$$

$Vout$ is directly connected to the positive input of the comparator, and it gradually decreases from $VDD - Vth$ at the time 0. Therefore, within $0{\sim}T$, $Vout$ and $Vramp$ have only one intersection point. Let this moment be $t1$, at this intersection, the comparator flips from high level to low level, that is, the comparator output converts the pixel output signal into a PWM signal with a pulse width of $t1$. Combine (1) and (2) to obtain the expression for pulse width:

$$Vout = VDD - \frac{Ipd \cdot t1}{C} - Vth$$
$$= Vramp = \frac{VDD - Vth}{T} \cdot t1 \qquad (3)$$

$$PW_{HDR} = t1 - 0 = \frac{(VDD - Vth) \cdot C}{\frac{(VDD - Vth) \cdot C}{T} + Ipd} \qquad (4)$$

where PW_{HDR} represents the pulse width of the comparator's output PWM signal in HDR mode. From (4), it can be seen that PW_{HDR} is inversely proportional to Ipd. When $Ipd = 0$, $PW_{HDR} = T$. And, when $Ipd = \infty$, $PW_{HDR} = 0$. Therefore, in an ideal scenario, the proposed pixel in the HDR mode would not experience saturation.

B. Linear Mode

When the pixel operates in the linear mode, the switch HDR is off and the key node voltage and control signal waveforms are shown in Fig. 3. The pixel is exposed within $0{\sim}T$. At the end of the exposure, $Vout$ satisfies (1) when $t = T$. The waveform of LIN is same as sel. At the time $t2{\sim}T$, the transmission gate conducts, and the pixel output $Vout$ is transmitted to the sample and hold (S/H) circuit through the column signal bus. Within $T{\sim}2T$, the positive input of the comparator is connected to the S/H, which maintains $Vout$

voltage level at the time T, while the negative input of the comparator is connected to a ramp voltage $Vramp$ that rises from 0 to $VDD - Vth$. Within $T \sim 2T$, there is a unique intersection point between the S/H voltage and $Vramp$, which causes the comparator output to transition from high level to low level. Let this moment be $t3$, the expression of $t3$ regarding the photocurrent can be obtained:

$$S/H = VDD - \frac{Ipd \cdot T}{C} - Vth$$
$$= Vramp = \frac{VDD - Vth}{T} \cdot (t3 - T) \qquad (5)$$

The pulse width of the comparator output signal can be expressed as:

$$PW_{LIN} = t3 - T = T - \frac{T^2}{(VDD - Vth) \cdot C} \cdot Ipd \qquad (6)$$

where PW_{LIN} is the pulse width of the PWM signal output of the comparator in the linear mode. From (6), it can be seen that PW_{LIN} has a linear relationship with Ipd, and there is no difference from the traditional 3T pixels.

III. Post-Layout Simulation Result

The proposed pixel layout adopts a stander 180nm technology, occupying an area of 6.6 × 6.6μm and a filling factor of 37.6%, as shown in Fig. 4. Each pixel contains one photodiode, four MOSFETs, three horizontal metal wires and three vertical metal wires.

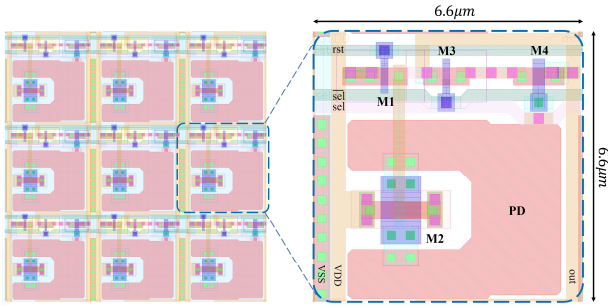

Fig. 4. Layout of proposed pixel.

The post-layout simulation uses a two-stage rail to rail operational amplifier circuit as a comparator to compare the pixel output signal $Vout$ with the ramp signal $Vramp$ and obtain the PWM signal. The parasitic parameters are extracted. The parasitic capacitance of the photodiode node is 1.6fF, and the threshold voltage of M2 is 0.91mV. Under a working voltage of 1V, set the exposure time T to 0.5ms, and simulate in linear mode and HDR mode, respectively. The curves of the relationship between the pulse duty cycle of the PWM signal and the photocurrent are shown in Fig. 5 and 6, respectively.

The post-layout simulation results show that the PWM signal in both operating modes have a duty cycle close to 100% when the photocurrent is low. They also exhibits a property of decreasing pulse width with increasing photocurrent. In the linear mode, the duty cycle of the PWM signal exhibits a good linearity within the photocurrent range of 1~6.5pA and is fully saturated at 7.6pA. In the HDR mode, the duty cycle of PWM signal exhibits an inverse relationship with the photocurrent. The response curve still shows downward trend even at a photocurrent of 300pA, which is approximately 39.5 times compared to the linear mode. Therefore it corresponds to a DR improvement of at least 31.9dB in the HDR mode respect to the linear mode.

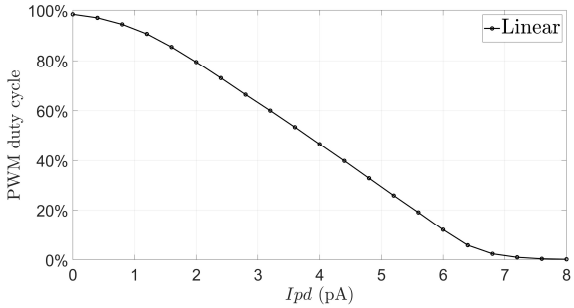

Fig. 5. Simulated response curve of the proposed pixel in linear mode.

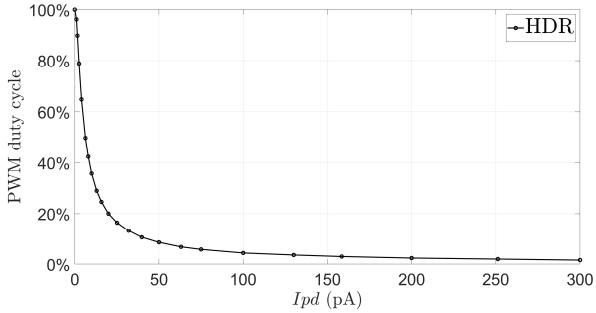

Fig. 6. Simulated response curve of the proposed pixel in HDR mode.

IV. Conclusion

This paper proposes an HDR pixel combined linear and inverse proportional response. The pixel circuit is composed of only 4 MOSFETs, achieves a 6.6μm pixel pitch and 37.6% fill factor under a stander 180nm CMOS technology. The use of hard reset structure and low threshold MOSFETs in the pixel circuit increases the swing of pixel output and improves the performance under the low supply voltage. In the HDR mode, the pixel output is dynamically read out onto the column bus and compared with the ramp voltage to obtain a PWM signal that responds inversely to the photocurrent, greatly expanding the dynamic range of the pixel. The post-layout simulation results show that the DR of the proposed pixel in the HDR mode is at least 31.9dB higher than that in the linear mode.

References

[1] R. Wang, Y. Yin, L. Li, X. Wang, and Y. Chang, "A high dynamic range CMOS image sensor with dual charge transfer phase," *IEEE International Conference on Solid-State and Integrated Circuit Technology*, Hangzhou, China, 2016, pp. 1369-1371.

[2] S. Lou, Y. Qu, G. Zhong, Y. Zheng, B. Xiong, Q. Zhou, Y. Li, X. Wang, and Y. Chang, "An over 140 dB dynamic range CMOS image sensor combined DCG and logarithmic response," *IEEE Transactions on Electron Devices*, vol. 70, no. 9, pp. 4719-4724, Sep. 2023.

[3] M. Seo, T. Takasawa, K. Yasutomi, K. Kagawa, and S. Kawahito, "A low-noise high-sensitivity CMOS image sensor for scientific and industrial applications," *IEEE SENSORS*, Valencia, Spain, 2014, pp. 2163-2166.

[4] A. Chiou and C. Hsieh, "An ULV PWM CMOS imager with Adaptive-Multiple-Sampling linear response, HDR imaging, and energy harvesting," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 1, pp. 298-306, Jan. 2019.

[5] N. Tu, R. Hornsey, and S. Ingram, "CMOS active pixel image sensor with combined linear and logarithmic mode operation," *IEEE Conference on Electrical and Computer Engineering*, Waterloo, Canada, 1998, pp. 754-757.

[6] H. Cheng and S. Collins, "A wide dynamic range integrating pixel with an accurately controlled logarithmic response," *IEEE International Conference on Sensing Technology*, Taipei, Taiwan, 2008, pp. 68-71.