A Self-Biased Subthreshold CMOS Voltage Reference With Temperature Compensation Circuit for IoT Self-powered Sensor Applications

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***Abstract*—This paper presents a subthreshold CMOS voltage reference structure that utilizes self-biased circuits. This voltage reference includes temperature compensation circuits to expand its operating temperature range and reduce its temperature coefficient. The proposed CMOS voltage reference is designed using a standard 0.18-μm CMOS process and has a small area of only 0.005 mm^2. Post-layout simulation results demonstrate that the power consumption of the circuit at room temperature (25°C) is only 1.65 nW at a power supply voltage of 1 V. In this case, the voltage reference output is 316.56 mV, with a temperature coefficient (TC) of 2.79 ppm/°C in a wide temperature range from -40 °C to 140 °C. Furthermore, the line sensitivity (LS) of the circuit is 0.022 %/V.**

Keywords—CMOS voltage reference (VR), subthreshold, self-biased, low power, line sensitivity, low supply voltage, temperature coefficient, low area.

I. INTRODUCTION

To ensure a stable voltage that is independent of process, supply voltage, and temperature (PVT) variations, a well-designed VR circuit is essential. The rapid development of IoT systems in recent years has resulted in the widespread use of low-supply voltage and low-power sensors. However, for self-powered IoT sensor applications, the power supply harvested from ambient energy is often unstable, leading to the need for VR designs with low power consumption, small area, and fast activation. In recent years, many VR circuit designs have been proposed to address the challenges of low power consumption and low-temperature variation. One design utilized a two-transistor VR circuit to achieve ultra-low power consumption and low supply voltage [1]. However, the circuit suffered from significant leakage current and large performance variations even after trimming. The sub-bandgap voltage reference (sub-BGR) that combined with the bipolar junction transistors (BJT) and MOS transistors working in the subthreshold region has emerged as a promising alternative to traditional BGR circuits due to its low power consumption [2-5]. However, the minimum supply voltage is limited by the base-emitter voltage of the BJT, and there is still a power consumption gap between sub-BGR and pure subthreshold CMOS VR circuits. The latter has been shown to have simplified bias circuits and reduced both power consumption and circuit complexity [6-8]. Among subthreshold CMOS VR circuit designs, the stacked diode-connected MOS transistors (SDMTs) have been shown to be effective in achieving PVT immunity for reference voltage through two NMOS transistors with different threshold voltages, making it suitable for low voltage and low power applications [8-11]. However, further improvement is required in terms of temperature coefficients.

In order to solve the mentioned problems, a modified SDMT voltage reference circuit without an operational amplifier is proposed, which features a self-biased circuit design that significantly reduces the circuit's complexity. The paper is structured as follows: Section II discusses the SDMT and the modified SDMT with temperature compensation. Section III provides the design details of the proposed CMOS VR and Section IV presents the post-simulation results. Finally, Section V concludes the paper.

II. SDMT WITH TEMPERATURE COMPENSATION

The use of MOS transistors operating in the subthreshold region enables the generation of complementary-to-absolute-temperature (CTAT) voltage and proportional-to-absolute-temperature (PTAT) voltage. This circuit offers lower power consumption and a lower supply voltage compared to the traditional BGR.

Fig. 1 shows the comparison of the traditional SDMT VR and the proposed SDMT VR with temperature compensation. M_1 and M_3 are thin-oxide NOMS transistors, and the rest transistors are thick-oxide NMOS transistors. All MOS transistors operating in the subthreshold region are biased by ideal current sources I, I_1, and I_2. The drain current (I_D) of these transistors can be expressed as (1).

$$I_D = \mu_n C_{OX} K V_T^2 \exp\left(\frac{V_{GS} - V_{TH}}{m V_T}\right)\left(1 - \exp\left(\frac{-V_{DS}}{V_T}\right)\right) \quad (1)$$

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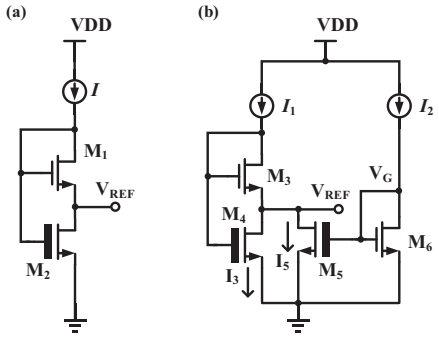

Fig. 1. Conceptual diagrams of (a) SDMT architecture [8] and (b) modified SDMT with temperature compensation circuit.

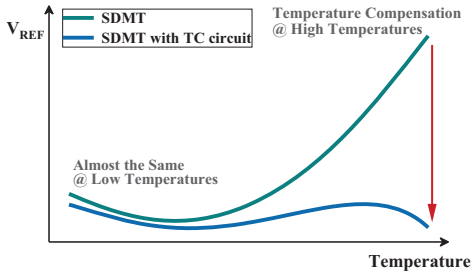

Fig. 2. Illustration of V_{REF} from traditional SDMT and SDMT with temperature compensation circuit.

where μ_n is the mobility of electrons, C_{OX} is the gate oxide capacitance, V_{TH} is the threshold voltage of the transistor, K is the aspect ratio (=W/L) of the transistor, $V_T = k_B T / q$ is the thermal voltage, k_B is the Boltzmann constant, and T is absolute temperature, q is the elementary charge, and m is the subthreshold slope factor. It can be approximated that the C_{OX} and V_{TH} of the same type of NMOS transistors are equal, and the subthreshold slope factor m of any NMOS transistor is equal. When $V_{DS} \geq 3V_T$, the drain current of the transistor in the subthreshold region can be approximated as:

$$I_D = \mu_n C_{OX} K V_T^2 \exp\left(\frac{V_{GS} - V_{TH}}{m V_T}\right). \quad (2)$$

For the traditional SDMT circuit, the same drain current flows through M_1 and M_2. The output voltage is the difference between the gate-source voltage of the two transistors with different gate oxide thicknesses. Therefore, its V_{REF} can be represented as (3).

$$V_{REF} = (V_{TH2} - V_{TH1}) + mV_T \ln\left(\frac{\mu_1 C_{OX1} K_1}{\mu_2 C_{OX2} K_2}\right) \quad (3)$$

It can be seen that the output voltage of the SDMT is insensitive to the bias current. However, it is only first-order coefficient compensation and cannot make the VR has good TC performance at high temperature, as shown in Fig. 2. Therefore, this paper proposes an improved SDMT circuit to compensate for temperature coefficient of VR at high temperature. The gate voltage V_G of M_5 in Fig. 1 can be expressed as:

$$V_G = mV_T \ln\frac{I_2}{\mu_6 C_{OX6} K_6 V_T^2} + V_{TH6}. \quad (4)$$

According to (2) and (4), the drain current of the M_5 can be written as:

$$I_5 = I_2 \times \frac{\mu_5 C_{OX5} K_5}{\mu_6 C_{OX6} K_6} \exp\left(\frac{V_{TH6} - V_{TH5}}{m V_T}\right). \quad (5)$$

Because V_{TH6} is smaller than V_{TH5} and V_T is proportional to temperature, the M_5 drain current I_5 is almost zero at low temperature. As the temperature increases, I_5 can be no longer ignored. Therefore, the temperature performance of the circuit at high temperature is compensated. The output voltage of the SDMT with temperature compensation can be expressed as:

$$V_{REF} = (V_{TH4} - V_{TH3}) + mV_T \ln\left(\frac{I_3}{I_1} \times \frac{\mu_3 C_{OX3} K_3}{\mu_4 C_{OX4} K_4}\right) \quad (6)$$

where $I_3 + I_5 = I_1$. The modified SDMT output voltage is insensitive to the bias current, similar to the traditional SDMT at low temperatures. However, as the temperature gradually increases, the voltage output of the traditional SDMT is dominated by high-order positive temperature coefficients, resulting in the increase of TC. In contrast, the improved SDMT with temperature compensation shows a decrease in the PTAT voltage (second term in 6) coefficient of V_{REF} as temperature increase causes I_5 increases, leading to temperature compensation at high temperatures. Therefore, by improving the SDMT circuit with a temperature compensation structure, the subthreshold CMOS VR proposed in this paper can operate in a wider temperature range and exhibit better TC performance, as shown in Fig. 2.

III. Design of the Proposed CMOS VR

A. Temperature Coefficient

As illustrated in Fig. 3, it shows the schematic of the proposed CMOS VR, which is composed of an improved SDMT with temperature compensation, a self-biased circuit and a start-up circuit. All MOS transistors are operated in the subthreshold region, and M_{N2} and M_{N3} are thick-oxide NMOS transistors. The branch currents I_{P1} and I_{P3} are mirrored from the bias current I_{bias} through cascode current mirrors. The final output reference voltage can be expressed as:

$$V_{REF} = (V_{THN2} - V_{THN1}) + mV_T \ln\left(\frac{I_{N2}}{I_{P1}} \times \frac{\mu_{N1} C_{OXN1} K_{N1}}{\mu_{N2} C_{OXN2} K_{N2}}\right) \quad (7)$$

$$I_{N2} + I_{N3} = I_{P1} \quad (8)$$

$$I_{N3} = I_{P3} \times \frac{\mu_{N3} C_{OXN3} K_{N3}}{\mu_{N4} C_{OXN4} K_{N4}} \exp\left(\frac{V_{THN4} - V_{THN3}}{m V_T}\right) \quad (9)$$

Based on (7)-(9), by adjusting the transistors' size of M_{N1}-M_{N4} and the current ratio of I_{P1}, I_{P3} and I_{bias}, it is possible to create CTAT voltage and PTAT voltage that are well compensated, so that the proposed CMOS VR can extend the operational temperature range and have good TC performance.

B. Process Variations

From (9), the temperature-independent V_{REF} is not only affected by the bias current, but also affected by the threshold voltage V_{TH} of the MOS transistors. Fig. 4 shows the TC of the proposed CMOS VR under different process corners. The Monte Carlo simulation results of output voltage and TC performance of the proposed design are shown in Fig. 5 and Fig. 6 respectively. In 200 runs, the average output voltage is 316.42 mV and its standard deviation is 1.49 mV. The average TC is 11.14 ppm/°C and its standard deviation is 6.07 ppm/°C.

C. Self-biased Circuit

The proposed design generates its bias current through M_{N6} via a self-bias feedback path from the output reference voltage. The generated bias current is then mirrored by the cascode current mirror structure to other branches, as shown in Fig. 3.

D. Start-up Circuit

The self-bias circuit implemented in the proposed design requires a start-up circuit to ensure normal operation. The start-up circuit comprises three MOS transistors, M_{S1}-M_{S3}. M_{S1} acts as a MOS capacitor. When the supply voltage is zero, M_{S3} and M_{S2} are both turned off. Upon powering on the circuit, the start-up circuit starts to work. The gate of M_{S2} charges continuously, causing the gate voltage of M_{S2} to increase until it turns on. The gate voltage of M_{P2}, M_{P4}, and M_{P6} are pulled down, leading to the circuit breaking away from the zero point and gradually entering a normal operating state. Once the output voltage reaches a steady state, M_{S3} turns on. This, in turn, pulls down the gate voltage of M_{S2}, and turns it off. At this point, the start-up circuit completes its task and the power consumption should be close to zero.

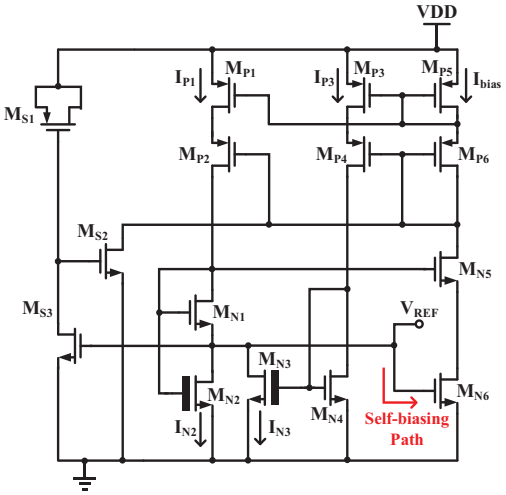

Fig. 3. Schematic of the proposed CMOS VR.

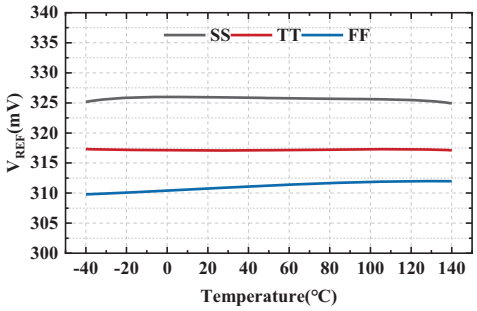

Fig. 4. Simulation results of the proposed VR over process corners.

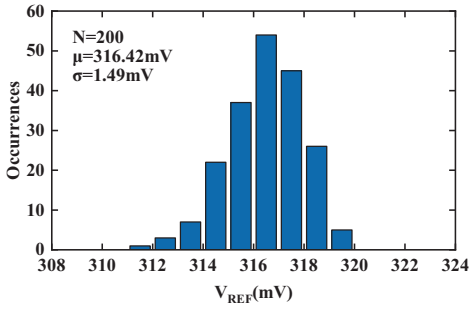

Fig. 5. The Monte Carlo simulation results of V_{REF}.

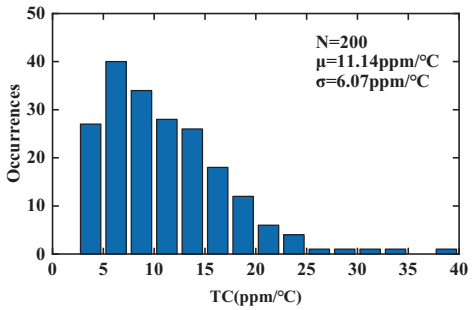

Fig. 6. The Monte Carlo simulation results of temperature coefficient.

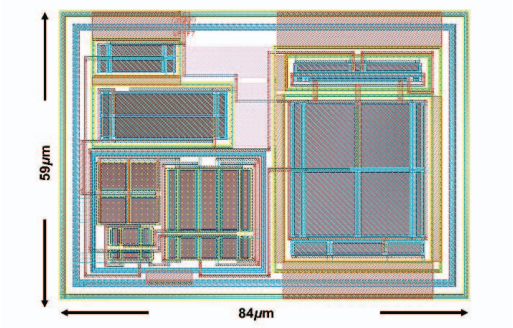

Fig. 7. Layout of the proposed CMOS VR.

TABLE I. PERFORMANCE SUMMARY AND COMPARISON WITH OTHER WORKS.

	this work [a]	JSSC'2020 [8] [b]	ISCAS'2022 [2] [c]	TCAS-I'2017 [9] [b]	ESSCIRC'2018 [10] [b]	TCAS-I'2020 [11] [b]	TCAS-II'2021 [7] [b]
Technology(nm)	**180**	180	130	180	180	180	180
Type	**CMOS**	CMOS	Sub-BGR	CMOS	CMOS	CMOS	CMOS
Supply Voltage(V)	**0.7-2.4**	0.9-1.8	0.9	0.6-3.3	0.5-2.5	0.34-1.8	0.25-1.8
Power (nW)	**1.65**	1.8	30	0.184	0.65	0.046	0.113
V_{REF}(mV)	**316.59**	261	474	378	211.5	147.9	118.1
Temp. Range(°C)	**-40~140**	-40~130	-20~80	0~120	-40~125	0~100	-40~140
TC(ppm/°C)	**3.81**	62	19	495	152.8	14.8	73.5
LS(%/V)	**0.022**	0.013	0.1	0.11	0.031	0.019	0.3
Area(mm^2)	**0.005**	0.005	0.04	0.0017	0.0012	0.0332	0.0009
Self-biased	**Yes**	Yes	No	Yes	Yes	Yes	Yes

[a] Post-simulation results. [b] Measurement results. [c] Simulation results.

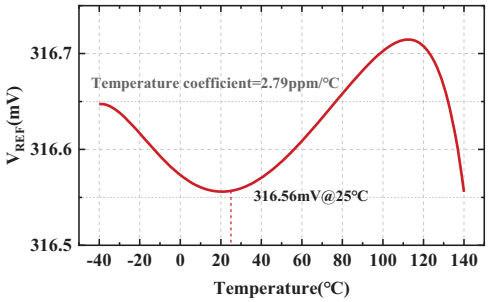

Fig. 8. Post-simulation results of the reference voltage from -40 °C to 140 °C.

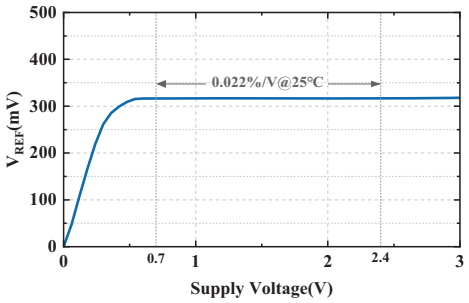

Fig. 9. Post-simulation results of the proposed CMOS VR line sensitivity.

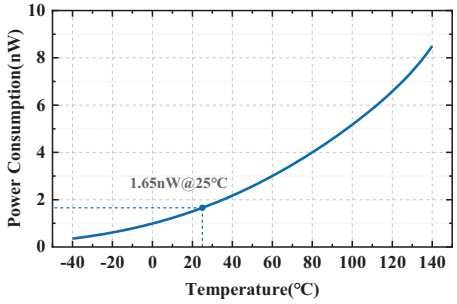

Fig. 10. Post-simulation results of the proposed CMOS VR power consumption at different temperature.

IV. POST-SIMULATION RESULTS

The proposed voltage reference circuit is implemented by all MOSFET, and designed using a standard 0.18-μm CMOS process. Fig. 7 shows the circuit layout and it occupies an area of 0.005 mm^2. Fig. 8 shows the TC of the proposed CMOS VR. Due to the use of an improved SDMT structure, the operating temperature range and TC performance have been significantly enhanced. As a result, the achieved TC is 2.79 ppm/°C within a wide temperature range of -40 °C to 140 °C.

Fig. 9 presents the LS of the proposed design at room temperature. The LS is improved by the cascode current mirror structure and the high impedance of the bias current branch. Moreover, there is a weak correlation between the output voltage and current. The LS of the circuit over a wide power supply voltage range (0.7 V - 2.4 V) is only 0.022%/V. Fig. 10 illustrates the power consumption at different temperatures when the supply voltage is 1 V. The circuit's power consumption at room temperature is only 1.65 nW. As the temperature gradually increases, the overall power consumption of the circuit continues to increase due to the rising bias current.

Table I presents a performance comparison of low-power reference circuits reported in recent years. The comparison shows that the TC performance of Sub-BGR is generally better than that of CMOS VR, the latter is more power-efficient. Achieving stable TC performance in a wide temperature range at the nW level is challenging. This work achieves a wider temperature range of 180°C (-40 °C to 140 °C) with better TC performance compared to other works. Moreover, the start-up circuit allows for a faster start-up time in low-power applications. Additionally, this work achieves good LS and PSRR performance and has a favorable area.

V. CONCLUSION

In this paper, an ultra-low power subthreshold CMOS voltage reference with a self-biased circuit based on SDMT structure with temperature compensation has been proposed. Without the use of operational amplifiers and capacitors, the proposed voltage reference achieves a temperature coefficient of 2.79 ppm/°C in a wide temperature range of -40 °C~140 °C, using a standard 0.18-μm CMOS process. Post-simulation results demonstrate the circuit's ability to maintain a stable output voltage V_{REF}, even when supply voltage or temperature changes significantly. The proposed design features very low power consumption and supply voltage with advantages in terms of area. The circuit is well-suited for low-voltage and low-power IoT self-powered sensor applications.

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