A High-impedance 3-MOSFET Pseudo-resistor for Instrumentation Amplifiers of Biomedical Sensors

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***Abstract*—The pseudo-resistor (PR) is widely used in biomedical sensor applications. It has a large resistance within an acceptable die area. This paper proposes an improved MOS PR structure with large resistance value, wide operating voltage range, and high linearity. By introducing an nMOS transistor in the traditional back-to-back 2-pMOS structure, the resistance value of the PR in this design is effectively increased, especially under the condition of low voltage difference. The proposed 3-MOS structure was selected after a comparison of different PR connection topologies. Its performance in terms of linearity of response, symmetrical dynamic range, frequency behavior and simplicity of implementation is considered. Simulation results based on a standard 0.18 µm CMOS process show that the proposed 3-MOS PR provides a resistance of about 430 GΩ in the voltage range of ± 1 V. In the case of low voltage difference, the 3-MOS PR is improved by about 170 GΩ compared with the traditional PR. Finally, an AC-coupled instrumentation amplifier for bio-electrical signal acquisition is designed and simulated using the proposed 3-MOS PR, and a low-frequency corner of 0.48 Hz is achieved. The output time-domain electrocardiogram (ECG) signal verifies the feasibility of the 3-MOS PR.**

Keywords—AC-coupled instrumentation amplifier (ACIA), biomedical sensor, high resistance, pseudo-resistor (PR).

I. Introduction

The physiological information provided by low-frequency low-amplitude bio-potential signals is crucial for biomedicine [1]. Instrumentation amplifiers (IAs) for physiological signal acquisition are a crucial component of biomedical sensor systems [2]. It is well known that bioelectrical signals have a wide distribution in the frequency range below 1 Hz, so IA needs to achieve extremely low high-pass (HP) corner (e.g. typically 0.5 Hz for EEG signals). Fig. 1(a) shows the structure of an AC-coupled IA (ACIA) commonly used in bio-signal acquisition [3]. Its mid-band gain is determined by the ratio of the input capacitor C_{IN} to the feedback capacitor C_F, $Gain = C_{IN} / C_F$. The frequency response of ACIA is described in Fig. 1(b). The HP corner frequency F_{HP} can be expressed as (1).

$$F_{HP} = \frac{1}{2\pi \cdot R_F \cdot C_F} \tag{1}$$

where R_F is the resistance of PR. Due to the limitation of full-chip integration, on-chip capacitors need to consider a good balance between power consumption and noise. The size of the capacitor in the passive resistor-capacitor network cannot occupy too much chip area due to the limitation of full-chip integration. From the published works, it seems that their capacitance is generally in the order of several fF to tens of pF [4]. Using a PR with a large resistance value is an area-effective way to achieve an extremely low F_{HP} [5]. PR can create a very large RC time constants in the bio-potential signal acquisition system.

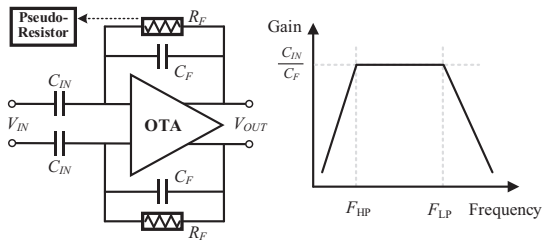

Fig. 1. (a) The structure of ACIA formed by PR. (b) Frequency response of ACIA. F_{LP} represents the low-pass corner frequency.

When transistors exhibit a given $V - I$ relationship with very high equivalent resistance while occupying a considerably smaller area than a physical resistor of equal value, this "devices" are called PR. They act as resistors from an electronic point of view and have been demonstrated their effectiveness in specific circuits. The switched capacitor resistors in [6] and the duty cycle modulated resistors in [7] can achieve large resistances while being immune to voltage swings. But the trade-off is that the capacitors and resistors occupy a large chip area and require additional clock generation circuitry. Voltage-controlled PR offers tunable resistance at the cost of additional biasing circuit which increases the complexity [8]. Operating in sub-threshold region, MOS-bipolar PR provides hundreds of GΩ resistance

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with negligible area consumption [9]. However, with the increasing of the differential voltage across the PR, the resistance drops quickly.

All these disadvantages motivated the research of alternative solutions for the design of high-value resistors. Through the detailed analysis of traditional PR at the device level, this paper optimizes the back-to-back 2-pMOS PR. One nMOS transistor was added between the back-to-back 2-pMOS PR to increase the resistance value at low voltage differences. The proposed 3-MOS PR features large resistance, wide operating range, and simple structure. The paper is organized as follows. Section II analyzes the characteristics of traditional single PR and symmetrical back-to-back PR. In Section III, the operating characteristics of the 3-MOS PR are described, and simulation results with different frequencies, temperatures and process corners are analyzed. Section IV shows the simulation results of the ACIA using the proposed PR based on a standard 0.18 µm CMOS process, and a typical electrocardiogram (ECG) signals is used for verification. Finally, the paper is concluded in Section V.

II. Analysis of Pseudo-Resistor Structures

A. Single MOS Pseudo-Resistor

The simple way to implement a high-resistance PR is to use a single MOS transistor. A pMOS with a lateral diode connection is shown in Fig. 2(a). To use this PR with relatively large bipolar signals, it is necessary to short-circuit the well and drain terminals. The current path is shown by the dashed line in the cross-section view of Fig. 2(b). The resulting device behaves as a MOSFET when $V_A > V_B > 0$ and as a diode when $0 < V_A < V_B$. When operating under $V_{BA} = V_B - V_A = 0$ V bias condition, the parasitic diode is off and the MOSFET is in the deep sub-threshold region.

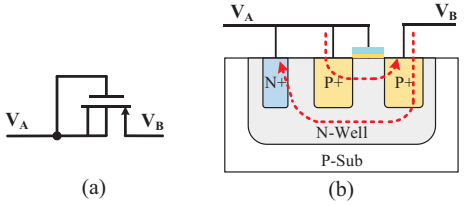

Fig. 2. (a) Single MOS PR: pMOS connected with gate–drain short-circuited. (b) Cross-section view of the PR.

In this condition, the current is inversely proportional to the length of the transistor. Consequently, the equivalent resistance can be evaluated by (2) for the sub-threshold current of the transistor [10].

$$I_{SD} = I_{SD0} \cdot \exp\left(\frac{V_{SG}}{nV_{\text{th}}}\right) \cdot \left[1 - \exp\left(-\frac{V_{SD}}{V_{\text{th}}}\right)\right] \tag{2}$$

where

$$I_{SD0} = 2n\mu C_{OX}\left(\frac{W}{L}\right)V_{th}^2 \cdot \exp\left(-\frac{|V_T|}{nV_{th}}\right) \tag{3}$$

where n is the sub-threshold slope, C_{OX} is the gate oxide capacitance per unit area, μ is the mobility of the carriers, $V_T = kT/q$ is the thermal voltage, (W/L) is the aspect ratio of the transistor, and V_{th} is its threshold voltage. The equivalent resistance of the PR around $V_{BA} = 0$ V is expressed by (4).

$$r_{eq0}\big|_{VAB=0} = \left(\frac{\partial I_{SD}}{\partial V_{SD}}\bigg|V_{SD}, V_{SG} = 0\right)^{-1} = \frac{V_{th}}{I_{SD0}} \tag{4}$$

Similarly, there is no conceptual difference in an nMOS as long as it is enclosed in its own floating p-well inside a DN-Well. Contrary to pMOS, when a small voltage is applied to the gate of nMOS, the resistance formed by the source-drain is very large. The $V - I$ characteristic curves of pMOS and nMOS with the same size are shown in Fig. 3. It is obvious that the diode-connected nMOS behaves as a MOSFET when $0 < V_A < V_B$. The states exhibited by the two types of devices are completely opposite. In other words, the impedance of nMOS is higher than that of pMOS when $V_{BA} > 0$.

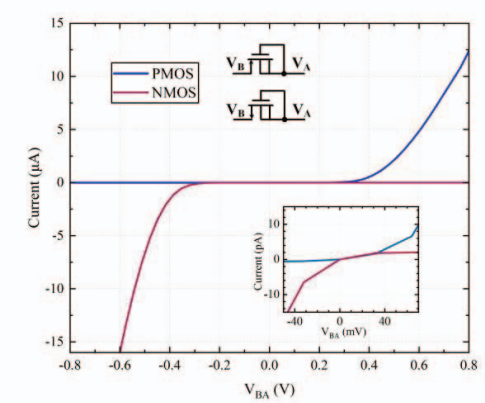

Fig. 3. The $V - I$ characteristic curves of diode-connected pMOS and nMOS with (W/L) = (1 µm/1 µm).

B. Symmetrical Back-to-Back 2-pMOS Pseudo-Resistors

Symmetrical PR has the same response to positive and negative currents, and suppresses even-order harmonics when stimulated by a sinusoidal signal near $V_{BA} = 0$ V. Under the same size and frequency, the resistance of back-to-back MOS PR is higher than that of back-to-back MOS bipolar PR [11]. The symmetrical structure implies that regardless of which terminal the signal enters from, the path of the current are similar. Fig. 4 illustrates the relationship between voltage V_{BA} and impedance of the symmetrical back-to-back PR. The perfectly symmetrical PR structure causes the symmetrical resistance values under ± V_{BA}. The simulation results show

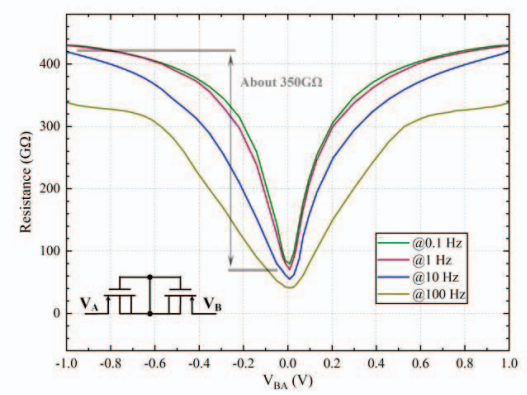

Fig. 4. The relationship between voltage and impedance of 2-pMOS PR at (W/L) = (1 µm/1 µm).

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that a resistance value of approximately 420 GΩ can be achieved within a dynamic range of 2 V, which is satisfactory for typical IAs. However, it is clear that the resistance value is significantly lower near V_{BA}= 0 V (about 70GΩ@1Hz). There is a resistance deviation of 350 GΩ at a frequency of 1 Hz, which severely impacts the linearity of the PR's response.

III. Proposed 3-MOS Pseudo-Resistor

To improve the linearity of the PR within a wide dynamic range, an nMOS was embedded into a back-to-back configuration of PR. The connection and cross-section of this 3-MOS structure are shown in Fig. 5. Considering that nMOS and pMOS exhibit opposite behaviors under the voltage V_{BA}, the nMOS does not form a conductive channel when the gate voltage is small. The gate of nMOS is connected to the substrate of two pMOS, meanwhile, the gates of the two pMOS are connected to the substrate of the nMOS. This can effectively improve the resistance value of the PR when the voltage between the two terminals is low. The addition of nMOS in the symmetrical structure has achieved high linearity while ensuring a sufficiently high resistance value. Fig. 6 depicts the $V - I$ characteristic curve of the 3-MOS PR at a small voltage difference for different sizes of nMOS. The current is proportional to the width of nMOS, which is consistent with the analysis in the Second II. The smaller the ratio of W/L causes the smaller current, and the larger resistance value of the 3-MOS PR.

Bio-electrical signals transmit information through the frequency and amplitude. In the ACIA, PR may be placed in the feedback loop to bias the input. The impedance is actually determined by the parallel connected DC resistance and the parasitic capacitance. Therefore, it is meaningful to investigate the frequency performance of PR. Fig. 7 shows the impedance of the 3-MOS PR at different frequencies. The results show that the impedance value of the proposed PR around V_{BA} = 0 V is significantly improved at each frequency. At a frequency of 1Hz, the minimum impedance value of 3-MOS PR is about 230 GΩ (about 160 GΩ higher than the traditional PR), and the fluctuation of the impedance value is approximately 200 GΩ (about 150 GΩ smaller than the traditional PR). Compared with the traditional back-to-back 2 pMOS PR, the proposed 3-MOS PR exhibits more stable resistance over a wide voltage swing range.

Fig. 8 presents the characteristics of the process and temperature corners of the proposed 3-MOS PR. Process corners named "tt", "ff" and "ss" are "typical", "fast-fast" and "slow-slow", which indicate the mobility of electron and hole carriers. As shown in Fig. 8, the slow corner at 0°C produces a higher impedance value of about 858 GΩ. Fast corner leads to lower impedance of PR at high temperature.

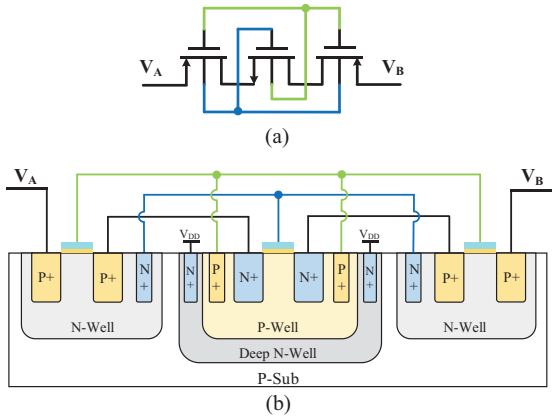

Fig. 5. (a) Circuit structure of the proposed 3-MOS PR. (b) Cross-sectional view of the 3-MOS PR.

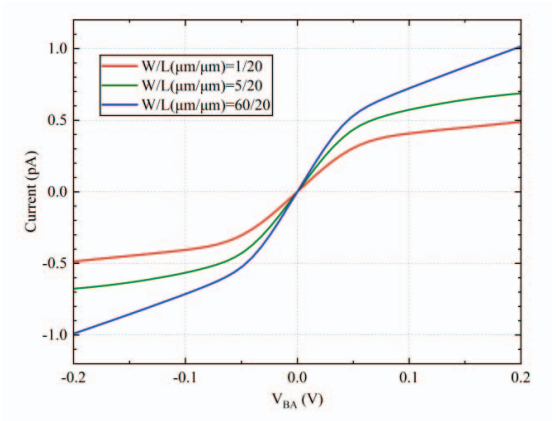

Fig. 6. The $V - I$ characteristic curves of the proposed 3-MOS PR with different sizes of nMOS.

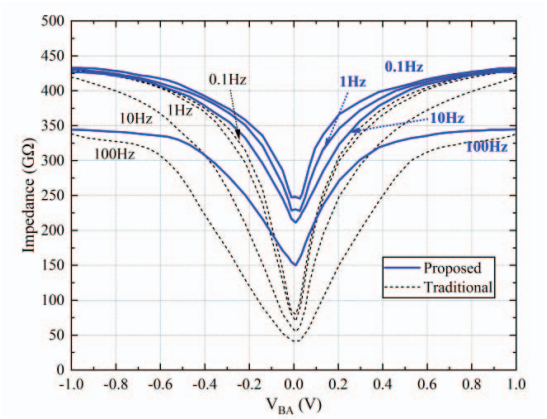

Fig. 7. Impedance–voltage relationship of the proposed PR at 0.1 Hz, 1 Hz, 10 Hz, and 100 Hz.

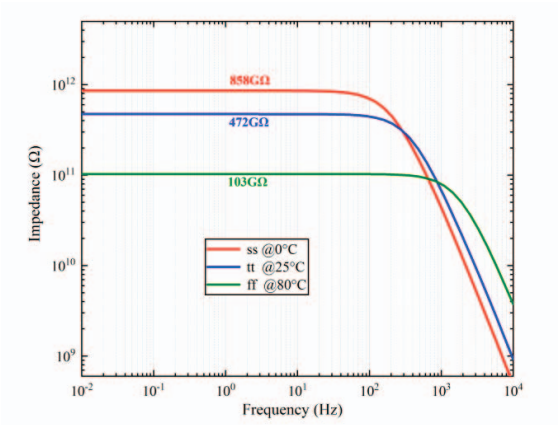

Fig. 8. Process and temperature corners of the proposed 3-MOS PR.

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IV. AC-coupled Instrumentation Amplifier

To verify the proposed 3-MOS PR, an AC-coupled IA is designed and simulated. Based on a standard 0.18 μm CMOS process, a two-stage operational transconductance amplifier (OTA), similar to the one depicted in [12], was employed. Considering the scenario of bioelectrical signal acquisition, the closed-loop gain of the IA is set to 40 dB. The value of C_{IN} is 200 pF, and the value of C_F is 2 pF. Fig. 9 shows the simulated bode plot of ACIA. Among them, the minimum high-pass cutoff frequency is 0.48 Hz. A very low HP corner frequency can be achieved in the IA through the proposed 3-MOS PR, which satisfies the requirement of acquiring low-frequency low-amplitude bio-electrical signals. In order to verify the feasibility of the designed 3-MOS PR, a standard time-domain ECG signal was input to the ACIA. Fig. 10 shows the simulation results of ACIA. The ECG input signals is amplified and the output clearly shows the P, T waves, and QRS complex.

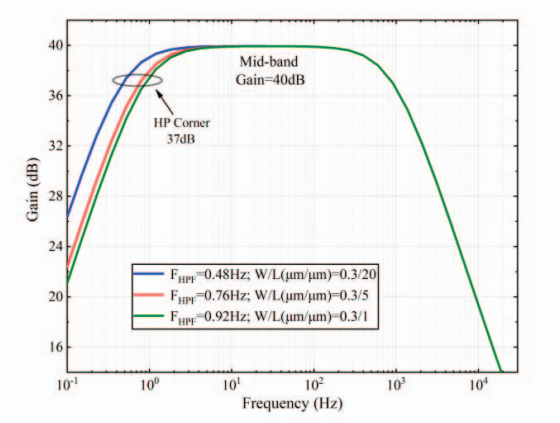

Fig. 9. Simulated bode plot of ACIA with 3-MOS PR.

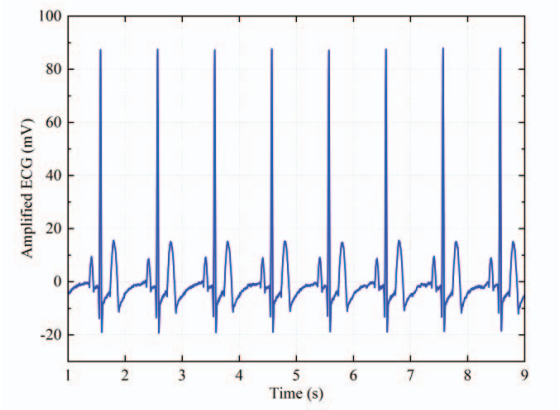

Fig. 10 Simulated ECG results with the addition of 3-MOS PR to the ACIA.

V. Conclusions

This paper discusses the detailed operation of single MOS PR and symmetrical back-to-back PR, and proposes a 3-MOS PR with improved linearity. Utilizing the complementary properties of nMOS and pMOS, the impedance value of the traditional 2-MOS PR at low voltage $|V_{BA}|$ is increased. According to the simulation results of a standard 0.18 μm process, the 3-MOS PR achieves a impedance range of 250–430 GΩ at 0.1 Hz, within the voltage swing range of 2 V. The simulations of process and temperature corners verify the high robustness of the proposed PR. The 3-MOS structure has advantages in linearity, frequency characteristics, simplicity of structure and chip area. An ACIA for bioelectrical signal acquisition validates the proposed 3-MOS PR structure. High-impedance PR are expected to be widely used in IC designs at a greater pace.

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