A 0.6V 10-bit 20kHz Capacitor Splitting Bypass Window SAR ADC for Biomedical Applications

Kangkang Sun
School of Electronics and Communication Engineering
Sun Yat-Sen University
Shenzhen, China
sunkk3@mail2.sysu.edu.cn

Feng Yan
School of Electronics and Communication Engineering
Sun Yat-Sen University
Shenzhen, China
yanf9@mail2.sysu.edu.cn

Huan Wu
School of Electronics and Communication Engineering
Sun Yat-Sen University
Shenzhen, China
wuhuan5@mail2.sysu.edu.cn

Jingjing Liu*
School of Electronics and Communication Engineering
Sun Yat-Sen University
Shenzhen, China
liujj77@mail.sysu.edu.cn

2023 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS) | 979-8-3503-8119-1/23/$31.00 ©2023 IEEE | DOI: 10.1109/APCCAS60141.2023.00065

***Abstract*—This paper proposes a fully differential 10-bit energy-efficient successive approximation register (SAR) analog-to-digital converter (ADC) that uses bypass window quantization technique based on multiple splits of the most significant bit (MSB) capacitor. Capacitor splitting of the digital-to-analog converter (DAC) is used to set up bypass windows. For signals within the bypass window range, some intermediate quantization are skipped to achieve lower power consumption and higher linearity. The proposed SAR ADC with bypass windows is designed using a standard 180nm CMOS technology. Simulation results show that the average power consumption of the capacitor array is only 72.08CV_{REF}^2. The differential nonlinearity (DNL) and integral nonlinearity (INL) are within 0.33 LSB and 0.25 LSB, respectively. With 0.6V supply and 20.83 kHz sampling rate, the effective number of bits (ENOB) of the ADC reaches 9.72 bits, and the figure of merit (FoM) is 2.56 fJ/conv.-step.**

Keywords—Analog-to-digital converter, successive approximation, capacitor splitting, bypass window, low power

I. INTRODUCTION

Successive approximation register analog-to-digital converters have significant advantages and potential in energy efficiency due to their unique quantization method and circuit structure. The internal digital structure can continue to benefit from the scaling of CMOS technology. The traditional binary search successive approximation quantization method must switch the voltage of the capacitor array according to a fixed procedure. For input signals within a certain range, there will be unnecessary conversion cycles, resulting in a large amount of power waste. This constitutes a design bottleneck for improving the energy efficiency of SAR ADCs.

The power consumption of SAR ADCs is mainly concentrated in three modules: DAC, comparator and digital logic circuit. For medium resolution SAR ADCs, capacitor switches with exponentially increasing accuracy consume most of the power [1]. Using appropriate capacitor arrays and flip strategies can greatly reduce the power consumption of ADCs. Therefore, many papers have proposed various quantization methods: monotonic [2], switching back [3], MCS [4] and Vcm-based [5]. To further reduce power consumption and avoid unnecessary conversion cycles, the concept of bypass switches is proposed [6]. However, this structure requires two additional comparators and an external reference voltage to implement bypass detection. These cause the problems such as the influence of window size on quantization accuracy, complex circuits and additional power consumption of bypass window detection logic. Jeong proposes a structure that adds dynamic trackable bypass windows based on physiological signal characteristics [7]. According to the different characteristics of human physiological signals, the range of window functions can be dynamically adjusted. When the signal exceeds the predefined window, the ADC switches back to full range mode to reacquire the signal. The window adjustment process wastes energy.

This paper proposes an efficient MSB capacitor splitting and bypass window SAR ADC structure. By introducing redundant bit unit capacitors in a monotonic manner, the total array capacitor value can be reduced from 2^{N-1} to 2^{N-2}, reducing the flipping power consumption by nearly half. At the same time, multiple capacitor splits are used. The quantization results during the capacitor flipping process are used to determine whether it is unnecessary capacitor switches that will be skipped, therefore improving the energy efficiency and linearity of the ADC.

This work is supported by National Science Foundation of China with project number 62174181.

II. ARCHITECTURE OF THE PROPOSED SAR ADC

Fig.1 shows the block diagram of the 10-bit capacitor splitting bypass window SAR ADC proposed in this paper. It consists of a pair of bootstrap sampling and hold switches, a differential capacitor array, a dynamic comparator and SAR control logic. Among them, the bootstrap sampling and hold switch uses the structure in [8], and the dynamic comparator uses the classic strong ARM latch structure [9].

A. Capacitor Splitting and Bypass Window

For a 10-bit DAC, the traditional DAC capacitor array splits the MSB capacitor to keep it consistent with the remaining capacitor array on the same side. This helps to realize the common centroid symmetry of the capacitor array layout and improve the matching. At the same time, the obtained 64C is split into two equal 32C capacitors. After splitting, the capacitor array has one more voltage switching cycle when participating in quantization. This cycle and the subsequent capacitor quantization results can be used to determine the bypass window.

The quantization process is divided into three stages: 1) quantization based on split capacitor; 2) quantization based on V_{CM}; 3) monotonic quantization. As shown in Fig. 2, during the sampling process, the input signal is connected to the top-plate of the capacitor array, i.e., $V_p=V_{in+}$, $V_n=V_{in-}$. At the same

2768-3516/23/$31.00 ©2023 IEEE
DOI 10.1109/APCCAS60141.2023.00065

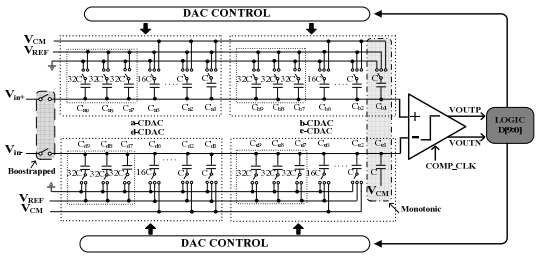


Fig.1. The proposed capacitor splitting bypass window SAR ADC architecture.

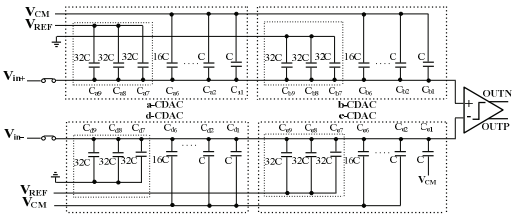


Fig.2. Illustration of capacitor array sampling.

time, the bottom-plates of the 32C capacitors of a-DAC and e-DAC, i.e., C_{a9}, C_{a8}, C_{a7}, C_{e9}, C_{e8}, and C_{e7}, are connected to V_{REF}, the bottom-plates of the 32C capacitors of b-DAC and d-DAC, i.e., C_{b9}, C_{b8}, C_{b7}, C_{d9}, C_{d8}, and C_{d7}, are connected to GND, and the other capacitors are connected to V_{CM}. The capacitor array quantization process is discussed below.

Compare the sampled V_p and V_n directly. If V_p>V_n, then D[9]=1, the bottom-plate of C_{a9} is changed to GND, and the bottom-plate of C_{d9} is changed to V_{REF}; otherwise, D[9]=0, the bottom-plate of C_{b9} is changed to V_{REF}, and the bottom-plate of C_{e9} is changed to GND. Then, perform the second voltage comparison. Since D[8] is quantized from 64C, i.e., "32C+32C" after flipping, the quantized value at this time cannot be exactly equal to D[8]. We define the quantized value of the first 32C as $D[8]_{1st}$ and the second 32C value as $D[8]_{2nd}$. Then $D[8]_{1st}$ and $D[8]_{2nd}$ jointly constitute D[8].

If D[9]=1 and $D[8]_{1st}$=0, it means that after the voltage switching of 32C, the polarity of V_p has changed. It can be determined that the range of V_p is [V_{CM}, 5V_{REF}/8]. Therefore, the voltage switching of C_{a8}, C_{a7}, C_{b8}, C_{b7}, C_{d8}, C_{d7}, C_{e8} and C_{e7} can be directly skipped. D[8] and D[7] are set to 0. Then, the voltage conversion of 16C is performed directly, i.e., C_{a6} and C_{b6} are connected to V_{REF}, and C_{d6} and C_{e6} are connected to GND. After that, the quantization is performed according to the normal SAR logic, as shown in the timing diagram (a) of Fig. 3. If D[9]=0 and $D[8]_{1st}$=1, it means that the range of V_p is [3V_{REF}/8, V_{CM}]. The voltage switching of C_{a8}, C_{a7}, C_{b8}, C_{b7}, C_{d8}, C_{d7}, C_{e8} and C_{e7} can be directly skipped. D[8] and D[7] are set to 1. Then, the voltage conversion of 16C is performed directly, i.e., C_{a6} and C_{b6} are connected to GND, and C_{d6} and C_{e6} are connected to V_{REF}. After that, the quantization is performed according to the normal SAR logic, as shown in the timing diagram (b).

If D[9]=1 and $D[8]_{1st}$=1, the voltage conversion of the second 32C in the capacitor array is performed, i.e., C_{a8} is connected to GND and C_{d8} is connected to V_{REF}. Then, voltage comparison is performed to obtain the third quantized value $D[8]_{2nd}$. If $D[8]_{2nd}$=0, it means that V_p just falls within [5V_{REF}/8, 6V_{REF}/8]. Therefore, the third 32C can be skipped and the voltage switching of the 16C in the array can be performed directly, i.e., C_{a6} and C_{b6} are connected to V_{REF}, C_{d6} and C_{e6} are connected to GND. At this time, D[8]=0 and D[7]=1. Then, the quantization is performed sequentially according to the SAR logic as shown in the timing diagram (c) of Fig. 3. If $D[8]_{2nd}$=1, the voltages are quantized sequentially according to the traditional SAR logic, where D[8]=1, as shown in the timing diagram (d).

If D[9]=0 and $D[8]_{1st}$=0, the second 32C capacitors C_{a7} and C_{b7} in the array are connected to V_{REF}, and C_{d7} and C_{e7} are connected to GND. Then, voltage comparison is performed to obtain the third quantized value $D[8]_{2nd}$. If $D[8]_{2nd}$=1, the third 32C can be skipped directly, C_{a6} and C_{b6} are connected to GND, C_{d6} and C_{e6} are connected to V_{REF}, where D[8]=1 and D[7]=0, as shown in the timing diagram (e). If $D[8]_{2nd}$=0, the voltages are quantized sequentially according to the traditional SAR logic, where D[8]=0, as shown in the timing diagram (f).

For the comparison result of the second least significant bit: If V_p>V_n, then D[1]=1, and the bottom-plate of C_{b1} is changed to GND. Otherwise, D[1]=0, and the bottom-plate of C_{b1} is changed to V_{REF}. Then, the magnitude of V_p and V_n is compared, i.e., D[0]. At this time, the entire quantization cycle is completed.

B. Switching Energy Analysis

For an N-bit capacitor array SAR ADC, if the probability of each bit occurrence during quantization is uniformly distributed, the average power consumption expressions of the monotonic switching scheme [2] and the Vcm-based switching scheme [5] during the quantization process can be deduced as (1) and (2) respectively.

$$E_{avg,mototonic} = \sum_{i=1}^{N-1}(2^{N-i-2})CV_{REF}^2 \tag{1}$$

$$E_{avg,Vcm-based} = \sum_{i=1}^{N-1}(2^{N-2i-2})(2^i-1)CV_{REF}^2 \tag{2}$$

When the input signal falls outside the bypass window voltage, the switching energy of the DAC can be expressed as:

$$E_{no,win} = \sum_{i=1}^{N-1}2^{N-2i-3}(2^i-1)CV_{REF}^2 - 2^{-N-1}CV_{REF}^2 \cdot \tag{3}$$

When the input signal falls within the first bypass window, the switching energy of the DAC can be expressed as:

$$E_{win1} = \sum_{i=2}^{N-1}2^{N-2i-3}(2^i-1)CV_{REF}^2 + (4-2^{-N-1})CV_{REF}^2 \cdot \tag{4}$$

When the input signal falls within the second bypass window, the switching energy of the DAC can be expressed as：

$$E_{win2} = \sum_{i=2}^{N-1}2^{N-2i-3}(2^i-1)CV_{REF}^2 + (2^{N-6}+2-2^{-N-1})CV_{REF}^2 \cdot \tag{5}$$

The simulation results of average switching energy with 10-bit resolution quantizer with different methods are shown in Fig. 4. It can be seen that due to the bypass window in the quantization of this structure, the average power consumption of proposed design is the lowest, that is only 72.08CV_{REF}^2.

C. Logic Control Circuit

For the proposed SAR ADC structure, the block diagram of logic control circuit is shown in Fig. 5. It mainly includes SAR logic circuit, bypass window control circuit and encoding

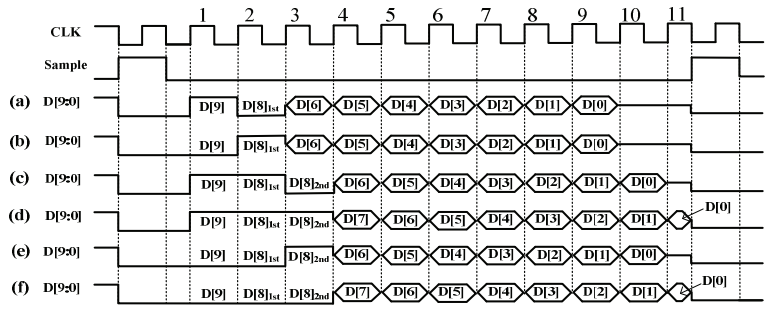


Fig.3. The timing diagrams of the proposed ADC during the quantization process

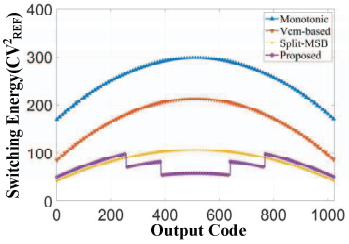


Fig.4. Simulation on average switching energy with 10-bit resolution.

module. The SAR logic circuit consists of 11 bit-slice (BS) modules [10]. The control signal "Valid" is obtained by the XOR logic of the comparator outputs "VOUTP" and "VOUTN". The inverted Sample signal works as EN9 to achieve the latching of each comparator output during the quantization process. Each BS module output sequentially enables next stage BS module.

The functions of the BS module are shown in Table I. Its internal circuit structure is shown in Fig. 6. The circuit is composed entirely of MOS transistors with a unit width-to-length ratio. Due to leakage current, the drain voltages of M1 and M2 may change from high level to low level during the entire SAR ADC conversion cycle, resulting in logic errors. In order to achieve correct logic functions of BS module under the three process corners (ff, tt and ss), M1 and M2 transistors use four-stacked NMOS with unit size to reduce leakage current effect.

D. Bypass Window Control Circuit

By the voltage of split capacitor before and after switching, the quantization results are used to determine whether the quantized signal is within the window. An XOR logic can be used here. If the XOR result of the two quantization logics is 1, it can be determined that the signal falls within the window voltage range. If the XOR result is 0, it means the input signal falls outside the window voltage range. Based on the working timing analysis in Section A, it is known that the main input variables of the first bypass window control module are: D[9], $D[8]_{1st}$ and $Q8_{1st}$. According to their logical relationship, the judgment module of the first bypass window can be obtained as shown in Fig. 7(a). Similarly, the input of the enable judgment module for the second window function should be $D[8]_{1st}$, $D[8]_{2nd}$ and $Q8_{2nd}$, and the output should be EN7. It has the same logical relationship as window 1.

The termination logic control circuit of the bypass window is located after the BS7 and before the BS6. Therefore, according to the logical relationship, the inputs of this module are D[9], $D[8]_{1st}$, $Q8_{1st}$, $D[8]_{2nd}$, $Q8_{2nd}$ and Q7. This means the

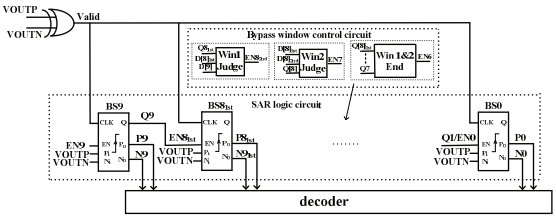


Fig.5. Block diagram of logic control circuit.

TABLE I. BS FUNCTION

Control signal	Function table
EN_i=0	P_o and N_o are cleared to 0, Q discharges to GND
EN_i=1	Valid pulls down to GND, P_o and N_o have outputs, and P_o=P_i, N_o=N_i, Q=VDD

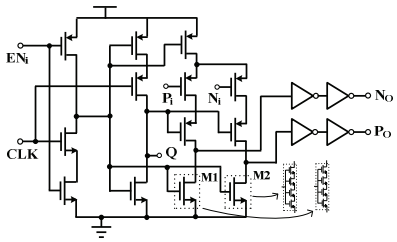


Fig.6. The schematic circuit of bit-slice module.

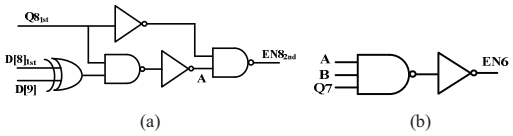


Fig.7. Bypass window control circuit, (a) Window 1 Judgement, (b) Window 1&2 End.

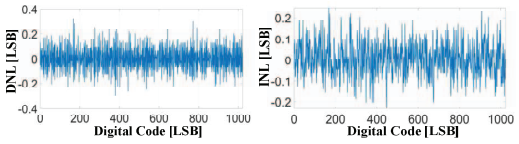
inputs are A, B (the signal at the same position as A in the window 2 Judgment module) and Q7. If any one of the three is 1, the BS6 can be enabled, that is, EN6=1. The circuit module of the bypass window termination is shown in Fig. 7(b). Due to the bypass window control circuit module being composed of only a few simple logic gate circuits, it has very low power consumption and high accuracy during the operation of the ADC.

III. SIMULATION RESULTS OF PROPOSED SAR ADC

The proposed 10-bit SAR ADC is designed based on a standard 180nm CMOS technology. Considering the power

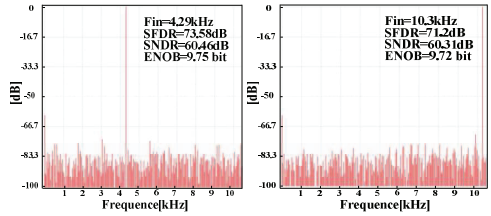
consumption of the quantizer, switching noise and the mismatch of unit capacitors, MIM capacitors with a value of about 19fF is selected as unit capacitor. By modeling in MATLAB, adding a 3σ = 10% mismatch error to the capacitance, the simulated DNL is +0.33/-0.3 LSB and INL is +0.25/-0.23 LSB. The output waveform is shown in Fig. 8.

The sampling rate of the SAR ADC with the MSB capacitor splitting and bypass window reaches 20.83kHz under a 0.6V power supply. Fig. 9 shows the 1024-point fast Fourier transform (FFT) curve of the transient ADC output simulated at the transistor level. At a sampling rate of 20.83kHz, when Fin is 4.2kHz and 10.23kHz, the ENOB of the SAR ADC is 9.75 bits and 9.72 bits respectively. The spurious free dynamic range (SFDR) is 73.58dB and 71.2dB respectively. The total power consumption is about 44.3nW. According to the FoM calculation formula defined by Power/(2^{ENOB}*fs), the FoM is about 2.56 fJ/Conv.-step. Fig. 10 shows the signal to noise distortion ratio (SNDR) and SFDR results within the Nyquist input range and there are no obvious changes. Fig. 11 shows the power consumption proportion of each module in the SAR ADC circuit at a working frequency of 20.83kHz. The CDAC module is the most power consuming. Table II lists the performance comparison results between the recently published bypass window SAR ADCs and the proposed work.



(a) (b)

Fig.8. Simulation results of (a) DNL, (b)INL with 3σ = 10% mismatch error.



(a) (b)

Fig.9. FFT spectrum at 20.83 kHz, (a) Fin is 4.2kHz, (b) Fin is 10.23kHz.

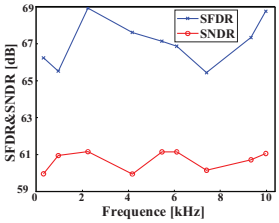


Fig.10. Dynamic performance versus Fin within the Nyquist input range.

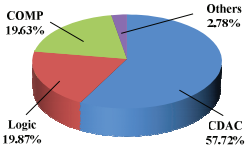


Fig.11. Power consumption ratio of each module in the proposed SAR ADC.

TABLE II. PERFORMANCE SUMMARY AND COMPARISON

Specification	TCAS-II 23[11]	MWSCAS 14[12]	TCAS-I 20[13]	JSSC 18[14]	This work
Process(nm)	180	65	180	180	180
Supply (V)	0.6	1.2	0.7	0.6	0.6
Bypass window	Yes	Yes	Yes	Yes	Yes
Fs (kHz)	50	150000	100	50	20
Resolution (bit)	12	10	12	10	10
ENOB (bit)	10.12	9.77	-	9.16	9.72
SFDR (dB)	82.4	82.8	80	68.7	71.2
Power (nW)	1540	1201000	1500	114	44.3
FoM (fJ/Conv.-step)	27.7	9.33	16.6	3.99	2.56

[a.] Results in this work and [12] are from simulation, while [11], [13]and [14] are measured.

IV. CONCLUSION

In this paper, a bypass window SAR ADC structure based on multiple splits of the MSB capacitor is proposed. By capacitor splitting and adding one more quantization cycle, two bypass windows are implemented. For signals located in the bypass window, some intermediate steps are skipped to achieve low power consumption and improve linearity. The proposed SAR ADC adopts 180nm CMOS technology. Under the condition of 0.6V power supply, it can achieve 10-bit accuracy of 20.83kHz. The prototype achieves 9.72 bits ENOB, 71.2dB SFDR in transistor-level simulations, and 2.56 fJ/Conv.-step FoM, which is very suitable as a data converter for low power medical electronic systems.

REFERENCES

[1] X. Tang et al., "Low-Power SAR ADC Design: Overview and Survey of State-of-the-Art Techniques," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 69, no. 6, pp. 2249-2262, June 2022.

[2] C. -C. Liu, S. -J. Chang, G. -Y. Huang and Y. -Z. Lin, "A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure," in IEEE Journal of Solid-State Circuits, vol. 45, no. 4, pp. 731-740, April 2010.

[3] G. -Y. Huang, S. -J. Chang, C. -C. Liu and Y. -Z. Lin, "10-bit 30-MS/s SAR ADC Using a Switchback Switching Method," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 21, no. 3, pp. 584-588, March 2013.

[4] Hariprasath V , Guerber J , Lee S H , et al. "Merged capacitor switching based SAR ADC with highest switching energy-efficiency," in Electronics Letters, vol. 46, no. 9, pp. 620-621, 2010.

[5] Y. Zhu et al., "A 10-bit 100-MS/s Reference-Free SAR ADC in 90 nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 45, no. 6, pp. 1111-1121, June 2010.

[6] G. -Y. Huang, S. -J. Chang, C. -C. Liu and Y. -Z. Lin, "A 1-μW 10-bit 200-kS/s SAR ADC With a Bypass Window for Biomedical Applications," in IEEE Journal of Solid-State Circuits, vol. 47, no. 11, pp. 2783-2795, Nov. 2012.

[7] S. Jeong et al., "A 120nW 8b sub-ranging SAR ADC with signal-dependent charge recycling for biomedical applications," 2015 Symposium on VLSI Circuits (VLSI Circuits), Kyoto, Japan, pp. C60-C61, 2015.

[8] M. Dessouky and A. Kaiser, "Rail-to-rail operation of very low voltage CMOS switched-capacitor circuits," 1999 IEEE International Symposium on Circuits and Systems (ISCAS), Orlando, FL, USA , pp. 144-147, 1999.

[9] B. Razavi, "The StrongARM Latch," in IEEE Solid-State Circuits Magazine, vol. 7, no. 2, pp. 12-17, Spring 2015.

[10] P. Harpe, G. Dolmans, K. Philips and H. de Groot, "A 0.7V 7-to-10bit 0-to-2MS/s flexible SAR ADC for ultra low-power wireless sensor nodes," 2012 Proceedings of the ESSCIRC (ESSCIRC), Bordeaux, France, pp. 373-376, 2012.

[11] Lee W E, Lin T H, "A 0.6-V 12-bit Set-and-Down SAR ADC With a DAC-Based Bypass Window Switching Method," in IEEE Transactions on Circuits and Systems II: Express Briefs, 2023.

[12] X. Wang, X. Zhou and Q. Li, "A energy-efficient high speed segmented prequantize and bypass DAC for SAR ADCs," 2014 IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS), College Station, TX, USA, pp. 97-100, 2014.

[13] Y. -H. Chung, Q. -F. Zeng and Y. -S. Lin, "A 12-bit SAR ADC With a DAC-Configurable Window Switching Scheme," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 2, pp. 358-368, Feb. 2020.

[14] T. -Y. Wang, H. -Y. Li, Z. -Y. Ma, Y. -J. Huang and S. -Y. Peng, "A Bypass-Switching SAR ADC With a Dynamic Proximity Comparator for Biomedical Applications," in IEEE Journal of Solid-State Circuits, vol. 53, no. 6, pp. 1743-1754, June 2018.