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CMOS EVEN HARMONIC SWITCHING MIXER FOR DIRECT CONVERSION RECEIVERS

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DC offset and high flicker noise are the main problems for the direct conversion CMOS mixer design. A novel even harmonic switching mixer implemented in a standard 0.18 μm CMOS process for applications in 2.45 GHz direct conversion receivers is proposed. The mixer circuit overcomes the problems of DC offset and high flicker noise. It achieves −8.24 dB gain, 5.2 dB DSB noise figure at 100 KHz, 17.25 dBm IIP3 and zero DC power consumption.

Keywords: Direct conversion; DC offset; switching mixer; even harmonic; flicker noise.

1. Introduction

The direct conversion techniques have increasingly gained more attention as a possible solution for the single-chip radio due to its low power, low complexity and easy integrating properties in recent years. However, a number of issues which do not exist or are not serious in the heterodyne architecture become important in the homodyne architecture, such as DC offset, flicker noise, I/Q mismatch, even order distortion and so on. Among these, the DC offset generated by LO self-mixing is the most critical. Approaches to remove the offset have so far mostly been focused on three methods. For modulation formats that have no or little spectral power at DC, AC coupling at the mixer output, or at some downstream stage, can be used to remove the offset.[1,2] This traditional method requires large capacitor values that are not realizable on-chip. The second common approach is the use of baseband analog and/or digital signal processing (DSP) techniques for offset estimation and cancellation.[3–5] It is a widely used method, but increases the complexity and cost of receivers. Another approach is to use a DC-offset-free mixing topology, such as harmonic mixers.[6–8] This technique gives a simple solution to solve DC offset, but less research has been done on it.

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In the direct conversion architecture, the down-converted spectrum is located around the zero frequency, so the flicker $(1/f)$ noise of the devices has a profound effect on the SNR, a severe problem in CMOS implementations.[9] The active mixers for direct conversion application implemented in the standard CMOS processes normally have a very high noise figure.[10] In order to achieve a good noise figure, BiCMOS processes are used with the disadvantage of high cost.[6,11] Reference 12 shows that using passive mixers is an effective method to reduce flicker noise in the CMOS technology. The switching mixer topology[13–15] is a very good passive mixer solution to solve the high noise figure. Unfortunately, not much attention has been paid to this solution.

In this paper, a novel CMOS even harmonic switching mixer with DC offset free and low noise figure is introduced. In Secs. 2 and 3, the topologies of an even harmonic mixer and a simple switching mixer are discussed, respectively. Then, Sec. 4 describes the design of the novel even harmonic switching mixer. Finally, Sec. 5 gives the conclusions.

2. An Even Harmonic Mixer

The block diagram of RF front-end using harmonic mixers for direct conversion receivers is shown in Fig. 1. Differential structures are used throughout the design to suppress common mode substrate noise and interference. Unlike the traditional architectures, the two sets of LO signals for the I and Q branches have 45° phase difference rather than 90° phase used in the standard structures.

The DC offset arises because the RF carrier and the LO signal operate at exactly the same frequency as shown in Fig. 2(a). First, the isolation between the LO port and the inputs of the mixer is not perfect, and a finite amount of feed-through, which is known as LO leakage, exists from the LO port to the mixer inputs. The leakage signal is reflected back at the outputs of LNA (ignoring the feed-through

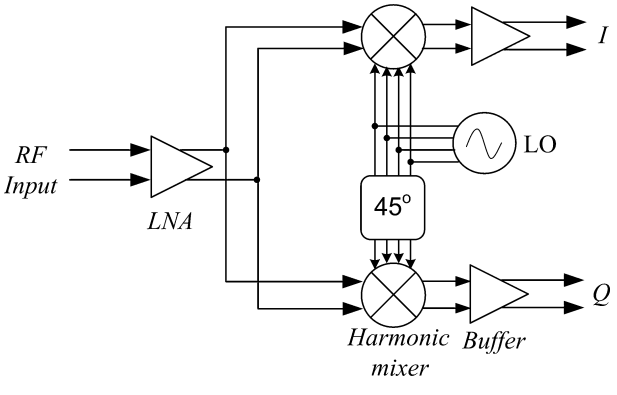

Fig. 1. Direct conversion front-end block diagram.

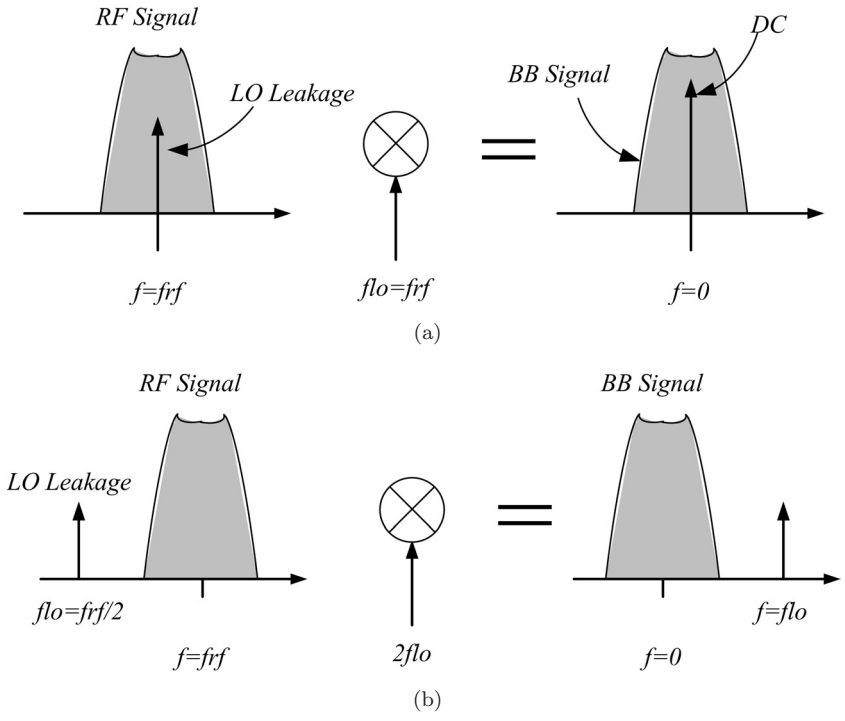

Fig. 2. Working principles of (a) the conventional mixer and (b) the harmonic mixer.

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from the LNA outputs to its inputs) and now mixed with the original LO signal, thus producing a DC component at the output of the mixer. For the harmonic mixing shown in Fig. 2(b), it is the second harmonic of the LO signal that takes part in the mixing process. As a result, the LO leakage does not generate a DC component but an output which is still situated at the LO frequency and can be easily filtered out.

Figure 3 shows the schematic of a bipolar or BiCMOS even harmonic mixer.[6] The quadrature LO signals are applied to the mixer at half the RF frequency. When operating with LO signals with large amplitude, the switching core ($Q3-Q10$) acts as a mixer. The resulting performance is that the circuit is mixing the RF signals with the one of twice the LO input frequency. For example, in the switching core ($Q3$–$Q6$), each transistor conducts only when the sinusoidal LO signal is close to the positive peak value. This makes the RF signal to be switched on every quarter cycle of the LO drive waveform, creating an effective $2f_{LO}$ signal.

Figure 4 shows the waveforms within the mixer driven by the quadrature LO inputs without the RF drive, to assist the reader in visualizing the generation of the doubled LO frequency internal to the mixer. The mixer design exploits the short off period of the devices in the switching core of the design. If the LO drive signals are ideal square waves, the switching core would have multiple transistors

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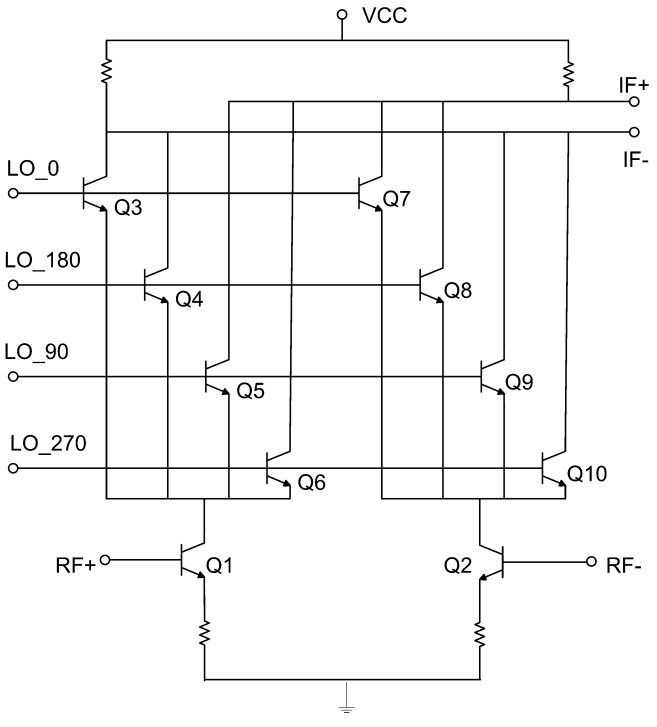

Fig. 3. Even harmonic mixer.

turn on simultaneously, resulting in no IF signal. Therefore, the performance is better when the LO signals become more triangular. But, the simulation result is almost identical when the mixer is driven by either a sinusoidal, or triangular sources. Figure 5 shows the effect of rise time as a function of LO pulse width on the conversion gain. Note that the conversion gain does not degrade by 3 dB until the rise time drops below one quarter of the pulse width. As the wave shape approaches a square wave, the conversion loss rises rapidly.

The characteristics of this even harmonic mixer are:

(i) The larger the LO power, the less the gain is. Because the LO power is larger, the wave shape is more like a square wave.
(ii) There is no DC offset caused by self-mixing of LO signals. It is suitable for direct conversion receiver.
(iii) It uses a bipolar or BiCMOS process. The fabrication cost is higher than that of the standard CMOS.

3. A Simple Switching Mixer

The switching mixer performs a multiplication between the RF signals and LO signals ideally represented by square waves switching between +1 and −1 (Fig. 6). It

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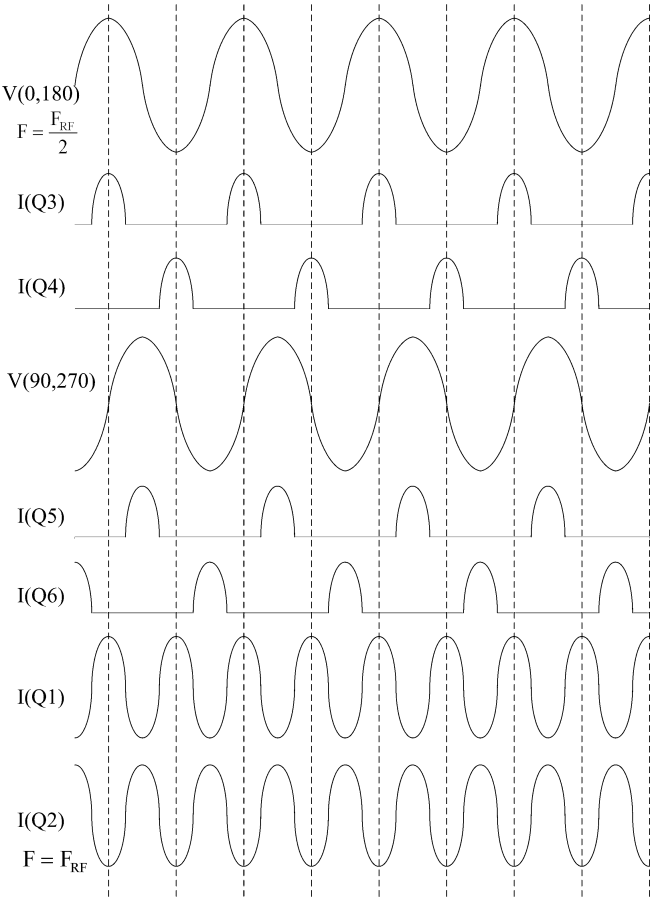

Fig. 4. LO waveforms.

has two bias voltages, $V_{\text{LO-DC}}$ and $V_{\text{IF-DC}}$ for LO input and IF output, respectively. The difference between $V_{\text{LO-DC}}$ and $V_{\text{IF-DC}}$ defines the gate–source bias voltage for the four transistors. If the gate–source bias voltage is exactly equal to the transistor threshold voltage V_{th}, the switching takes place precisely when the local oscillator output reaches the bias voltage. In this case, the mixer conversion gain is maximized.

The four identical transistors working in the triode region operate as switches. When the transistors are turned on, they are equivalent to resistors. The value is given by:

$$R_{\text{on}} = \frac{L}{\mu_n C_{\text{ox}} W[(V_{\text{gs}} - V_{\text{th}}) - V_{\text{ds}}]}, \tag{1}$$

where L is the gate length, μ_n is the average electron mobility in the channel, C_{ox} is the gate oxide capacitor per unit area, and W is the gate width. The theoretical

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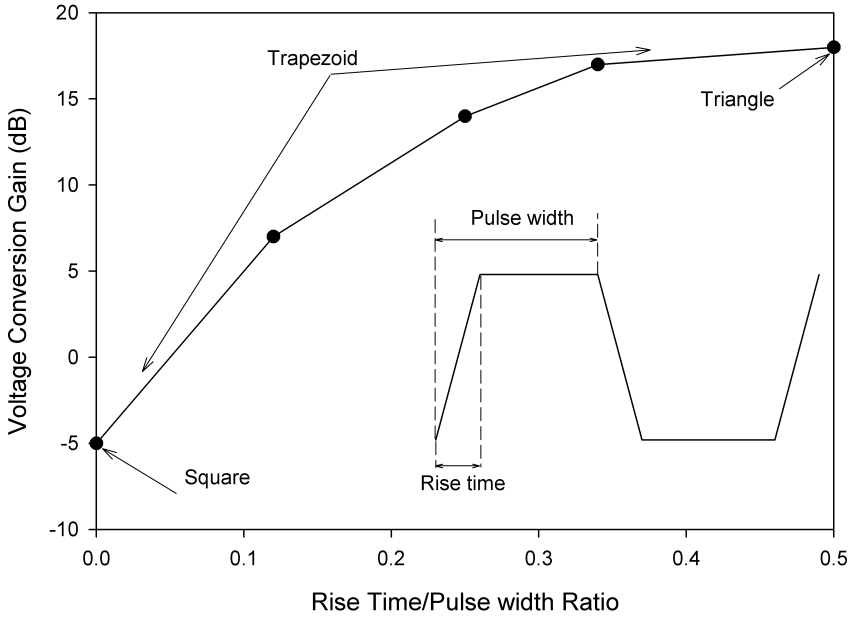

Fig. 5. Conversion gain versus LO wave shapes, rise time/pulse width ratio.

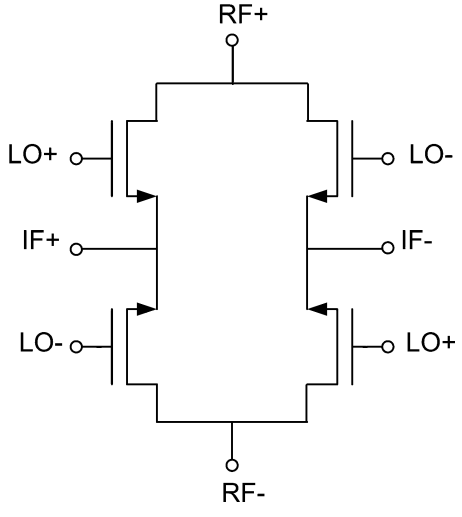

Fig. 6. Simple switching mixer.

optimum conversion gain for the simple switching mixer is equal to $2/\pi(-3.9\,\mathrm{dB})$ assuming that the LO signal at the gate is a square waveform and the turn-on resistance R_{on} is zero. When the LO power and gate width W are increased, the performance of the switching mixer is better. Because the larger sinusoidal

LO signal is closer to a square wave and the transistors behave more like ideal switches. Moreover, we can see from Eq. (1) that a large W gives a small turn-on resistance. Reference 10 shows that little effect on the conversion gain (loss) and noise figure is seen when the LO power and gate width are increased beyond certain values.

The distinct advantages of CMOS switching mixers are the zero power consumption and low noise figure. This is because MOS transistors can turn on without a bias current as long as $V_{\rm gs} > V_{\rm th}$. The bias current in the transistors is zero, leading to a low flicker noise. Another advantage is the inherent linearity of the switching mixer due to the good linearity of MOS devices operated in the triode region. But, this simple switching mixer will have DC offset problem due to LO self-mixing if it is used in the direct conversion receivers.

The characteristics of the switching mixer are:

(i) The larger LO power will give better performance parameters, such as higher conversion gain, lower NF, higher 1 dB compression point.
(ii) The larger device width W will give better performance parameters. However, these performance parameters cannot be improved further when W exceeds a certain value.
(iii) A lower NF and higher linearity than that of active CMOS mixers are obtained due to no bias current.

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4. Design of an Even Harmonic Switching Mixer

As explained in the previous sections, the switching mixer has a low NF due to no bias current. The even harmonic mixer has no DC offset due to the difference of the LO frequency and the RF frequency. If these two circuits are combined together, the characteristics of low NF and DC offset free could be obtained.

Figure 7 shows the schematic of the proposed even harmonic switching mixer without the biasing circuit for simplicity. The transistors $M1$–$M8$ working in the triode region operate as switches connecting either the input or the inverse of the input to the output terminal. The novel even harmonic switching mixer utilizes the method in Sec. 2 to create the effective twice LO switching frequency.

4.1. *Design of an even harmonic switching mixer*

The design parameters for the even harmonic switching mixer are the transistor channel width W and channel length L, the local oscillator amplitude $V_{\rm LO}$, and the DC bias voltages $V_{\rm LO\_bias}$ and $V_{\rm BB\_bias}$ for the LO input and baseband output, respectively. The difference between $V_{\rm LO\_bias}$ and $V_{\rm BB\_bias}$ defines the gate–source voltage $V_{\rm GS}$ for all the eight identical transistors. The baseband bias voltage $V_{\rm BB\_bias}$ should be chosen to ensure compatibility with subsequent stages. It has no influence on the performance of the mixer. The $V_{\rm GS}$ should be equal to the

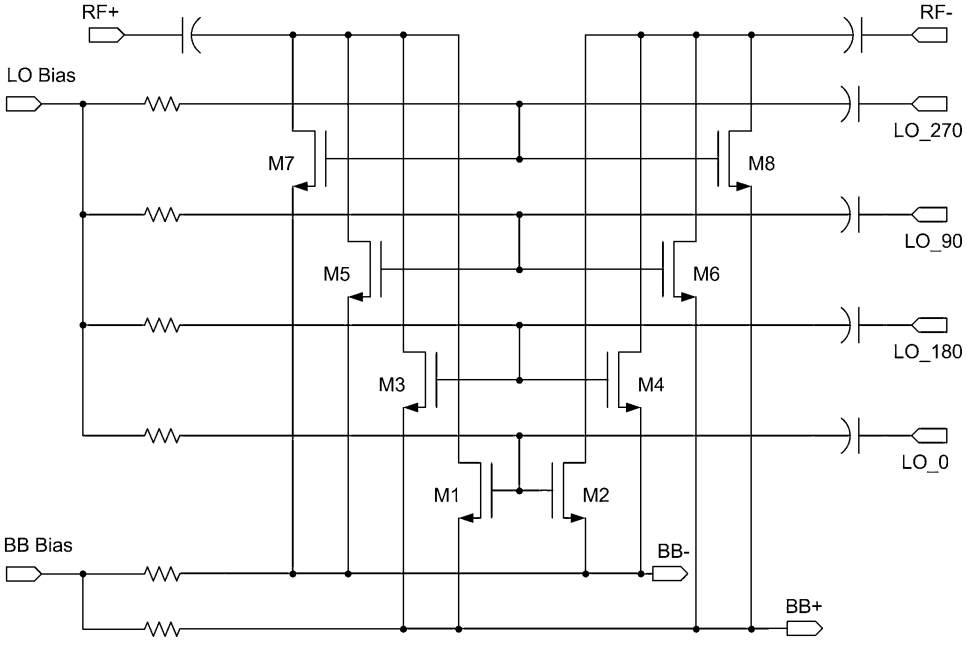

Fig. 7. Even harmonic switching mixer.

transistor threshold voltage V_{th}, and the switching takes place precisely when the local oscillator output reaches the bias voltage. Therefore, the performance is optimized when $V_{\text{LO\_bias}} = V_{\text{BB\_bias}} + V_{\text{th}}$.

Transistor dimensions and LO power are selected as the variables for the analysis and simulation of the mixer gain. Because the conversion gain is generally small for the switching type mixer, the optimization of the mixer gain becomes an important issue. The gate length is chosen to be $0.18\,\mu$m. It is found that the conversion gain first increases and then decreases while the transistor width is increasing, see Fig. 8. When $W < 70\,\mu$m, the characteristic of the mixer is dominated by the switching type. The transistors behave more like switches as transistor width is increased. When $W > 70\,\mu$m, the characteristic of the mixer is dominated by the even harmonic type. The transistors switch sharply, the conversion gain is small. So, the performance is optimized when $W = 70\,\mu$m.

The conversion gain is also dependent on the LO power. When the sinusoidal LO signal is increased, the transistors are closer to ideal switches and the gain increases according to the characteristic of the switching mixers. However, if the LO signal is closer to a square wave, the gain also tends to be reduced according to the mixing topology in Ref. 6. So, there is also a trade-off. Figure 9 shows the graph of the conversion gain versus LO amplitude (peak-to-peak). When the LO amplitude is 1.5 V, the slope of the curve is almost zero and the gain approaches the maximum.

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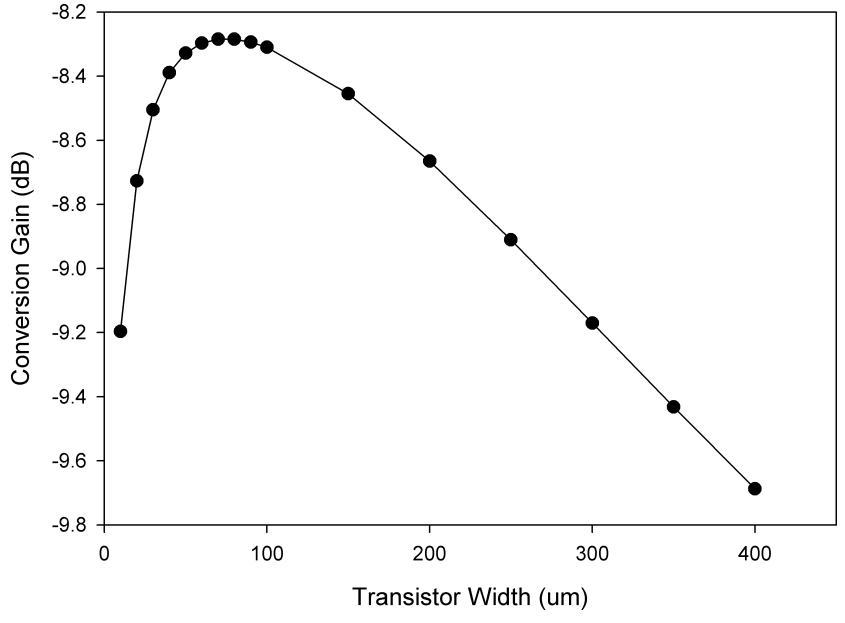

Fig. 8. Single end conversion gain versus transistor width.

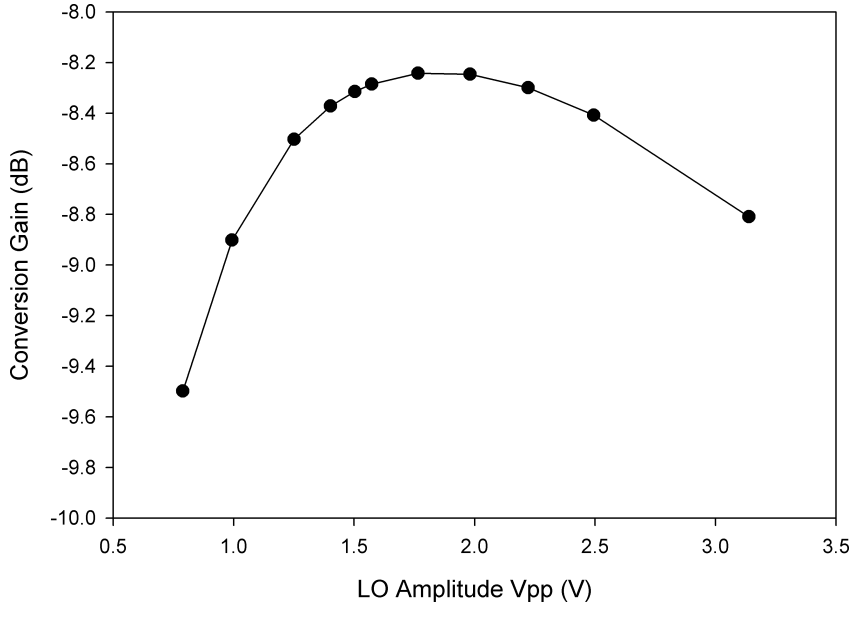

Fig. 9. Single end conversion gain versus LO amplitude (peak-to-peak).

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The circuit parameters setup are:

(i) The baseband bias voltage is chosen 0.6 V by considering the voltage level of subsequent stages. It can be changed to any value without affecting the performance.
(ii) The LO bias voltage is 1.19 V, then the gate–source bias voltage for the four transistors is $V_{GS} = V_{LO\_bias} - V_{BB\_bias} = 1.19 - 0.6 = 0.59 \geq V_{th} = 0.590\,V$.
(iii) The LO signal is set at 1.5 V and 1.225 GHz.
(iv) The RF signal is −40 dBm at 2.445 GHz for direct conversion application. After mixing with twice the LO frequency, the baseband output is at 5 MHz.
(v) Normal MOS is used. $L = 0.18\,\mu m, W = 70\,\mu m$.

4.2. *Results and comparison*

In this section, the simulation results of the designed even harmonic mixer are given. Then, a comparison of the performance is carried out between the designed circuit and the existing designs in the literature.

(i) Single end conversion gain = −8.24 dB; Fig. 10 shows the single end conversion gain. The crosshair marker *A* shows the RF input signal is −58.78 dBV at 2.445 GHz and the crosshair marker *B* shows the baseband output is −67.03 dBV at 5 MHz. As a result, the gain (conversion loss) is −8.24 dB.
(ii) 1 dB compression point = 7.10 dBm (Fig. 11).
(iii) IIP3 = 17.25 dBm (Fig. 12).
(iv) Noise figure = 5.21 dB at 100 KHz (Fig. 13).

A comparison of the performance is carried out between the four circuits. They are the proposed even harmonic switching mixer, the even harmonic mixers in

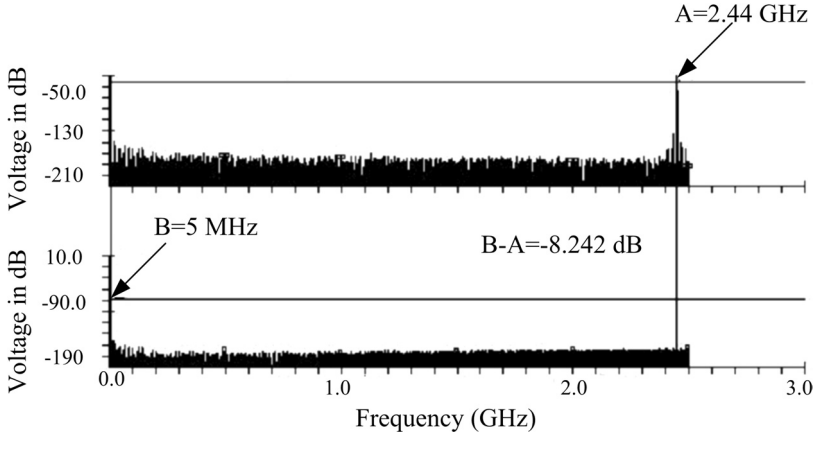

Fig. 10. Single end conversion gain.

Table 1. Performance comparisons.

	This work	Ref. 6	Ref. 7	Ref. 10
Technology	0.18 μm CMOS	0.35 μm BiCMOS	0.25 μm CMOS	0.25 μm CMOS
Mixer type	Harmonic switching	Harmonic Gilbert	Harmonic Gilbert	Switching
DC offset	No	No	No	Yes
Number of transistors	8	10	20	4
RF/LO freq. (GHz)	2.445/1.225	2.144/1.07	2.0122/1.006	2.105/2.1
Output freq. (MHz)	5	4	0.2	5
Supply current (mA)	0	4.6	1.71	0
LO V_{pp} (V)	1.5	0.5	—	1.0
Gain (dB)	−8.24	18.2	11.61	−6.1
DSB NF (dB)	5.2 at 100 KHz	8.0	12	5.6
IIP3 (dBm)	17.25	−6.6	−13.5	21

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Refs. 6 and 7, and the switching mixer in Ref. 10. The proposed circuit was constructed and simulated using Cadence SpectreRF. The performance parameters of the selected mixer circuits are shown in Table 1.

The proposed mixer has two transistors less, lower noise figure and higher IIP3 comparing to Ref. 6. Moreover, the DC power consumption is zero due to zero bias current. Another disadvantage of Ref. 6 is the higher cost of the BiCMOS technology. The even harmonic mixer in Ref. 7 is implemented in a 0.25 μm standard CMOS process. So, the noise figure is high due to the high flicker noise. Furthermore, there are 20 transistors in this double-balanced mixer. This increases the cost and complexity of the circuit. The switching mixer in Ref. 10 has the DC offset due to the LO self-mixing in direct conversion receivers. As shown, the proposed mixer has both the characteristics of even harmonic mixers and switching mixers. The DC offset problem is solved due to the even harmonic technique used. The low noise figure is caused by the zero bias current in the transistors. The conversion gain is

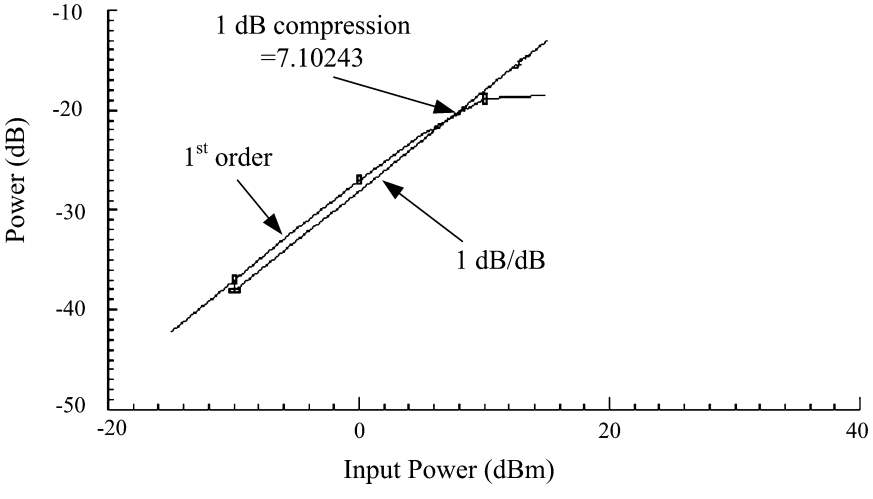

Fig. 11. 1 dB compression point.

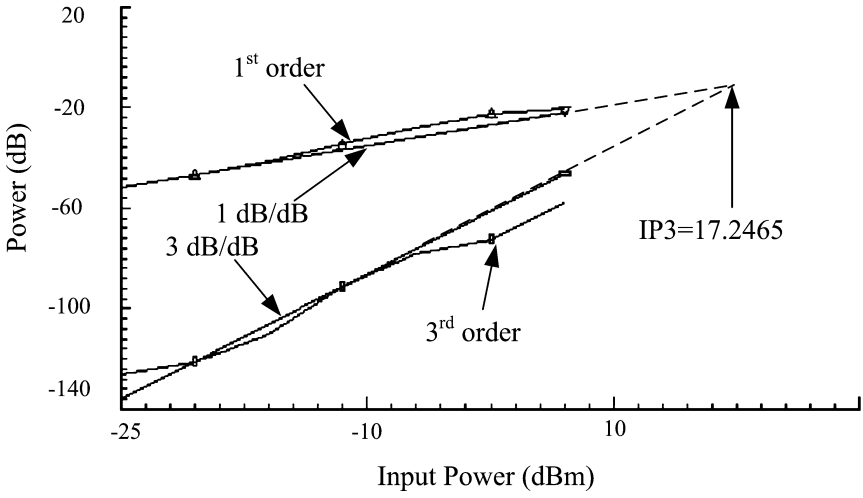

Fig. 12. IIP3.

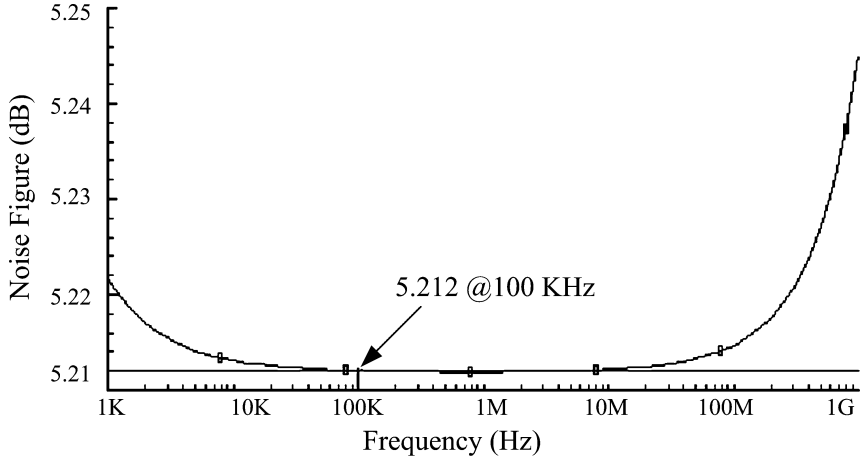

Fig. 13. Noise figure.

less than unity, but it is not critical and can be compensated by using a low noise amplifier (LNA) with a high gain in the direct conversion receivers.

5. Conclusion

In this paper, an even harmonic mixer and a simple switching mixer are discussed first. Due to the special mixing topology of the even harmonic mixer, there is no DC offset caused by self-mixing of LO signals. Moreover, higher LO power will cause

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a lower mixer gain. The performance of the simple switching mixer is better when transistor width is increasing and LO power is higher. However, it has DC offset if used in direct conversion receivers.

A novel even harmonic switching mixer with DC offset free and low noise figure, especially for the direct conversion application, is proposed. The characteristic of the even harmonic mixer gives a zero DC offset. The low noise figure and high linearity are due to the switching type of the mixer. Switching type mixers need the transistors to switch sharply to obtain good performance. However, to create the effective twice LO frequency here requires the transistors to turn on slowly. Therefore, appropriate design parameters are chosen to optimize the circuit. The proposed mixer is actually a combination of the even harmonic mixer and the switching mixer. It attains a better performance than that of the above mixers. Moreover, this even harmonic switching mixer is simple and easy to design.

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