An Optically Powered, Free Space Optical Communications Receiver

Jingjing Liu, Grahame E. Faulkner, Steve Collins, Dominic C. O'Brien and Steve J. Elston
Department of Engineering Science
University of Oxford
Oxford OX1 3PJ
jingjing.liu@eng.ox.ac.uk

***Abstract*—Two of the key components of sensor motes are a power source and a communications receiver. One approach to creating very small motes is to use free space optical communication and to scavenge power from the optical downlink. In this paper photodiodes are described that were made on a standard CMOS process and generate electrical power from the downlink beam. These photodiodes can be used to power the optical receiver that converts the modulation on the downlink to a bit stream.**

I. INTRODUCTION

It has been predicted that in the future wireless sensor networks may become ubiquitous with billions of autonomous low-power nodes networked together [1]. The smallest type of node that has been proposed for these networks are small disposable sensor motes sometimes referred to as 'smart dust' [2]. Typically, these motes should be smaller than 1mm on a side and scavenge power from the environment. One challenge created by these constraints is to create an efficient communications system. Larger network nodes typically rely upon RF communications. However, the isotropic gains of small antennas mean that these systems are effectively broadcast systems that require a relatively large power budget.

A potential alternative to RF communications is free space optical communications. Optical communications for wireless sensor networks that combine passive and active data transmission within each node have been developed [2]. Although the active data transmission incorporated in these devices avoids the need for a line-of-sight to the base station it significantly increases the power consumption and cost of each node .

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For applications in which a line-of-sight is available simpler nodes can be used that scavenge power and use passive communications between the node and the base station [3]. Two key components of the system are the photodiode that is needed to scavenge power and the optical receiver to detect the modulation of an optical downlink from a base station. In section II the characteristics of a power scavenging diode are presented. This is followed in section III by a description of a receiver circuit. The performance of this circuit is described in section IV. Section V is concluding remarks.

II. POWER DIODE RESPONSE

The system concept is that a base station sits above a coverage area in which smart dust motes are located. The base station uses a liquid crystal spatial light modulator to display a hologram that steers light to the desired position within the area. The resulting beam of light illuminates individual motes. Each mote is designed to scavenge power from the beam, decode information that is modulated onto the beam and communicate with the base station by modulating a retro-reflected beam. The preferred wavelengths for the communications link are near infra-red wavelengths that are invisible but detectable with a silicon photodiode and the smart dust has therefore been tested at 830nm. A model of optical system in the proposed base station design shows that the power density in its output beam varies with both range and angle. At this wavelength the model predicts that the optical power density will vary from 600μW/mm^2 at two metres from the base station to 0.45μW/mm^2 at thirty metres.

The first important function of the mote is to convert the optical power of the beam into electrical power. This can be achieved using a photodiode. When a photodiode is used as a power source only a fraction of the photo-generated current I_{ph} will flow through the load. If the current through the load

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is I_L, then the difference between these two currents (I_{ph} - I_L) is balanced by a forward bias current flowing from P type to N type inside the diode. The forward bias voltage is the voltage across the loaded photodiode. This means that for a load current I_L the voltage across the photodiode $V_{photodiode}$ is

$$V_{photodiode} = V_T \ln\left(\frac{I_{ph} - I_L}{I_T} + 1\right),$$

where V_T is thermal voltage and I_T is saturation current. The maximum voltage that can be generated by a single photodiode is limited, but the available voltage can be increased by connecting photodiodes in series.

To allow two diodes to be connected in series in the same silicon substrate smart dust circuits have been manufactured using the UMC 0.25µm 1P5M Mixed CMOS process that is available from the Europractice IC Service. In this triple well process a deep N-well, known as the T-well, is formed below a P-well so that it can be isolated from the substrate. Using this process an optical power scavenging circuit has been manufactured by connecting a Pwell/Twell junction in series with an Nwell/Psub junction.

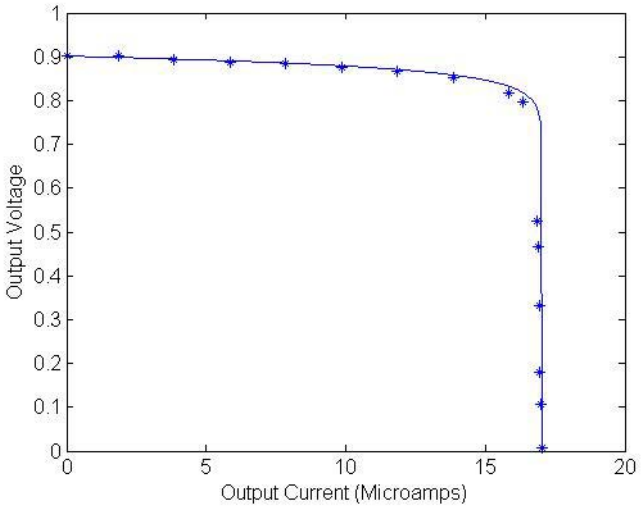

Figure 1. The load line for the series connected photodiodes showing 16 data points compared to the expected behaviour.

The load lines of the two series connected diodes have been measured using a source-measure unit of an Agilent 4155B as a programmable current sink. Figure 1 shows the relationship between the current flowing through the load and the voltage across the load when the input optical power is 252 µW. These results show that at this input power the open circuit voltage of the diodes is 0.9V. As expected the output voltage changes slowly until the output current becomes similar to the photocurrent, which in this case is approximately 17 µA. At this point the output voltage collapses to zero. The result is a maximum power operating point, when the voltage is 0.79V and the current is 16.5 µA.

As expected results such as those in Figure 2 show that the open circuit voltage is proportional to the logarithm of the optical power. In particular since the power voltage is generated using two diodes operated in series the open circuit voltage increases by approximately 115mV when optical power increases by an order of magnitude. As the results in Figure 2 show this means that the maximum available power voltage ranges from 0.9V to 0.5V over the important range of optical input powers. The aim is to develop circuits that operate correctly when the voltage available to power them varies over this range.

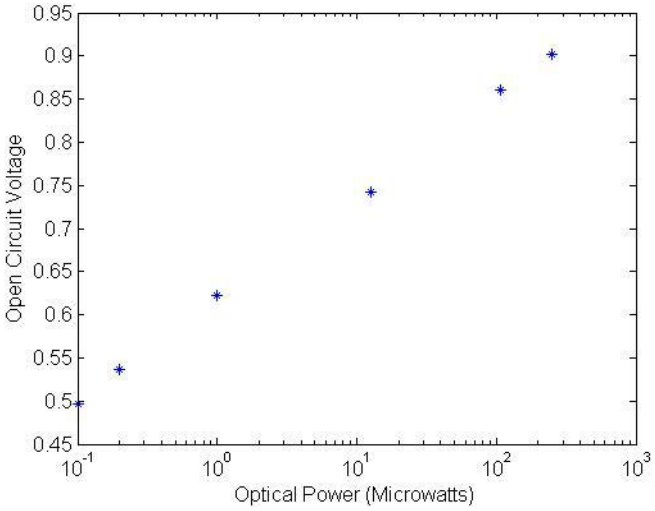

Figure 2. The open circuit voltage as a function of the optical power falling in the detector.

III. The Receiver Circuit

Data will be transmitted from a base-station to the mote by modulating the downlink beam. A second key component of the smart dust mote is an optical receiver to convert this modulation on the downlink into a bit stream. The receiver that has been designed is formed from two parts, a detector and a comparator.

One of the challenges when designing the receiver is to accommodate the large variation of the optical signal strength from the base station. This will cause a change in the absolute optical signal of three or more orders of magnitude. The one characteristic of the optical signal from the base station that will be independent of range is that the modulation is a known fraction or percentage of the optical power. Since this is the only constant, the most reliable detectors are those asynchronous detectors whose output signal depends only upon the percentage modulation in the input signal.

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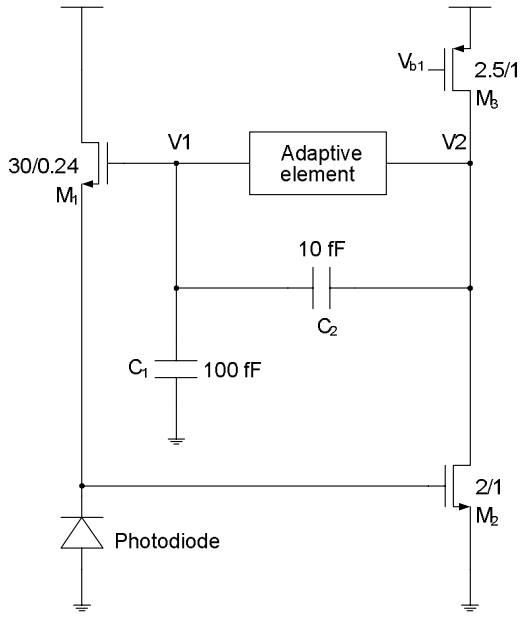

Figure 3 . A schematic circuit diagram of the detector circuit showing the width and length of each transistor

A detector circuit that has been used to perform this function is shown in Figures 3 and 4. The circuit in Figure 3 is based upon a design previously described by Delbrück and Mead [4]. However, to improve the temporal response of the circuit the compact single MOSFET adaptive element used previously has been replaced by the transconductor shown in Figure 4, which together with capacitances that load its output forms a low-pass filter.

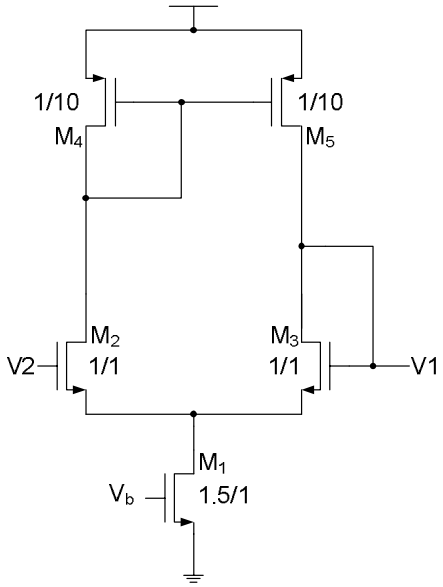

Figure 4. A schematic circuit diagram of the adaptive element that has been used.

The adaptive behaviour of the detector means that it responds to changes in the photocurrent. This means that the detector is unable to respond correctly to a conventionally encoded digital signal that might contain long runs of ones or zeros. To avoid this problem Manchester encoding can be used. In a Manchester or Phase code each bit of data is represented by a transition rather than a level. The transitions that represent data occur in the middle of each bit period and depending upon the data stream there may also be a transition at the beginning of each period. This means that the maximum time between transitions is one period.

The output from the detector is an analogue signal. The amplitude of the AC component of this analogue signal depends upon the percentage modulation depth of the input. This is therefore constant. However, the DC component of this signal depends upon the average optical input power. To recover the digital bit stream from this analogue signal the instantaneous analogue voltage must be compared to its DC component. The DC component is available within the detector circuit at the gate of the load transistor, i.e. M_1 in Figure 3. A comparator is therefore required with one of its inputs connected to the detector output and the other one connected to the gate of this device.

The UMC process provides two kinds of transistors. One is the normal transistor; the other is a transistor with a thicker gate oxide and higher threshold voltage. Transistors M_1 – M_4, in Figure 5, have this higher threshold voltage in order to reduce the current flowing through this circuit and therefore the power consumption.

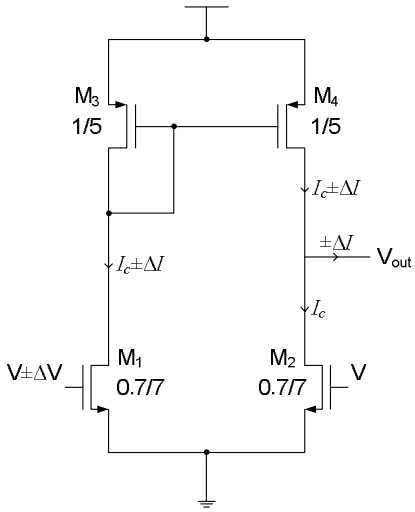

Figure 5. A schematic circuit diagram of the comparator circuit.

In addition to limiting the power consumption the other key design criterion for the comparator is to ensure that its offset voltage is smaller than the AC component of the input signal. The information provided by UMC suggests that a standard deviation of the offset voltage of less than 5mV can be achieved in the gate area $5\mu m^2$ of both types of devices in the comparator. To limit the power consumption of the circuit the input devices should be relatively long and thin.

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The output from the comparator circuit forms the input to two inverters that are connected in series to create a rail-to-rail digital output.

IV. Experimental Results

The fully integrated receiver circuit will drive a load formed by the gate capacitance of another MOSFET which is smaller than the capacitance of a bond-pad. To test the receiver under typical loading conditions a source-follower buffer was included between the output of the receiver and the bond-pad.

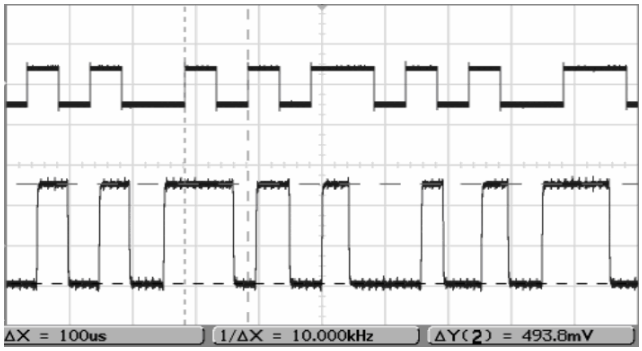

Figure 6. Typical successful results from a correctly decoded input signal at 10kbits/s. The top trace is the input and the bottom trace is the delayed and inverted output.

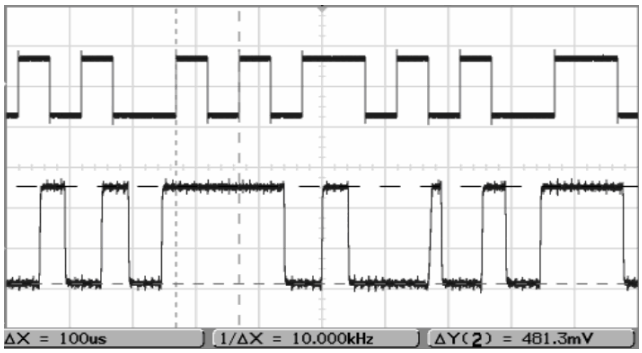

Figure 7 . Typical results that show the failure to detect one of the input bits, the one between the two cursors, when the power voltage is 0.5V and the data rate is 10kbits/s.

As expected the performance of the system depends upon the voltage available from the power diodes. When the optical power density is 336 nW/mm^2, the voltage available from the power diodes is 0.52V and at this power supply voltage the circuit consumes 6nA. Figure 6 shows the receiver operating successfully at a data rate of 10kbits/s and a modulation depth of 20%. Under these conditions the receiver continues to work up to 11kbits/s, however at higher frequencies the comparator current is too small to drive its load capacitance reliably. At frequencies less than 3kbits/s the low pass filter in the adaptive detector circuit attenuates the amplitude of the detectors output. As a result, at this optical power density the receiver works correctly for data rates between 3 kbits/s and 11 kbits/s.

When the power density reduces below this level the voltage available to power the receiver also reduces. When this voltage is 0.5V, results such as those in Figure 7, show that occasionally a transition is missed and a bit error occurs. These errors occur because the average input voltage to the comparator depends upon the optical power density. This means that as the optical power density decreases the current flowing through the comparator also decreases and eventually a point is reached at which this current is too small to drive the inverters that load the comparator.

V. Conclusions

In the future wireless sensor networks may become ubiquitous. Many larger nodes will incorporate RF communications. However, this is inefficient for the smaller disposable sensor motes sometimes referred to as ‘smart dust’. An alternative for these systems is optical free space communications. Two components of smart dust with optical free space communications have been designed and tested. The first component is photodiode that scavenged power from the downlink. The maximum voltage available from these devices varies from 0.9V to 0.5V as the optical power density changes.

A receiver circuit has been tested which can be powered by these diodes. Using Manchester encoded data it is possible to detect a signal with a modulation depth of 20% at frequencies between 3kbits/s and 11kbits/s at all power voltages greater than 0.52V. This voltage corresponds to an estimated range between the base station and the mote of 30m. Once the base station is completed, this predicted performance will be tested.

Acknowledgment

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