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A 0.7-V 7.4-nW 6.4-ppm/°C CMOS Subthreshold Voltage Reference With Temperature Compensation Circuit

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ABSTRACT

This paper proposes a nanowatt voltage reference (VR) with temperature coefficient compensation. All transistors work in the subthreshold region. The complementary-to-absolute-temperature (CTAT) voltage and proportional-to-absolute-temperature (PTAT) voltage are mainly generated by two NMOS transistors with different threshold voltages. At the same time, a simple temperature compensation circuit is designed to optimize the temperature coefficient at high temperatures, so that the proposed VR circuit can generate a reference voltage with a wider temperature range and a lower temperature coefficient. The proposed VR circuit is implemented using a standard 0.18-μm CMOS process with an active area of only 0.022 mm^2. The postlayout simulation results show that the proposed VR circuit generates a reference voltage of 308.21 mV at room temperature. Its temperature coefficient is 6.4 ppm/°C over a temperature range of −40°C°C–140°C, with a power consumption of 7.4 nW. The voltage line sensitivity (LS) is 0.098%/V, and the power supply ripple rejection (PSRR) is −72 dB @DC and −42 dB @10 MHz.

1 | Introduction

Nowadays, the technology of the Internet of Things (IoTs) is developing rapidly. This has led to an increasing demand for low-power, long-lasting devices. The IoT sensors develop towards small size, low voltage, and low power, or even self-powered by scavenging energy from the environment. The reference circuit, as one of the most important circuits in integrated circuit systems, plays a crucial role in sensor circuits. To meet the requirements of IoT sensor circuits, a voltage reference (VR) circuit with a stable voltage independent of process, power supply voltage, and temperature (PVT) is required under the condition of low working voltage and low power consumption.

Traditional bandgap reference (BGR) has certain advantages in performance and stability. A voltage mode sub-1 V bandgap VR achieves a relatively low temperature coefficient (TC) while consuming 7.5 μW [1]. However, when considering the power consumption performance, the power consumption of the BGR is very high. A MOS-only ultra-low-power reference circuit has been presented [2]. To save chip area and power consumption, a high-slope PTAT voltage generator is developed to minimize the number of PTAT stages required to compensate for the CTAT voltage. However, it is still limited in terms of temperature performance. The reference circuits using OPA operating in the subthreshold region could generate a reference voltage that exhibits good PVT stability [3–9]. This serves as a promising solution for low-power reference circuits, yet the power consumption in the mentioned studies using OPA can be further reduced. A self-biased temperature-compensated CMOS VR operating at picowatt-level power consumption is presented [10].

Similarly, a self-biased reference circuit based on the stacked diode-connected MOS transistor structure without amplifiers

and start-up circuits is proposed [11]. Many self-biased VR circuits are introduced [12–15]. The design of the self-biased circuit significantly reduces the power consumption of the reference circuit. However, self-biased reference circuits often lack temperature performance. Through a triode-regulated structure, a femto-watt VR is obtained [15]. However, the ultra-low power consumption results in the susceptibility of this reference voltage to temperature and process variations. Another extensively explored approach is the subthreshold bandgap reference (sub-BGR) circuit utilizing subthreshold transistors and BJTs [16–20]. A second-order temperature compensation method is proposed, achieving a TC of 19 ppm/°C for the output voltage at a power consumption of 30 nW [16]. Sub-BGR offers good temperature performance and power supply rejection ratio (PSRR). However, limited by the base–emitter voltage of the bipolar junction transistors, sub-BGR cannot achieve ultra-low power consumption. In addition, the new BGR using switch capacitor technology has good accuracy [21], but its power consumption can still be further optimized.

To solve some of the problems mentioned above, this work proposes a CMOS subthreshold VR circuit using a temperature compensation circuit, without BJTs and resistors. This work utilizes operational amplifiers operating in the subthreshold region and further reduces the TC of the circuit through a low-power temperature compensation scheme. The rest of the paper is organized as follows: Section 2 discusses the proposed design and working mechanism. Section 3 discusses the key design considerations of the proposed circuit. Section 4 describes the postlayout simulation results and the performance comparison of the proposed VR circuit with relevant research works. Finally, in Section 5, the main conclusions are presented.

2 | Operation Principles of the Proposed VR Circuit

The CMOS subthreshold VR circuit proposed in this work is shown in Figure 1. It includes a start-up circuit, a bias circuit, an OPA circuit, a VR core circuit, and a temperature compensation circuit. The low-TC of the circuit is mainly realized by the temperature compensation circuit, which adjusts the voltage deviation of the output voltage of the VR core circuit at high temperatures.

2.1 | Start-Up Circuit

The start-up circuit consists of M_{S1}, M_{S2}, and M_{S3} and can make the VR circuit deviate from the original zero bias point into the normal operation state, wherein M_{S1} acts as a capacitor [4]. MOS varactors are increasingly used in microelectronics as voltage-controlled capacitors [22]. After powering up the circuit, the start-up circuit initiates its operation.

The gate of M_{S2} charges continuously through the MOS capacitor, causing the gate voltage to gradually increase and allowing the channel of M_{S2} to gradually conduct. At this point, the drain voltage of M_{S2} is pulled down. This process leads the circuit to depart from the zero start-up point and gradually takes the MOS transistors to the biasing operating point required by the design. When the output VR is greater than the turn-on voltage of M_{S3}, the gate voltage of M_{S2} is pulled down and so the start-up circuit is turned off. A ramp voltage is used for power-up, with a power-up time set to 20 μs. The circuit's start-up process is depicted in Figure 2, showing the voltage changes at each node, and they are consistent with theoretical analysis.

2.2 | The Proposed VR Circuit

All transistors in the circuit are biased in the subthreshold region. The purpose is to reduce the power supply voltage and power consumption. Among them, M_{N8} and M_{N11} are thick-oxide NMOS, and the rest are thin-oxide transistors. The main part of the VR circuit can generate PTAT voltage and CTAT voltage for first-order TC compensation. When $V_{DS} \geq 3V_T$, the drain current of the MOSFET in the subthreshold region can be approximated as

$$I_D = \mu_n C_{OX} K(m-1) V_T^2 \exp\left(\frac{V_{GS} - V_{TH}}{mV_T}\right) \quad (1)$$

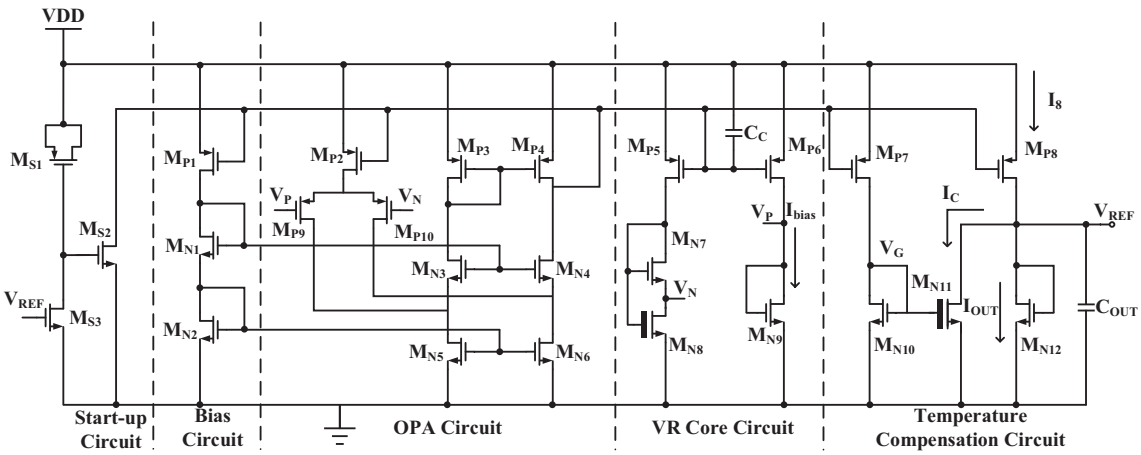

FIGURE 1 | The circuit diagram of the proposed CMOS subthreshold voltage reference.

where μ_n is the mobility of electrons, C_{OX} is the gate-oxide capacitance per unit area, V_{TH} is the threshold voltage of the transistor, K is the aspect ratio ($=W/L$) of the transistor, $V_T = k_B T/q$ is the thermal voltage, k_B is the Boltzmann constant, and T is absolute temperature, q is the elementary charge, and $m = 1+C_{OX}/C_d$ is the subthreshold slope factor, where C_d is the depletion capacitance per unit area. In the circuit, the bodies of all MOSFETs are connected to either ground or VDD. The influence of the body effect on the temperature performance analysis can be ignored [23]. In a simple analysis, it can be approximated that the C_{OX} and V_{TH} of the same type of NMOS transistors are equal. Assume that different types of NMOS transistors have the same subthreshold slope factor m (in the CMOS process used, m is 1.03 and 1.13 for thick-oxide NMOS transistors and thin-oxide NOMS transistors, respectively). Since the drain current of M_{N7} and M_{N8} are equal, $I_{DN7} = I_{DN8}$. There is a threshold voltage difference between M_{N7} and M_{N8}; the voltage V_N is as follows:

$$V_N = (V_{THN8} - V_{THN7}) + mV_T \ln\left(\frac{C_{OXN7}K_{N7}}{C_{OXN8}K_{N8}}\right) \quad (2)$$

It can be seen that V_N is independent of the branch current. Due to the use of NMOS transistors with different gate oxide thicknesses, it generates a threshold voltage difference ΔV_{TH}, which is a CTAT voltage. Due to the operational amplifier, voltage V_p is forced to be the same as V_N, so the bias current I_{bias} is as follows:

$$Ibias = \mu_n \frac{C_{OXN9}C_{OXN7}}{C_{OXN8}}\left(\frac{K_{N9}K_{N7}}{K_{N8}}\right)(m-1)V_T^2 \times \exp\left(\frac{V_{THN8} - V_{THN7} - V_{THN9}}{mV_T}\right) \quad (3)$$

The final output VR is generated by I_{OUT}, and $I_{OUT} = I_8 - I_C$, where I_8 is a copy of I_{bias} through the current mirror. I_C is the compensation current, which is used to compensate for the TC at high temperatures. The bias voltage V_G and I_C are as follows:

$$V_G = (V_{THN8} - V_{THN7}) + mV_T \ln\left(\frac{K_{P7}C_{OXN7}K_{N7}K^{N9}}{K_{P6}C_{OXN8}K_{N8}K^{N10}}\right) \quad (4)$$

$$I_C = \mu_n C_{OXN7}(m-1)\left(\frac{K_{N9}K_{N7}K_{P7}K_{N11}}{K_{N8}K_{N10}K_{P6}}\right)V_T^2 \exp\left(\frac{-V_{THN7}}{mV_T}\right) \quad (5)$$

It can be concluded that I_C is an increasing function of temperature. So, it mainly compensates for the high-temperature part of the VR output. Finally, the VR output voltage V_{REF} generated by I_{OUT} through the active load M_{N12} is as follows:

$$V_{REF} = V_{THN12} - V_{THN7} + mV_T \ln \left[\frac{K_{N7}K_{N9}}{K_{N8}K_{P6}K_{N12}} \times \left(\frac{C_{OXN7}K_{P8}}{C_{OXN8}}\exp\left(\frac{V_{THN8} - V_{THN9}}{mV_T}\right) - \frac{K_{P7}K_{N11}}{K_{N10}}\right)\right] \quad (6)$$

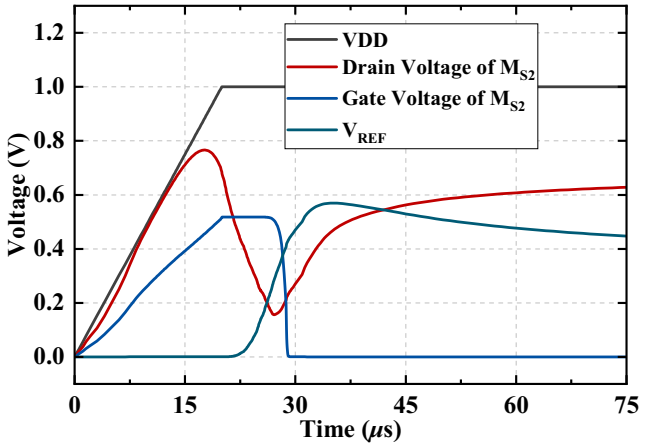

FIGURE 2 | The simulation results of the start-up process for the proposed VR circuit.

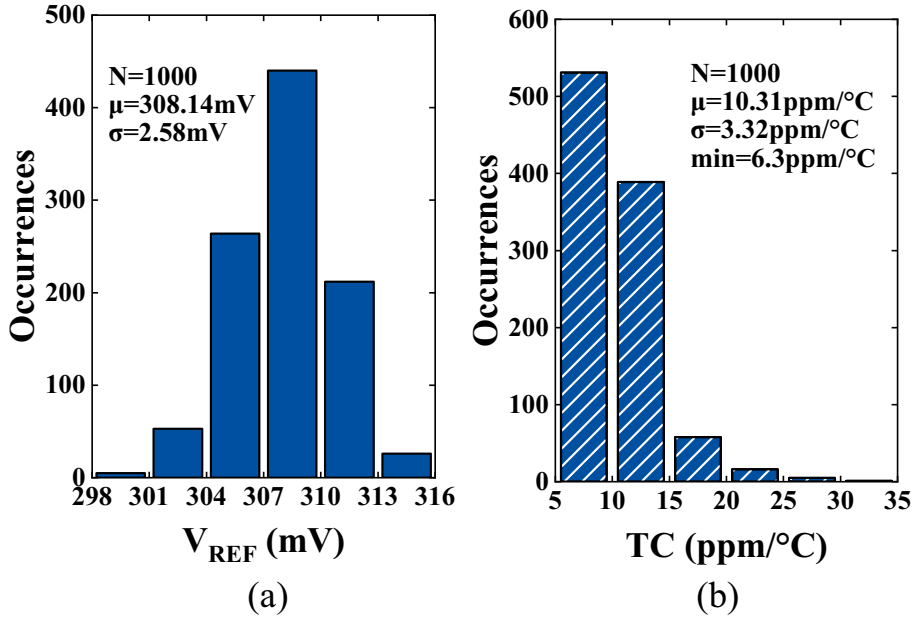

FIGURE 3 | The Monte Carlo simulation results of the proposed VR circuit. (A) V_{REF}, (B) TC-V_{REF}.

Let $A=\exp[(V_{THN8}\text{-}V_{THN9})/mV_T]$ and $B=K_{P7}K_{N11}/K_{N10}$. In (6), term A rapidly increases with decreasing temperature. This causes term A to be much larger than term B at low temperatures and so term B can be ignored. At the same time, M_{N9} and M_{N12} have the same aspect ratio. So V_{THN9} and V_{THN12} are equal. As a result, the approximate expression for V_{REF} at low temperatures can be simplified as (7).

$$V_{REF,low} = V_{THN8} - V_{THN7} + mV_T \ln\left[\frac{C_{OXN7}K_{N7}K_{N9}K_{P8}}{C_{OXN8}K_{N8}K_{P6}K_{N12}}\right] \quad (7)$$

It can be seen that the proposed V_{REF} has a similar format as (2) at low temperatures, and the first-order TC can be optimized by adjusting the aspect ratio of the MOSFETs in (7). When the circuit works in a high-temperature range, V_{REF} is no longer dominated by the first-order TC. As the temperature rises, term A decreases significantly, and term B can no longer be ignored. The temperature compensation circuit acts as a current sink at high temperatures. Therefore, the TC of the VR output is reduced, and the VR circuit operating temperature range is also increased. At the same time, the power consumption of the entire circuit is also determined by each transistor's size, so the optimal size of each transistor is a balance between performance and power.

3 | Design Considerations of the Proposed VR Circuit

3.1 | Process and Mismatch Variations

The stacked diode-connected MOS transistor structure (M_{N7} and M_{N8}) used in the proposed circuit has a reduced slope of TC so that it can extend the operational temperature range. Meanwhile, this stacked diode-connected MOS transistor structure utilizes the difference in threshold voltages as the CTAT voltage, ensuring that the circuit's voltage output has a good process tolerance. Figure 3 shows the Monte Carlo simulation results of the output VR. The Monte Carlo simulations in this work consider mismatch and process variations. Over 1000 runs, the average output VR is 308.14 mV, and its standard deviation is 2.58 mV. The average TC of the VR output is 10.31 ppm/°C, while its standard deviation is 3.32 ppm/°C. Its minimum TC is 6.3 ppm/°C.

Figure 4 shows the output voltage under different process corners. The simulated TCs are 6–50 ppm/°C from −40°C to 140°C among five different corners. At the same time, the output voltage at different process corners can remain stable under changes in the power supply voltage.

3.2 | Analysis of LS and PSRR

Both LS and PSRR are key performance parameters of VR circuits. In low-voltage and low-power applications, the operating bandwidth of transistors in the subthreshold region is low, resulting in poor PSRR performance and greater impact from power supply voltage disturbances. Therefore, the improvement of these parameters is particularly critical. The LS is used to evaluate the dependence of V_{REF} on the change of DC voltage.

$$LS = \frac{\Delta V_{REF}}{V_{REF} \cdot \Delta VDD} \times 100\% \quad (8)$$

where ΔVDD is the power supply voltage range in which the VR circuit can work normally and ΔV_{REF} is the corresponding output voltage variation range. It can be seen from (6) that the output voltage does not depend on the supply voltage. Equation (6) is a simplified expression for the output voltage, which neglects the differences in the subthreshold slope factor m for different types of NMOS transistors. Therefore, LS performance is still limited by the coupling of VDD to V_{REF}.

Figure 5 shows the equivalent small-signal model of the proposed VR circuit used for the PSRR analysis. R_8, R_9, R_{11}, R_{12} represent the equivalent resistance seen from the respective nodes.

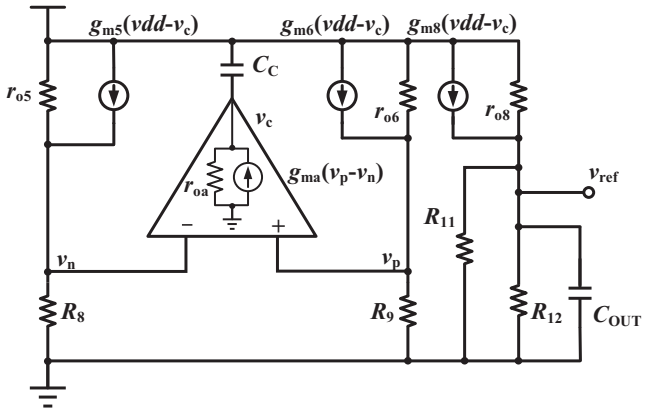

FIGURE 5 | The small-signal model of the proposed VR circuit for PSRR analysis.

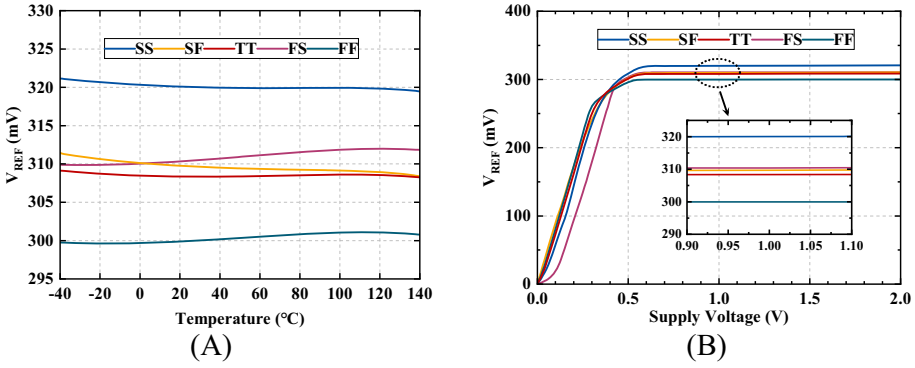

FIGURE 4 | The simulation results of the output voltage over different process corners with respect to (A) temperature and (B) supply voltage.

g_{ma} and r_{oa} are the equivalent transconductance and output resistance of the operational amplifier, respectively. C_C is the compensation capacitance between node C and *vdd*. g_{m5}, g_{m6}, g_{m8}, r_{o5}, r_{o6}, and r_{o8} are the transconductance and output impedance of M_{P5}, M_{P6}, M_{P8}, respectively. R represents the equivalent resistance of the parallel connection of M_{N11} and M_{N12}. C_{OUT} is the output capacitance at the V_{REF} output VR node. The simplified PSRR expression and its dominant poles and zero are shown in (9–11). The poles at the OPA input nodes are ignored.

$$\frac{v_{ref}}{vdd} = \frac{\frac{1}{(r_{o8}+R)}R\left(1+g_{m8}r_{o8}\right)}{\left(1+g_{ma}r_{oa}\left(g_{m6}R_B - g_{m5}R_A\right)\right)} \frac{\left(1+s/z_1\right)}{\left(1+s/p_1\right)\left(1+s/p_2\right)} \tag{9}$$

$$R_B = R_9 // r_{o6},\quad R_A = R_8 // r_{o5},\quad R = R_{11} // R_{12} \tag{10}$$

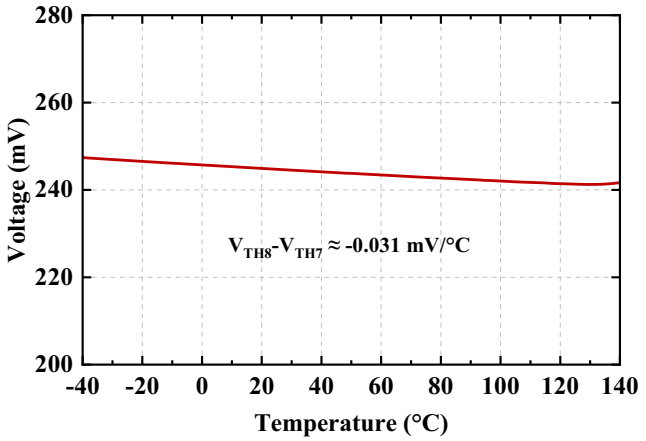

FIGURE 6 | The simulation result of the threshold difference between V_{TH8} and V_{TH7}.

TABLE 1 | The design parameters of the proposed VR circuit.

Components	W/L (μm/μm)	Components	W/L (μm/μm)
M_{S1}	4×5/5	M_{N2}	2/10
M_{S2}	4/20	M_{N3}	6/8
M_{S3}	10/20	M_{N4}	6/8
M_{P1}	1/20	M_{N5}	4×2/10
M_{P2}	4×1/20	M_{N6}	4×2/10
M_{P3}	2/8	M_{N7}	4×9/20
M_{P4}	2/8	M_{N8}	2/19
M_{P5}	2×1/20	M_{N9}	1/20
M_{P6}	8×1/20	M_{N10}	1/20
M_{P7}	4×1/20	M_{N11}	2×7/20
M_{P8}	8×1/20	M_{N12}	1/20
M_{P9}	2×4/4	C_C	3×24/24
M_{P10}	2×4/4	C_{OUT}	8×24/24
M_{N1}	4/10		

$$z_1 = \frac{1+g_{m8}r_{o8}}{r_{oa}C_c}, p_1 = \frac{1}{C_{OUT}\left(r_{o8} \| R\right)}, p_2 = \frac{\left(g_{m6}R_B - g_{m5}R_A\right)}{C_c/g_{ma}} \tag{11}$$

To enhance PSRR, it is recommended to increase the value of z_1 and decrease p_1. According to the analysis derived from (9–11), C_C should be reduced, while C_{OUT} should be increased to improve PSRR. In practical circuit design, maintaining stability requires a sufficiently large C_C. Therefore, efforts should be made to minimize C_C while ensuring the circuit stability. Simultaneously, considering the on-chip capacitor's impact on area consumption, C_{OUT} cannot be excessively large. Consequently, achieving a balance between the values of C_C and C_{OUT} is crucial for optimizing the PSRR performance, stability, and on-chip area utilization. In the proposed design, C_C is approximately 1.7 pF and C_{OUT} is approximately 4.5 pF.

3.3 | Proposed Sizing for Temperature Compensation

From (7), the PTAT voltage, which is used to compensate for the first-order coefficient of CTAT, depends on K_{N7}, K_{N8}, K_{N9}, K_{N12}, K_{P6}, and K_{P8} parameters. The current I_C shown in (5) is

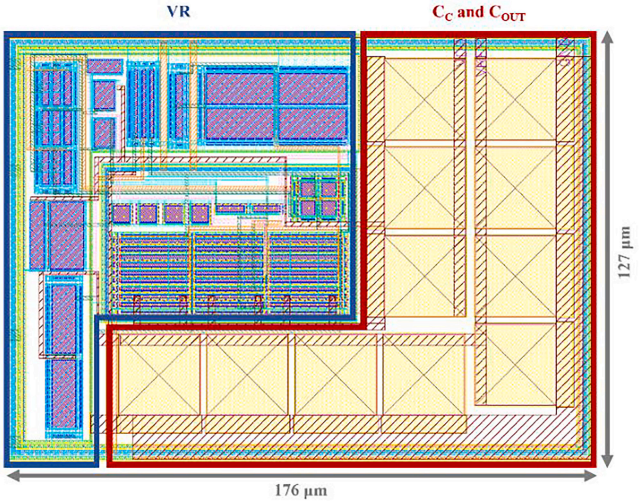

FIGURE 7 | The layout of the proposed voltage reference circuit.

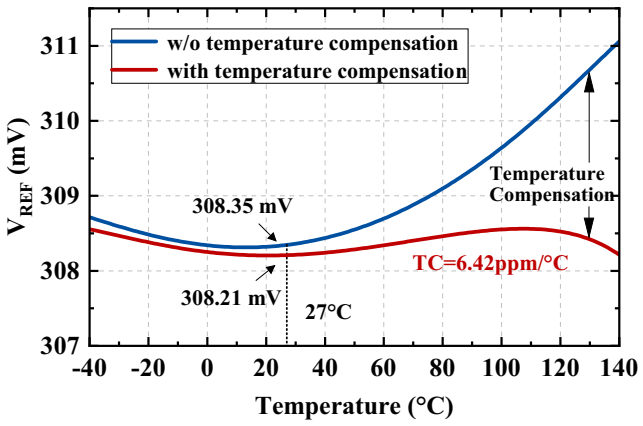

FIGURE 8 | Comparison of the simulated V_{REF} with and without the proposed temperature compensation circuit.

used to compensate for the high-TC of the circuit, which is determined by K_{N7}, K_{N8}, K_{N9}, K_{P6}, K_{P7}, K_{N10}, and K_{N11} parameters. The simulation result for V_{TH8}-V_{TH7} in (7) is illustrated in Figure 6, with its CTAT slope being −0.031 mV/°C. Based on the theoretical analysis, the design parameter is shown in Table 1.

4 | The Postlayout Simulation Results

The proposed VR circuit is implemented by all MOSFET and designed using a standard 0.18-μm CMOS process. Figure 7 shows the circuit layout, and it occupies an area of 0.022 mm^2, which includes output capacitor C_{OUT} and compensation capacitor C_C. The capacitors occupy a significant amount of silicon area, so it requires a balance between the area and capacitance value in the design. Figure 8 shows the postlayout simulation results of V_{REF} respect to the temperature with and without the proposed temperature compensation circuit. It can be seen that without the temperature compensation circuit, V_{REF} rises rapidly at high temperatures, limiting the circuit's temperature performance and operating temperature range. The TC is evaluated using the following expression [10]:

$$TC = \frac{V_{REF,MAX} - V_{REF,MIN}}{(T_{MAX} - T_{MIN})V_{REF,NOR}} \times 10^6 \quad (12)$$

where $V_{REF,\,NOR}$ represents the output voltage of the circuit at room temperature (27°C). The proposed VR circuit has an improved TC in the high temperature range, and the operating temperature range is −40°C°C–140°C. Due to the temperature compensation circuit, the TC of the proposed VR circuit is 6.42 ppm/°C. The output voltage of the proposed VR at room temperature is 308.21 mV.

Figure 9A shows the postlayout simulation results of the PSRR and it is −72 dB in the DC state, −37 dB at 100 Hz and −42 dB at 10 MHz. This is sufficient to suppress primary interference coupled from the power supply voltage to the output voltage. As in the theoretical analysis, the two poles and one zero are also marked in the figure. Figure 9B shows the postlayout simulation results of LS. When the power supply voltage reaches above 0.7 V, the circuit outputs a stable reference voltage. The LS of the proposed VR circuit is only 0.098%/V at room temperature within a power supply voltage range of 0.7 V to 2.2 V. Figure 9C presents the postlayout simulated start-up duration observed at a temperature of 27°C. Incorporating the straightforward start-up circuit, the system achieves a start-up time of roughly 1.3 ms. This marks a significant improvement, with the start-up time reduced by approximately 145 times when compared to the identical circuit without the start-up circuit. Figure 9D illustrates the postlayout simulated power consumption of the proposed circuit at different temperatures. The static power consumption of the circuit at room temperature is 7.35 nW. Due to the absence of temperature compensation in the current within the circuit, the power consumption increases with the rising temperature, demonstrating a positive correlation with temperature. At 120°C, the static power consumption of the circuit reaches 34.72 nW.

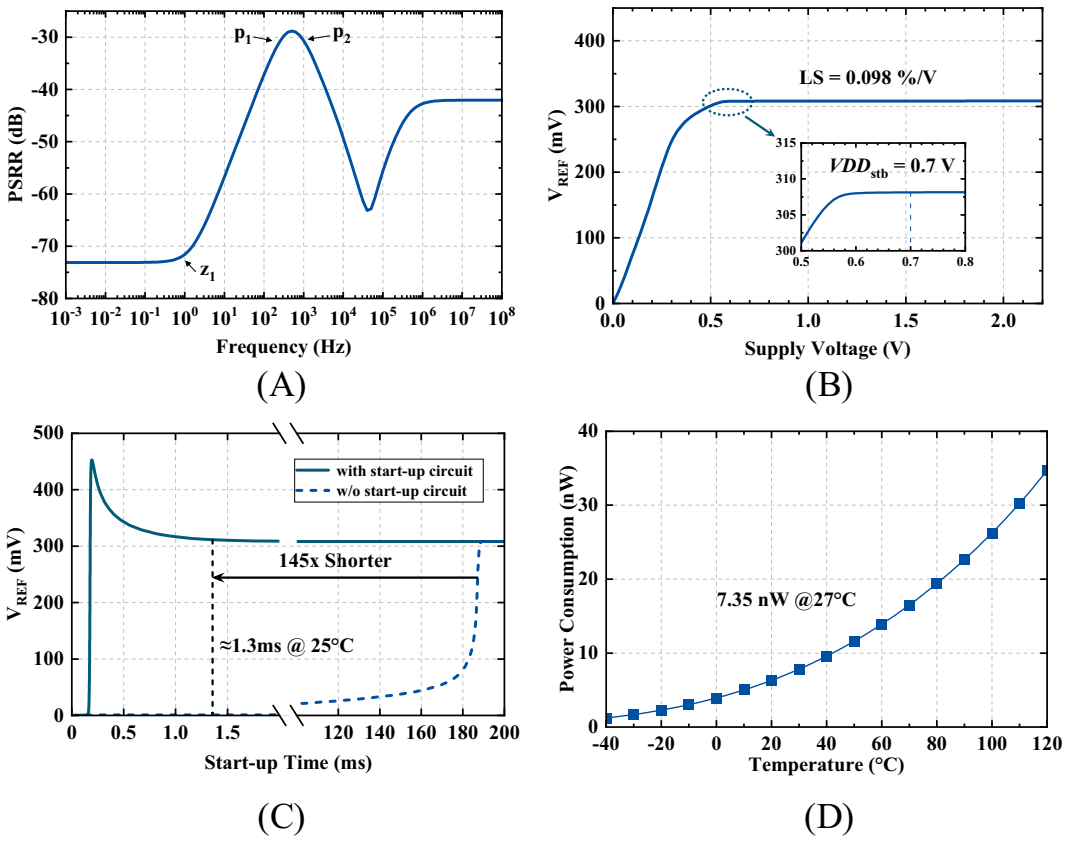

FIGURE 9 | The postlayout simulation results of the proposed VR circuit, (A) PSRR, (B) LS, (C) start-up time with and without the start-up circuit at room temperature, (D) power consumption.

A FoM that considers the main performance parameters of a VR, such as temperature range, TC, power, and silicon area [24], can be expressed as

$$\text{FoM} = \frac{\left(T_{\text{MAX}} - T_{\text{MIN}}\right)^2}{\text{TC} \times \text{Power} \times \text{Area}}. \tag{13}$$

The expression of this FoM indicates that the product between TC, power at room temperature, and silicon area must be as low as possible. BGR with higher precision [25] consumes relatively more power. This means that the resistorless solutions have advantages since the integrated resistors tend to occupy large areas when designing the circuit with low power [26].

Table 2 summarizes the performance comparison of the proposed circuit with various state-of-the-art VR circuits. After adding a temperature compensation circuit, the proposed circuit has a good TC performance with 6.42 ppm/°C in a wide temperature range of −40°C°C–140°C. In addition, since the proposed circuit uses an OPA, it also exhibits low linearity sensitivity and high power supply rejection ratio compared to the OPA-less subthreshold reference circuits. When $VDD = 1$ V, the proposed circuit has a power consumption of 7.35 nW at room temperature, which has a significant power advantage compared to other VR circuits using OPAs.

At the same time, since no resistance element is used in the circuit, it occupies a smaller area compared to other works.

TABLE 2 | Performance summary and comparison with other works.

	This work[a]	TCASII 2021[a] [1]	TCASI 2019[b] [3]	TCASII 2018[b] [6]	TCASII 2018[b] [7]	MJ 2020[a] [9]	ISCAS 2022[a] [16]	ICTA 2023[a] [23]
Technology (nm)	180	45	180	180	180	180	130	180
Type	CMOS	BGR	CMOS	CMOS	CMOS	CMOS	Sub-BGR	CMOS
Supply voltage (V)	0.7–2.2	1.1	0.7–2	0.4–1.8	0.6–2.0	0.7–2.0	0.9	0.8–2.0
Power (nW)	7.4	7500.0	28.0	9.6	30.5	21.0	30.0	15.6
V_{REF} (mV)	308	500	368	210	218	66	474	333
Temp. range (°C)	−40–140	−40–125	−40–120	−40–140	−40–125	−40–120	−20–80	0–120
TC (ppm/°C)	6.4	24.4	43.1	82.0	23.5	89.8	19.0	77.4
LS (%/V)	0.098	0.150	0.027	0.027	0.400	0.760	0.100	0.500
PSRR (dB)	−72@DC	−61@DC	−59@10 Hz	−59@10 Hz	−66.4@10 Hz	−90@10 Hz	N/A	−48@10 Hz
	−37@100 Hz		−39@1KHz	−47@1KHz	−42@1KHz			−31@1KHz
	−42@10 MHz	−12@30 MHz	−39@1 MHz	−53@1 MHz	−42@10 MHz	−64@1 MHz		−9@1 MHz
σ/μ (%)	0.84	0.17	0.35	0.31	0.45	1.7	0.95	0.22
Area (mm^2)	0.022	0.08	0.055	0.021	0.075	0.010	0.04	0.055
FoM ($°C^3 nW^{-1} mm^{-2}$)	3.12×10^{10}	1.86×10^{6}	3.86×10^{8}	1.96×10^{9}	5.06×10^{8}	1.36×10^{9}	4.39×10^{8}	2.17×10^{8}

[a]Postlayout simulation results.
[b]Measurement results.

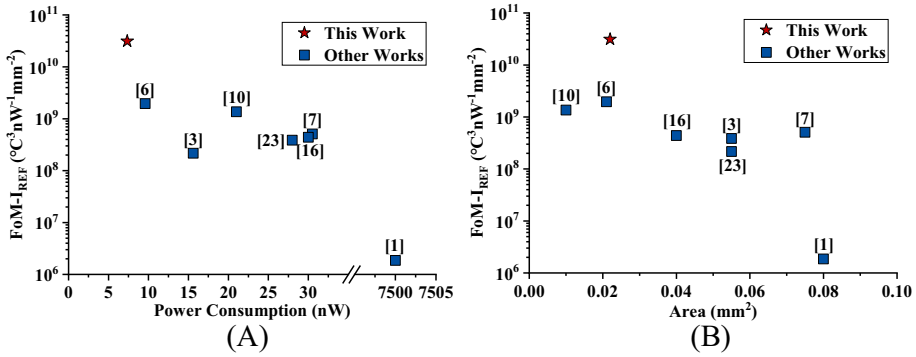

FIGURE 10 | The FoM comparison between the proposed circuits and other works with respect to (A) power and (B) area.

From (6), it can be inferred that the circuit relies on threshold voltage to generate the CTAT voltage, and the compensation current of the temperature compensation circuit is also related to the threshold voltage. Thus, the circuit is influenced by the process variations. In comparison with the published low-power reference voltage circuits, the proposed circuit does not excel in σ/μ, but the FoM indicating the overall performance is much better than others in Table 2. Figure 10 shows a comparison of the FoM among the proposed circuit and the published low-power VR circuits. The proposed circuit exhibits advantages in terms of area and power while having the best FoM performance.

5 | Conclusions

This paper proposes a subthreshold VR circuit with TC compensation. The VR is generated by two NMOS transistors with different threshold voltages, and then its temperature performance is further improved through a simple and low-power temperature compensation circuit. The theoretical analysis is deduced. This circuit is implemented using a standard 0.18-μm CMOS process. The postlayout simulation results show that the TC of the proposed VR circuit is 6.42 ppm/°C over a temperature range of −40°C°C–140°C, with a power consumption of 7.4 nW. This circuit is a promising solution for low-power low-voltage IoT sensor applications.

Data Availability Statement

Data sharing is not applicable to this article as no new data were created or analyzed in this study.

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