Dead-Zone Free, Static Phase Offset Improvement Phase Detector for High Resolution and Low Jitter Delay-Locked Loop

Dead-Zone Free, Static Phase Offset Improvement Phase Detector for High Resolution and Low Jitter Delay-Locked Loop

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Abstract. This work presents a phase detector (PD) having dead-zone free and static phase offset improvement performance. The proposed phase detector inherits the low power consumption advantage of the conventional phase detector using two true-single-phase clocking (TSPC) DFFs. It also effectively reduces the static phase offset, even in the presence of inevitable charge pump current mismatch. And the dead-zone problem of conventional TSPC PD is overcome by using a falling edge delay inverter. The PD is implemented using a standard 180nm CMOS technology. The dimension of the PD's layout is 11μm×16μm. Post-layout simulation shows that the power consumption is 53.8μW at 250MHz and 160μW at 800MHz. It achieves tiny static phase offset even if the charge pump has a 3.8% current mismatch.

Keywords: Phase Detector, Dead-Zone Free, Static Phase Offset, Delay-Locked Loop

1. Introduction

Delay-locked loops (DLL) are widely used in ADCs, TDCs and other circuits that require high-resolution, multiphase and low jitter clock. And they are also particularly useful in high-speed communication systems, where clock skew and jitter can cause significant signal degradation. The performance of a DLL depends on several factors such as the design of phase detector (PD), charge pump (CP), loop filter, voltage-control-delay line (VCDL), and the quality of the reference clock signal. The phase detector plays a significant role in the delay locked loop. As shown in Figure 1, the phase detector block converts the phase difference between the input reference clock (REF) and the clock output (FB) into a pulse signal. The FB comes from the last stage of Voltage Controlled Delay Line (VCDL). The pulse signal generated by the PD determines the charging and discharging time of the capacitor, which actually acts as a loop filter. Therefore the phase error is converted into a rising or falling voltage signal and it is fed back to the VCDL to control the signal delay. In this way, the phase error can be calibrated. The performance of the PD directly affect the performance of the DLL, including the jitter, phase noise, and static phase offset. Therefore, the design and optimization of the PD are essential for achieving high-performance DLLs in various applications.

The conventional reset-path based PD is widely used because of its dead-zone free ability, as shown in Figure 2 [1-3]. The phase detector consists of two D flip-flops and an AND gate on the reset path. The reset path guarantees that the extremely small input phase difference can be detected and the phase

detector outputs have enough pulse width to open the switches of charge pump. However, the pulse width generated by the reset-path based PD is usually so wide because of the delay of the reset path. This causes the charge pump will charges and discharges simultaneously when the DLL is in locked state. Static phase offset will occur due to the current mismatch of charge pump [4]. So the charge pump requires additional circuitry to improve current matching, which increases design complexity [5,6].

TSPC phase detector without reset path can detect a phase difference below 10ps, and reduces the requirement for the current matching of charge pump [7-9]. But its output pulse will become too narrow to turn on the charge pump switches when the phase difference of two input signals is small. This will causes the DLL to enter the dead zone. Random phase errors will accumulate and the DLL's output will have considerable jitter. One transistor is added to the output state of the TSPC PD block to reduce the dead zone [8], but the slow falling edge of output pulse causes the charge pump to turn off slowly, reduces the operation speed and increases the leakage current of charge pump. The requirement of an additional bias voltage is another drawback. [10] utilizes diode-connected devices to eliminate dead zone but also causes the charge pump to turn off slowly.

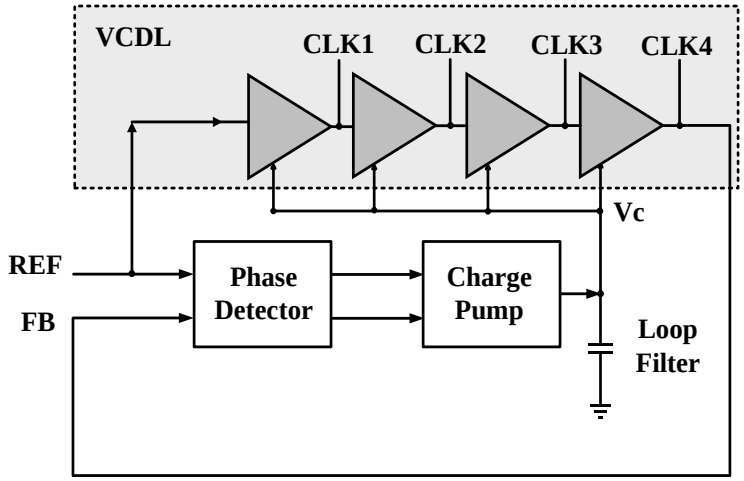

Figure 1. The structure of DLL system.

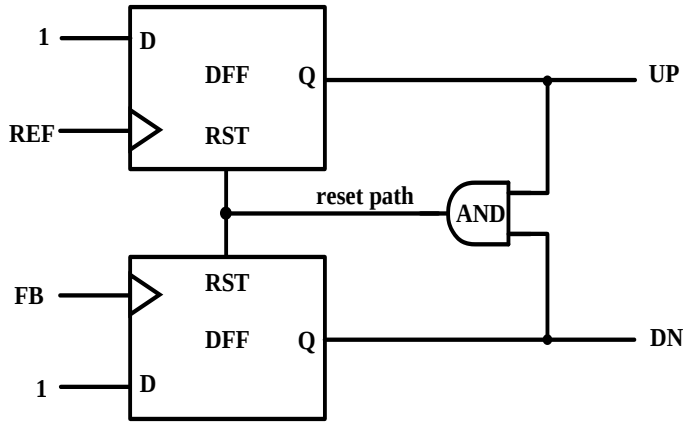

Figure 2. The structure of conventional reset-path based PD.

In this paper, the proposed PD overcomes the dead-zone problem of TSPC phase detector by adding a delay cell without additional bias voltage requirement. Additionally, even when the phase error of the two input signals is minimal, there can still be significant differences in the width and height of the two output pulses from the phase detector. This effectively reduces the static phase offset, even in the presence of inevitable charge pump current mismatch. The rest of the article is organized as follows,

Section II discusses the proposed design and working mechanism. Section III describes the simulations result and the performance of the proposed phase detector. Section IV concludes the work.

2. Proposed Phase Detector Design

The structure of the proposed dead-zone free phase detector is illustrated in Figure 3 and Figure 4 respectively. As shown in Figure 3, the proposed phase detector consists of two identical modified TSPC blocks. The modified TSPC block is composed of a phase detection circuit and a falling edge delay inverter. The falling edge delay inverter inverts the CLK1 signal and mainly delays the falling edge of signal CLK1_D. The stack forcing technique[11] is applied to the NMOS of the inverter to increase the output falling edge delay and reduce the power consumption. Thus, the MOS capacitor M12 only require very small size to achieve a suitable delay time t_{delay}. And t_{delay} can be estimated by (1).

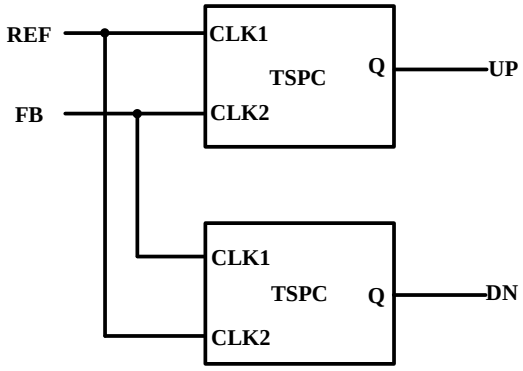

Figure 3. The structure of proposed phase detector

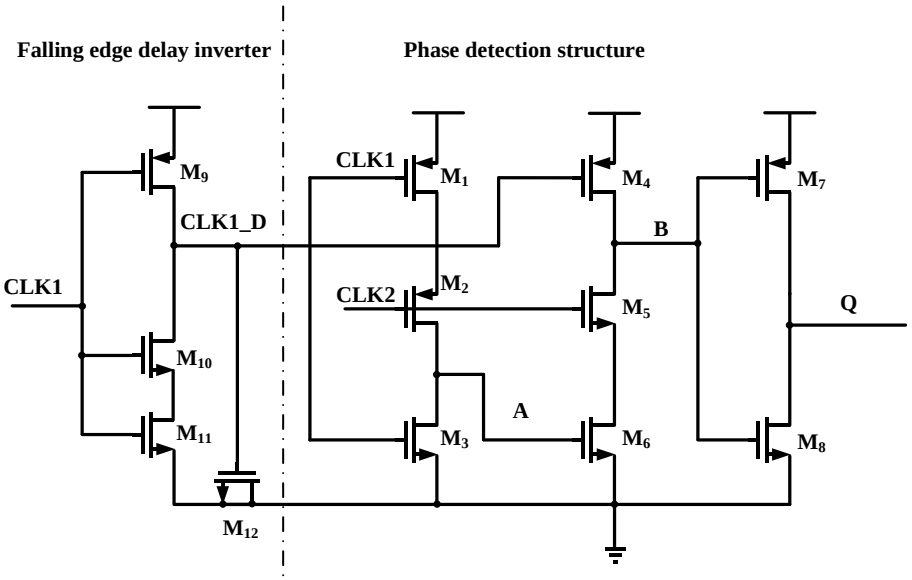

Figure 4. The structure of conventional reset-path based PD.

$$t_{delay} = \frac{CV_{DD}}{2\bar{i}} \tag{1}$$

Where C is the capacitance of MOS capacitor M12, $\bar{i}$ and V_{DD} are the average discharging current of the inverter and the supply voltage respectively. The source, drain and body of M12 all connect to ground and V_{GS} is high enough, so the capacitance C can be estimated by (2).

$$C = \frac{WL\varepsilon_{ox}}{t_{ox}} \tag{2}$$

Where ε_{ox} and t_{ox} are the dielectric constant and thickness of the gate oxide layer, and W and L are the dimensions of the transistor. The working mechanism of the modified TSPC block is described in the below.

2.1. CLK1 lags behind CLK2

Define both CLK1 and CLK2 signal at low logic as the initial state. Consider the case that CLK1 lags behind CLK2. The rising edge of CLK2 arrives at time t_{clk2} first, M2 is closed and M5 is opened. At this time, M6 is still open because node A is at logic high in the initial state. Node B is discharged to low logic through M5 and M6. And then node Q rises to high level. At time t_{clk1}, CLK1's rising edge arrives and opens M3, node A is discharged to low logic and M6 is closed. At time $t_{clk1}+t_{delay}$, signal CLK_D's falling edge arrives, opens M4 and charges node B to high level. The output Q becomes low logic. Define $\Delta t = t_{clk1} - t_{clk2}$, and suppose B and Q have the same height and width of pulse, then the duration time t_{pulse} of pulse Q can be estimated by (3).

$$t_{pulse} = \Delta t + t_{delay} \tag{3}$$

And the pulse height of Q can be expressed as

$$V_{pulse} = \min\left(\frac{\bar{i}_B \times (t_{delay,M3} + |\Delta t|)}{C_B}, V_{DD}\right) \tag{4}$$

Therefore, even when Δt is extremely small, the generated pulse also wide enough to enables the charge pump to turn on and eliminate the dead-zone.

2.2. CLK1 leads CLK2

Consider the case that CLK1 leads CLK2. The high logic of CLK1 firstly arrive at time t_{clk1} and node A is discharged by M3 to low logic after a period of time $t_{delay,M3}$. So M6 is shut down at time $t_{clk1}+t_{delay,M3}$ .Rising edge of CLK2 arrive at time t_{clk2} and open M5. Notice that CLK1_D turn on M4 at time $t_{clk1}+t_{delay}$. Let $t_{delay} \gg t_{delay,M3}$ by proper sizing of transistors. Then there are two cases:

- $t_{clk2} < t_{clk1} + t_{delay,M3}$. M5 is opened before M6 is closed. The discharge time of node B is $t_{delay,M3} - |\Delta t|$, then the pulse height of Q can be expressed as (5).

$$V_{pulse} = \min\left(\frac{\bar{i}_B \times (t_{delay,M3} - |\Delta t|)}{C_B}, V_{DD}\right) \tag{5}$$

  Where $\bar{i}_B$ and CB are the average discharge current and parasitic capacitance at node B respectively. And the pulse width of Q can be expressed as (6).

$$t_{pulse} = t_{delay} - |\Delta t| \tag{6}$$

- $t_{clk2} > t_{clk1} + t_{delay,M3}$, M6 is closed before M5 is opened, node B can't be discharged. The output Q can't generate a pulse of a certain height.

From (3) to (6), we can easily conclude that not only the generated pulse width but also the generated pulse height of "UP" and "DN" of the proposed PD have a difference of $2\Delta t$ and $\frac{2\bar{i}_B \times |\Delta t|}{C_B}$ respectively when the phase difference Δt between REF and FB is tiny. And the static phase offset can be significantly reduced even the charge pump mismatch exists.

3. Simulation Results of Proposed Phase Detector

Transient simulation results of the proposed phase detector are illustrated in Figure 5. Firstly, let REF lead FB by 1ns, as shown in Figure 5(a). The "UP" signal is charged to logic high along with the arrival of rising edge of REF signal. And the falling edge of "UP" signal does not arrive immediately after the arrival of FB's rising edge, but arrives after a certain delay. It is worth noting that the "UP" signal can quickly drop to low level thus the switches of the charge pump can be turned off in time. And "DN" signal remains unchanged from the beginning to the end. When REF lead FB by 10ps, the simulation result is shown in Figure 5(b). The output pulses "UP" and "DN" still have significant difference.

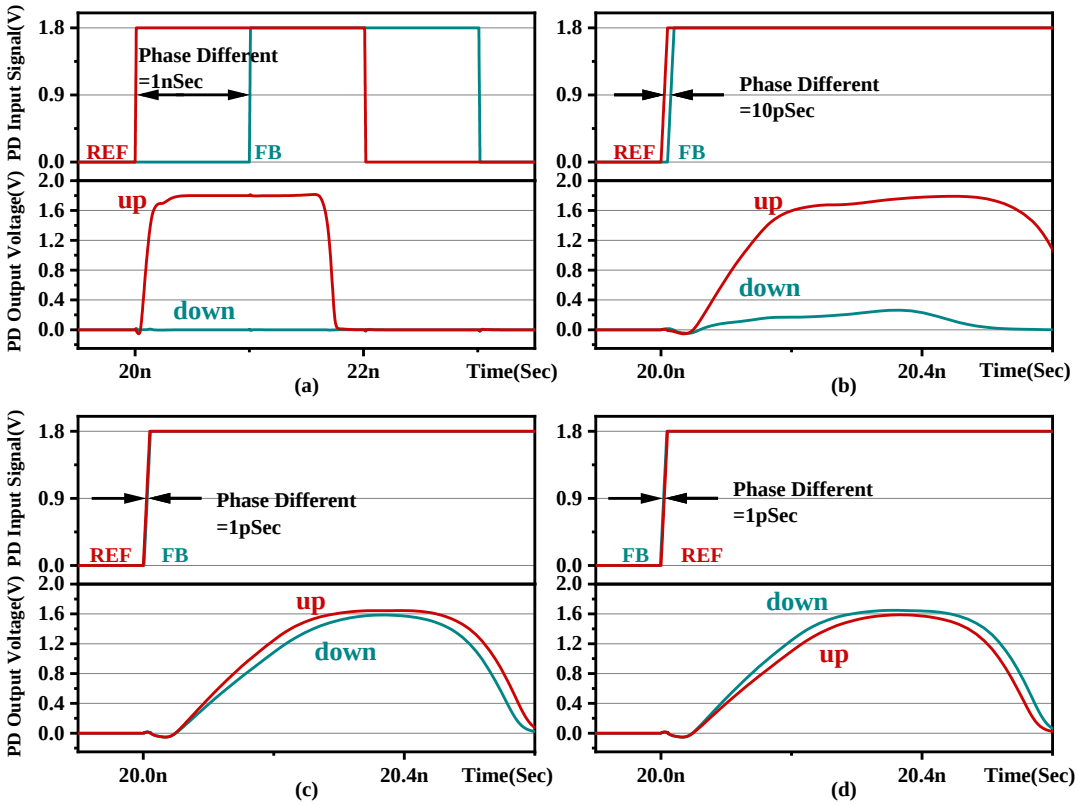

Figure 5. Transient behavior of the input and output signal of proposed PD when (a)REF leads FB by 1ns, (b) REF leads FB by 10ps, (c) REF leads FB by 1ps and (d)REF lags FB by 1ps

In other works, such as reset-path based PD[2], which has equal pulse height for both "UP" and "DN" signals and a difference in pulse width equal to the phase error of the input signal, is susceptible to charge pump mismatch, as illustrated in Figure 6. In case where there is a current mismatch in the charge pump, and the charging current controlled by the "UP" signal exceeds the discharge current controlled by the "DN" signal, the DLL will automatically adjust to make the pulse width of the "DN" signal greater than the pulse width of the "UP" signal. This ensures that the amount of charge flowing into and out of the loop filter capacitor is balanced in order to maintain a constant voltage "Vc" on the loop filter capacitor node. But the difference in pulse widths between "UP" and "DN" indicates that the DLL has a static phase error between the two input clock signals "REF" and "FB" of the phase detector. This error is also known as the static phase offset issue because the difference between the two pulse widths is derived from and equal to the static phase error of the two input signals "REF" and "FB" when the DLL is locked. In this work, the static phase offset issue caused by charge pump mismatch can be greatly reduced by the proposed phase detector. The results presented in Figure 5(c) and Figure 5(d) support our theoretical analysis, indicating that the proposed PD is less susceptible to charge pump current mismatch compared to other works, as evidenced by the larger width and height differences between the "UP" and "DN" output pulses at the input signal phase difference of $\pm 1ps$. Hence the proposed PD can improve the performance of DLL.

A charge pump which has the similar structure as [9] is used to verify the performance of the proposed PD. The charge and discharge current of the charge pump are 41.22μA and 42.82μA respectively. It is about a 3.8% mismatch when the output voltage of CP is 0.9V. Combine the proposed phase detector and the charge-pump circuit above with a 2pF loop-filter capacitor together, as illustrated in Figure 7. Change the phase difference between two input clock signals of the proposed phase detector, and observe the voltage change on the loop filter capacitor output node "Vc" in each clock cycle, we can get the transfer-characteristics of the system structure in Figure 7. under CMOS process corner and temperature variations, as shown in Figure 8. The input phase difference is changed from -200ps to +200ps. And the absolute value of voltage change decreases as the absolute value of phase difference decreases. It can be further observed from the focused area in Figure 8 that under the conditions of different temperatures and process corners, the transfer-characteristics curves all pass through the coordinate origin with a certain slope, which verify the dead-zone free and tiny static phase offset characteristics of the proposed PD.

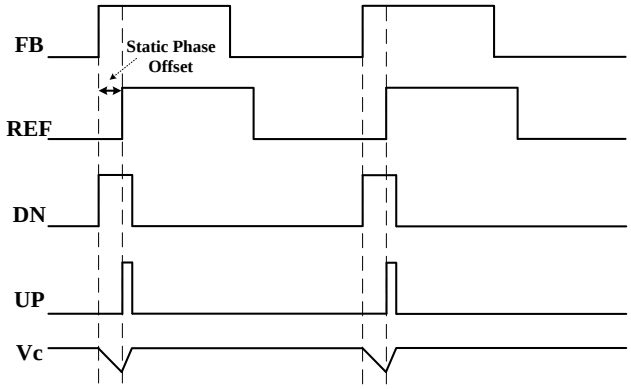

Figure 6. Static phase offset produced by reset-path based PD.

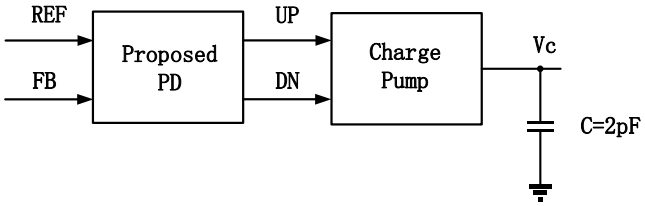

Figure 7. System structure for transfer characteristic testing.

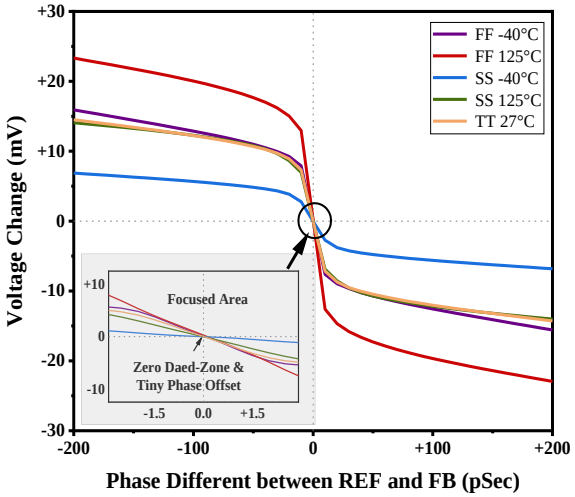

Figure 8. Transfer characteristic of the phase detector with charge pump

The proposed phase detector was implemented with $11\mu m \times 16\mu m$ dimensions ($0.000176 mm^2$) using single poly six-metal 180nm CMOS technology. The layout is shown in Figure 9. The performance of phase detector was simulated considering the parasitic parameters of the layout. The power consumption of the proposed PD is 53.8μW at 250MHz and 160μW at 800MHz. Table 1 shows the comparison among the proposed work and the other previous works. Although the power consumption is not the lowest in the table, the proposed phase detector has the ability of both dead-zone free and static phase offset improvement with a relatively lower power consumption. It also achieves smaller circuit area. These characteristics allow it to be used in a wide range of applications.

Table 1. Comparison of different Phase Detector design

Design Specification	**[9]**	**[12]**	**[13]**	**Proposed Work**
Process	180nm	180nm	130nm	180nm
Supply	1.8V	1.8V	1.2V	1.8V
Power	28μW @ 217MHz 104μW @ 800MHz	500μW @1GHz	134μW @128MHz	53.8μW @ 250MHz 160μW @ 800MHz
Area	-	$19\mu m \times 16\mu m$	-	$11\mu m \times 16\mu m$
Dead-zone free	No	No	Yes	Yes
Static phase offset improvement	Yes	No	No	Yes

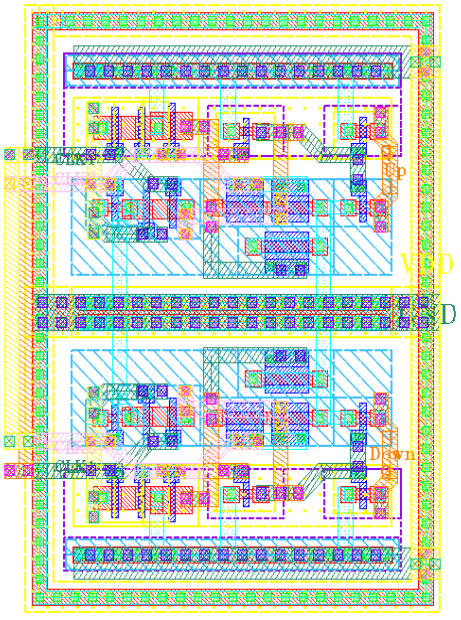

Figure 9. Layout of proposed phase detector

4. Conclusion

In conclusion, the proposed phase detector offers novel solution to both the dead-zone problem and static phase offset problem in phase detector. By using a falling edge delay inverter and capitalizing on the characteristics of the differences in both width and height between its output pulse signals “UP”

and “DN” when the input signals have tiny phase difference, the phase detector is able to effectively reduce the static phase offset even if the charge pump have inevitable mismatches, without sacrificing the charge pump turn-off speed. This is an improvement over existing solutions, which can’t provide any solution to both problems of dead zone and static phase offset at once. Furthermore, the proposed phase detector is highly versatile and can be applied to a wide range of high resolution and low jitter applications, including high resolution TDCs and ADCs. Overall, the results presented in this paper demonstrate the effectiveness and potential of the proposed phase detector in overcoming the limitations of current solutions. Further research and development in this area could lead to even more efficient delay-locked loop designs, with important applications in various fields.

5. References

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