An Adaptive Dark Current Compensation Analog Front-End with Reconfigurable Transimpedance Amplifier for Fluorescence Temperature Sensors

Bingjun Xiong, Jingjing Liu, Member, IEEE, Yang Wang, Yuchen Wang, Feng Yan, Jian Yang, and Yafei Zhang

Abstract-In this brief, a low-power CMOS analog front-end (AFE) circuit is proposed for fluorescence optical fiber temperature sensors. The CMOS AFE utilizes a novel adaptive dark current compensation technique to eliminate static operating point offsets in the front-end circuit, which occur due to the quick increases of photodiode dark current at high temperatures. The reconfigurable transimpedance amplifier (TIA) supports both high and low gain modes. Fabricated using a 180nm CMOS process, the AFE chip exhibits a -3dB bandwidth of 10kHz, a transimpedance gain of 158.51dBΩ, and an inputreferred noise current of 14.89fA/\(\sqrt{Hz}\) in its high gain mode. Under a 3.3V power supply, the circuit consumes 62.4µW in this mode. The temperature sensor prototype utilizing this AFE chip achieves high-precision measurements, with an average error of -0.1°C and a standard deviation of 0.33°C across a range from -30°C to 100°C.

Index Terms—Temperature sensor, Analog front-end circuit, Dark current compensation, Regulated current mirror.

I. INTRODUCTION

IDAR-based perception solutions are crucial for intelligent applications in low-altitude drones, industrial robots, and advanced autonomous vehicles [1]. These applications encounter significant challenges in complex environments. Specifically, high temperatures and strong crosstalk can severely impair the sensor measurement accuracy. The operating temperature of vehicle-mounted LiDAR must remain below 80°C to ensure optimal performance. Exceeding this limit can lead to device instability or failure, compromising environmental perception and decision-making processes, and ultimately increasing accident risk [2]. Thus, implementing real-time temperature monitoring is essential for maintaining the safety and functionality of LiDAR systems. Laser emitters and photoelectric sensors are the primary heat sources.

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Bingjun Xiong, Jingjing Liu, Yuchen Wang, Feng Yan, and Yafei Zhang are with the School of Electronics and Communication Engineering, Sun Yatsen University, Shenzhen 518107, China (e-mail: xiongbj@mail2.sysu.edu.cn; liujj77@mail.sysu.edu.cn; wangych79@mail2.sysu.edu.cn; yanf9@mail2.sysu.edu.cn; zhangyf273@mail2.sysu.edu.cn).

Yang Wang is with the College of Integrated Circuit Science and Engineering, Nanjing University of Posts and Telecommunications, Nanjing, 210023, China (wangyangjyz@njupt.edu.cn).

Jian Yang is with the School of Physics and Electronics, Hunan Normal University, Changsha 410081, China (e-mail: 514625349@qq.com).

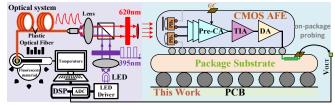


Fig. 1. The illustration of the fluorescence optical fiber temperature sensor system.

Additionally, the circuits and processors in the signal control unit generate electromagnetic signals. Optical fiber temperature sensors have many advantages over traditional ones, which are susceptible to electromagnetic interference and require frequent maintenance and calibration [3-6]. These advantages include high sensitivity, rapid response, resistance to electromagnetic interference, strong stability, and remote monitoring capabilities. Therefore, optical fiber temperature sensors offer a reliable safety monitoring solution for autonomous driving LiDAR systems [7-8].

The fluorescent optical fiber temperature sensor consists of rare earth fluorescent materials, optical path components, light emitting diode (LED) light source driving circuit, fluorescent signal AFE circuit and signal processor module [9]. The temperature measurement principle is depicted in Fig. 1. The LED is modulated by the light source driving circuit to emit pulsed excitation light with adjustable power. This light travels through a multimode quartz optical fiber to the sensor probe, where it excites the rare earth fluorescent material. The emitted weak fluorescence signal returns to the photodiode (PD) along the original optical path. The AFE converts this signal into a voltage for subsequent processing. The signal processor collects the fluorescence decay curve, calculates the fluorescence lifetime, and converts it into temperature data. Photodiodes are widely used as photodetectors in fluorescent fiber temperature sensors, converting fluorescence signals into photocurrent [10]. The AFE circuit typically consisting of a TIA and a post-amplifier (PA), converts this photocurrent into a voltage signal for subsequent digitization and analysis [11], 12]. The DC current from the background light source and the photodiode's dark current degrade sensing accuracy. They alter the input DC level of the front-end circuit, reducing sensor sensitivity [13]. In [14], variable transimpedance gain was implemented using shunt-shunt feedback, where different feedback resistors adjusted the gain. However, this method also affects the receiver's input impedance.

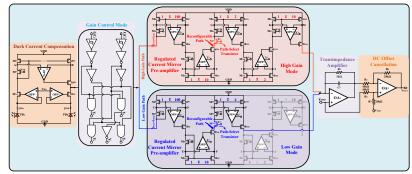


Fig. 2. The schematic diagram of the proposed CMOS AFE circuit.

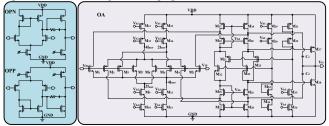


Fig. 3. The schematic diagram of the operational amplifiers.

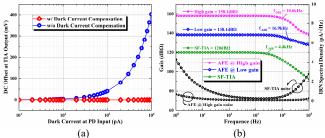


Fig. 4. (a) Cancellation of offset from the TIA output. (b) Frequency response simulation results of the proposed CMOS AFE.

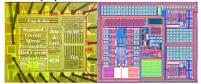


Fig. 5. Microscope image and layout of the proposed CMOS AFE.

As the photodiode's responsivity varies with load resistance, the generated current may deviate from the intended value in different gain modes, complicating practical applications. In [15], a current mirror based common-gate amplifier with a level shifter is utilized as a TIA to achieve low input impedance. However, the drain voltage of the current mirror transistor varies significantly with the output pulse, posing challenges for accurate current mirroring. In [16], an adaptive DC photocurrent cancellation circuit, comprising a low-pass error amplifier and a bypass transistor, is used to eliminate the photodiode's DC photocurrent. The above studies have addressed the influence of the photodiode's DC offset on the TIA performance from various perspectives. However, they do not account for the quick increase in the photodiode's dark current under high-temperature conditions, and its impact on the front-end circuit. The dark current of the photodiode rises exponentially with ambient temperature. In high-temperature environments, this dark current becomes significant and cannot be ignored [13]. A sharp increase in dark current can

shift the static operating point of the AFE circuit, leading to distortion. Additionally, it can cause a sudden rise in power consumption, further heating the sensor chip and potentially resulting in damage.

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In this brief, a CMOS AFE circuit is proposed for fluorescence optical fiber temperature sensors. The circuit uses adaptive dark current compensation, which addresses the offsets caused by quick increases in dark current at high temperatures. The reconfigurable TIA supports both high and low gain modes, achieving a precise current replication ratio. The TIA converts the photocurrent signal into a voltage, while DC offset cancellation technique (DCOC) eliminates the DC voltage at the output stage. The rest of this brief is organized as follows. Section II introduces the proposed the CMOS AFE. The experimental results and discussions are presented in Section III. Section IV concludes this brief.

II. DESIGN OF THE PROPOSED AFE CIRCUIT

The proposed AFE circuit consists of a dark current compensation circuit, a gain control (GC) module, a regulated current mirror preamplifier, a TIA and a DCOC circuit. This section presents the analysis of the AFE circuit implementation. The schematic diagram of the dark current compensation circuit is depicted on the left of Fig. 2. In this configuration, the PD_B is responsible for detecting the fluorescent signal, while the PD_A, shielded by the top metal, produces only dark current due to leakage. The anodes of the two photodiodes are grounded. The cathodes of PD_A and PD_B are connected to the inverting input terminals of operational amplifiers OPP₁ and OPP₂, respectively. The non-inverting terminals of both amplifiers are tied to the reference voltage $V_{\rm BG}$, ensuring identical reverse bias conditions for the photodiodes.

In this design, two types of operational amplifiers, OPP and OPN, are used in the dark current compensation module and the regulated current mirror preamplifier module. Both amplifiers feature a two stage operational amplifiers design with RC Miller compensation, and are depicted on the left of Fig. 3. Operational amplifier OPN₁ operates in a deep negative feedback state, ensuring that the V_{DS} voltages of PMOS transistors M_{P2} and M_{P3} are approximately equal. This configuration, involving PMOS transistors M_{P1} to M_{P4} and operational amplifier OPN₁, forms a regulated current mirror structure.

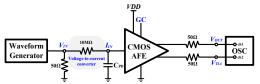


Fig. 6. Measurement setup for the frequency response of the AFE circuit.

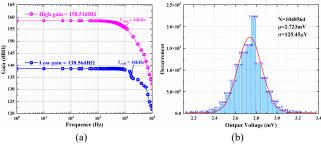
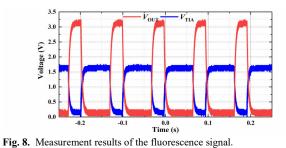


Fig. 7. (a) Measurement results of the CMOS AFE transimpedance gain. (b) Measurement results of the noise statistics for the proposed CMOS AFE.

Consequently, the accuracy of current mirror replication ratio is enhanced. By subtracting the dark current from the sensed photocurrent using a regulated current mirror, a pure photocurrent signal is generated and forwarded to the next stage, effectively achieving dark current compensation. After passing through the dark current compensation circuit, the pure photocurrent signal is directed to a regulated current mirror preamplifier.

The closed-loop negative feedback of the operational amplifier OPN2 equalizes the drain voltages of the PMOS transistors M_{P6} and M_{P7}, ensuring precise photocurrent amplification based on the configured mirror ratio. A large current gain is achieved by multiple stage of regulated current mirror preamplifiers. The gain control module facilitates adjustable gain selection by configuring the preamplifier with specific mirror ratios. In this design, setting GC to 1:0 enables high-gain mode with a mirror ratio of 40000, and setting GC to 0:1 enables low-gain mode with a mirror ratio of 4000. Specifically, the high-gain path is indicated by the crimson box in Fig. 2, while the low-gain path is indicated by the lavender box. Both paths utilize a shared two-stage, regulated current mirror preamplifier structure. Path selection is achieved using transistors M_{N7} and M_{N12}, enabling a configurable gain mode. When the control signal Y4 is low and Y₅ is high (as generated by the GC module), M_{N7} is turned off and M_{N12} is turned on, directing the current signal to the low-gain path. Conversely, when Y4 is high and Y5 is low, M_{N7} is turned on and M_{N12} is turned off, shutting off the lowgain path and routing the signal through the high-gain path.

The operational amplifier OA_1 , feedback resistor R_F , and compensation capacitor C_F form a TIA that converts the preamplifier's output current into a voltage signal. The DCOC circuit functions as the output stage, eliminating the DC offset voltage, and delivering the voltage signal to the subsequent signal processing circuit. In this design, rail-to-rail operational amplifiers are utilized in both the TIA module (OA1) and the DCOC module (OA₂), and are depicted on the right of Fig. 3. Rail-to-rail input is achieved through a complementary differential pair, while constant transconductance is ensured by a 2:1 tail current source. To obtain a rail-to-rail output



swing, the operational amplifier's output stage employs a class

AB configuration. Additionally, a floating complementary bias structure, comprising two linear transconductance circuits, stabilizes the gate voltage of the M₃₇ and M₃₈ at the output stage. This design strategy enhances the drive capability of the operational amplifier and minimizes crossover distortion, thereby improving the overall performance. Therefore, the transimpedance gain R_T of the entire CMOS AFE can be expressed as:

$$R_T = \begin{cases} 80000R_F GC = 1:0 \\ 8000R_F GC = 0:1 \end{cases}$$
 (1)

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Noise analysis of the multi-stage amplifier reveals that the first stage predominantly determines the overall noise level. The equivalent noise current of the first stage in the proposed CMOS AFE primarily arises from the common-gate amplifier circuit with M_{N2} as the input, M_{P6} as a diode-connected load, and the cascode current mirror composed of M_{P3} and M_{P4}. Consequently, the total equivalent input-referred current noise power is given by the following formula:

$$\frac{\overline{i}_{n,in}^2}{\overline{g}_{MN2}^2} \approx \frac{4kT}{g_{MN2}^2} \left(\gamma \cdot g_{MN2} + \gamma \cdot g_{MP3} + \gamma \cdot g_{MP4} + \frac{1}{g_{MP6}} \right)$$
(2)

Fig. 4(a) illustrates the simulation results of the proposed dark current compensation circuit, showing its effectiveness in suppressing the influence of dark current on the DC offset voltage at the TIA output. This suppression ensures the stability of the TIA's static operating point. Fig. 4(b) illustrates the simulation results of the AFE frequency response in two typical gain modes. In the high gain mode, the AFE consumes 18.9µA of current. With this same power consumption, the maximum gain of proposed CMOS AFE achieves 80 times greater than the traditional shunt feedback (SF) TIA. Furthermore, the bandwidth expands from 4.4kHz to 10.6MHz, and the noise current spectral density is significantly reduced.

III. EXPERIMENTAL RESULTS AND DISCUSSION

The proposed CMOS AFE is fabricated using a standard 180nm CMOS process with an effective size of 977µm by 785µm and its microscope image and layout are shown in Fig. 5. Fig. 6 depicts the measurement setup for the frequency response. The input 50Ω resistor provides impedance matching with both the cable and the printed circuit board (PCB). A $10M\Omega$ resistor is employed as a voltage-to-current converter, while a 0.5pF capacitor, CPD, models the parasitic capacitance of the photodiode. The digital control signal GC is used to adjust the gain of the circuit. The output of the AFE is connected to an oscilloscope, which is impedance-matched at 50Ω .

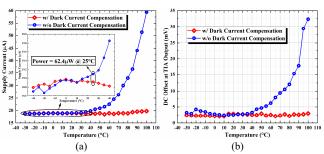


Fig. 9. (a) Measurement results of supply current at different temperatures.(b) Measurement results of DC offset voltage at different temperatures.

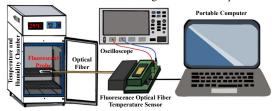


Fig. 10. Measurement platform of the proposed fluorescence optical fiber temperature sensor.

To evaluate the frequency response of the proposed CMOS AFE, a RIGOL DG5352 waveform generator produces a 0.2V peak-to-peak ($V_{\rm PP}$) sinusoidal input voltage $V_{\rm IN}$. This voltage is converted to a 20nA peak-to-peak input current signal $I_{\rm IN}$. The output voltage $V_{\rm OUT}$ is displayed using an SDS6204 H10 Pro oscilloscope.

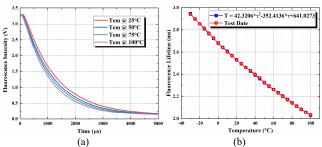
By varying the frequency of the sinusoidal signal while keeping the amplitude constant at $0.2V_{\rm PP},~V_{\rm OUT}$ is recorded to derive the transimpedance gain curve. Fig. 7(a) shows the frequency response of the high gain mode, with a transimpedance gain of 158.51dB, and a -3dB bandwidth of 10kHz. Similarly, the low gain mode exhibits a transimpedance gain of 138.5dB, and a -3dB bandwidth of 16kHz.

Fig. 7(b) presents the integrated output noise measured using an SDS6204 H10 Pro oscilloscope, which features a bandwidth of 2 GHz. In the high gain mode, the root mean square (RMS) noise is measured to be 125.45 μ V. Based on this measurement, the average equivalent input-referred noise power spectral density (PSD) can be obtained as shown in (3).

$$i_{n,in,avg} = 125.45 \mu V / 158.51 dB \cdot \sqrt{10kHz} = 14.89 fA / \sqrt{Hz}$$
 (3)

The output voltages $V_{\rm TIA}$, and $V_{\rm OUT}$ of the CMOS AFE were measured, with continuous adjustments made to the LED's operating current to optimize the fluorescence signal, as depicted in Fig. 8. Through fine-tuning, a robust fluorescence signal with a 3.2V peak-to-peak value was achieved, facilitating accurate lifetime determination by the signal processing system.

Fig. 9 shows the measurement results of the power supply current of the proposed CMOS AFE, and the output DC offset voltage of the TIA at different temperatures. These results were obtained through optoelectronic testing using a cascaded PD and TIA structure. The test setup comprised a precision temperature and humidity chamber, a source meter (KEYSIGHT B2910BL), and a DC voltage source. During testing, the AFE chip was placed in the chamber under darkroom environment and powered by a DC supply. The chamber maintained a stable temperature, while the source meter recorded the supply current and TIA output DC offset voltage across the temperature range.



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Fig. 11. (a) Fluorescence decay curves collected at various temperatures. (b) Relationship between fluorescence lifetime and external temperature changes.

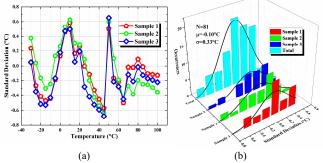


Fig. 12. (a) Standard temperature error measured by three CMOS AFE sample chips. (b) Statistical results of standard temperature errors by three CMOS AFE sample chips.

The results indicate that, without the dark current compensation circuit, the power supply current increases with temperature. This rise is primarily due to the elevated PD dark current level. However, when the proposed dark current compensation circuit is utilized, the power supply current remains nearly stable at $18.9\mu A.$ At $25^{\circ}C,$ the total power consumption of the CMOS AFE circuit is $62.4\mu W.$ Similarly, the measurement results demonstrate the effect of temperature on the TIA's output DC offset voltage, which is primarily caused by the PD's dark current. The proposed dark current compensation circuit maintains this voltage at a stable 3mV. This stability ensures that the static operating point of the subsequent circuit remains consistent.

To activate the prototype's temperature detection capability, a comprehensive calibration is necessary. This involves measuring fluorescence lifetimes at standardized temperatures to establish their relationship with temperature. Repeated calibrations are essential to minimize random errors. Fig. 10 illustrates the fluorescence temperature sensing measurement platform, which includes a precise temperature and humidity chamber (± 0.01 °C), the fluorescence optical fiber temperature sensor, an oscilloscope, and a PC. Initially, the chamber temperature is set to -30°C. Once stabilized, the prototype captures the fluorescence signal. The CMOS AFE output is processed through the ADC and MCU for fluorescence lifetime extraction, which is then automatically logged by the PC. To reduce experimental errors, fluorescence lifetimes were measured 200 times at each temperature point, and the average value was calculated. The temperature was gradually increased from -30°C to 100°C, with measurements results recorded at 5°C intervals. Fig. 11(a) illustrates the decay curves at selected temperatures: 25°C, 50°C, 75°C, and 100°C. The relationship between fluorescence lifetime (τ) and external temperature (T) was established, as shown in Fig. 11(b). The results indicate that τ decreases as T increases,

aligning with established theoretical predictions. The data points demonstrate strong linearity with the fitted curve. Additionally, calibration experiments revealed a quadratic relationship between τ and T:

$$T = 42.3206\tau^2 - 352.4136\tau + 641.0273 \tag{4}$$

To assess the accuracy of the proposed prototype's temperature measurements, a temperature and humidity chamber was employed for each constant temperature test. The temperature was calculated using Equation (4) on a PC and compared with the chamber's standard temperature. Fig. 12(a) illustrates the measurement errors, defined as the difference between the prototype readings and the chamber's standard temperatures. To minimize random errors, 200 readings were averaged at each standard temperature point. Fig. 12(b) presents statistical data from three CMOS AFE sample chips. Three prototypes were tested with total 81 temperature points. The statistical mean temperature was found to be -0.1°C, with a standard deviation of 0.33°C. Table I shows the performance comparison of the proposed frontend circuit with other works. For fairly comparing the performance among the works, a figure of merit (FoM) is defined based on [1] and [17] as follows:

$$FoM = \frac{Gain(\text{dB}\Omega) \cdot BW(kHz)}{IRN(pA/\sqrt{Hz}) \cdot Power(mW)}$$
 (5)

In Table I, it is evident that the FoM of the proposed CMOS AFE circuit surpasses other works. It demonstrates significant advantages, particularly in power consumption and noise performance. Table II compares the temperature sensor's performance with state-of-the-art technologies. The results indicate that the sensor developed with the proposed CMOS AFE circuit achieves significant improvements in the measurement accuracy.

TABLE I PERFORMANCE COMPARISON WITH ANALOG FRONT END CIRCUIT

	This work	SJ'24 ^[9]	SJ'20 ^[11]	TVLSI'24 ^[17]
Process	180 nm	180 nm	130 nm	180 nm
Supply	3.3 V	3.3 V	1.2 V	3.3 V
Gain (dBΩ)	158.51	120.23	98.6	107
Bandwidth	10 kHz	6.7 kHz	43.3 kHz	165 MHz
IRN PSD	14.89 fA/√Hz	8.79 pA/√Hz	1.19 pA/√Hz	2.29 pA/√Hz
Power (mW)	0.0624	1.12	2.16	51.48
Area (mm2)	0.766	0.25	2.2	10.5
FoM	1.71×10 ⁶	8.18×10 ¹	1.66×10 ³	1.49×10 ⁵

TABLE II
PERFORMANCE COMPARISON WITH RECENT TEMPERATURE SENSORS

TERFORMANCE COMPARISON WITH RECENT TEMPERATURE SENSORS						
	This work	TCASII'24[3]	JSSC'24 ^[5]	TCASII'22 ^[6]		
Process	180 nm	180 nm	180 nm	180 nm		
Supply	3.3 V	2 V	1.8 V	1.8 V		
Power	62.4 μW	300 μW	61.2 μW	600 μW		
T. Range (°C)	-30 to 100	-40 to 75	-50 to 100	-30 to 100		
Accuracy	0.33	1	1.96	0.74		

IV. CONCLUSION

This brief proposes a reconfigurable analog AFE circuit with dark current compensation, fabricated using a 180nm CMOS process. In the high gain mode, the AFE circuit achieves a transimpedance gain of 158.51dB Ω , a -3dB bandwidth of 10kHz, an input-referred noise current spectrum density of 14.89fA/ $\sqrt{\text{Hz}}$, and a power consumption of 62.4 μ W. The temperature sensor prototype's testing within -30°C to 100°C show an average temperature error of -0.1°C and a standard deviation of 0.33°C. This AFE circuit is suitable for high-precision fluorescent fiber temperature sensor applications.

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