An Ultra-Low Power CMOS Subthreshold Voltage Reference with Temperature Coefficient Compensation

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Abstract This paper presents a nanowatt voltage reference (VR) with an ultra-low power consumption temperature coefficient compensation. All transistors are biased in the subthreshold region to reduce the power consumption of the proposed VR circuit. The complementary-to-absolute-temperature (CTAT) voltage and proportional-to-absolute-temperature (PTAT) voltage are mainly generated by two NMOS transistors with different threshold voltages. At the same time, a simple temperature compensation circuit is designed to optimize the temperature coefficient at high temperatures, so that the circuit can generate a reference voltage with a wider temperature range and a lower temperature coefficient. The proposed VR circuit is fabricated in a 0.18-μm CMOS process with a silicon area of only 0.022 mm^2. Theoretical analysis and post-layout simulation results verified the reliability and performance improvement of circuit operation. The proposed VR circuit generates a

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reference voltage of 308.21 mV with a temperature coefficient of 6.42 ppm/°C over a wide temperature range of −40 ~ 40 °C. The power consumption of the circuit is 7.04 nW. The voltage line sensitivity (LS) is 0.099%/V.

Keywords Voltage reference · Low power · Low supply voltage · Temperature compensation · Temperature coefficient · Subthreshold

1 Introduction

Nowadays, the Internet of Things (IoT) technology is developing rapidly. The IoT sensors are developed for small size, low voltage, and low power, or even self-powered by harvesting energy from the environment. So, we need to design a voltage reference circuit with good performance and meet the requirements of low voltage and low power consumption. A voltage reference circuit is a very basic module in the analog circuit field. The performance of a voltage reference circuit often affects the overall performance of the entire system. The VR circuit needs to generate a stable voltage independent of process, power supply voltage, and temperature under the condition of low and unstable power supply voltage and low power consumption. Therefore, sub-threshold CMOS voltage reference circuits have attracted more and more attention in recent years.

Sub-threshold CMOS circuits using leakage currents are becoming more widely used [1], as well as in reference circuits. In 2012, with the introduction of a two-transistor voltage reference using leakage currents, the power consumption and power supply of the VR circuit were reduced without the use of bipolar junction transistors (BJT) [2]. Then, based on the two-transistor structure, the bias current can be set and a stable reference circuit can be built by taking advantage of the virtual short characteristic of the input end of the operational amplifier (OPA). However, their power consumption is relatively high [3–6]. In 2020, a self-biased reference circuit based on the two-transistor structure without amplifiers and start-up circuits was proposed. It has advantages in power consumption and start-up time, but the temperature coefficient is only 62 ppm/°C [7]. In 2022, a voltage reference circuit combining sub-threshold transistors and BJTs was proposed, but due to the use of BJT transistors, power consumption is relatively high, and minimum power supply voltage is limited [8].

To solve some of the problems mentioned above, this work proposes a CMOS subthreshold voltage reference circuit using a temperature compensation circuit, without BJT transistors. The rest of the paper is organized as follows, Section 2 discusses the proposed design and working mechanism. Section 3 describes the simulation results and the performance of the proposed VR circuit. Section 4 concludes the work.

2 The Proposed Voltage Reference Circuit

The CMOS subthreshold voltage reference circuit proposed in this work is shown in Fig. 1. This circuit includes a start-up circuit, a bias circuit, an OPA circuit, a VR core circuit, and a temperature compensation circuit. The start-up circuit includes M_{S1}, M_{S2}, and M_{S3}, which can make the circuit deviate from the original zero bias point into the normal operation state, wherein M_{S1} acts as a capacitor. When the power supply is just powered on, the voltage reference output voltage value is zero. At this time M_{S3} is turned off, through continuous charging. When the gate voltage of M_{S2} increases, it causes M_{S2} to be turned on. And then all the gate voltages of M_{P5} and M_{P6} are pulled down. The two branches of the VR core circuit start to flow current, and this current is copied to each branch of the voltage reference circuit through the current mirrors. Finally, the circuit starts to work normally. When the output voltage reference is greater than the V_{TH} of M_{S3}, M_{S3} is turned on and the gate voltage of M_{S2} is pulled down. So M_{S2} is turned off and the start-up circuit is turned off. The low-temperature coefficient of the circuit is mainly realized by the temperature compensation circuit, which adjusts the voltage deviation of the output voltage of the voltage reference core circuit at high temperatures.

2.1 Operating Principle

All the transistors in the circuit are biased in the sub-threshold region. The purpose is to reduce the power supply voltage and power consumption. Among them, M_{N8} and M_{N11} are thick-oxide NMOS, and the rest are thin-oxide transistors. The main part of the voltage reference circuit can generate PTAT voltage and CTAT voltage for first-order temperature coefficient compensation. The drain current of the subthreshold transistor is as follows:

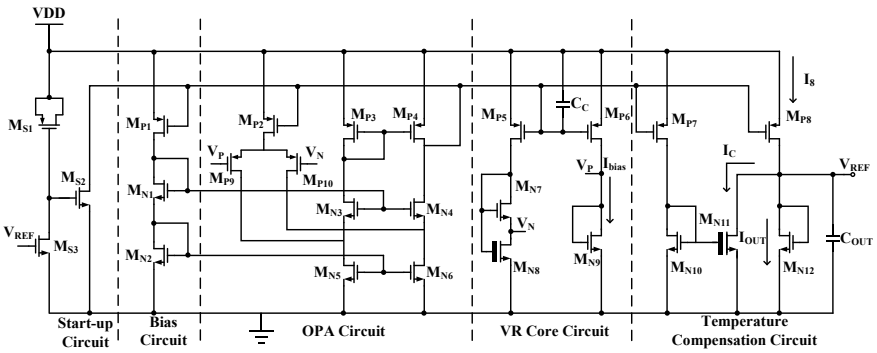

Fig. 1 Proposed CMOS subthreshold voltage reference

$$I_{\mathrm{D}} = \mu_{\mathrm{n}} C_{\mathrm{OX}} (m-1) K V_{\mathrm{T}}^2 \exp\left(\frac{V_{\mathrm{GS}} - V_{\mathrm{TH}}}{m V_{\mathrm{T}}}\right)\left(1 - \exp\left(\frac{-V_{\mathrm{DS}}}{V_{\mathrm{T}}}\right)\right) \tag{1}$$

where μ_{n} is the mobility of the electrons, C_{OX} is the gate-oxide capacitance per unit area, V_{TH} is the threshold voltage of the transistor, K is the aspect ratio (=W/L) of the transistor, $V_{\mathrm{T}} = k_{\mathrm{B}}T/q$ is the thermal voltage, k_{B} is the Boltzmann constant, and T is absolute temperature, q is the elementary charge, and m is the subthreshold slope factor. In the derivation process, it can be approximated that the C_{OX} and V_{TH} of the same type of NMOS transistors are equal, and the subthreshold slope factor m of all NMOS transistors is the same. When $V_{\mathrm{DS}} \geq 3V_{\mathrm{T}}$, the drain current of the transistor in the subthreshold region can be approximated as:

$$I_{\mathrm{D}} = \mu_{\mathrm{n}} C_{\mathrm{OX}} (m-1) K V_{\mathrm{T}}^2 \exp\left(\frac{V_{\mathrm{GS}} - V_{\mathrm{TH}}}{m V_{\mathrm{T}}}\right) \tag{2}$$

Since the drain current of $\mathrm{M_{N7}}$ and $\mathrm{M_{N8}}$ are equal, $I_{\mathrm{DN7}} = I_{\mathrm{DN8}}$. There is a threshold voltage difference between $\mathrm{M_{N7}}$ and $\mathrm{M_{N8}}$, the voltage of node N is as follows:

$$V_{\mathrm{N}} \approx (V_{\mathrm{THN8}} - V_{\mathrm{THN7}}) + m V_{\mathrm{T}} \ln\left(\frac{C_{\mathrm{OXN7}} K_{\mathrm{N7}}}{C_{\mathrm{OXN8}} K_{\mathrm{N8}}}\right) \tag{3}$$

It can be seen that the voltage of the node N is independent of the branch current. Due to the use of NMOS transistors with different gate oxide thicknesses, there is a threshold voltage difference ΔV_{TH} between them, and the difference in threshold voltage generates a CTAT voltage:

$$\Delta V_{\mathrm{TH}} = \Delta V_{\mathrm{TH0}} + (\alpha_{\mathrm{N8}} - \alpha_{\mathrm{N7}})(T - T_0) \tag{4}$$

where α is the first-order temperature coefficient of the threshold voltage, and $\alpha < 0$. ΔV_{TH0} is the threshold voltage difference at normal temperature, and T_0 is the normal temperature of 300 K. At the same time, the ΔV_{TH} has a negative temperature coefficient reduced by $(\alpha_{\mathrm{N8}} - \alpha_{\mathrm{N7}})$. The slope of the thermal voltage V_{T} generating PTAT voltage does not need to be too large to offset the first-order temperature coefficient. So, it can also reduce the number of PTAT stages. According to the characteristics of the operational amplifier, the voltage at node P is forced to be the same as the node N, so the bias current I_{bias} is:

$$\begin{aligned} I\mathrm{bias} = \mu_{\mathrm{n}} \frac{C_{\mathrm{OXN9}} C_{\mathrm{OXN7}}}{C_{\mathrm{OXN8}}} (m-1)\left(\frac{K_{\mathrm{N9}} K_{\mathrm{N7}}}{K_{\mathrm{N8}}}\right) \\ V_{\mathrm{T}}^2 \exp\left(\frac{V_{\mathrm{THN8}} - V_{\mathrm{THN7}} - V_{\mathrm{THN9}}}{m V_{\mathrm{T}}}\right) \end{aligned} \tag{5}$$

The final output voltage reference is generated by I_{OUT}, and $I_{\mathrm{OUT}} = I_8 - I_{\mathrm{C}}$, where I_8 is the current copied by I_{bias} through the current mirror. I_{C} is the compensation current generated by the temperature compensation circuit, which is used to

compensate for the temperature coefficient at high temperatures. Finally, the voltage reference output value generated by I_{OUT} through the active load M_{N12} is as follows:

$$V_{REF} \approx V_{THN12} + mV_T \ln\left[\frac{C_{OXN7}K_{N7}K_{N9}K_{P8}}{C_{OXN8}K_{N8}K_{P6}K_{N12}}\right. \\ \left.\exp\left(\frac{V_{THN8} - V_{THN7} - V_{THN9}}{mV_T}\right) - \frac{K_{N7}K_{N9}K_{P7}K_{N11}}{K_{N8}K_{P6}K_{N10}K_{N12}}\exp\left(\frac{-V_{THN7}}{mV_T}\right)\right] \tag{6}$$

It can be seen that in the low-temperature range, V_T is small, and $\exp(-V_{THN7}/mV_T) = K_C$ can be ignored. Then (6) can be approximate to be (7).

$$V_{REF} \approx V_{THN8} - V_{THN7} + mV_T \ln\left[\frac{C_{OXN7}K_{N7}K_{N9}K_{P8}}{C_{OXN8}K_{N8}K_{P6}K_{N12}}\right] \tag{7}$$

In the low-temperature range, V_{REF} is similar to the voltage of node N. The CTAT voltage and the coefficient-controllable PTAT voltage can be superimposed to eliminate the first-order temperature coefficient by adjusting the transistors' size. When the circuit is in a high-temperature range, the voltage is no longer dominated by the first-order temperature coefficient. As the temperature rises, the temperature coefficient needs to be compensated. With the continuous increase of V_T, K_C can no longer be ignored and the continuously increasing voltage reference output is reduced. Therefore, the temperature performance and operating temperature range of the circuit are effectively improved. The PTAT voltage, which is used to compensate for the first-order coefficient of CTAT, depends on K_{N7}, K_{N8}, K_{N9}, K_{P6}, and K_{P8} parameters. The current I_C is used to compensate for the high-temperature coefficient of the circuit, which is determined by K_{N7}, K_{N8}, K_{N9}, K_{P6}, K_{P7}, K_{N10}, K_{N11}, and K_{N12} parameters. At the same time, the power consumption of the entire circuit is also determined by each transistor's size, so the optimal size of each transistor is a balance between performance and power.

2.2 Analysis of LS

Both LS and PSRR are key indicators that need to be paid attention to in voltage reference circuits. In low-voltage and low-power applications, the operating bandwidth of transistors in the subthreshold region is low, resulting in poor PSRR performance and greater impact from power supply voltage disturbances. Therefore, the improvement of these indicators is particularly critical. The index LS to evaluate the dependence of V_{REF} on the change of direct current (DC) voltage is defined as:

$$LS = \frac{\Delta V_{REF}}{\Delta VDD \times V_{REF}} \times 100\% \tag{8}$$

where ΔVDD and ΔV_{REF} are respectively the power supply voltage range in which the reference voltage circuit works normally and the corresponding reference voltage output variation range. It can be seen from the derivation of (6) that as long as the drain-source voltage V_{DS} of the NMOS transistor in the circuit is greater than or equal to $3V_T$, the reference voltage output does not depend on the change of supply voltage. However, in the derivation process, the current mirror circuits are regarded as ideal devices, and all actual LS will depend on the LS of the current mirror transistors.

3 Post-simulation Results

The proposed voltage reference circuit is implemented by all MOSFET, and designed using a standard 0.18-μm CMOS process. Figure 2 shows the circuit layout, the area occupied by the circuit is 0.022 mm^2, which includes 4.5 pF output capacitance C_{OUT} and 1.7 pF compensation capacitance C_C. Figure 3 shows the simulation results of the temperature performance with and without the temperature compensation circuit. It can be seen that without the temperature compensation circuit, V_{REF} rises rapidly at high temperatures, limiting the circuit's temperature performance and operating temperature range. The proposed VR circuit has an improved temperature coefficient in the high-temperature range. The temperature compensation circuit compensates for the rapidly increasing V_{REF} under high-temperature conditions and realizes the temperature coefficient compensation. Finally, the temperature coefficient of the circuit is reduced to 6.42 ppm/°C, and the operating temperature range of the proposed VR circuit is increased to −40 ~ 140 °C.

Figure 4 shows the post-simulation results of voltage line sensitivity. When the power supply voltage is 0.7–2.2 V, the LS of the proposed VR circuit is only 0.099%/V at room temperature (25 °C). Figure 5 shows the power consumption performance of the mentioned voltage reference circuit at different temperatures when the power supply voltage is 1 V. It can be seen that the power consumption at room temperature is as low as 7.04 nW. Figures 6 and 7 show the start-up time at 25 °C and −40 °C, respectively. The start-up time of the circuit is about 1.3 ms at room temperature.

Table 1 summarizes the performance comparison of low-power reference circuits that have been reported in recent years. With the introduction of an efficient temperature compensation circuit, the circuit can achieve a good temperature coefficient performance in a wide temperature range of −40 °C to 140 °C, while also maintaining low power consumption. Additionally, as the proposed design utilizes an OPA, the circuit exhibits low LS. After integrating the start-up circuit, the start-up time at room temperature has been reduced to 1.3 ms. At the same time, even if the circuit adds a compensation capacitor and an output capacitor, it occupies a smaller area in the same type of circuit.

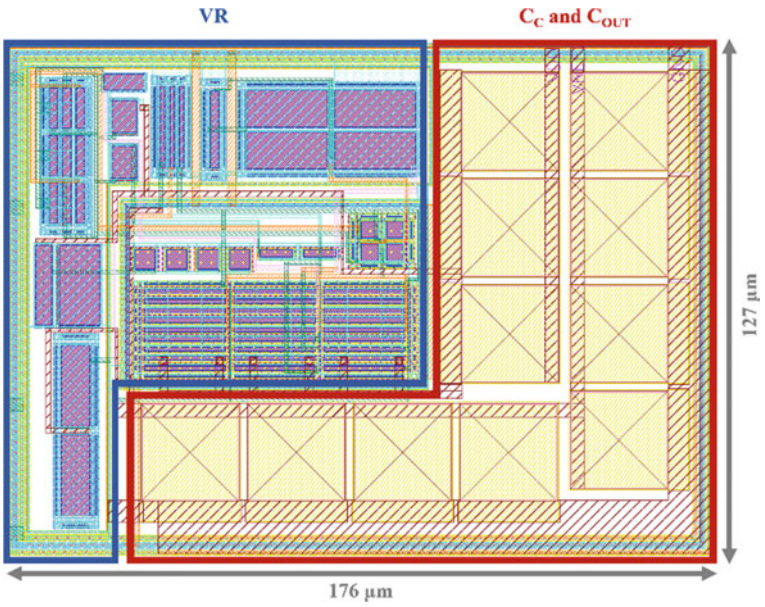

Fig. 2 Layout of the proposed reference

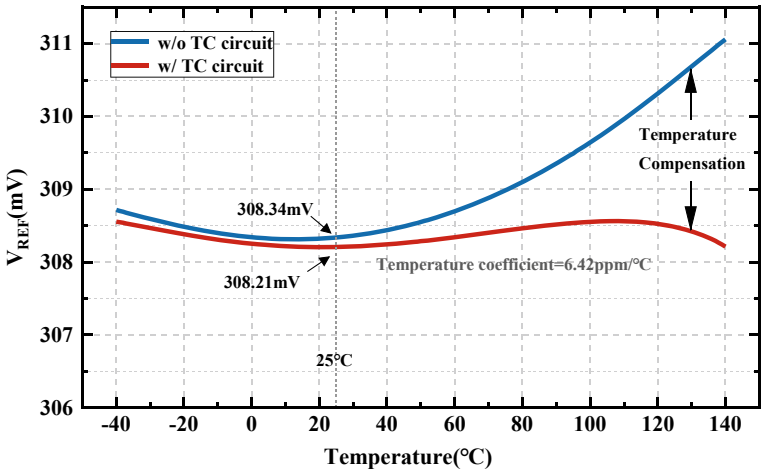

Fig. 3 Comparison of simulated V_{REF} with and without temperature compensation circuit

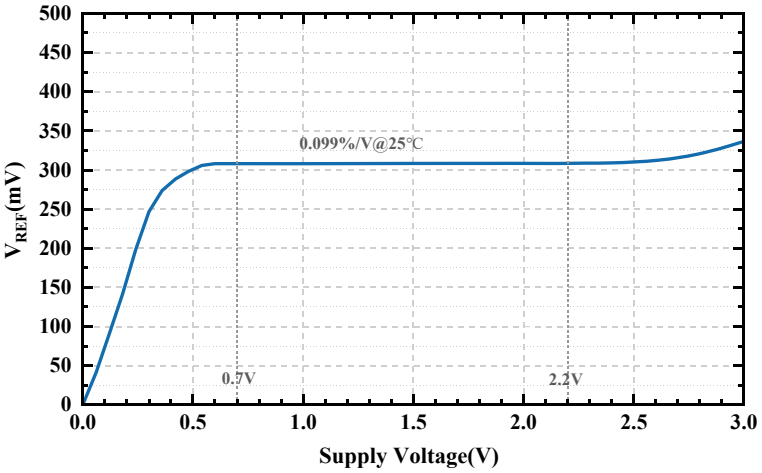

Fig. 4 Post-simulation of LS of the proposed circuit at room temperature

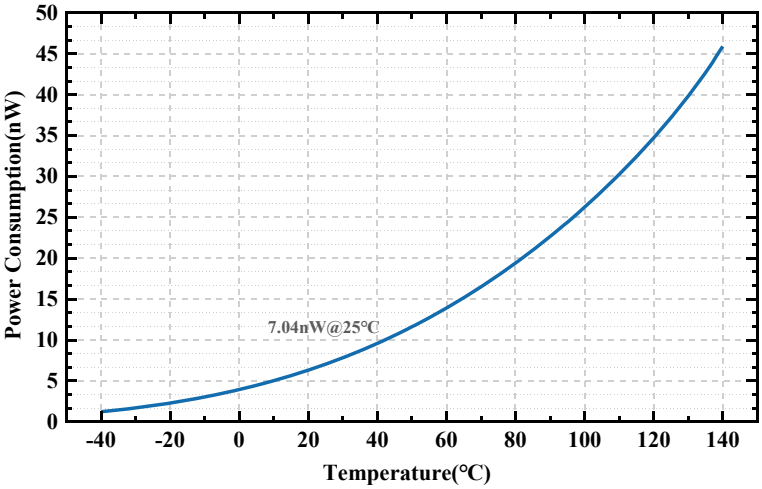

Fig. 5 Post-simulated power consumption at different temperatures

4 Conclusion

This paper presents a subthreshold voltage reference circuit with an efficient temperature coefficient compensation. The voltage reference is generated by two NMOS transistors with different threshold voltages to preliminarily offset of low-order temperature coefficient. A simple and low-power temperature compensation circuit is employed to further enhance its temperature performance and range. The circuit is fabricated in a 0.18-μm CMOS process. A theoretical analysis has been conducted.

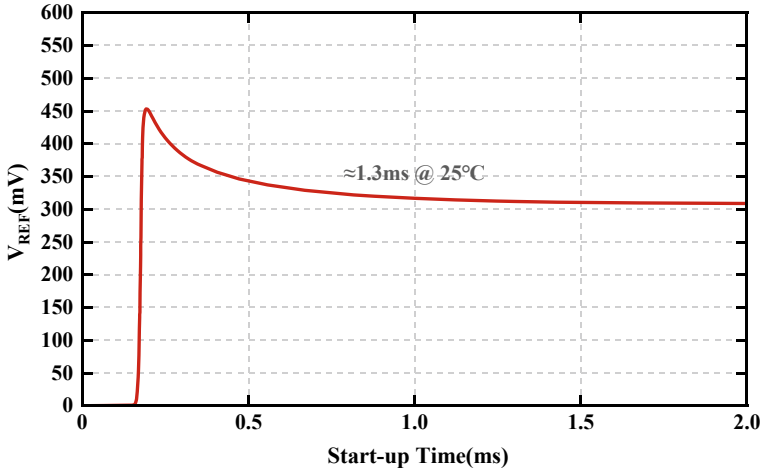

Fig. 6 Post-simulated start-up time at room temperature

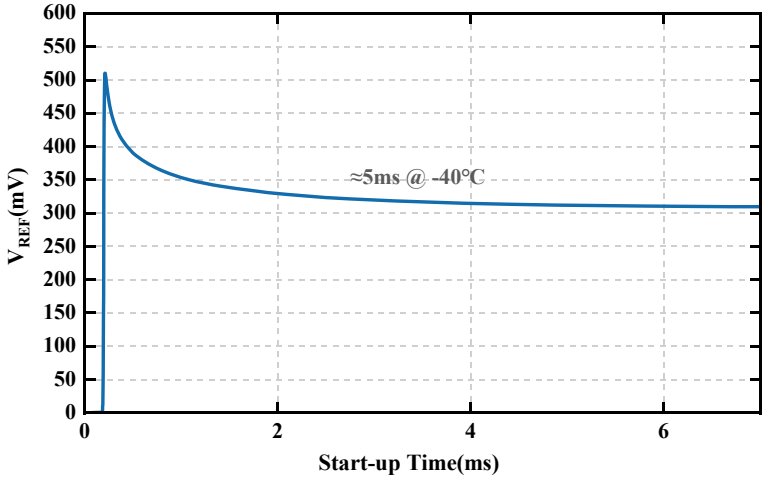

Fig. 7 Post-simulated start-up time at −40 °C

Post-layout simulation results demonstrate that, even under significant variations in power supply voltage and temperature conditions, the circuit maintains a relatively stable voltage output. Additionally, the power consumption of this circuit is very low, which has advantages compared to similar circuits. In conclusion, this circuit offers a practical solution for low-voltage, low-power IoT sensor applications.

Table 1 Performance summary and comparison with other works

	This work [a]	JSSC' 2021 [7][b]	TCASII' 2018 [6][b]	ISCAS' 2022 [8][c]	ISCAS '2020 [9][b]	JSSC' 2013 [10][b]	TCASII'2018 [11][b]
Technology (nm)	180	180	180	130	180	180	180
Type	CMOS	CMOS	CMOS	Sub-BGR	Sub-BGR	Sub-BGR	CMOS
Supply Voltage (V)	0.7–2.2	0.9–1.8	0.4–1.8	0.9	0.65	0.7–1.8	0.6–2.0
Power (nW)	7.04	1.8	9.6	30	1	52.5	30.5
V_{REF}(mV)	308.21	261	210	474	260	548	218.3
Temp. Range (°C)	–40 ~ 140	–40 ~ 130	−40 ~ 140	−20 ~ 80	−50 ~ 85	–40 ~ 120	−40 ~ 125
TC (ppm/°C)	6.42	62	82	19	95	114	23.5
LS (%/V)	0.099	0.013	0.027	0.1	0.23	N/A	0.4
1% Settling Time (ms)	1.3	0.2	N/A	N/A	N/A	6	N/A
Area (mm^2)	0.022	0.005	0.021	0.04	0.075	0.0246	0.075

[a] Post-simulation results. [b] Measured results. [c] Simulation results

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