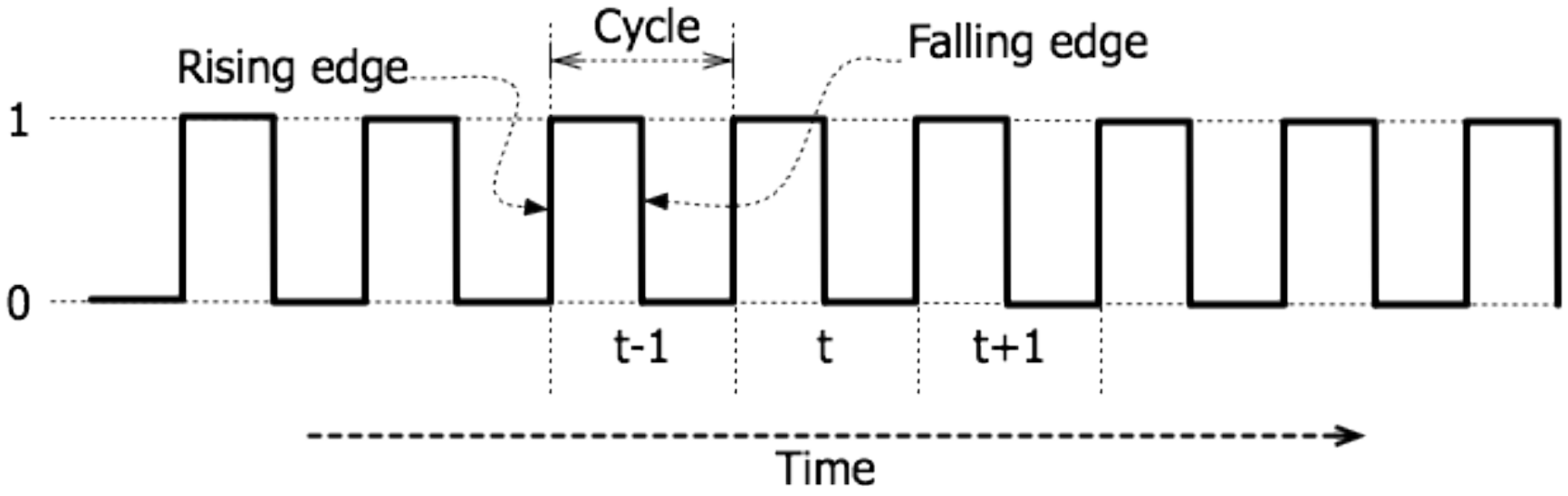
Sequential Logic Circuits

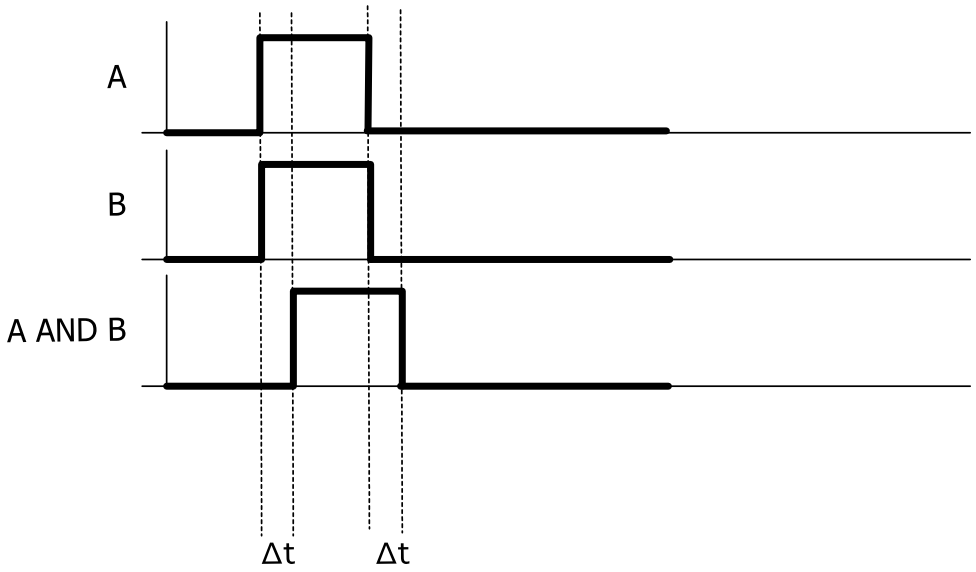
Hyunok Oh

Clock



Gate Delay

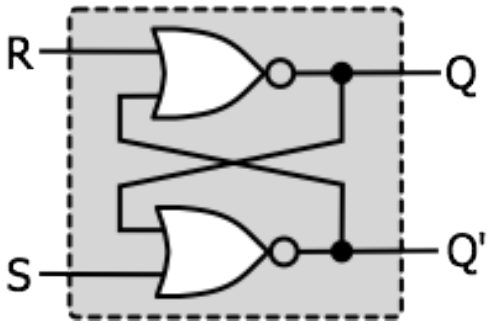
- propagation delay

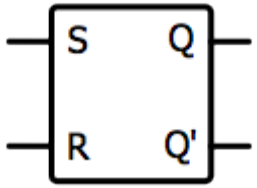


SR Latch

- **1 bit store**
  - Output is not defined when inputs are 1
  - Output is feedback to input
  - As input changes, output changes

S	R	Q
0	0	Q_{prev} (no change)
0	1	0
1	0	1
1	1	Undefined

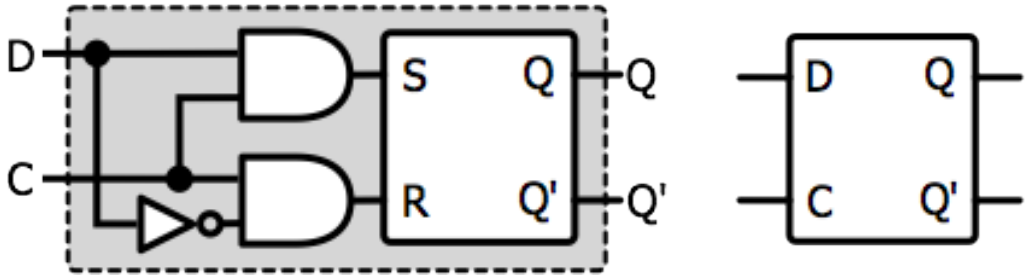




D Latch

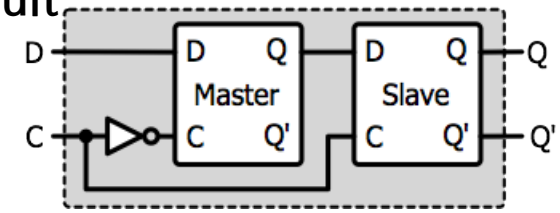
- When C=0, no output changes
- When C=1, output changes as input D changes

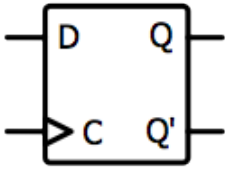
C	D	Q
0	X	Q_{prev} (no change)
1	0	0
1	1	1

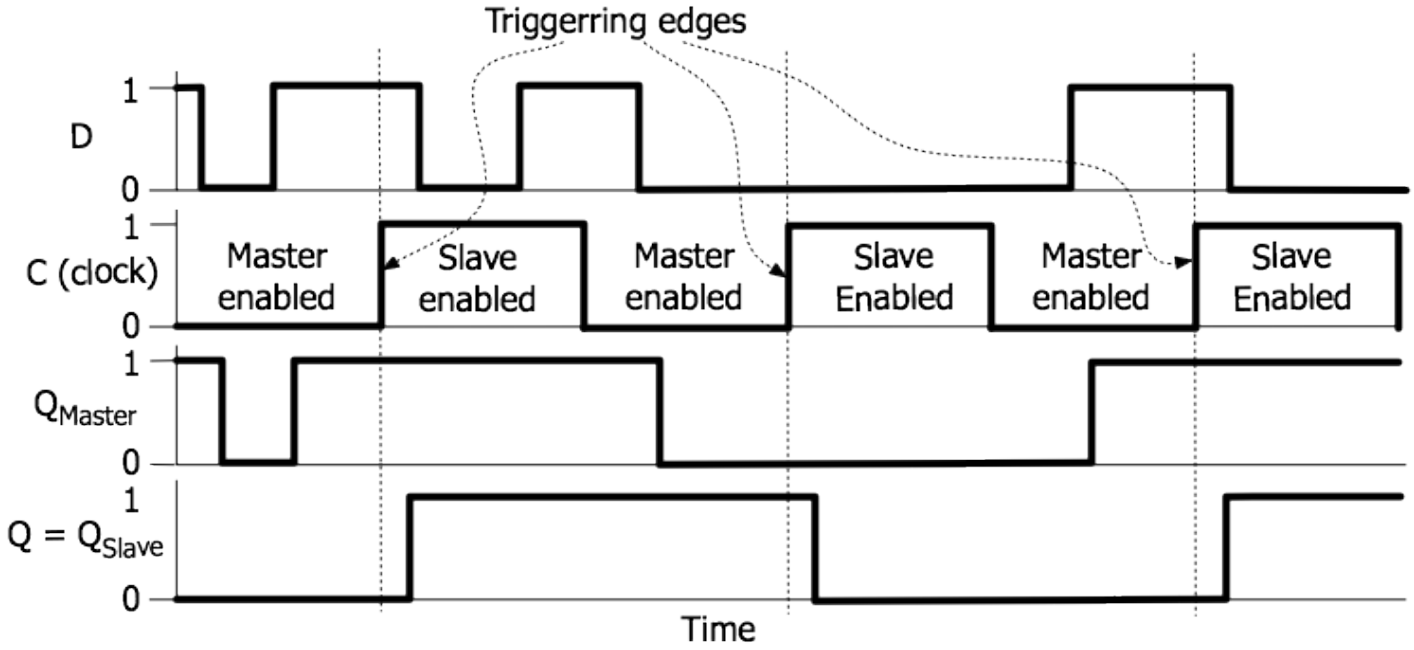


D Flipflop

- **When clock is rising to 1, input is reflected in the circuit**
  - Consider the small propagation delay

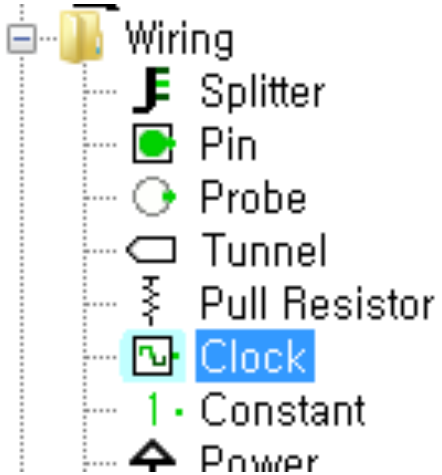


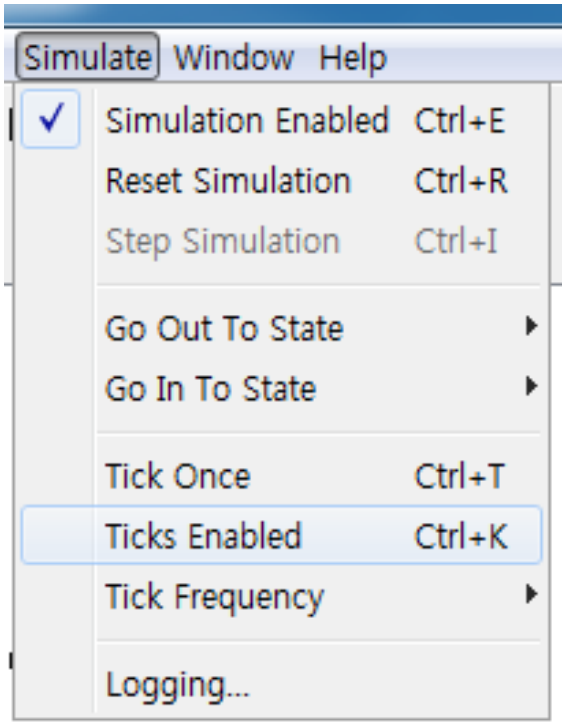




Clock in Logisim

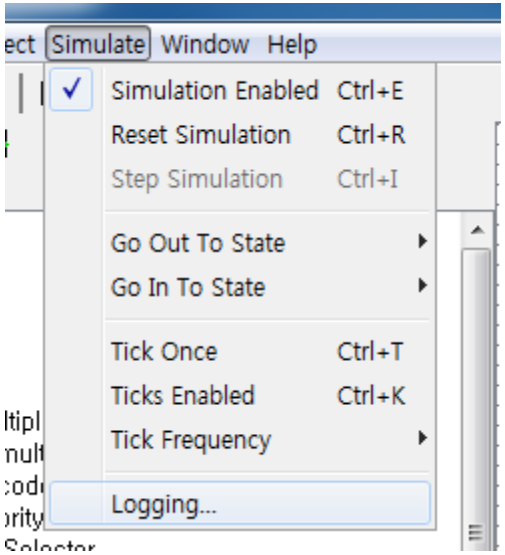
- You can enable the clock and change clock frequency

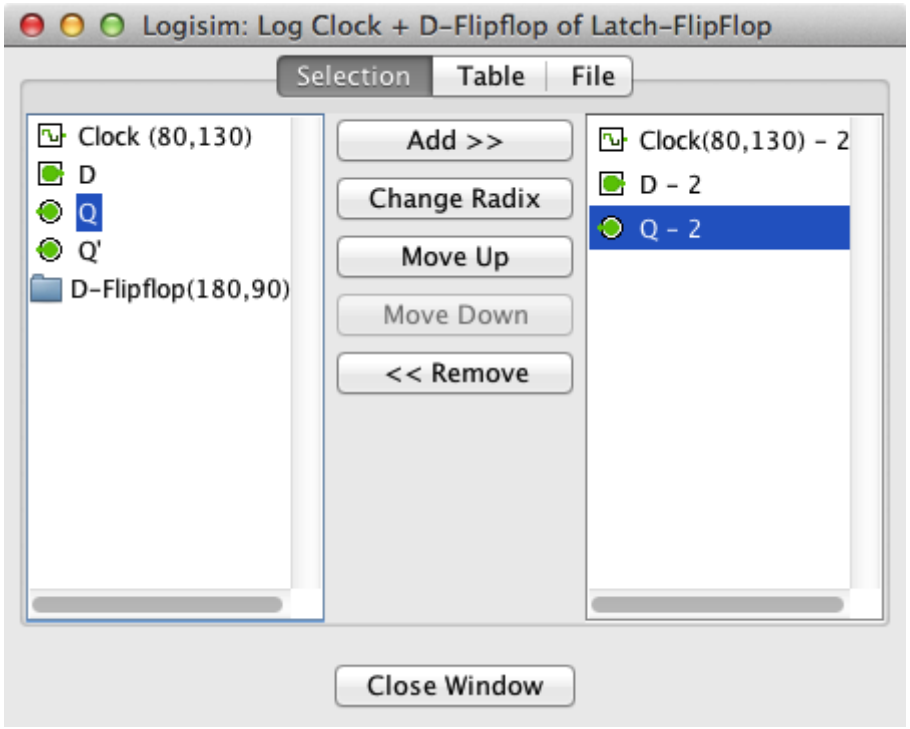




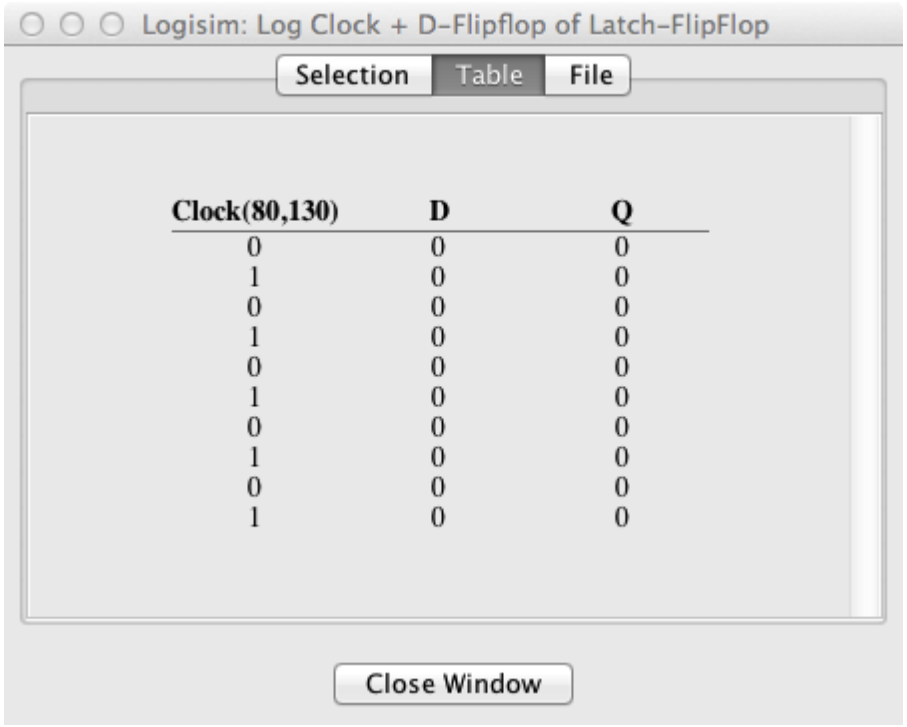
Logging in Logisim

- You can track input and output using logging module





- ‘Table’ tab shows the tracked values
- The logging results can be stored in a file



Logisim 실습

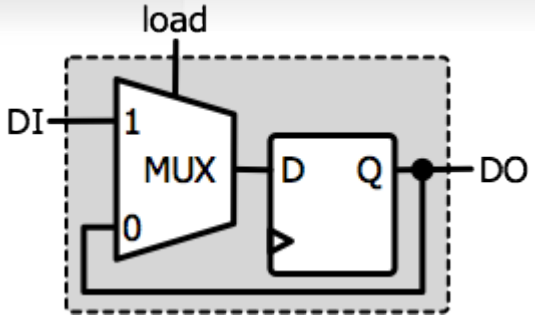
- Load sequential.circ in logisim, and verify the functionality of SR latch, D latch and D flipflop

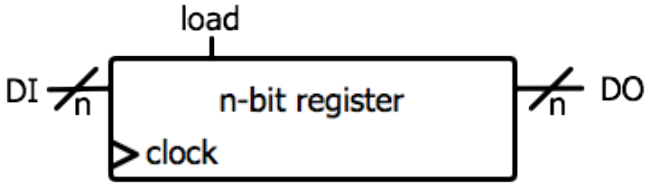
- Check the output of D flipflop after connecting a clock to D flipflop.

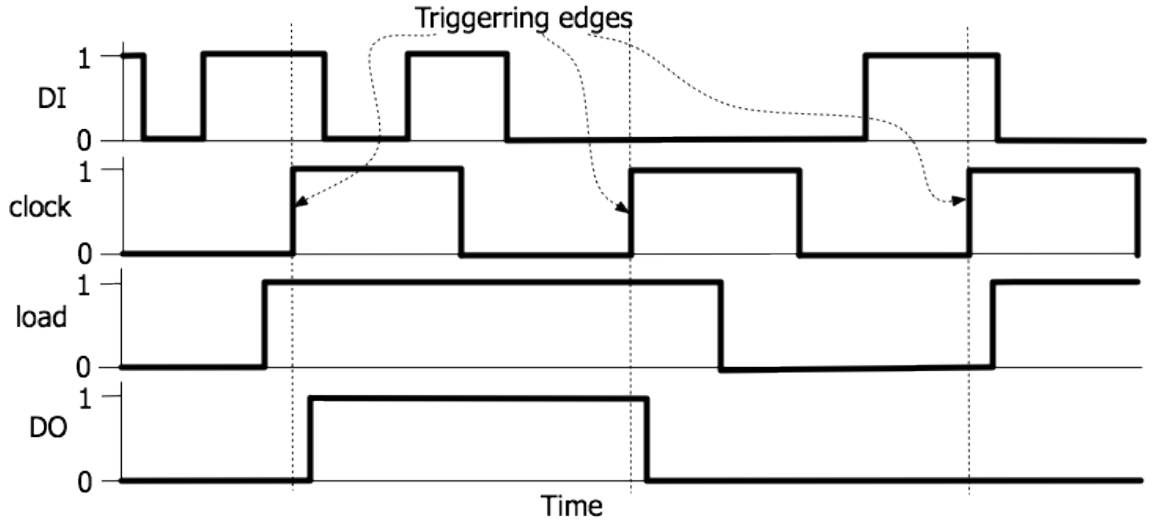
Register

- a storage to store a binary
  - a set of flipflops

- When **Load=1 and clock is rising, input is loaded into the register and the stored value is produced.**



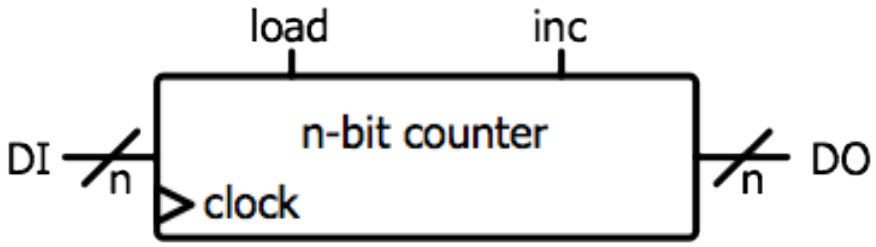


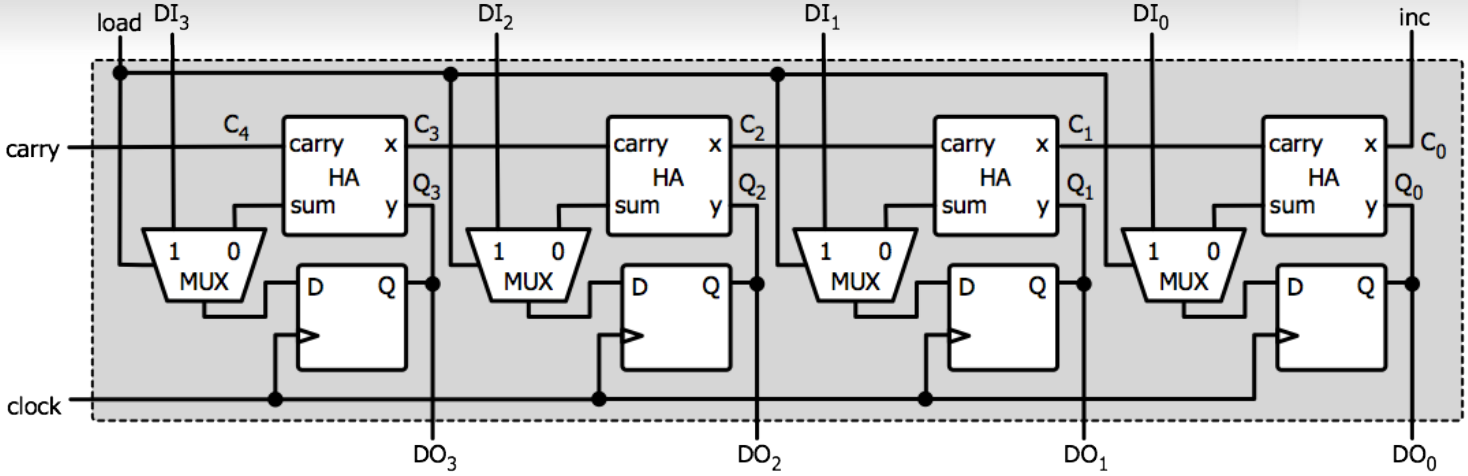


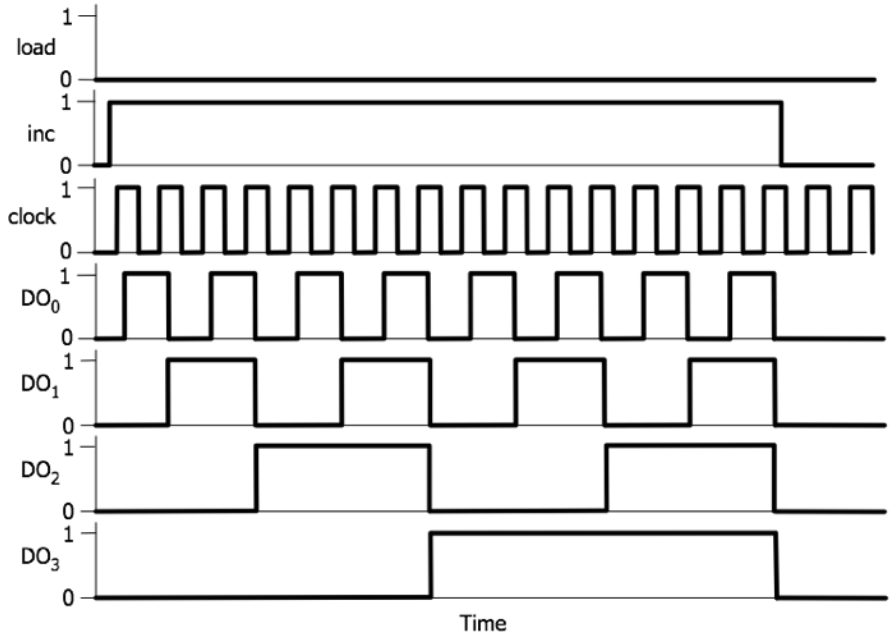
Logisim Lab

- Load sequential.circ in logisim and check 1-bit, 4-bit registers
- Connect a clock to 4-bit register and check the output

Binary Counter




load
DI3
DI2
DI1
DI0
inc
carry
C4
C3
C2
C1
C0
carry
x
HA
sum
y
Q3
Q2
Q1
Q0
1 0
MUX
D
Q
clock
DO3
DO2
DO1
DO0

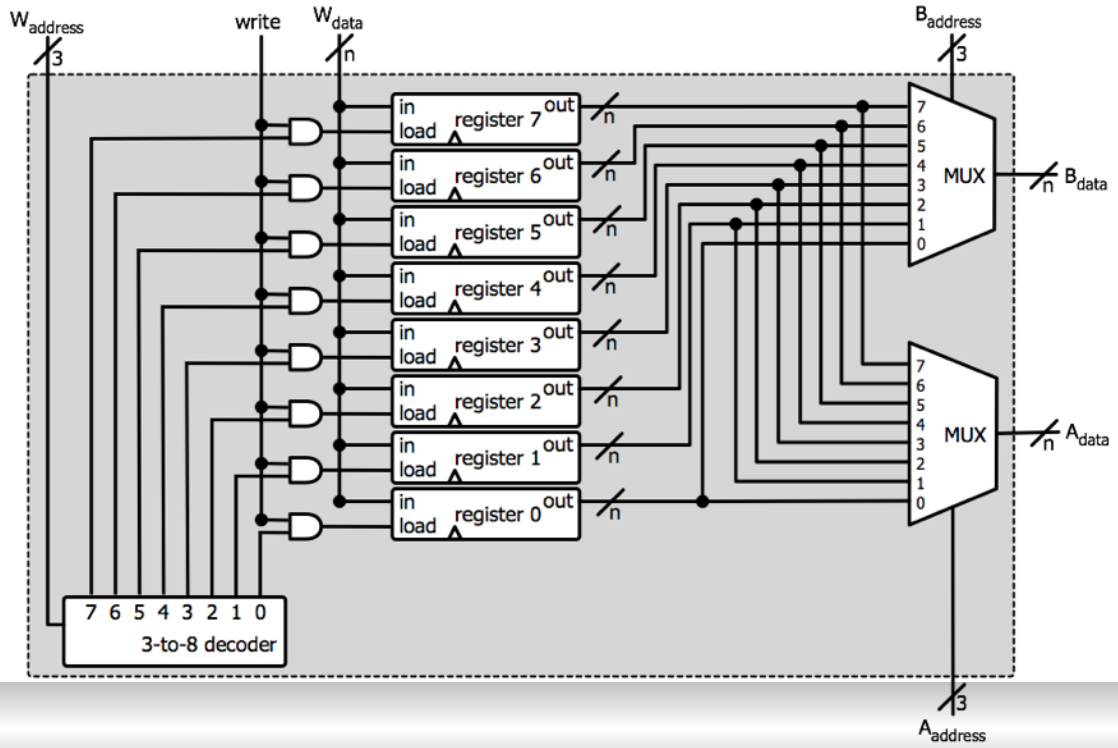

load
inc
clock
DO0
DO1
DO2
DO3
1
0
Time

Logisim Lab

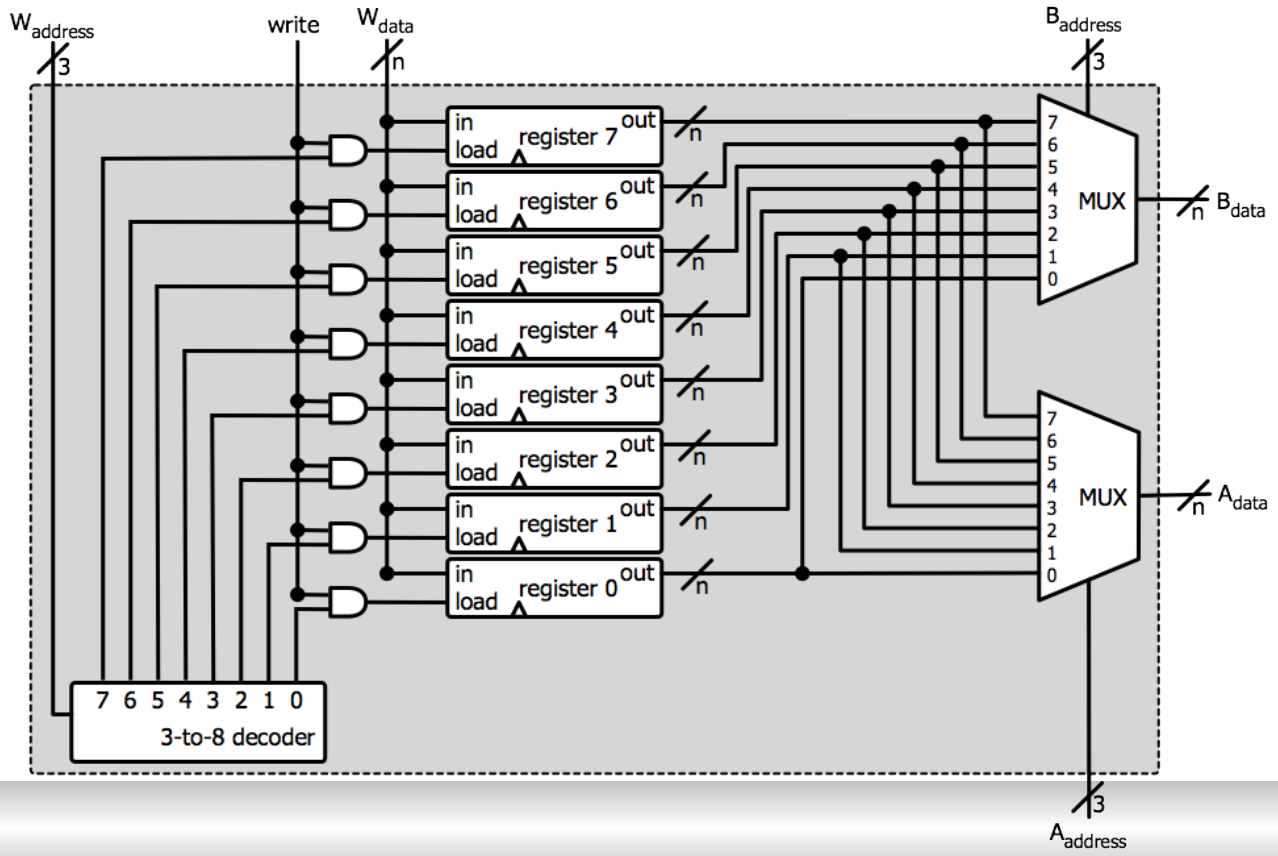
- Load sequential.circ in logisim and check 4-bit binary counter

Register File

- A set of registers in CPU
- Using register number, you can read from and write to a specific register
  - For 8 registers, 3 bits are used for register number
- For writing, give $W_{address}$ and set write=1
- Data is provided through W_{data}



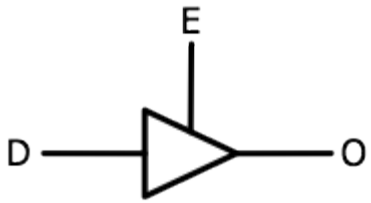
- For reading, two n bits A_{data}, B_{data} are output values $A_{address}$ and $B_{address}$ are register number



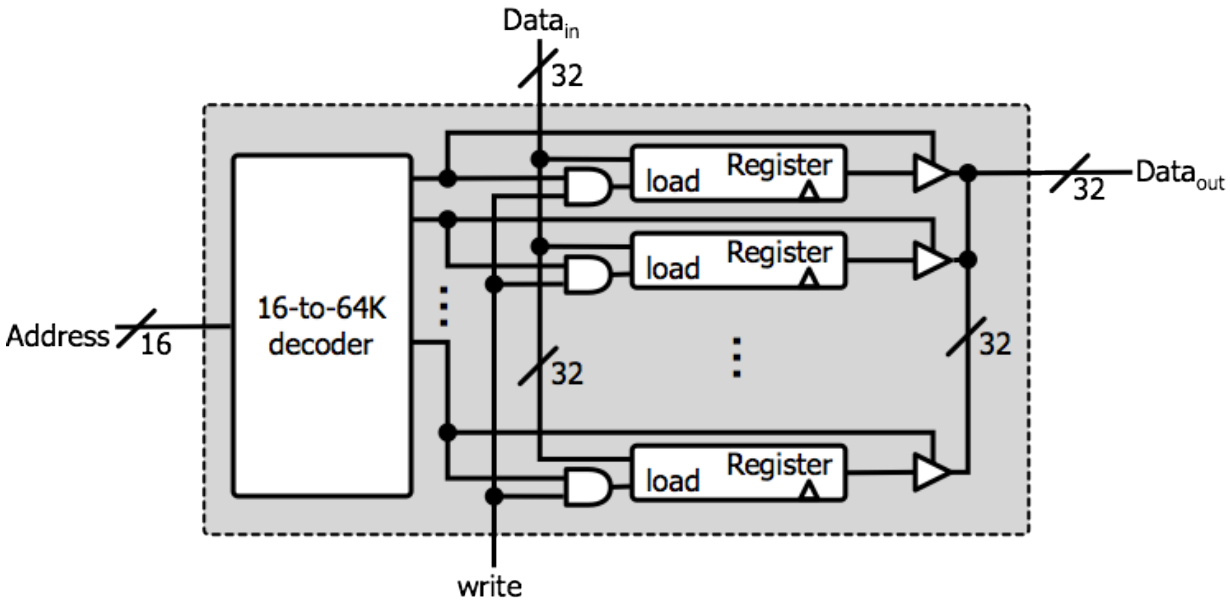
Tristate Buffer

- There are three states of 0, 1, and Hi-Z (high-impedance)
  - Hi-Z : disconnected
  - It is a switch

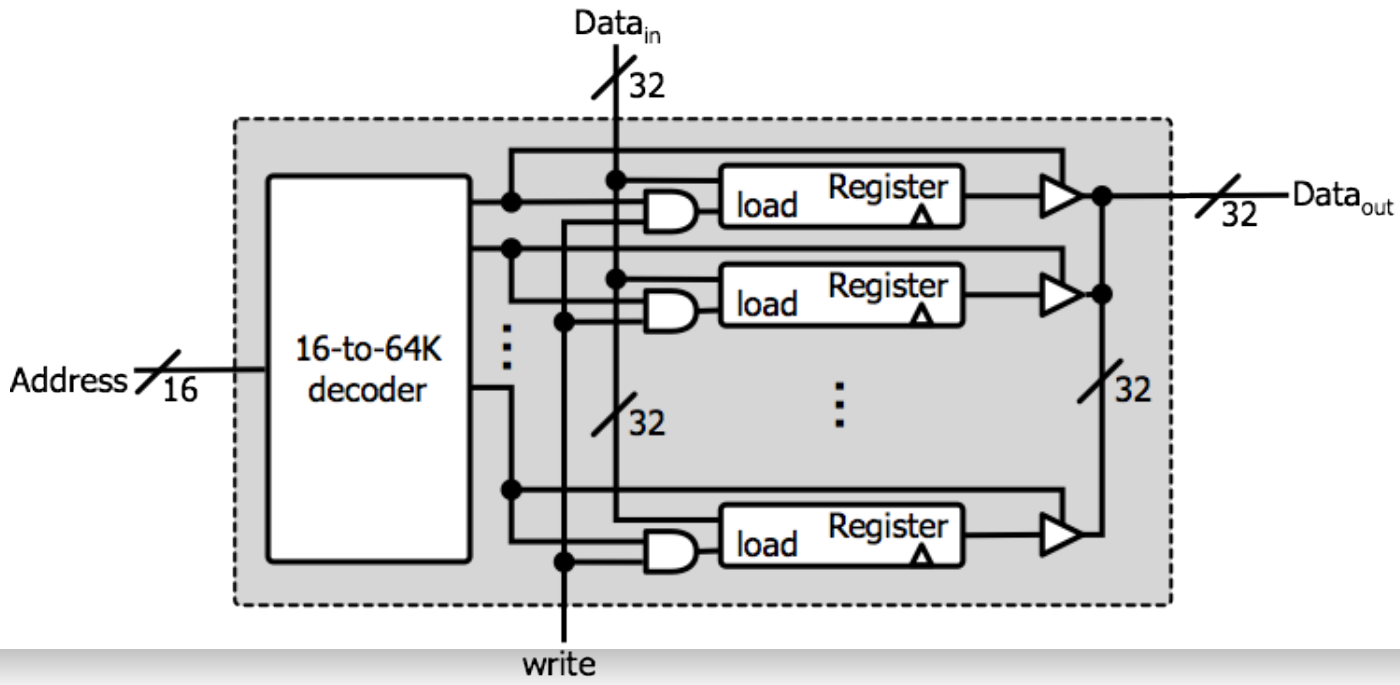
E	D	O
0	X	Hi-Z
1	0	0
1	1	0



RAM


Data$_{in}$
32
Register
load
Register
load
Register
load
Data$_{out}$
32
16-to-64K
decoder
Address
16
32
32
write

- Read (write = 0)
- Write (write = 1)



ROM

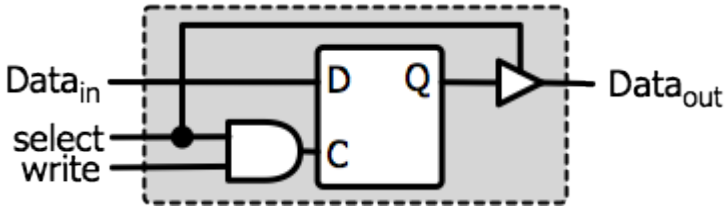
- Read-Only Memory
- non-volatile

Logisim Lab

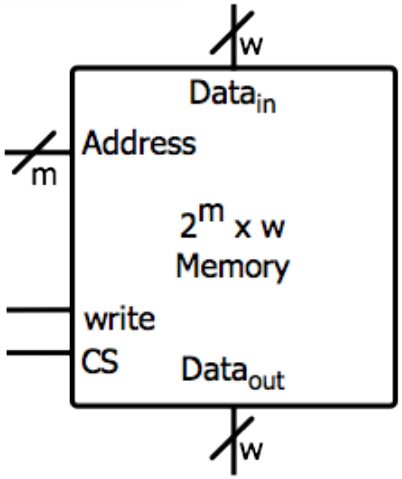
- Load sequential.circ in logisim, and check memory

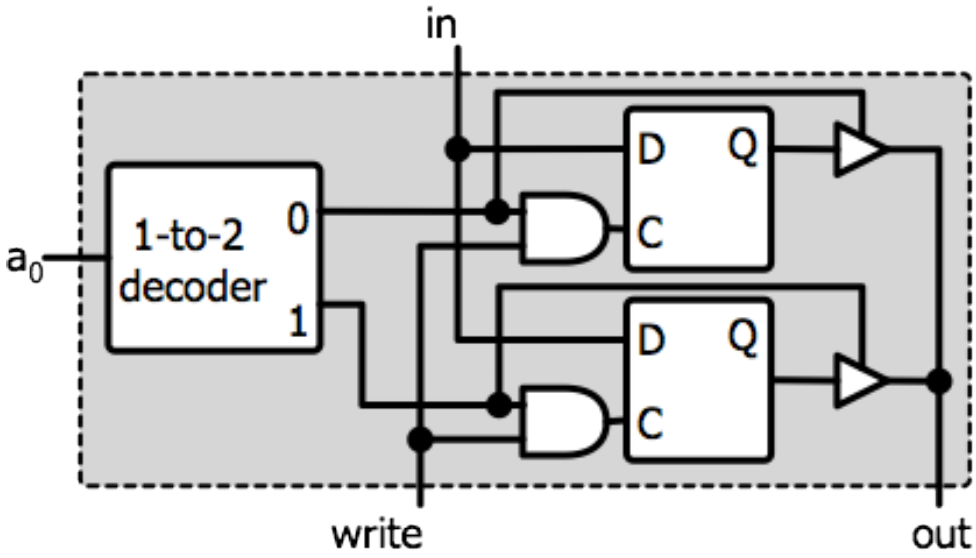
Memory Cell

- Using Select, control $Data_{out}$



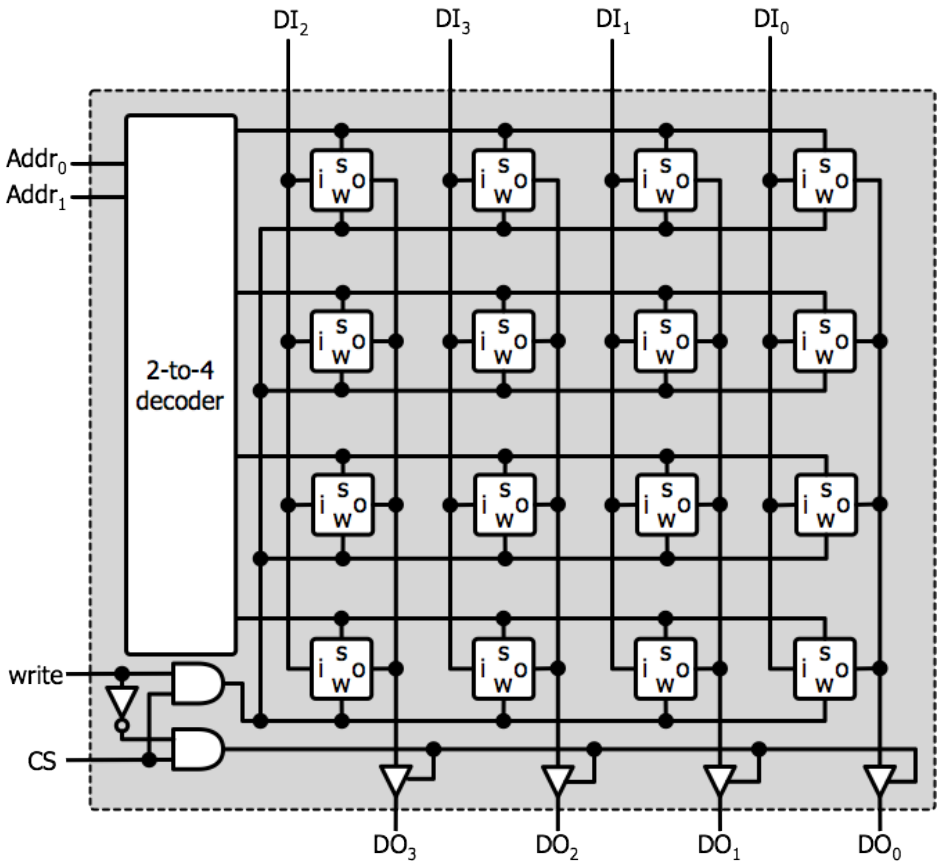
1 bit storage



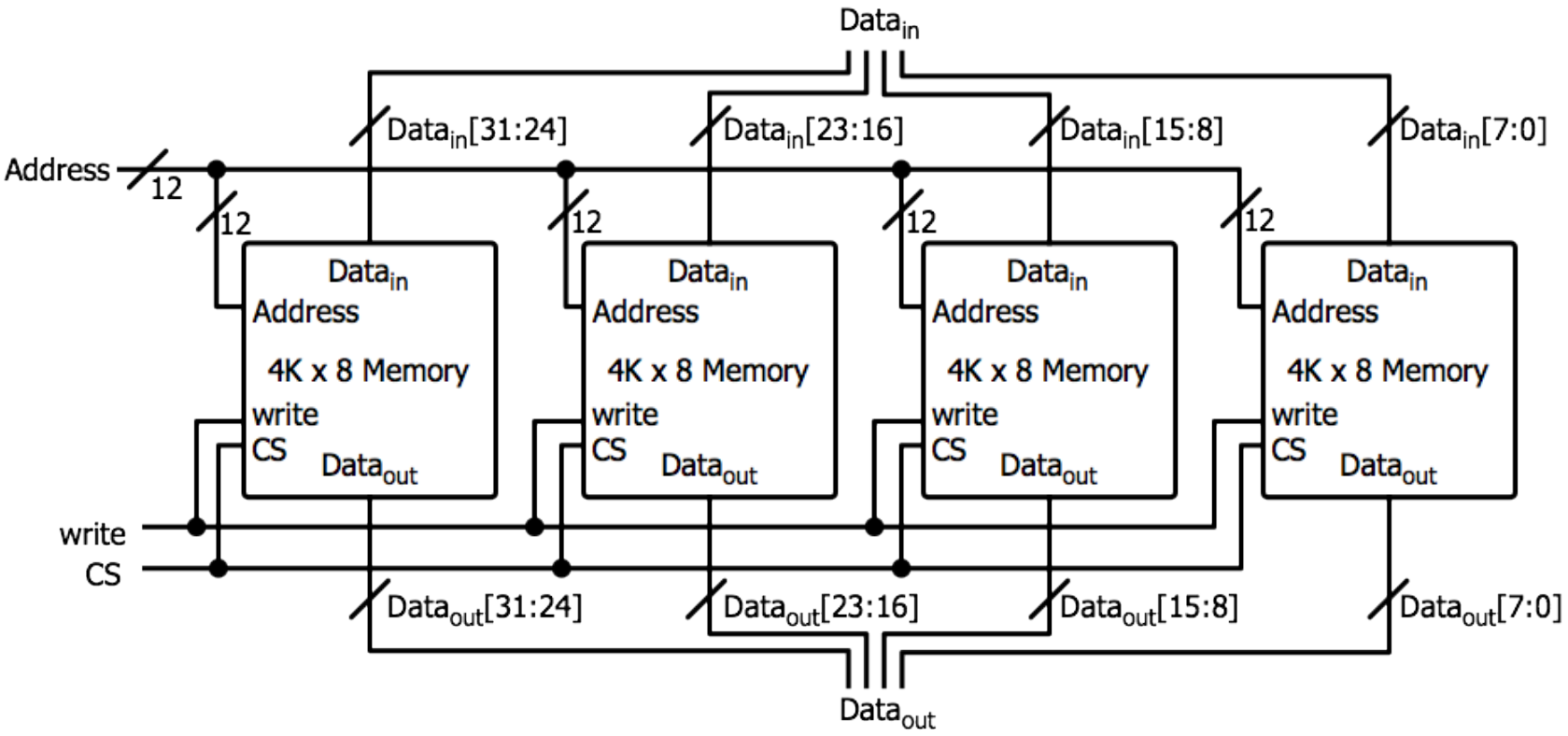


2 x 1 Memory

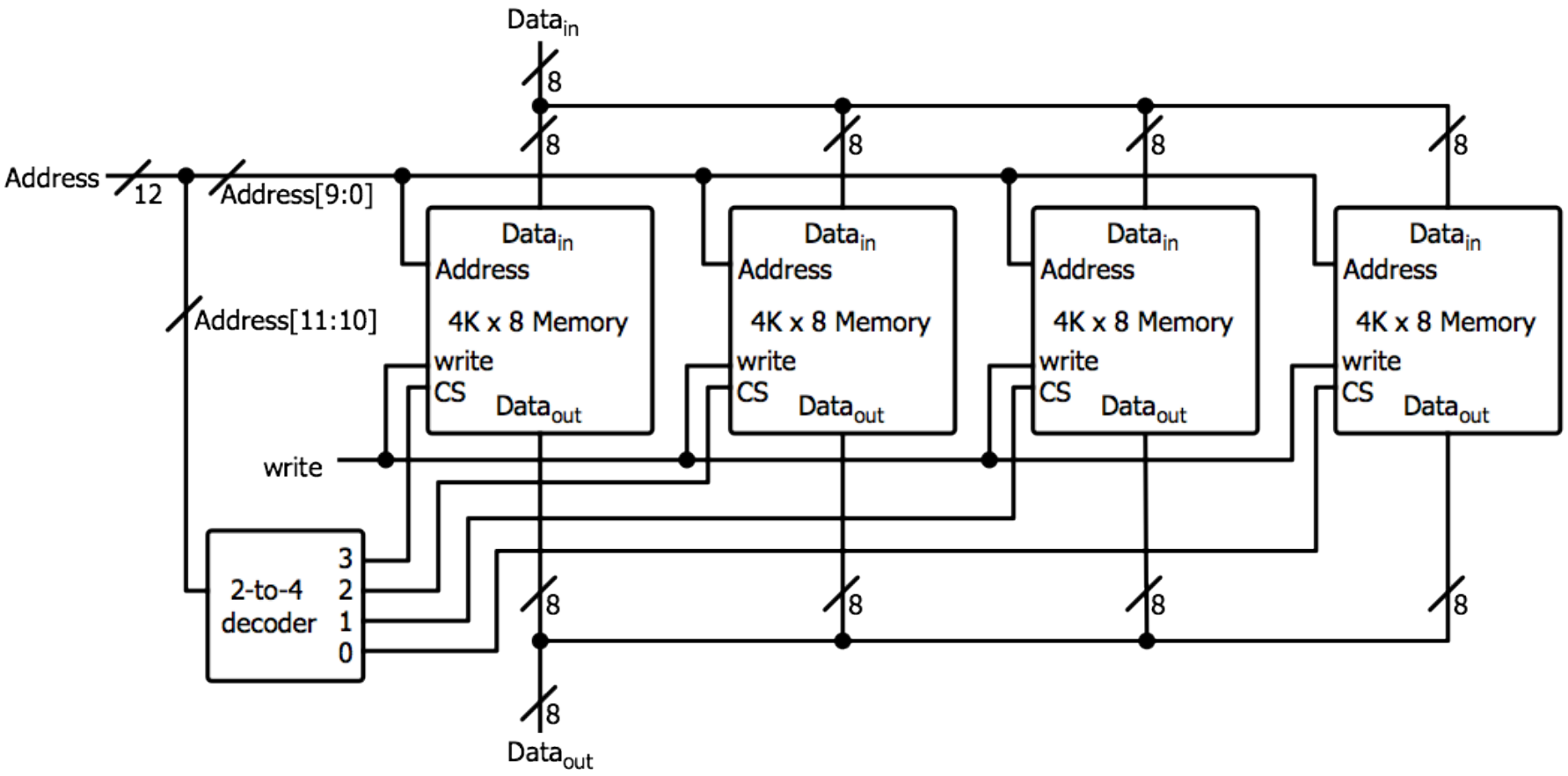
4 × 4 RAM


DI2
DI3
DI1
DI0
Addr0
Addr1
2-to-4
decoder
write
CS
DO3
DO2
DO1
DO0

Large RAM


Data$_{in}$
Data$_{in}$[31:24]
Data$_{in}$[23:16]
Data$_{in}$[15:8]
Data$_{in}$[7:0]
Address
12
12
12
12
12
Data$_{in}$
Address
4K x 8 Memory
write
CS
Data$_{out}$
Data$_{in}$
Address
4K x 8 Memory
write
CS
Data$_{out}$
Data$_{in}$
Address
4K x 8 Memory
write
CS
Data$_{out}$
Data$_{in}$
Address
4K x 8 Memory
write
CS
Data$_{out}$
write
CS
Data$_{out}$[31:24]
Data$_{out}$[23:16]
Data$_{out}$[15:8]
Data$_{out}$[7:0]
Data$_{out}$

Larger RAM


Data$_{in}$
8
8
8
8
8
Address
12
Address[9:0]
Address[11:10]
Data$_{in}$
Address
4K x 8 Memory
write
CS
Data$_{out}$
write
2-to-4
decoder
3
2
1
0
8
8
8
8
8
Data$_{out}$