Digital Pulse Width Modulator Architectures

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Abstract— **This paper presents a survey and classification of architectures for integrated circuit implementation of digital pulse-width modulators (DPWM) targeting digital control of high-frequency switching DC-DC power converters. Previously presented designs are identified as particular cases of the proposed classification. In order to optimize circuit resources in terms of occupied area and power consumption, a general architecture based on tapped delay lines is proposed, which includes segmentation of the input digital code to drive binary-weighted delay cells and thermometer-decoded unary delay cells. Integrated circuit design of a particular example of the segmented DPWM is described. The segmented DPWM prototype chip operates at 1 MHz switching frequency and has low power consumption and very small silicon area (0.07 mm^2 in a standard 0.5 micron CMOS process). Experimental results validate the functionality of the proposed segmented DPWM.**

I. INTRODUCTION

Feasibility of practical high-frequency, high-performance digital controllers for DC-DC applications has recently been demonstrated [1-3]. Based on custom architectures and microelectronic realizations of the key building blocks, including high-resolution high-frequency digital pulse-width modulators (DPWM), simplified discrete-time compensator schemes, and A/D converters, such controllers can offer the advantages of lower sensitivity to parameter variations, programmability, and reduction or elimination of external passive components, without compromising dynamic performance, simplicity or cost.

A high-frequency, high-resolution DPWM circuit is one of the critical blocks for successful practical realization of digital control for switching power converters. A high-resolution DPWM is necessary to accomplish precise voltage regulation and avoid undesirable quantization effects, such as limit-cycle oscillations [17]. Although other modulation schemes (such as sigma-delta) can be envisaged, and other control schemes with varying switching frequency (such as sliding-mode and hysteretic control) can be used, the use of constant-frequency pulse-width modulation is widespread in switching power converters. Discussions in this paper, although general in nature, are mainly limited to single-output, trailing-edge pulse width modulation. Extensions to multiple outputs or other modulation schemes are relatively simple.

In the standard analog trailing-edge pulse width modulation, an analog input signal is compared to a given carrier to provide amplitude to time domain conversion, as shown in Figure 1. The usual particular case of a linear ramp ("saw-tooth") as the carrier results in a linear relationship between the input signal and the output pulse width.

When targeting the implementation of a pulse-width modulator with a digital signal as the input, a proper means to provide the digital to time domain conversion is required, while pursuing high-frequency capability, low area, and low power consumption. Figure 2 shows a conceptual DPWM realization: instead of the carrier ramp which is used to measure the time in the analog PWM of Fig. 1, the time is quantized into a number of discrete time slots of length t_d, and a particular slot is selected by the digital control input word d. The digital comparator, which is used to select the time slot in the DPWM of Fig. 2, serves the purpose of the

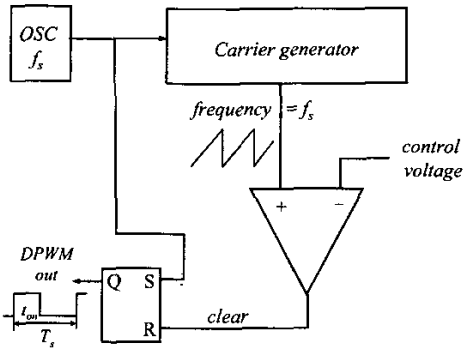

Figure 1 Conceptual block diagram of an analog PWM.

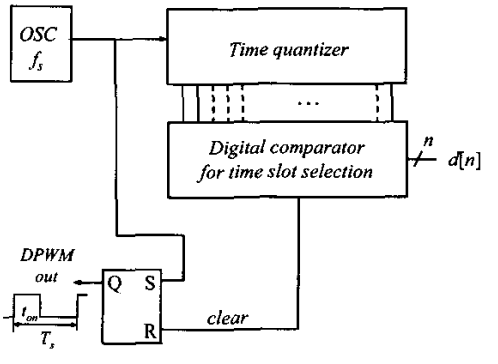

Figure 2 Conceptual block diagram of a digital PWM.

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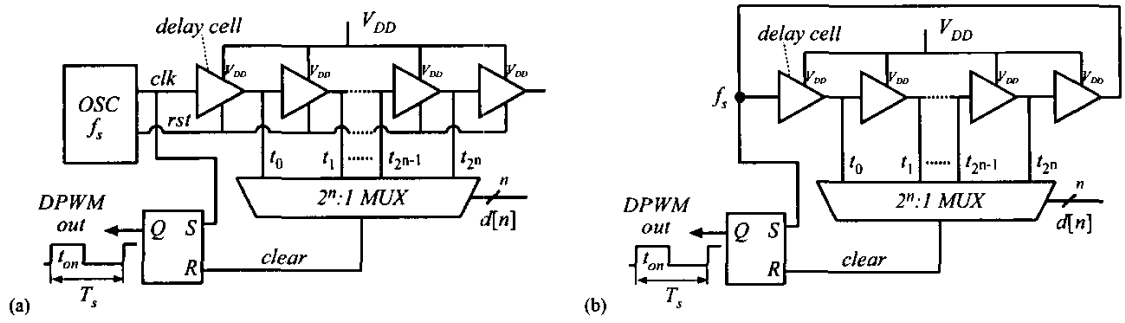

Figure 3 Delay-line based digital pulse width modulator (DPWM) architectures: (a) open-loop tapped delay line DPWM, and (b) tapped delay line DPWM forming a ring oscillator.

analog comparator in Fig. 1.

There are many possible circuit implementations of the DPWM conceptually shown in Fig. 2 [1-9, 11, 15-16], with different characteristics in terms of high-frequency capability, complexity, area, power consumption, sensitivity to process/temperature variations, linearity, etc.

In this paper, a survey and comparison of different candidate architectures implementing the DPWM block in an IC environment is presented in Section II. A novel segmented DPWM architecture is introduced in Section III. Section IV presents a comprehensive classification of DPWM architectures according to the three criteria: time quantization, selection of time slots, and frequency synchronization. Previously presented designs are identified as particular cases of the proposed classification. A DPWM integrated circuit, which has been designed as a proof of concept of the segmented architecture, is reported in Section V along with experimental results. The circuit is designed to operate at a switching frequency of 1 MHz and is well suited for a range of DC-DC applications. Conclusions of the paper are presented in Section VI.

II. Review of DPWM Architectures

The first reported method for implementing a DPWM is based on the direct digital emulation of the ramp waveform by means of a fast-clocked counter, which is loaded by the input digital code at the beginning of the cycle, and thus generating a time-varying digital code following a sawtooth signal that is compared with zero by a digital zero detector [4]. This counter-based DPWM closely follows the general block diagram of Fig. 2. An excellent linearity is achieved in the digital to time domain conversion through the use of a $2^n f_s$ clock to divide the time period $T_s = 1/f_s$ for an n-bit DPWM. For a high switching frequency f_s and a high DPWM resolution n, the need for the very high frequency clock is the main disadvantage of this approach.

A subsequently proposed architecture that circumvents the high-frequency clock problem of the counter-based DPWM is based on a tapped delay line [5], as depicted in Figure 3(a). This circuit takes advantage of the linear propagation of a given pulse from a reference clock *clk* through the delay cells connected in cascade, to select a given pulse width quantized as a function of the selected number of cells. This selection can be obtained from the digital input code by means of a 2^n to 1 multiplexer driven by the digital input code d. The multiplexer selects the signal that resets the output PWM signal, thus performing the function of selecting one of the time slots generated by the delay-line time quantizer.

The delay line in Figure 3(a) operates in an open-loop manner in the sense that the switching frequency f_s is imposed by an external oscillator, while the total delay of the line should be designed in order for the maximum delay to match the switching period. As the semiconductor material properties (and therefore the cell delay t_d) vary with process and temperature, this condition cannot be satisfied at all process/temperature corners. Consequently, the executed duty cycle D_{exec} is not always the same as the duty cycle command D_{comd} represented by the input digital signal. As an alternative, the delay line itself can be used to form a ring oscillator (Figure 3(b)), which generates the clock at the switching frequency. With this configuration, the resulting switching frequency is imposed by the delay line itself, and thus the maximum duty cycle can be guaranteed. In this case, the process/temperature variation causes a drift in the switching frequency f_s rather than affecting the executed duty cycle and duty cycle command relationship, which always remains $D_{exec} = D_{comd}$. The analog equivalent of the open-loop circuit of Figure 3(a) consists of an integrator based on a capacitor that is discharged by means of an external clock, whereas the approach of Figure 3(b) corresponds to an astable oscillator that provides the sawtooth waveform by including the switched integrator in a closed loop configuration. In order to control the cell delay, or to enable synchronization to an external clock, design guidelines for the delay-line based DPWM cells can resort to well-known techniques in the area of DLL (delay locked loops) used in communication circuits [12-14]. In that sense, the use of weak inverters to select the desired square-wave fundamental mode out of the possible frequency modes can be envisaged. Additionally, a DLL based scheme can be used to generate multiphase PWM signals [2]. Note as well that this delay oscillator might also be synchronized to an external system clock, if required. DLL technique can also be utilized in open loop delay line in order to control the cell delay and thereby force a fixed

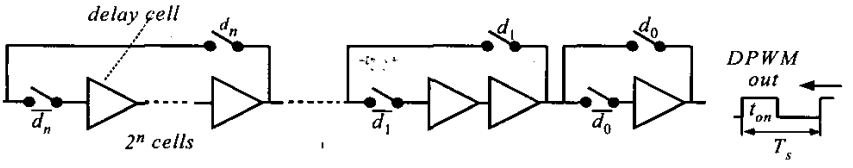

Figure 4 Binary-weighted delay-line digital pulse width modulator architecture.

relationship between D_{exec} and D_{comd}.

As far as the design of the digital delay cells composing the delay line is concerned, note that the delay of each cell depends on both its supply voltage and size, factors that directly impinge on the output current capability and the output node capacitance, and thus on the delay. This dependence provides guidelines to design the cell. Additionally, differential cells might be used to minimize noise sensitivity of delay cells to voltage supply. A reported work takes advantage of the delay dependence on the current supplying the delay cells to implement a CMOS-suited analog PWM using a plain delay-controlled line [11], that uses starved inverters [5] to limit and control the current available to charge each delay cell output node. Delay cells with the cell delay t_d inversely proportional to the input voltage have been used to construct feed-forward delay-line DPWM circuits [15, 16].

One of the disadvantages of the delay line based approach is the nonlinearity in the digital to time domain conversion, which has its origin in the cell delay mismatch due to process variations across the length of the delay line and any extra mismatched delay in the path of delay cell output to the reset terminal of the flip-flop. The most important disadvantage for this architecture is the large size required by the multiplexer in charge of gating the desired delay line tap to the flip-flop. A power and area efficient solution can be implemented by considering a hybrid counter/delay-line based design, trading-off multiplexer area versus counter clock frequency [1, 3, 6-9]. In the hybrid approach, the two cases reported so far employ either the counter with the most significant bits to provide a coarse pulse width and the finer pulse width being generated by the delay line selected by the least significant bits, or vise versa. The addition of coarse and fine pulse widths is accomplished by a series connection of the two sub-circuits. The work in [8] identifies the optimum degree of hybridation by evaluating power consumption versus distortion, since the application is a digitally controlled class-D switching power audio amplifier where linearity is very important. The THD is due to the mismatch of both characteristics, which, although individually monotonic, combine into a global characteristic with distortion.

III. SEGMENTED DPWM ARCHITECTURE

All previous delay-line based architectures require the number of unary delay cells to be proportional to the total number of quantization levels, i.e. 2^n, and hence there is the need to convert the n-bit digital code to a 2^n-bit thermometer-code version to select the proper cell in delay-based architectures (which is both area and power consuming). As the DPWM resolution (n) increases, the circuit resources required for the encoding increases exponentially, making this kind of approach less desirable for small area, low power IC applications.

An alternative approach, proposed in this paper, considers binary-weighting the delay cells so that they can be directly driven by the digital code. This architectural approach is depicted in Figure 4. In this case, the delay line is composed of cells whose delays are scaled with binary weights. The architecture considers direct use of switches driven by the digital code that either bypass or include the delay of a given binary-weighted cell in the signal path, so that the output pulse width corresponds to the expected value of the digital-to-time conversion.

Note that while the binary weighted cells can actually be implemented as a series connection of unary cells (for the sake of regularity of the integrated-circuit layout and hence matching), the required area resources of both approaches are similar as regards the delay line, but drastically reduced in the binary-weighted case due to the lack of an area-consuming multiplexer.

A disadvantage of this binary-weighted DPWM architecture is that the linearity of the digital to time domain conversion degrades to an extent that even the monotonicity is not inherently guaranteed by the architecture itself, as is the case with thermometer-decoded unary cells. In fact, as the number of bits increases, it becomes increasingly difficult to guarantee monotonicity because of the large layout area in which the cells are spread out. A certain matching between cells has to be provided to achieve a given linearity performance, requiring statistical analysis. It can be noted that similar binary-weighted architectures are used in Nyquist-rate current-steering D/A converters [10].

In order to leverage the advantages of the thermometer code approach (the inherent linearity), while obtaining a small area, a compromise can be obtained by the segmentation. Therefore, in order to trade-off resources versus performance, a segmented architecture, depicted in Figure 5, is proposed in this work, for which the DPWM circuit is segmented into two sub-DPWM circuits. The q most significant bits (the upper part of the segmented input code) are thermometer decoded and select from a delay line a given pulse width with 2^q time slots. The output of this first segment (with a guaranteed monotonic characteristic) is connected in series with a binary-weighted group of cells driven by the n-q least significant bits. The cascade connection of the two sub-circuits results in time addition and hence the final pulse width is selectable with the resolution provided by the n-bit input code.

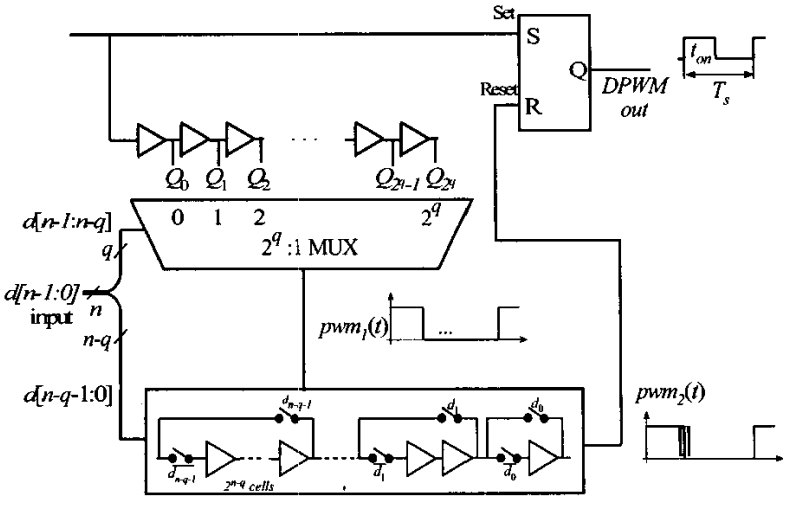

Figure 5 Segmented digital pulse width modulator architecture.

IV. DPWM CLASSIFICATION

The survey of DPWM architectures done so far, and the discussions made therein, enable us to put forward the following thesis for a comprehensive classification of DPWM realizations. There are two basic processes that occur in a DPWM performing digital to time domain conversion for a given n-bit digital input code, as shown in the conceptual diagram of Fig. 2. These are the *time quantization* and the *selection of time slots*. The first process divides the switching period T_s into 2^n slots using either a delay line or through a fast clock of $2^n f_s$ frequency. The second process selects the proper time slot by either tapping the desired delay cell or by comparing the counter output to the digital code. Apart from these, the DPWM may also be categorized according to frequency synchronization. This leads us to a classification based on the following three criteria.

A. Time quantization scheme

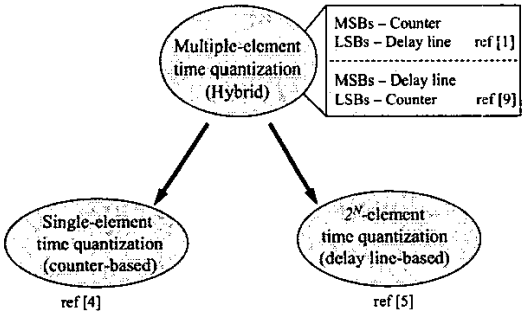

Figure 6 Classification of the DPWM according to the time quantization scheme.

For an n bit DPWM, the total switching period T_s can be quantized into 2^n slots using a variety of possible schemes. On one extreme end is the case when a single element is used to measure each of these slots as is the situation with the counter-based DPWM. The other extreme is when each slot is measured using an individual element dedicated to that slot. The pure delay-line based approach is an example of this category. In between these two extremes, many choices exist with varying number of elements for the time quantization, and fall under the category of hybrid approach. For the classification purpose with respect to the time quantization scheme, the hybrid structure can be considered the most generalized case, whereas the counter based and the delay-line based approaches are the special cases. Figure 6 elaborates the classification according to the time quantization scheme.

B. Selection of time slots

Once the switching period T_s is quantized, the next step is the selection of a time slot. Again the possibilities are numerous; the selection of time slot using a thermometer code (Figure 2) or a binary code (Figure 4) or a combination of the two in the segmented approach (Figure 5) being the particular examples. Similar to the classification of Section *A*, in the top-down approach, this classification has the segmented scheme as the most general approach, and then the two special cases are the thermometer code and the binary weighted code. The segmented design itself can have many different possible structures. The number of segments can vary from a minimum of two (as shown in Fig. 5) to any number allowed by the size of the DPWM. Furthermore it can have the thermometer code as MSBs while employing the binary code for LSBs or vice versa in the case of 2-segment architectures and many more possibilities exist in multiple-segment architectures. It should be noted that the approach of Fig. 5, where the MSBs are realized using the

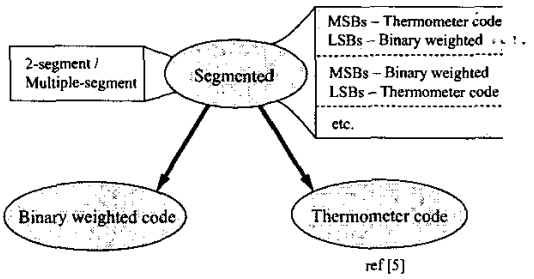

Figure 7 Classification of the DPWM according to the selection of time slots.

thermometer code is preferred for improved linearity. The classification according to the time-slot selection scheme is shown in Figure 7. Note that different designs perform differently with respect to area/power, linearity, complexity of design etc., as discussed earlier.

C. *Frequency synchronization*

Here the DPWM is classified into two categories:

- Open loop, $2^n t_d \neq T_s$
- Closed loop, $2^n t_d = T_s$

The first category (open loop) is the case when the DPWM time slot t_d is independent of the switching frequency f_s and the second (closed loop) is the situation when the two are related by a fixed ratio. Delay line based *open loop design* is an example of the first category where time slots are equal to the cell delay t_d whereas f_s is externally imposed, and owing to process variations, is not related to t_d according to a constant ratio. Delay-line operating as a *ring oscillator* constitutes an example for the second category where the switching frequency f_s is determined by the DPWM itself and hence always has a fixed relationship with t_d. Similar examples can be constructed in the counter-based design where in one case the counter clock is independent of f_s and in another case the two are related by a fixed ratio.

As discussed in Section II, delay-locked-loop (DLL) techniques can be used to control the cell delay t_d, or to enable synchronization of a closed-loop DPWM to an external clock.

V. IC IMPLEMENTATION OF A SEGMENTED DPWM

In order to validate the proposed segmented architecture, a particular 6-bit proof-of-concept DPWM IC was designed and fabricated [15]. The design considers segmentation of the input digital code in three segments.

The segmented structure of the DPWM is shown in Figure 8: a positive edge of the square wave clock after passing through a *delay compensation unit* sets the SR flip-flop, which starts the output pulse. Simultaneously, the clock starts propagating through a series of delay cells: unit cell → sixteen cells → sixteen cells → sixteen cells → dummy cell. According to the values of the bits D_5 and D_4, one of the taps in the delay line of segment-3 is selected, and the rising edge of the signal at that tap passes through the 4 to 1 multiplexer to the next segment. At this stage again a similar transfer of the signal occurs through the selection of the desired tap. Finally the positive edge of the signal resets the SR flip-flop marking the end of the output pulse. The length of the path for the signal through the segmented structure is determined by the inputs bits D_5-D_0 to the input digital word to the DPWM The presence of an extra delay cell at the beginning of each of the segmented

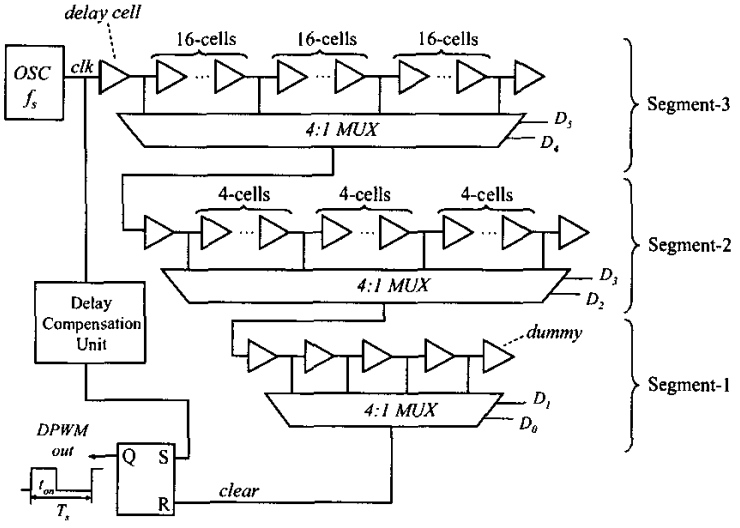

Figure 8 Block diagram of the segmented DPWM integrated circuit prototype.

Table 1 Comparison of the segmented and the thermometer code experimental DPWM ICs.

IC	# of Delay cells	# of MUX cells	Area (mm^2)	Current (μA) @V_{in} =5.0V, f_{clk} = 1MHz	Routing Complexity	Linearity
Segmented	75	6	0.0675	111	Low	Poor
Thermometer-code	67	24	0.0833	132	High	Good

stage, and one dummy delay cell at the end of these stages aims to provide similar driving and loading environment to each of the delay cells in the structure. Note that due to multiplexers and extra unit cells in the beginning of each stage, a certain amount of extra delay is introduced in the path of the signal from the clock input to the *Reset* input of the SR flip-flop. This extra delay is almost constant irrespective of the D_5-D_0 selection set. To balance this extra delay, the *delay compensation unit*, which is composed of matching delay and multiplexer cells, is employed.

With the aim of comparing the segmented architecture with a plain thermometer-code design (shown in Figure 3(a)), these two versions of the DPWM were implemented on prototype ICs in a 0.5μ CMOS process. Both DPWM's are designed to operate at the switching frequency of 1 MHz. The layout of the segmented architecture is shown in Figure 9. The DPWM area is 0.07 mm^2. There is a significant area and complexity improvement in the segmented design over the plain delay-line based design. Furthermore, due to the fewer number of units in the design, power consumption is also reduced. A comparison is presented in Table 1. Figure 10(a) and (b) show experimental results of the implemented DPWMs: the measured duty ratio of the output pulse as a function of the digital command input, validating their functionality. The segmented DPWM, as expected, shows a greater degree of nonlinearity in its digital to time domain conversion. At closer inspection, it can be seen that this nonlinear character is periodic with a periodicity equal to an interval of four in the digital duty command. For closed-loop DC-DC controller applications, a degree of nonlinearity can be tolerated. Nevertheless, it is important to point out that, compared to a plain thermometer-code design, the segmented design requires a much more careful layout to ensure monotonicity.

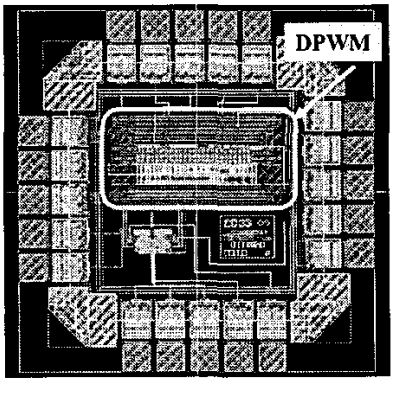

Figure 9 Layout of the segmented DPWM test chip.

VI. Conclusions

A high-frequency, high-resolution digital pulse-width modulator (DPWM) is a key component for successful realization of practical digital control for high-frequency switching power converters. This paper presents a survey and a comprehensive classification of DPWM architectures. The classification is based on three criteria: time quantization scheme, selection of time slots, and frequency synchronization. Previously presented designs are identified as particular cases of the proposed classification.

A new, segmented DPWM architecture is introduced aiming to optimize resources by segmentation of the input digital code to drive binary-weighted delay cells and thermometer-decoded unary delay cells. A particular proof-of-concept design case consisting of a three-segment six-bit DPWM integrated circuit operating at 1 MHz switching frequency, with low power consumption and very small silicon area (less than 0.07 mm^2 in a standard 0.5 μm CMOS process) is described, and experimental results are shown to validate its functionality.

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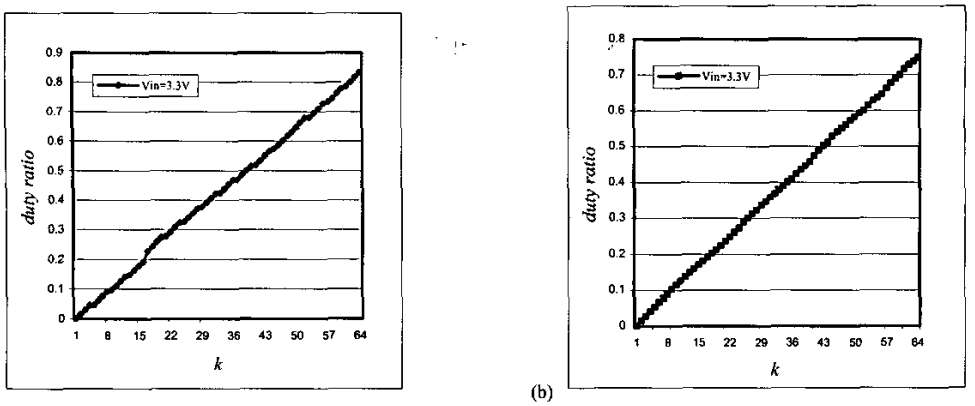

(a) (b)

Figure 10 Experimental results: measured duty ratio of the output pulse as a function of the 6-bit digital command k, for V_{in} = 3.3 V, (a) segmented DPWM IC (b) thermometer code DPWM IC.

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