Investigation of Delay Compensation Circuit Techniques to Reduce Timing Walk

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Abstract:

Two methods are investigated to reduce the timing walk for an integrated ASIC chip to less than 1 ns without requiring an off-chip delay line. In each method a delay compensation circuit is used to adjust the position of the timing marker dependent upon the size of the input signal. For signals with identical rise times a large signal will usually generate its timing pulse faster than a small signal. The first circuit is added to a monolithic constant fraction discriminator (CFD). Using one control signal based on the input signal size, an analog delay is used to delay the zero-crossing signal to the comparator for signals above a certain threshold. After analog delay compensation, the timing walk of the CFD is 660ps or 54% of the value of the CFD without analog compensation for a signal size range of 10. The second circuit is added to a simple leading-edge discriminator. The circuit uses digital delay lines, where the length of the delay is based on the size of the input signal. The timing walk is reduced by 83%, from 4.05ns (without digital compensation) to 700ps (with digital compensation) for a signal size range of 8.

I. INTRODUCTION

Accurate time placement of incoming events is very important for coincidence detection. Timing walk can be caused by both variations in the size of the signal and the rise time of the signal. This work assumes that the rise time of the signals is not varying. For PET imaging applications, valid events may have different amplitudes because of the light statistics associated with the deposited energy and because of gain differences between the front end electronics (i.e., photomultiplier tubes) of different detector modules. On the other hand, the input signals usually have similar rise times. The timing walk for PET coincidence electronics is typically 1-2 ns for a signal size range of 4.

The most common type of circuit used to achieve precise timing is the constant fraction discriminator (CFD). However, CFD timing usually requires an off-chip delay line. This makes it difficult to implement a CFD on a single ASIC chip. Tanaka and Binkley have previously reported on monolithic CFD designs [1-3] with moderate timing performance. The basic CFD timing circuit block diagram is shown in Figure 1. While the zero crossing point is relatively insensitive to signal size, the reason for the timing walk is that the generation of the timing signal depends upon the magnitude and slope of the mixed signal. Due to current limitations associated with implementing an integrated circuit, the comparator (that generates the timing signal) has limited slew rate capability. Therefore when the mixed signal is large, the comparator is able to generate the timing marker faster than when the mixed signal is small. An analog delay circuit has been designed to adjust the generation of the timing signal depending upon whether the signal is above or below a user selectable value.

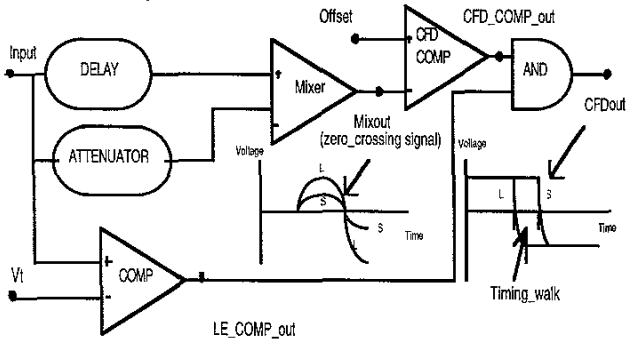

Figure 1. CFD timing circuit.

A second common type of timing circuit is the leading-edge discriminator. While not as accurate as the CFD, leading-edge discriminators are often used because they are very simple to implement. The timing walk associated with a leading-edge discriminator is illustrated in Figure 2. If both a large signal and a small signal have the same rise time, the large input signal will cross the voltage threshold sooner than the small signal. The timing difference between the largest and smallest input signals represents the maximum timing walk associated with the circuit. For example, the timing difference between a large signal (with peak value of 300mV and 10ns rise time) and a small signal (with peak value 30mV and 10ns rise time) could be as large as 1.8ns. To reduce the time walk associated with a leading-edge discriminator we have designed a circuit that selectively delays the generation of the timing pulse depending upon the relative size of the input signal.

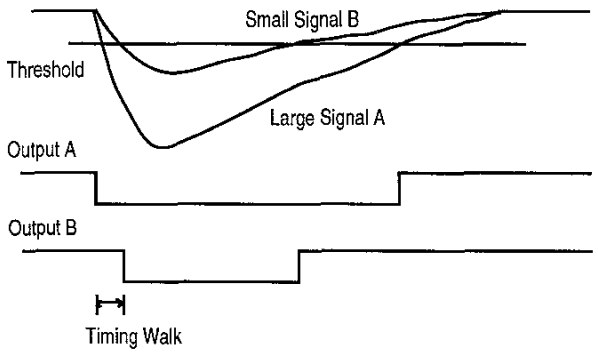

Figure 2. Timing walk for a leading-edge discriminator.

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II. ANALOG DELAY COMPENSATION FOR A CFD TIMING CIRCUIT

The basic CFD circuit block diagram is shown in Figure 3. Figure 4 shows the 'Delay and Amplifier with Compensation Circuit'. The input signal experiences three amplifier delays. At the output of the third amplifier, a 3pf capacitor, C_{walk}, is used to adjust the amount of analog delay added to the input signal. The capcitative load C_{walk} is controlled by the digital switch. When the *Walk_Control* signal is high the switch is closed. When the *Walk_Control* signal is low the switch is open. The threshold voltage of the leading-edge comparator is set to the mid-point between the slowest and the fastest anticipated signals. For signals larger than the value of $V_{timewalk}$, the *Walk_Control* signal is set high and the capacitive load delays the output signal. The delayed signal is then mixed with the original input to generate a zero-crossing signal. Figure 5 shows the zero-crossing signals for different size input signals without analog delay compensation. Figure 6 shows the zero-crossing signals for different size input signals with analog delay compensation.

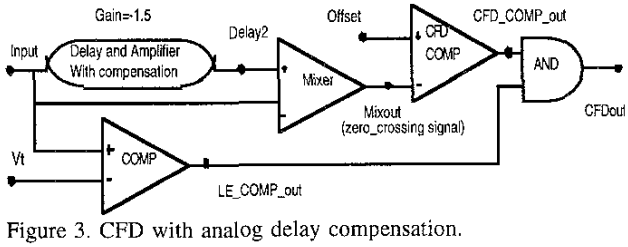

Figure 3. CFD with analog delay compensation.

The CFD comparator takes the zero-crossing signal and produces the timing signal cfdout. COMP is used to generate leading edge timing. The AND gate is used to prevent triggering on noise.

The timing output after the CFD comparator is heavily dependent on the position of the zero-crossing signal at the output of the mixer. Figure 7 shows the Hspice simulation waveform of the timing signal (cfdout) without analog compensation. Figure 8 shows the Hspice simulation waveform of the timing signal (cfdout) with analog compensation. The timing walk between the 40mV peak input signal and 400mV peak input signal is about 660ps with the analog compensation. Table 1 gives the comparison of the timing walk between the typical CFD and the CFD with analog delay compensation. The timing walk for a signal size range of 10 is reduced from **1.22ns** to **660ps**.

Table 1: Comparison of the timing walk relative to 400mV timing pulse of the CFD circuit with/without compensation

Input Signal Peak Voltage (mV)	400	320	120	80	40
Timing Walk Relative to 400mV Timing Pulse Without Compensation (ns)	0.00	-0.06	0.35	0.50	**1.16**
Timing Walk Relative to 400 mV Timing Pulse With Compensation (ns)	0.00	-0.06	0.31	**-0.35**	0.31

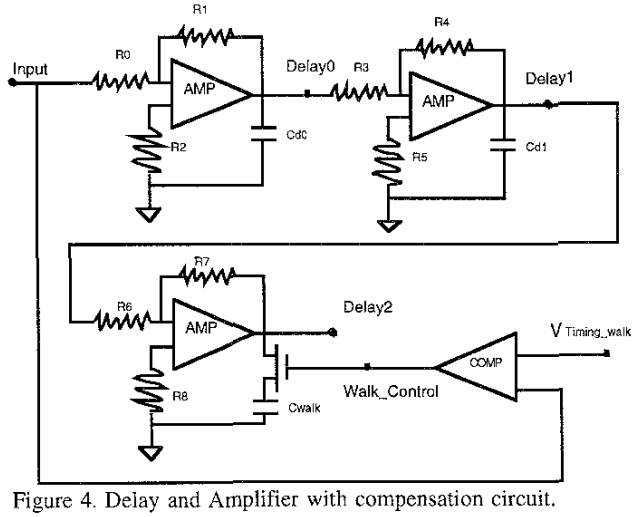

Figure 4. Delay and Amplifier with compensation circuit.

All the simulations are based on the extracted layout netlist for a CFD circuit design. The typical input is assumed to have a 10ns rising time and a 40-300 ns decay time. After analog delay compensation, the timing walk is reduced to 54% of the CFD circuit without analog delay compensation.

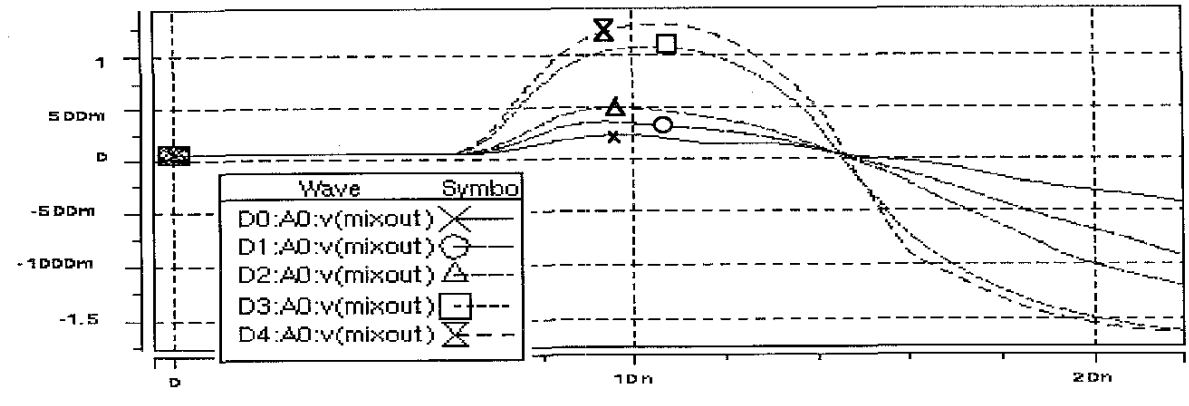

Figure 5. Hspice simulation waveforms of the mixout signals of the CFD circuit without analog delay compensation. (D0: input peak 40mV; D1: input peak 80mV; D2: input peak 120mV; D3: input peak 320mV; D4: input peak 400mV).

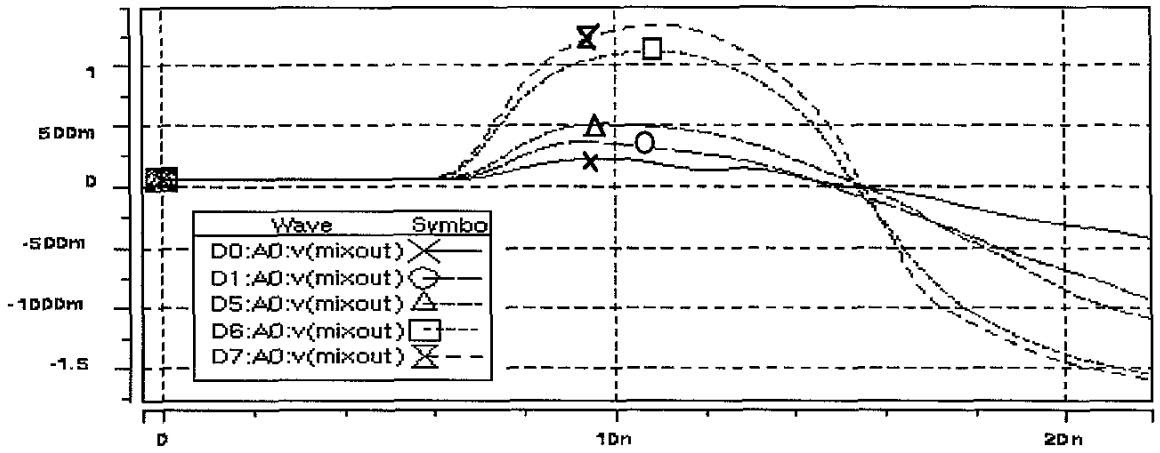

Figure 6. Hspice simulation waveforms of the mixout signals of the CFD circuit with analog delay compensation. (D0: input peak 40mV; D1: input peak 80mV; D5: input peak 120mV; D6: input peak 320mV; D7: input peak 400mV).

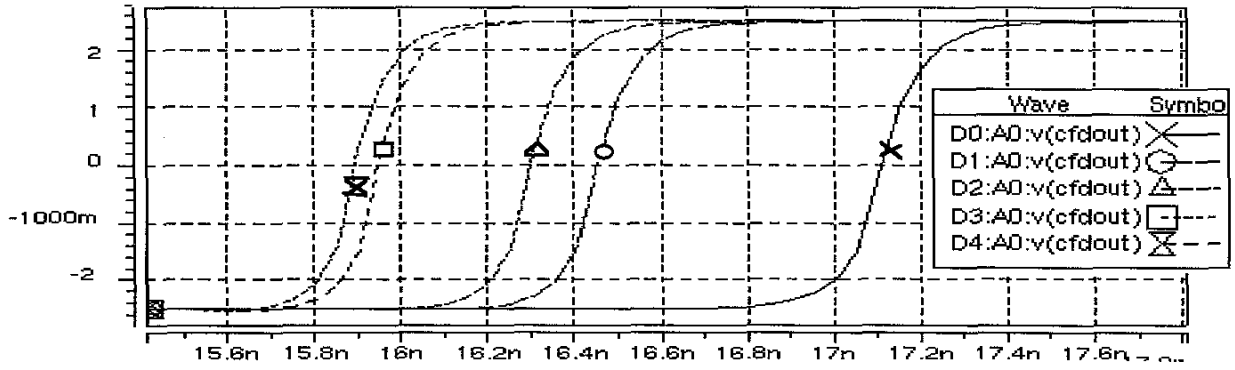

Figure 7. Hspice simulation waveforms of the CFD timing signals without analog delay compensation. (D0: input peak 40mV; D1: input peak 80mV; D2: input peak 120mV; D3: input peak 320mV; D4: input peak 400mV).

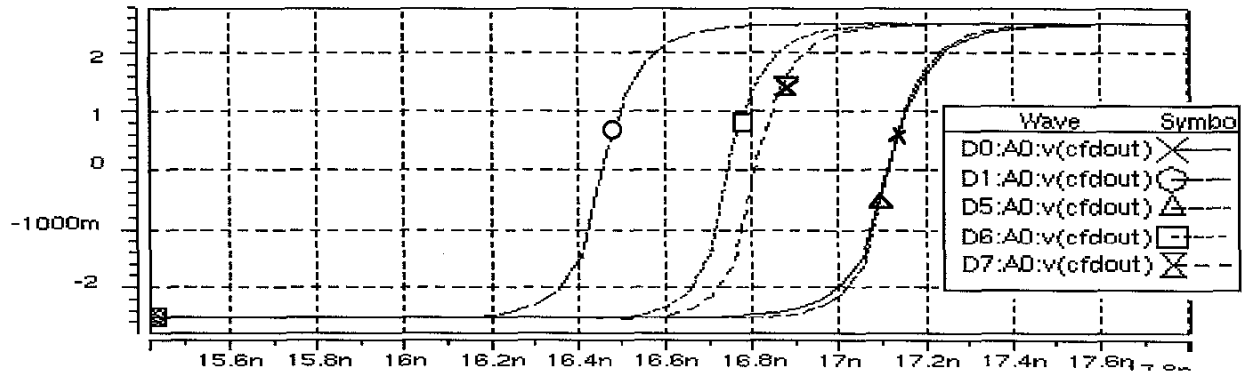

Figure 8. Hspice simulation waveforms of the CFD timing signals with analog delay compensation. (D0: input peak 40mV; D1: input peak 80mV; D5: input peak 120mV; D6: input peak 320mV; D7: input peak 400mV).

III. DIGITAL DELAY COMPENSATION FOR A LEADING-EDGE DISCRIMINATOR

In leading-edge discriminator, the input signal is compared with one threshold voltage. If the input signal is larger than the threshold voltage, the leading-edge timing signal is generated by the comparator. A leading-edge discriminator usually generates a larger timing walk compared to a CFD because of the variation in time between signals of different heights reaching the threshold voltage level. In order to reduce the timing walk between the large signals and the small signals, the timing pulse of the large signals needs to be delayed with respect to the timing of the small signals.

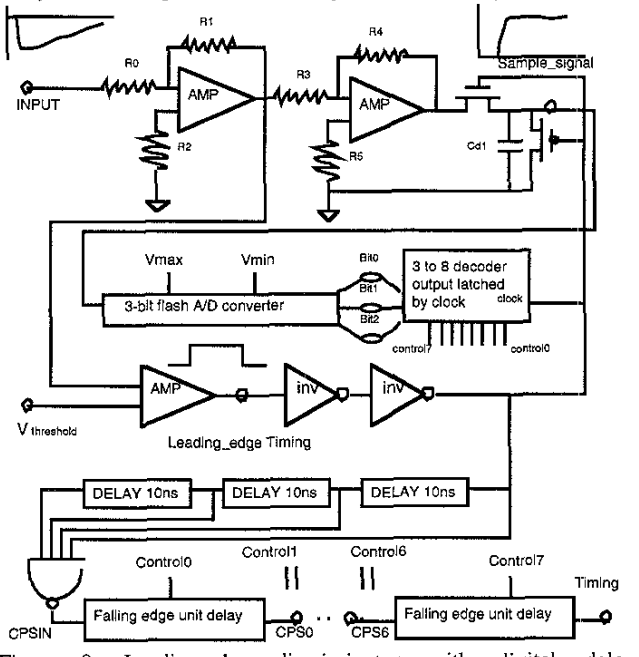

Figure 9. Leading-edge discriminator with digital delay compensation.

The schematic of our digital delay compensation circuit for leading-edge discriminator is shown in Figure 9. The input signal is sampled and digitized by a 3-bit flash Analog to Digital (A/D) Converter. The sampling switch is controlled by the leading edge timing signal. After the 3 to 8 decode, the decoded signal is latched and used to control the 'Falling edge unit delay' circuit. The internal vdd and vss of the A/D converter are adjustable off-chip: making the circuit more robust to processing variations and to mismatches between a real device and Hspice model parameters.

The 'Falling edge unit delay' circuit is shown in Figure 10. When the control signal is low, the NAND2-A is disabled and no extra delay is added. When the control signal is high, the NAND2-A is enabled and two extra gates delays are added to the falling edge of the input signal. Hspice simulation (Figure 11) shows that each unit delay is 600ps.

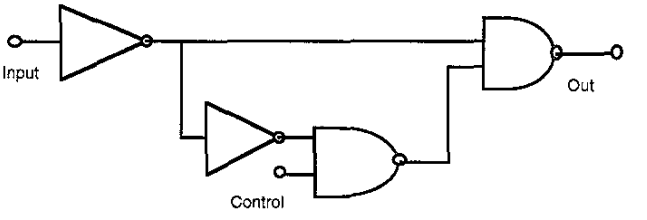

Figure 10. Falling edge unit delay circuit.

Without the digital delay compensation, the timing walk between a 30mV (peak value) signal and a 250mV (peak value) signal is 4.05ns (Figure 12). With the digital delay compensation, the timing signal for the 250mV (peak value) input is delayed about 4ns (6-unit delays) and the timing walk is reduced to 50ps (Figure 13). Table 2 lists the number of unit-delays added to different size input signals. Because of the non-linearity of the timing walk related to input signal size, the ADC is designed also designed to be non-linear. The ADC step size was determined by the Hspice simulation data to minimize the timing walk for signals with a signal range of 8.

Using our digital compensation circuit (with a 3-bit ADC), the time walk associated with our simple leading-edge discriminator was reduced by 83%, from **4.05ns** to **700ps** (one-unit delay range) for a signal range of 8.

Table 2. Comparison of the timing walk relative to 250mV timing pulse of the leading edge discriminator with/without delay compensation.

Input Signal Peak Value (mV)	30	70	90	110	130	150	170	190	230	250
Timing Walk Without Compensation (ns)	**4.05**	2.43	1.90	1.56	1.23	0.91	0.71	0.55	0.14	0.00
Timing Walk With Compensation (ns)	0.05	0.13	0.22	0.42	0.63	0.34	**0.70**	0.57	0.14	0.00
Number of the Unit Delays	0	2	3	4	5	5	6	6	6	6

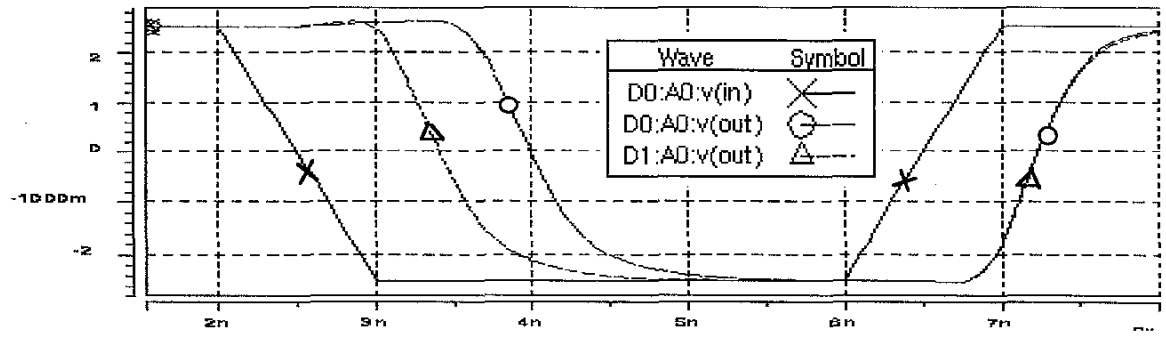

Fig. 11: Hspice simulation waveforms of the unit delay circuit. (D0: unit delay circuit enabled; D1: unit delay circuit disabled).

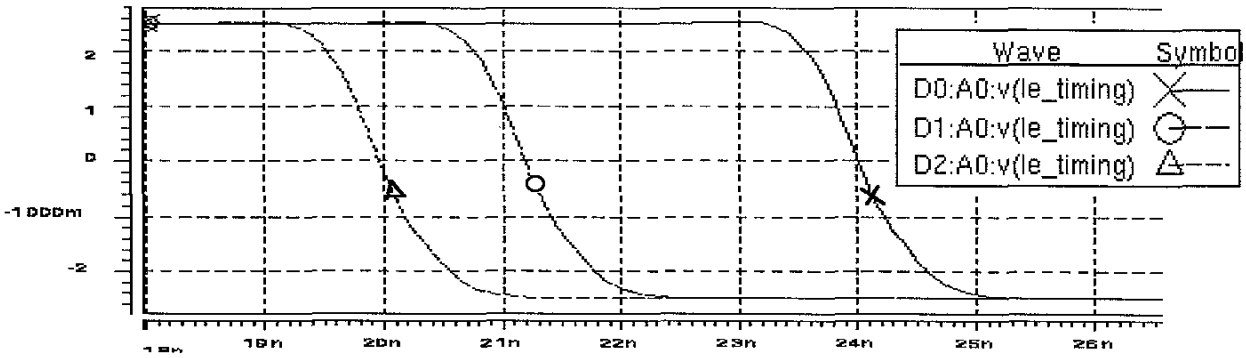

Figure 12. Timing walk without digital compensation (D0: input peak 30mV; D1: input peak 130mV; D2: input peak 250mV)

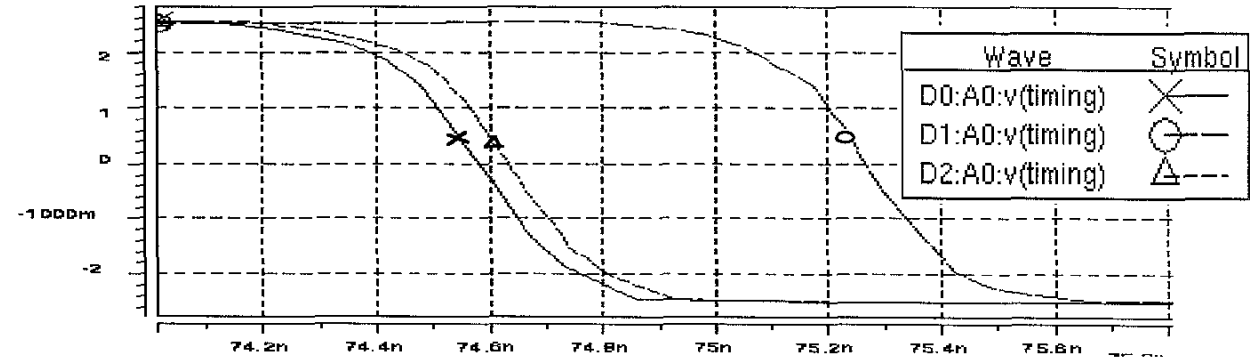

Figure 13. Timing walk with digital compensation (D0: input peak 30mV; D1: input peak 130mV; D2: input peak 250mV). Note that the horizontal scales between Figures 12 and 13 are different.

IV. CONCLUSION

Two circuits have been designed to improve the timing characteristics of integrated timing circuits. Using our analog delay compensation circuit, the timing walk for a monolithic CFD can be reduced by ~50% (from 1.22ns to 660ps for a signal size range of 10). Using a digital technique, the timing walk for a simple leading-edge discriminator can be reduced by ~80% (from 4.05ns to 700ps for a signal size range of 8). The results were obtained using simulated (noise free) signals. An ASIC chip containing the CFD with analog compensation and a leading-edge discriminator with digital delay compensation is being implemented using 1.2um AMI process. The design has been sent to MOSIS for fabrication.

V. REFERENCES

[1] D. M. Binkley and M.E.Casey, IEEE Transaction on Nuclear Science NS-35: pp226-230, 1988.

[2] M. Tanaka, et al, Conference Record of the 1992 IEEE Nuclear Science Symposium and Medical Imaging Conference, pp611-615.

[3] D. Binkley, Nuclear Science Symposium and Medical Imaging Conference 1994 IEEE Conference Record, pp815-819.