“All-in-one” Processors with ISP
CV2880

User Guide
V1.1

Revised: Dec. 9, 2014 Original

Revision History

Version Number	Revision Date	Author	Description of Changes
1.0	Dec/09/2014	Joe	Initial version

Index

Section 1 Introduction

1.1 Overview

The CV2880 is a cost-effective and high performance sensor image signal and video signal processor for cameras and high-end analog display application. The CV2880 provides all key IC functions required for image capture, processing and display timing control. On-chip functions include PLL, high quality zoom and shrink scaling engines, Motion adaptive interlacing, intelligent picture enhancement, an on-screen display controller and 10 bits DACs. With all these functions integrated onto a single device, the CV2880 eliminates the need for several system components simplifying the design and reducing the cost while maintaining a high degree of flexibility and quality.

1.2 Features

- Input Formats
  - 5M(2596x1944) pixels CMOS sensor bayer input
  - BT656/BT1120/YC16Bits
  - RGB/YUV 24Bits
  - Supports SD and HD, interlaced scan and progressive scan, Operation up to 165 MHz.
  - Auto Mode detection
- Intelligent Image Processing
  - Black and white level expansion
  - Flesh Tone Correction
  - Horizontal Peaking
  - Digital Luminance Transient Improvement
  - Digital Chroma Transient Improvement
  - ACCE(Adaptive Color & Contrast Enhancement)
  - Gamma correction
  - AE/AF/AWB for sensor bayer input
  - Vertical flip/horizontal mirror
- Deinterlacing
  - Edge Correction and Motion-adaptive SDTV (NTSC/PAL) / HDTV(1080i) deinterlacing
  - Film mode support for 3:2 and 2:2 pull-down
  - Advanced 2D and 3D Noise Reduction for cross-color suppression
- Scaling
  - Fully programmable zoom ratios
  - Independent Horizontal/vertical scaling
  - Advanced zoom algorithm provides high image quality
- On-chip OSD controller
  - On-chip RAM for high-quality programmable menus
  - 1,2,and 4-bit per pixel character cells
  - Programmable character cells size
  - Horizontal and vertical stretch of OSD menus
  - Blinking, transparency and blending

- Output Formats
  - BT.656/BT.1120/YC16bit/24B RGB/YUV
  - Support SD and HD, Operation up to 165 MHz.
  - Composite video(CVBS and S-Video)
- Analog Video Encoder Output.
  - 10 bits DACs
  - Three CVBS or One S-Video and One CVBS
  - Ypbpr(SOY) and RGB
- Embedded Frame Buffer Memory
- Electrical and Mechanical Characteristics
  - 1.8V/3.3V power supplier
  - 80-Pin HLQFP package

Section 2 Overview

2.1 Block Diagram

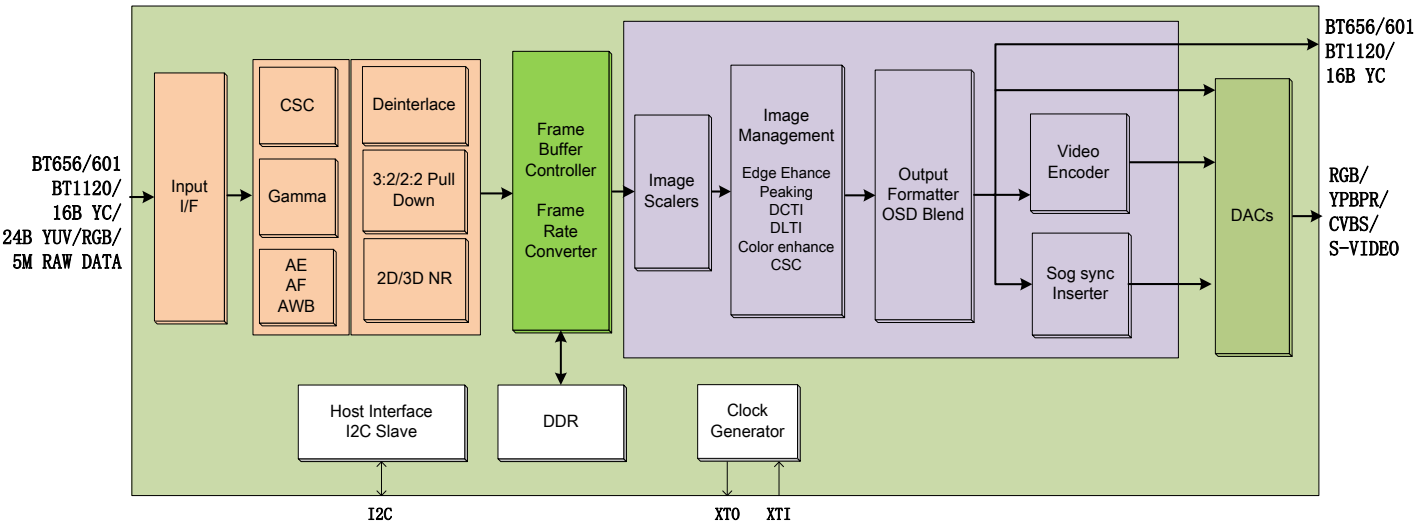


Figure 1. Block Diagram

2.2 Pin Diagram

Unless otherwise stated, unused input pins must be tied to ground, and unused output pins left open.

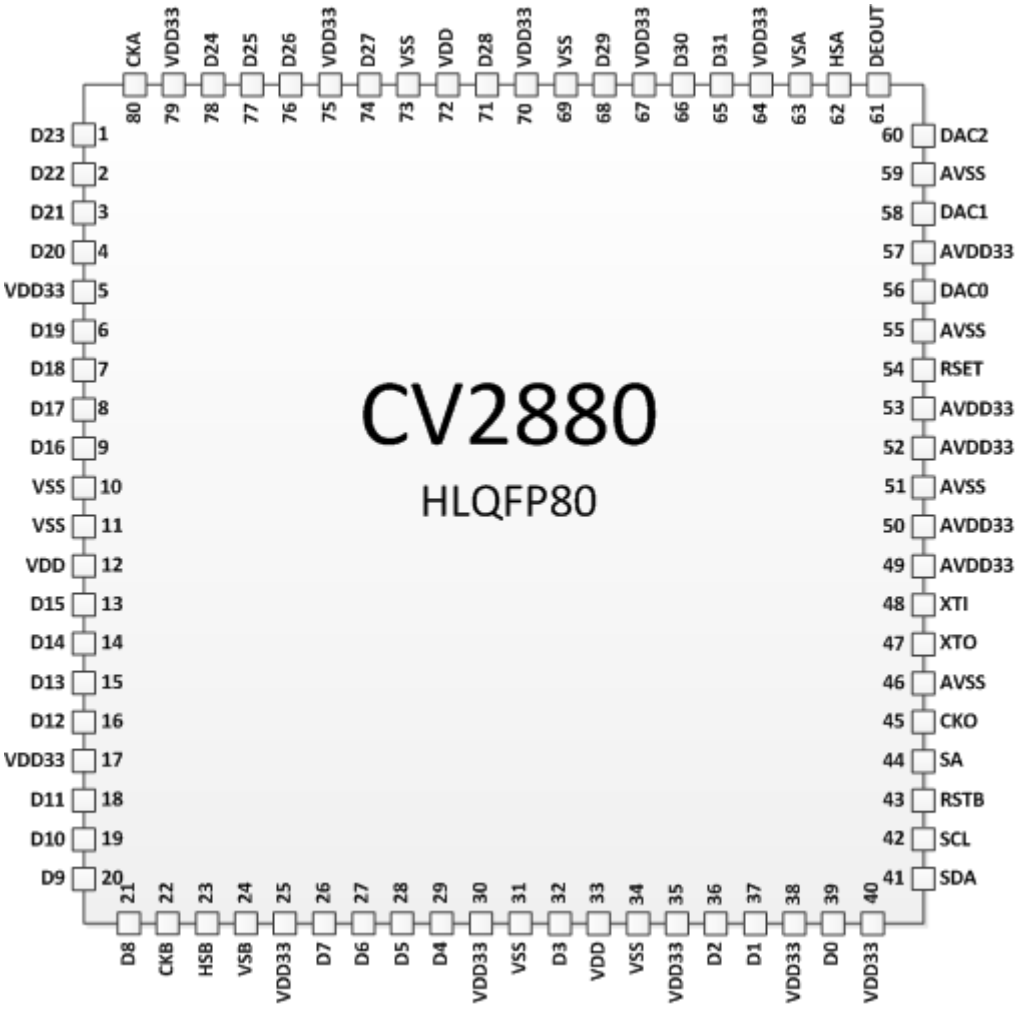


Figure 2. Pin Diagram

2.3 Pin descriptions

Table 1. Power supply pins

VDD	12,33,72	Power	Digital Core Power. 1.8 V.
AVDD33	49,50,52,53,57	Power	Analog Core Power 3.3 V.
VDD33	5,17,25,30,35,38,40 64,67,70,75,79	Power	Digital IO Power 3.3 V.
VSS	10,11,31,34,69,73	Ground	IO Ground.
AVSS	46,51,55,59	Ground	Analog Core Ground.

Table 2. Control and Configuration Pins

RSTB	43	LVTTL Schmitt 3.3 V tolerant	Input	External Reset pin (Active low). This pin has an Internal pull-up. It can be left open when external reset is not required.
SCL	42	LVTTL Schmitt Open drain 3.3 V tolerant	Input	Local I2C Clock. This pin is true open drain, An external pull-up resistor 4.7K is required.
SDA	41	LVTTL Schmitt Open drain 3.3 V tolerant	Inout	Local I2C Data. This pin is true open drain, An external pull-up resistor 4.7K is required.
SA	44	LVTTL Schmitt Open drain 3.3 V tolerant	Input	Chip address,Internal Pull-Up resistor 100K.

Table 3. Normal pins

D31~D0	—	LVTTL Schmitt 3.3 V	Input/output	Digital data in/out
DEOUT	61	LVTTL Schmitt 3.3 V	Output	Data Enable.
HSA	62	LVTTL Schmitt 3.3 V	Output	Horizontal Sync Output.
VSA	63	LVTTL Schmitt 3.3 V	Output	Vertical Sync Output.
CKA	80	LVTTL Schmitt 3.3 V	Output	Output Data Clock.
HSB	23	LVTTL Schmitt 3.3 V	Input	Horizontal Sync Input.
VSB	24	LVTTL Schmitt 3.3 V	Input	Vertical Sync Input.
CKB	22	LVTTL Schmitt 3.3 V	Input	Input Data Clock.
XTI	48	LVTTL Schmitt 3.3 V	Input	Crystal Clock Input.
XTO	47	LVTTL Schmitt 3.3 V	Output	Crystal Clock Output.
CKO	33	LVTTL Schmitt 3.3 V	Output	Programmable Clock Ouptut Of one or half Crystal Frequency.
RSET	54	—	Analog IO	DAC swing R set, An external 10K to ground.
DAC0	56	—	Analog IO	B/Pb/CVBS/Y_Svideo
DAC1	58	—	Analog IO	G/Y/CVBS/C_Svideo
DAC2	60	—	Analog IO	R/Pr/CVBS

2.4 Electrical Characteristics

Table 4. Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
VDD33	Supply Voltage	-0.3	—	4	V	1,2,3
VDD	Digital Core Supply Voltage	-0.3	—	2.2	V	1, 2
AVDD33	Analog Core Supply Voltage	-0.3	—	4	V	1, 2
Vi	Input Voltage	-0.3	—	VDD33 + 0.3	V	1,2
Vo	Output Voltage	-0.3	—	VDD33 + 0.3	V	1,2
Tj	Junction Temperature	—	—	125	^{o}c	—
TSgt	Storage Temperature	-65		150	^{o}c	—

Notes:

1. Permanent device damage can occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under Normal Operating Conditions
3. Voltage undershoot or overshoot cannot exceed absolute maximum conditions

Table 5. ESD Specifications

Symbol	Parameter	Min	Typ	Max	Units	Note
Latch up	ESD Latch up	±150	—,	—	mA	—
HBM	Human Body Model	±8000	—	—	V	—
MM	Machine Model	±400	—	—	V	—

Table 6. Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
VDD33	IO Supply Voltage	2.97	3.3	3.63	V	—
VDD	Digital Core Supply Voltage	1.62	1.8	1.98	V	—
AVDD33	Analog Core Supply Voltage	2.97	3.3	3.63	V	—

2.5 DC Specifications

Table 7. Digital I/O Specifications

Symbol	Parameter	Pin Type[1]	Conditions	Min	Typ	Max	Units	Note
Vih	HIGH Level Input Voltage	LVTTL	—	2	—	—	V	1
Vil	LOW Level Input Voltage	LVTTL	—	—	—	0.8	V	1
Vih	HIGH Level Input Voltage	LVTTL	—	1.2	—	—	V	2
Vil	LOW Level Input Voltage	LVTTL	—	—	—	0.6	V	2

Notes:

1. IO set as 3.3v input tolerant.
2. IO set as 1.8v input tolerant.

Table 8. Crystal

Symbol	Parameter	Conditions	Min	Typ	Max	Units
xtal	External Crystal Freq	—	—	27	—	MHz

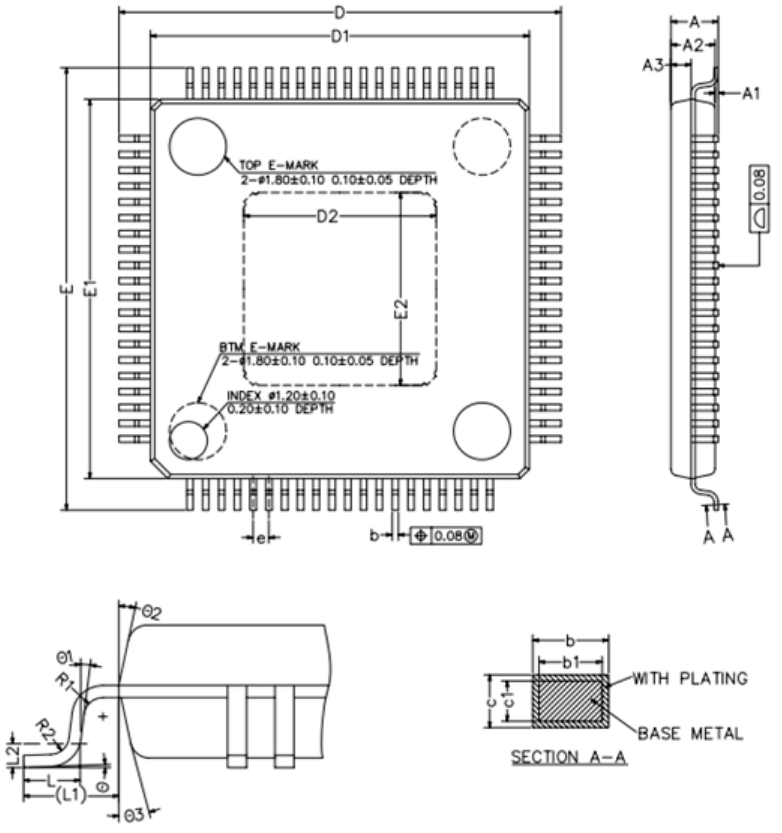
Table 9. DC Power consume (under normal operating conditions unless otherwise specified**)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDD33	IO Supply Voltage	1080i (74.25MHz) input, 1080p VGA output	—	90	—	mA
VDD	Digital Core Supply Voltage		—	330	—	mA
AVDD33	Analog Core Supply Voltage		—	75	—	mA

Section 3 Data Mapping

CV2880 can support 8bits BT601/BT656/BT1120 16bits YUV422 24bits RGB/YUV444 data Input and Output. CV2880 support Byte Swapping function, D[31:24] D[23:16] D[15:8] D[7:0] of CV2880 can be easily used as digital input and output signals.

Section 4 Package



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	13.80	14.00	14.20
D1	11.90	12.00	12.10
D2	6.10REF		
E	13.80	14.00	14.20
E1	11.90	12.00	12.10
E2	6.10REF		
e	0.40	0.50	0.60
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	–	–
R2	0.08	–	0.20
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°