CAT9883C

150MSPS Triple 8-bit Video Analog-to-Digital Data Converter

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FEATURES

- 0.5 V to 1.0 V Analog Input Range
- Ultra Wide Range Conversion Rate (480i~1080P)
- Adjustable Analog Input Bandwidth
- 4:2:2 Output Format Mode
- Digital Output Tri-State
- 3.3 V Power Supply
- Full Sync Processing
- Midscale Clamping
- Power-Down Mode
- Max. Power Dissipation under 800mW @ SXGA (1280x1024x75Hz)
- Automatic Offset Calibration
- Automatic Gain Balance
- Built-In Analog AGC (iGO™)
- Built-In smart de-macrovision
- Green Package (Optional)

Applications

- RGB/YUV Signal Conversion Processing
- LCD Monitors and TV
- Projectors
- Rear Projection TV
- Plasma Display Panels
- Digital TV
- Set-Top Box

GENERAL DESCRIPTION

A top-notch video analog front-end, the CAT9883C converts RGB or YUV triple analog video inputs into 8-bit digital outputs. Specifically, it works to convert analog inputs to digital outputs at up to 8-bits/150MSPS, which means it supports 1080P video format out of the box.

The CAT9883C integrates three ADCs with programmable gain control, PLL, clamp control and offset cancellation. The robust PLL design, which delivers high precision and low jitter, generates pixel clocks from 12MHz to 150MHz. It also supports full sync processing for composite sync and sync-on-green graphic applications.

Equipped with auto-calibration function for ADC inter-channel offset and gain mismatch, the CAT9883C is free of any external adjustment for the sake of color balancing.

The CAT9883C also offers full sync processing for composite sync and sync-on-green applications. Clamp and COAST signals are generated internally or may be provided by the user through Clamp and COAST pin.

The CAT9883C is fabricated in 0.35um mixed-mode CMOS process and available in 80-lead LQFP package.

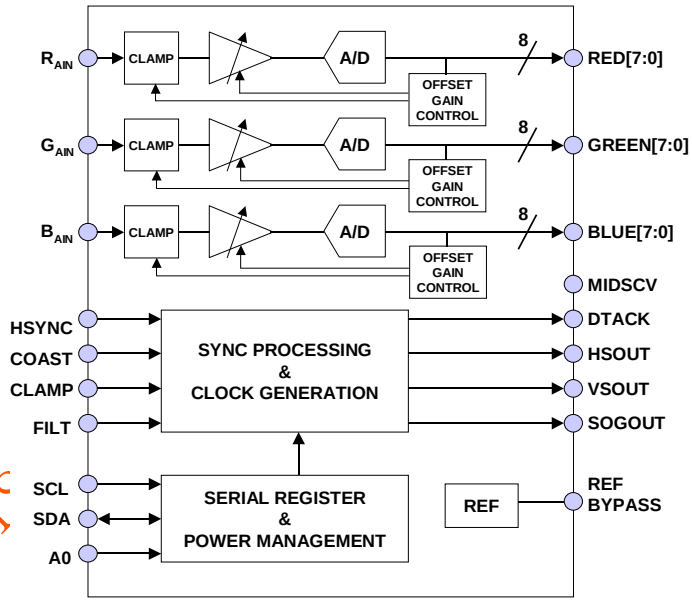


Figure 1. CAT9883C Functional Block Diagram

SPECIFICATIONS

Analog Interface (V_D = 3.3 V, V_{DD} = 3.3 V, ADC Clock = Maximum Conversion Rate, unless otherwise noted.)

Table 1. Electrical Characteristics

		Test	CAT9883C-150			
Parameter	**Temp**	**Level**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION				8		Bits
DC ACCURACY						
Differential Nonlinearity	25℃	I		±0.5	±1.25	LSB
Integral Nonlinearity	25℃	I		±0.5	±2.0	LSB
No Missing Codes	Full	VI		Guaranteed		
ANALOG INPUT						
Input Voltage Range						
Minimum	Full	VI			0.5	V p-p
Maximum	Full	VI	1.0			V p-p
Input Bias Current	25℃	IV			1	µA
REFERENCE OUTPUT						
Output Voltage	Full	VI	1.16	1.22	1.28	V
Temperature Coefficient	Full	V		±50	0.5	ppm/℃
SWITCHING PERFORMANCE						
Maximum Conversion Rate	Full	VI	150			MSPS
Minimum Conversion Rate	Full	IV			10	MSPS
Clock to Data Skew	Full	IV	–0.5		+2.0	ns
HSYNC Input Frequency	Full	IV	15		110	kHz
Maximum PLL Clock Rate	Full	VI	150			MHz
Minimum PLL Clock Rate	Full	IV			10	MHz
PLL Jitter	25℃	IV		400 [1]		ps p-p
DIGITAL INPUTS						
Input Voltage, High (V_{IH})	Full	VI	2.5			V
Input Voltage, Low (V_{IL})	Full	VI			0.8	V
Input Current, High (I_{IH})	Full	V			–1.0	µA
Input Current, Low (I_{IL})	Full	V			+1.0	µA
Input Capacitance	25℃	V		3		pF
DIGITAL OUTPUTS						
Output Voltage, High (V_{OH})	Full	VI	Vdd– 0.1			V
Output Voltage, Low (V_{OL})	Full	VI			0.1	V
Duty Cycle DATACK	Full	IV	45	50	55	%
Output Coding				Binary		
POWER SUPPLY						
VD Supply Voltage	Full	IV	3.15	3.3	3.6	V
VDD Supply Voltage	Full	IV	2.5	3.3	3.6	V
PVD Supply Voltage	Full	IV	3.15	3.3	3.6	V
ID Supply Current (V_D)	25℃	V		TBD		mA
IDD Supply Current (V_{DD})[2]	25℃	V		TBD		mA
IPVD Supply Current (P_{VD})	25℃	V		TBD		mA
Total Power Dissipation	Full	VI		TBD		mW
Power-Down Supply Current	Full	VI		TBD		mA
Power-Down Dissipation	Full	VI		TBD		mW
DYNAMIC PERFORMANCE						
Signal-to-Noise Ratio (SNR)	25℃	V		43		dB
(Without Harmonics)	Full	V		42		dB
Crosstalk	Full	V		55		dBc
THERMAL CHARACTERISTICS						
θ_{JC} Junction-to-Case						
Thermal Resistance		V		16		℃/W
θ_{JA} Junction-to-Ambient						
Thermal Resistance		V		35		℃/W

NOTES

[1]1280x1024 @ 75Hz, delay triggered 1uS. Integrated 1000 cycles.
[2]DATACK Load = 15 pF, Data Load = 5 pF.
*Specifications subject to change without notice

ABSOLUTE MAXIMUM RATINGS*

V_D	3.6 V
V_{DD}	3.6 V
Analog Inputs	VD to 0.0 V
VREF IN	VD to 0.0 V
Digital Inputs	5 V to 0.0 V
Digital Output Current	20 mA
Operating Temperature	0℃ to +70℃
Storage Temperature	–65℃ to +150℃
Maximum Junction Temperature	150℃
Maximum Case Temperature	150℃
ESD Human Body Mode	2000 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

I. 100% production tested.
II. 100% production tested at 25℃ and sample teste d at specified temperatures.
III. Sample tested only.
IV. Parameter is guaranteed by design and characterization testing.
V. Parameter is a typical value only.
VI. 100% production tested at 25℃; guaranteed by design and characterization testing

WARNING:
CAT9883C is an ESD sensitive device. Though it has protection circuit, however, it may be damaged by much higher discharged voltage. To prevent any possible damage of performance and reliability, please handle it with care and make sure of your environment to meet regulations to avoid such ESD damage.

Pin Configuration

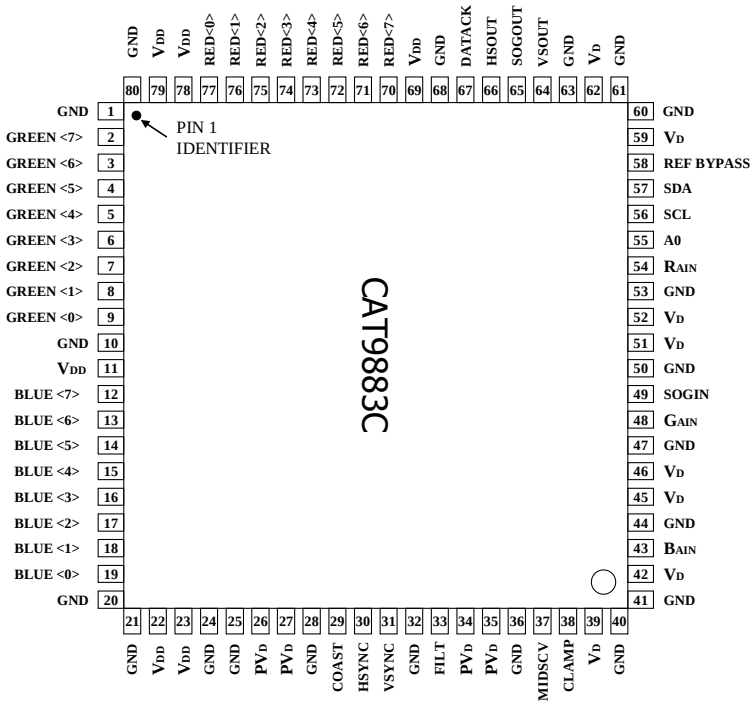


Figure 2. CAT9883C Pin Configuration

Table 2. Complete Pinout List

Pin Type	Mnemonic	Function	Value	Pin No.
Inputs	RAIN	Analog Input for Converter R	0.0 V to 1.0 V	54
	GAIN	Analog Input for Converter G	0.0 V to 1.0 V	48
	BAIN	Analog Input for Converter B	0.0 V to 1.0 V	43
	HSYNC	Horizontal SYNC Input	3.3 V CMOS	30
	VSYNC	Vertical SYNC Input	3.3 V CMOS	31
	SOGIN	Input for Sync-on-Green	0.0 V to 1.0 V	49
	CLAMP	Clamp Input (External CLAMP Signal)	3.3 V CMOS	38
	COAST	PLL COAST Signal Input	3.3 V CMOS	29
Outputs	Red [7:0]	Outputs of Converter Red, Bit 7 is the MSB	3.3 V CMOS	70–77
	Green [7:0]	Outputs of Converter Green, Bit 7 is the MSB	3.3 V CMOS	2–9
	Blue [7:0]	Outputs of Converter Blue, Bit 7 is the MSB	3.3 V CMOS	12–19
	DATACK	Data Output Clock	3.3 V CMOS	67
	HSOUT	HSYNC Output (Phase-Aligned with DATACK)	3.3 V CMOS	66
	VSOUT	VSYNC Output (Phase-Aligned with DATACK)	3.3 V CMOS	64
	SOGOUT	Sync-on-Green Slicer Output	3.3 V CMOS	65
References	REF BYPASS	Internal Reference Bypass	1.25 V	58
	MIDSCV	Internal Midscale Voltage Bypass		37
	FILT	Connection for External Filter Components for Internal PLL		33
Power Supply	VD	Analog Power Supply	3.3 V	39, 42, 45, 46, 51, 52, 59, 62
	VDD	Output Power Supply	3.3 V	11, 22, 23, 69, 78, 79
	PVD	PLL Power Supply	3.3 V	26, 27, 34, 35
	GND	Ground	0 V	1, 10, 20, 21, 24, 25, 28, 32, 36, 40, 41, 44, 47, 50, 53, 60, 61, 63, 68, 80
Control	SDA	Serial Port Data I/O	3.3 V CMOS	57
	SCL	Serial Port Data Clock (100 kHz Maximum)	3.3 V CMOS	56
	A0	Serial Port Address Input 1	3.3 V CMOS	55

PIN FUNCTION DESCRIPTIONS

INPUTS

R_{AIN}: Analog Input for Red Channel

G_{AIN}: Analog Input for Green Channel

B_{AIN}: Analog Input for Blue Channel
High impedance inputs that accept the Red, Green, and Blue channel graphics signals, respectively. (The three channels are identical, and can be used for any colors, but colors are assigned for convenient reference.) They accommodate input signals ranging from 0.5 V to 1.0 V full scale. Signals should be ac-coupled to these pins to support clamp operation.

HSYNC: Horizontal Sync Input.
This input receives a logic signal that establishes the horizontal timing reference and provides the frequency reference for pixel clock generation. The logic sense of this pin is controlled by serial register 0EH Bit 6 (Hsync Polarity). Only the leading edge of Hsync is active; the trailing edge is ignored. When Hsync Polarity = 0, the falling edge of Hsync is used. When Hsync Polarity = 1, the rising edge is active. The input includes a Schmitt trigger for noise immunity, with a nominal input threshold of 1.5 V.

VSYNC: Vertical Sync Input.
This is the input for vertical sync.

SOGIN: Sync-on-Green Input.
This input is provided to assist with processing signals with embedded sync, typically on the Green channel. The pin is connected to a high speed comparator with an internally generated threshold. The threshold level can be programmed in 10 mV steps to any voltage between 10 mV and 330 mV above the negative peak of the input signal. The default voltage threshold is 150 mV. When connected to an ac-coupled graphics signal with embedded sync, it will produce a noninverting digital output on SOGOUT. (This is usually a composite sync signal, containing both vertical and horizontal sync information that must be separated before passing the horizontal sync signal to Hsync.) When not used, this input should be left unconnected. For more details on this function and how it should be configured, refer to the Sync-on-Green section.

CLAMP: External Clamp Input.
This logic input may be used to define the time during which the input signal is clamped to ground. It should be exercised when the reference dc level is known to be present on the analog input channels, typically during the back porch of the graphics signal. The CLAMP pin is enabled by setting control bit Clamp Function to 1, (register 0FH, Bit 7, default is 0). When disabled, this pin is ignored and the clamp timing is determined internally by counting a delay and duration from the trailing edge of the Hsync input. The logic sense of this pin is controlled by Clamp Polarity register 0FH, Bit 6. When not used, this pin must be grounded and Clamp Function programmed to 0.

COAST: Clock Generator Coast Input (Optional).
This input may be used to cause the pixel clock generator to stop synchronizing with Hsync and continue producing a clock at its current frequency and phase. This is useful when processing signals from sources that fail to produce horizontal sync pulses during the vertical interval. The COAST signal is generally *not* required for PC-generated signals. The logic sense of this pin is controlled by Coast Polarity (register 0FH, Bit 3). When not used, this pin may be grounded and Coast Polarity programmed to 1, or tied HIGH (to VD through a 10 k~ resistor) and Coast Polarity programmed to 0. Coast Polarity defaults to 1 at power-up.

REFERENCES

REF BYPASS: Internal Reference BYPASS.
Bypass for the internal 1.22 V band gap reference. It should be connected to ground through a 0.1 µF capacitor. The absolute accuracy of this reference is ±4%, and the temperature coefficient is ±50 ppm, which is adequate for most CAT9883C applications. If higher accuracy is required, an external reference may be employed instead.

MIDSCV: Midscale Voltage Reference BYPASS.
Bypass for the internal midscale voltage reference. It should be connected to ground through a 0.1 µF capacitor. The exact voltage varies with the gain setting of the Blue channel.

FILT: External Filter Connection.
For proper operation, the pixel clock generator PLL requires an external filter. Connect the filter shown in Figure 6 to this pin. For optimal performance, minimize noise and parasitics on this node.

OUTPUTS

HSOUT: Horizontal Sync Output.

A reconstructed and phase-aligned version of the Hsync input. Both the polarity and duration of this output can be programmed via serial bus registers. By maintaining alignment with DATACK and Data, data timing with respect to horizontal sync can always be determined.

VSOUT: Vertical Sync Output.

A reconstructed and phase-aligned version of the video Vsync. The polarity of this output can be controlled via a serial bus bit. The placement and duration in all modes is set by the graphics transmitter.

SOGOUT: Sync-On-Green Slicer Output.

This pin outputs either the signal from the Sync-on-Green slicer comparator or an unprocessed but delayed version of the Hsync input. (Note: Besides slicing off SOG, the output from this pin gets no other additional processing on the CAT9883C. Vsync separation is performed via the sync separator.)

DATA OUTPUTS

RED: Data Output, Red Channel.

GREEN: Data Output, Green Channel.

BLUE: Data Output, Blue Channel.
The main data outputs. Bit 7 is the MSB. The delay from pixel sampling time to output is fixed. When the sampling time is changed by adjusting the PHASE register, the output timing is shifted as well. The DATACK and HSOUT outputs are also moved, so the timing relationship among the signals is maintained. For exact timing information, refer to Figures 7, and 8.

DATA CLOCK OUTPUTS

DATACK: Data Output Clock.
This is the main clock output signal used to strobe the output data and HSOUT into external logic. It is produced by the

internal clock generator and is synchronous with the internal pixel sampling clock. When the sampling time is changed by adjusting the PHASE register, the output timing is shifted as well. The Data, DATACK, and HSOUT outputs are all moved, so the timing relationship among the signals is maintained.

POWER SUPPLY

V_D: Main Power Supply.
These pins supply power to the main elements of the circuit. They should be filtered and as quiet as possible.

V_{DD}: Digital Output Power Supply.
A large number of output pins (up to 25) switching at high speed (up to 110 MHz) generates a lot of power supply transients (noise). These supply pins are identified separately from the VD pins so special care can be taken to minimize output noise transferred into the sensitive analog circuitry. If the CAT9883C is interfacing with lower voltage logic, V_{DD} may be connected to a lower supply voltage (as low as 2.5 V) for compatibility.

PV_D: Clock Generator Power Supply.
The most sensitive portion of the CAT9883C is the clock generation circuitry. These pins provide power to the clock PLL and help the user design for optimal performance. The designer should provide quiet, noise-free power to these pins.

GND: Ground.
The ground return for all circuitry on-chip. It is recommended that the CAT9883C be assembled on a single solid ground plane, with careful attention given to ground current paths.

SERIAL PORT (2-Wire)

SDA: Serial Port Data I/O.

SCL: Serial Port Data Clock.

A0: Serial Port Address Input 1.
For a full description of the 2-wire serial register and how it works, refer to the 2-Wire Serial Control Port section.

Design Guide

General Description

The CAT9883C is a fully integrated solution for capturing analog RGB signals and digitizing them for display on flat panel monitors or projectors. The circuit is ideal for providing a computer interface for high-resolution monitors or as the front end to high performance video scan converters. Implemented in a high performance CMOS process, the interface can capture signals with pixel rates up to 150 MHz.

The CAT9883C includes all necessary input buffering, signal dc restoration (clamping), offset and gain (brightness and contrast) adjustment, pixel clock generation, sampling phase control, and output data formatting. All controls are programmable via a 2-wire serial interface. Full integration of these sensitive analog functions makes system design straightforward and less sensitive to the physical and electrical environment.

Digital Inputs

All digital inputs on the CAT9883C operate to 3.3 V CMOS levels. However, all digital inputs are 5 V tolerant. Applying 5 V to them will not cause any damage.

Input Signal Handling

The CAT9883C has three high impedance analog input pins for the Red, Green, and Blue channels. They will accommodate signals ranging from 0.5 V to 1.0 V p-p. Signals are typically brought onto the interface board via a DVI-I connector, a 15-pin D connector, BNC connectors, or RCA connectors.

As a sample-data system without input gain amplifier, the ultrawide bandwidth inputs of the CAT9883C (300 MHz) can sample incoming video signals without gain loss and thus provide very sharp image outputs.

In many systems, however, there are mismatches, reflections, and noise, which can result in excessive ringing and distortion of the input waveform. This makes it more difficult to establish a sampling phase that provides good image quality. It has been shown that a simple low-pass circuit like a small inductor in series with the input is effective to provide a high quality signal over a wider range of conditions.

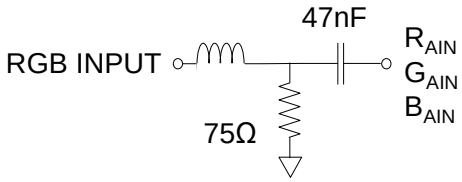


Figure 3. Analog Input Interface Circuit

Hsync, Vsync Inputs

The interface also takes a horizontal sync signal, which is used to generate the pixel clock and clamp timing. This can be either a sync signal directly from the graphics source, or a preprocessed TTL or CMOS level signal.

The Hsync input includes a Schmitt trigger buffer for immunity to noise and signals with long rise times. In typical PC based graphic systems, the sync signals are simply TTL-level drivers feeding unshielded wires in the monitor cable. As such, no termination is required.

Serial Control Port

The serial control port is designed for 3.3V logic. If there are 5V drivers on the bus, these pins should be protected with 150 Ω series resistors placed between the pull-up resistors and the input pins.

Output Signal Handling

The digital outputs are designed and specified to operate from a 3.3 V power supply (VDD). They can also work with a VDD as low as 2.5 V for compatibility with other 2.5 V logic.

Clamping

RGB Clamping

To properly digitize the incoming signal, the dc offset of the input must be adjusted to fit the range of the on-board A/D converters.

The key to clamping is to identify a portion (time) of the signal when the graphic system is known to be producing black. An offset is then introduced which results in the A/D converters producing a black output (code 00h) when the known black input is present. The offset then remains in place when other signal levels are processed, and the entire signal is shifted to eliminate offset errors.

In most PC graphics systems, black is transmitted between active video lines. In systems with embedded sync, a blacker-than-black signal (Hsync) is produced briefly to signal the CRT that it is time to begin a retrace. For obvious

reasons, it is important to avoid clamping on the tip of Hsync. Fortunately, there is virtually always a period following Hsync, called the back porch, where a good black reference is provided. This is the time when clamping should be done.

The clamp timing can be established by simply exercising the CLAMP pin at the appropriate time (with External Clamp = 1). The polarity of this signal is set by the Clamp Polarity bit.

A simpler method of clamp timing employs the CAT9883C internal clamp timing generator. The Clamp Placement register is programmed with the number of pixel times that should pass after the trailing edge of HSYNC before clamping starts. A second register (Clamp Duration) sets the duration of the clamp. These are both 8-bit values, providing considerable flexibility in clamp generation. The clamp timing is referenced to the trailing edge of Hsync because, though Hsync duration can vary widely, the back porch (black reference) always follows Hsync. A good starting point for establishing clamping is to set the clamp placement to 09H (providing 9 pixel periods for the graphics signal to stabilize after sync) and set the clamp duration to 14H (giving the clamp 20 pixel periods to reestablish the black reference).

Clamping is accomplished by placing an appropriate charge on the external input coupling capacitor. The value of this capacitor affects the performance of the clamp. If it is too small, there will be a significant amplitude change during a horizontal line time (between clamping intervals). If the capacitor is too large, then it will take excessively long for the clamp to recover from a large change in incoming signal offset.

YUV Clamping

YUV graphic signals are slightly different from RGB signals in that the dc reference level (black level in RGB signals) can be at the midpoint of the graphics signal rather than at the bottom. For these signals, it can be necessary to clamp to the midscale range of the A/D converter range (80H) rather than at the bottom of the A/D converter range (00H).

Clamping to midscale rather than to ground can be accomplished by setting the clamp select bits in the serial bus register. Each of the three converters has its own selection bit so that they can be clamped to either midscale or ground independently. These bits are located in register 10H and are Bits 0~2. The midscale reference voltage that each A/D converter clamps to is provided on the MIDSCV pin, (Pin 37). This pin should be bypassed to ground with a 0.1µF capacitor, (even if midscale clamping is not required).

Gain and Offset Control

The CAT9883C can accommodate input signals with inputs ranging from 0.5 V to 1.0 V full scale. The full-scale range is set in three 8-bit registers (Red Gain, Green Gain, and Blue Gain). Larger gain setting maps output code to larger input range.

The offset control shifts the entire input range. Three 7-bit registers (Red Offset, Green Offset, Blue Offset) provide independent settings for each channel. The offset controls provide a ±63 LSB adjustment range. This range is connected with the gain setting, so 1 offset code maps to 1 LSB regardless how much the gain code is.

Figure 4 illustrates the interaction of gain and offset controls. The magnitude of an LSB in offset adjustment is proportional to the full-scale range, so changing the full-scale range also changes the offset. The change is minimal if the offset setting is near midscale. When changing the offset, the full-scale range is not affected, but the full-scale level is shifted by the same amount as the zero scale level.

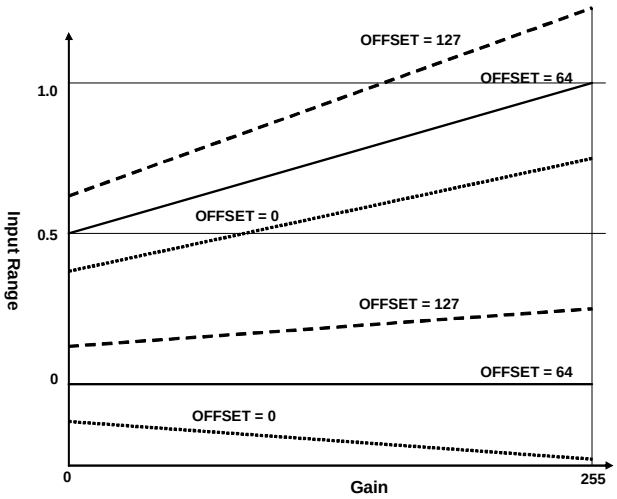


Figure 4. Gain and Offset Control

Sync-on-Green

The Sync-on-Green input operates in two steps. First, it sets a baseline clamp level off of the incoming video signal with a negative peak detector. Second, it sets the sync trigger level to a programmable level (typically 150 mV) above the negative peak. The Sync-on-Green input must be ac-coupled to the Green analog input through its own capacitor, as shown in Figure 5. The value of the capacitor must be 1nF±20%. If Sync-on-Green is not used, this connection is not required. Note that the Sync-on-Green signal is always negative polarity.

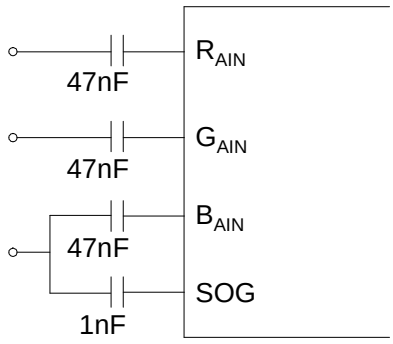


Figure 5. Typical Clamp Configuration

Clock Generation

The PLL characteristics are determined by the loop filter design, by the PLL Charge Pump Current, and by the VCO range setting. The loop filter design is illustrated in Figure 6. Recommended settings of VCO range and charge pump current for VESA standard display modes and TV modes are listed in Table II.

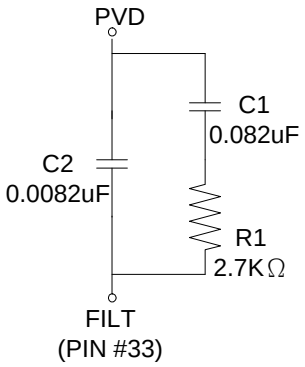


Figure 6. PLL Loop Filter

Four programmable registers are provided to optimize the performance of the PLL. These registers are:

1. The 12-Bit Divisor Register. The input Hsync frequencies range from 15 kHz to 110 kHz. The PLL multiplies the frequency of the Hsync signal, producing pixel clock frequencies in the range of 12 MHz to 150 MHz. The Divisor Register controls the exact multiplication factor. This register may be set to any value between 221 and 4095. (The divide ratio that is actually used is the programmed divide ratio plus one.)
2. The 2-Bit VCO Range Register. To improve the noise performance of the CAT9883C, the VCO operating frequency range is divided into three overlapping regions. The VCO Range Register sets this operating range. The frequency ranges for the lowest and highest regions are shown in Table III.
3. The 3-Bit Charge Pump Current Register. This register allows the current that drives the low-pass loop filter to be varied. The possible current values are listed in Table IV.
4. The 5-Bit Phase Adjust Register. The phase of the generated sampling clock may be shifted to locate an optimum sampling point within a clock cycle. The Phase Adjust Register provides 32 phase-shift steps of 11.25 degrees each. The Hsync signal with an identical phase shift is available through the HSOUT pin.

The COAST pin is used to allow the PLL to continue to run at the same frequency, in the absence of the incoming Hsync signal or during disturbances in Hsync (such as equalization pulses). This may be used during the vertical sync period, or any other time that the Hsync signal is unavailable. The polarity of the COAST signal may be set through the Coast Polarity Register. Also, the polarity of the Hsync signal may be set through the Hsync Polarity Register. If not using automatic polarity detection, the Hsync and COAST Polarity bits should be set to match the respective polarities of the input signals.

Table 3. Recommended VCO Range and Charge Pump Current Settings for Standard Display Formats

Standard	Resolution	Refresh Rate	Horizontal Frequency	CAT9883C		
				Pixel Rate	VCORNGE	Current
PC Mode						
VGA	640 × 480	60 Hz	31.5 kHz	25.175 MHz	00	110
		72 Hz	37.7 kHz	31.500 MHz	00	110
		75 Hz	37.5 kHz	31.500 MHz	00	110
		85 Hz	43.3 kHz	36.000 MHz	01	100
SVGA	800 × 600	56 Hz	35.1 kHz	36.000 MHz	01	100
		60 Hz	37.9 kHz	40.000 MHz	01	100
		72 Hz	48.1 kHz	50.000 MHz	01	101
		75 Hz	46.9 kHz	49.500 MHz	01	101
		85 Hz	53.7 kHz	56.250 MHz	01	101
XGA	1024 × 768	60 Hz	48.4 kHz	65.000 MHz	10	101
		70 Hz	56.5 kHz	75.000 MHz	10	100
		75 Hz	60.0 kHz	78.750 MHz	10	100
		80 Hz	64.0 kHz	85.500 MHz	10	101
		85 Hz	68.3 kHz	94.500 MHz	10	101
SXGA	1280 × 1024	60 Hz	64.0 kHz	108.000 MHz	10	110
		75 Hz	80.0 kHz	135.000 MHz	11	110
TV Mode						
480i	640x480	60 Hz	15.75 kHz	13.50 MHz	00	010
480P	640x480	60 Hz	31.47 kHz	27.00 MHz	00	110
720P	1280x720	60 Hz	45.00 kHz	74.25 MHz	10	100
1080i	1920x1080	60 Hz	33.75 kHz	74.25 MHz	10	100
1080P	1920x1080	60 Hz	67.5 kHz	148.5 MHz	11	110

Table 4. VCO Frequency Range

PV1	PV0	Pixel Clock Range (MHz)
0	0	12 - 32
0	1	32 - 64
1	0	64 - 110
1	1	110 - 150

Table 5. Charge Pump Current/Control Bits

Ip2	Ip1	Ip0	Current(μA)
0	0	0	50
0	0	1	100
0	1	0	150
0	1	1	250
1	0	0	350
1	0	1	500
1	1	0	750
1	1	1	1500

Power Management

The CAT9883C uses the activity detect circuits, the active interface bits in the serial bus, the active interface override bits, and the power-down bit to determine the correct power state. There are three power states, full-power, seek mode, and power-down. Table IV summarizes how the CAT9883C determines what power mode to be in and which circuitry is powered on/off in each of these modes. The power-down command has priority over the automatic circuitry.

Table 6. Power-Down Mode Descriptions

Mode	Reg of PWRDN[1]	Sync Detect	Active Circuitry
Full-Power	1	1	Whole chip
Seek Mode	1	0	Serial Bus, Sync Activity Detect, S0G, BandGap Reference
Power-Down	0	X	Serial Bus, Sync Activity Detect, S0G, BandGap Reference

NOTES

[1]Power-down is controlled via Bit1 in serial bus register 0FH

[2]Sync detect is determined by OR-ing Bits 7, 4, and 1 in serial bus register 14H

Timing

The following timing diagrams show the operation of the CAT9883C.

The output data clock signal is created so that its rising edge always occurs between data transitions, and can be used to latch the output data externally.

There is a pipeline in the CAT9883C, which must be flushed before valid data becomes available. This means four data sets are presented before valid data is available.

Hsync Timing

Horizontal Sync (Hsync) is processed in the CAT9883C to eliminate ambiguity in the timing of the leading edge with respect to the phase-delayed pixel clock and data.

The Hsync input is used as a reference to generate the pixel sampling clock. The sampling phase can be adjusted, with respect to Hsync, through a full 360° in 32 steps via the Phase Adjust Register (to optimize the pixel sampling time). Display systems use Hsync to align memory and display write cycles, so it is important to have a stable timing relationship between Hsync output (HSOUT) and data clock (DATACK).

Three things happen to Horizontal Sync in the CAT9883C. First, the polarity of Hsync input is determined and will thus have a known output polarity. The known output polarity can be programmed either active high or active low (register 0EH, Bit 5). Second, HSOUT is aligned with DATACK and data outputs. Third, the duration of HSOUT (in pixel clocks) is set via register 07H. HSOUT is the sync signal that should be used to drive the rest of the display system.

Coast Timing

In most computer systems, the Hsync signal is provided continuously on a dedicated wire. In these systems, the COAST input and functions are unnecessary, and should not be used and the pin should be permanently connected to the inactive state.

In some systems, however, Hsync is disturbed during the Vertical Sync period (Vsync). In some cases, Hsync pulses disappear. In other systems, such as those that employ Composite Sync (Csync) signals or embedded Sync-on- Green (SOG), Hsync includes equalization pulses or other distortions during Vsync. To avoid upsetting the clock generator during Vsync, it is important to ignore these distortions. If the pixel clock PLL sees extraneous pulses, it will attempt to lock to this new frequency, and will have changed frequency by the end of the Vsync period. It will then take a few lines of correct Hsync timing to recover at the beginning of a new frame, resulting in a "tearing" of the image at the top of the display.

The COAST input is provided to eliminate this problem. It is an asynchronous input that disables the PLL input and allows the clock to free-run at its then-current frequency. The PLL can free-run for several lines without significant frequency drift.

Sync Slicer

The purpose of the sync slicer is to extract the sync signal from Sync-on-Green. The sync signal is extracted from the Green channel in a two-step process. First, the SOG input is clamped to its negative peak (typically 0.3 V below the black level). Next, the signal goes to a comparator with an adjustable trigger level, nominally 0.15 V above the clamped level. The "sliced" sync is typically a composite sync signal containing both Hsync and Vsync.

Sync Separator

A sync separator extracts the Vsync signal from a composite sync signal. It does this through a low-pass filter-like or integrator-like operation. It works on the fact that the Vsync signal stays active for a much longer time than the Hsync signal, so it rejects any signal shorter than a threshold value, which is somewhere between an Hsync pulsewidth and a Vsync pulsewidth.

The sync separator on the CAT9883C is simply an 8-bit digital counter with an internal clock. It works independently of the polarity of the composite sync signal. (Polarities are determined elsewhere on the chip.) The basic idea is that the counter counts up when Hsync pulses are present. But since Hsync pulses are relatively short in width, the counter only reaches a value of N before the pulse ends. It then starts counting down eventually reaching 0 before the next Hsync pulse arrives. The specific value of N will vary for different video modes, but will always be less than 255. For example with a 1 µs width Hsync, the counter will only reach 5 (1 µs/200 ns = 5). Now, when Vsync is present on the composite sync the counter will also count up. However, since the Vsync signal is much longer, it will count to a higher number M. For most video modes, M will be at least 255. So, Vsync can be detected on the composite sync signal by detecting when the counter counts to higher than N. The specific count that triggers detection (T) can be programmed through the serial register (11H).

Once Vsync has been detected, there is a similar process to detect when it goes inactive. At detection, the counter first resets to 0, then starts counting up when Vsync goes away. Similar to the previous case, it will detect the absence of Vsync when the counter reaches the threshold count (T). In this way, it will reject

noise and/or serration pulses. Once Vsync is detected to be absent, the counter resets to 0 and begins the cycle again.

Tri-State the Data Output

CAT9883C data output disable (tri-state output) is controlled through bit 6 of register 85H. One can only tri-state the output using this bit. Power down this chip using bit 1 of 0FH will not make the data output tri-state.

Auto offset/color/gain calibration

CAT9883C offset/color/gain calibration can be done automatically by setting registers. If it is only offset or offset/color calibration that is needed, CAT9883C also offer the option.

After calibration, the CAT9883C can be viewed as a pseudo-ideal ADC free of gain and offset error.

Sometimes because the ground of the system board is noisy, the offset after calibration might drift to 2~4LSB. Under this situation, user can do calibration longer but only once. Details please reference our design-in quick guide.

User can set the gain and offset as wish after the calibration. That mean the system designer can adjust the color analogly to get largest dynamic range.

Input anti-aliasing filter

To prevent from input signal path noise, CAT9883C equipped with analog anti-aliasing filter. Default cut off frequency is 300MHz. If user needs to change the cutoff frequency, please check our design-in quick guide.

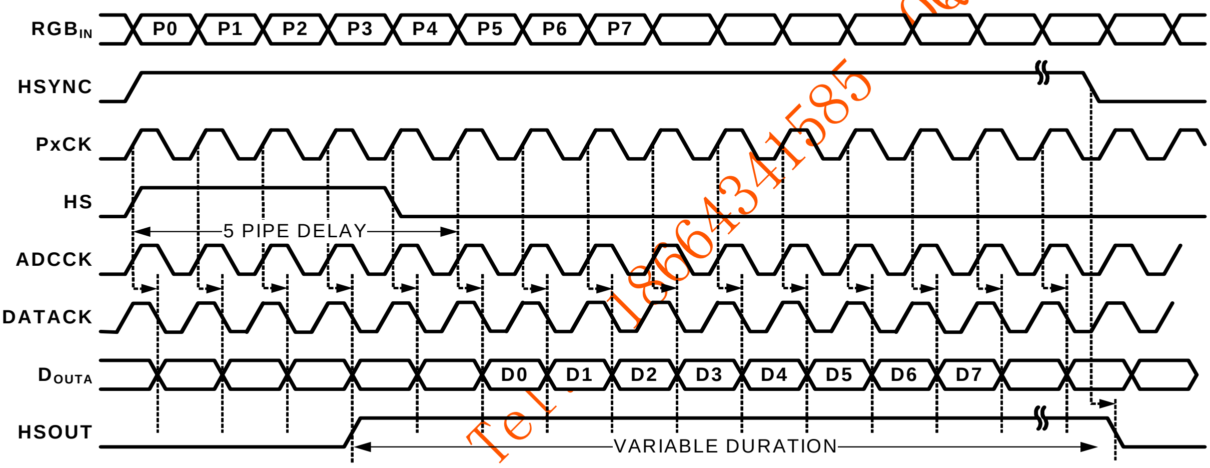


Figure 7. 4:4:4 Mode (For RGB and YUV)

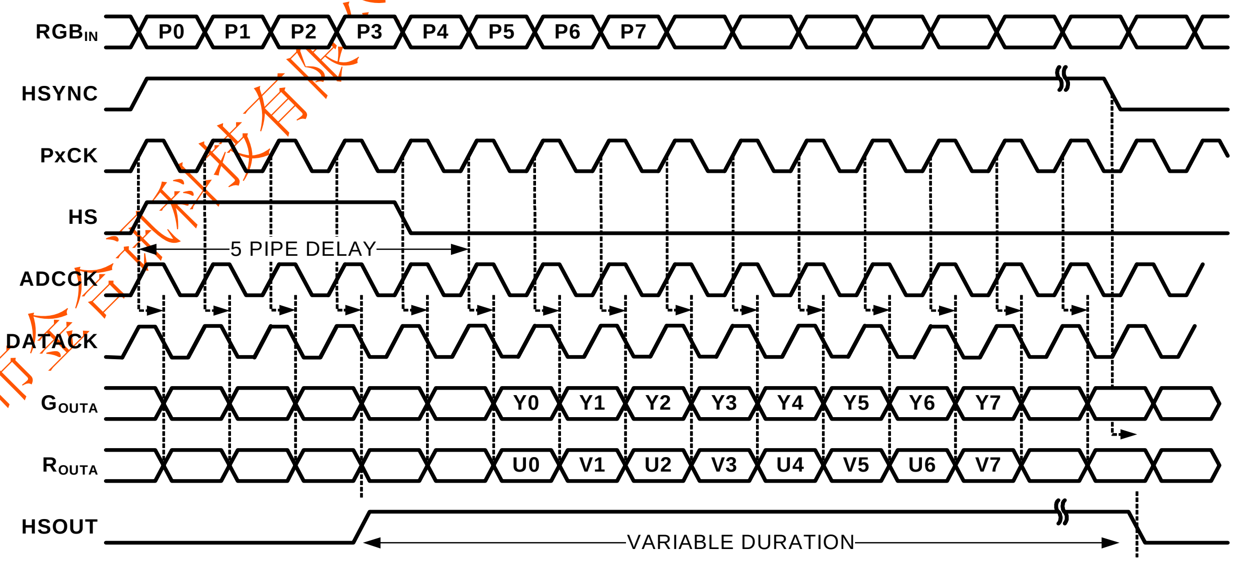


Figure 8. 4:2:2 Mode (For YUV Only)

2-WIRE SERIAL CONTROL PORT

A 2-wire serial interface control interface is provided. Up to two CAT9883C devices may be connected to the 2-wire serial interface, with each device having a unique address.

The 2-wire serial interface comprises a clock (SCL) and a bidirectional data (SDA) pin. The analog flat panel interface acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on SCL and SDA are pulled high by external pull-up resistors.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA must change only when SCL is low. If SDA changes state while SCL is high, the serial interface interprets that action as a start or stop sequence.

There are five components to serial bus operation:

I. Start Signal
II. Slave Address Byte
III. Base Register Address Byte
IV. Data Byte to Read or Write
V. Stop Signal

When the serial interface is inactive (SCL and SDA are high) communications are initiated by sending a start signal. The start signal is a high-to-low transition on SDA while SCL is high. This signal alerts all slaved devices that a data transfer sequence is coming.

The first eight bits of data transferred after a start signal comprise a 7-bit slave address (the first seven bits) and a single R/*W* Bit (the eighth bit). The R/*W* Bit indicates the direction of data transfer, read from (1) or write to (0) the slave device. If the transmitted slave address matches the address of the device (set by the state of the SA_{1-0} input pins in Table VI, the CAT9883C acknowledges by bringing SDA low on the ninth SCL pulse. If the addresses do not match, the CAT9883C does not acknowledge.

Table 7. Serial Port Addresses

Bit 7 A6(MSB)	Bit 6 A5	Bit 5 A4	Bit 4 A3	Bit 3 A2	Bit 2 A1	Bit 1 A0
1	0	0	1	1	0	0
1	0	0	1	1	0	1

Data Transfer via Serial Interface

For each byte of data read or written, the MSB is the first bit of the sequence.

If the CAT9883C does not acknowledge the master device during a write sequence, the SDA remains high so the master can generate a stop signal. If the master device does not acknowledge the CAT9883C during a read sequence, the CAT9883C interprets this as "end of data." The SDA remains high so the master can generate a stop signal.

Writing data to specific control registers of the CAT9883C requires that the 8-bit address of the control register of interest be written after the slave address has been established. This control register address is the base address for subsequent write operations. The base address auto-increments by one for each byte of data written after the data byte intended for the base address. If more bytes are transferred than there are available addresses, the address will not increment and remains at its maximum value of 14H. Any base address higher than 14H will not produce an acknowledge signal.

Data is read from the control registers of the CAT9883C in a similar manner. Reading requires two data transfer operations:

The base address must be written with the R/*W* Bit of the slave address byte low to set up a sequential read operation.

Reading (the R/*W* Bit of the slave address byte high) begins at the previously established base address. The address of the read register auto increments after each byte is transferred.

To terminate a read/write sequence to the CAT9883C, a stop signal must be sent. A stop signal comprises a low-to-high transition of SDA while SCL is high.

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

Serial Interface Read/Write Examples

Write to one control register

I. Start Signal
II. Slave Address Byte (R/*W* Bit = Low)
III. Base Address Byte
IV. Data Byte to Base Address
V. Stop Signal

Write to four consecutive control registers

I. Start Signal
II. Slave Address Byte (R/*W* Bit = Low)
III. Base Address Byte
IV. Data Byte to Base Address
V. Data Byte to (Base Address + 1)
VI. Data Byte to (Base Address + 2)
VII. Data Byte to (Base Address + 3)
VIII. Stop Signal

Read from one control register

I. Start Signal
II. Slave Address Byte (R/*W* Bit = Low)
III. Base Address Byte
IV. Start Signal
V. Slave Address Byte (R/*W* Bit = High)
VI. Data Byte from Base Address
VII. Stop Signal

Read from four consecutive control registers ~ Start Signal

I. Slave Address Byte (R/*W* Bit = Low)
II. Base Address Byte
III. Start Signal
IV. Slave Address Byte (R/*W* Bit = High)
V. Data Byte from Base Address
VI. Data Byte from (Base Address + 1)
VII. Data Byte from (Base Address + 2)
VIII. Data Byte from (Base Address + 3)
IX. Stop Signal

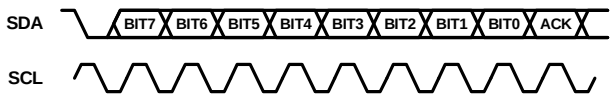


Fig 9. Serial Interface-Typical Byte Transfer

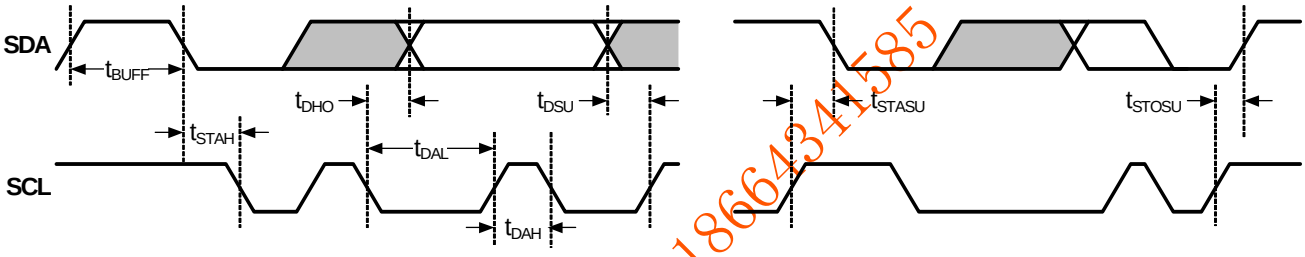


Figure 10. Serial Port Read/Write Timing

Table 8. Serial Port Read/Write Timing

Parameter	Min. Value	Unit
t_{BUFF}	4.7	µS
t_{STAH}	4.0	µS
t_{DHO}	0.3	µS
t_{DAL}	4.7	µS
t_{DAH}	4.0	µS
t_{DSU}	0.3	µS
t_{STASU}	4.0	µS
t_{STOSU}	4.0	µS

PCB Layout Design Guide

PCB LAYOUT RECOMMENDATIONS

Analog Interface Inputs

I. Place the CAT9883C as close as possible to the video connector(s).

II. Place the 75Ohm termination resistors as close to the CAT9883C chip as possible.

III. Use 75Ohm matched impedance traces.

IV. It is recommended that the R, G and B signal traces from video connectors to chip inputs should be on the same layer where the chip resides.

V. Reduce the amount of noise that gets coupled to the inputs.

VI. Avoid running any digital traces near the analog inputs.

VII. Low-pass filtering the analog inputs can sometimes help to reduce noise. This can be achieved by:

A. Placing a series ferrite bead prior to the 75Ohm termination resistor.

B. Placing a 100Ohm to 120Ohm resistor between the 75Ohm termination resistor and the input coupling capacitor.

Power Supply Bypassing

I. It is recommended to bypass each group of power supply pin with a 0.1µF capacitor.

II. It is also recommended that the bypass capacitor be located within about 0.5cm distance of each power pin.

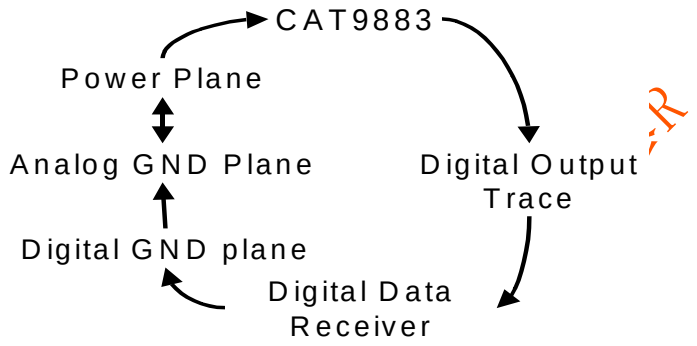
III. Avoid placing the capacitor on the opposite side of the PC board from the CAT9883C.

IV. Do not make the power connection between the capacitor and the power pin.

V. It is particularly important to maintain low noise and good stability of PVD (better to provide separate regulated supplies for VD and PVD).

VI. It is also recommended to use a single ground plane for the entire board (at least place a single ground plane under the CAT9883C).

VII. Notice the longest current loop as shown in the following graph. Shorter loop makes better performance.



PLL

I. Place the PLL loop filter components as close to the FILT pin as possible.

II. It is recommended that the PLL loop filter components should be on the same layer where the chip resides.

III. Do not place any digital or other high frequency traces near these components.

IV. Use the values suggested in the data sheet with 10% tolerances or less.

Outputs (Both Data and Clocks)

I. Try to minimize the trace length that the digital outputs have to drive.

II. It's recommended to add a series resistor of value 22Ohm to 100Ohm to suppress reflections, reduce EMI, and reduce the current spikes inside the CAT9883C.

III. The series resistors should be place as close to the CAT9883C pins as possible.

IV. Try not to add vias or extra length to the output trace in order to get the resistors closer.

V. If possible, limit the capacitance that each of the digital outputs drives less than 10pF.

Digital Inputs

I. Minimize the Hsync/Vsync trace length and do not run any digital or other high frequency traces near it.

Voltage Reference

I. Bypass with a 0.1 µF capacitor.

II. It is recommended that the Midscv and Ref_Bypass pin bypass capacitors should be on the same layer where the chip resides.

III. Place as close to the CAT9883C pin as possible.

IV. Make the ground connection as short as possible.

2-Wire Serial Register Map

The CAT9883C is initialized and controlled by a set of registers, two-line serial interface port, which determine the operating modes. An external controller is employed to write and read the control registers through the employed to write and read the control registers through the two-line serial interface port.

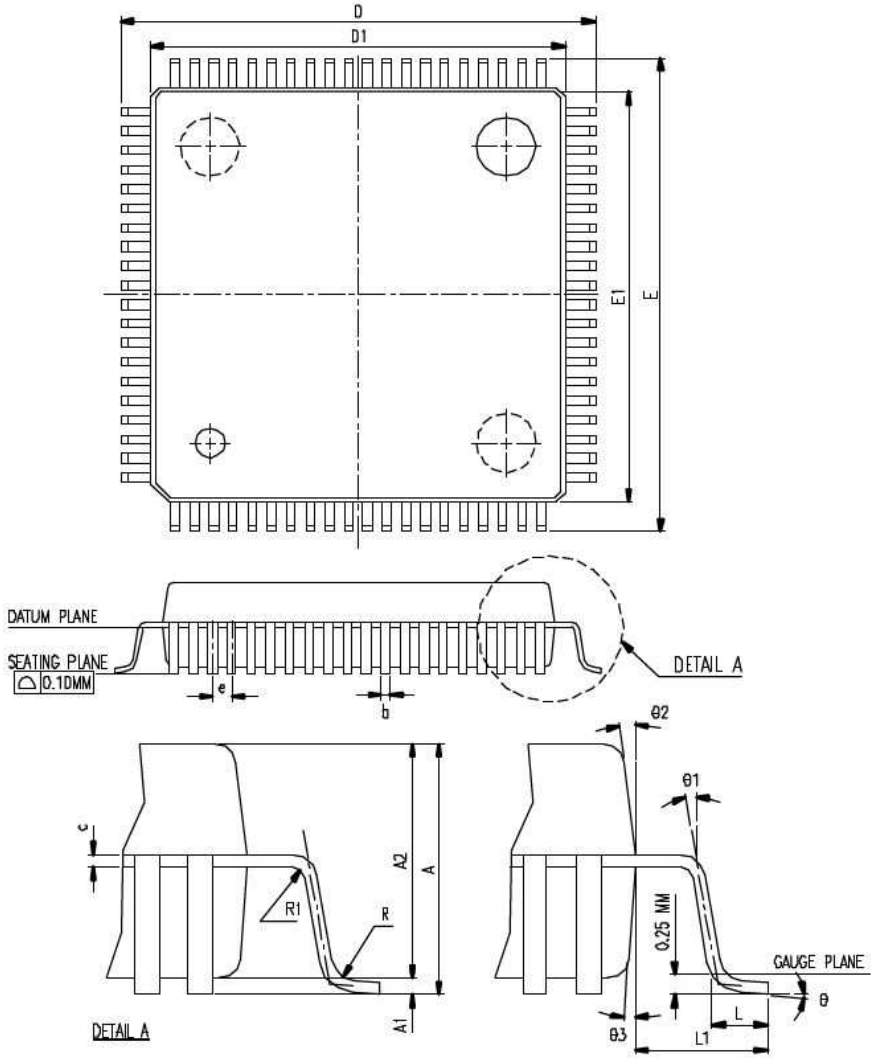
Table 9. Control Register Map

Hex Address	Write and Read or Read Only	Bits	Default Value	Register Name	Function
00H	RO	7:0		Chip Revision	An 8-bit register that represents the silicon revision level. Revision 0 = 0000 0000.
01H*	R/*W*	7:0	01101001	PLL Div MSB	This register is for Bits [11:4] of the PLL divider. Greater values mean the PLL operates at a faster rate. This register should be loaded first whenever a change is needed. This will give the PLL more time to lock.
02H*	R/*W*	7:4	1101****	PLL Div LSB	Bits [7:4] of this word are written to the LSBs [3:0] of the PLL divider word.
03H	R/*W*	7:3	01******		Bits [7:6] VCO Range. Selects VCO frequency range.
			001*		Bits [5:3] Charge Pump Current. Varies the current that drives the low-pass filter.
04H	R/*W*	7:3	10000***	Phase Adjust	ADC Clock Phase Adjustment. Larger values mean more delay. (1 LSB = T/32)
05H	R/*W*	7:0	10000000	Clamp Placement	Places the Clamp signal an integer number of clock periods after the trailing edge of the Hsync signal.
06H	R/*W*	7:0	10000000	Clamp Duration	Number of clock periods that the Clamp signal is actively clamping.
07H	R/*W*	7:0	00100000	Hsync Output Pulsewidth	Sets the number of pixel clocks that HSOUT will remain active.
08H	R/W	7:0	10000000	Red Gain	Controls ADC input range (contrast) of each respective channel. Greater values give less contrast.
09H	R/W	7:0	10000000	Green Gain	
0AH	R/W	7:0	10000000	Blue Gain	
0BH	R/W	7:1	1000000*	Red Offset	Controls dc offset (brightness) of each respective channel. Greater values decrease brightness.
0CH	R/W	7:1	1000000*	Green Offset	
0DH	R/W	7:1	1000000*	Blue Offset	
0EH	R/*W*	7:0	0******	Sync Control	Bit 7 – Hsync Polarity Override. (Logic 0 = Polarity determined by chip, Logic 1 = Polarity set by Bit 6 in register 0EH.)
			*1******		Bit 6 – Hsync Input Polarity. Indicates polarity of incoming Hsync signal to the PLL. (Logic 0 = Active Low, Logic 1 = Active High.)
			0***		Bit 5 – Hsync Output Polarity. (Logic 0 = Logic High Sync, Logic 1 = Logic Low Sync.)
			0*		Bit 4 – Active Hsync Override. If set to Logic 1, the user can select the Hsync to be used via Bit 3. If set to Logic 0, the active interface is selected via Bit 6 in register 14H.
			****0***		Bit 3 – Active Hsync Select. Logic 0 selects Hsync as the active sync. Logic 1 selects Sync-on-Green as the active sync. Note that the indicated Hsync will be used only if Bit 4 is set to Logic 1 or if both syncs are active. (Bits 1, 7 = Logic 1 in register 14H.)
			*****0**		Bit 2 – Vsync Output Invert. (Logic 1 = No Invert, Logic 0 = Invert.)
			******0*		Bit 1 – Active Vsync Override. If set to Logic 1, the user can select the Vsync to be used via Bit 0. If set to Logic 0, the active interface is selected via Bit 3 in register 14H.

			*******0		Bit 0 – Active Vsync Select. Logic 0 selects Raw Vsync as the output Vsync. Logic 1 selects Sync Separated Vsync as the output Vsync. Note that the indicated Vsync will be used only if Bit 1 is set to Logic 1
0FH	R/W	7:1	0*******		Bit 7 – Clamp Function. Chooses between Hsync for Clamp signal or another external signal to be used for clamping. (Logic 0 = Hsync, Logic 1 = Clamp.)
			*1******		Bit 6 – Clamp Polarity. Valid only with external Clamp signal. (Logic 0 = Active High, Logic 1 Selects Active Low.)
			0***		Bit 5 – Coast Select. Logic 0 selects the coast input pins to be used for the PLL coast. Logic 1 selects Vsync to be used for the PLL coast.
			0*		Bit 4 – Coast Polarity Override. (Logic 0 = Polarity determined by chip, Logic 1 = Polarity set by Bit 3 in register 0FH.)
			****1***		Bit 3 – Coast Polarity. Selects polarity of external Coast signal. (Logic 0 = Active Low, Logic 1 = Active High.)
			*****1**		Bit 2 – Seek Mode Override. (Logic 1 = Allow Low Power Mode, Logic 0 = Disallow Low Power Mode.)
			****** 1*		Bit 1 – PWRDN. Full Chip Power-Down, Active Low. (Logic 0 = Full Chip Power-Down, Logic 1 = Normal.)
10H	R/W	7:3	10111 ***	Sync-on-Green	Sync-on-Green Threshold. Sets the voltage level of the Sync-on-Green slicer's comparator.
			*****0**	Threshold	Bit 2 – Red Clamp Select. Logic 0 selects clamp to ground. Logic 1 selects clamp to midscale (voltage at Pin 37).
			******0*		Bit 1 – Green Clamp Select. Logic 0 selects clamp to ground. Logic 1 selects clamp to midscale (voltage at Pin 37).
			*******0		Bit 0 – Blue Clamp Select. Logic 0 selects clamp to ground. Logic 1 selects clamp to midscale (voltage at Pin 37).
11H	R/W	7:0	00100000	Sync Separator Threshold	Sync Separator Threshold. Sets how many internal 5 MHz clock periods the sync separator will count to before toggling high/low. This should be set to some number greater than the maximum Hsync or equalization pulsewidth.
12H	R/W	7:0	00000000	Pre-Coast	Pre-Coast. Sets the number of Hsync periods that Coast becomes active prior to Vsync.
13H	R/W	7:0	00000000	Post-Coast	Post-Coast. Sets the number of Hsync periods that Coast stays active following Vsync.
14H	RO	7:0		Sync Detect	Bit 7 – Hsync detect. It is set to Logic 1 if Hsync is present on the analog interface; otherwise it is set to Logic 0.
					Bit 6 – AHS: Active Hsync. This bit indicates which analog Hsync is being used. (Logic 0 = Hsync Input Pin, Logic 1 = Hsync from Sync-on-Green.)
					Bit 5 – Input Hsync Polarity Detect. (Logic 0 = Active Low, Logic 1 = Active High.)
					Bit 4 – Vsync Detect. It is set to Logic 1 if Vsync is present on the analog interface; otherwise it is set to Logic 0.
					Bit 3 – AVS: Active Vsync. This bit indicates which analog Vsync is being used. (Logic 0 = Vsync Input Pin, Logic 1 = Vsync from Sync Separator.)
					Bit 2 – Output Vsync Polarity Detect. (Logic 0 = Active Low, Logic 1 = Active High.)
					Bit 1 – Sync-on-Green Detect. It is set to Logic 1 if sync is present on the Green video input; otherwise it is set to 0.
					Bit 0 – Input Coast Polarity Detect. (Logic 0 = Active Low, Logic

					1 = Active High.)
15H	R/*W*	7:0	1111****	Test Register	Bits [7:4] Reserved for future use.
			****1***		Bit 3 – Reserved for future use.
			*****1**		Bit 2 – Reserved for future use.
			******1*		Bit 1 – 4:2:2 Output Formatting Mode (Logic 0 = 4:2:2 mode, Logic 1=4:4:4 mode)
			*******1		Bit 0 – Reserved for future use.
16H	R/*W*	7:0		Test Register	Reserved for future use.
17H	RO	7:0		Test Register	Reserved for future use.
18H	RO	7:0		Test Register	Reserved for future use.
84H	R/*W*	7:0	0000****	Calibration	Default Setting; Must set to 0000 for proper operation.
			****00**		Calibration Mode Setting: “00” for no calibration; “01” for offset calibration; “10” for white balance calibration; “11” for AGC control on TV signal;
			******11		Default Setting; Must set to 11 for proper operation.
85H	R/*W*	6:6	*1******	Data output Enable	Data output Enable; Logic 0=Tri-State Output
80H~85H	Reserved for future use or customerization. Please contact CAT for more details.				

PACKAGE OUTLINE DIMENSION

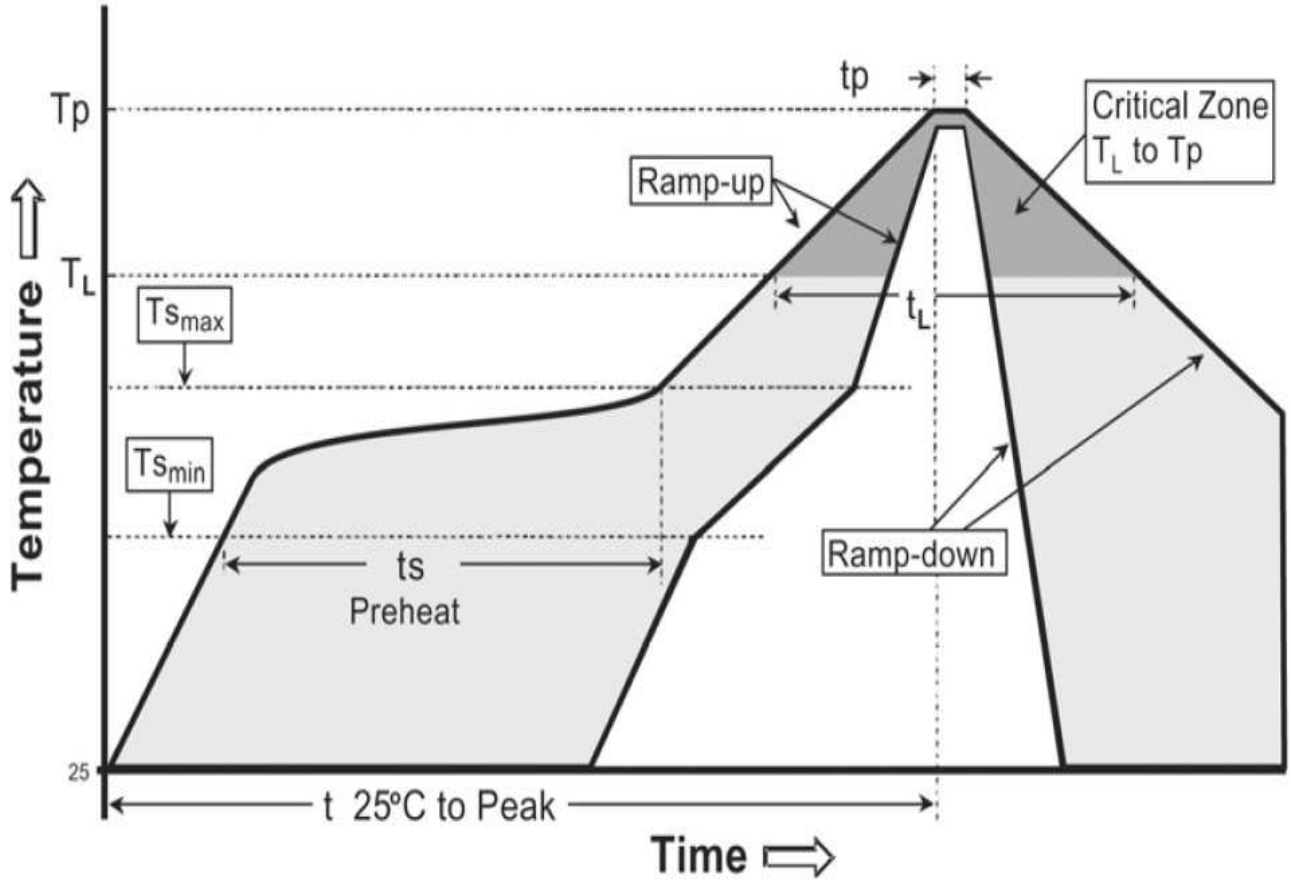


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN	NOM	MAX
A			1.60			0.063
A1	0.05		0.15	0.001		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.22	0.30	0.33	0.009	0.012	0.013
c	0.09		0.16	0.004		0.006
e	0.65 BASIC			0.026 BASIC		
D	16.00 BASIC			0.630 BASIC		
D1	14.00 BASIC			0.551 BASIC		
E	16.00 BASIC			0.630 BASIC		
E1	14.00 BASIC			0.551 BASIC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
R1	0.08			0.003		
R	0.08		0.20	0.003		0.008
θ	0	3.5	7	0	3.5	7
θ1	0			0		
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
JEDEC	MS-026 (BEC)					

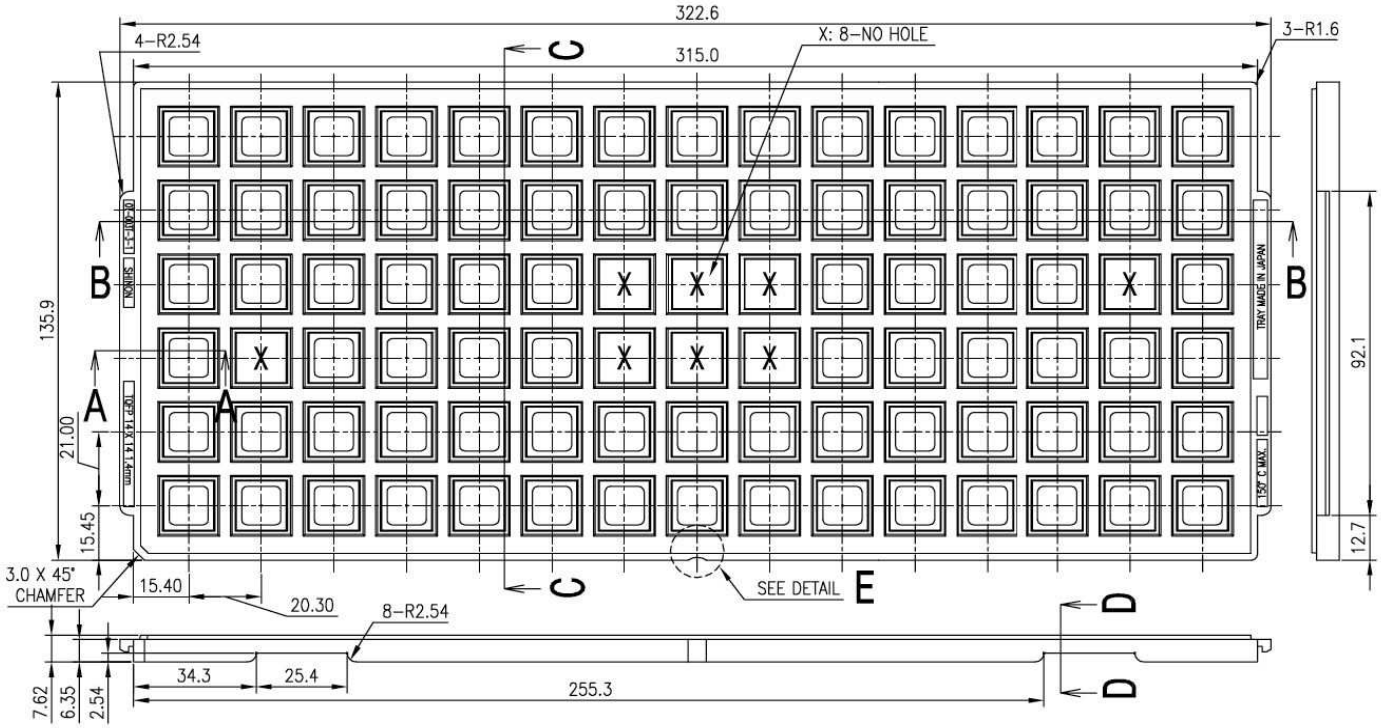
Classification Reflow Profiles

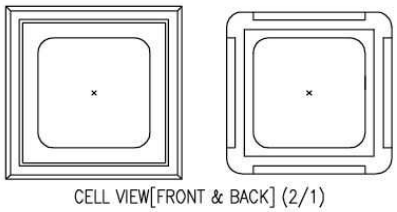
Reflow Profile	Pb-Free Assembly
Average Ramp-Up Rate (Ts_{max} to Tp)	3℃/second max.
Preheat -Temperature Min(Ts_{min}) -Temperature Max(Ts_{max}) -Time(ts_{min} to ts ts_{max})	 150℃ 200℃ 60-180 seconds
Time maintained above: -Temperature(T_L) -Time(t_L)	217℃ 60-150 seconds
Peak Temperature(Tp)	260 +0 /-5℃
Time within 5 ℃ of actual Peak Temperature(tp)	20-40 seconds
Ramp-Down Rate	6℃/second max.
Time 25℃ to Peak Temperature	8 minutes max.

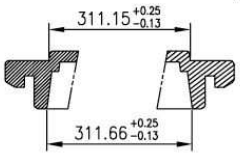
Note: All Temperature refer to topside of the package, measured on the package body surface.



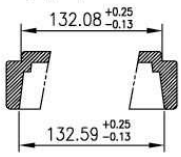
Carrier Tray Dimensions



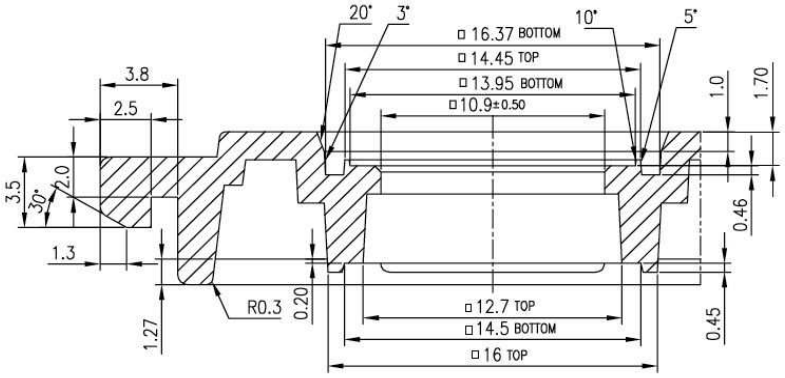

CELL VIEW[FRONT & BACK] (2/1)



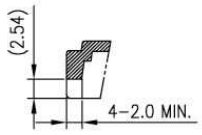
SECTION B–B(3/2)



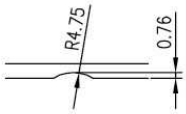
SECTION C–C(3/2)



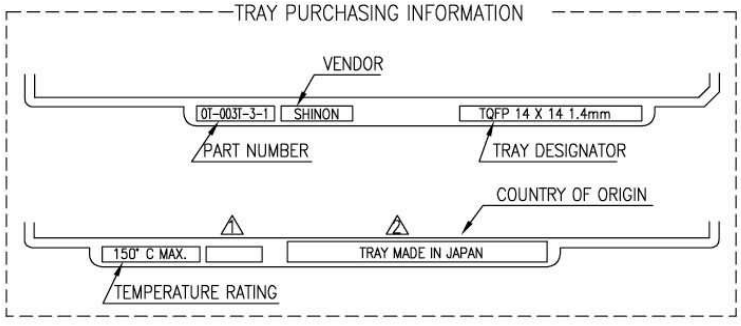
SECTION A–A(4/1)



SECTION D–D(3/2)



DETAIL E (3/2)



NOTES

1.SURFACE ELECTRIC RESISTIVITY:1×10 ~9×10 Ω/□. (BY TEST ASTM D257)

2.WARPAGE IS WITHN 0.76mm.

HEADQUARTERS:
3F, No.1, Jin-Shan 8th St., Hsin-Chu City 300, Taiwan (R.O.C.)
Tel: +886-3-666-8301
Fax: +886-3-666-8630
Website: http://www.chipadvanced.com

TAIPEI OFFICE:
4F, No.112, Jhouzih St., Neihu District, Taipei City 114, Taiwan (R.O.C.)
Tel: +886-2-87516119
Fax: +886-2-87516359