RK61X
Brief

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Revision History

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Chapter 1 Introduction

RK61X is a partner chip for Rockchip mobile application processor. It can minimize the external components in Rockchip's Table and TV BOX solution; reduce the total cost and PCB size.

RK61X includes two RGB display input interface with double data rate. With the internal MUX function, it can output 1080P HDMI signal to TV and output RGB/LVDS/MIPI signal to TFT panel. In this case, RK61X can support dual panel (TV and TFT)display.

RK61X includes a audio codec, which with two I2S/PCM interface, two differential microphone input and audio processing function.

RK61X provides a complete set of display interface to support very flexible applications as follows :

- 2 RGB display input interface with double data rate
- 1 LVDS display output interface with double channels
- 1 MIPI display output interface with 4 data lanes
- 1 HDMI display output interface
- 1 RGB display input interface shared with LVDS
- 1 RGB display input interface shared with RGB display input interface
- Audio interface: one 4ch I2S/PCM interface, one 1ch I2S/PCM interface and one SPDIF rx interface
- I2Cconfigured interface

This document will provide guideline on how to use RK61X correctly and efficiently. The chapter 1 will introduce the features, block diagram, signal descriptions and system usage of RK61X, the chapter 2 to chapter 15 will describe the full function of each module in detail.

RK61X contains two versions:RK616 and RK618,the difference like follow：For RK616 ,it contains the chapters2,3,4,5,,8,9,10,12,13. For RK618,it contains the all chapters.

Table 11 The difference of RK616 and RK618

	RK616	RK618
PACKAGE	144-L	216-L
HDMI	support	support
SINGLE LVDS	support	support
DOUBLE LVDS	don't support	support
MIPI	don't support	support
ACODEC Normal	support	support
VIF/SCALER	support	support

1.1 Features

1.1.1 Display interface

- Two 24BIT RGB input interface with dual data rate

- supports MIPI,LVDS and RGB interface to TFT LCD
- With scaler function, LVDS/MIPI/RGB and HDMI can output at the same time

1.1.2 HDMI

- Very low power operation, less than 60mW in PHY during 1080P HD display
- HDMI 1.4/1.3/1.2/1.1, HDCP 1.2 and DVI 1.0 standard compliant transmitter
- Supports data rate from 25MHz, 1.65bps up to 3.4Gbps over a Single channel HDMI
- Support 3D function defined in HDMI 1.4 spec
- TMDS Tx Drivers with programmable output swing, resister values and pre-emphasis
- Supports all DTV resolutions including 480i/576i/480p/576p/720p/1080i/1080p
- Digital video interface supports a pixel size of 24bits color depth in RGB
- S/PDIF output supports PCM, Dolby Digital, DTS digital audio transmission (32-192kHz Fs) using IEC60958 and IEC 61937
- Multiphase 4MHz fixed bandwidth PLL with low jitter
- DDC Bus I2C master interface at 3.3V
- HDCP encryption and decryption engine contains all the necessary logic to encrypt the incoming audio and video data
- Support HDMI LipSync if needed as addon feature
- Lower power operation with optimal power management feature
- Embedded ESD, scan support logic.
- The EDID and CEC function are also supported by HDMI Transmitter Controller
- Optional Monitor Detection supported through Hot Plug

1.1.3 LVDS

- 35MHz~150MHz clock support
- 28:4 data channel compression at data rates up to 945 Mbps per channel
- Support VGA,SVGA,XGA and single pixel SXGA
- Comply with the Standard TIA/EIA-644-A LVDS stand
- Support 8bit format-1, format-2, format-3 display mode, Support 6bit display mode.
- Display mode can be select by input MUX
- Low power mode

1.1.4 MIPI D-PHY

- Mixed-signal D-PHY mixed-signal hard-macro- LS Transmitter and LS/HS Receiver solution
- Designed to MIPI® v1.0 Specifications
- Integrated PHY Protocol Interface (PPI) supports interface to CSI, DSI and UniPro™ MIPI® protocols
- 1.0GHz maximum data transfer rate per lane
- Expandable to support 4 data lanes, providing up to 4Gbps transfer rate
- HS, LP and ULPS modes supported
- 10Mbps per lane in low-power mode
- Unidirectional and bi-directional modes supported
- Automatic termination control for HS and LP modes

- Low-Power dissipation: HS less than 3mA/Lane
- Tx/Rx Buffers with tunable On-Die-Termination and advanced equalization.
- Embedded ESD, boundary scan support logic.

1.1.5 MIPI Controller

- Support video and command modes
- PPI interface to the D-PHY
- Configurable from 1 to 4 data lanes output
- Supports up to 1Gb/s per data lane
- Bi-directional communication and escape mode support
- Programmable display resolutions, up to 2048x1080
- Multiple peripheral support capability with configurable virtual channels
- Video mode pixel formats: RGB565, RGB666 packed and loosely, RGB888
- Supports transmission of all generic commands
- ECC and checksum capabilities
- Supports ultra-low power mode
- Fault recovery schemes

1.1.6 Scaler

- Support max line pixel input upto 2560
- Support scaling down and scale up function
- Max output resolution 2048x1536

1.1.7 Audio Codec

- Two I2S/PCM interface
- Pure logic process, no need for Mixed signal process.
- Very low power, can be made <6.5mA in 3.3V for playback.
- 18 to 24 bit high order Sigma-Delta modulation for DAC with >93 dB SNR.
- 16 to 18 bit high order Sigma-Delta modulation for ADC with >90 dB SNR.
- Digital interpolation and decimation filter integrated.
- Line-in, microphone and speaker out interface.
- On-chip analog post filter and digital filters.
- Single–ended or differential microphone input.
- Automatic gain control for smooth audio recording.
- Sampling rate of 8k/12k/16k/24k/32k/48k/44.1k/96k Hz
- Support 16ohm to 32ohm headphone and speaker phone output.
- 3.3V analog +/-10% power supply for analog and 1.2/1.1/1.0V for digital core.
- Mono, Stereo supported.

1.1.8 Chip controll

- I2C slave interface
- External clock input for Chip working, this clock can share with MCLK (12M)
- Interrupt output for HDMI in and other function
- Two PLL , one for dual datarate input logic; the other for scaler

1.2 Block Diagram

The following diagram shows the basic block diagram for RK61X

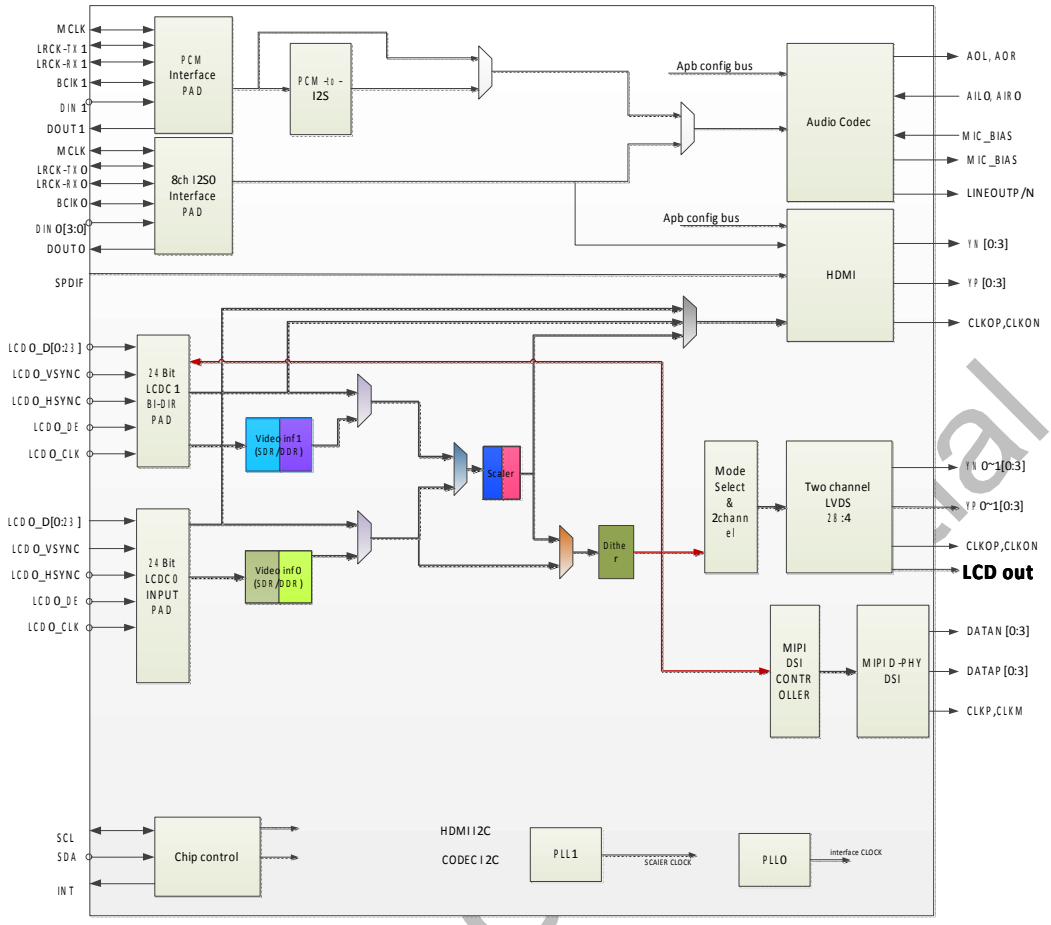

Fig. 11 RK61X Block Diagram

1.3 Pin Description

In this chapter, the pin description is all power/ground descriptions in Table 1-1, include analog power/ground.

1.3.1 RK61X power/ground IO descriptions

Table 12 RK616 Power/Ground IO informations

Group	Ball #	Min(V)	Typ(V)	Max(V)	Descriptions
GND	C3,C5,B7,C6,D5,F6,F7,G7,J11 , L10,E8,F9,C10,B12	N/A	N/A	N/A	Internal Core Ground and Digital IO Ground
VCC	G5,J6	N/A	3.3	N/A	Digital IO Power

VDD	F5,F8,H7,D10	N/A	1.2	N/A	Internal Core Power
LVDS_VCC	A11,A12,B11, E10,F10	N/A	2.5	N/A	LVDS Analog power
PLL1VDD_1V2	J10	N/A	1.2	N/A	PLL1 1.2 power
PLL2VDD_1V2	K10	N/A	1.2	N/A	PLL2 1.2 power
PLL1VDD_3V3	K10	N/A	3.3	N/A	PLL1 3.3 power
PLLVSS	K11	N/A	N/A	N/A	PLL analog ground
AVCC	C4,C7 A7,B8,B9	N/A	3.3	N/A	HDMI 3.3 analog power CODEC Analog power
HDMIVDD	D6	N/A	1.2	N/A	HDMI 1.2 analog power
CODEC_AVSS	C8,D7	N/A	N/A	N/A	CODEC Analog ground

Table 13 RK618 Power/Ground IO informations

Group	Ball #	Min(V)	Typ(V)	Max(V)	Descriptions
GND	C3,C8,C11,C14,F6,F7,F9 F11,G7,G8,G9,G10,H7,H8,H9 H10,J2,J6,J7,J8,J9,J10,K6,K7 K8,K9,K10,K11,L6,L9,L10,L11 P9,P12,R3	N/A	N/A	N/A	Internal Core Ground and Digital IO Ground
VCC	F8,G6,L7	N/A	3.3	N/A	Digital IO Power
VDD	H6,F10,L8	N/A	1.2	N/A	Internal Core Power
LVDS_VCC	P6,P8,P11	N/A	2.5	N/A	LVDS Analog power
PLL1VDD_1V2	L4	N/A	1.2	N/A	PLL1 1.2 power
PLL2VDD_1V2	L4	N/A	1.2	N/A	PLL2 1.2 power
PLL1VDD_3V3	L1	N/A	3.3	N/A	PLL1 3.3 power

PLLVSS	K2	N/A	N/A	N/A	PLL analog ground
AVCC	R16,H16,K16	N/A	3.3	N/A	HDMI 3.3 analog power CODEC Analog power
HDMIVDD	K15	N/A	1.2	N/A	HDMI 1.2 analog power
CODEC_AVSS	A7,B8,B9	N/A	N/A	N/A	CODEC Analog ground
HDMI_AVSS	L14,M14,P14,R15	N/A	N/A	N/A	HDMI Analog ground
MIPIPLL_2V5	M4	N/A	2.5	N/A	MIPI PLL analog power
MIPIAVDD_1V2	L3	N/A	1.2	N/A	MIPI analog power
MIPI_AVSS	L2,M3,P3,T3	N/A	N/A	N/A	MIPI analog ground

1.3.2 RK61X function IO descriptions

Table 14 RK61X IO descriptions

Port name	BALL# (144-L) RK616	BALL# (216-L) RK618	Pad dir	Reset value	Pull up/down	Power Supply	Pin Description
IO_LCDC1_DATA[8]	H8	E1	I/O	input	pull down	LCDC	LCD interface 1 data 8
IO_LCDC1_DATA[7]	G8	F5	I/O	input	pull down	LCDC	LCD interface 1 data 7
IO_LCDC1_DATA[6]	M9	F4	I/O	input	pull down	LCDC	LCD interface 1 data 6
IO_LCDC1_DATA[5]	L9	F3	I/O	input	pull down	LCDC	LCD interface 1 data 5
IO_LCDC1_DATA[4]	K9	F2	I/O	input	pull down	LCDC	LCD interface 1 data 4
IO_LCDC1_DATA[3]	J9	F1	I/O	input	pull down	LCDC	LCD interface 1 data 3
IO_LCDC1_DATA[2]	H9	G1	I/O	input	pull down	LCDC	LCD interface 1 data 2
IO_LCDC1_DATA[1]	G9	G2	I/O	input	pull down	LCDC	LCD interface 1 data 1
IO_LCDC1_DATA[0]	M10	H5	I/O	input	pull down	LCDC	LCD interface 1 data 0
IO_LCDC1_DEN	M11	H4	I/O	input	pull down	LCDC	lcdc1 data enable signal
IO_LCDC1_DCLKP	L11	H1	I/O	input	pull down	LCDC	lcdc1 clock out
IO_LCDC1_DCLKN	---	H2	I/O	input	pull down	LCDC	lcdc1 clock out(Negative)
IO_LCDC1_HSYNCN	M12	J1	I/O	input	pull down	LCDC	lcdc0 horizontal sync signal
IO_LCDC1_VSYNCN	L12	K1	I/O	input	pull down	LCDC	lcdc0 vertical sync signal
IO_I2S1SDO	H12	H3	O		pull down	LCDC	I2S1 SDO
IO_I2S1BCLK	J12	J5	I/O		pull down	LCDC	I2S1 SCLK
IO_I2S1SLRCKRX	K12	J4	I/O		pull down	LCDC	I2S1 LRCK for ADC
IO_I2S1SLRCKTX	H11	J3	I/O		pull down	LCDC	I2S1 LRCK for DAC
IO_I2S1SDI	G10	L5	I		pull down	LCDC	I2S1 SDI
IO_MIPIPHY_DATAN0	---	M1	A			MIPIPHY	MIPI data lane0 serial data output(Negative)
IO_MIPIPHY_DATAP0	---	M2	A			MIPIPHY	MIPI data lane0 serial data output
IO_MIPIPHY_DATAN1	---	N1	A			MIPIPHY	MIPI data lane1 serial data output(Negative)
IO_MIPIPHY_DATAP1	---	N2	A			MIPIPHY	MIPI data lane1 serial data output
IO_MIPIPHY_CLKN	---	P1	A			MIPIPHY	MIPI clock lane serial data output(Negative)
IO_MIPIPHY_CLKP	---	P2	A			MIPIPHY	MIPI clock lane serial data output
IO_MIPIPHY_DATAP2	---	R2	A			MIPIPHY	MIPI data lane2 serial data output
IO_MIPIPHY_DATAN2	---	R1	A			MIPIPHY	MIPI data lane2 serial data output(Negative)
IO_MIPIPHY_DATAP3	---	T2	A			MIPIPHY	MIPI data lane3 serial data output
IO_MIPIPHY_DATAN3	---	T1	A			MIPIPHY	MIPI data lane3 serial data output(Negative)
IO_LCDC_DEN	---	R4	O	0	pull down	RGB	lcdc data enable signal(LVDS used as RGB Output)
IO_LCDC_DCLK	---	T4	O	0	pull down	RGB	lcdc clock out
IO_LCDC_HSYNCN	---	N5	O	0	pull down	RGB	lcdc horizontal sync signal
IO_LCDC_VSYNCN	---	M6	O	0	pull down	RGB	lcdc0 vertical sync signal
IO_LCDC_DATA23	---	P5	O	0	pull down	RGB	LCD interface data 23
IO_LCDC_DATA22	---	N6	O	0	pull down	RGB	LCD interface data 22
IO_LCDC_DATA21	---	N8	O	0	pull down	RGB	LCD interface data 21
IO_LCDC_DATA20	---	M8	O	0	pull down	RGB	LCD interface data 20

IO_LVDS_PADN_8	---	T5	A			LVDS	Transmit serial data out (Negative), n=1~8
IO_LVDS_PADP_8	---	R5	A			LVDS	Transmit serial data out, n=1~8
IO_LVDS_CLKN2	---	T6	A			LVDS	Output clock (Negative)
IO_LVDS_CLKP2	---	R6	A			LVDS	Output clock
IO_LVDS_PADN_7	---	T7	A			LVDS	Transmit serial data out (Negative), n=1~8
IO_LVDS_PADP_7	---	R7	A			LVDS	Transmit serial data out, n=1~8
IO_LVDS_PADN_6	---	T8	A			LVDS	Transmit serial data out (Negative), n=1~8
IO_LVDS_PADP_6	---	R8	A			LVDS	Transmit serial data out, n=1~8
IO_LVDS_PADN_5	---	T9	A			LVDS	Transmit serial data out (Negative), n=1~8
IO_LVDS_PADP_5	---	R9	A			LVDS	Transmit serial data out, n=1~8
IO_LVDS_XRES	E9	T15	A			LVDS	LVDS current biasing generation,Connect 12Kohm resistor to ground
IO_LVDS_PADN_4	C11	T10	A			LVDS	Transmit serial data out, n=1~8
IO_LVDS_PADP_4	C12	R10	A			LVDS	Transmit serial data out (Negative), n=1~8
IO_LVDS_CLKN1	E11	T11	A			LVDS	Output clock (Negative)
IO_LVDS_CLKP1	E12	R11	A			LVDS	Output clock
IO_LVDS_PADN_3	D11	T12	A			LVDS	Transmit serial data out (Negative), n=1~8
IO_LVDS_PADP_3	D12	R12	A			LVDS	Transmit serial data out, n=1~8
IO_LVDS_PADN_2	F11	T13	A			LVDS	Transmit serial data out (Negative), n=1~8
IO_LVDS_PADP_2	F12	R13	A			LVDS	Transmit serial data out, n=1~8
IO_LVDS_PADN_1	G11	T14	A			LVDS	Transmit serial data out (Negative), n=1~8
IO_LVDS_PADP_1	G12	R14	A			LVDS	Transmit serial data out, n=1~8
IO_HDMI_EXTR	A2	T16	A			HDMI	Connect 1.9Kohm resistor to ground to generate reference current.
IO_HDMI_TX3N	A6	P15	A			HDMI	TMDS negative clock line
IO_HDMI_TX3P	B6	P16	A			HDMI	TMDS positive clock line.
IO_HDMI_TX0N	A5	N15	A			HDMI	TMDS channel 0 negative data line.
IO_HDMI_TX0P	B5	N16	A			HDMI	TMDS channel 0 positive data line.
IO_HDMI_TX1N	A4	M15	A			HDMI	TMDS channel 1 negative data line.
IO_HDMI_TX1P	B4	M16	A			HDMI	TMDS channel 1 positive data line.
IO_HDMI_TX2N	A3	L15	A			HDMI	TMDS channel 2 negative data line.
IO_HDMI_TX2P	B3	L16	A			HDMI	TMDS channel 2 positive data line.
IO_ACODEC_IN3L	B10	L13	A			ACODEC	Left line input
IO_ACODEC_IN3R	A10	M13	A			ACODEC	Right line input
IO_ACODEC_MIC1N	C9	J11	A			ACODEC	Negative input for left microphone

IO_ACODEC_MIC1P	---	J12	A			ACODEC	Positive input for left microphone
IO_ACODEC_MICBIAS 1	D9	M11	A			ACODEC	Microphone bias ouput1
IO_ACODEC_MICBIAS 2	---	L12	A			ACODEC	Microphone bias ouput2
IO_ACODEC_MIC2P	---	H13	A			ACODEC	Positive input for right microphone
IO_ACODEC_MIC2N	---	H12	A			ACODEC	Negative input for right microphone
IO_ACODEC_IN1N	---	F12	A			ACODEC	Negative line input
IO_ACODEC_IN1P	---	F13	A			ACODEC	Positive line input
IO_ACODEC_VCM	D8	J16	A			ACODEC	Common mode reference voltage decoupling pin
IO_ACODEC_LINE1	---	F14	A			ACODEC	Line output 1
IO_ACODEC_LINE2	---	H14	A			ACODEC	Line output 2
IO_ACODEC_SPKL	A8	J14	A			ACODEC	Left speaker output
IO_ACODEC_SPKR	A9	J15	A			ACODEC	Right speaker output
NC	---	F15	A			ACODEC	Don`t connected,left floating
NC	---	G15	A			ACODEC	Don`t connected,left floating
NC	---	G16	A			ACODEC	Don`t connected,left floating
NC	---	F16	A			ACODEC	Don`t connected,left floating
NC	---	D15	A			ACODEC	Don`t connected,left floating
NC	---	E15	A			ACODEC	Don`t connected,left floating
NC	---	E16	A			ACODEC	Don`t connected,left floating
NC	---	D16	A			ACODEC	Don`t connected,left floating
IO_HDMI_CEC	E7	E13	I/0		pull up	LCDC	HDMI CEC control line.
IO_HDMI_HDP	E6	C16	I/0		pull up	LCDC	HDMI HPD Hot plug detect
IO_HDMI_I2CSDA	D4	N12	I/0		pull up	LCDC	DDC channel SDA in. For tri - state gate use
IO_HDMI_I2CSCL	E5	N11	I/0		pull up	LCDC	DDC channel SCL in. For tri - state gate use
IO_I2C_SDA	E2	M9	I/0		pull up	LCDC	I2C SDA
IO_I2C_SCL	D1	N9	I		pull up	LCDC	I2C SCL
IO_CLKIN	D2	C15	I		pull down	LCDC	RK61X clock input
IO_I2S0SDO	B2	E14	O		pull down	LCDC	I2S0 sdo
IO_I2S0BCLK	A1	B16	I/O		pull down	LCDC	I2S0 SCLK
IO_I2S0SLRCKRX	B1	B15	I/O		pull down	LCDC	I2S0 LRCK for ADC
IO_I2S0SLRCKTX	C2	A16	I/O		pull down	LCDC	I2S0 LRCK for DAC
IO_I2S0SDI[0]	C1	D12	I		pull down	LCDC	I2S0 sdi[0]
IO_I2S0SDI[1]	D3	E11	I		pull down	LCDC	I2S0 sdi[1]
IO_I2S0SDI[2]	E4	B14	I		pull down	LCDC	I2S0 sdi[2]
IO_I2S0SDI[3]	E3	A15	I		pull down	LCDC	I2S0 sdi[3]
IO_SPDIF	F4	H11	I		pull down	LCDC	SPDIF input
IO_TEST	F3	G11	I		pull down	LCDC	test input
IO_NPOR	F2	A14	I		pull up	LCDC	power on reset
IO_INT	E1	D11	I		pull down	LCDC	RK61X interrupt output
IO_LCDC0_VSYNCN	K5	B13	I		pull down	LCDC	lcdc0 vertical sync signal
IO_LCDC0_HSYNCN	L5	C12	I		pull down	LCDC	lcdc0 horizontal sync signal

IO_LCDC0_DEN	L4	A13	I		pull down	LCDC	lcdc0 data enable signal
IO_LCDC0_DCLKP	M5	A12	I		pull down	LCDC	lcdc0 clock out
IO_LCDC0_DCLKN	---	B12	I		pull down	LCDC	lcdc0 clock out(Negative)
IO_LCDC0_DATA[23]	F1	C9	I		pull down	LCDC	LCD interface 0 data 23
IO_LCDC0_DATA[22]	G1	B11	I		pull down	LCDC	LCD interface 0 data 22
IO_LCDC0_DATA[21]	G2	E9	I		pull down	LCDC	LCD interface 0 data 21
IO_LCDC0_DATA[20]	G3	A11	I		pull down	LCDC	LCD interface 0 data 20
IO_LCDC0_DATA[19]	G4	D9	I		pull down	LCDC	LCD interface 0 data 19
IO_LCDC0_DATA[18]	H1	B10	I		pull down	LCDC	LCD interface 0 data 18
IO_LCDC0_DATA[17]	H2	A10	I		pull down	LCDC	LCD interface 0 data 17
IO_LCDC0_DATA[16]	H3	B9	I		pull down	LCDC	LCD interface 0 data 16
IO_LCDC0_DATA[15]	H4	A9	I		pull down	LCDC	LCD interface 0 data 15
IO_LCDC0_DATA[14]	J1	A8	I		pull down	LCDC	LCD interface 0 data 14
IO_LCDC0_DATA[13]	J2	E8	I		pull down	LCDC	LCD interface 0 data 13
IO_LCDC0_DATA[12]	J3	B8	I		pull down	LCDC	LCD interface 0 data 12
IO_LCDC0_DATA[11]	J4	D8	I		pull down	LCDC	LCD interface 0 data 11
IO_LCDC0_DATA[10]	K1	A7	I		pull down	LCDC	LCD interface 0 data 10
IO_LCDC0_DATA[9]	K2	A6	I		pull down	LCDC	LCD interface 0 data 9
IO_LCDC0_DATA[8]	K3	B7	I		pull down	LCDC	LCD interface 0 data 8
IO_LCDC0_DATA[7]	K4	A5	I		pull down	LCDC	LCD interface 0 data 7
IO_LCDC0_DATA[6]	L1	B6	I		pull down	LCDC	LCD interface 0 data 6
IO_LCDC0_DATA[5]	L2	C6	I		pull down	LCDC	LCD interface 0 data 5
IO_LCDC0_DATA[4]	M1	A4	I		pull down	LCDC	LCD interface 0 data 4
IO_LCDC0_DATA[3]	M2	E6	I		pull down	LCDC	LCD interface 0 data 3
IO_LCDC0_DATA[2]	L3	B5	I		pull down	LCDC	LCD interface 0 data 2
IO_LCDC0_DATA[1]	M3	D6	I		pull down	LCDC	LCD interface 0 data 1
IO_LCDC0_DATA[0]	M4	D5	I		pull down	LCDC	LCD interface 0 data 0
IO_LCDC1_DATA[23]	J5	A3	I/O	input	pull down	LCDC	LCD interface 1 data 23
IO_LCDC1_DATA[22]	H5	A2	I/O	input	pull down	LCDC	LCD interface 1 data 22
IO_LCDC1_DATA[21]	M6	B4	I/O	input	pull down	LCDC	LCD interface 1 data 21
IO_LCDC1_DATA[20]	L6	A1	I/O	input	pull down	LCDC	LCD interface 1 data 20
IO_LCDC1_DATA[19]	K6	C5	I/O	input	pull down	LCDC	LCD interface 1 data 19
IO_LCDC1_DATA[18]	H6	B3	I/O	input	pull down	LCDC	LCD interface 1 data 18
IO_LCDC1_DATA[17]	G6	B2	I/O	input	pull down	LCDC	LCD interface 1 data 17
IO_LCDC1_DATA[16]	M7	B1	I/O	input	pull down	LCDC	LCD interface 1 data 16
IO_LCDC1_DATA[15]	L7	C1	I/O	input	pull down	LCDC	LCD interface 1 data 15
IO_LCDC1_DATA[14]	K7	C2	I/O	input	pull down	LCDC	LCD interface 1 data 14
IO_LCDC1_DATA[13]	J7	D1	I/O	input	pull down	LCDC	LCD interface 1 data 13
IO_LCDC1_DATA[12]	M8	E4	I/O	input	pull down	LCDC	LCD interface 1 data 12
IO_LCDC1_DATA[11]	L8	D2	I/O	input	pull down	LCDC	LCD interface 1 data 11
IO_LCDC1_DATA[10]	K8	E3	I/O	input	pull down	LCDC	LCD interface 1 data 10
IO_LCDC1_DATA[9]	J8	E2	I/O	input	pull down	LCDC	LCD interface 1 data 9

Notes :

①: ***Pad types : I = input , O = output , I/O = input/output (bidirectional) ,***
AP = Analog Power , AG = Analog Ground
DP = Digital Power , DG = Digital Ground
A = Analog

②: ***Output Drive strength is configurable, it's the suggested value in this table. Unit is mA , only Digital IO have drive value***

③: ***Reset state: I = input without any pull resistor O = output***

④: *It is die location. For examples, "Left side" means that all the related IOs are always in left side of die*

⑤: *Power supply means that all the related IOs are in this IO power domain. If multiple powers are included, they are connected together in one IO power ring*

⑥ *The pull up/pull down is configurable.*

1.4 Package information

1.4.1 RK616 Dimension

RK616 package is TFBGA (HF) 10x10 0.8P 144L_2L Substrate

(body: 10mm x 10mm ; ball size : 0.4mm ; ball pitch : 0.8mm)

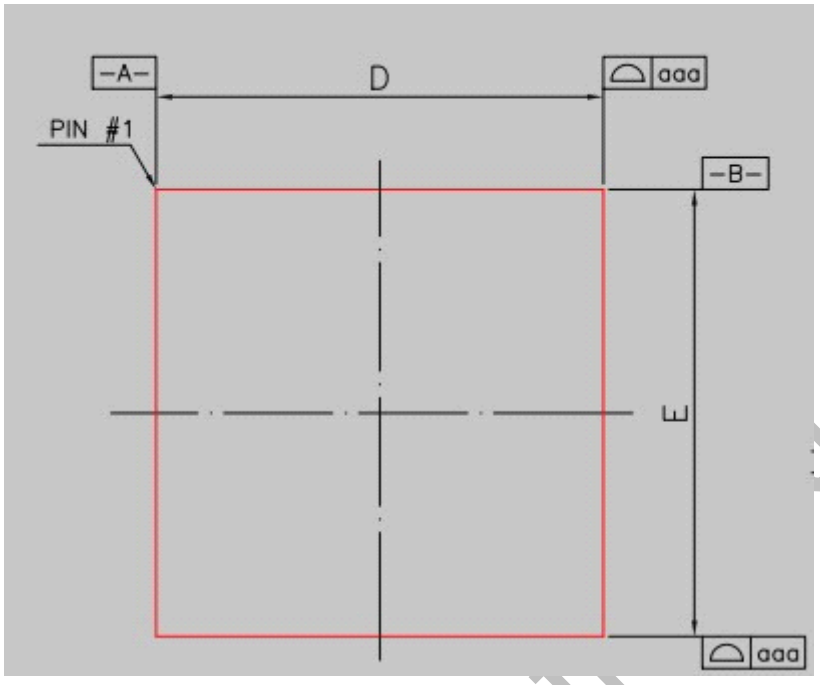

Fig. 12 RK616 TFBGA(HF) Package Top View

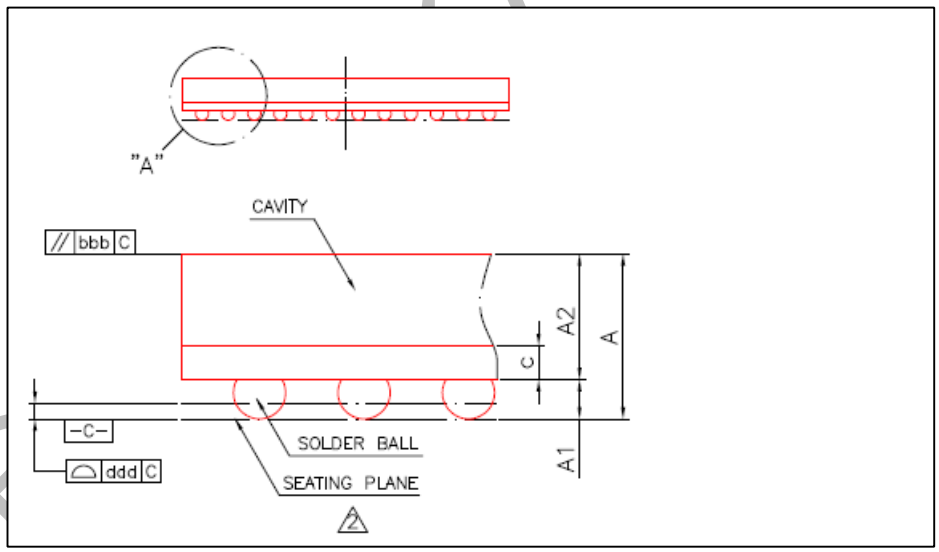

Fig. 13 RK616 TFBGA(HF) Package Side View

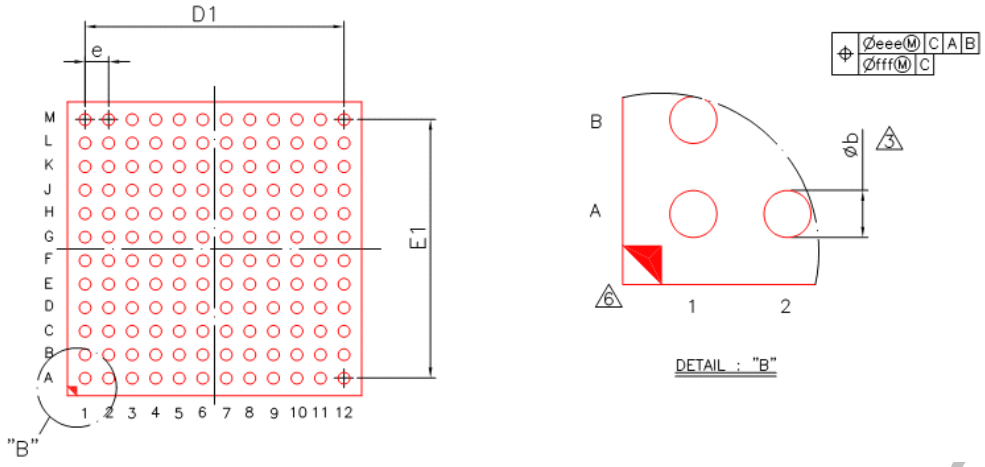

Fig. 14 RK616 TFBGA(HF) Package Bottom View

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.055
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	9.90	10.00	10.10	0.390	0.394	0.398
E	9.90	10.00	10.10	0.390	0.394	0.398
D1	---	8.80	---	---	0.346	---
E1	---	8.80	---	---	0.346	---
e	---	0.80	---	---	0.031	---
b	0.35	0.40	0.45	0.014	0.016	0.018
aaa	0.15			0.006		
bbb	0.20			0.008		
ddd	0.12			0.005		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	12/12			12/12		

Fig. 15 RK616 TFBGA(HF) Package Dimension

1.4.2 RK618 Dimension

RK618 package is TFBGA (HF) 11x11 0.65P 216L_2L Substrate
(body: 11mm x 11mm ; ball size : 0.3mm ; ball pitch : 0.65mm)

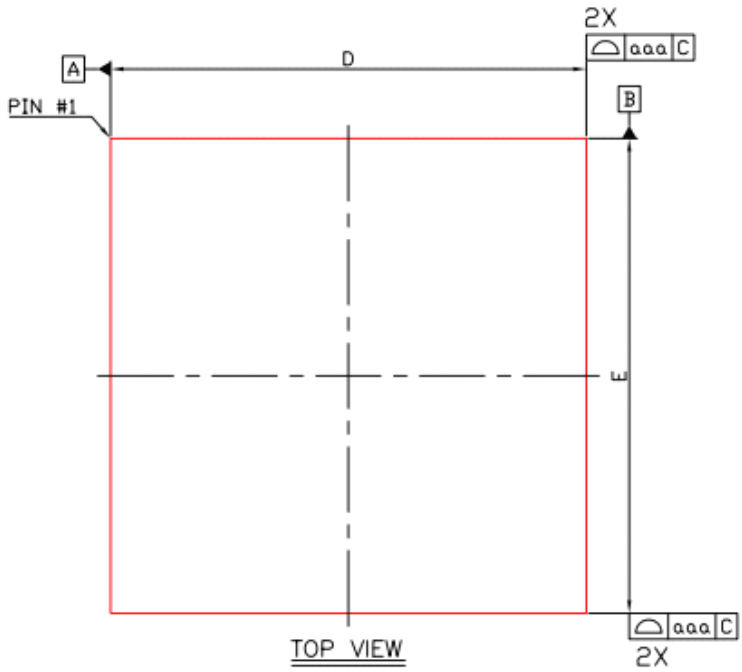

Fig. 16 RK618 TFBGA(HF) Package Top View

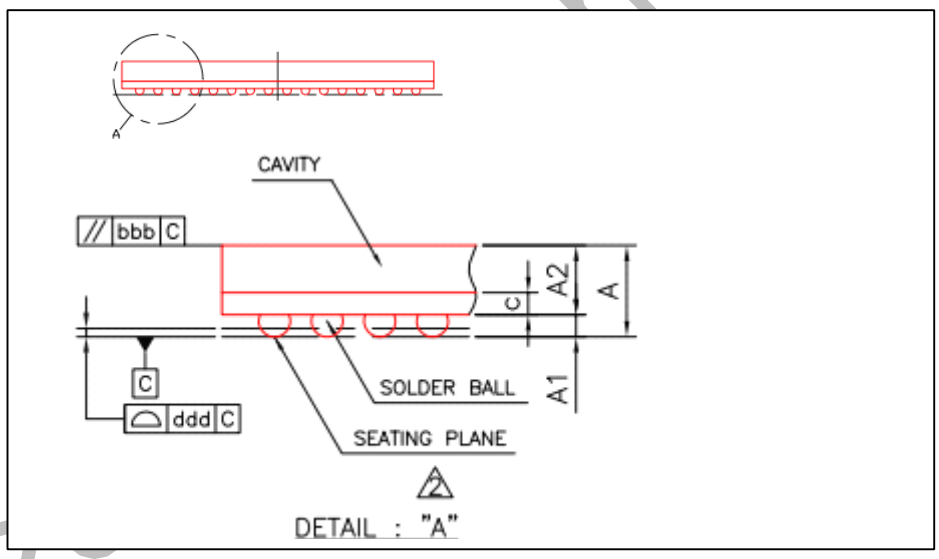

Fig. 17 RK618 TFBGA(HF) Package Side View

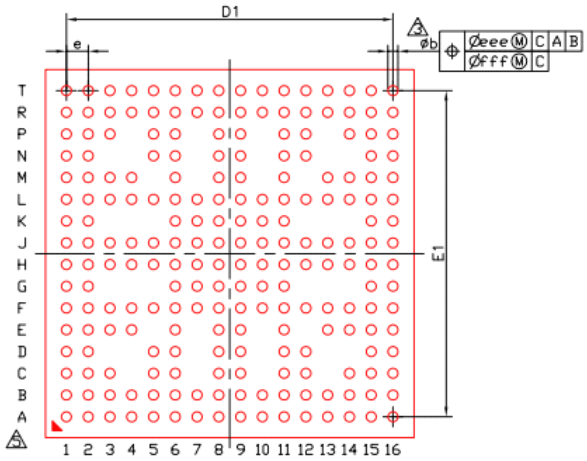

Fig. 18 RK618 TFBGA(HF) Package Bottom View

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.30	---	---	0.051
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	10.90	11.00	11.10	0.429	0.433	0.437
E	10.90	11.00	11.10	0.429	0.433	0.437
D1	----	9.75	----	----	0.384	----
E1	----	9.75	----	----	0.384	----
e	----	0.65	----	----	0.026	----
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa	0.15			0.006		
bbb	0.10			0.004		
ddd	0.08			0.003		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	16 /16			16 /16		

Fig. 19 RK618 TFBGA(HF) Package Dimension

1.4.3 RK616 Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	
A	I2S0_SCLK	HDMI_EXTR	HDMI_TX2N	HDMI_TX1N	HDMI_TX0N	HDMI_TXCN	CODEC_AVCC	AOL	AOR	IN3R	LVDS_VCC	LVDS_VCC	A
B	I2S0_LRCK_RX	I2S0_SDO	HDMI_TX2P	HDMI_TX1P	HDMI_TX0P	HDMI_TXCP	VSS	CODEC_AVCC	CODEC_AVCC	IN3L	LVDS_VCC	VSS	B
C	I2S0_SDI_D0	I2S0_LRCK_TX	VSS	HDMIVCC_3V3	VSS	VSS	HDMIVCC_3V3	CODEC_AVSS	MIC1N	VSS	LCD_D9/LVDS0_D3N	LCD_D8/LVDS0_D3P	C
D	I2C_SCL	I2S0_CLK	I2S0_SDI_D1	HDMI_SDA	VSS	HDMIVDD_1V2	CODEC_AVSS	VCM	MICBIAS1	VDD	LCD_D5/LVDS0_D2N	LCD_D4/LVDS0_D2P	D
E	INT	I2C_SDA	I2S0_SDI_D3	I2S0_SDI_D2	HDMI_SCL	HDMI_HPD	HDMI_CEC	VSS	LVDS_EXTR	LVDS_VCC	LCD_D7/LVDS0_CLKN	LCD_D6/LVDS0_CLKP	E
F	LCD0_D23	NPOR	TEST	SPDIF	VDD	VSS	VSS	VDD	VSS	LVDS_VCC	LCD_D3/LVDS0_D1N	LCD_D2/LVDS0_D1P	F
G	LCD0_D22	LCD0_D21	LCD0_D20	LCD0_D19	VCC	LCD1_D17	VSS	LCD1_D7	LCD1_D1	I2S1_SDI	LCD_D1/LVDS0_D0N	LCD_D0/LVDS0_D0P	G
H	LCD0_D18	LCD0_D17	LCD0_D16	LCD0_D15	LCD1_D22	LCD1_D18	VDD	LCD1_D8	LCD1_D2	PLL1VDD_3V3	I2S1_LRCK_TX	I2S1_SDO	H
J	LCD0_D14	LCD0_D13	LCD0_D12	LCD0_D11	LCD1_D23	VCC	LCD1_D13	LCD1_D9	LCD1_D3	PLL1VDD_1V2	VSS	I2S1_SCLK	J
K	LCD0_D10	LCD0_D9	LCD0_D8	LCD0_D7	LCD0_VSYNC	LCD1_D19	LCD1_D14	LCD1_D10	LCD1_D4	PLL2VDD_1V2	PLLVSS	I2S1_LRCK_RX	K
L	LCD0_D6	LCD0_D5	LCD0_D2	LCD0_DEN	LCD0_HSYNC	LCD1_D20	LCD1_D15	LCD1_D11	LCD1_D5	VSS	LCD1_DCLK	LCD1_VSYNC	L
M	LCD0_D4	LCD0_D3	LCD0_D1	LCD0_D0	LCD0_DCLK	LCD1_D21	LCD1_D16	LCD1_D12	LCD1_D6	LCD1_D0	LCD1_DEN	LCD1_HSYNC	M
	1	2	3	4	5	6	7	8	9	10	11	12	

Fig. 110 RK616 Ball Mapping Diagram

1.4.4 RK618 Ball Map

216	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	LCD1_D20	LCD1_D22	LCD1_D23	LCD0_D4	LCD0_D7	LCD0_D9	LCD0_D10	LCD0_D14	LCD0_D15	LCD0_D17	LCD0_D20	LCD0_DCLKP	LCD0_DEN	NPOR	I2S0_SDI_D3	I2S0_LRCK_TX	A
B	LCD1_D16	LCD1_D17	LCD1_D18	LCD1_D21	LCD0_D2	LCD0_D6	LCD0_D8	LCD0_D12	LCD0_D16	LCD0_D18	LCD0_D22	LCD0_DCLKN	LCD0_VSYNC	I2S0_SDI_D2	I2S0_LRCK_RX	I2S0_SCLK	B
C	LCD1_D15	LCD1_D14	VSS		LCD1_D19	LCD0_D5		VSS	LCD0_D23		VSS	LCD0_HSYNC		VSS	I2S0_CLK	HDMI_HPD	C
D	LCD1_D13	LCD1_D11			LCD0_D0	LCD0_D1		LCD0_D11	LCD0_D19		INT	I2S0_SDI_D0			CPGND	CPVDD	D
E	LCD1_D8	LCD1_D9	LCD1_D10	LCD1_D12		LCD0_D3		LCD0_D13	LCD0_D21		I2S0_SDI_D1		HDMI_CEC	I2S0_SDO	CBN	CBP	E
F	LCD1_D3	LCD1_D4	LCD1_D5	LCD1_D6	LCD1_D7	VSS	VSS	LCD_VCC0	VSS	VDD	VSS	IN1N	IN1P	LINE1	HPL	CPVEE	F
G	LCD1_D2	LCD1_D1				LCD_VCC1	VSS	VSS	VSS	VSS	TEST				HPAGNDFB	HPR	G
H	LCD1_DCLKP	LCD1_DCLKN	I2S1_SDO	LCD1_DEN	LCD1_D0	VDD	VSS	VSS	VSS	VSS	SPDIF	MIC2N	MIC2P	LINE2	CODEC_AVSS	CODEC_AVCC1	H
J	LCD1_HSYNC	VSS	I2S1_LRCK_TX	I2S1_LRCK_RX	I2S1_SCLK	VSS	VSS	VSS	VSS	VSS	MIC1N	MIC1P	CODEC_AVSS	AOL	AOR	VCM	J
K	LCD1_VSYNC	PLLVSS				VSS	VSS	VSS	VSS	VSS	VSS				HDMIVDD_1V2	CODEC_AVCC2	K
L	PLLVDD_3V3	MIPI_AVSS	MIPIAVDD_1V2	PLLVDD_1V2	I2S1_SDI	VSS	LCD_VCC2	VDD	VSS	VSS	VSS	MICBIAS2	IN3L	HDMI_AVSS	HDMI_TX2N	HDMI_TX2P	L
M	MIPI_D0N	MIPI_D0P	MIPI_AVSS	MIPIPLL_2V5		LCD_HSYNC		LCD_D20	I2C_SDA		MICBIAS1		IN3R	HDMI_AVSS	HDMI_TX1N	HDMI_TX1P	M
N	MIPI_D1N	MIPI_D1P			LCD_VSYNC	LCD_D22		LCD_D21	I2C_SCL		HDMI_SCL	HDMI_SDA			HDMI_TX0N	HDMI_TX0P	N
P	MIPI_CLKN	MIPI_CLKP	MIPI_AVSS		LCD_D23	LVDS_VCC		LVDS_VCC	VSS		LVDS_VCC	VSS		HDMI_AVSS	HDMI_TXCN	HDMI_TXCP	P
R	MIPI_D2N	MIPI_D2P	VSS	LCD_DEN	LCD_D18/LVDS1_D3P	LCD_D16/LVDS1_CLKP	LCD_D14/LVDS1_D2P	LCD_D12/LVDS1_D1P	LCD_D10/LVDS1_D0N	LCD_D8/LVDS0_D3P	LCD_D8/LVDS0_CLKP	LCD_D4/LVDS0_D2P	LCD_D2/LVDS0_D1P	LCD_D0/LVDS0_D0P	HDMI_AVSS	CODEC_AVCC1	R
T	MIPI_D3N	MIPI_D3P	MIPI_AVSS	LCD_DCLK	LCD_D19/LVDS1_D3N	LCD_D17/LVDS1_CLKN	LCD_D15/LVDS1_D2N	LCD_D13/LVDS1_D1N	LCD_D11/LVDS1_D0N	LCD_D9/LVDS0_D3N	LCD_D7/LVDS0_CLKN	LCD_D5/LVDS0_D2N	LCD_D3/LVDS0_D1N	LCD_D1/LVDS0_D0N	LVDS_EXTR	HDMI_EXTR	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Fig. 111 RK618 Ball Mapping Diagram

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