bq28z610 Impedance Track™ Gas Gauge for 1-Series to 2-Series Li-Ion/Li-Polymer Battery Packs

1 Features

- MASTER Mode I²C™ Broadcasts for Autonomous Battery Charging Control
- High-Accuracy Coulomb Counter with Input Offset Error < 1 µV (Typical)
- High-Side FET Drive Allows Serial Bus Communication During Fault Conditions
- Analog Front End with Two Independent ADCs
  - Support for Simultaneous Current and Voltage Sampling
- Bus Communications Interface
  - I²C
- SHA-1 Hash Message Authentication Code (HMAC) Responder for Increased Battery Pack Security
  - Split Key (2 × 64) Stored in Secure Memory
- Programmable Protection Levels for:
  - Overcurrent in Discharge
  - Short-Circuit Current in Charge
  - Short-Circuit Current in Discharge
  - Overvoltage
  - Undervoltage
  - Overtemperature
- Supports a 1-mΩ to 3-mΩ Current Sense Resistor
- Compact 12-Terminal SON Package (DRZ)

2 Applications

- Portable and Wearable Health Devices

3 Description

The Texas Instruments bq28z610 Impedance Track™ gas gauge enables autonomous charge control through Master Mode I²C broadcasts of charging current and voltage information, eliminating software overhead that is typically incurred by the system's host controller.

The bq28z610 device provides a fully integrated pack-based solution with a flash programmable custom reduced instruction-set CPU (RISC), safety protection, and authentication for 1-series to 2-series cell Li-Ion and Li-Polymer battery packs.

The bq28z610 gas gauge communicates via an I²C compatible interface and combines an ultra-low-power, high-speed TI bqBMP processor, high-accuracy analog measurement capabilities, integrated flash memory, an array of peripheral and communication ports, an N-channel FET drive, and a SHA-1 Authentication transform responder into a complete, high-performance battery management solution.

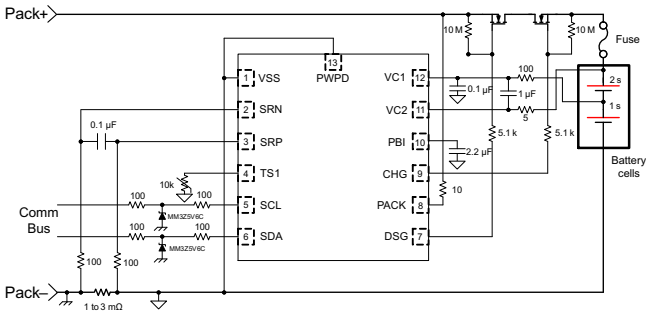
The bq28z610 device provides an array of battery and system safety functions, including overcurrent in discharge, short circuit in charge, and short circuit in discharge protection for the battery, as well as FET protection for the N-channel FETs, internal AFE watchdog, and cell balancing. Through firmware, the devices can provide a larger array of features including protection against overvoltage, undervoltage, overtemperature, and more.

Device Information(1)

DEVICE NAME	PACKAGE	BODY SIZE
bq28z610	VSON (12)	4 mm × 2.5 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



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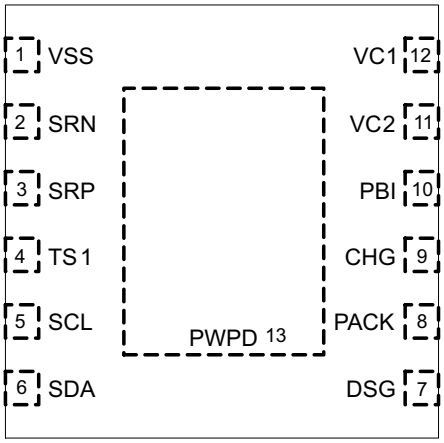
5 Revision History

DATE	REVISION	NOTES
April 2014	*	Initial Release

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	DRZ		
VSS	1	P	Device ground
SRN	2	IA	Analog input pin connected to the internal coulomb-counter peripheral for integrating a small voltage between SRP and SRN where SRP is the top of the sense resistor.
SRP	3	IA	Analog input pin connected to the internal coulomb-counter peripheral for integrating a small voltage between SRP and SRN where SRP is the top of the sense resistor.
TS1	4	IA	Input for ADC to the oversampled ADC channel
SCL	5	I/O	Serial Clock
SDA	6	I/O	Serial Data
DSG	7	O	N-Channel FET drive output pin
PACK	8	IA, P	Pack sense input pin
CHG	9	O	N-Channel FET drive output pin
PBI	10	P	Power supply backup input pin
VC2	11	IA, P	Sense voltage input pin for most positive cell, balance current input for most positive cell. Primary power supply input and battery stack measurement input (BAT)
VC1	12	IA	Sense voltage input pin for least positive cell, balance current input for least positive cell
PWPD		—	Exposed Pad, electrically connected to VSS (external trace)

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

DESCRIPTION	PINS	VALUE
Supply voltage range, V_{CC}	VC2, PBI	–0.3 to 30 V
Input voltage range, V_{IN}	PACK	–0.3 to 30 V
	TS1	–0.3 to V_{REG} + 0.3 V
	SRP, SRN	–0.3 to 0.3 V
	VC2	VC1 – 0.3 to VC1 + 8.5 V, or VSS + 30 V
	VC1	VSS – 0.3 to VSS + 8.5 V, or VSS + 30 V
Output voltage range, V_O	CHG, DSG	–0.3 to 32 V
Maximum VSS current, I_{SS}		50 mA
Functional Temperature, T_{FUNC}		–40 to 110°C
Lead temperature (soldering, 10 s), T_{SOLDER}		300°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

		MIN	MAX	UNIT
T_{STG}	Storage temperature range	–65	150	°C
ESD(1) Rating	HBM(2)	–2	2	kV
	CDM(3)	–500	500	V
	MM	–200	200	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
(2) Level listed above is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Typical values stated where T_A = 25ºC and VCC = 7.2 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 2.2 V to 26 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	VC2, PBI	2.2		26	V
$V_{SHUTDOWN–}$	Shutdown voltage	$V_{PACK} < V_{SHUTDOWN–}$	1.8	2.0	2.2	V
$V_{SHUTDOWN+}$	Start-up voltage	$V_{PACK} > V_{SHUTDOWN–} + V_{HYS}$	2.05	2.25	2.45	V
V_{HYS}	Shutdown voltage hysteresis	$V_{SHUTDOWN+} – V_{SHUTDOWN–}$		250		mV
V_{IN}	Input voltage range	SDA, SCL, SMBD, SMBC			5.5	V
		TS1			V_{REG}	
		SRP, SRN	–0.2		0.2	
		VC2	V_{VC1}		V_{VC1} + 5	
		VC1	V_{VSS}		V_{VSS} + 5	
		PACK			26	
V_O	Output voltage range	CHG, DSG			26	V
C_{PBI}	External PBI capacitor		2.2			µF
T_{OPR}	Operating temperature		–40		85	°C

7.4 Thermal Information

THERMAL METRIC(1)		DRZ (12 Pins)	UNIT
$R_{\theta JA, High K}$	Junction-to-ambient thermal resistance(2)	186.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance(3)	90.4	
$R_{\theta JB}$	Junction-to-board thermal resistance(4)	110.7	
ψ_{JT}	Junction-to-top characterization parameter(5)	96.7	
ψ_{JB}	Junction-to-board characterization parameter(6)	90	
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance(7)	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

7.5 Supply Current

Typical values stated where T_A = 25ºC and VCC = 7.2 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 2.2 V to 7.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{NORMAL}	NORMAL Mode	CHG = ON, DSG = ON, No Flash Write and CPU = ON		400	500	µA
		CHG = ON, DSG = ON, No Flash Write and CPU = Halted		250	300	
I_{SLEEP}	SLEEP Mode	CHG = OFF, DSG = ON, No Communication on Bus		90	160	µA
		CHG = OFF, DSG = OFF, No Communication on Bus		38	120	
$I_{SHUTDOWN}$	SHUTDOWN Mode			0.5	2	µA

7.6 Power Supply Control

Typical values stated where T_A = 25ºC and VCC = 7.2 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 2.2 V to 7.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{SWITCHOVER-}$	VC2 to PACK switchover voltage	$V_{VC2} < V_{SWITCHOVER-}$	2.0	2.1	2.2	V
$V_{SWITCHOVER+}$	PACK to VC2 switchover voltage	$V_{VC2} > V_{SWITCHOVER-} + V_{HYS}$	3.0	3.1	3.2	V
V_{HYS}	Switchover voltage hysteresis	$V_{SWITCHOVER+} - V_{SWITCHOVER-}$		1000		mV
I_{LKG}	Input Leakage current	VC2 pin, VC2 = 0 V, PACK = 25 V			1	µA
		PACK pin, VC2 = 25 V, PACK = 0 V			1	
		VC2 and PACK pins, VC2 = 0 V, PACK = 0 V, PBI = 25 V			1	
$R_{PACK(PD)}$	Internal pulldown resistance	PACK	30	40	50	kΩ

7.7 Low-Voltage General Purpose I/O, TS1

Typical values stated where T_A = 25ºC and VCC = 7.2 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 2.2 V to 7.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IH}	High-level input		0.65 x V_{REG}			V
V_{IL}	Low-level input				0.35 x V_{REG}	V
V_{OH}	Output voltage high	I_{OH} = – 1.0 mA	0.75 x V_{REG}			V
V_{OL}	Output voltage low	I_{OL} = 1.0 mA			0.2 x V_{REG}	V
C_{IN}	Input capacitance			5		pF
I_{LKG}	Input leakage current				1	µA

7.8 Power-On Reset (POR)

Typical values stated where T_A = 25ºC and VCC = 7.2 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 2.2 V to 7.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{REGIT–}$	Negative-going voltage input	V_{REG}	1.51	1.55	1.59	V
V_{HYS}	Power-on reset hysteresis	$V_{REGIT+} – V_{REGIT–}$	70	100	130	mV
t_{RST}	Power-on reset time		200	300	400	µs

7.9 Internal 1.8-V LDO

Typical values stated where T_A = 25ºC and VCC = 7.2 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 2.2 V to 7.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{REG}	Regulator voltage		1.6	1.8	2.0	V
$\Delta V_{O(TEMP)}$	Regulator output over temperature	$\Delta V_{REG}/\Delta T_A$, I_{REG} = 10 mA		±0.25%		
$\Delta V_{O(LINE)}$	Line regulation	$\Delta V_{REG}/\Delta V_{BAT}$, V_{BAT} = 10 mA	–0 .6%		0.5%	
$\Delta V_{O(LOAD)}$	Load regulation	$\Delta V_{REG}/\Delta I_{REG}$, I_{REG} = 0 mA to 10 mA	–1.5%		1.5%	
I_{REG}	Regulator output current limit	V_{REG} = 0.9 x $V_{REG(NOM)}$, V_{IN} > 2.2 V	20			mA
I_{SC}	Regulator short-circuit current limit	V_{REG} = 0 x $V_{REG(NOM)}$	25	40	50	mA
$PSRR_{REG}$	Power supply rejection ratio	$\Delta V_{BAT}/\Delta V_{REG}$, I_{REG} = 10 mA, V_{IN} > 2.5 V, f = 10 Hz		40		dB
V_{SLEW}	Slew rate enhancement voltage threshold	V_{REG}	1.58	1.65		V

7.10 Current Wake Comparator

Typical values stated where T_A = 25ºC and VCC = 7.2 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 2.2 V to 7.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{WAKE}	Wake voltage threshold	$V_{WAKE} = V_{SRP} – V_{SRN}$ WAKE_CONTROL[WK1, WK0] = 0,0	±0.3	±0.625	±0.9	mV
		$V_{WAKE} = V_{SRP} – V_{SRN}$ WAKE_CONTROL[WK1, WK0] = 0,1	±0.6	±1.25	±1.8	mV
		$V_{WAKE} = V_{SRP} – V_{SRN}$ WAKE_CONTROL[WK1, WK0] = 1,0	±1.2	±2.5	±3.6	mV
		$V_{WAKE} = V_{SRP} – V_{SRN}$ WAKE_CONTROL[WK1, WK0] = 1,1	±2.4	±5.0	±7.2	mV
$V_{WAKE(DRIFT)}$	Temperature drift of V_{WAKE} accuracy			0.5%		°C
t_{WAKE}	Time from application of current to wake			0.25	0.5	ms
$t_{WAKE(SU)}$	Wake up comparator startup time	[WKCHGEN] = 0 and [WKDSGEN] = 0 to [WKCHGEN] = 1 and [WKDSGEN] = 1		250	640	µs

7.11 Coulomb Counter

Typical values stated where T_A = 25ºC and VCC = 7.2 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 2.2 V to 7.6 V (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Input voltage range		–100		100	mV
Full scale range		$–V_{REF1}/10$		$+V_{REF1}/10$	mV
Differential nonlinearity	16-bit, No missing codes			±1	LSB
Integral nonlinearity	16-bit, Best fit over input voltage range		±5.2	±22.3	LSB
Offset error	16-bit, Post-calibration		±1.3	±2.6	LSB
Offset error drift	15-bit + sign, Post-calibration		0.04	0.07	LSB/°C
Gain error	15-bit + sign, Over input voltage range		±131	±492	LSB
Gain error drift	15-bit + sign, Over input voltage range		4.3	9.8	LSB/°C
Effective input resistance		2.5			MΩ

7.12 ADC Digital Filter

Typical values stated where T_A = 25ºC and VCC = 7.2 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 2.2 V to 7.6 V (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
t_{CONV}	ADCTL[SPEED1, SPEED0] = 0, 0		31.25		ms
	ADCTL[SPEED1, SPEED0] = 0, 1		15.63		
	ADCTL[SPEED1, SPEED0] = 1, 0		7.81		
	ADCTL[SPEED1, SPEED0] = 1, 1		1.95		
Resolution	No missing codes, ADCTL[SPEED1, SPEED0] = 0, 0		16		Bits
Effective resolution	With sign, ADCTL[SPEED1, SPEED0] = 0, 0	14	15		Bits
	With sign, ADCTL[SPEED1, SPEED0] = 0, 1	13	14		
	With sign, ADCTL[SPEED1, SPEED0] = 1, 0	11	12		
	With sign, ADCTL[SPEED1, SPEED0] = 1, 1	9	10		

7.13 ADC Multiplexer

Typical values stated where T_A = 25ºC and VCC = 7.2 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 2.2 V to 7.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
K	Scaling factor	VC1–VSS, VC2–VC1	0.1980	0.2000	0.2020	—
		VC2–VSS, PACK–VSS	0.0485	0.050	0.051	
		V_{REF1}/2	0.490	0.500	0.510	
V_{IN}	Input voltage range	VC2–VSS, PACK–VSS	–0.2		20	V
		TS1	–0.2		0.8 × V_{REF1}	
		TS1	–0.2		0.8 × V_{REG}	
I_{LKG}	Input leakage current	VC1, VC2 cell balancing off, cell detach detection off, ADC multiplexer off			1	µA

7.14 Cell Balancing Support

Typical values stated where T_A = 25ºC and VCC = 7.2 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 2.2 V to 7.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
R_{CB}	Internal cell balance resistance	$R_{DS(ON)}$ for internal FET switch at 2 V < V_{DS} < 4 V			200	Ω

7.15 Internal Temperature Sensor

Typical values stated where T_A = 25ºC and VCC = 7.2 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 2.2 V to 7.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{TEMP}	Internal temperature sensor voltage drift	V_{TEMPP}	–1.9	–2.0	–2.1	mV/°C
		V_{TEMPP} – V_{TEMPN} (1)	0.177	0.178	0.179	

(1) Assured by design

7.16 NTC Thermistor Measurement Support

Typical values stated where T_A = 25ºC and VCC = 7.2 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 2.2 V to 7.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$R_{NTC(PU)}$	Internal pull-up resistance	TS1	14.4	18	21.6	kΩ
$R_{NTC(DRIFT)}$	Resistance drift over temperature	TS1	–360	–280	–200	PPM/°C

7.17 High-Frequency Oscillator

Typical values stated where T_A = 25ºC and VCC = 7.2 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 2.2 V to 7.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
f_{HFO}	Operating frequency			16.78		MHz
$f_{HFO(ERR)}$	Frequency error	T_A = –20°C to 70°C, includes frequency drift	–2.5%	±0.25%	2.5%	
		T_A = –40°C to 85°C, includes frequency drift	–3.5%	±0.25%	3.5%	
$t_{HFO(SU)}$	Start-up time	T_A = –20°C to 85°C, Oscillator frequency within +/–3% of nominal, CLKCTL[HFRAMP] = 1			4	ms
		Oscillator frequency within +/–3% of nominal, CLKCTL[HFRAMP] = 0			100	µs

7.18 Low-Frequency Oscillator

Typical values stated where T_A = 25ºC and VCC = 7.2 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 2.2 V to 7.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
f_{LFO}	Operating frequency			262.144		kHz
$f_{LFO(LP)}$	Operating frequency in low power mode			247		kHz
$f_{LFO(ERR)}$	Frequency error	T_A = –20°C to 70°C, includes frequency drift	–1.5%	±0.25%	1.5%	
		T_A = –40°C to 85°C, includes frequency drift	–2.5%	±0.25%	2.5%	
$f_{LFO(LPERR)}$	Frequency error in low power mode		–5%		5%	
$f_{LFO(FAIL)}$	Failure detection frequency		30	80	100	kHz

7.19 Voltage Reference 1

Typical values stated where T_A = 25ºC and VCC = 7.2 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 2.2 V to 7.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{REF1}	Internal reference voltage	T_A = 25°C, after trim	1.215	1.220	1.225	V
$V_{REF1(DRIFT)}$	Internal reference voltage drift	T_A = 0°C to 60°C, after trim		±50		PPM/°C
		T_A = –40°C to 85°C, after trim		±80		

7.20 Voltage Reference 2

Typical values stated where T_A = 25ºC and VCC = 7.2 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 2.2 V to 7.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{REF2}	Internal reference voltage	T_A = 25°C, after trim	1.215	1.220	1.225	V
$V_{REF2(DRIFT)}$	Internal reference voltage drift	T_A = 0°C to 60°C, after trim		±50		PPM/°C
		T_A = –40°C to 85°C, after trim		±80		

7.21 Instruction Flash

Typical values stated where T_A = 25ºC and VCC = 7.2 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 2.2 V to 7.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
	Data retention		10			Years
	Flash programming write cycles		1000			Cycles
$t_{PROGWORD}$	Word programming time	T_A = –40°C to 85°C			40	µs
$t_{MASSERASE}$	Mass-erase time	T_A = –40°C to 85°C			40	ms
$t_{PAGEERASE}$	Page-erase time	T_A = –40°C to 85°C			40	ms
$I_{FLASHREAD}$	Flash-read current	T_A = –40°C to 85°C			2	mA
$I_{FLASHWRITE}$	Flash-write current	T_A = –40°C to 85°C			5	mA
$I_{FLASHERASE}$	Flash-erase current	T_A = –40°C to 85°C			15	mA

7.22 Data Flash

Typical values stated where T_A = 25ºC and VCC = 7.2 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 2.2 V to 7.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
	Data retention		10			Years
	Flash programming write cycles		20000			Cycles
$t_{PROGWORD}$	Word programming time	T_A = –40°C to 85°C			40	µs
$t_{MASSERASE}$	Mass-erase time	T_A = –40°C to 85°C			40	ms
$t_{PAGEERASE}$	Page-erase time	T_A = –40°C to 85°C			40	ms
$I_{FLASHREAD}$	Flash-read current	T_A = –40°C to 85°C			1	mA
$I_{FLASHWRITE}$	Flash-write current	T_A = –40°C to 85°C			5	mA
$I_{FLASHERASE}$	Flash-erase current	T_A = –40°C to 85°C			15	mA

7.23 Current Protection Thresholds

Typical values stated where T_A = 25ºC and VCC = 7.2 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 2.2 V to 7.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{OCD}	OCD detection threshold voltage range	$V_{OCD} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1	–16.6		–100	mV
		$V_{OCD} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0	–8.3		–50	
ΔV_{OCD}	OCD detection threshold voltage program step	$V_{OCD} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1		–5.56		mV
		$V_{OCD} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0		–2.78		
ΔV_{SCC}	SCC detection threshold voltage range	$V_{SCC} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1	44.4		200	mV
		$V_{SCC} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0	22.2		100	
ΔV_{SCC}	SCC detection threshold voltage program step	$V_{SCC} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1		22.2		mV
		$V_{SCC} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0		11.1		
V_{SCD1}	SCD1 detection threshold voltage range	$V_{SCD1} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1	–44.4		–200	mV
		$V_{SCD1} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0	–22.2		–100	
ΔV_{SCD1}	SCD1 detection threshold voltage program step	$V_{SCD1} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1		–22.2		mV
		$V_{SCD1} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0		–11.1		
V_{SCD2}	SCD2 detection threshold voltage range	$V_{SCD2} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1	–44.4		–200	mV
		$V_{SCD2} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0	–22.2		–100	
ΔV_{SCD2}	SCD2 detection threshold voltage program step	$V_{SCD2} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1		–22.2		mV
		$V_{SCD2} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0		–11.1		

7.24 Current Protection Timing

Typical values stated where T_A = 25ºC and VCC = 7.2 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 2.2 V to 7.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{OCD}	OCD detection delay time		1		31	ms
Δt_{OCD}	OCD detection delay time program step			2		ms
t_{SCC}	SCC detection delay time		0		915	µs
Δt_{SCC}	SCC detection delay time program step			61		µs
t_{SCD1}	SCD1 detection delay time	PROTECTION_CONTROL[SCDDx2] = 0	0		915	µs
		PROTECTION_CONTROL[SCDDx2] = 1	0		1850	
Δt_{SCD1}	SCD1 detection delay time program step	PROTECTION_CONTROL[SCDDx2] = 0		61		µs
		PROTECTION_CONTROL[SCDDx2] = 1		121		
t_{SCD2}	SCD2 detection delay time	PROTECTION_CONTROL[SCDDx2] = 0	0		458	µs
		PROTECTION_CONTROL[SCDDx2] = 1	0		915	
Δt_{SCD2}	SCD2 detection delay time program step	PROTECTION_CONTROL[SCDDx2] = 0		30.5		µs
		PROTECTION_CONTROL[SCDDx2] = 1		61		
t_{DETECT}	Current fault detect time	$V_{SRP} – V_{SRN} = V_T – 3$ mV for OCD, SCD1, and SC2, $V_{SRP} – V_{SRN} = V_T + 3$ mV for SCC			160	µs
t_{ACC}	Current fault delay time accuracy	Max delay setting	–10%		10%	

7.25 N-CH FET Drive (CHG, DSG)

Typical values stated where T_A = 25ºC and VCC = 7.2 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 2.2 V to 7.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
	Output voltage ratio	$Ratio_{DSG} = (V_{DSG} – V_{VC2})/V_{VC2}$, 2.2 V < V_{VC2} < 4.07 V, 10 MΩ between PACK and DSG	2.133	2.333	2.467	—
		$Ratio_{CHG} = (V_{CHG} – V_{VC2})/V_{VC2}$, 2.2 V < V_{VC2} < 4.07 V, 10 MΩ between BAT and CHG	2.133	2.333	2.467	
$V_{(FETON)}$	Output voltage, CHG and DSG on	$V_{DSG(ON)} = V_{DSG} – V_{VC2}$, V_{VC2} ≥ 4.07 V, 10 MΩ between PACK and DSG, V_{VC2} = 18 V	8.75	9.5	10.25	V
		$V_{CHG(ON)} = V_{CHG} – V_{VC2}$, V_{VC2} ≥ 4.07 V, 10 MΩ between VC2 and CHG, V_{VC2} = 18 V	8.75	9.5	10.25	
$V_{(FETOFF)}$	Output voltage, CHG and DSG off	$V_{DSG(OFF)} = V_{DSG} – V_{PACK}$, 10 MΩ between PACK and DSG	–0.4		0.4	V
		$V_{CHG(OFF)} = V_{CHG} – V_{BAT}$, 10 MΩ between VC2 and CHG	–0.4		0.4	
t_R	Rise time	V_{DSG} from 0% to 35% $V_{DSG(ON)(TYP)}$, V_{BAT} ≥ 2.2 V, C_L = 4.7 nF between DSG and PACK, 5.1 kΩ between DSG and C_L, 10 MΩ between PACK and DSG		200	500	µs
		V_{CHG} from 0% to 35% $V_{CHG(ON)(TYP)}$, V_{VC2} ≥ 2.2 V, C_L = 4.7 nF between CHG and VC2, 5.1 kΩ between CHG and C_L, 10 MΩ between VC2 and CHG		200	500	
t_F	Fall time	V_{DSG} from $V_{DSG(ON)(TYP)}$ to 1 V, V_{VC2} ≥ 2.2 V, C_L = 4.7 nF between DSG and PACK, 5.1 kΩ between DSG and C_L, 10 MΩ between PACK and DSG		40	300	µs
		V_{CHG} from $V_{CHG(ON)(TYP)}$ to 1 V, V_{VC2} ≥ 2.2 V, C_L = 4.7 nF between CHG and VC2, 5.1 kΩ between CHG and C_L, 10 MΩ between VC2 and CHG		40	200	

7.26 I²C Interface I/O

Typical values stated where T_A = 25ºC and VCC = 7.2 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 2.2 V to 7.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IH}	Input voltage high	SCL, SDA, V_{REG} = 1.8 V (STANDARD and FAST modes)	0.7 × V_{REG}			V
V_{IL}	Input voltage low	SCL, SDA, V_{REG} = 1.8 V (STANDARD and FAST modes)	–0.5		0.3 × V_{REG}	V
V_{OL}	Output low voltage	SCL, SDA, V_{REG} = 1.8 V, I_{OL} = 3 mA (FAST mode)			0.2 × V_{REG}	V
		SCL, SDA, V_{REG} > 2.0 V, I_{OL} = 3 mA (STANDARD and FAST modes)			0.4	V
C_{IN}	Input capacitance				10	pF
I_{LKG}	Input leakage current			1		µA
R_{PD}	Pull-down resistance			3.3		kΩ

7.27 I²C Timing

Typical values stated where T_A = 25ºC and VCC = 7.2 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 2.2 V to 7.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_R	Clock rise time	10% to 90%			300	ns
t_F	Clock fall time	90% to 10%			300	ns
t_{HIGH}	Clock high period		600			ns
t_{LOW}	Clock low period		1.3			µs
$t_{SU(START)}$	Repeated start setup time		600			ns
$t_{d(START)}$	Start for first falling edge to SCL		600			ns
$t_{SU(DATA)}$	Data setup time		100			ns
$t_{HD(DATA)}$	Data hold time		0			µs
$t_{SU(STOP)}$	Stop setup time		600			ns
t_{BUF}	Bus free time between stop and start		1.3			µs
f_{SW}	Clock operating frequency	SLAVE mode, SCL 50% duty cycle			400	kHz

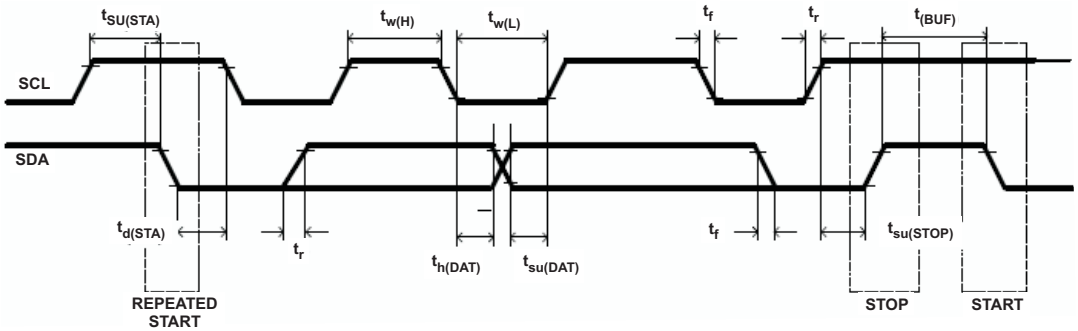


Figure 1. I²C Timing

7.28 Typical Characteristics

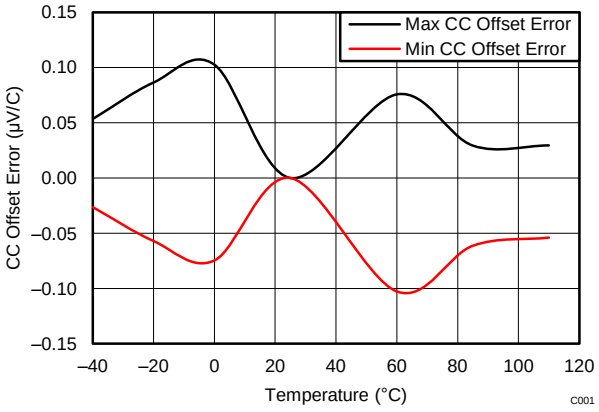


Figure 2. CC Offset Error Vs. Temperature

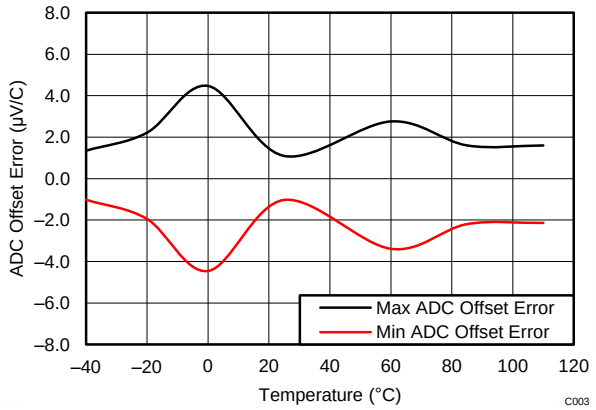


Figure 3. ADC Offset Error Vs. Temperature

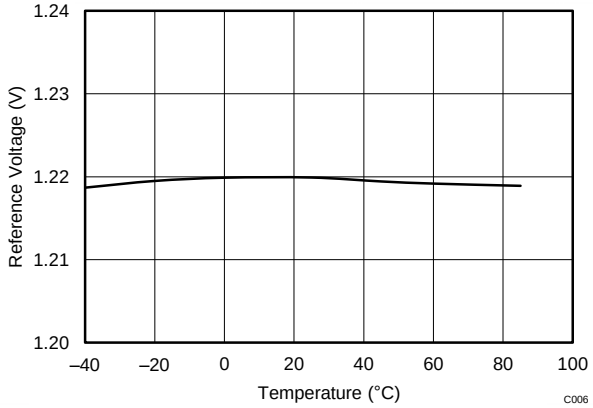


Figure 4. Reference Voltage Vs. Temperature

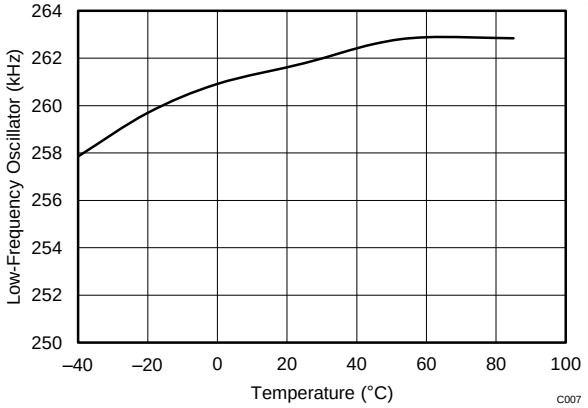


Figure 5. Low-Frequency Oscillator Vs. Temperature

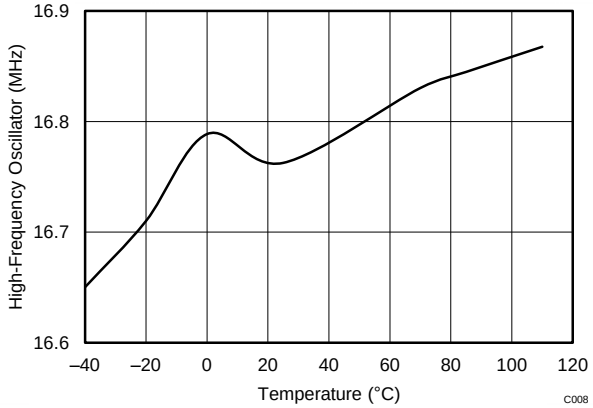
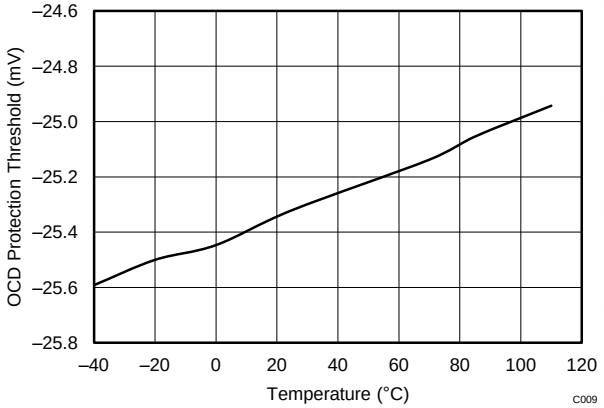


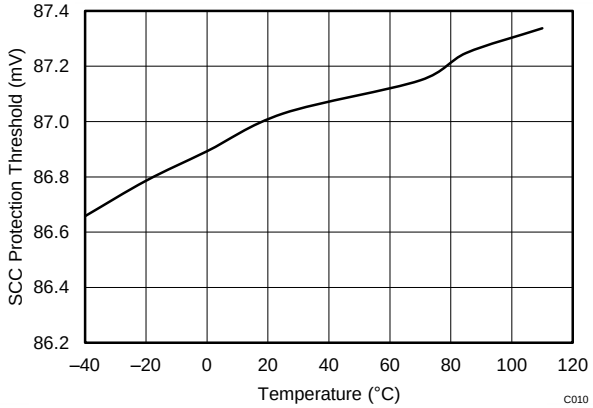
Figure 6. High-Frequency Oscillator Vs. Temperature



Threshold setting is 25 mV.

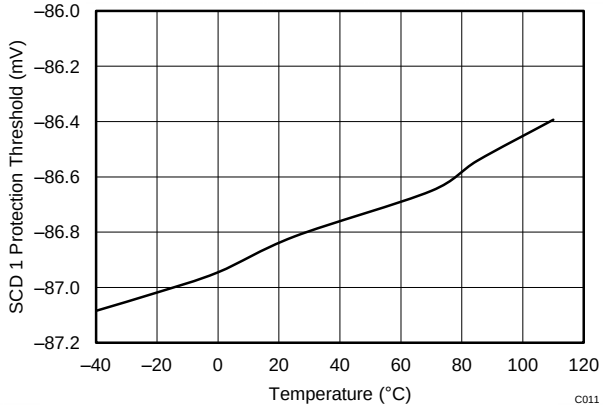
Figure 7. Overcurrent Discharge Protection Threshold Vs. Temperature

Typical Characteristics (continued)



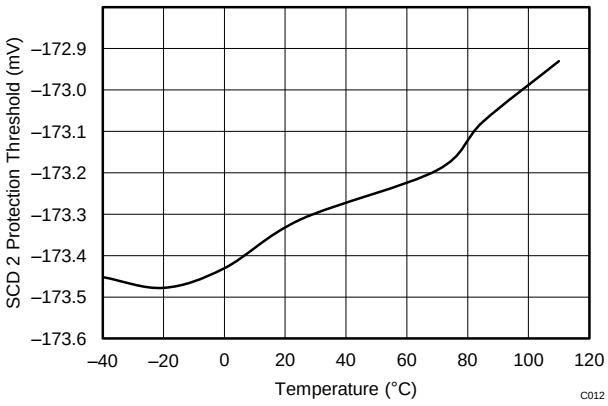
Threshold setting is 25 mV.

Figure 8. Short Circuit Charge Protection Threshold Vs. Temperature



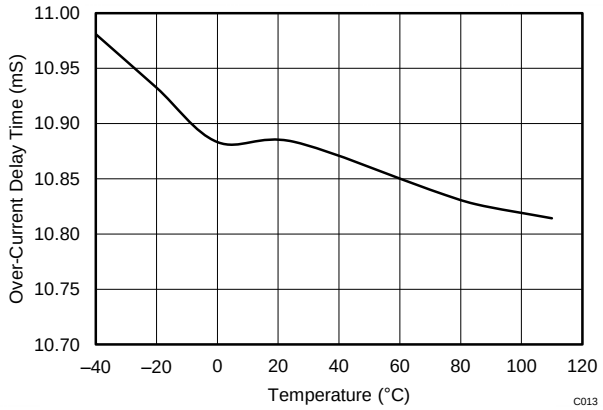
Threshold setting is –88.85 mV.

Figure 9. Short Circuit Discharge 1 Protection Threshold Vs. Temperature



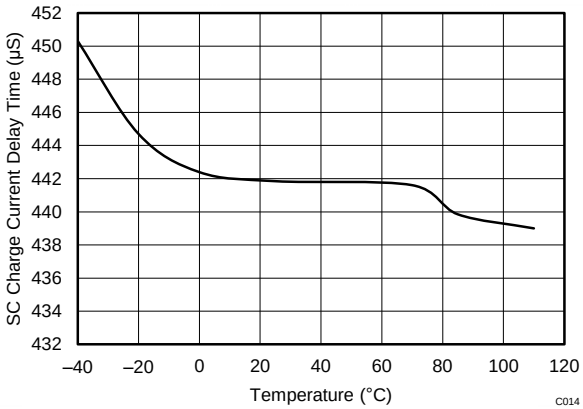
Threshold setting is –177.7 mV.

Figure 10. Short Circuit Discharge 2 Protection Threshold Vs. Temperature



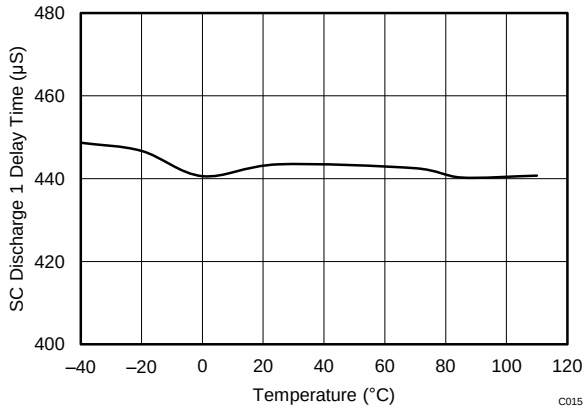
Threshold setting is 11 ms.

Figure 11. Overcurrent Delay Time Vs. Temperature



Threshold setting is 465 µs.

Figure 12. Short Circuit Charge Current Delay Time Vs. Temperature



Threshold setting is 465 µs (including internal delay).

Figure 13. Short Circuit Discharge 1 Delay Time Vs. Temperature

Typical Characteristics (continued)

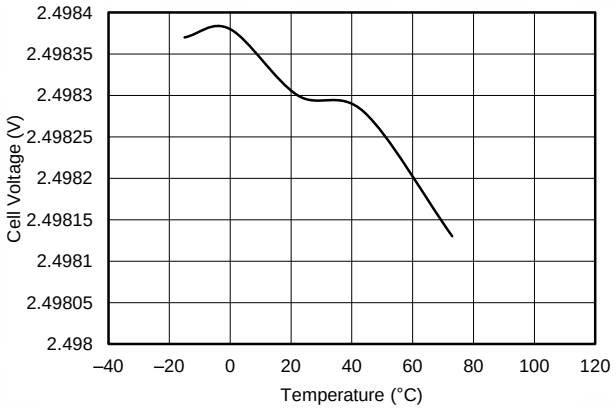
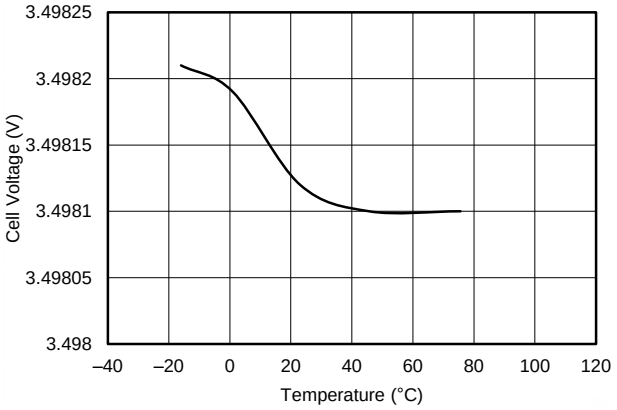
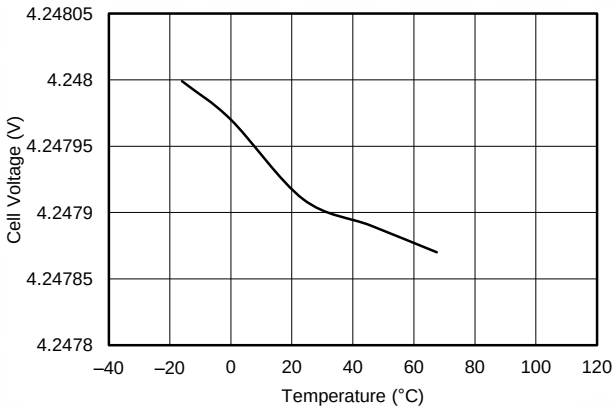


Figure 14. V_{CELL} Measurement at 2.5-V Vs. Temperature



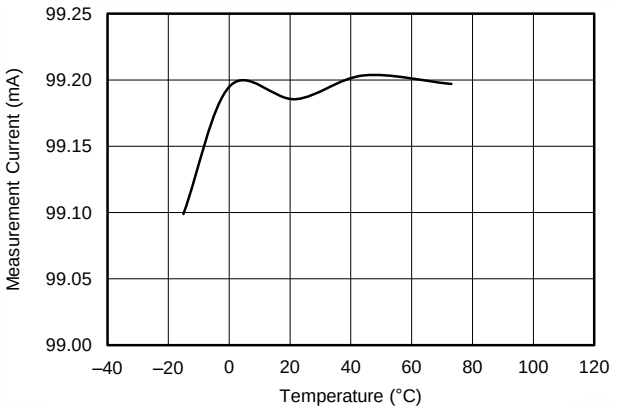
This is the V_{CELL} average for single cell.

Figure 15. V_{CELL} Measurement at 3.5-V Vs. Temperature



This is the V_{CELL} average for single cell.

Figure 16. V_{CELL} Measurement at 4.25-V Vs. Temperature



I_{SET} = 100 mA

Figure 17. I measured Vs. Temperature

8 Detailed Description

8.1 Overview

The bq28z610 gas gauge is a fully integrated battery manager that employs flash-based firmware and integrated hardware protection to provide a complete solution for battery stack architectures composed of 1-series or 2-series cells. The bq28z610 device interfaces with a host system via an I^2C protocol. High-performance, integrated analog peripherals enable support for a sense resistor down to 1 mΩ and simultaneous current/voltage data conversion for instant power calculations. The following sections detail all of the major component blocks included as part of the bq28z610 device.

8.2 Functional Block Diagram

Figure 18 depicts the analog and digital peripheral content in the bq28z610 device.

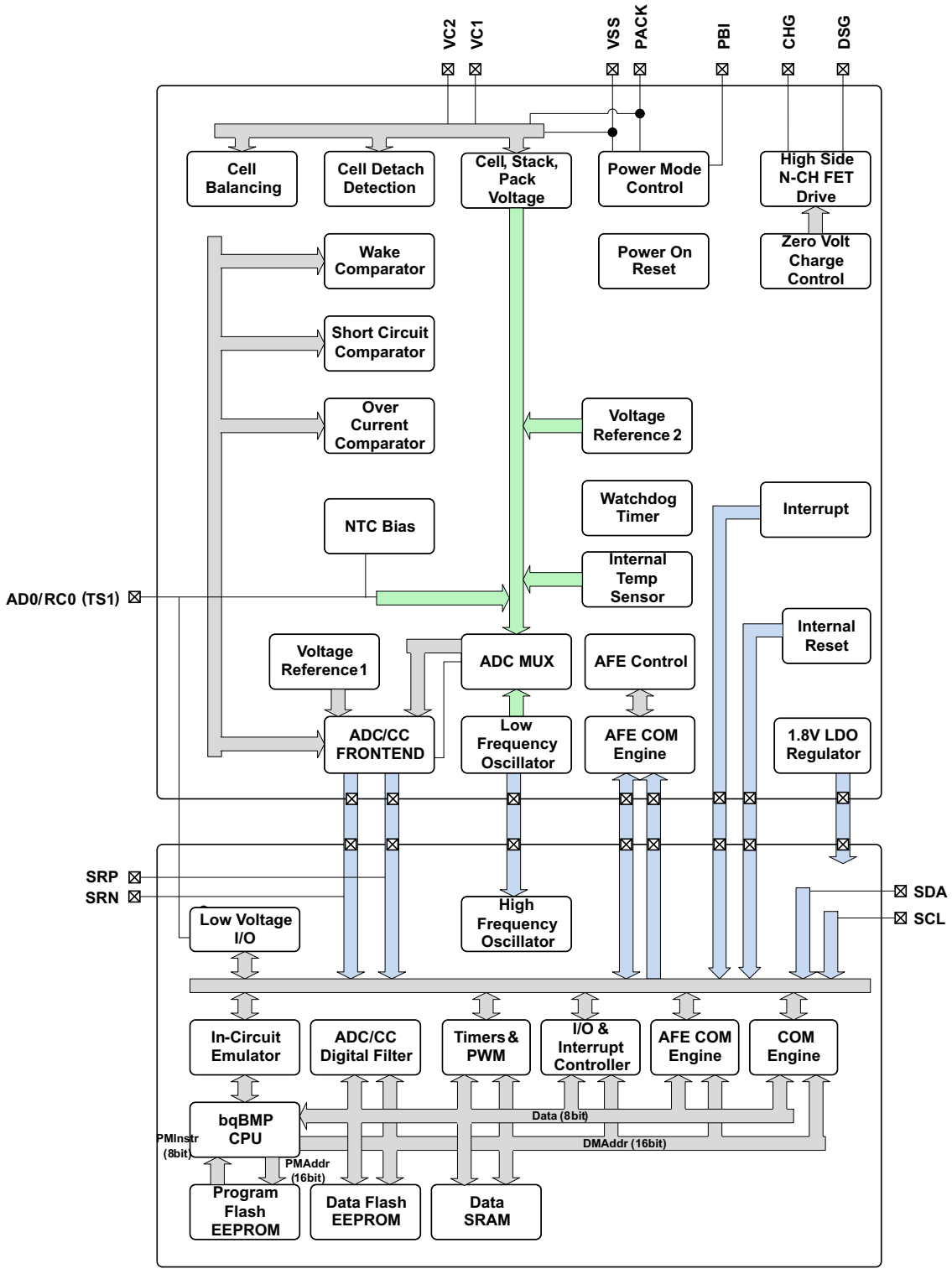


Figure 18. bq28z610 Functional Block Diagram

8.3 Feature Description

8.3.1 Battery Parameter Measurements

The bq28z610 device measures cell voltage and current simultaneously and also measures temperature to calculate the information related to remaining capacity, full charge capacity, state of health, and other gauging parameters.

8.3.1.1 bq28z610 Processor

The bq28z610 device employs a custom, TI-proprietary processor design that features a Harvard architecture and operates at frequencies up to 4.2 MHz. Using an adaptive, three-stage instruction pipeline, the bq28z610 processor supports variable instruction length of 8, 16, or 24 bits.

8.3.2 Coulomb Counter (CC)

The first ADC is an integrating converter designed specifically for coulomb counting. The converter resolution is a function of its full-scale range and number of bits, yielding a 3.74-µV resolution.

8.3.3 CC Digital Filter

The CC digital filter generates a 16-bit conversion value from the delta-sigma CC front-end. Its FIR filter uses the LFO clock output, which allows it to stop the HFO clock during conversions. New conversions are available every 250 ms while CCTL[CC_ON] = 1. Proper use of this peripheral requires turning on the CC modulator in the AFE.

8.3.4 ADC Multiplexer

The ADC multiplexer provides selectable connections to the VCx inputs, TS1 inputs, internal temperature sensor, internal reference voltages, internal 1.8-V regulator, PACK input, and VSS ground reference input. In addition, the multiplexer can independently enable the TS1 input connection to the internal thermistor biasing circuitry, and also enables the user to short the multiplexer inputs for test and calibration purposes.

8.3.5 Analog-to-Digital Converter (ADC)

The second ADC is a 16-bit delta-sigma converter designed for general-purpose measurements. The ADC automatically scales the input voltage range during sampling based on channel selection. The converter resolution is a function of its full-scale range and number of bits, yielding a 38-µV resolution. The default conversion time of the ADC is 31.25 ms, but is user-configurable down to 1.95 ms. Decreasing the conversion time presents a tradeoff between conversion speed and accuracy, as the resolution decreases for faster conversion times.

8.3.6 ADC Digital Filter

The ADC digital filter generates a 24-bit conversion result from the delta-sigma ADC front end. Its FIR filter uses the LFO clock, which allows it to stop the HFO clock during conversions. The ADC digital filter is capable of providing two 24-bit results: one result from the delta-sigma ADC front-end and a second synchronous result from the delta-sigma CC front-end.

8.3.7 Internal Temperature Sensor

An internal temperature sensor is available on the bq28z610 device to reduce the cost, power, and size of the external components necessary to measure temperature. It is available for connection to the ADC using the multiplexer, and is ideal for quickly determining pack temperature under a variety of operating conditions.

8.3.8 External Temperature Sensor Support

The TS1 input is enabled with an internal 18-kΩ (Typ.) linearization pull-up resistor to support the use of a 10-kΩ (25°C) NTC external thermistor, such as the Semitec 103AT-2. The NTC thermistor should be connected between VSS and the individual TS1 pin. The analog measurement is then taken via the ADC through its input multiplexer. If a different thermistor type is required, then changes to configurations may be required.

Feature Description (continued)

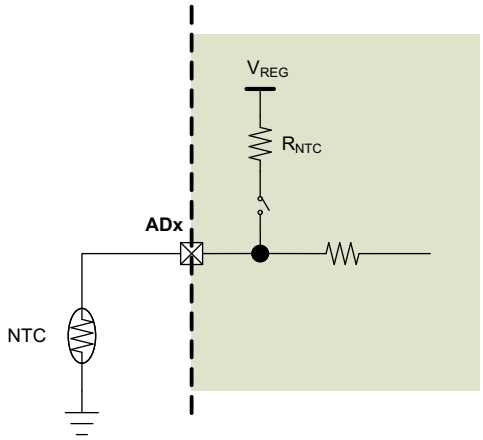


Figure 19. External Thermistor Biasing

8.3.9 Power Supply Control

The bq28z610 device manages its supply voltage dynamically according to operating conditions. When $V_{VC2} > V_{SWITCHOVER–} + V_{HYS}$, the AFE connects an internal switch to BAT and uses this pin to supply power to its internal 1.8-V LDO, which subsequently powers all device logic and flash operations. Once VC2 decreases to $V_{VC2} < V_{SWITCHOVER–}$, the AFE disconnects its internal switch from VC2 and connects another switch to PACK, allowing sourcing of power from a charger (if present). An external capacitor connected to PBI provides a momentary supply voltage to help guard against system brownouts due to transient short-circuit or overload events that pull VC2 below $V_{SWITCHOVER–}$.

8.3.10 Power-On Reset

In the event of a power-cycle, the bq28z610 AFE holds its internal RESET output pin high for t_{RST} duration to allow its internal 1.8-V LDO and LFO to stabilize before running the AGG. The AFE enters power-on reset when the voltage at V_{REG} falls below $V_{REGIT–}$ and exits reset when V_{REG} rises above $V_{REGIT–} + V_{HYS}$ for t_{RST} time. After t_{RST}, the bq28z610 AGG will write its trim values to the AFE.

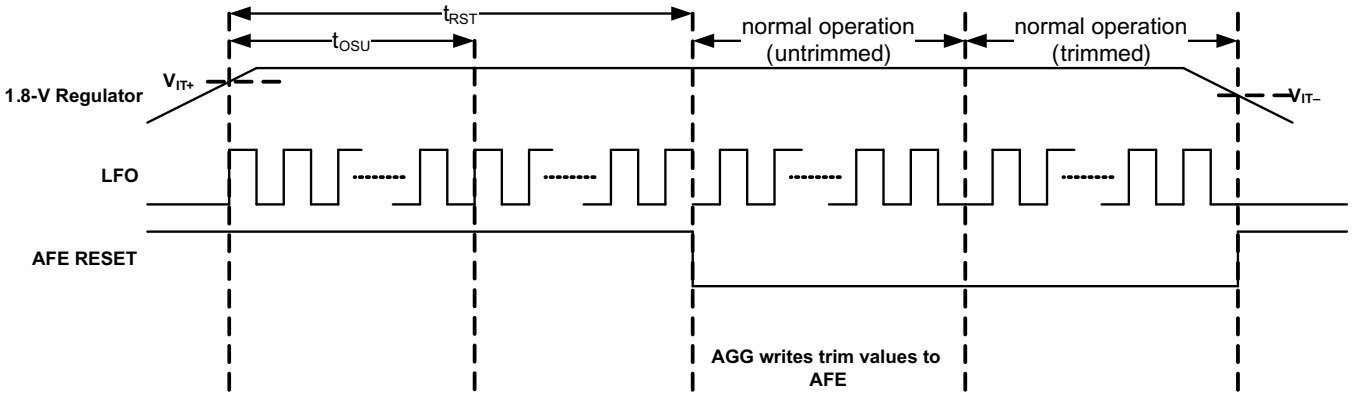


Figure 20. POR Timing Diagram

8.3.11 Bus Communication Interface

The bq28z610 device has an I^2C bus communication interface. This device has the option to broadcast information to a smart charger to provide key information to adjust the charging current and charging voltage based on the temperature or individual cell voltages.

Feature Description (continued)

CAUTION

If the device is configured as a single-master architecture (an application processor) and an occasional NACK is detected in the operation, the master can resend the transaction. However, in a multi-master architecture, an incorrect ACK leading to accidental loss of bus arbitration can cause a master to wait incorrectly for another master to clear the bus. If this master does not get a bus-free signal, then it must have in place a method to look for the bus and assume it is free after some period of time. Also, if possible, set the clock speed to be 100 kHz or less to significantly reduce the issue described above for multi-mode operation.

8.3.12 Cell Balancing Support

The integrated cell balancing FETs included in the bq28z610 device enable the AFE to bypass cell current around a given cell or numerous cells to effectively balance the entire battery stack. External series resistors placed between the cell connections and the VCx input pins set the balancing current magnitude. The cell balancing circuitry can be enabled or disabled via the CELL_BAL_DET[CB2, CB1] control register. Series input resistors between 100 Ω and 1 kΩ are recommended for effective cell balancing.

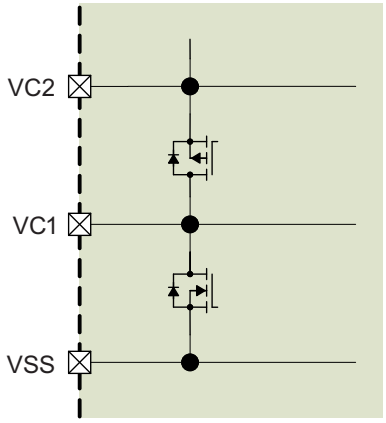


Figure 21. Internal Cell Balancing

8.3.13 N-Channel Protection FET Drive

The bq28z610 device controls two external N-Channel MOSFETs in a back-to-back configuration for battery protection. The charge (CHG) and discharge (DSG) FETs are automatically disabled if a safety fault (AOLD, ASSC, ASCD, SOV) is detected, and can also be manually turned off using AFE_CONTROL[CHGEN, DSGEN] = 0, 0. When the gate drive is disabled, an internal circuit discharges CHG to VC2 and DSG to PACK.

8.3.14 Low Frequency Oscillator

The bq28z610 AFE includes a low frequency oscillator (LFO) running at 262.144 kHz. The AFE monitors the LFO frequency and indicates a failure via LATCH_STATUS[LFO] if the output frequency is much lower than normal.

8.3.15 High Frequency Oscillator

The bq28z610 AGG includes a high frequency oscillator (HFO) running at 16.78 MHz. It is synthesized from the LFO output and scaled down to 8.388 MHz with 50% duty cycle.

8.3.16 1.8-V Low Dropout Regulator

The bq28z610 AFE contains an integrated 1.8 V LDO that provides regulated supply voltage for the device CPU and internal digital logic.

Feature Description (continued)

8.3.17 Internal Voltage References

The bq28z610 AFE provides two internal voltage references with V_{REF1}, used by the ADC and CC, while V_{REF2} is used by the LDO, LFO, current wake comparator, and OCD/SCC/SCD1/SCD2 current protection circuitry.

8.3.18 Overcurrent in Discharge Protection

The overcurrent in discharge (OCD) function detects abnormally high current in the discharge direction. The overload in discharge threshold and delay time are configurable via the OCD_CONTROL register. The thresholds and timing can be fine-tuned even further based on a sense resistor with lower resistance or wider tolerance via the PROTECTION_CONTROL register. The detection circuit also incorporates a filtered delay before disabling the CHG and DSG FETs. When an OCD event occurs, the LATCH_STATUS[OCD] bit is set to 1 and is latched until it is cleared and the fault condition has been removed.

8.3.19 Short-Circuit Current in Charge Protection

The short-circuit current in charge (SCC) function detects catastrophic current conditions in the charge direction. The short-circuit in charge threshold and delay time are configurable via the SCC_CONTROL register. The thresholds and timing can be fine-tuned even further based on a sense resistor with lower resistance or wider tolerance via the PROTECTION_CONTROL register. The detection circuit also incorporates a blanking delay before disabling the CHG and DSG FETs. When an SCC event occurs, the LATCH_STATUS[SCC] bit is set to 1 and is latched until it is cleared and the fault condition has been removed.

8.3.20 Short-Circuit Current in Discharge 1 and 2 Protection

The short-circuit current in discharge (SCD) function detects catastrophic current conditions in the discharge direction. The short-circuit in discharge thresholds and delay times are configurable via the SCD1_CONTROL and SCD2_CONTROL registers. The thresholds and timing can be fine-tuned even further based on a sense resistor with lower resistance or wider tolerance via the PROTECTION_CONTROL register. The detection circuit also incorporates a blanking delay before disabling the CHG and DSG FETs. When an SCD event occurs, the LATCH_STATUS[SCD1] or LATCH_STATUS[SCD2] bit is set to 1 and is latched until it is cleared and the fault condition has been removed.

8.3.21 Primary Protection Features

The bq28z610 gas gauge supports the following battery and system level protection features, which can be configured using firmware:

- Cell Undervoltage Protection
- Cell Overvoltage Protection
- Overcurrent in CHARGE Mode Protection
- Overcurrent in DISCHARGE Mode Protection
- Overload in DISCHARGE Mode Protection
- Short Circuit in CHARGE Mode Protection
- Overtemperature in CHARGE Mode Protection
- Overtemperature in DISCHARGE Mode Protection
- Precharge Timeout Protection
- Fast Charge Timeout Protection

8.3.22 Gas Gauging

This device uses the Impedance Track™ technology to measure and determine the available charge in battery cells. The accuracy achieved using this method is better than 1% error over the lifetime of the battery. There is no full charge/discharge learning cycle required. See the *Theory and Implementation of Impedance Track Battery Fuel-Gauging Algorithm* Application report (SLUA364B) for further details.

8.3.23 Charge Control Features

This device supports charge control features, such as:

- JEITA temperature ranges T1, T2, T3, T4, T5, and T6. Reports charging voltage and charging current based

Feature Description (continued)

on the active temperature range

- More complex charging profiles, including sub-ranges within a standard temperature range
- Reports the appropriate charging current required for constant current charging and the appropriate charging voltage needed for constant voltage charging to a smart charger, using the bus communication interface
- Determines the chemical state of charge of each battery cell using the Impedance Track method and with the use of cell balancing for multiple cells in series reduces the voltage difference between cells
- Pre-charging/zero-volt charging
- Charge inhibit and charge suspend if battery pack temperature is out of programmed range.
- Reports charging faults and indicates charge status via charge and discharge alarms

8.3.24 Authentication

This device supports security by:

- Authentication by the host using SHA-1 method
- SHA-1 authentication required by the gas gauge before device can be unsealed or allow full access

8.4 Device Functional Modes

This device supports three modes, but the current consumption varies, based on firmware control of certain functions and modes of operation:

- NORMAL mode: In this mode, the device performs measurements, calculations, protection decisions and data updates every 250-ms intervals. Between these intervals, the device is operating in a reduced power stage to minimize total average current consumption.
- SLEEP mode: In this mode, the device performs measurements, calculations, protection decisions and data updates in adjustable time intervals. Between these intervals, the device is operating in a reduced power stage to minimize total average current consumption.
- SHUTDOWN mode: The device is completely disabled.

8.4.1 Lifetime Logging Features

The device supports data logging of several key parameters for warranty and analysis:

- Maximum and Minimum Cell Temperature
- Maximum Current in CHARGE or DISCHARGE Mode
- Maximum and Minimum Cell Voltages

8.4.2 Configuration

The device supports accurate data measurements and data logging of several key parameters.

8.4.2.1 Coulomb Counting

The device uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement. The ADC measures charge/discharge flow of the battery by measuring the voltage across a very small external sense resistor. The integrating ADC measures a bipolar signal from a range of –100 mV to 100 mV, with a positive value when $V_{(SRP)} - V_{(SRN)}$, indicating charge current and a negative value indicating discharge current. The integration method uses a continuous timer and internal counter, which has a rate of 0.65 nVh.

8.4.2.2 Cell Voltage Measurements

The bq28z610 measures the individual cell voltages at 250-ms intervals using an ADC. This measured value is internally scaled for the ADC and is calibrated to reduce any errors due to offsets. This data is also used for calculating the impedance of the individual cell for Impedance Track gas gauging.

8.4.2.3 Current Measurements

The current measurement is performed by measuring the voltage drop across the external sense resistor (1 mΩ to 3 mΩ) and the polarity of the differential voltage determines if the cell is in the CHARGE or DISCHARGE mode.

Device Functional Modes (continued)

8.4.2.4 Auto Calibration

The auto-calibration feature helps to cancel any voltage offset across the SRP and SRN pins for accurate measurement of the cell voltage, charge/discharge current, and thermistor temperature. The auto-calibration is performed when there is no communication activity for a minimum of 5 s on the bus lines.

8.4.2.5 Temperature Measurements

This device has an internal sensor for on die temperature measurement and ability to support external temperature measurements via the external NTC on the TS1 pin. These two measurements are individually enabled and configured.

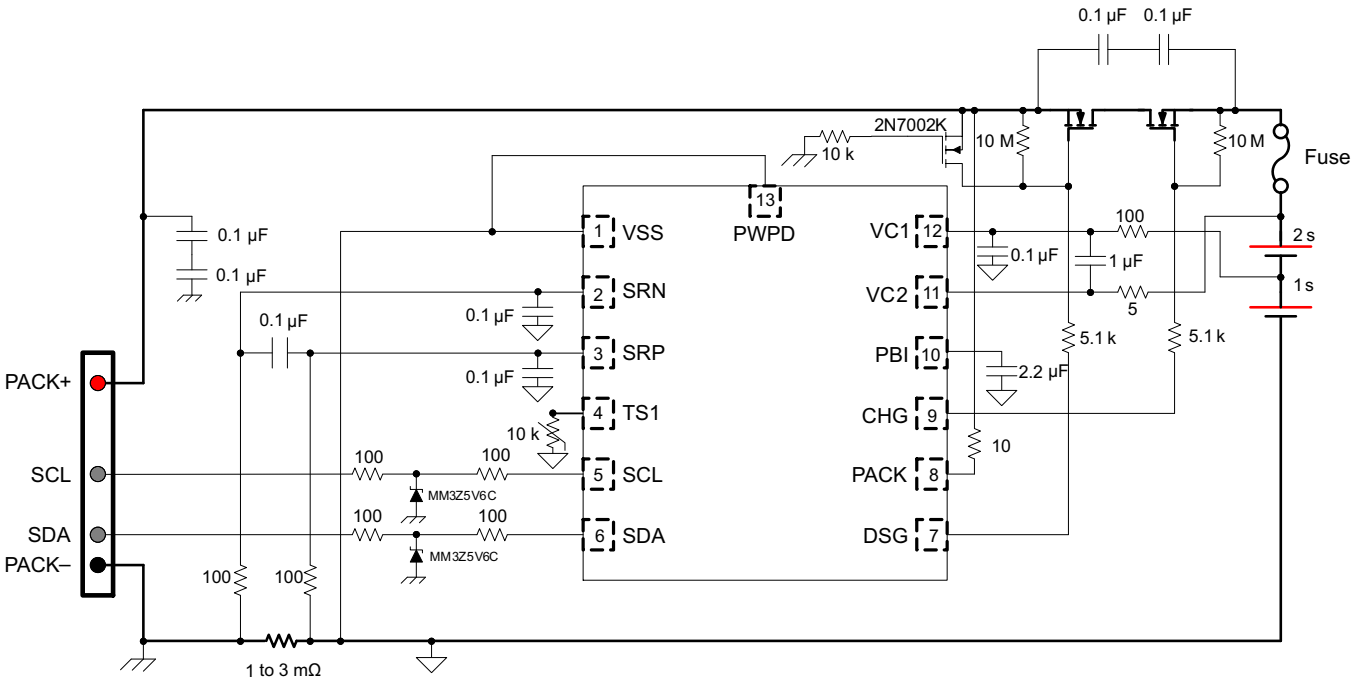
9 Applications and Implementation

9.1 Application Information

The bq28z610 gas gauge is a primary protection device that can be used with a 1-series or 2-series Li-Ion/Li Polymer battery pack. To implement and design a comprehensive set of parameters for a specific battery pack, the user needs Battery Management Studio (bqStudio), which is a graphical user-interface tool installed on a PC during development. The firmware installed in the product has default values, which are summarized in the *bq28z610 Technical Reference Manual* (SLUUA65) for this product. Using the BMS tool, these default values can be changed to cater to specific application requirements during development once the system parameters are known, such as fault trigger thresholds for protection, enable/disable of certain features for operation, configuration of cells, chemistry that best matches the cell used, and more. This data can be referred to as the "golden image."

9.2 Typical Applications

The following is the bq28z610 application schematic for the 2-series configuration.



Note: The input filter capacitors of 0.1 µF for the SRN and SRP pins must be located near the pins of the device.

Figure 22. bq28z610 2-Series Cell Typical Implementation

9.2.1 Design Requirements (Default)

Design Parameter	Example
Cell Configuration	2s1p (2-series with 1 Parallel)
Design Capacity	4400 mAH
Device Chemistry	100 (LiCoO2/graphitized carbon)
Cell Overvoltage at Standard Temperature	4300 mV
Cell Undervoltage	2500 mV
Shutdown Voltage	2300 mV
Overcurrent in CHARGE Mode	6000 mA
Overcurrent in DISCHARGE Mode	–6000 mA
Short Circuit in CHARGE Mode	0.1 V/Rsense across SRP, SRN

Typical Applications (continued)

Design Parameter	Example
Short Circuit in DISCHARGE 1 Mode	0.1 V/Rsense across SRP, SRN
Safety Over Voltage	4500 mV
Cell Balancing	Disabled
Internal and External Temperature Sensor	Enabled
Under Temperature Charging	0°C
Under Temperature Discharging	0°C
BROADCAST Mode	Enabled

9.2.2 Detailed Design Procedure

9.2.2.1 Setting Design Parameters

For the firmware settings needed for the design requirements, refer to the *bq28z610 Technical Reference Manual* (SLUUA65).

- To set the 2s1p battery pack, go to data flash ***Configuration: DA Configuration*** register's bit 0 (CC0) = 1.
- To set design capacity, set the data flash value to 4400 in the ***Gas Gauging: Design: Design Capacity*** register.
- To set device chemistry, go to data flash ***SBS Configuration: Data: Device Chemistry***. The bqStudio software automatically populates the correct chemistry identification. This selection is derived from using the bqCHEM feature in the tools and choosing the option that matches the device chemistry from the list.
- To protect against cell overvoltage, set the data flash value to 4300 in ***Protections: COV: Standard Temp***.
- To protect against cell undervoltage, set the data flash value to 2500 in the ***Protections: CUV*** register.
- To set the shutdown voltage to prevent further pack depletion due to low pack voltage, program ***Power: Shutdown: Shutdown*** voltage = 2300.
- To protect against large charging currents when the AC adapter is attached, set the data flash value to 6000 in the ***Protections: OCC: Threshold*** register.
- To protect against large discharging currents when heavy loads are attached, set the data flash value to –6000 in the ***Protections: OCD: Threshold*** register.
- Program a short circuit delay timer and threshold setting to enable the operating the system for large short transient current pulses. These two parameters are under ***Protections: ASCC: Threshold*** = 100 for charging current. The discharge current setting is Protections: ASCD:Threshold = –100 mV.
- To prevent the cells from overcharging and adding a second level of safety, there is a register setting that will shutdown the device if any of the cells voltage measurement is greater than the Safety Over Voltage setting for greater than the delay time. Set this data flash value to 4500 in ***Permanent Fail: SOV: Threshold***.
- To disable the cell balancing feature, set the data flash value to 0 in ***Settings: Configuration: Balancing Configuration***: bit 0 (CB).
- To enable the internal temperature and the external temperature sensors: Set ***Settings:Configuration: Temperature Enable***: Bit 0 (TSInt) = 1 for the internal sensor; set Bit 1 (TS1) = 1 for the external sensor.
- To prevent charging of the battery pack if the temperature falls below 0°C, set ***Protections: UTC:Threshold*** = 0.
- To prevent discharging of the battery pack if the temperature falls below 0°C, set ***Protections: UTD:Threshold*** = 0.
- To provide required information to the smart chargers, the gas gauge must operate in BROADCAST mode. To enable this, set the [BCAST] bit in ***Configuration: SBS Configuration*** 2: Bit 0 [BCAST] = 1.

Each parameter listed for fault trigger thresholds has a delay timer setting associated for any noise filtering. These values, along with the trigger thresholds for fault detection, may be changed based upon the application requirements using the data flash settings in the appropriate register stated in the *bq28z610 Technical Reference Manual* (SLUUA65).

9.2.3 Calibration Process

The calibration of Current, Voltage, and Temperature readings is accessible by writing 0xF081 or 0xF082 to *ManufacturerAccess()*. A detailed procedure is included in the *bq28z610 Technical Reference Manual* (SLUUA65) in the *Calibration* section. The description allows for calibration of Cell Voltage Measurement Offset, Battery Voltage, Pack Voltage, Current Calibration, Coulomb Counter Offset, PCB Offset, CC Gain/Capacity Gain, and Temperature Measurement for both internal and external sensors.

10 Power Supply Requirements

There are two inputs for this device, the PACK input and VC2. The PACK input can be an unregulated input from a typical AC adapter. This input should always be greater than the maximum voltage associated with the number of series cells configured. The input voltage for the VC2 pin will have a minimum of 2.2 V to a maximum of 26 V with the recommended external RC filter.

11 Layout

11.1 Layout Guidelines

- The layout for the high-current path begins at the PACK+ pin of the battery pack. As charge current travels through the pack, it finds its way through protection FETs, a chemical fuse, the lithium-ion cells and cell connections, and the sense resistor, and then returns to the PACK– pin. In addition, some components are placed across the PACK+ and PACK– pins to reduce effects from electrostatic discharge.
- The N-channel charge and discharge FETs must be selected for a given application. Most portable battery applications are a good option for the CSD16412Q5A. These FETs are rated at 14-A, 25-V device with Rds(on) of 11 mΩ when the gate drive voltage is 10 V. The gates of all protection FETs are pulled to the source with a high-value resistor between the gate and source to ensure they are turned off if the gate drive is open. The capacitors (both 0.1 µF values) placed across the FETs are to help protect the FETs during an ESD event. The use of two devices ensures normal operation if one of them becomes shorted. For effective ESD protection, the copper trace inductance of the capacitor leads must be designed to be as short and wide as possible. Ensure that the voltage rating of both these capacitors are adequate to hold off the applied voltage if one of the capacitors becomes shorted.
- The quality of the Kelvin connections at the sense resistor is critical. The sense resistor must have a temperature coefficient no greater than 50 ppm in order to minimize current measurement drift with temperature. Choose the value of the sense resistor to correspond to the available overcurrent and short-circuit ranges of the bq28z610. Select the smallest value possible in order to minimize the negative voltage generated on the bq28z610 VSS node(s) during a short circuit. This pin has an absolute minimum of –0.3 V. Parallel resistors can be used as long as good Kelvin sensing is ensured. The device is designed to support a 1-mΩ to 3-mΩ sense resistor.
- A pair of series 0.1-µF ceramic capacitors is placed across the PACK+ and PACK– pins to help in the mitigation of external electrostatic discharges. The two devices in series ensure continued operation of the pack if one of the capacitors becomes shorted. Optionally, a transorb such as the SMBJ2A can be placed across the pins to further improve ESD immunity.
- In reference to the gas gauge circuit the following features require attention for component placement and layout; Differential Low-Pass Filter, I^2C communication and PBI (Power Backup Input).
- The bq28z610 uses an integrating delta-sigma ADC for current measurements. Add a 100-Ω resistor from the sense resistor to the SRP and SRN inputs of the device. Place a 0.1-µF filter capacitor across the SRP and SRN inputs. Optional 0.1-µF filter capacitors can be added for additional noise filtering for each sense input pin to ground, if required for your circuit. Place all filter components as close as possible to the device. Route the traces from the sense resistor in parallel to the filter circuit. Adding a ground plane around the filter network can add additional noise immunity.

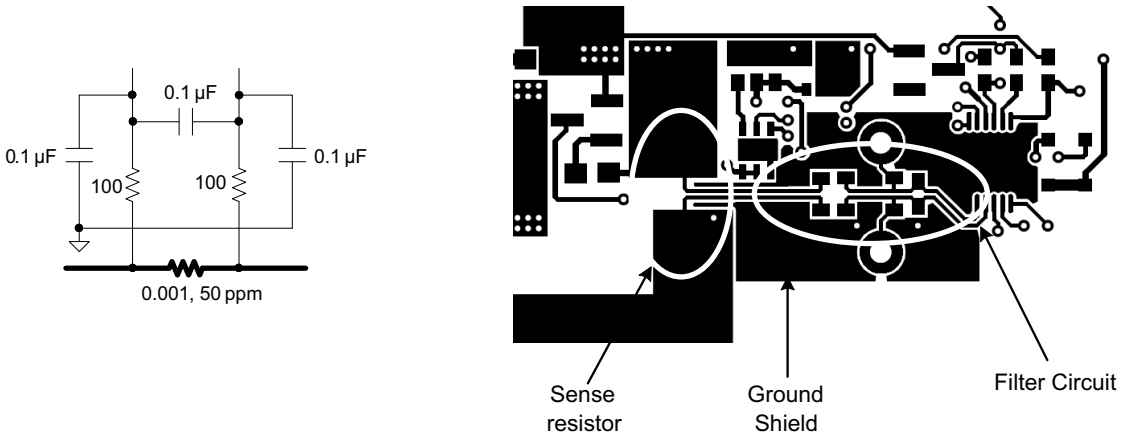


Figure 23. bq28z610 Differential Filter

- The bq28z610 has an internal LDO that is internally compensated and does not require an external decoupling capacitor. The PBI pin is used as a power supply backup input pin providing power during brief transient power outages. A standard 2.2-µF ceramic capacitor is connected from the PBI pin to ground, as shown in application example.
- The I^2C clock and data pins have integrated high-voltage ESD protection circuits; however, adding a Zener

Layout Guidelines (continued)

diode and series resistor provides more robust ESD performance. The I^2C clock and data lines have internal pull-down. When the gas gauge senses that both lines are low (such as during removal of the pack), the device performs auto-offset calibration and then goes into SLEEP mode to conserve power.

11.1.1 Layout Example

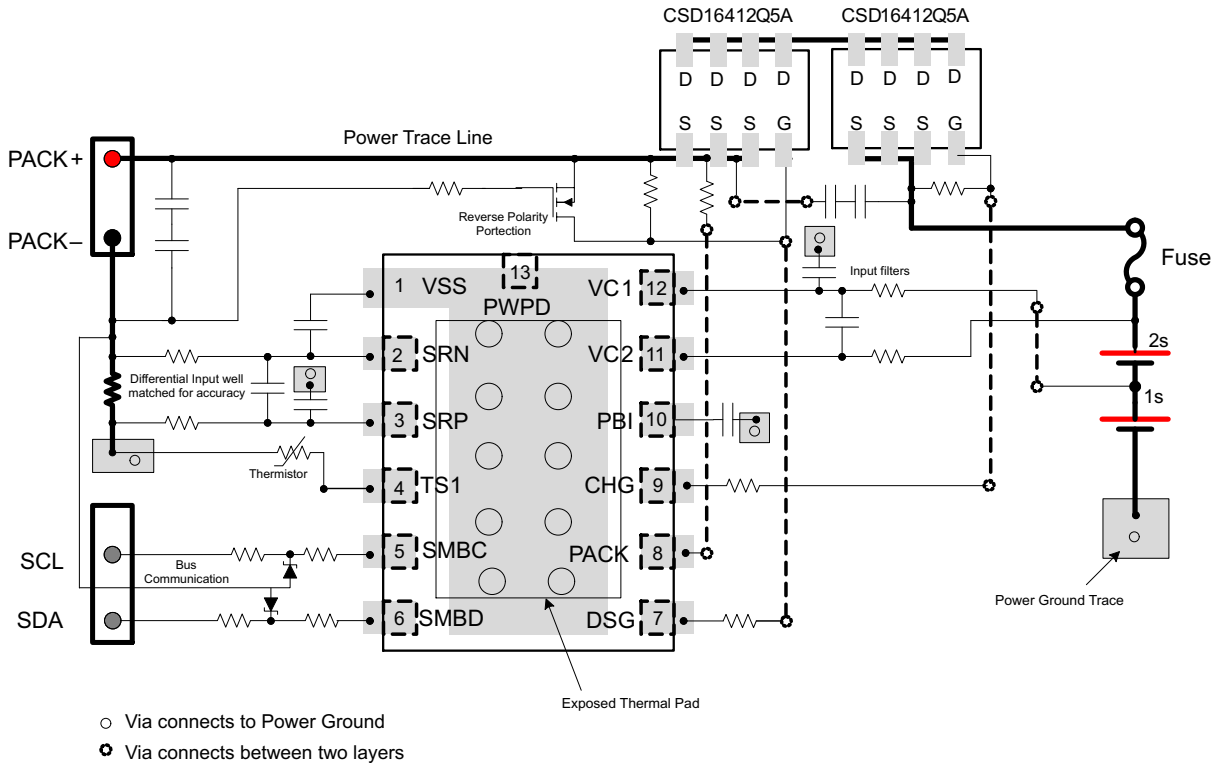


Figure 24. bq28z610 Board Layout

12 Device and Documentation Support

12.1 Trademarks

Impedance Track is a trademark of Texas Instruments.
I^2C is a trademark of NXP B.V. Corporation.

12.2 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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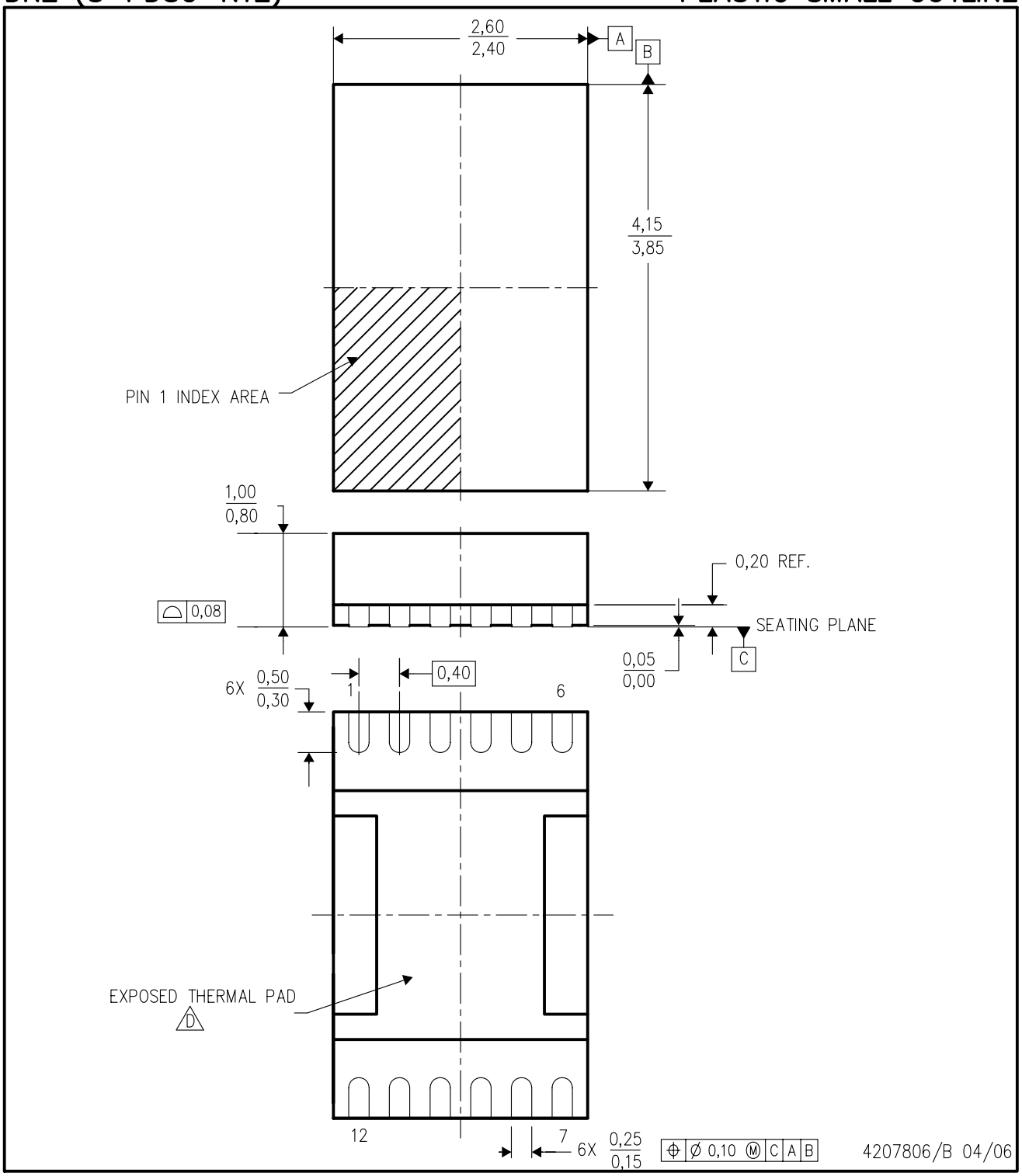
12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

DRZ (S–PDSO–N12) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. This package is lead–free.

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