

Assembly Program Analysis

Simulation Result

The table below follows the full code provided in this document, table below shows the effect of `JMP` and `PRESENT` as well.

Some degree of pipelining are applied to instructions that involves load and storage, the result will show up in the next cycle (next `IF1`).

Code	Time Duration	Mem\Reg\Port Location
<code>NOOP</code>	$0ns - 160ns$	n\ a
<code>LDR R1 #123</code>	$160ns - 400ns$	R1
<code>AND R2 R1 #111</code>	$400ns - 640ns$	R2
<code>LDR R3 R2</code>	$640ns - 840ns$	R3
<code>LDR R4 \$2</code>	$840ns - 1120ns$	R4
<code>SUBV R4 R1 #23</code>	$1120ns - 1360ns$	R4
<code>CLFZ</code>	$1120ns - 1520ns$	n\ a
<code>SUB R1 #23</code>	$1520ns - 1760ns$	n\ a
<code>STR R2 \$100</code>	$1760ns - 2000ns$	\$100
<code>LDR R6 \$100</code>	$2000ns - 2280ns$	R6
<code>ADD R7 R7 R3</code>	$2280ns - 2440ns$	R7
<code>PRESENT R8 \$16</code>	$2440ns - 2680ns$	n\ a
<code>NOOP</code>	$2680ns - 2840ns$	n\ a
<code>NOOP</code>	$2840ns - 3000ns$	n\ a
<code>NOOP</code>	$3000ns - 3160ns$	n\ a
<code>SSOP R1</code>	$3160ns - 3320ns$	SOP
<code>LSIP R11</code>	$3320ns - 3480ns$	R11
<code>MAX R1 #200</code>	$3480ns - 3720ns$	R1
<code>DCALLBL R2 #123</code>	$3720ns - 4840ns$ (blocked)	R0

AND R9 R1 #111	4840ns – 5080ns	R9
DCALLNB R2 #100	5080ns – 5320ns	DPCR
ADD R14 R13 #10	5320ns – 5560ns	R14
LDR R14 \$0	5560ns – 5920ns	R14
NOOP	5920ns – 6080ns	n\
NOOP	6080ns – 6240ns	n\
LDR R14	6240ns – 6520ns	R14
SUB R14 #3	6520ns – 6760ns	n\
OR R15 R14 #22	6760ns – 7000ns	R15
OR R15 R15 R3	7000ns – 7160ns	R15
STR R12 #55	7160ns – 7400ns	\$0
LDR R2 \$0	7400ns – 7680ns	R2
STR R12 R3	7680ns – 7840ns	\$0
LDR R2 \$0	7840ns – 8120ns	R2
SEOT	8120ns – 8280ns	EOT
SSVOP R4	8280ns – 8440ns	SVOP
CEOT	8440ns – 8600ns	EOT
LER R0	8600ns – 8760ns	R0
CER	8760ns – 8920ns	ER
STRPC \$0	8920ns – 9160ns	\$0
LDR R2 \$0	9160ns – 9440ns	R2
AND R0 R8 #20	9440ns – 9680ns	R0
JMP 20	9680ns – 9920ns	\$20
CLFZ	9920ns – 10120ns	z
NOOP	10120ns – 10240ns	n\
NOOP	10240ns – 10400ns	n\
NOOP	10400ns – 10560ns	n\
NOOP	10560ns – 10720ns	n\

SSOP R1	10720ns – 10880ns	SOP
LSIP R11	10880ns – 11040ns	R11
MAX R1 #200	11040ns – 11280ns	R1
DCALLBL R2 #100	11280ns – ∞ (blocked)	DPCR

Full Code Used for testing ReCOP

```

1  start NOOP
2  LDR R1 #123
3  AND R2 R1 #111
4  LDR R3 R2
5  LDR R4 $2
6  SUBV R4 R1 #23
7  CLFZ
8  SUB R1 #23
9
10 STR R2 $100
11 LDR R6 $100
12 ADD R7 R7 R3
13 PRESENT R8 $16
14 CLFZ
15 NOOP
16 NOOP
17 NOOP
18 NOOP
19 SSOP R1
20 LSIP R11
21 MAX R1 #200
22 DCALLBL R2 #123
23 AND R9 R1 #111
24 DCALLNB R2 #100
25 ADD R14 R13 #10
26 LDR R14 $0
27 NOOP
28 NOOP
29 LDR R14 $0
30 SUB R14 #3
31 OR R15 R14 #22
32 OR R15 R15 R3
33 STR R12 #55
34 LDR R2 $0
35 STR R12 R3
36 LDR R2 $0
37 SEOT
38 SSVOP R4

```

```
39      CEOT
40      LER  R0
41      CER
42      STRPC $0
43      LDR  R2  $0
44      AND  R0  R8  #20
45      JMP  20
46      NOOP
47      DCALLBL R0
48
49  ENDPROG
```