



Department of Electrical and Computer Engineering
COMPSYS 701 – Advanced Digital Systems Design
Final Report

Heterogeneous Multiprocessor System on Network-on-Chip Design

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Abstract

Processors architecture size and maximum frequencies are hitting their limits. To further improve performance, multi-core systems are required.

Keywords

Processor design; Network-on-chip

I. INTRODUCTION

II. NETWORK-ON-CHIP STRUCTURE

A. Basic Architecture

B. Configuration

III. REACTIVE COPROCESSOR (AJS)

A. Control Unit

B. Datapath

C. Data Format

D. Simulation

IV. APPLICATION SPECIFIC PROCESSOR

A. Control Unit

B. Datapath

C. Operations

D. Data Format

V. ASP NETWORK INTERFACE

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B. Interaction with TDMA-MIN

C. Timing

D. Simulation

E. Sythesis

F. FPGA Testing

G. Performance Analysis

VI. JOP NETWORK INTERFACE

VII. JAVA PROGRAMMES

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IX. PERFORMANCE ANALYSIS

X. CONCLUSION

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