1. Description

PSC2945 combines a highly integrated switch-mode charger, to minimize single-cell Lithium-ion (Li-ion) charging time from a USB power source, and a boost regulator to power a USB peripheral from the battery.

Its low impedance power path optimizes switch-mode operation efficiency, reduces battery charge time and extends battery life during discharging phase. The I2C serial interface with charging and system settings makes the device a truly flexible solution.

The device supports 3.5-12V input voltage sources, including standard USB host port and USB charging port with programmable over-voltage protection. The device also supports USB On-the-Go operation by providing on the VBUS with an accurate current limit.

The power path management regulates the system slightly above battery voltage but does not drop below 3.55V minimum system voltage (programmable). With this feature, the system keeps operating even when the battery is completely depleted or removed. When the input source current or voltage limit is reached, the power path management automatically reduces the charge current to zero and then starts discharges the battery until the system power requirement is met. This supplement mode operation keeps the input source from getting overloaded.

The device initiates and completes a charging cycle when host control is not available. It automatically charges the battery in three phases: pre-conditioning, constant current, and constant voltage. In the end, the charger automatically terminates when the charge current is below a preset limit in the constant voltage phase. Later on, when the battery voltage falls below the recharge threshold, the charger automatically starts another charging cycle.

The charge device provides various safety features for battery charging and system operation, including charging safety timer, and over-voltage/over-current protections.

The STAT output reports the charging status. The INT output can be used to notify the host when VBUS insertion and withdrawal or a fault occurs.

The PSC2945 is available in a 24-pin, 4mm x 4mm x 0.55mm QFN package.

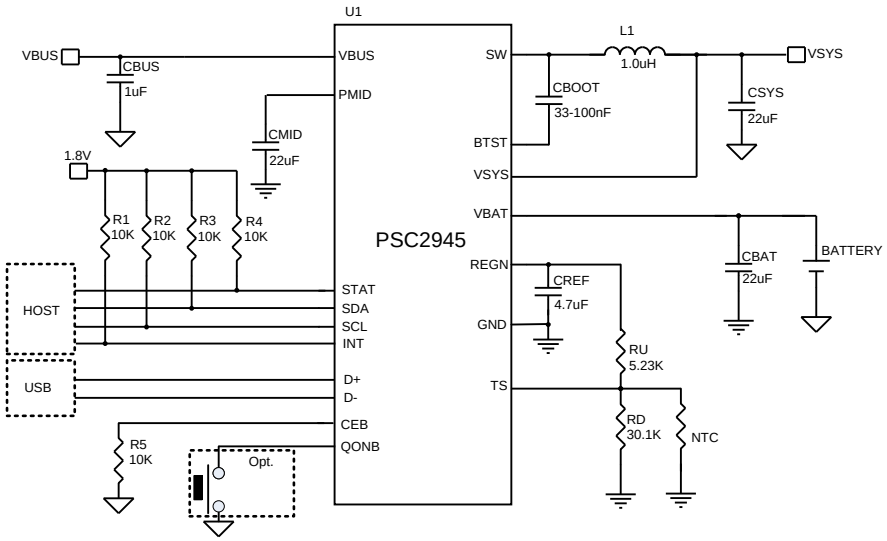


Figure 1.1: Typical Application

2. Features

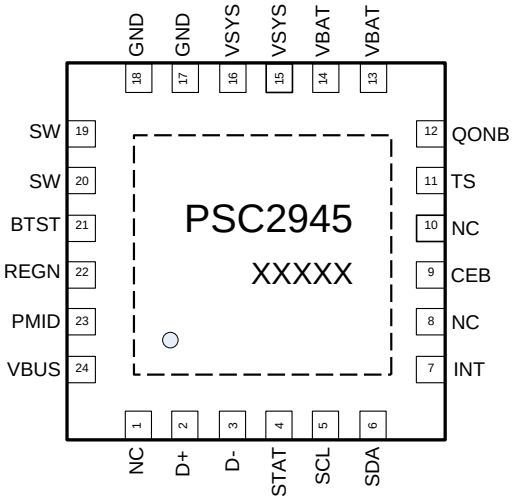
- Fully Integrated, High-Efficiency Switching Mode 3A Charger.
  - Charge Voltage Accuracy: ±0.5% 25℃
  - ±7.5% Charge Current Regulation Accuracy
  - 20V Absolute Maximum Input Voltage
  - 13.9V Maximum Input Operating Voltage
  - Weak Input Sources Accommodated by Reducing Charging Current to Maintain Minimum VBUS Voltage
- Power Path Management
  - Instant system on with NO battery or deeply discharged battery
  - Battery can be completely turned off after Charging Done
  - Supports Ultra low leakage ship mode
- Programmable through I2C Interface:
  - Input Current limit
  - Fast-Charge/Termination Current
  - Charger Voltage
  - Termination Enable
- Small Footprint 1-2.2μH External Inductor
- Low Reverse Leakage to Prevent Battery Drain to VBUS
- High Battery Discharge Efficiency With 25mΩ Battery Discharge MOSFET
- High Integration Includes All MOSFETs, Current Sensing and Loop Compensation
- 10μA Low Battery Leakage Current to Support Ship Mode
- 12uA Low Battery Leakage Current in standby Mode
- 5V, 2A Boost Mode for USB OTG: 90% efficiency at 5V/1A
- QFN24L4x4mm^2 package

3. Applications

- Cellular Phones, Smart Phones, PDAs
- Tablet, Portable Media Players

Key Components	Recommended specification
L1	Inductor, 1.0-2.2uH, +-20%, Isat>4A
C_{MID}	Capacitor, 22μF , +-10%, >16V
C_{REF}	Capacitor, 4.7μF, +-10%, >6V
C_{BUS}	Capacitor, 1.0μF, +-10%, >16V
C_{BOOT}	Capacitor, 100nF, +-10%, >10V

4. Pin Configuration and Marking



PSC2945: Product ID
XXXXX: Production Tracing Code

Figure 4.1: QFN4X4-24L TOP view

Pin functions

Name	Pin #	Type	Description
VBUS	24	P	Charger Input Voltage. Place a 1-μF ceramic capacitor from VBUS to GND and place it as close as possible to IC.
-	1,8,10	-	NC.
DP	2	IO	Positive data-port for USB transceiver.
DM	3	IO	Negative data-port for USB transceiver.
STAT	4	O	Open drain charge status output to indicate charger status. HIGH indicates charge disabled.
SCL	5	I	I^2C Interface clock. Connect SCL to the logic rail through a 10-kΩ resistor.
SDA	6	I/O	I^2C Interface data. Connect SDA to the logic rail through a 10-kΩ resistor.
INT	7		Open-drain interrupt Output. The INT pin sends an pulse to host to report charger device status and fault.
CEB	9	I	Charge Enable pin. Battery charging is enabled when this pin is driven low. Battery charging (Excluding Ishort) and Vsys regulator are disable when CEB is high.

Name	Pin #	Type	Description
TS	11	A	Temperature qualification voltage input. Connect a negative temperature coefficient thermistor between TS and GND. 103AT-2 thermistor is preferred.
QONB	12	IO	BATFET enable/reset control input. The pin contains internal pull-up so it could be floating if it is not used. Pull down QONB for about 430ms will turn on BATFET and exit ship mode. When VBUS is not valid, a logic low of typically 20s duration cuts VSYS from VBAT for 430ms and then re-enables BATFET to provide full system power reset.
VBAT	13,14	P	Battery connection point to the positive pin of the battery pack. The internal Q4 is connected between VBAT and VSYS. Connect 22 µF x2 closely to the VBAT pin.
VSYS	15,16	P	System power supply. Connect 22 µF x2 closely to the VBAT pin.
GND	17,18	G	Power ground connection for high-current power converter node. On PCB layout, connect directly to ground connection of input and output capacitors of the charger. A single point connection is recommended between power PGND and the analog GND near the IC PGND pin.
SW	19,20	O	Switching node connecting to output inductor. Internally SW is connected to the source of the High-side NMOS and the drain of the low-side NMOS.
BTST	21	P	PWM high side driver positive supply. Internally, the BTST is connected to the anode of the boost-strap diode.
REGN	22	P	PWM low side driver positive supply output. Internally, REGN is connected to the cathode of the boost- strap diode.
PMID	23	O	Power input to the charge regulator. Connect a 22uF ceramic capacitor from PMID to analog GND.
Thermal PAD	Thermal PAD	P	Exposed pad for heat dissipation. Always solder thermal pad to the board, and have via on the thermal pad plane star-connecting to GND.

5. Specifications

5.1 Maximum Ratings and Thermal Characteristics

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Parameter (TA=25℃ unless otherwise noted**)**		**Symbol**	**Min.**	**Max.**	**Units**
VBUS Voltage	Continuous	V_{BUS}	-0.3	20	V
STAT, INT Voltage		V_{STAT}	-0.3	7	V
PMID		V_I	-0.3	20	V
SW Voltage			-0.3	18	
VSYS, VBAT, REGN, CEB Voltage			-0.3	7	
Voltage on Other Pins		V_O	-0.3	6.5(1)	V
Maximum VBUS Slope above 5.5V when Boost or Charger are Active		$\frac{dV_{BUS}}{dt}$		4	V/μs
Electrostatic Discharge Protection Level	Human Body Model per JESD22-A114	ESD	2000		V
	Charged Device Model per JESD22-C101		500		
Junction Temperature		T_J	-40	+150	℃
Storage Temperature		T_{STG}	-65	+150	℃
Lead Soldering Temperature, 10 Seconds		T_L		+260	℃

Note:

1: Lesser of 6.5V or V_I + 0.3V.

5.2 Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Prisemi does not recommend exceeding them or designing to absolute maximum ratings.

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{BUS}	4.5	12	V
Maximum Battery Voltage when Boost enabled	$V_{BAT(MAX)}$		4.5	V
Input Current	Iin		2.5	A
Output Current	Isys		3	A
Fast Charging Current			3	A
Discharge Current thru internal MOSFET			4.5	A
Ambient Temperature	T_A	-30	+85	℃
Junction Temperature (see Thermal Protection section)	T_J	-30	+140	℃

5.3 Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperature T_A.

Parameter	Symbol	Typical	Units
Junction-to-Ambient Thermal Resistance	θ_{JA}	35	℃/W
Junction-to-PCB Thermal Resistance	θ_{JB}	10	℃/W

5.4 Electrical Characteristics

Unless otherwise specified: according to the circuit of Fig.1.1; recommended operating temperature range for T_J and T_A; V_{BUS}=5.0V, Charge Mode; and typical values are for T_J=25℃.(Unless otherwise noted.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
VBUS Current	I_{VBUS}	$V_{BUS}>V_{BUS(MIN)}$, PWM Switching		8		mA
		$V_{BUS}>V_{BUS(MIN)}$; PWM Enabled, Not Switching ;		1.3		mA
VBAT to VBUS Leakage Current	I_{LKG}	0℃<T_J<85℃, V_{BAT}=4.2V,V_{BUS}=0V		0.2		μA
Battery Leakage	I_{BAT}	VBAT = 4.2 V, No VBUS, Not in boost mode, BATFET Disabled. TJ < 85°C		10		μA
Battery Leakage	I_{BAT}	VBAT = 4.2 V, No VBUS, Not in boost mode, BATFET Enabled. TJ < 85°C		12		μA
Charge Voltage Range	V_{OREG}		3.6		4.45	V
Charge Voltage Accuracy		TJ=25℃	-0.5%		+0.5%	
		TJ=0~125℃	-1%		1%	
Output Charge Current Range	I_{OCHRG}	V_{LOWV} < V_{BAT} < V_{OREG}	400		2800	mA
Charge Current Accuracy		T_J<85℃,VBAT=3.8V REG04[6:4]=100 REGA0[6:5]=01		±7.5		%
Pre-charge Current	I_{PRECHG}	REGA0[6:5]=00		165		mA
		REGA0[6:5]=01		303		
		REGA0[6:5]=10		433		
		REGA0[6:5]=11		560		
Linear Charging Current	I_{SHORT}		11	18	25	mA
Battery Short Voltage	V_{SHORT}		2.2	2.4	2.5	V
Termination Current Range	$I_{(TERM)}$	V_{BAT} > V_{OREG} – V_{RCH}	140		470	mA
Wake-up voltage Range	V_{wakeup}	Pre-Charge Current if VBAT is lower than V_{wakeup}	2.85	3.0	3.15	V
VBUS Operating Voltage	V_{IN_VALID}	Valid VBUS voltage for charging	3.5		13.9	V
VBUS Validation Time	t_{VBUS_VALID}			25		ms
Special Charger Setpoint	V_{SP}		-3		+3	%

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Recharge Threshold	V_{RCH}	Below $V_{(OREG)}$		190		mV
	t_{RCH}			10		ms
Sleep-Mode Entry Threshold, $V_{BUS} – V_{BAT}$	V_{SLP}	V_{BUS} Falling		0.25		V
System regulation voltage	V_{SYS_MIN}		3.2	3.6	3.6	V
System Regulation Voltage	V_{SYS_MAX}			4.5		V
SYS-BAT MOSFET	$R_{ON(Q4)}$	Temperature: 25℃		25	40	mΩ
SYS-BAT MOSFET	$R_{ON(Q4)}$	Temperature: 0-85℃		25	45	mΩ
Input current pulse control						
Current stop pulse width	T_{pump_stop}		430	500	570	ms
Current long on pulse width	T_{pump_on1}		240	300	360	ms
Current short on pulse width	T_{pump_on2}		70	100	130	ms
Current pulse off pulse	T_{pump_off}		70	100	130	ms
Current stop start delay	T_{pump_delay}		80	150	225	ms

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
VBUS to PGND Resistance	R_{VBUS}	Normal Operation		1500		KΩ
VBUS Over-Voltage Shutdown	$VBUS_{OVP}$	V_{BUS} Rising (need i2c set)	6.9		13.9	V
Hysteresis		V_{BUS} Falling		140		mV
Thermal Shutdown Threshold(4)	$T_{SHUTDWN}$	T_J Rising		145		℃
Hysteresis(4)		T_J Falling		10		
High-Level Input Voltage	V_{IH}		1.2			V
Low-Level Input Voltage	V_{IL}				0.4	V
Input Bias Current	I_{IN}	Input Tied to GND or V_{IN}		0.01	1.00	μA
STAT Output Low	$V_{STAT(OL)}$	I_{STAT}=10mA			0.4	V
STAT High Leakage Current	$I_{STAT(OH)}$	V_{STAT}=5V			1	μA
Q3 On Resistance (VBUS to PMID)	$R_{DS(ON)}$	$I_{IN(LIMIT)}$=500mA		42		mΩ
Q1 On Resistance (PMID to SW)				35		
Q2 On Resistance (SW to GND)				35		
Maximum Duty Cycle (charge)	D_{MAX}				98.5	%
Minimum Duty Cycle (charge)	D_{MIN}			0		%
Boost Output Voltage at VBUS	V_{BOOST}	3.0V<V_{BAT}<4.5V;	4.8	5.15	5.3	V
Boost Mode Quiescent Current	$I_{BAT(BST)}$	PFM Mode, V_{BAT}=3.6V, I_{OUT}=0		1		mA
Current Limit (Q1)	$I_{LIM(BST)}$	Peak Limit		1.3		A
Current Limit (Q4)	$I_{LIM(BAT)}$	REGA0[6:5]=00: Rlim=4K		2.24		A
		REGA0[6:5]=01: Rlim=2K		4.23		
		REGA0[6:5]=10: Rlim=1.33K		6.09		
		REGA0[6:5]=11: Rlim=1K		7.85		
	T_{ocp_flt}	Deglitch time for OCP		1		ms
Min Battery Voltage for Boost	$UVLO_{BST}$			2.9		V
12H timer	t_{12H}	Charger Enabled		12		hour
90-Minute Timer	T_{90MIN}	90-Minute Mode		90		min
90-Second Timer	T_{90s}	90-second Mode		90		Sec

Notes: 4: Guaranteed by design; not tested in production.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
JEITA Thermistor Comparator (BUCK MODE)						
Cold (0°C) threshold	T1	As Percentage to REGN		73.30		%
Falling				71.50		
Cool (10°C) threshold,	T2			68.00		
Falling				66.80		
Warm (45°C) threshold,	T3			44.70		
Falling				45.70		
Hot (60°C) threshold,	T5			34.20		
Falling				35.30		
Timing for QONB (external Key)						
QONB time to full system reset; BATFET switch on-off-on	Tqon_rst2	–10℃ ≤ TJ ≤ 60℃		20		s
BATFET's off time during full system reset	Tqon_off			430		ms
QONB low time to exit ship mode	Tship_exit			430		ms

5.5 I2C Timing Specifications

Guaranteed by design.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
SCL Clock Frequency	f_{SCL}	Standard Mode			100	kHz
		Fast Mode			400	
Bus-Free Time between STOP and START Conditions	t_{BUF}	Standard Mode		4.7		µs
		Fast Mode		1.3		

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
START or Repeated START Hold Time	$t_{HD;STA}$	Standard Mode		4		µs
		Fast Mode		600		ns
SCL LOW Period	t_{LOW}	Standard Mode		4.7		µs
		Fast Mode		1.3		
SCL HIGH Period	t_{HIGH}	Standard Mode		4		µs
		Fast Mode		600		ns
Repeated START Setup Time	$t_{SU;STA}$	Standard Mode		4.7		µs
		Fast Mode		600		ns
Data Setup Time	$t_{SU;DAT}$	Standard Mode		250		ns
		Fast Mode		100		
Data Hold Time	$t_{HD;DAT}$	Standard Mode	0		3.45	µs
		Fast Mode	0		900	ns
SCL Rise Time	t_{RCL}	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	
SCL Fall Time	t_{FCL}	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	
SDA Rise Time Rise Time of SCL after a Repeated START Condition and after ACK Bit	t_{RDA} t_{RCL1}	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
SDA Fall Time	t_{FDA}	Standard Mode		$20+0.1C_B$	300	ns
		Fast Mode		$20+0.1C_B$	300	
Stop Condition Setup Time	$t_{SU;STO}$	Standard Mode		4		μs
		Fast Mode		600		ns
Capacitive Load for SDA, SCL	C_B				400	pF

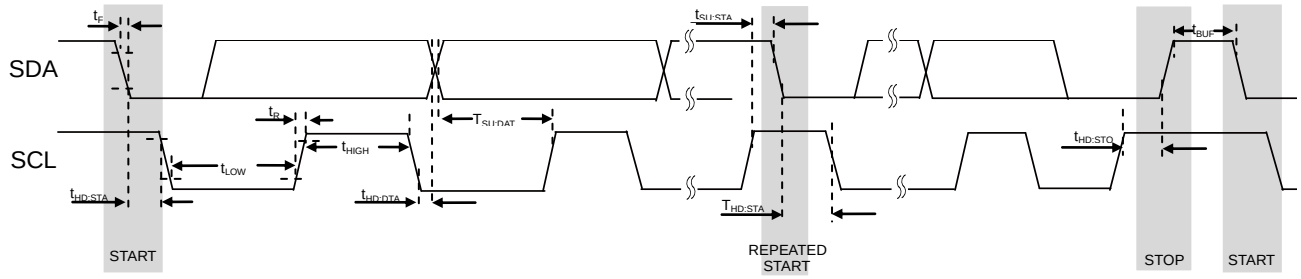


Figure 5.1: I²C Interface Timing for Fast and Slow Modes

5.6 Typical Performance Plots

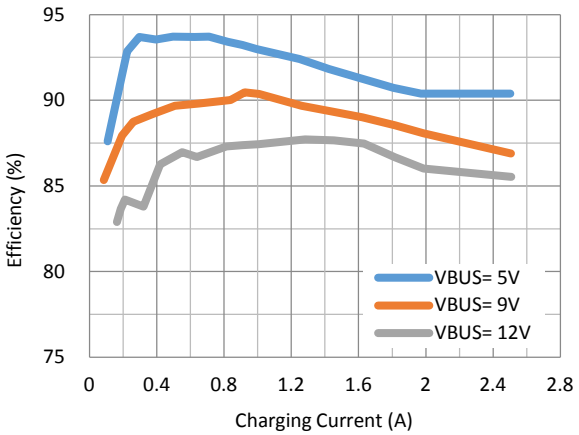


Fig1. Charge Efficiency vs. Charge Current

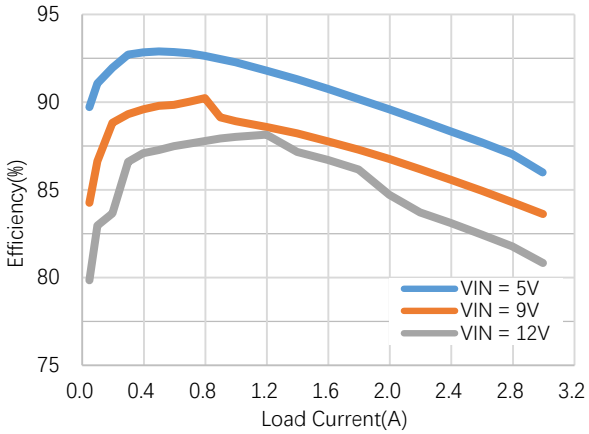


Fig2. System Efficiency vs. System Load Current

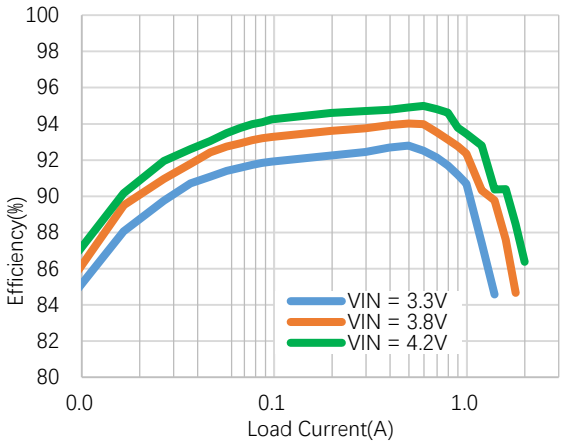


Fig3. Boost Mode Efficiency vs. VBUS Load Current

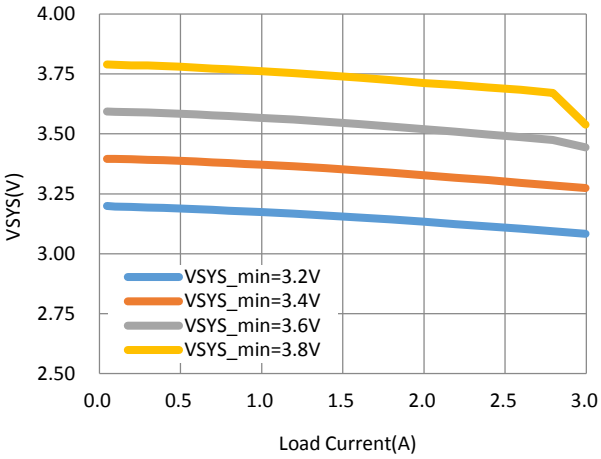


Fig4. VSYS Voltage Regulation vs. System Load Current

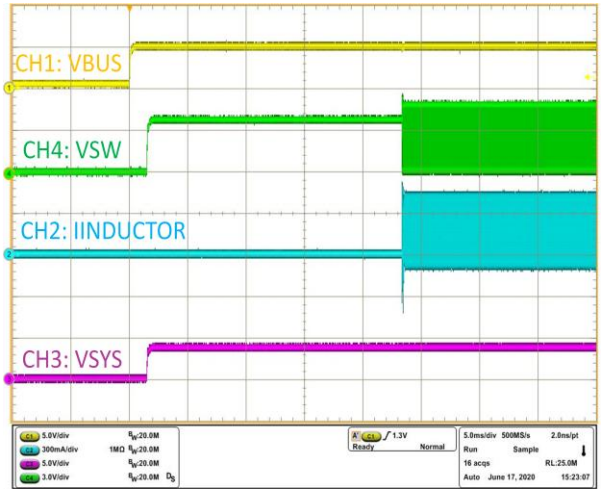


Fig5. Power Up with Charge Enabled(VBAT=3.8V)

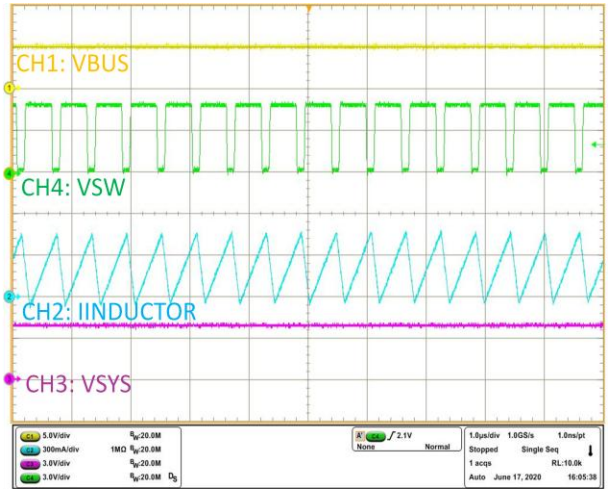


Fig6. Switching in Buck Mode
(Vbus=5V,Icharge=200mA)

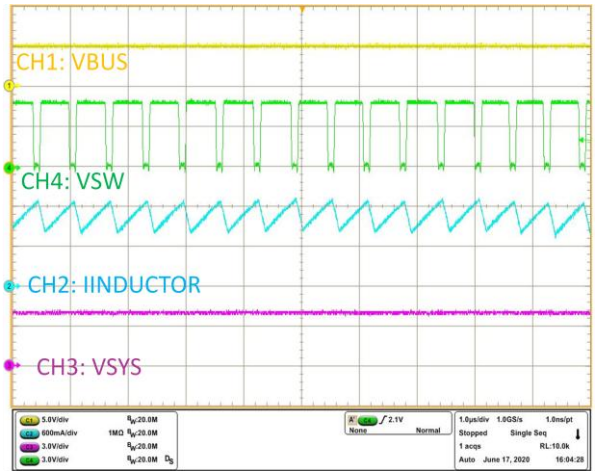


Fig7. Switching in Buck Mode
(Vbus=5V,Icharge=1A)

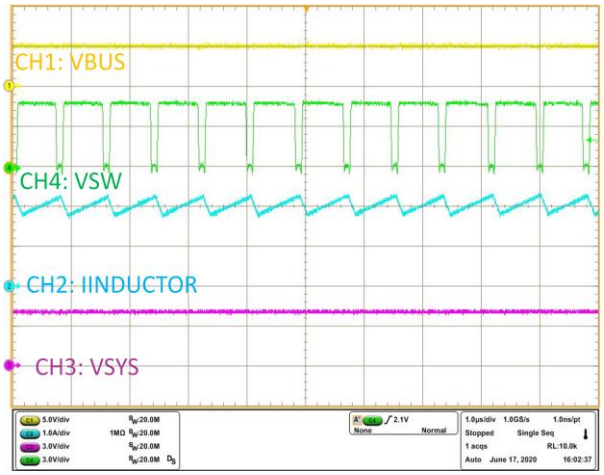


Fig8. Switching in Buck Mode
(Vbus=5V,Icharge=2A)

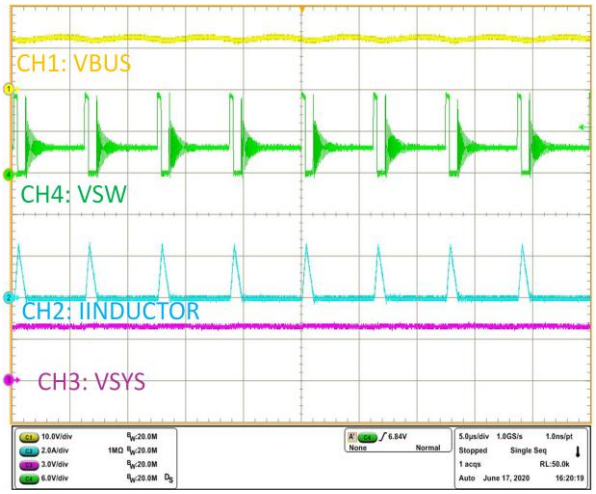


Fig9. Switching in Buck Mode
(Vbus=12V,Icharge=200mA)

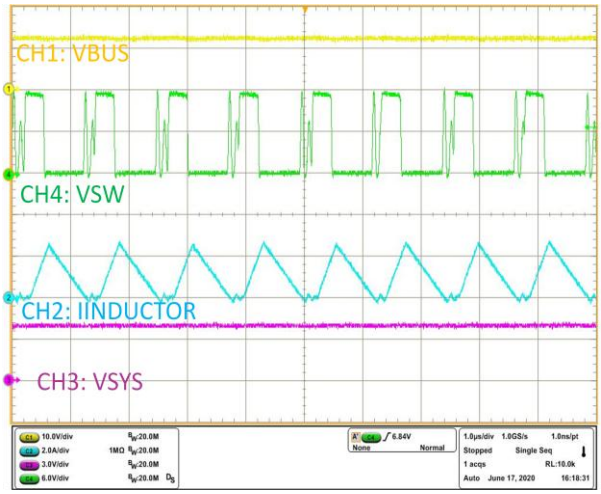


Fig10. Switching in Buck Mode
(Vbus=12V,Icharge=1A)

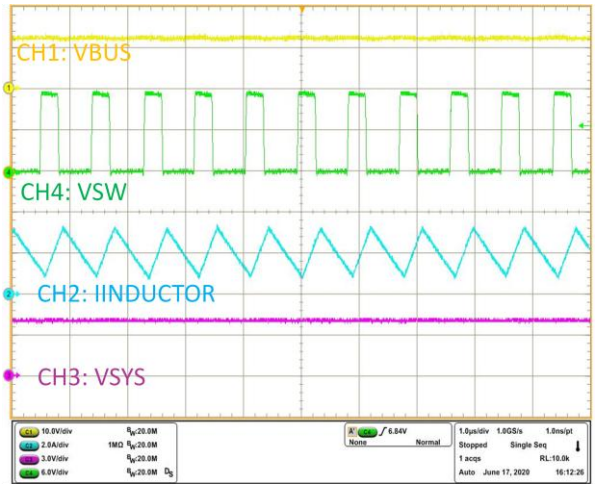


Fig11. Switching in Buck Mode
(Vbus=12V,Icharge=2A)

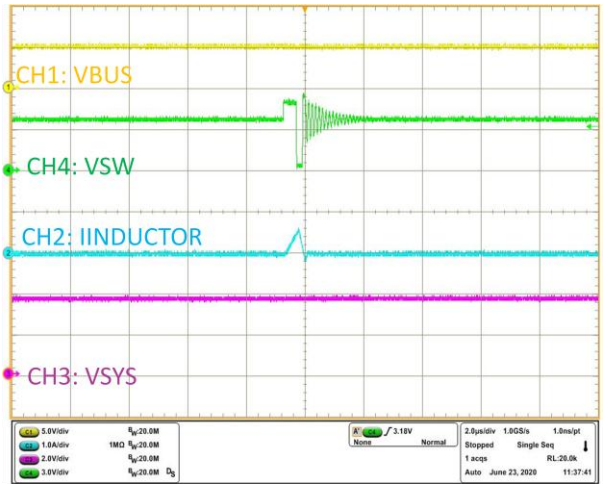


Fig12. VSYS Operation
(Vbus=5V,Vsys=3.6V,Isys=No Load)

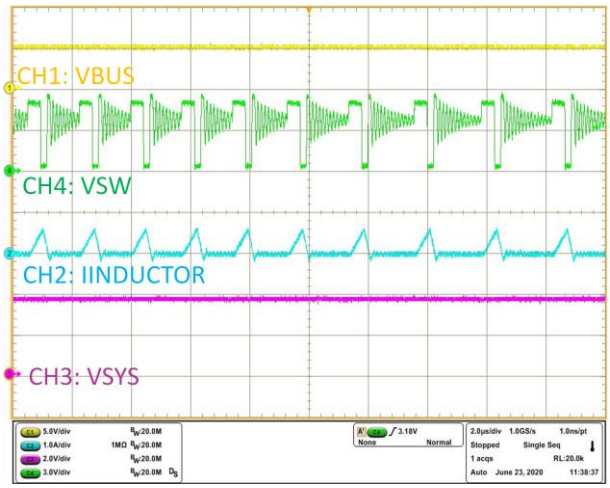


Fig13. VSYS Operation
(Vbus=5V,Vsys=3.6V,Isys=100mA)

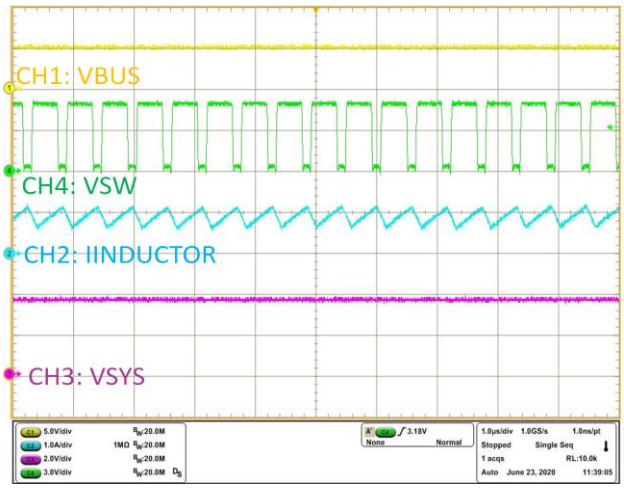


Fig14. VSYS Operation
(Vbus=5V,Vsys=3.6V,Isys=1A)

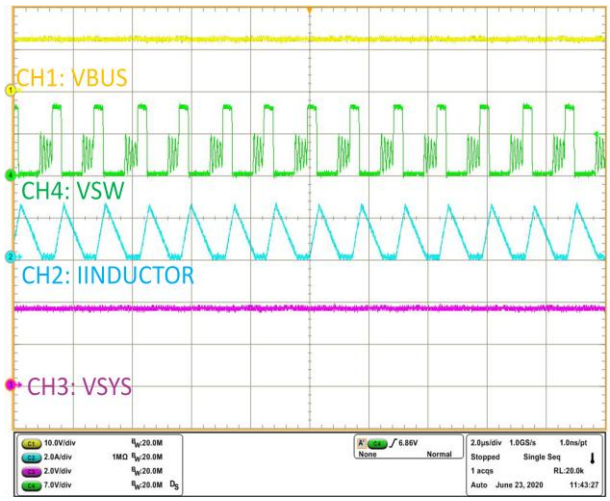


Fig15. VSYS Operation
(Vbus=12V,Vsys=3.6V,Isys=1A)

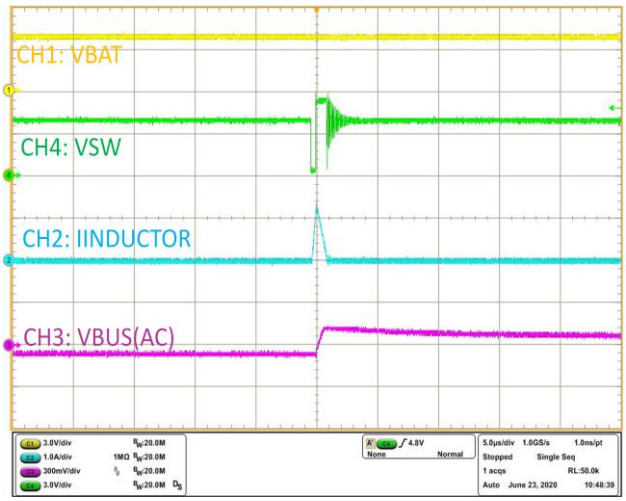


Fig16. OTG Switching
(Vbat=3.8V, No Load)

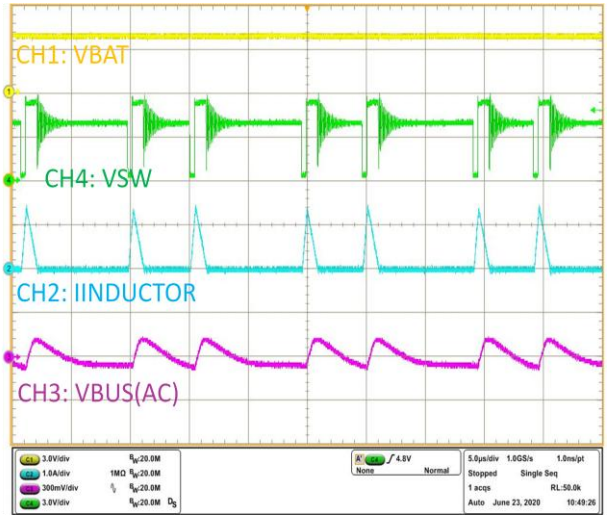


Fig17. OTG switching
(Vbat=3.8V,Iload=100mA)

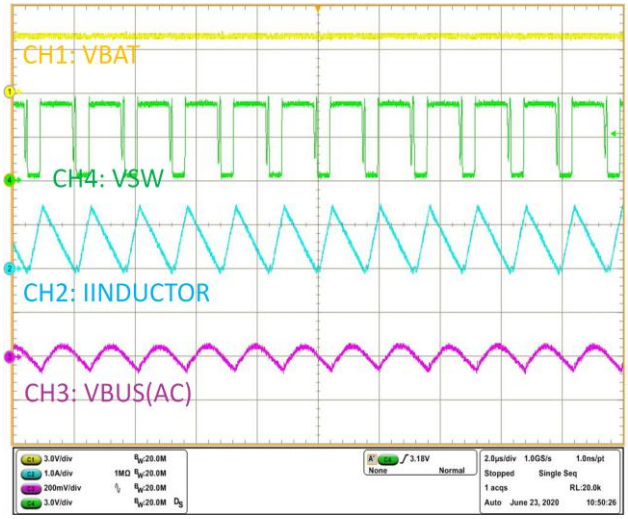


Fig18. OTG switching
(Vbat=3.8V,Iload=500mA)

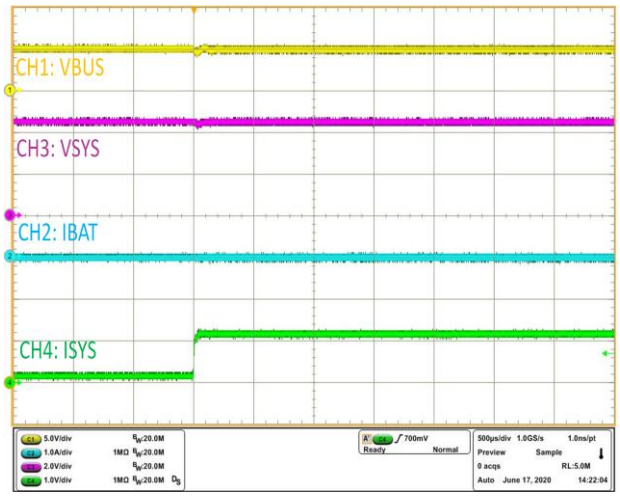


Fig19. System Load Transient
(Input is not over load, ISYS is only supported from BUS)

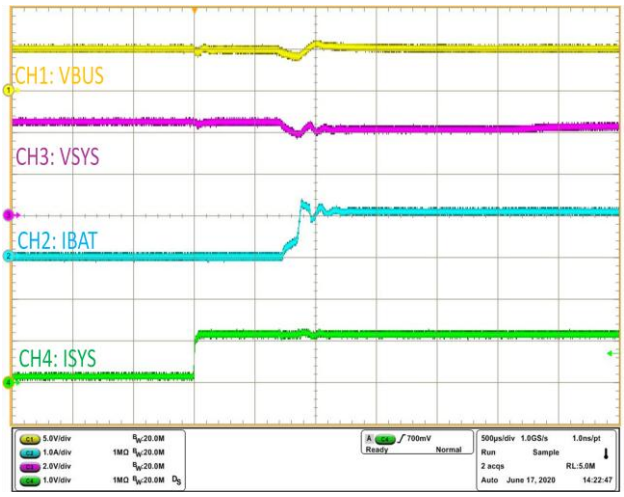


Fig20. System Load Transient
(Input is over load, ISYS is supported from both BUS and BAT)

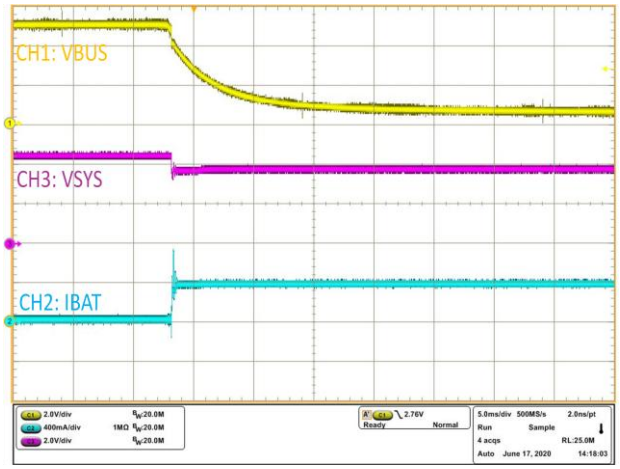


Fig21. System Load Transient
(Q4 turn on, ISYS supported from BAT after BUS input remove)

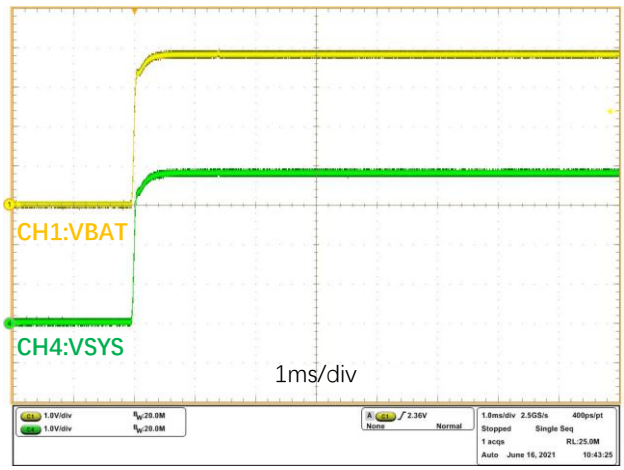


Fig22. System Start up from Battery
(No Load, VBUS Float)

6. Detailed Description

6.1 Circuit Overview

The PSC2945 is an I2C controlled power path management device and a single cell Li-Ion battery charger. It integrates the input reverse-blocking FET (RBFET, Q3), high-side switching FET (HSFET, Q1), low-side switching FET (LSFET, Q2), and battery FET (BATFET, Q4) between system and battery. The device also integrates the bootstrap diode for the high-side gate drive.

6.2 Function Block Diagram

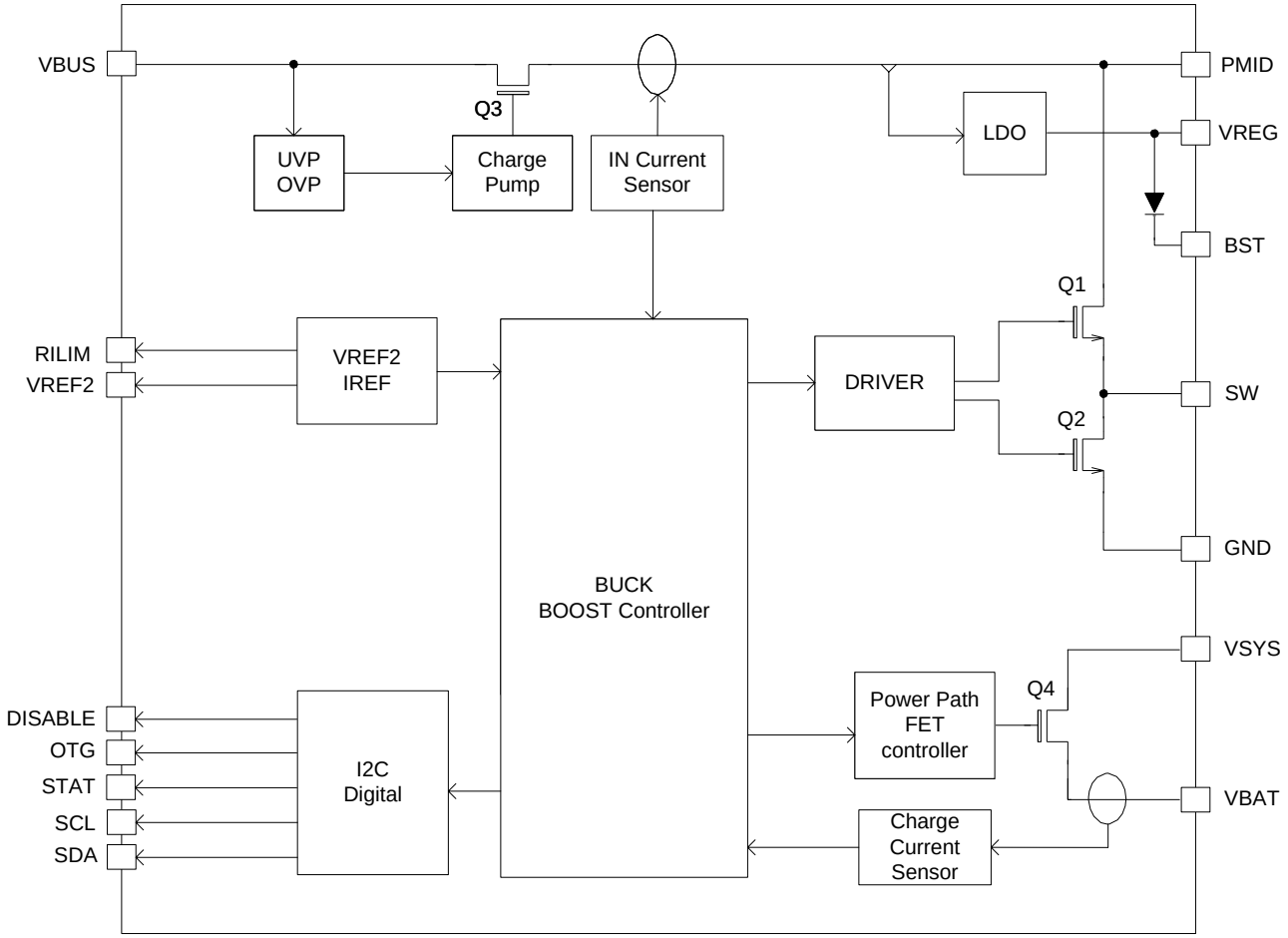


Figure 6. 1: Block Diagram

6.3 Feature description

6.3.1 Power Up from Battery without DC Source

When VBAT is powered up, the BATFET turns on and connects battery to system. The low RDSON in BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time..

6.3.2 BATFET Turn Off

If there is valid VBUS, BATFET turns off only in any of below conditions:

1) VBAT is fully charged;
2) VBAT is below VSHORT;
3) Setting REG02[3](QOFF) from “0” to “1” (only rising edge is effective) allows the user to turn off the BATFET when the IC doesn’t work in charging mode and boost mode.
4) In charging mode and boost mode, setting REG02[3] from “0” to “1” is invalid, but the BATFET can be turned off by setting REG04[3](DISCHG) to “1” in charging mode.

6.3.3 Interrupt to Host (INTB)

In some applications, the host does not always monitor the charger operation. The INT pulse notifies the systems on the device operation. The following events will generate 5-25ms INT pulse.

- USB/adapter insertion and withdrawal
- Charge complete
- Disable NTC detect
- Over voltage occur or remove
- Over current occur or remove
- BAT temperature become abnormal or return to normal.

When a fault occurs, the charger device sends out INT and keeps the fault state in REG09 until all the faults are cleared. Before all the faults are cleared, the charger device would not send any INT upon new faults.

6.3.4 Shipping Mode

6.3.3.1 enter ship mode

To extend battery life and minimize power when system is powered off during system idle, shipping, or storage, the device can turn off BATFET so that the system voltage is zero to minimize the leakage. The BATFET can be turned off by setting QOFF bit to “1”.

6.3.3.2 exit ship mode

When the BATFET is disabled (in shipping mode) and indicated by setting QOFF, one of the following events can enable BATFET to restore system power:

1. Plug in adapter
2. Set QOFF from “1” to “0” (falling edge is effective) ;
3. Reset all by write “1” to REG04[7];
4. A logic high to low transition on QONB pin with tSHIPMODE deglitch time to enable BATFET to exit shipping mode.
5. Write register to enable boost.

6.3.5 Power path management

6.3.5.1 Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by REG05[1:0]. Even with a fully depleted battery, the system is regulated above the minimum system voltage (default 3.55 V).

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is regulated at the minimum system voltage. As the battery voltage rises to Vsysmin-100mv, BATFET is fully turned on in switch mode.

When the battery is fully charged, the system is regulated at about VOREG+100mV.

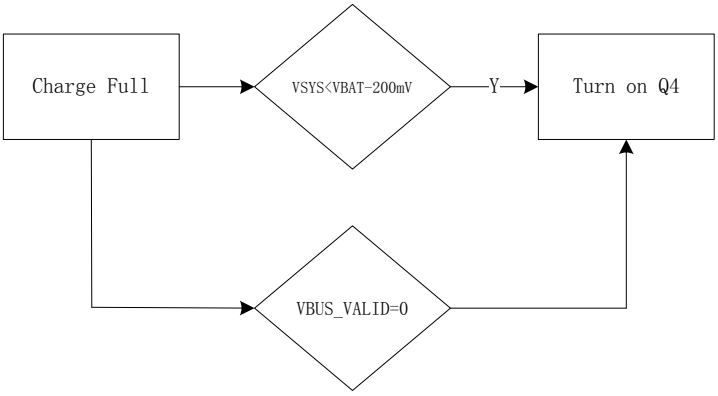
6.3.5.2 Dynamic Power Management

To meet maximum current limit in USB spec and avoid over loading the adapter, the device features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage.

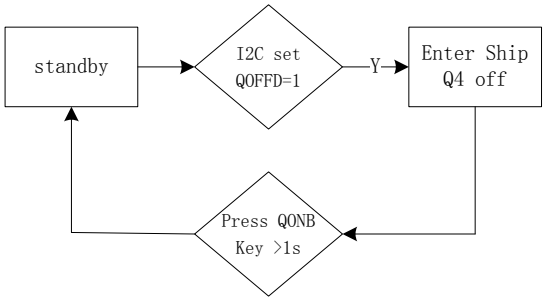
When input source is over-loaded, either the current exceeds the input current limit or the voltage falls below the input voltage limit. The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the device automatically enters the supplement mode. Battery starts discharging so that the system is supported from both the input source and battery.

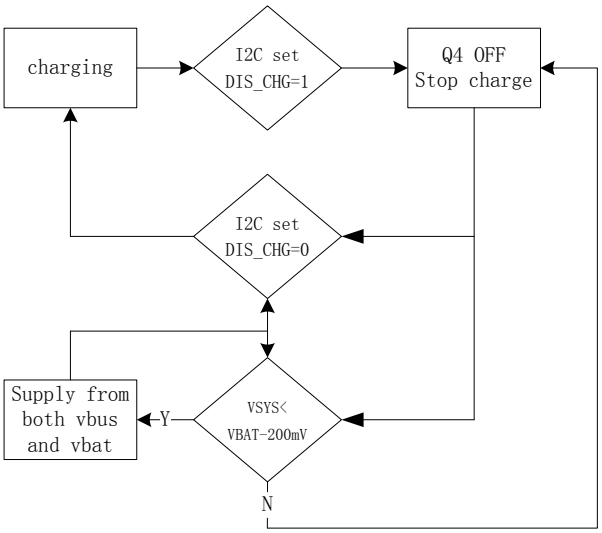
Charge done during system on



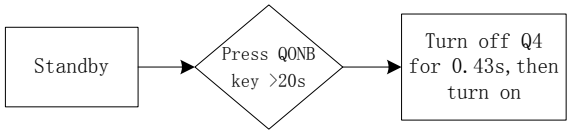
Ship mode



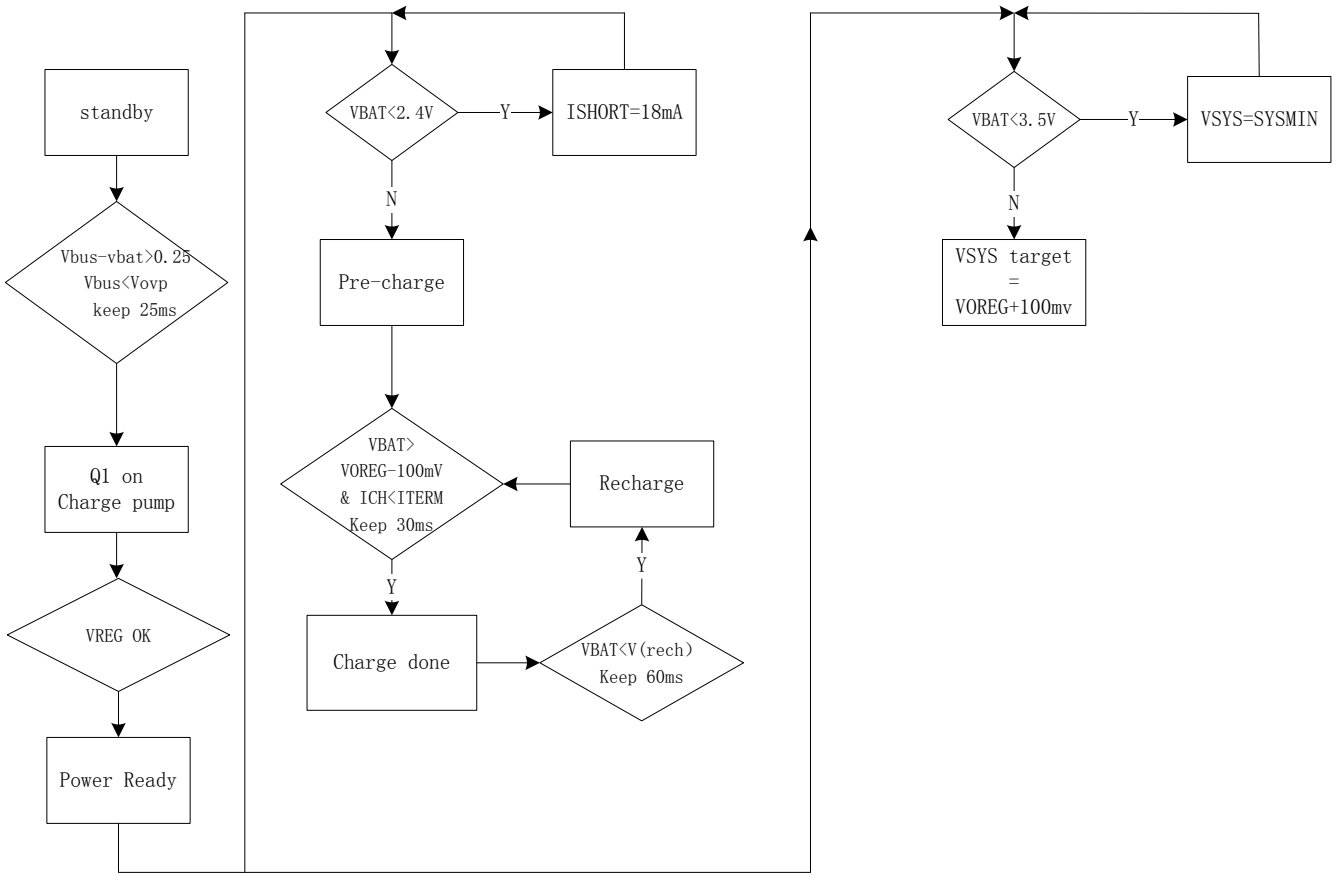
Turn off Q4 during charging



Force system reset



6.3.6 Charge Mode



6.3.6.1 Four regulation loops:

1. Charging Current: Limits the maximum charging current. This current is sensed using internal BATFET.
2. Charge Voltage: The regulator is restricted from exceeding this voltage. As the internal battery voltage rises, the battery's internal impedance and BATFET work in conjunction with the charge voltage regulation to decrease the amount of current flowing to the battery. Battery charging is completed when the current thru BATFET drops below the I_{TERM} threshold.
3. Input Current: Limits the amount of current drawn from VBUS. This current is sensed internally and can be programmed through the I^2C interface.
4. Input Voltage: PSC2945 employ an additional loop to limit the amount of drop on VBUS to a programmable voltage (V_{SP}) to accommodate "special chargers" that limit current to a lower current than might be available from a "normal" USB wall charger.

6.3.6.2 Battery Charging Curve

The device charges the battery in four phases: activating, preconditioning, constant current, Fast-CC and constant voltage.

Table 6. Charging Current Setting

VBAT	Charging Phase	Recommended Charge current	Setting Reg	Recommended Reg setting
$V_{BAT} < V_{SHORT}$ (Typical 2.4 V)	ISHORT	18mA	-	-
$V_{SHORT} \le V_{BAT} < V_{BATLOWV}$ (Typical 2.4 V ≤ V_{BAT} < 3 V)	Pre-CC	560mA	REGA0[6:5]	REGA0[6:5] = 11
$V_{BAT} \ge V_{BATLOWV}$ (Typical 3V ≤ V_{BAT} < 3.5 V)	CC	819mA	REGA0[6:5] REG04[6:5]	REGA0[6:5] = 11 REG04[6:4] =110
$V_{BAT} \ge V_{BATLOWV}$ (Typical V_{BAT} ≥ 3.5 V)	Fast-CC	2494mA	REGA0[6:5] REG90 [7:6] REG04 [6:4]	REGA0[6:5] =11 REG90 [7:6]=11 REG04 [6:4]=110

Note: If the charger device is in DPM regulation during charging, the actual charging current will be less than the programmed value.

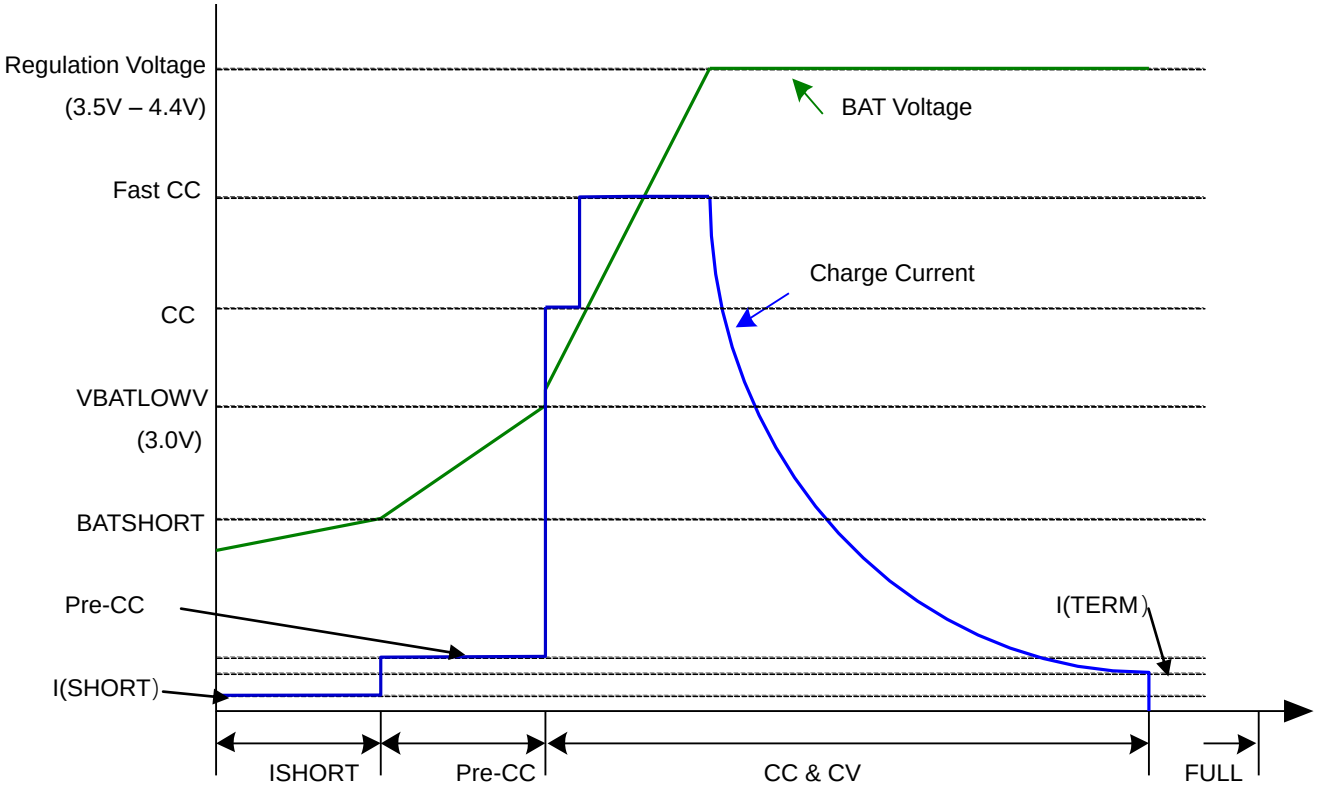


Figure 6.2: Charge Curve, I_{CHARGE} Not Limited by I_{INLIM}

6.3.6.3 Charge termination

The device terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is complete, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn back on to engage supplement mode. When termination occurs, the status register REG00[1:0] is 10. Termination can be disabled by writing 1 to REG01[3].

The host can disable charging and VSYS power through CEB pin, or set REG01[2] high.

Setting QOFF(REG02[3]) from 0 to 1 will cut VSYS from VBAT so as to disable charging, which won't impact VSYS.

6.3.6.4 Charger safety timer

The charger has a time out function for normal charge. For normal charging the timer is set to 12 hours.

If the charger is still operating after typical 12 hours, BATFET will be turned OFF and will be turned on if the condition (VOREG-VBAT) >100mV is met, or plugging out the adapter.

The 12-hour timer can be reset by plugging out/in the adapter.

6.3.6.5 Charging Status Indicator (STAT)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive LED as the application diagram shows.

--	STAT
VBUS is valid	LOW
NO valid VBUS	HIGH

6.3.6.6 Thermal Shutdown

During charge operation, the device monitors the internal junction temperature T_J to avoid overheat the chip and limits the IC surface temperature. When the internal junction temperature exceeds 140°C, the device is disabled, and is enabled if junction temperature lower than 120°C.

6.3.6.7 Input Over-Voltage Detection

When the VBUS exceeds $VBUS_{OVP}$, the IC suspends charging

When VBUS falls about 150mV below $VBUS_{OVP}$, the fault is cleared and charging resumes after VBUS is revalidated.

6.3.6.8 Battery Short Protection

If the battery voltage falls below V_{short} (2.4V typical), the device will turn off BATFET and keep 18mA linear charging current to VBAT.

6.3.6.9 Jeita

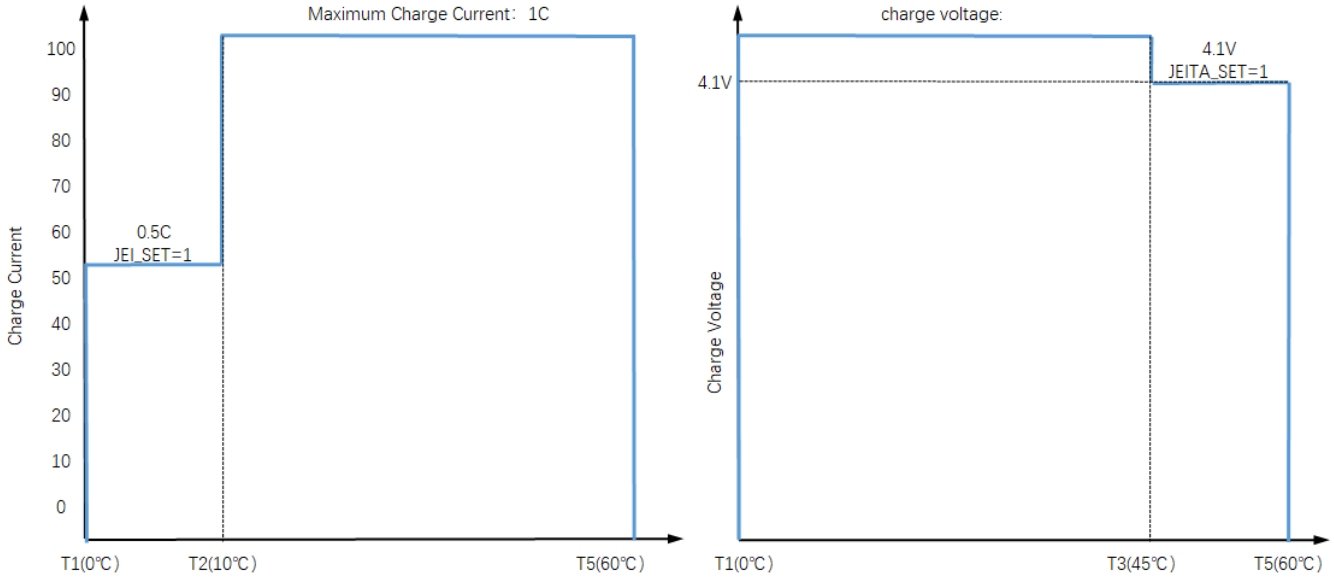
JEITA Guideline Compliance During Charging Mode

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

To initiate a charge cycle, the voltage on TS pin must be within the VT1 to VT5 thresholds. If TS voltage exceeds the T1-T5 range, the controller suspends charging and waits until the battery temperature is within the T1 to T5 range.

At cool temperature (T1-T2), JEITA recommends the charge current to be reduced to half of the charge current or lower. At warm temperature (T3-T5), JEITA recommends charge voltage less than 4.1 V.

The charger provides flexible voltage/current settings beyond the JEITA requirement. The voltage setting at warm temperature (T3-T5) can be VOREG or 4.1V (configured by JEITA_SET). The current setting at cool temperature (T1-T2) can be further reduced to 50% of fast charge current (JEITA_SET).

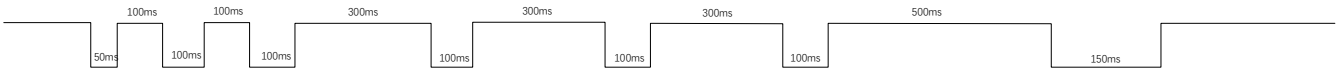


Note: 103AT as thermistor.

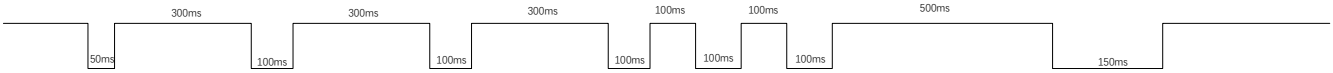
6.3.6.10 Current pulse modulation

The device includes interface to support adjustable high voltage adapter using input current pulse protocol.

Current pattern to request higher input voltage.



Current pattern to request lower input voltage;



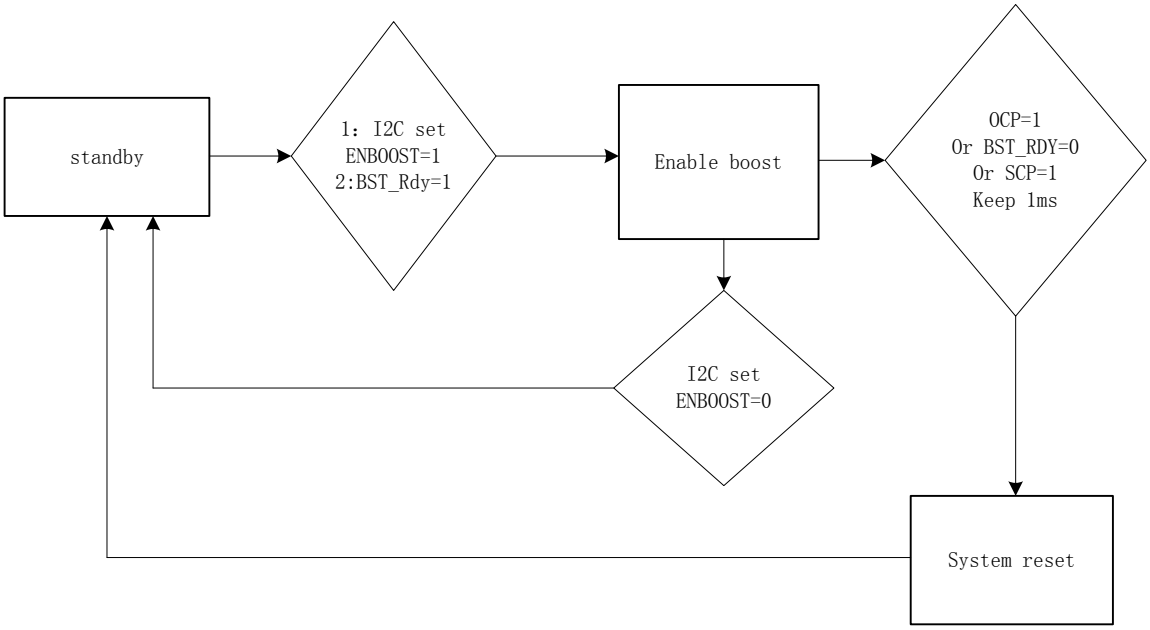
Current pulse can be programmed directly by control **DIS_PWM(REGA0[7])**.

6.3.7 Charger Parameters Description

Assuming that V_{OREG} is programmed to the cell's fully charged "float" voltage, the current that the battery accepts with the PWM regulator limiting its output (sensed at VBAT) to V_{OREG} declines, and the charger enters the voltage regulation phase of charging. When the current declines to the programmed I_{TERM} value, the charge cycle is complete. Charge current termination can be disabled by setting the TE bit (REG1[3]).
The charger output or "float" voltage can be programmed by the OREG bits from 3.6V to 4.45V as shown in REG02[6:4].

6.3.8 BOOST mode

Boost Mode can be enabled by setting ENBOOST=1 through I2C. If there is valid VBUS, boost converter will be suspended.



6.3.8.1 Startup

When the boost regulator is shut down, current flow is prevented from V_{BAT} to V_{BUS}, as well as reverse flow from V_{BUS} to V_{BAT}.

6.3.8.2 Soft Start

This IC has built-in soft start function to prevent the IC being out of control. The reference voltage is slightly raised to the normal voltage within about 100us.

6.3.8.3 BST State

This is the normal operating mode of the regulator. The regulator uses a cot modulation scheme. The minimum t_{OFF} is proportional to $\frac{V_{IN}}{V_{OUT}}$ Which keeps the regulator's switching frequency reasonably constant in CCM.

To ensure the VBUS does not pump significantly above the regulation point, the boost switch remains off as long as FB > V_{REF}.

6.3.8.4 Over current protection

The device monitors the BATFET current to ensure safe boost mode operation.
If over-current condition is detected, the device will lower the output voltage first.
After about 400us, if it's still in over-current conditions, the device will reset and quit boost mode.

6.3.9 I2C Interface

The PSC2945's serial interface is compatible with Standard, Fast, Fast Plus, and High-Speed Mode I^2C-Bus® specifications. The PSC2945's SCL line is an input and its SDA line is a bi-directional open-drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

Slave Address

Table 19. I^2C Slave Address Byte

Part Types	7	6	5	4	3	2	1	0
PSC2945	1	1	0	1	0	1	0	R/ $\overline{W}$

In hex notation, the slave address assumes a 0 LSB. The hex slave address for the PSC2945 is D4H.

Bus Timing

As shown in Figure 6.3, data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.

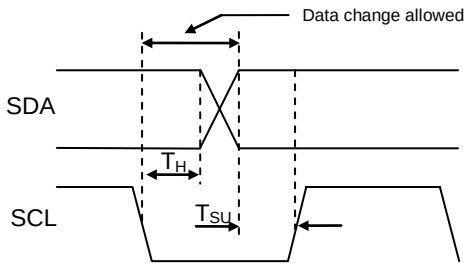


Figure 6.3: Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 6.4.

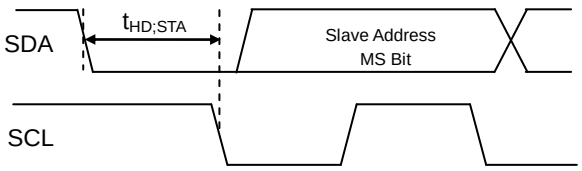


Figure 6.4: Start Bit

A transaction ends with a STOP condition, which is defined as SDA transitioning from 0 to 1 with SCL HIGH, as shown in Figure 6.5.

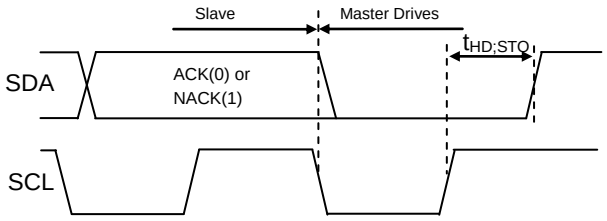


Figure 6.5: Stop Bit

During a read from the PSC2945, the master issues a Repeated Start after sending the register address and before resending the slave address. The Repeated Start is a 1-to-0 transition on SDA while SCL is HIGH, as shown in Figure 6.6.

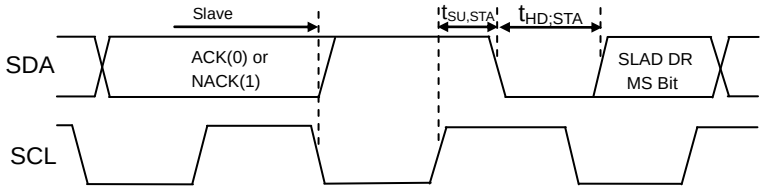


Figure 6.6: Repeated Start Timing

Read and Write Transactions

The figures below outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as Master Drives Bus and Slave Drives Bus

All addresses and data are MSB first.

Table 20. Bit Definitions for Figure 6.7, Figure 6.8

Symbol	Definition
S	START, see Figure 6.4
A	ACK. The slave drives SDA to 0 to acknowledge the preceding packet.
$\overline{A}$	NACK. The slave sends a 1 to NACK the preceding packet.
R	Repeated START, see Figure 6.6
P	STOP, see Figure 6.5

Figure 6.7: Write Transaction

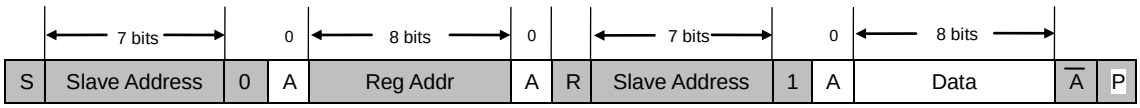


Figure 6.8: Read Transaction

Register Descriptions

Table 8. I²C Register Address

IC	Register	Address Bits							
	REG#	7	6	5	4	3	2	1	0
PSC2945	00	0	0	0	0	0	0	0	0
	01	0	0	0	0	0	0	0	1
	02	0	0	0	0	0	0	1	0
	03	0	0	0	0	0	0	1	1
	04	0	0	0	0	0	1	0	0
	05	0	0	0	0	0	1	0	1
	80	1	0	0	0	0	0	0	0
	90	1	0	0	1	0	0	0	0
	A0	1	0	1	0	0	0	0	0

Table 9. Register Bit Definitions

This table defines the operation of each register bit for all IC versions. Default values are in bold text.

Register Address:00		**Default Value=**		
7	BAT_TEMP ERR	0	R	1 indicates temperature of battery is abnormal
6	VBAT_LOW	0	R	1 indicates battery voltage is below 3.0v
5	VSHORT	0	R	1 indicates battery voltage is below 2.4V
4	VBUS_IBUS	0	R	1 indicates input current limit loop is controlling charger;
3	VBUS_VSP	0	R	Special charger is not active(vbus is able to stay above Vsp)
		1		Special charger has been detected and vbus is being regulated to Vsp.
2	ICHG	0	R	1 indicates Charger is in CC (constant current) mode;
1:0	STAT	00	R	Status: 00: standby 01: in charging progress 10: charge done; 11: in boost mode;

Register Address:01		**Default Value=0b 0010 0000**		
7-5	IINLIM	001	R/W	Iput current limit： 420mA(000) /**1.2A(001)** /370mA(010) /760mA(011)/ 950mA(100) /2.1A(101) /2.5A(110) /1.7A(111） Note：DIS_DCP=0: the current limit set as 1.7A(111) at DCP=1, and set as 420mA(000) at DCP=0: DIS_DCP=1(disable DCP detect)，IINLIMIT=1.2A(default);
4	DIS_DCP	0	R/W	1: disable DCP detection, input current limit is only set by IINLIM;
3	TEB	0	R/W	0：Enable charge current termination;
2:1	-	-	-	Reserve
0	ENBOOST	0	R/W	Disable boost
		1		Enable boost
Register Address:02		**Default Value= 0b 0000 0000**		
7	SUB20MV	0	R/W	1: Charge voltage is decreased by 20mV;
6-4	VOREG	000	R/W	Charge voltage setting： **4.20V（000）**/4.35V(001)/4.40V(010)/4.10V(011)/ 3.60V(100)/ 4.45V(101~111)
3	QOFF	0	R/W	“0” to “1” transition will turn off Q4; “1” to “0” transition will turn on Q4,(See 6.3.2 BATFET turn off)
2	DIS_THM	0	R/W	Temperature of battery is normally detected, charge parameters will be programmed according JEITA profile.
		1		Temperature of battery is not detected.
1	DIS_90S	0	R/W	1:disable 90-second timer ;
0	JEITA_SET	0	R/W	Charge parameters are not changed if battery is in “warm” or “cool” status.
		1		Charge voltage is changed to 4.1V if battery is “warm”; Charge current is reduced by half if battery is “cool”

Register Address:03		**Default Value= 0b 1111 1xxx**		
7-4	Vendor	1111	R	Vendor code; 1111 indicates Prisemi.
3:2	BC	-	R	10: SDP; 11:DCP mode; 00/01: RESERVED
1:0	DP/DM	00	R	DP/DM Output Voltage Level (H or L)
Register Address:04		**Default Value=0b 0100 0001**		
7	RESET	0	R/W	Read return “0”, write “1” will reset all.
6-4	ICHG	100	R/W	See page32 for Charge current setting.
3	DIS_CHG	0	R/W	DIS_CHG is valid when VBUS is powered on. 0：Enable Charger；1：Disable Charging by turning off Q4.
2-0	ITERM	001	R/W	See page32 for Termination current setting.
Register Address:05		**Default Value= 0b 0100 0010**		
7	ADD20MV	0	R/W	1: Charge voltage is increased by 20mV;
6:4	VSP	100	R/W	Input voltage limit setting: 4.35V（000）/4.40V(001)/4.45V(010)/4.50V(011)/ **4.57V(100)**/4.65V(101)/8.5V(110)/11.5V(111)
3-2	OVP_SEL	00	R/W	Input over-voltage setting: 13.9V(00)/11.1(01)/6.9V(10)/disable OVP(11)
1-0	SYSMIN	10	R/W	Minimum system regulation voltage if vbus is valid; 3.15V(00)/3.35V(01)/**3.55V(10)**/3.75V(11)
Register Address:80		**Default Value= 0b0000 0000**		
7	VBUS_UVP	0	R	1：indicates input voltage is under-voltage;
6	VBUS_OVP	0	R	1：indicates input voltage is over-voltage;
2-0	BAT_TEMP	000	R	Indicates status of battery’s temperature: 100：cold；101：cool；110：warm；111：hot；
Register Address:90		**Default Value= 0b 0000 0000**		
7:6	Ratio	0	R/W	Current Setting Ratio
5	VDN	0	R/W	PEP Protocol, rising edge trigger, send Step-down instruction
4	VUP	0	R/W	PEP Protocol, rising edge trigger, send Step-up instruction
3	EN_FD	0	R/W	0:Disable OCP, turn off Q4 in battery discharge mode. 1: Enable OCP (2A-6A programmable)
2:0	-	-	-	Reserve

Register Address:A0		Default Value= 0b 0000 0000		
7	DIS_PWM	0	R/W	Used to send current modulation by system; 0：Enable PWM;　1：Disable PWM
6:5	RES_SEL	00	R/W	Choose resistance to set the charge current; 00：4K, 01: 2K, 10: 1.33K, 11: 1K
4:0	-	-	-	Reserve

Charging Current Setting

RegA0 [6:5]	Reg90 [7:6]	Icharge (mA)							
		reg04[6:4]							
		0	1	10	11	100	101	110	111
[11] 1k	[00]	433	476	520	563	606	650	693	736
	[11]	1559	1715	1871	2027	2183	2339	2494	2650
[10] 1.33k	[00]	326	358	391	423	456	488	521	553
	[11]	1172	1289	1407	1524	1641	1758	1875	1993
[01] 2k	[00]	217	238	260	281	303	325	346	368
	[11]	780	857	935	1013	1091	1169	1247	1325
[00] 4k	[00]	108	119	130	141	152	162	173	184
	[11]	390	429	468	507	546	585	624	663

Terminate Current Setting

Reg90 [7:6]	Iterm reg04[2:0], (mA)							
	0	1	10	11	100	101	110	111
[00]	33	47	62	76	90	104	119	134
[11]	60	120	180	240	290	350	410	470

7. PCB Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see Figure 7.1) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Place input capacitor as close as possible to PMID pin and GND pin connections and use shortest copper trace connection or GND plane.
2. Place inductor input pin to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
3. Put output capacitor near to the inductor and the IC. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using thermal pad as the single ground connection point. Or using a 0Ω resistor to tie analog ground to power ground.
5. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the IC. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.
6. Decoupling capacitors should be placed next to the IC pins and make trace connection as short as possible.
7. It is critical that the exposed thermal pad on the backside of the IC package be soldered to the PCB ground.

Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.

8. The via size and number should be enough for a given current path.

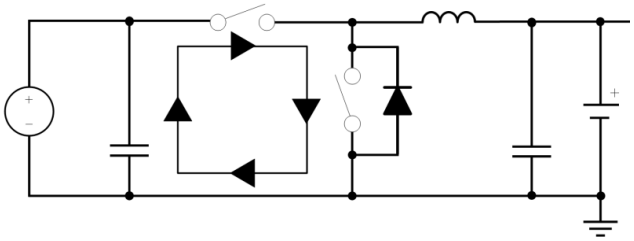
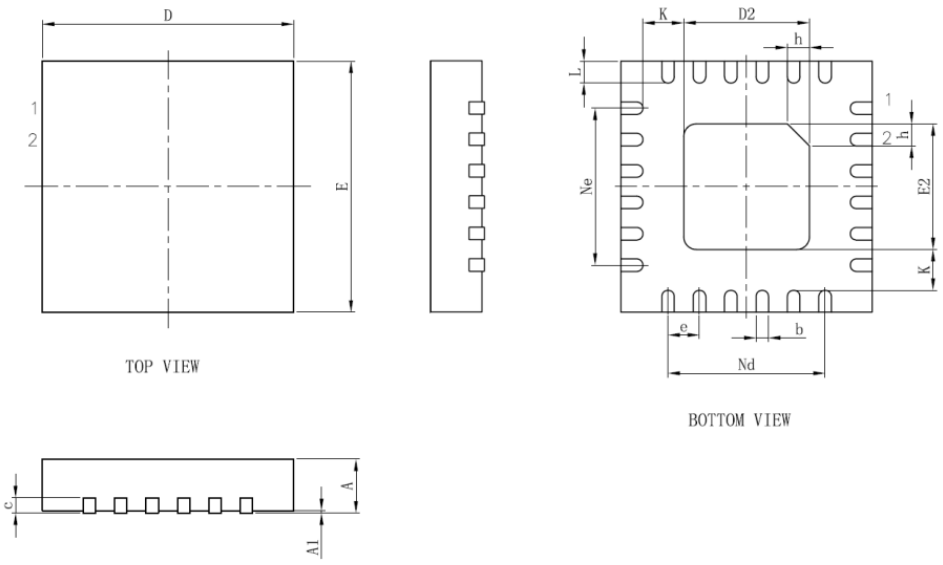


Figure 7.1: high frequency current path

8. Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	1.90	2.00	2.10
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	1.90	2.00	2.10
L	0.30	0.40	0.50
K	0.20	—	—
h	0.30	0.35	0.40

Ordering Information

Device	Package	Reel	Shipping
PSC2945	QFN4x4-24L (Pb-Free)	7"	3000 / Tape & Reel

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