PAW3370DM-T4QU: Low Power Optical Gaming Navigation Chip

General Description

PAW3370DM-T4QU is PixArt Imaging's new low power gaming navigation chip suitable for wired and wireless gaming application. It has the latest state-of-the-art low-power architecture and automatic power management modes, making it ideal for battery-operated, power-sensitive cordless gaming devices. It provides excellent gaming experience with the features of high speed and high resolution even in low power mode to fulfill gamers' need. It is packaged in 16pin staggered dual-in-line package (DIP) and designed to be used with LM19-LSI or L0AE-LSI1 lens to achieve optimum performance.

Key Features

- Low power consumption of typical 1.5mA @ run mode
- Programmable rest modes
- 16 pin molded lead-frame DIP package with 850nm illumination source
- High speed motion detection 400ips* and acceleration 50g*
- Selectable resolutions up to 19,000cpi
  - 50cpi step size from 50cpi to 10,000cpi
  - 100cpi step size from 10,100cpi to 19,000cpi
- Four-wire serial port interface (SPI)
- Internal oscillator — no clock input needed
- Customizable response time and downshift time for rest modes
- Angle snapping
- Lift detection options
  - 1mm setting
  - 2mm setting
  - Manual Lift Cut Off Calibration

Applications

- Wired and wireless Gaming Optical Mouse
- Trackball application

Key Parameters

Parameter	Value
Power Supply Voltage	VDD: 1.8 – 2.1V VDDIO: 1.8 – 3.3V
Interface	4-wire Serial SPI
Supply Current @ VDD & VDDIO = 1.9V *Note: includes LED current*	Low Power Gaming Mode 1 ▪ Run: 1.5 mA ▪ Power Down: 3 µA
Resolution (cpi)	Up to 19000
Tracking Speed (ips)	400*
Acceleration (g)	50*
Package Size (mm)	10.90 x 16.20 x 5.01

Note: * - Low Power Gaming Mode 1

Ordering Information

Part Number	Package Type
PAW3370DM-T4QU	16pin-DIP Optical Gaming Navigation Chip
LM19-LSI	Round Lens
L0AE-LSI1	Trim Lens

RoHS compliant

For any additional inquiries, please contact us at https://www.pixart.com

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1.0 Introduction

1.1 Overview

The PAW3370DM is an optical navigation chip targeted for high-end corded gaming mouse. It contains an image array as Image Acquisition System (IAS), a Digital Signal Processor (DSP), a four wire serial port, a power control circuit and built-in LED driver integrated with Illumination source in a package as shown in the block diagram. The chip measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement. The IAS acquires microscopic surface images via the lens and illumination system. These images are processed by the DSP to determine the direction and distance of motion. The DSP calculates the Δx and Δy relative displacement values. An external microcontroller reads the Δx and Δy information from the chip serial port. The microcontroller then translates the data into USB, or RF signals before sending them to the host PC or game console.

Note: Throughout this document PAW3370DM-T4QU is referred to as the chip.

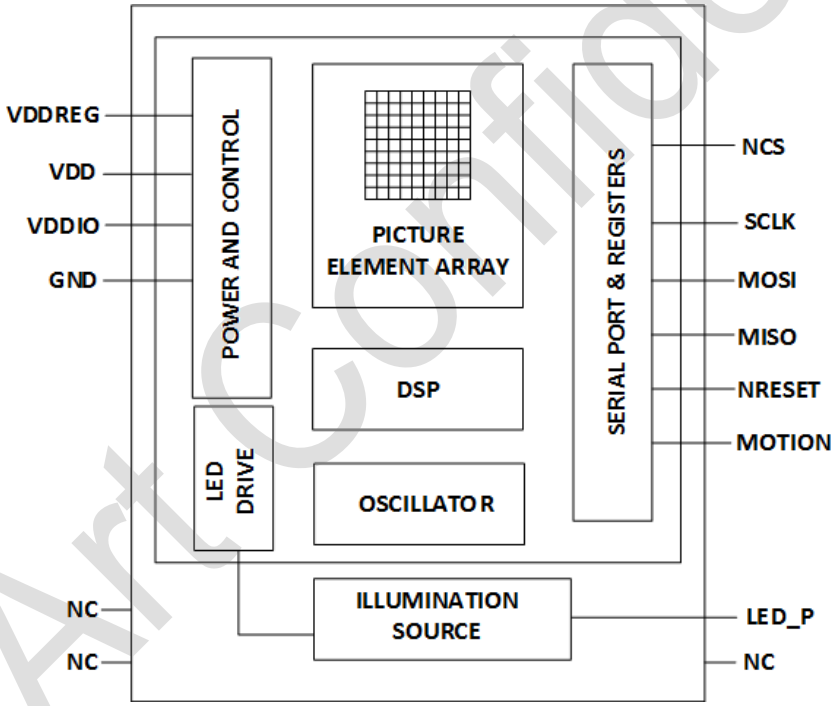


Figure 1. Functional Block Diagram

1.2 Terminology

Term	Description
DSP	Digital Signal Processing
LED	Light Emitting Diode
NCS	Chip Select
VDDREG	LDO output (only for sensor internal usage)
VDD	Supply voltage
VDDIO	I/O power supply
SCLK	Serial Clock
MOSI	Serial Data Input
MISO	Serial Data Output
NRESET	Chip reset
SPI	Serial Peripheral Interface
GND	Ground
MOTION	Motion Detect

1.3 Pin Configuration

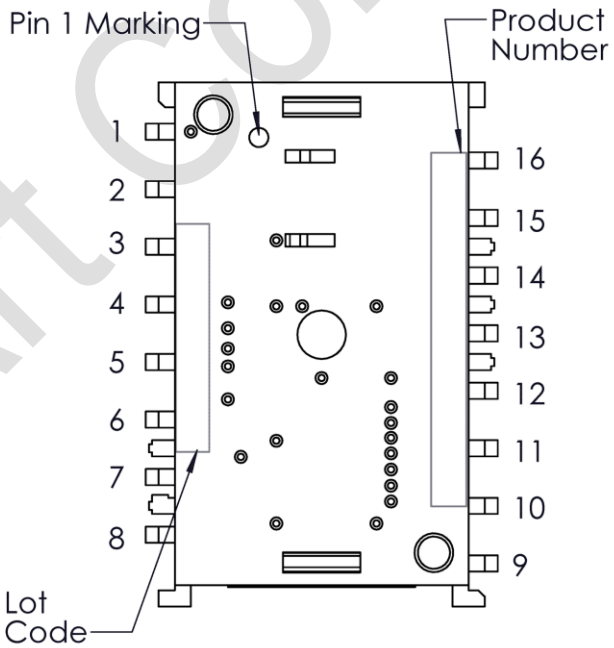


Figure 2. Device Pinout

Table 1. Pins Description

Pin No.	Function	Symbol	Type	Description
1	Reserved	NC	NC	No connection
2	Reserved	NC	NC	No connection
3	Supply Voltage and I/O Voltage	VDDREG	Power	LDO output (only for sensor internal usage)
4		VDD	Power	Power supply
5		VDDIO	Power	I/O power supply
6	Reserved	NC	NC	No Connection
7	Reset Control	NRESET	Input	Chip reset (Active Low)
8	Ground	GND	GND	Ground
9	Motion Output	MOTION	Output	Motion detect
10	4-wire SPI	SCLK	Input	Serial data clock
11		MOSI	Input	Serial data input
12		MISO	Output	Serial data output
13		NCS	Input	Chip select (Active Low)
14	Reserved	NC	NC	No connection
15	LED	LED_P	Input	LED Anode
16	Reserved	NC	NC	No connection

2.0 Operating Specifications

2.1 Regulatory Requirements

- Passes FCC "Part15 Subpart, Class B", "ICES-003:2016 Issue 6, Class B" and "ANSI C63.4:2014" when assembled into a mouse with shielded USB cable using ferrite bead and following PixArt's recommendations.
- Passes IEC 62471:2006 Photo biological safety of lamps and lamp systems.

2.2 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T_S	-40	85	°C	
Lead Solder Temperature	T_{SOLDER}		260	°C	For 7 seconds, 1.6mm below seating
Supply Voltage	V_{DD}	-0.5	2.10	V	
	V_{DDIO}	-0.5	3.30	V	
ESD	ESD_{HBM}		2	kV	Human Body Model on All pins
Input Voltage	V_{IN}	-0.5	V_{DDIO}	V	All I/O pins.

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are the stress ratings only and functional operation of the device at these or any other condition beyond those indicated for extended period of time may affect device reliability.
2. The inherent design of this component causes it to be sensitive to electrostatic discharge. The ESD threshold is listed above . To prevent ESD induced damage, take adequate ESD precautions when handling this product

2.3 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating Temperature	T_A	0		40	°C	
Power Supply Voltage	V_{DD}	1.8	1.9	2.1	V	Including 100mVp-p supply noise
	V_{DDIO}	1.8	1.9	3.3	V	Including 100mVp-p supply noise (V_{DDIO} must be same or greater than V_{DD})
Power Supply Rise Time	t_{RT}	0.15		20	ms	0 to VDD & VDDIO
Supply Noise	V_{NA}			100	mV_{p-p}	10kHz – 75MHz
Serial Port Clock Frequency	f_{SCLK}			8	MHz	Active drive, 50% duty cycle
Distance from Lens Reference Plane to Tracking Surface	Z	2.20	2.40	2.60	mm	
Speed Low Power Gaming Mode 1 Low Power Gaming Mode 2 Corded Gaming Mode Office Mode	S	 400 200 400 30			ips	Tested on QCK at 45 degree
Acceleration Low Power Gaming Mode 1 Low Power Gaming Mode 2 Corded Gaming Mode Office Mode	A	 50 40 50 10			g	In run mode Tested on QCK at 45 degree
Load Capacitance	C_L			20	pF	MISO, MOTION
Lift Cutoff 1mm setting	$Lift_{1mm}$		1		mm	LM19-LSI & l0AE-LSI1
Lift Cutoff 2mm setting	$Lift_{2mm}$		2		mm	LM19-LSI & l0AE-LSI1
Lift Cutoff (Manual Calibration)	$Lift_{CAL}$		1		mm	LM19-LSI & l0AE-LSI1
Resolution Error	Res_{Err}		0.5		%	In Low Power Gaming Mode 1 Up to 200ips at 3000cpi on QCK

Note: PixArt does not guarantee the chip performance if the operating temperature is beyond the specified limit.

2.4 Thermal Specifications

Table 4. Thermal Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	T_S	-25	-	80	°C	
Lead-free Solder Temperature	T_P	-	-	260	°C	For 10 seconds, 1.6mm below seating plane for wave soldering

2.5 DC Characteristics

Table 5. DC Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
DC Supply Current (Run mode)						Average Run current on QCK Includes I_{LED}
Low Power Gaming Mode 1	$I_{DD\_RUN\ [LPGM1\ mode]}$		1.5		mA	Measured at 1ms polling rate
Low Power Gaming Mode 2	$I_{DD\_RUN\ [LPGM2\ mode]}$		1.2		mA	Measured at 8ms polling rate
Corded Gaming Mode	$I_{DD\_RUN\ [Corded\ mode]}$		3.0		mA	Measured at 1ms polling rate
Office Mode	$I_{DD\_RUN\ [Office\ mode]}$		0.5		mA	Measured at 8ms polling rate
DC Supply Current (Rest mode)						Average Rest current
Low Power Gaming Mode 1 & Corded Gaming Mode	$I_{DD\_REST1\ (LPGM1\ mode)}$		610		uA	Includes I_{LED}
	$I_{DD\_REST2\ (LPGM1\ mode)}$		25		uA	
	$I_{DD\_REST3\ (LPGM1\ mode)}$		5		uA	
Low Power Gaming Mode 2	$I_{DD\_REST1\ (LPGM2\ mode)}$		160		uA	
	$I_{DD\_REST2\ (LPGM2\ mode)}$		25		uA	
	$I_{DD\_REST3\ (LPGM2\ mode)}$		5		uA	
Office Mode	$I_{DD\_REST1\ (Office\ mode)}$		75		uA	
	$I_{DD\_REST2\ (Office\ mode)}$		10		uA	
	$I_{DD\_REST3\ (Office\ mode)}$		5		uA	
Power Down Current	I_{PD}		3		uA	
Input Low Voltage	V_{IL}			0.3* V_{DDIO}	V	SCLK, MOSI, NCS
Input High Voltage	V_{IH}	0.7* V_{DDIO}			V	SCLK, MOSI, NCS
Input Hysteresis	V_{I_HYS}		100		mV	SCLK, MOSI, NCS,
Input Leakage Current	I_{LEAK}		± 1	± 10	uA	Vin=V_{DDIO} or 0V, SCLK, MOSI, NCS
Output Low Voltage	V_{OL}			0.45	V	I_{OUT} = 1mA, MISO, MOTION
Output High Voltage	V_{OH}	V_{DDIO} -0.45			V	I_{OUT} = -1mA, MISO, MOTION
Input Capacitance	C_{in}		10		pF	SCLK, MOSI, NCS

Note: All the parameters are tested under recommended operating conditions. Typical values at 25 °C, V_{DD} & V_{DDIO} = 1.9 V & LED current = 24mA

2.6 AC Characteristics

Table 6. AC Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Motion Delay After Reset	$t_{MOT-RST}$	50			ms	From reset to valid motion, assuming motion is present
Shutdown	t_{STDWN}			500	ms	From Shutdown mode active to low current This timing could be affected by Rest3 period
Wake up from Shutdown	t_{WAKEUP}	50			ms	From Shutdown mode inactive to valid motion. Notes: A RESET must be asserted after a shutdown. Refer to section "5.2 Power Down Sequence", also note $t_{MOT-RST.}$
MISO Rise Time	t_{r-MISO}		6		ns	C_L = 20pF
MISO Fall Time	t_{f-MISO}		6		ns	C_L = 20pF
MISO Delay After SCLK	$t_{DLY-MISO}$			38	ns	From SCLK falling edge to MISO data valid, C_L = 20pF with 10kOhm pull up resistor.
MISO Hold Time	$t_{hold-MISO}$	31.25			ns	Data held until next falling SCLK edge
MOSI Hold Time	$t_{hold-MOSI}$	31.25			ns	Amount of time data is valid after SCLK rising edge
MOSI Setup Time	$t_{setup-MOSI}$	31.25			ns	From data valid to SCLK rising edge
SPI Time Between Write Commands	t_{SWW}	5			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second data byte.
SPI Time Between Write And Read Commands	t_{SWR}	5			µs	From rising SCLK for last bit of the 1st data byte, to rising SCLK for last bit of the second address byte
SPI Time Between Read And Subsequent Commands	t_{SRW} t_{SRR}	2			µs	From rising SCLK for last bit of the 1st data byte, to falling SCLK for the 1st bit of data being read.
SPI Read Address-Data Delay	t_{SRAD}	2			µs	From rising SCLK for last bit of the address byte, to falling SCLK for the 1st bit of data being read.

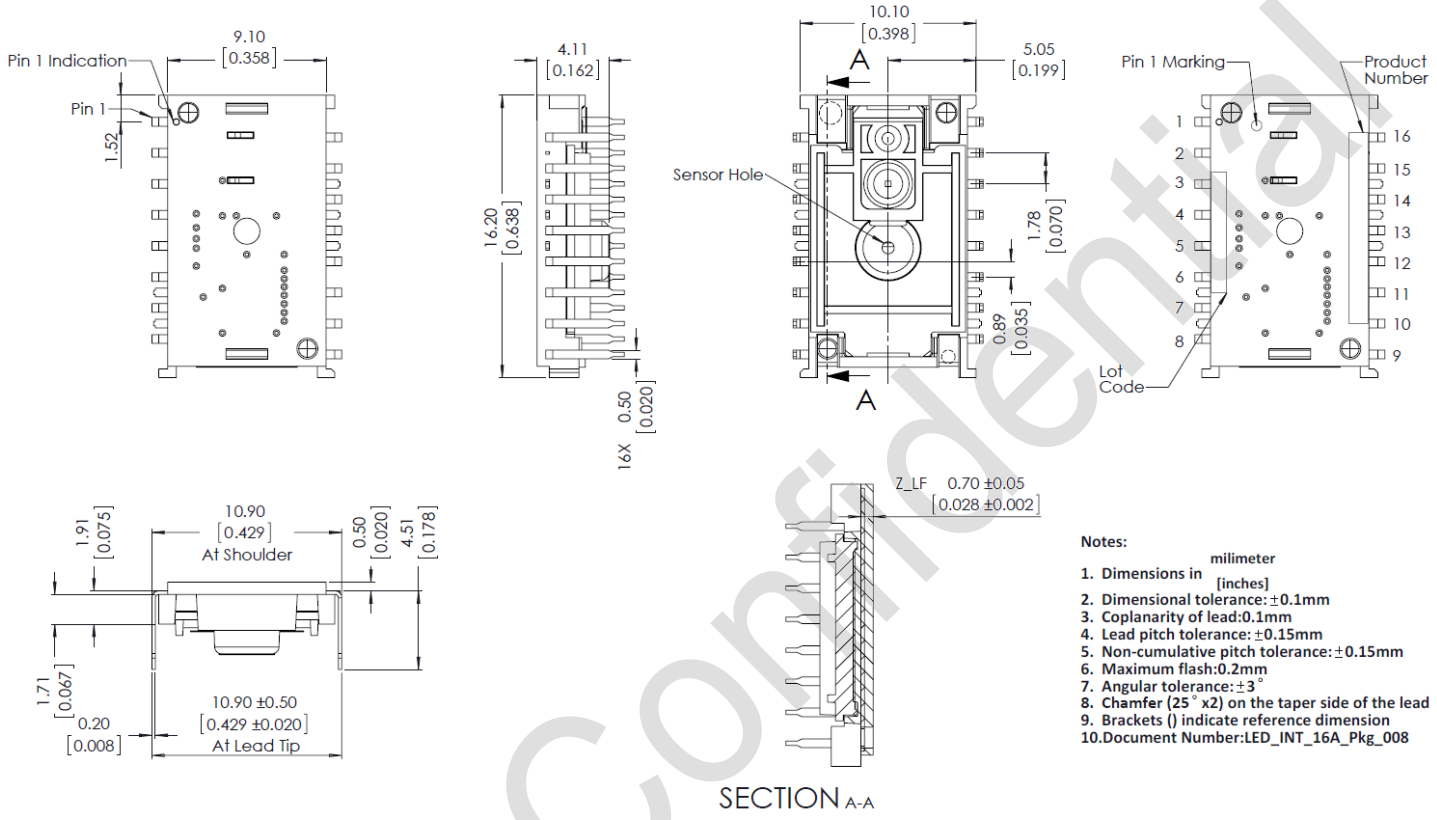
Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
NCS Inactive After Motion Burst	t_{BEXIT}	500			ns	Minimum NCS inactive time after motion burst before next SPI usage
NCS To SCLK Active	$t_{NCS-SCLK}$	120			ns	From last NCS falling edge to 1st SCK rising edge.
SCLK To NCS Inactive (For Read Operation)	$t_{SCLK-NCS\ read}$	120			ns	From last SCLK rising edge to NCS rising edge, for valid MISO data transfer.
SCLK To NCS Inactive (For Write Operation)	$t_{SCLK-NCS\ write}$	1			µs	From last SCLK rising edge to NCS rising edge, for valid MOSI data transfer.
NCS To MISO High-Z	$t_{NCS-MISO}$			500	ns	From NCS rising edge to MISO high-Z state
Transient Supply Current	I_{DDT}		70		mA	Max supply current during the supply ramp from 0V to V_{DD} with min 150us and max 20ms rise time. (Does not include charging currents of bypass capacitors)
	I_{DDTIO}		60		mA	Max supply current during the supply ramp from 0V to V_{DDIO} with min 150us and max 20ms rise time. (Does not include charging currents of bypass capacitors)

Note: All the parameters are tested under recommended operating conditions. Typical values at 25 °C & VDD & VDDIO =1.9V

3.0 Mechanical Specifications

This section covers PAW3370's guidelines and recommendations in term of chip, lens & PCB assemblies.

3.1 Chip Package Dimension



Notes:
1. Dimensions in milimeter [inches]
2. Dimensional tolerance: ±0.1mm
3. Coplanarity of lead:0.1mm
4. Lead pitch tolerance: ±0.15mm
5. Non-cumulative pitch tolerance: ±0.15mm
6. Maximum flash:0.2mm
7. Angular tolerance: ±3°
8. Chamfer (25° x2) on the taper side of the lead
9. Brackets () indicate reference dimension
10. Document Number:LED_INT_16A_Pkg_008

Figure 3. Package Outline Drawing

CAUTION: It is advised that normal static discharge precautions be taken in handling and assembling of this component to prevent damage and/or degradation which may be induced by ESD.

3.2 Package Marking Identification

Refer to Figure 2. Pinout

Table 7. Package Marking Description

Items	Marking	Remark
Product Number	PAW3370DM-T4QU	
Lot Code	AYWWXXXXX	**A**: Assembly house **Y**: Year **WW**: Week **XXXXX**: PixArt reference

3.3 Packing Information

3.3.1 Packing Tube

- Quantity: 25 units per tube
- Size : 500 mm X 13.5 mm X 7.0 mm

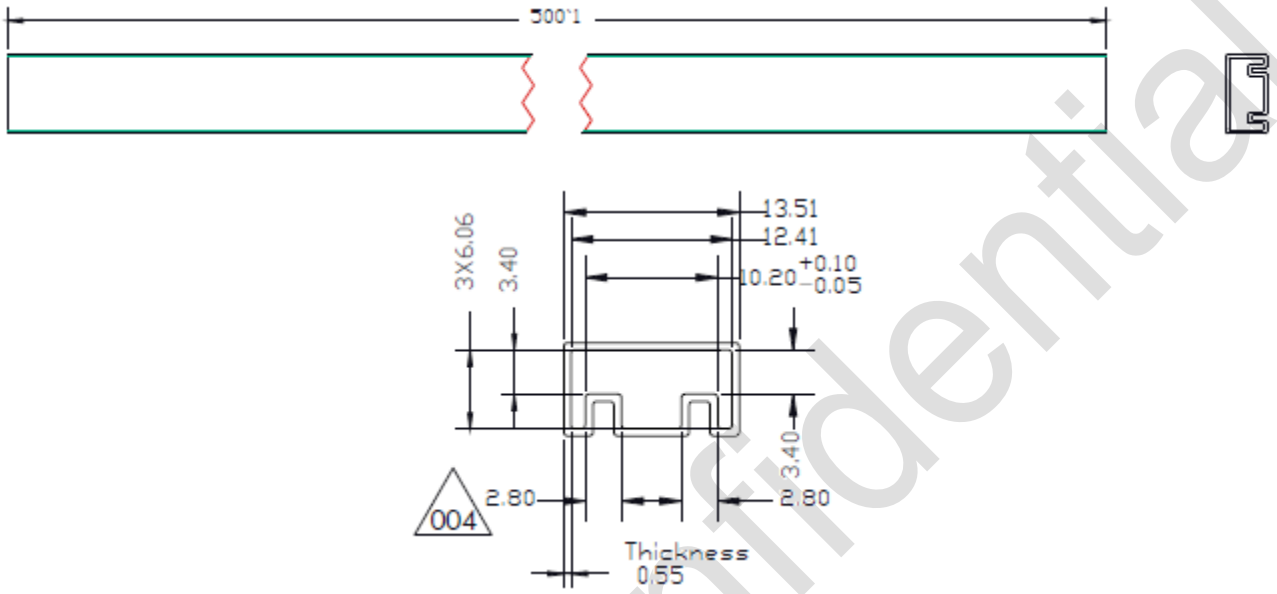
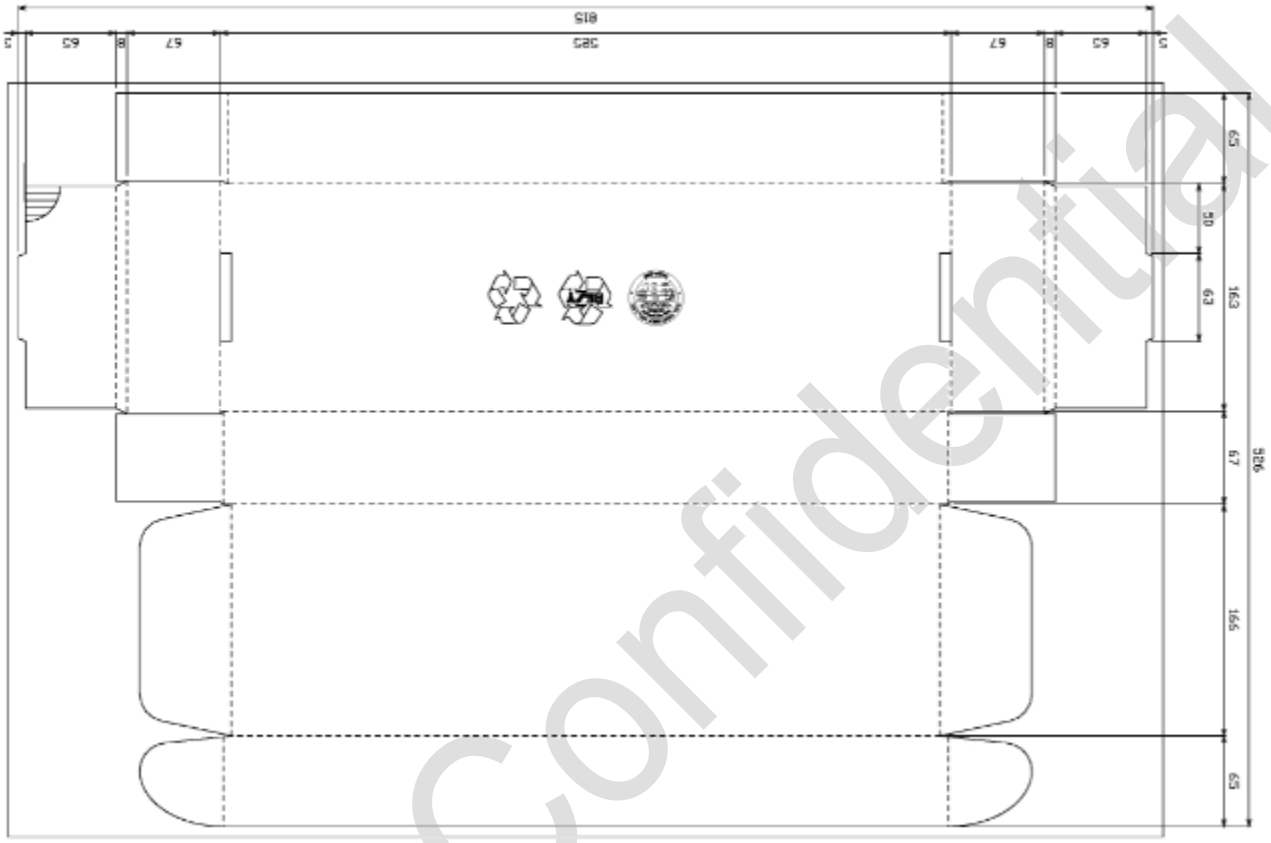


Figure 4. Packing Tube

3.3.2 Inner Box

- Quantity: 1000 units per box
- Size : 163 mm X 525 mm X 67 mm)

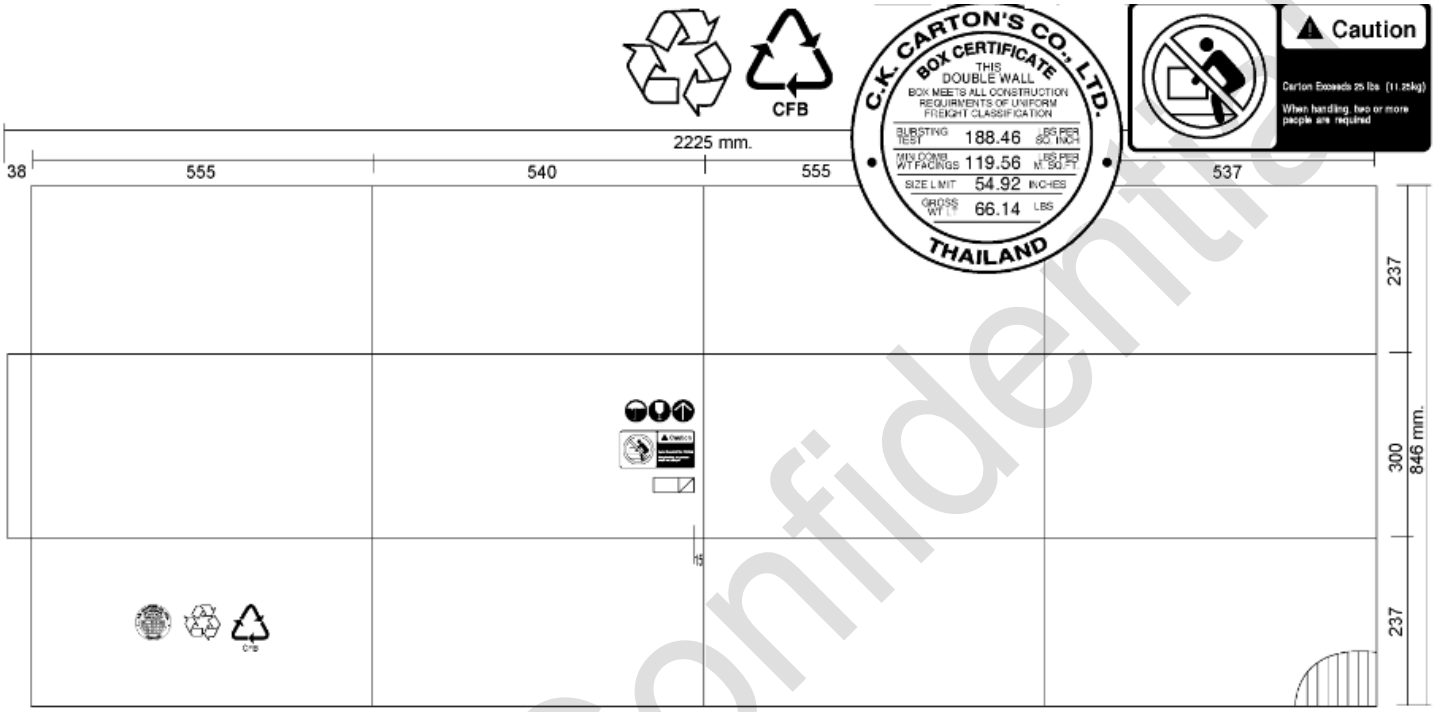


Note: All dimensions are in mm

Figure 5. Inner Box Dimension

3.3.3 Shipping Carton

- Quantity: 12,000 units per carton
- Size : 540 mm X 550 mm X 300 mm



Note: All dimensions are in mm

Figure 6. Shipping Carton Dimension

4.0 Design References

4.1 Reference Schematic

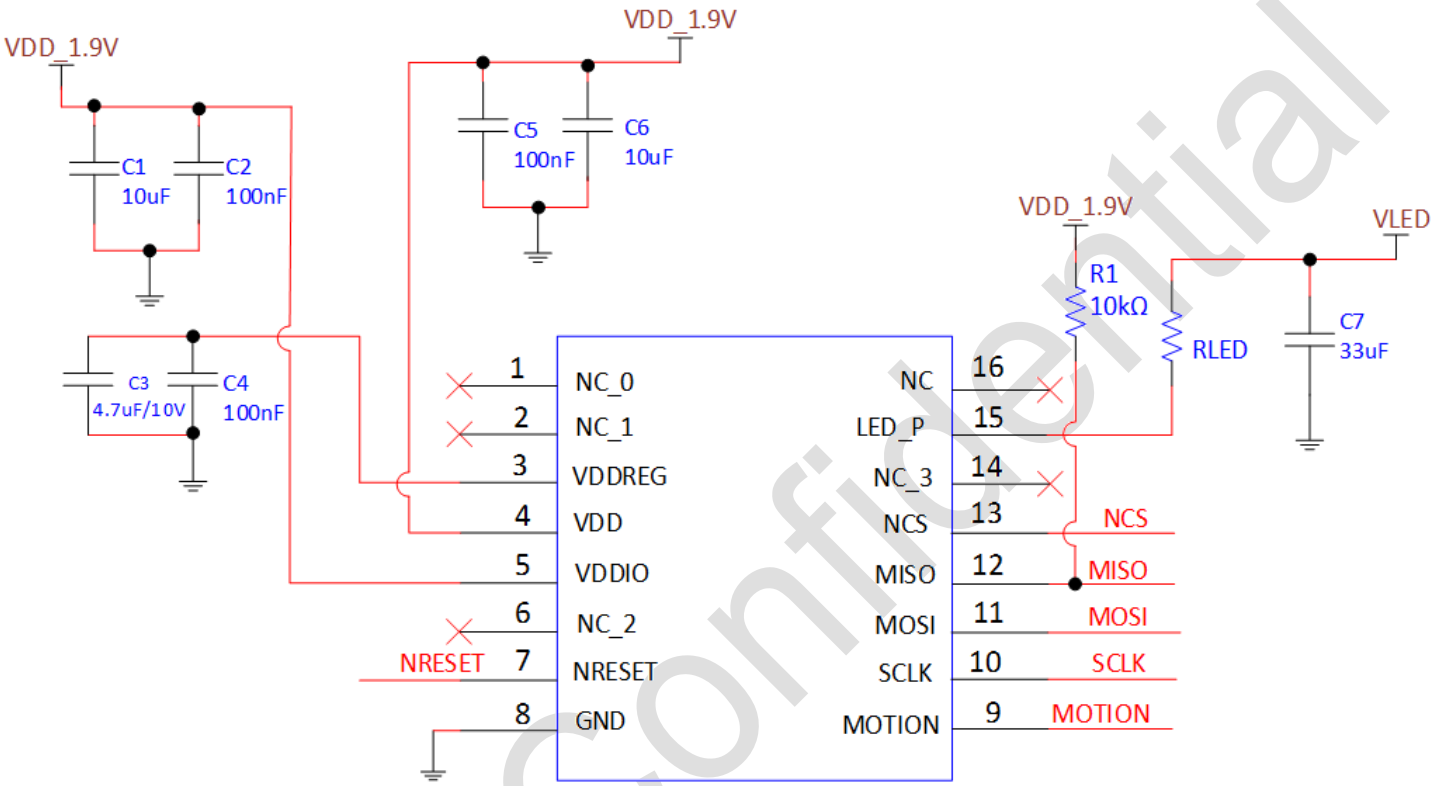


Figure 7. Schematic diagram for PAW3370DM-T4QU Chip

Table 8. Recommended R_{LED}

V_{LED} (V)	Recommended R_{LED} (Ω)
1.9	16

4.2 Recommended PCB Footprint

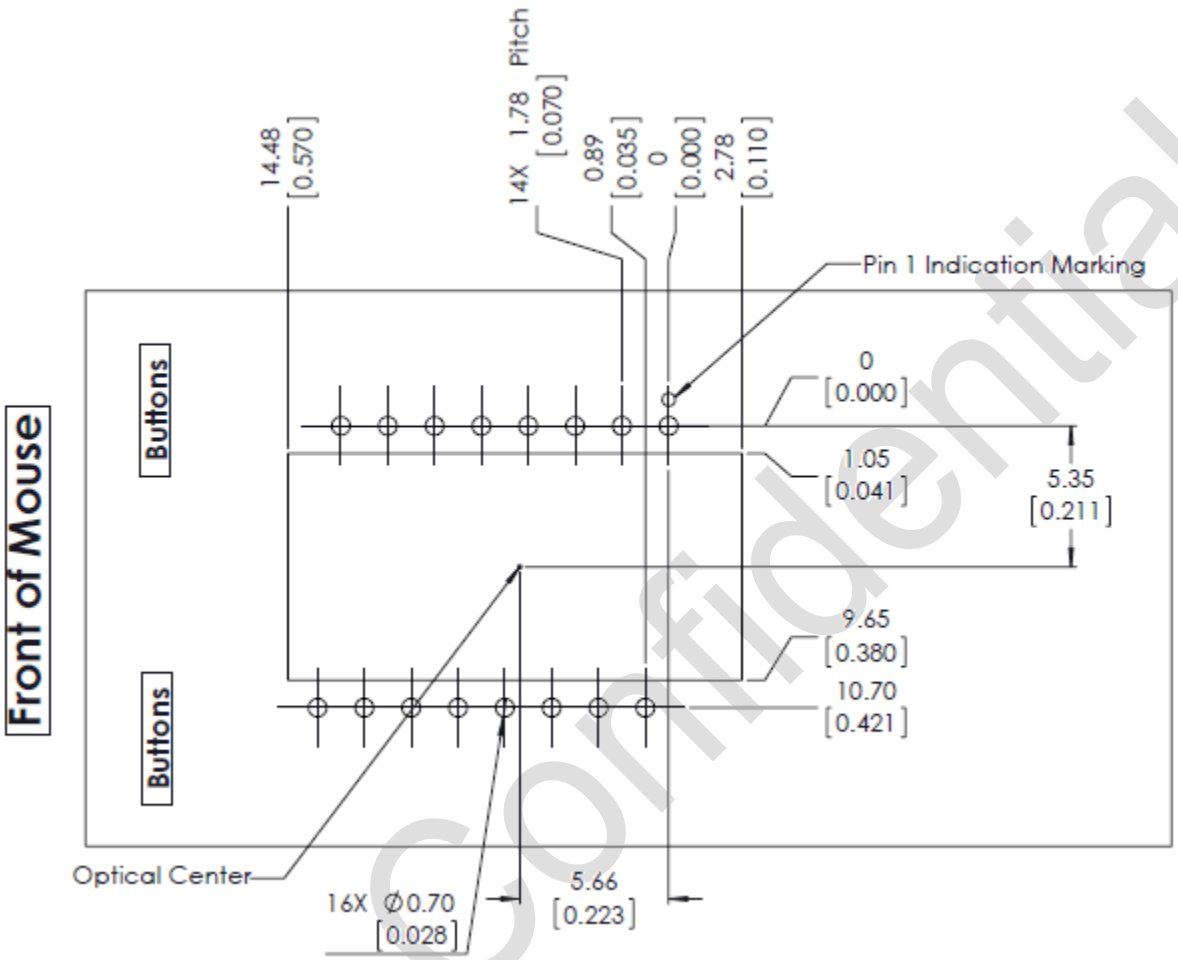


Figure 8. Recommended chip orientation, mechanical cutouts & spacing (Top View)

4.3 Assembly Guide

4.3.1 PCB Assembly Recommendations

1. Insert the integrated chip and all other electrical components into PCB.
2. Wave-solder the entire assembly in a no-wash solder process utilizing solder-fixture. A solder-fixture is required to protect the chip from flux spray and wave solder.
3. Avoid getting any solder flux onto the chip body as there is potential for flux to seep into the chip package. The solder fixture should be designed to expose only the chip leads to flux spray & molten solder while shielding the chip body and optical apertures. The fixture should also set the chip at the correct position and height on the PCB.
4. Place the lens onto the base plate. Care must be taken to avoid contamination on the optical surfaces.
5. Remove the protective Kapton tapes from optical apertures of the chip. Care must be taken to prevent contaminants from entering the apertures. Do not place the PCB with the chip facing up during the entire product assembly process. Hold the PCB vertically when removing Kapton tape.
6. Remove the protective Kapton tapes from optical apertures of the chip. Care must be taken to prevent contaminants from entering the apertures. Do not place the PCB with the chip facing up during the entire mouse assembly process. Hold the PCB vertically when removing Kapton tape.
7. Insert PCB assembly over the lens onto the base plate aligning post to retain PCB assembly. The chip package will self-align to the lens via the guide posts. The optical position reference for the PCB is set by the base plate and lens. Note that the PCB motion due to button presses must be minimized to maintain optical alignment.
8. Install mouse top case. There must be a feature in the top case to press down onto the PCB assembly to ensure all components are stacked or interlocked to the correct vertical height

4.3.2 System Assembly View

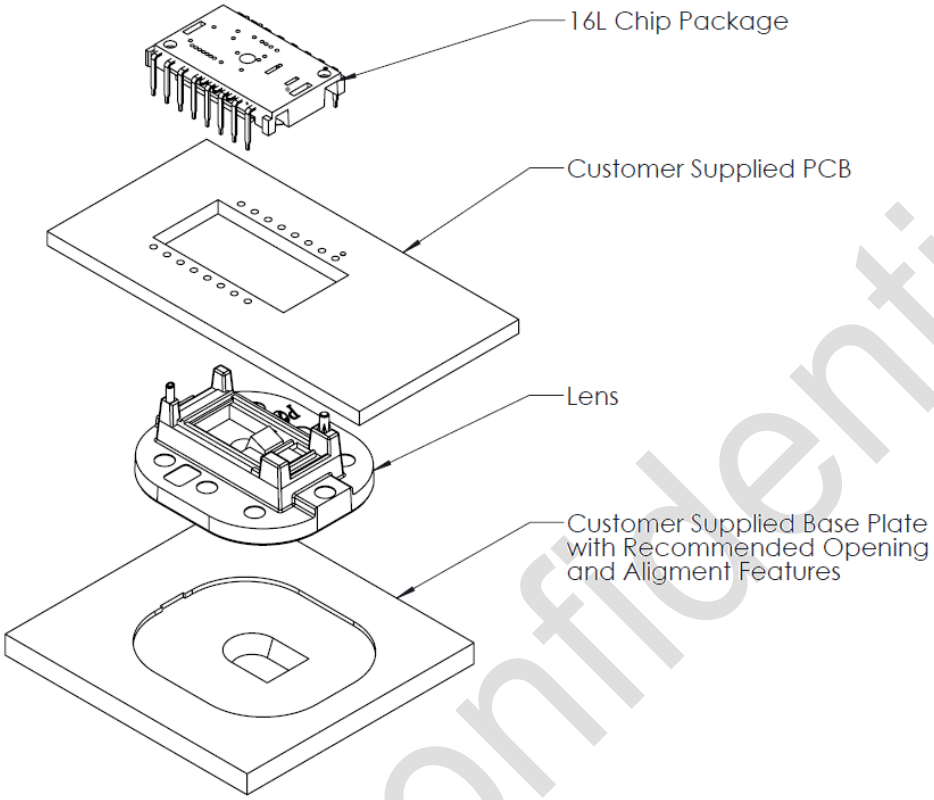


Figure 9. Exploded View of Assembly with LM19-LSI Lens

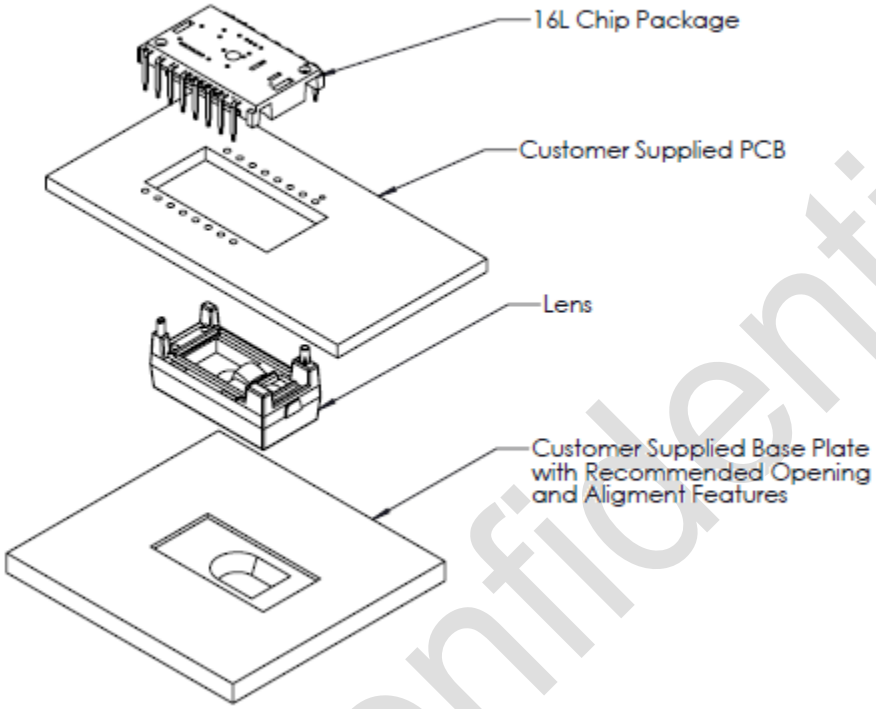


Figure 10 Exploded View of System Assembly with L0AE-LSI1 Lens

5.0 Power States & Sequence

5.1 Power-Up Sequence

Although the sensor performs an internal power up self-reset, it is still recommend that the Power_Up_Reset register is written every time power is applied. The appropriate sequence is as follows:

1. Apply power to VDD and VDDIO in any order, with a delay of no more than 100ms in between each supply. Ensure all supplies are stable.
2. Wait for 50ms.
3. Drive NCS high, and then low to reset the SPI port.
4. Write 0x5A to Power_Up_Reset register (or alternatively toggle the NRESET pin).
5. Wait for at least 5ms.
6. Load Power-up initialization register setting.
7. Read from registers 0x02, 0x03, 0x04, 0x05 and 0x06 one time regardless of the motion bit state.

5.2 Power-Up Initialization Register Setting

Note: Power-up initialization register setting must be loaded into the chip before performing any register read.

1. Write register 0x7F with value 0x12
2. Write register 0x47 with value 0x00
3. Write register 0x7F with value 0x00
4. Write register 0x18 with value 0x00
5. Write register 0x40 with value 0x80
6. Write register 0x55 with value 0x01
7. Wait for at least 1ms
8. Write register 0x7F with value 0x0E
9. Write register 0x43 with value 0x1D
10. Read register 0x46 and store in Var“R1”
11. Write register 0x43 with value 0x1E
12. Read register 0x46 and store in Var“R2”
13. Write register 0x7F with value 0x14
14. Write register 0x6A with value “R1”
15. Write register 0x6C with value “R2”
16. Write register 0x7F with value 0x00
17. Write register 0x55 with value 0x00
18. Write register 0x4D with value 0x50
19. Write register 0x4E with value 0x3B
20. Write register 0x4F with value 0x46
21. Write register 0x54 with value 0x34
22. Write register 0x77 with value 0x24
23. Write register 0x7F with value 0x05
24. Write register 0x44 with value 0xA8
25. Write register 0x46 with value 0x15

26. Write register 0x4A with value 0x14
27. Write register 0x51 with value 0x10
28. Write register 0x53 with value 0x0C
29. Write register 0x55 with value 0xC9
30. Write register 0x5B with value 0xEA
31. Write register 0x61 with value 0x13
32. Write register 0x62 with value 0x0B
33. Write register 0x64 with value 0x18
34. Write register 0x6D with value 0x86
35. Write register 0x7D with value 0x85
36. Write register 0x7E with value 0x03
37. Write register 0x7F with value 0x06
38. Write register 0x60 with value 0xB0
39. Write register 0x61 with value 0x00
40. Write register 0x6D with value 0x29
41. Write register 0x6E with value 0x23
42. Write register 0x7E with value 0x40
43. Write register 0x7F with value 0x07
44. Write register 0x42 with value 0x15
45. Write register 0x7F with value 0x08
46. Write register 0x42 with value 0x28
47. Write register 0x43 with value 0x32
48. Write register 0x7F with value 0x09
49. Write register 0x40 with value 0x03
50. Write register 0x7F with value 0x0A
51. Write register 0x4A with value 0x28
52. Write register 0x4C with value 0x28
53. Write register 0x49 with value 0x00
54. Write register 0x4F with value 0x02
55. Write register 0x7F with value 0x0C
56. Write register 0x40 with value 0x90
57. Write register 0x41 with value 0x50
58. Write register 0x42 with value 0x0C
59. Write register 0x43 with value 0xA8
60. Write register 0x44 with value 0x47
61. Write register 0x45 with value 0x01
62. Write register 0x4D with value 0x4F
63. Write register 0x4E with value 0x1B
64. Write register 0x54 with value 0x00
65. Write register 0x55 with value 0x60
66. Write register 0x56 with value 0x60
67. Write register 0x58 with value 0x30

68. Write register 0x59 with value 0x63
69. Write register 0x7F with value 0x0D
70. Write register 0x4B with value 0x23
71. Write register 0x4C with value 0x40
72. Write register 0x4E with value 0x6B
73. Write register 0x5E with value 0xC3
74. Write register 0x4F with value 0x02
75. Write register 0x7F with value 0x10
76. Write register 0x45 with value 0x1E
77. Write register 0x46 with value 0xF0
78. Write register 0x48 with value 0x0F
79. Write register 0x49 with value 0x88
80. Write register 0x4C with value 0x15
81. Write register 0x4F with value 0x00
82. Write register 0x51 with value 0x6F
83. Write register 0x52 with value 0x90
84. Write register 0x54 with value 0x64
85. Write register 0x55 with value 0xF0
86. Write register 0x5C with value 0x40
87. Write register 0x61 with value 0xEE
88. Write register 0x62 with value 0xE5
89. Write register 0x7F with value 0x14
90. Write register 0x53 with value 0x0C
91. Write register 0x4A with value 0x67
92. Write register 0x6D with value 0x20
93. Write register 0x6E with value 0x00
94. Write register 0x73 with value 0x83
95. Write register 0x74 with value 0x00
96. Write register 0x7A with value 0x16
97. Write register 0x63 with value 0x14
98. Write register 0x62 with value 0x14
99. Write register 0x7F with value 0x00
100. Write register 0x5B with value 0x40
101. Write register 0x61 with value 0xAD
102. Write register 0x51 with value 0xEA
103. Write register 0x19 with value 0x9F
104. Read register 0x20 at 1ms interval until 0x0F is obtained of read up to 100ms, this register read interval must be carried out at 1ms interval with timing tolerance of +/- 1%.
105. Write register 0x19 with value 0x10
106. Write register 0x61 with value 0xD5
107. Write register 0x40 with value 0x00
108. Write register 0x7F with value 0x00

During power-up there will be a period of time after the power supply is high but before any clocks are available. The table below shows the state of the various pins during power-up and reset.

Table 9. State of Signal Pins after VDD is Valid

Pin	During Reset	After Reset
NRESET	Functional	Functional
NCS	Ignored	Functional
MISO	Undefined	Depends on NCS
SCLK	Ignored	Depends on NCS
MOSI	Ignored	Depends on NCS
MOTION	Undefined	Functional

5.3 NRESET

The NRESET pin is used to perform the full chip reset. When asserted, it performs the same reset function as the Power_Up_Reset_Register. The NRESET pin needs to be asserted (held to logic 0) for at least 100 ns duration for the chip to reset.

Note: NRESET pin has built in weak pull up circuit. During active low reset phase, it can draw a static current of up to 600uA.

5.4 Power-Down Sequence

PAW3370DM-T4QU can be set in Shutdown mode by writing to Shutdown register 0x3B with value 0xB6. The SPI port should not be accessed when Shutdown mode is asserted, except the power-up command (writing 0x5A to register 0x3A). Other ICs on the same SPI bus can be accessed, as long as the chip's NCS pin is not asserted.

To de-assert Shutdown mode:

1. Drive NCS high, and then low to reset the SPI port.
2. Write 0x5A to Power_Up_Reset register.
3. Wait for at least 5ms.
4. Load power up initialization register setting as per Section 5.0, step 6.
5. Read from registers 0x02, 0x03, 0x04, 0x05 and 0x06 one time regardless of the motion bit state.

Table 10. Status during Shutdown Mode

Pin	Status
NRESET	High
NCS	High[*1]
MISO	Hi-Z[*2]
SCLK	Ignore if NCS = 1[*3]
MOSI	Ignore if NCS = 1[*4]
MOTION	Output High

Notes:

*1. NCS pin must be held to 1 (high) if SPI bus is shared with other devices. It is recommended to hold to 1 (high) during Shutdown unless powering up the Chip. It must be held to 0 (low) if the chip is to be re-powered up from shutdown (writing 0x5a to register 0x3a).

*2. MISO should be either externally pulled up or down during shutdown in order to meet the low power consumption specification in the datasheet.

*3. SCLK is ignored if NCS is 1 (high). It is functional if NCS is 0 (low).

*4. MOSI is ignored if NCS is 1 (high). If NCS is 0 (low), any command present on the MOSI pin will be ignored except power-up command (writing 0x5a to register 0x3a).

CAUTION: *There is long wakeup time from shutdown. Shutdown should not be used for power management during normal mouse motion.*

6.0 Serial Peripheral Interface Communication

6.1 Signal Description

The synchronous serial port is used to write and read registers in the chip.

The port is a four wire port. The host microcontroller always initiates communication. The chip never initiates any data transfers. SCLK, MOSI and NCS may be driven directly by a microcontroller. The port pins may be shared with other SPI slave devices. When the NCS pin is driven high, the input signals are ignored and the output is tri-stated.

Table 11. SPI Port Signals Description

Signal Name	Functional Description
SCLK	Clock input, generated by the master (microcontroller).
MOSI	Input data. (Master Out/Slave In)
MISO	Output data. (Master In/Slave Out)
NCS	Chip select input (active low). NCS needs to be low to activate the serial port; otherwise, MISO will be high Z, and MOSI & SCLK will be ignored. NCS can also be used to reset the serial port in case of an error.

6.2 Motion Bit Timing

The motion pin is an active low output that signals the micro-controller when motion has occurred. The motion pin is lowered whenever the motion bit is set; in other words, whenever there is non-zero data in the Delta_X_L, Delta_X_H, Delta_Y_L or Delta_Y_H registers. Clearing the motion bit (by reading Delta_X_L, Delta_X_H, Delta_Y_L or Delta_Y_H registers) will put the motion pin high.

6.3 Chip Select Operation

The serial port is activated after NCS goes low. If NCS is raised during a transaction, the entire transaction is aborted and the serial port will be reset. After a transaction is aborted, the normal address-to-data or transaction-to-transaction delay is required before beginning the next transaction. In order to improve communication reliability, all serial transactions should be framed by NCS. In other words, the port should not remain enabled during periods of non-use because any ESD and EFT/B event could be interpreted as serial communication and put the chip into an unknown state. In addition, NCS must be raised after each burst-mode transaction is complete or to terminate burst-mode operation. The port is not available for further use until burst-mode is terminated.

6.4 Write Operation

Write operation, defined as data going from the micro-controller to chip, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The chip reads MOSI on rising edges of SCLK.

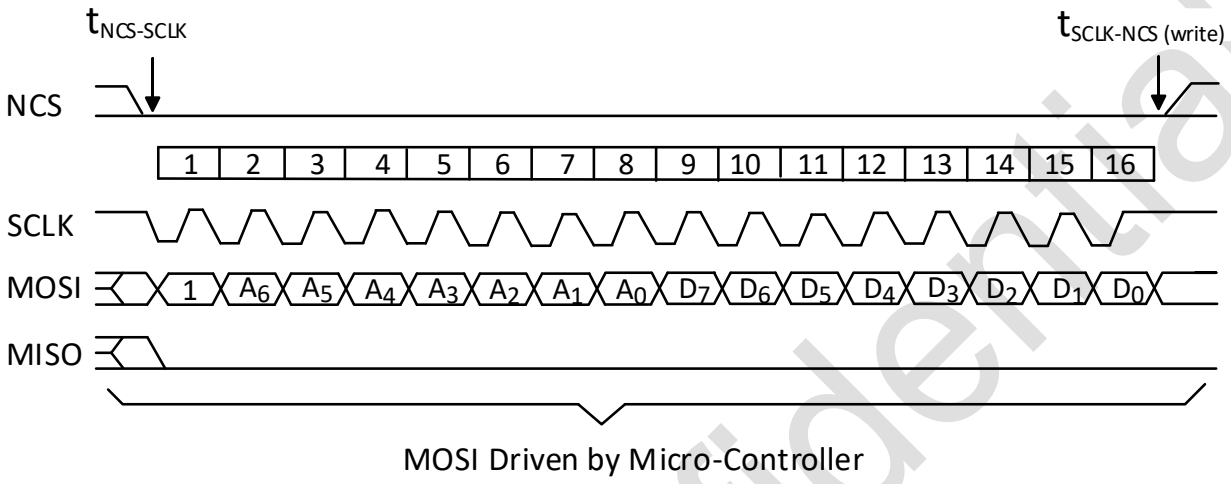


Figure 11. Write Operation

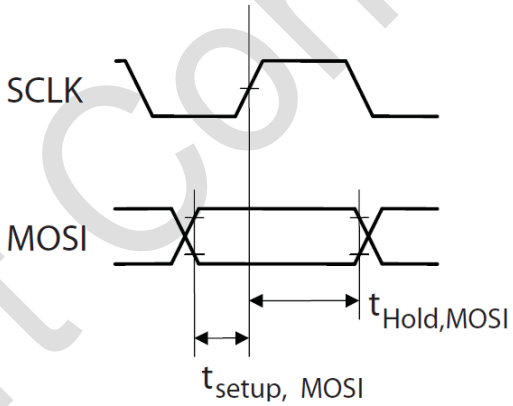


Figure 12. MOSI Setup and Hold Time

6.5 Read Operation

A read operation, defined as data going from chip to the micro-controller, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address, is sent by the micro-controller over MOSI, and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by PAW3370DM-T4QU chip over MISO. The chip outputs MISO bits on falling edges of SCLK and samples MOSI bits on every rising edge of SCLK.

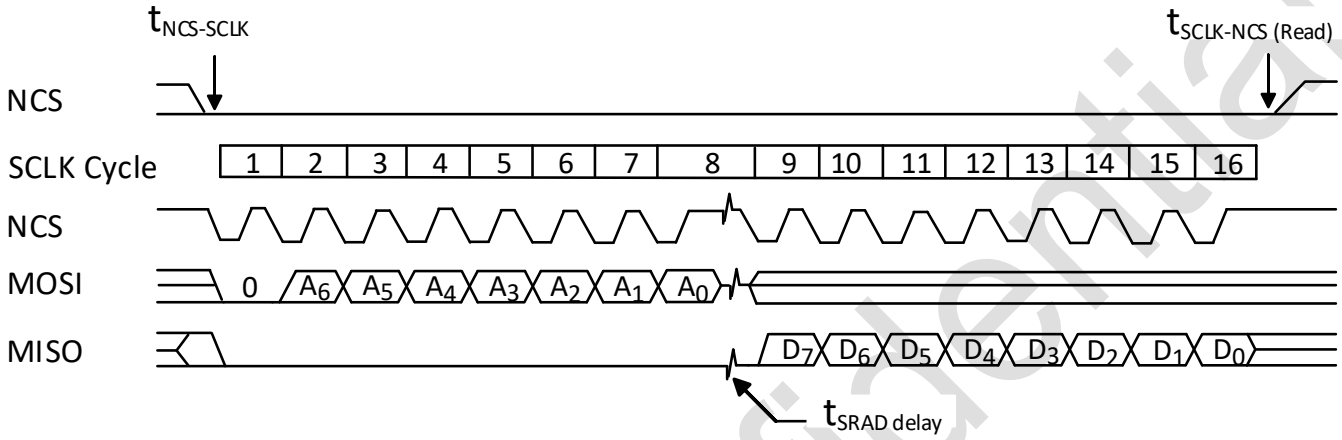


Figure 13. Read Operation

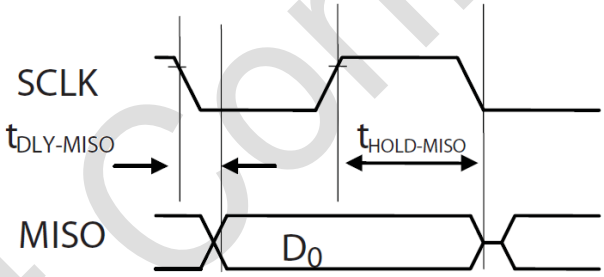


Figure 14. MISO Delay and hold time

Note: The minimum high state of SCLK is also the minimum MISO data hold time of PAW3370DM-T4QU chip. Since the falling edge of SCLK is actually the start of the next read or write command, the chip will hold the state of data on MISO until the falling edge of SCLK.

6.6 Required Timing between Read and Write Commands

There are minimum timing requirements between read and write commands on the serial port.

If the rising edge of the SCLK for the last data bit of the second write command occurs before the t_{SWW} delay, then the first write command may not complete correctly.

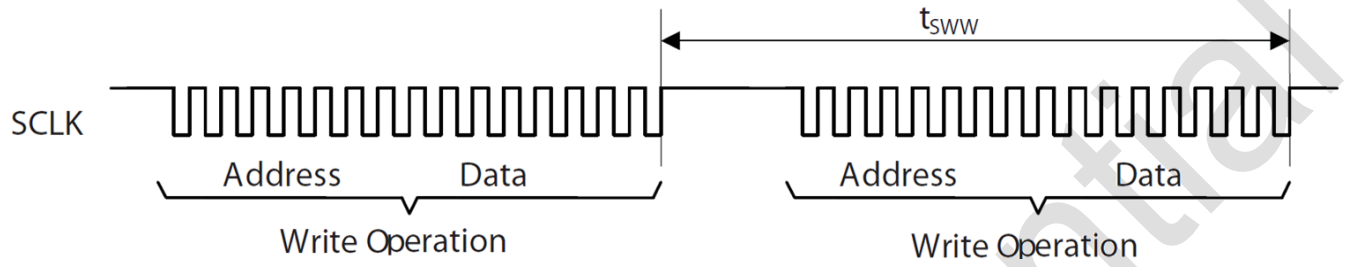


Figure 15. Timing between two Write commands

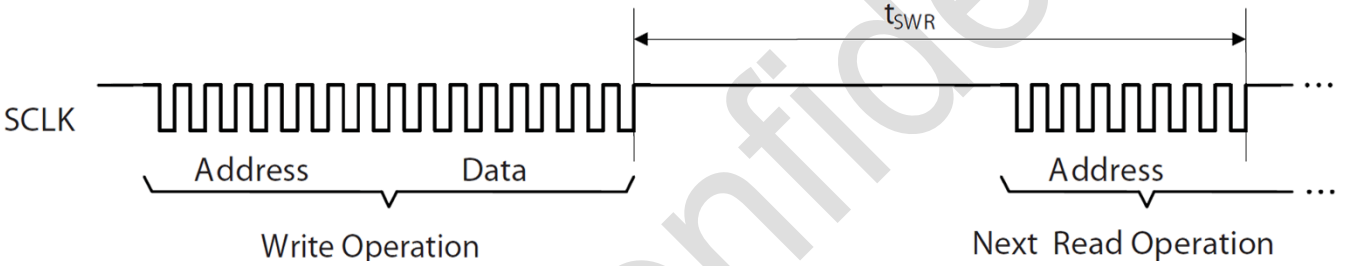


Figure 16. Timing between Write and Either Write or Subsequent Read Commands

If the rising edge of SCLK for the last address bit of the read command occurs before the t_{SWR} required delay, the write command may not complete correctly. During a read operation SCLK should be delayed at least t_{SRAD} after the last address data bit to ensure that the chip has time to prepare the requested data.

The falling edge of SCLK for the first address bit of either the read or write command must be at least t_{SRR} or t_{SRW} after the last SCLK rising edge of the last data bit of the previous read operation. In addition, during a read operation SCLK should be delayed after the last address data bit to ensure that the chip has time to prepare the requested data.

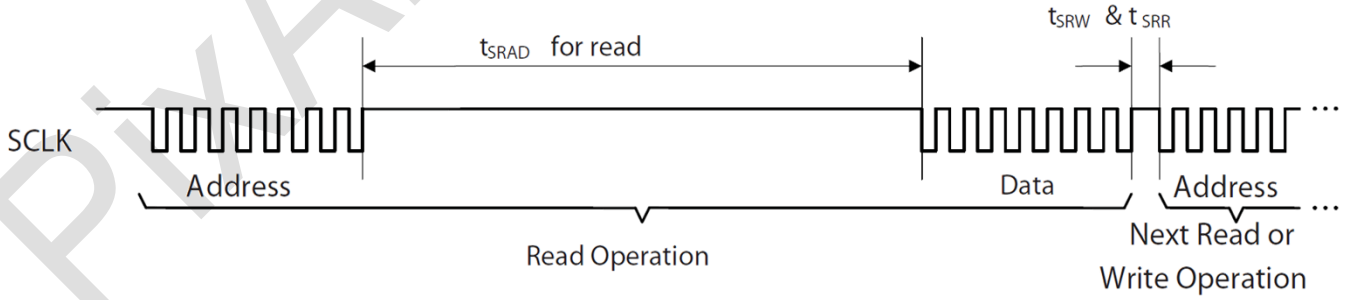


Figure 17. Timing between Read and Either Write or Subsequent Read Commands

6.7 Burst Mode Operation

Burst mode is a special serial port operation mode which may be used to reduce the serial transaction time for predefined registers. The speed improvement is achieved by continuous data clocking to or from multiple registers without the need to specify the register address and by not requiring the normal delay period between data bytes.

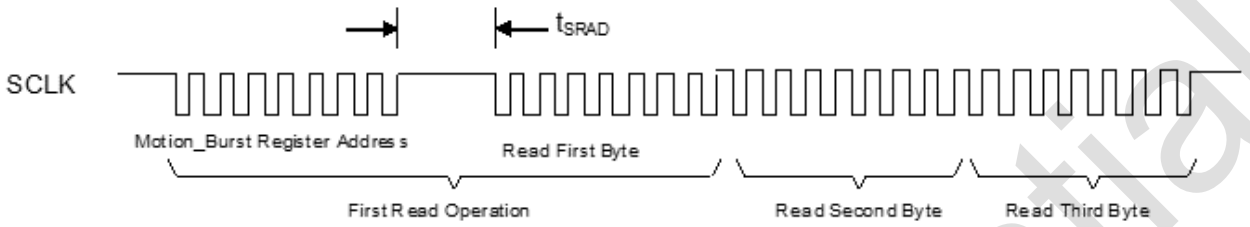


Figure 18. Motion Burst Timing

Motion Burst Read

Reading the Burst_Motion_Read register activates this mode. The chip will respond with the following motion burst report in order. Motion burst report:

BYTE[00] = Motion
BYTE[01] = Chip_Observation
BYTE[02] = Delta_X_L
BYTE[03] = Delta_X_H
BYTE[04] = Delta_Y_L
BYTE[05] = Delta_Y_H
BYTE[06] = SQUAL
BYTE[07] = RawData_Sum
BYTE[08] = Maximum_RawData
BYTE[09] = Minimum_RawData
BYTE[10] = Shutter_Upper
BYTE[11] = Shutter_Lower

After sending the register address, the microcontroller must wait for t_{SRAD}, and then begin reading data. All data bits can be read with no delay between bytes by driving SCLK at the normal rate. The data are latched into the output buffer after the last address bit is received. After the burst transmission is complete, the microcontroller must raise the NCS line for at least t_{BEXIT} to terminate burst mode. The serial port is not available for use until it is reset with NCS, even for a second burst transmission.

Procedure to start motion burst as below.

1. Pull NCS line to low.
2. Read Motion_Burst register (address 0x16).
3. Wait for t_{SRAD}.
4. Start reading SPI Data continuously up to 12 bytes.
   Motion burst may be terminated by pulling NCS high for at least t_{BEXIT}.
5. To read new motion burst data, start again from step 1.

Burst mode must be terminated by the micro-controller by raising the NCS line for at least t_{BEXIT}. The serial port is not available for use until it is reset with NCS signal, even for a second Burst transmission.

Note: Motion burst data can be read from Motion_Burst register even in rest modes.

7.0 System Control

7.1 Gaming and Office Mode Setting

PAW3370DM-T4QU can be programmed to different gaming and office modes per the register settings in the table below. Please note that upon chip start-up per the recommended Power-Up Sequence, the chip is set to Low Power Gaming Mode 1 as default.

Table 12. Low Power Gaming Modes Setting

Low Power Gaming Mode 1 (Default)	Low Power Gaming Mode 2
1. Write register 0x7F with value 0x05	1. Write register 0x7F with value 0x05
2. Write register 0x40 with value 0x80	2. Write register 0x40 with value 0x8C
3. Write register 0x53 with value 0x0C	3. Write register 0x53 with value 0x10
4. Write register 0x55 with value 0xC9	4. Write register 0x55 with value 0xC9
5. Write register 0x61 with value 0x13	5. Write register 0x61 with value 0x13
6. Write register 0x62 with value 0x0B	6. Write register 0x62 with value 0x18
7. Write register 0x7D with value 0x85	7. Write register 0x7D with value 0x86
8. Write register 0x7E with value 0x03	8. Write register 0x7E with value 0x03
9. Write register 0x7F with value 0x06	9. Write register 0x7F with value 0x06
10. Write register 0x60 with value 0XB0	10. Write register 0x60 with value 0X80
11. Write register 0x61 with value 0x00	11. Write register 0x61 with value 0x01
12. Write register 0x62 with value 0x10	12. Write register 0x62 with value 0x10
13. Write register 0x63 with value 0x00	13. Write register 0x63 with value 0x00
14. Write register 0x7F with value 0x00	14. Write register 0x7F with value 0x00
15. Write register 0x54 with value 0x34	15. Write register 0x54 with value 0x34
16. Write register 0x77 with value 0x31	16. Write register 0x77 with value 0x31
17. Write register 0x78 with value 0x01	17. Write register 0x78 with value 0x04
18. Write register 0x79 with value 0x4F	18. Write register 0x79 with value 0x14
19. Write register 0x7A with value 0x08	19. Write register 0x7A with value 0x08
20. Write register 0x7B with value 0x4A	20. Write register 0x7B with value 0x4A

Table 13. Corded Gaming and Office Modes Setting

Corded Mode	Office Mode
1. Write register 0x7F with value 0x05	1. Write register 0x7F with value 0x05
2. Write register 0x40 with value 0x80	2. Write register 0x40 with value 0x80
3. Write register 0x53 with value 0x0C	3. Write register 0x53 with value 0x10
4. Write register 0x55 with value 0xC9	4. Write register 0x55 with value 0x84
5. Write register 0x61 with value 0x13	5. Write register 0x61 with value 0x11
6. Write register 0x62 with value 0x04	6. Write register 0x62 with value 0x50
7. Write register 0x7D with value 0x85	7. Write register 0x7D with value 0x85
8. Write register 0x7E with value 0x03	8. Write register 0x7E with value 0x23
9. Write register 0x7F with value 0x06	9. Write register 0x7F with value 0x06
10. Write register 0x60 with value 0X40	10. Write register 0x60 with value 0x00
11. Write register 0x61 with value 0x00	11. Write register 0x61 with value 0x06
12. Write register 0x62 with value 0x10	12. Write register 0x62 with value 0x60
13. Write register 0x63 with value 0x00	13. Write register 0x63 with value 0x00
14. Write register 0x7F with value 0x00	14. Write register 0x7F with value 0x00
15. Write register 0x54 with value 0x34	15. Write register 0x54 with value 0x42
16. Write register 0x77 with value 0x31	16. Write register 0x77 with value 0x0C
17. Write register 0x78 with value 0x01	17. Write register 0x78 with value 0x0A
18. Write register 0x79 with value 0x4F	18. Write register 0x79 with value 0x02
19. Write register 0x7A with value 0x08	19. Write register 0x7A with value 0x19
20. Write register 0x7B with value 0x4A	20. Write register 0x7B with value 0x0C

Note: Corded Gaming mode provides similar tracking performance as Low Power Gaming Mode 1 with consistent delta_X and delta_Y report size over USB report rate.

7.2 Power Management for Wireless Mode

PAW3370DM-T4QU has three power-saving modes. Each mode has a different motion detection period with its respective response time to mouse motion. Response time is the time taken for the chip to 'wake up' from rest mode when motion is detected. When left idle, the chip automatically changes or downshift from Run mode to Rest1, then to Rest2 and finally to Rest3 which consumes the least amount of current.

The current consumption is lowest at Rest3 and highest at Rest1. However the time required for chip to respond to motion from Rest1 is the shortest and longest from Rest3. Downshift time is the elapsed time (under no motion condition) from an existing mode to the next mode. For example, it takes 20s for the chip which is in Rest1 mode to change (downshift) to Rest2. The response time and downshift time for each mode is shown in the following table.

However user can change the timing setting for each mode via register 0x77 through 0x7C.

Table 14. Rest Modes Response & Downshift Time

Mode	Low Power Gaming Mode 1 (Default)		Low Power Gaming Mode 2		Office Mode	
	Response Time	Downshift Time	Response Time	Downshift Time	Response Time	Downshift Time
Rest1	1ms	1s	4ms	1s	10ms	248ms
Rest2	32ms	20s	32ms	20s	100ms	5s
Rest3	500ms	600s	500ms	600s	500ms	300s

Note: These timings are based on Power-Up Initialization Register Setting in section 5.0 and subjected to change if any of the register 0x77 to 0x7C value is updated

7.3 Universal Lift Cut Off Setting

The Universal Lift Cut Off setting applies to all PixArt Standard Gaming Surfaces. The lift-cut off can be set to 1mm and 2mm when mated with the LM19-LSI and L0AE-LSI1 lens, per the register settings in the table below.

Please note that upon sensor start-up per the recommended Power-Up Sequence, the lift cut off is set to 1mm as default.

Table 15. Lift Cut Off Setting for LM19-LSI and L0AE-LSI1 lens

Lens	Lift Cut Off Setting	Register Setting
LM19-LSI & L0AE-LSI1	1mm setting (Default in Power Up Sequence)	1. Write register 0x7F with value 0x0C 2. Write register 0x40 with value 0x90 3. Write register 0x41 with value 0x50 4. Write register 0x42 with value 0x0C 5. Write register 0x43 with value 0xA8 6. Write register 0x44 with value 0x47 7. Write register 0x45 with value 0x01 8. Write register 0x4A with value 0x19 9. Write register 0x4B with value 0x18 10. Write register 0x4C with value 0x60 11. Write register 0x4E with value 0x1B 12. Write register 0x6D with value 0x7F 13. Write register 0x7F with value 0x00
	2mm setting	1. Write register 0x7F with value 0x0C 2. Write register 0x40 with value 0x14 3. Write register 0x41 with value 0x14 4. Write register 0x42 with value 0x20 5. Write register 0x43 with value 0x18 6. Write register 0x44 with value 0xD3 7. Write register 0x45 with value 0x0E 8. Write register 0x4A with value 0x0A 9. Write register 0x4B with value 0x08 10. Write register 0x4C with value 0x45 11. Write register 0x4E with value 0x0F 12. Write register 0x6D with value 0x5F 13. Write register 0x7F with value 0x00

7.5 Manual Lift Cut Off Calibration

PAW3370 has the capability to optimize its lift performance by tuning internal parameter on a specific gaming mat or tracking surface, this feature involves end user interaction.

7.5.1 Lift Cut Off Calibration Procedures

1. Ensure that the chip is powered up according to the Power Up Sequence in section 5.0.
2. Prompt the user that the manual lift cut off calibration is about to begin and ensure that the mouse is placed nominally on the surface (mouse is not lifted).
3. Start the calibration procedure by loading the following register values in sequence:
   - Write register 0x7F with value 0x06
   - Write register 0x71 with value 0x01
   - Write register 0x7F with value 0x0C
   - Read register 0x4E and store its value into Var_Config
   - Write register 0x4E with value 0x00
   - Write register 0x7F with value 0x00
   - Write register 0x40 with value 0x80
   - Write register 0x7F with value 0x04
   - Write register 0x40 with value 0x81
4. The calibration procedure can be started by a SW prompt to the user or user-initiated through a mouse-click event. Recommend to move the mouse over a distance of >20inch to cover most area of the tracking surface.
5. Write register 0x40 with value 0x80, then write register 0x40 with value 0x00 to stop the Calibration.
6. Read register 0x4C bit[2] to check the status of the calibration process.
   - If the returned value is HIGH, it indicates the calibration is completed, proceed to step7.
   - Whereas LOW indicates the calibration is incomplete, repeat step5.
7. Check register 0x4C bit[0],
   - If the returned value of bit[0] is HIGH, the calibration is completed successfully, proceed to step 8.
   - Else, the calibration is failed, load the following register values to exit the lift cut off calibration process, then restart from step 1.
     i. Write register 0x7F with value 0x0C
     ii. Write register 0x4E with value Var_Config
     iii. Write register 0x7F with value 0x06
     iv. Write register 0x71 with value 0x00
     v. Write register 0x7F with value 0x00
     vi. Write register 0x40 with value 0x00
8. Write register 0x7F with value 0x04
9. Read register 0x4D and store its value into VarA
10. Read register 0x4E and store its value into VarB
11. Write register 0x7F with value 0x0C
12. Write register 0x4E with value Var_Config
13. Write register 0x7F with value 0x00
14. Write register 0x40 with value 0x00
15. Prompt the user that the calibration process is completed, continue to section 7.5.2.

7.5.2 Enable Lift Cut Off Calibration Registers Setting

Write the following set of register values to enable lift cut off calibration register setting. VarA and VarB obtained from section 7.5.1 would be used in this section.

1. Write register 0x7F with value 0x09
2. Write register 0x5D with VarA
3. Write register 0x5B with VArB
4. Write register 0x7F with value 0x06
5. Write register 0x71 with value 0x01
6. Write register 0x73 with value 0x0C
7. Write register 0x7F with value 0x00

7.5.3 Disable Lift Cut Off Calibration Registers Setting

Write the following set of register values to disable lift cut off calibration registers setting in Section 7.5.2 and revert to previous lift cut off setting (1mm or 2mm lift cut off setting).

1. Write register 0x7F with value 0x06
2. Write register 0x71 with value 0x00
3. Write register 0x73 with value 0x00
4. Write register 0x7F with value 0x00

7.6 Raw Data Grab

Raw data grab is the way to download a full array of raw data values from a single frame. Once raw data grab is enabled, the next complete frame image will be stored to memory. In order to stream out the Raw Data values, register read operation is used.

Procedure to start frame capture burst mode is listed as below:

1. Write register 0x7F with value 0x00
2. Write register 0x40 with value 0x80
3. Write register 0x7F with value 0x13
4. Write register 0x47 with value 0x30
5. Write register 0x7F with value 0x00
6. Write register 0x55 with value 0x04
7. Continuously read register 0x02 until getting both OP_Mode_1 and OP_Mode_0 equal to 0.
8. Write register 0x58 with value 0xFF
9. Continuously read register 0x59 until getting PG_FIRST as "1"
10. Continuously read register 0x59 until getting PG_VALID as "1".
11. Read register 0x58 for 7 bit ADC data (RAWDATA 6-0). Repeat (10) and (11) for 900 times to form a complete picture element array information.
12. Write register 0x55 with value 0x00
13. Write register 0x40 with value 0x00
14. Write register 0x7F with value 0x13
15. Write register 0x47 with value 0x20
16. Write register 0x7F with value 0x00

Last Raw Data

29	59	89	119	149	179	209	239	269	299	329	359	389	419	449	479	509	539	569	599	629	659	689	719	749	779	809	839	869	899
28	58	88	118	148	178	208	238	268	298	328	358	388	418	448	478	508	538	568	598	628	658	688	718	748	778	808	838	868	898
27	57	87	117	147	177	207	237	267	297	327	357	387	417	447	477	507	537	567	597	627	657	687	717	747	777	807	837	867	897
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
2	32	62	92	122	152	182	212	242	272	302	332	362	392	422	452	482	512	542	572	602	632	662	692	722	752	782	812	842	872
1	31	61	91	121	151	181	211	241	271	301	331	361	391	421	451	481	511	541	571	601	631	661	691	721	751	781	811	841	871
0	30	60	90	120	150	180	210	240	270	300	330	360	390	420	450	480	510	540	570	600	630	660	690	720	750	780	810	840	870

First Raw Data

+Y

Top X-ray View of Mouse

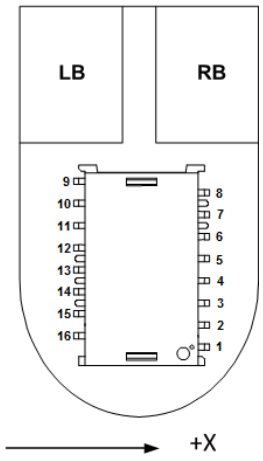


Figure 19. Raw Data Address Map for 30x30 (Chip looking on the navigation surface through the lens)

Note: The X/Y reporting direction shown above follows all the power up initialization sequence in the Power Up section.

8.0 Registers

8.1 Registers List

The chip registers are accessible via the serial port. The registers are used to read motion data and status as well as to set the device configuration.

Table 16. Register List

Address	Register Name	Access	Reset Value
0x00	Product_ID	R	0x4E
0x02	Motion	RW	0x20
0x03	Delta_X_L	R	0x00
0x04	Delta_X_H	R	0x00
0x05	Delta_Y_L	R	0x00
0x06	Delta_Y_H	R	0x00
0x07	SQUAL	R	0x00
0x08	RawData_Sum	R	0x00
0x09	Maximum_RawData	R	0x00
0x0A	Minimum_RawData	R	0x7F
0x0B	Shutter_Lower	R	0x00
0x0C	Shutter_Upper	R	0x01
0x15	Chip_Observation	RW	0x40
0x16	Burst_Motion_Read	R	0x00
0x3A	Power_Up_Reset	W	0x00
0x3B	Shutdown	W	0x00
0x40	Performance	RW	0x00
0x4D	Config 1	RW	0x90
0x4E	Resolution	RW	0x12
0x56	Angle_Snap	RW	0x04
0x58	RawData _Grab	RW	0x00
0x59	RawData _Grab_Status	R	0x00
0x5A	Ripple_Control	RW	0x10
0x5B	Axis_Control	RW	0x60
0x5F	Inv_Product_ID	R	0xB1
0x77	Run_DownShift	RW	0x0C
0x78	Rest1_Period	RW	0x01
0x79	Rest1_Downshift	RW	0x4F
0x7A	Rest2_Period	RW	0x08
0x7B	Rest2_Downshift	RW	0x4A
0x7C	Rest3_Period	RW	0x3F
0x7D	Run_Downshift_Mult	RW	0x07
0x7E	Rest_Downshift_Mult	RW	0x77

8.2 Register Descriptions

8.2.1 Product_ID

Register Name	Product_ID							
Address	0x00							
Access	Read			**Reset Value**		0x4E		
Bit	7	6	5	4	3	2	1	0
Field	PID_{7-0}							
Description	This register contains a unique identification assigned to the PAW3370DM-T4QU. The value in this register does not change; it can be used to verify that the serial communications link is functional.							

8.2.2 Motion

Register Name	Motion							
Address	0x02							
Access	Read/Write			**Reset Value**		0x20		
Bit	7	6	5	4	3	2	1	0
Field	MOT	Reserved	1	Reserved	Lift_Stat	Reserved	OP_Mode_1	OP_Mode_0

Description

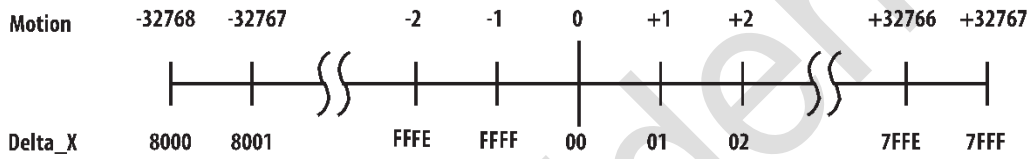
This register allows the user to determine if motion has occurred since the last time it was read. The procedure to read the motion registers (Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H) is as follows:

1. Read the Motion register. This will freeze the Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H register values.
2. If the MOT bit is set, Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers should be read in the given sequence to get the accumulated motion. Note: if Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers are not read before the motion register is read for the second time, the data in Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H will be lost.
3. To read a new set of motion data (Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H), repeat from Step 1.

Field Name	Description
MOT	Motion since last report **0 = No motion** 1 = Motion occurred, data ready for reading in Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers
Lift_Stat	Indicate the lift status of chip 0 – Chip on surface 1 – Chip lifted
$OP\_Mode_{1:0}$	00 – Run Mode 01 – Rest 1 10 - Rest 2 11 - Rest 3

Write any value to this register will clear all motion data.

8.2.3 DELTA_X_L

Register Name	DELTA_X_L							
Address	0x03							
Access	Read			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0
Description	16 bits 2's complement number. Lower 8 bits of Delta_X. X movement is counts since last report. Absolute value is determined by resolution. 							

8.2.4 DELTA_X_H

Register Name	DELTA_X_H							
Address	0x04							
Access	Read			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	X_{15}	X_{14}	X_{13}	X_{12}	X_{111}	X_{10}	X_9	X_8
Description	16 bits 2's complement number. Upper 8 bits of Delta_X. Delta_X_H must be read after Delta_X_L to have the full motion data. ***Note:*** *It is recommended that register 0x02, 0x03, 0x04, 0x05 and 0x06 to be read sequentially.*							

8.2.5 DELTA_Y_L

Register Name	DELTA_Y_L							
Address	0x05							
Access	Read			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
Description	16 bits 2's complement number. Lower 8 bits of Delta_Y. Y movement is counts since last report. Absolute value is determined by resolution.  							

8.2.6 DELTA_Y_H

Register Name	DELTA_Y_H							
Address	0x06							
Access	Read			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8
Description	16 bits 2's complement number. Upper 8 bits of Delta_Y. Delta_Y_H must be read after Delta_Y_L to have the full motion data. ***Note:*** *It is recommended that register 0x02, 0x03, 0x04, 0x05 and 0x06 to be read sequentially.*							

8.2.7 SQUAL

Register Name	SQUAL							
Address	0x07							
Access	Read			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	SQ_7	SQ_6	SQ_5	SQ_4	SQ_3	SQ_2	SQ_1	SQ_0
Description	The SQUAL (Surface quality) register is a measure of the number of valid features visible by the chip in the current frame. Use the following formula to find the total number of valid features. Number of Features = SQUAL Register Value * 4 The maximum SQUAL register value is 0xB6. Since small changes in the current frame can result in changes in SQUAL, variations in SQUAL when looking at a surface is expected. SQUAL values are only valid when chip is in run mode. Disable Rest mode before measuring SQUAL.							

8.2.8 RAWDATA_SUM

Register Name	RAWDATA_SUM							
Address	0x08							
Access	Read			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	RDS_7	RDS_6	RDS_5	RDS_4	RDS_3	RDS_2	RDS_1	RDS_0
Description	This register is used to find the chip average raw data value. It reports the upper byte of a 17-bit counter which sums all 900 raw data in the current frame. To find the average raw data value follows the formula below: Average pixel value = PIX_ACCUM*512/900 The maximum register value is 0xDF(hex) or 223(dec) and the minimum register value is 0. The raw data sum value can change every frame. Disable rest mode before reading Raw Data sum value.							

8.2.9 MAXIMUM_RAWDATA

Register Name	MAXIMUM_RAWDATA							
Address	0x09							
Access	Read			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	$MaxRD_7$	$MaxRD_6$	$MaxRD_5$	$MaxRD_4$	$MaxRD_3$	$MaxRD_2$	$MaxRD_1$	$MaxRD_0$
Description	Maximum Raw Data value in current frame. Minimum value = 0, maximum value = 127. The maximum raw data value can change every frame.							

8.2.10 MINIMUM_RAWDATA

Register Name	MINIMUM_RAWDATA							
Address	0x0A							
Access	Read			Reset Value		0x7F		
Bit	7	6	5	4	3	2	1	0
Field	$MinRD_7$	$MinRD_6$	$MinRD_5$	$MinRD_4$	$MinRD_3$	$MinRD_2$	$MinRD_1$	$MinRD_0$
Description	Minimum Raw data value in current frame. Minimum value = 0, maximum value = 127. The minimum raw data value can change every frame.							

8.2.11 SHUTTER_LOWER

Register Name	SHUTTER_LOWER							
Address	0x0B							
Access	Read			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0
Description	Lower byte of the 12-bit Shutter register.							

8.2.12 SHUTTER_UPPER

Register Name	SHUTTER_UPPER							
Address	0x0C							
Access	Read			Reset Value		0x01		
Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Reserved	S_{11}	S_{10}	S_9	S_8
Description	Upper 4-bit of the 12-bit Shutter register. Units are clock cycles of the internal oscillator. Read Shutter_Upper first, then Shutter_Lower. They should be read consecutively. The shutter is adjusted to keep the average raw data values within normal operating ranges. The shutter value is checked and automatically adjusted to a new value if needed on every frame when operating in default mode.							

8.2.13 CHIP_OBSERVATION

Register Name	CHIP_OBSERVATION							
Address	0x15							
Access	Read/Write			Reset Value		0x40		
Bit	7	6	5	4	3	2	1	0
Field	CO_7	CO_6	CO_5	CO_4	CO_3	CO_2	CO_1	CO_0
Description	To read this register, user must clear the register by writing 0x00, wait for a minimum T_{dly_obs} ms & read the register. The value of CO_{7-0} should be **0xBF** or **0xB7** if the chip is working correctly. If the value is incorrect, recommend to perform chip reset and reload the power up initialization setting as per section 5.2 in this data sheet. The register may be used as part of recovery scheme to detect a problem caused by EFT/B or ESD event. T_{dly_obs} is defined as the longest frame period + 10% variation. The longest frame period is when chip is in Rest3 mode. Clock frequency tolerance value need to be taken into account. For example if the default Rest3 period of 500ms is used, then T_{dly_obs} = 500ms + 50ms							

8.2.14 BURST_MOTION_READ

Register Name	BURST_MOTION_READ							
Address	0x16							
Access	Read			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	MB_7	MB_6	MB_5	MB_4	MB_3	MB_2	MB_1	MB_0
Description	The Burst_Motion_Read register is used for high-speed access to the Motion, Observation, Delta_X_L, Delta_X_H, Delta_Y_L, Delta_Y_H, SQUAL, Raw Data_Sum, Maximum_RawData, Minimum_RawData, Shutter_Upper and Shutter_Lower registers. See Burst Mode-Motion Read section 6.7 for use details.							

8.2.15 POWER_UP_RESET

Register Name	POWER_UP_RESET							
Address	0x3A							
Access	Write			Reset Value		NA		
Bit	7	6	5	4	3	2	1	0
Field	$PRST_7$	$PRST_6$	$PRST_5$	$PRST_4$	$PRST_3$	$PRST_2$	$PRST_1$	$PRST_0$
Description	Write 0x5A to this register to reset the chip and all settings will revert to default values. Reset is required after recovering from Shutdown mode.							

8.2.16 SHUTDOWN

Register Name	SHUTDOWN							
Address	0x3B							
Access	Write			Reset Value		NA		
Bit	7	6	5	4	3	2	1	0
Field	SD_7	SD_6	SD_5	SD_4	SD_3	SD_2	SD_1	SD_0
Description	Write 0xB6 to set the chip to Shutdown mode. Refer to the Shutdown section for more details on recovery procedure.							

8.2.17 PERFORMANCE

Register Name	PERFORMANCE							
Address	0x40							
Access	Read/Write			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	AWAKE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Description

This register configures the operating mode of the chip.

Field Name	Description
AWAKE	**0: Enable Rest Mode** 1: Disable Rest Mode

8.2.18 CONFIG1

Register Name	CONFIG1							
Address	0x4D							
Access	Read/Write			Reset Value		0x90		
Bit	7	6	5	4	3	2	1	0
Field	CON	1	Reserved	1	Reserved	Reserved	Reserved	Reserved

Description

This register configures the dpi step size of the chip. Upon chip start-up per the recommended Power-Up Sequence, the chip is set to 50cpi step size as default.

Field Name	Description
CON	Change dpi step size 0 = 50 dpi **1 = 100 dpi**

8.2.19 RESOLUTION

Register Name	RESOLUTION							
Address	0x4E							
Access	Read/Write			Reset Value		0x12		
Bit	7	6	5	4	3	2	1	0
Field	RES_7	RES_6	RES_5	RES_4	RES_3	RES_2	RES_1	RES_0

Description

This register set the chip resolution, the approximate resolution value for each register setting can be defined using the table shown below. The maximum resolution setting of 50cpi step size is 10000cpi, configure the chip to 100cpi step size in order to select up to 19000cpi. Please note that upon chip start-up per the recommended Power-Up Sequence, the chip is set to 3000cpi and 50cpi step size as default.

Note: Recommend to set bit-7 in RIPPLE_CONTROL register to enable the ripple control when select resolution of 5000cpi and above.

Field Name	Description
$RES_{7:0}$	To select chip resolution from 50cpi to 10000cpi, write register 0x4D with value 0x50 to set the step size of approximately 50cpi. 0x00: 50cpi 0x01: 100cpi 0x02: 150cpi : **0x3B: 3000cpi (default)** : 0xC7: 10000cpi To select chip resolution from 10100cpi to 19000cpi, write register 0x4D with value 0xD0 to set the step size of approximately 100cpi. 0x64: 10100cpi 0x65: 10200cpi 0x66: 10300cpi : 0xBD: 19000cpi (max)

8.2.20 ANGLE_SNAP

Register Name	ANGLE_SNAP							
Address	0x56							
Access	Read/Write			Reset Value		0x04		
Bit	7	6	5	4	3	2	1	0
Field	EN	0	0	0	0	1	0	0
Description	Write to this register to enable angle snap feature. Field Name: EN — Description: 0: Angle snap disable; 1: Angle snap enable							

8.2.21 RAWDATA_GRAB

Register Name	RAWDATA_GRAB							
Address	0x58							
Access	Read/Write			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved	$RAWDATA_6$	$RAWDATA_5$	$RAWDATA_4$	$RAWDATA_3$	$RAWDATA_2$	$RAWDATA_1$	$RAWDATA_0$
Description	This register contains the raw data levels when the Raw Data Grab process is enabled. For details of the Raw Data Grab process please refer to section 7.0.							

8.2.22 RAWDATA_GRAB_STATUS

Register Name	RAWDATA_GRAB_STATUS							
Address	0x59							
Access	Read			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	PG_VALID	PG_FIRST	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Description	This register provides additional information for user to monitor the chip navigation status. Field Name: PG_VALID — Description: 1 = Raw Data Grab valid Field Name: PG_FIRST — Description: 1 = Raw Data Grab first							

8.2.23 RIPPLE_CONTROL

Register Name	RIPPLE_CONTROL							
Address	0x5A							
Access	Read/Write			Reset Value		0x10		
Bit	7	6	5	4	3	2	1	0
Field	EN	Reserved	Reserved	1	Reserved	Reserved	Reserved	Reserved
Description	Set bit-7 to enable ripple control.							

Field Name	Description
EN	**0: Ripple Control Disable.** 1: Ripple Control Enable.

8.2.24 AXIS_CONTROL

Register Name	AXIS_CONTROL							
Address	0x5B							
Access	Read/Write			Reset Value		0x60		
Bit	7	6	5	4	3	2	1	0
Field	Swap_XY	INV_Y	INV_X	Reserved	Reserved	Reserved	Reserved	Reserved
Description	The register set the axis direction of the chip reporting.							

Field Name	Description
Swap_XY	1: Swap XY directions
INV_Y	1: Invert Y direction
INV_X	1: Invert X direction

8.2.25 INV_PROD_ID

Register Name	INV_PROD_ID							
Address	0x5F							
Access	Read			Reset Value		0xB1		
Bit	7	6	5	4	3	2	1	0
Field	$IPID_{7-0}$							
Description	This register value is the inverse of the Product_ID register value. It is used to test the SPI port hardware.							

8.2.26 RUN_DOWNSHIFT

Register Name	RUN_DOWNSHIFT							
Address	0x77							
Access	Read/Write			Reset Value		0x0C		
Bit	7	6	5	4	3	2	1	0
Field	RD_7	RD_6	RD_5	RD_4	RD_3	RD_2	RD_1	RD_0
Description	This register set the Run to Rest1 downshift time. Use the formula below for calculation. Run Downshift time (ms) = RD[7:0] x RUN_DOWNSHIFT_MULT (default 256) x 80.77us Example for 12k FPS = 49 x 256 x 80.77us = 1s (default) Please note that upon chip start-up per the recommended Power-Up Sequence, RD[7:0] is set to 49 as default. Max Downshift time is 189 x 256 x 80.77us = 3.9s Min value is 0x01. A value of 0x00 will be internally clipped to 0x01. All the above values are expected to have +/- 10% tolerance.							

8.2.27 REST1_PERIOD

Register Name	REST1_PERIOD							
Address	0x78							
Access	Read/Write			Reset Value		0x01		
Bit	7	6	5	4	3	2	1	0
Field	$R1R_7$	$R1R_6$	$R1R_5$	$R1R_4$	$R1R_3$	$R1R_2$	$R1R_1$	$R1R_0$
Description	This register set the Rest1 period Rest1 period = R1P[7:0] x 1ms Default Rest1 period = 1 x 1ms = 1ms Min value is 0x01. A value of 0x00 is invalid. All the above values are expected to have +/- 10% tolerance.							

8.2.28 REST1_DOWNSHIFT

Register Name	REST1_DOWNSHIFT							
Address	0x79							
Access	Read/Write			Reset Value		0x4F		
Bit	7	6	5	4	3	2	1	0
Field	$R1D_7$	$R1D_6$	$R1D_5$	$R1D_4$	$R1D_3$	$R1D_2$	$R1D_1$	$R1D_0$
Description	This register set the Rest1 to Rest2 downshift time. Use the formula below for calculation. Rest1 Downshift time (ms) = R1D[7:0] x REST1_DOWNSHIFT_MULT (default 256) x REST1 period (default 1ms) Default = 79 x 256 x 1ms = 20224ms = 20s Min value is 0x01. A value of 0x00 will be internally clipped to 0x01. All the above values are expected to have +/- 10% tolerance.							

8.2.29 REST2_PERIOD

Register Name	REST2_PERIOD							
Address	0x7A							
Access	Read/Write			Reset Value		0x08		
Bit	7	6	5	4	3	2	1	0
Field	$R2P_7$	$R2P_6$	$R2P_5$	$R2P_4$	$R2P_3$	$R2P_2$	$R2P_1$	$R2P_0$
Description	This register set the Rest2 period Rest2 period = R2P[7:0] x 4ms Default Rest2 period = 8 x 4ms = 32ms Min value is 0x01. A value of 0x00 is invalid. All the above values are expected to have +/- 10% tolerance.							

8.2.30 REST2_DOWNSHIFT

Register Name	REST2_DOWNSHIFT							
Address	0x7B							
Access	Read/Write			Reset Value		0x4A		
Bit	7	6	5	4	3	2	1	0
Field	$R2D_7$	$R2D_6$	$R2D_5$	$R2D_4$	$R2D_3$	$R2D_2$	$R2D_1$	$R2D_0$
Description	This register set the Rest2 to Rest3 downshift time. Use the formula below for calculation. Rest2 Downshift time (ms) = R2D[7:0] x REST2_DOWNSHIFT_MULT (default 256) x rest2_period (default 32ms) Default = 74 x 256 x 32ms = 606.208s = 10 min Min value is 0x01. A value of 0x00 will be internally clipped to 0x01. All the above values are expected to have +/- 10% tolerance.							

8.2.31 REST3_PERIOD

Register Name	REST3_PERIOD							
Address	0x7C							
Access	Read/Write			Reset Value		0x3F		
Bit	7	6	5	4	3	2	1	0
Field	$R3P_7$	$R3P_6$	$R3P_5$	$R3P_4$	$R3P_3$	$R3P_2$	$R3P_1$	$R3P_0$
Description	This register set the Rest3 period Rest3 period = R3P[7:0] x 8ms Default Rest3 period = 63 x 8ms = 504ms Min value is 0x01. A value of 0x00 is invalid. All the above values are expected to have +/- 10% tolerance.							

8.2.32 RUN_DOWNSHIFT_MULT

Register Name	RUN_DOWNSHIFT_MULT							
Address	0x7D							
Access	Read/Write			Reset Value		0x07		
Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Reserved	RUN_M_3	RUN_M_2	RUN_M_1	RUN_M_0

Description

This register set the Run Downshift Multiplier. (Refer to the formula in Register RUN_DOWNSHIFT)

Field Name	Description	
$RUN\_M_{0:3}$	Hex	RUN_DOWNSHIFT_MULT
	0x0	2
	0x1	4
	0x2	8
	0x3	16
	0x4	32
	0x5	64
	0x6	128
	0x7	256 (default)
	0x8	512
	0x9	1024
	0xA	2048

8.2.33 REST_DOWNSHIFT_MULT

Register Name	REST_DOWNSHIFT_MULT							
Address	0x7E							
Access	Read/Write			Reset Value		0x77		
Bit	7	6	5	4	3	2	1	0
Field	Reserved	$REST\_M_6$	$REST\_M_5$	$REST\_M_4$	Reserved	$REST\_M_2$	$REST\_M_1$	$REST\_M_0$

Description

This register set the REST Downshift Multiplier. (Refer to the formula in Register REST1_DOWNSHIFT and REST2_DOWNSHIFT)

Field Name	Description	
$REST\_M_{0:2}$	Hex	REST2_DOWNSHIFT_MULT
	0x0	2
	0x1	4
	0x2	8
	0x3	16
	0x4	32
	0x5	64
	0x6	128
	0x7	256 (default)
$REST\_M_{4:6}$	Hex	REST1_DOWNSHIFT_MULT
	0x0	2
	0x1	4
	0x2	8
	0x3	16
	0x4	32
	0x5	64
	0x6	128
	0x7	256 (default)

8.3 Bit Masks for Register Write

Special precaution needs to be taken for some of the registers have “Reserved” bit. In order to overwrite specific bits in the register, one need to read and store its current value first, then apply bit masking and write back the new value into the register. This is accomplished by using bitwise operators such as AND(&), OR(|), or INVERSE(~).

Example:

To disable the Rest Mode in Register 0x40 (set bit-7 to 1)

Read register 0x40 and store in VarA

VarA |= 0x80

Write register 0x40 with value VarA

To enable the Rest Mode in Register 0x40 (set bit-7 to 0)

Read register 0x40 and store in VarA

VarA &= ~ 0x80

Write register 0x40 with value VarA

Document Revision History

Revision Number	Date	Description
0.80	31 Jan 2020	Initial creation
0.81	17 July 2020	Pg 23 – added a note in section 5.2 Pg 26 – removed step 109 and correction on step 18 in power up sequence Pg 41 – added Lift_Stat bit into Motion register Pg 46 – updated description of *CHIP_OBSERVATION* Pg 48 – updated register 0x4D Pg 49 – updated description of *RESOLUTION* Pg 37 – correction on step 7 in section 7.5.1
1.0	28 Sep 2020	Pg 11,12,35 – added Corded Gaming Mode Pg 1, 11, 23, 37- added L0AE-LSI1