***** Valued Customer: If this stackup is accepted, please add this PDF to the production data package *****

Job number:	LD10651	**Material:**	PCL-370HR
Part number:	ISEELOC 8 LAYER STACK UP	**Impedance:**	Yes
Customer:	GORILLA CIRCUITS INC.	**Date:**	14-May-2020
Panel size:	16X18	**Created by:**	LERBI.DELEON

Stackup Report

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GORILLA CIRCUITS INC.

Layer	Type	CU Weight	CU %	Material Description	Via Structure	Segment	Glass Style	Material Family	Copper Plating Thickness [mil]	Thickness after lamination [mil]
Soldermask										0.80
L1	Signal	H	100			Foil			1.40	2.00 *
				Press thk = 6.22 mil		Prepreg	2113(59)	PCL-370HR		6.22
							106(76)	PCL-370HR		
L2	Plane	H	70							0.60
				4.0 mil H/H		Core		PCL-370HR		4.00
L3	Mixed	H	40							0.60
				Press thk = 4.26 mil		Prepreg	106(76)	PCL-370HR		4.26
							106(76)	PCL-370HR		
L4	Plane	H	70							0.60
				3.0 mil H/H		Core		PCL-370HR		3.00
L5	Signal	H	25							0.60
				Press thk = 3.10 mil		Prepreg	2113(59)	PCL-370HR		3.10
L6	Signal	H	25							0.60
				3.0 mil H/H		Core		PCL-370HR		3.00
L7	Plane	H	70							0.60
				Press thk = 4.26 mil		Prepreg	106(76)	PCL-370HR		4.26
							106(76)	PCL-370HR		
L8	Mixed	H	40							0.60
				4.0 mil H/H		Core		PCL-370HR		4.00
L9	Plane	H	70							0.60
				Press thk = 6.22 mil		Prepreg	106(76)	PCL-370HR		6.22
							2113(59)	PCL-370HR		
L10	Signal	H	100			Foil			1.40	2.00 *
Soldermask										0.80

*** Estimated Cu Plating for reference use only.**

Specification (Over mask on plated copper:):	mil
Overall Board Thickness:	39.37
Tolerance:	+4.0/-4.0
Min-Max Board Thickness:	35.4-43.4

Anticipated Board Thickness:	mil
After lamination:	44.06
Over mask on plated copper::	48.46

Impedance Table

Layer	Impedance Requiremnt [ohms]	Tolerance [ohms] +	Tolerance [ohms] -	Type	Upper Ref	Lower Ref	Designed Line Width [mil]	Plotted Line Width [mil]	Designed Spacing [mil]	Coplanar Spacing [mil]	Finished Line Width [mil]	Finished Spacing [mil]	Impedance Simulation [ohms]
L1	50	5.0	5.0	Coated microstrip SE	--	L2	10.50	11.25	--	--	10.50	--	49.8
L1	50	5.0	5.0	Coated microstrip SE	--	L3	18.00	18.75	--	--	18.00	--	50.4
L3	50	5.0	5.0	Single-Ended	L4	L2	3.50	4.00	--	--	3.50	--	49.4
L3	90	9.0	9.0	Differential	L4	L2	4.00	4.50	5.00	--	4.00	5.00	90.5
L8	50	5.0	5.0	Single-Ended	L7	L9	3.50	4.00	--	--	3.50	--	49.4
L8	90	9.0	9.0	Differential	L7	L9	4.00	4.50	5.00	--	4.00	5.00	90.5
L10	50	5.0	5.0	Coated microstrip SE	--	L9	10.50	11.25	--	--	10.50	--	49.8
L10	50	5.0	5.0	Coated microstrip SE	--	L8	18.00	18.75	--	--	18.00	--	50.4

Remarks:

Please Note: The stackup may change if the final manufacturing data is different from the information used to create this stackup

Mat Typ	Material Description	Rsn%	PNL	1 Pnl	Notes
Foil	Foil - 0.5 oz - Foil		16x18	2	
Core	PCL-370HR - 3.0 mil H/H		16x18	2	
Core	PCL-370HR - 4.0 mil H/H		16x18	2	
Prepreg	PCL-370HR - 106	76%	16x18	6	
Prepreg	PCL-370HR - 2113	59%	16x18	3	

Drill Progs	Technology	Depth
Drill1	Mechanical	44.06

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Please Note:

IPC-6012 has a minimum dielectric requirement of 0.003543" and any targeted dielectric thickness of 0.0045" or less may violate this requirement.

Acceptance of this proposed stack-up will be taken as a waiver for this requirement. Note that with this exception, the minimum dielectric thickness shall be 0.000984". If this is not acceptable please get back to us ASAP so we can make the necessary changes.

Note that the granting of this waiver does not affect the product meeting IPC-6012 Class 2 or Class 3 requirements. Also note that targeted thickness .0046" and greater shall have a minimum tolerance of +/-.001 after lamination.