

The accuracy of IEEE 1588 time synchronization protocol and its improvement

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Abstract — Among the technologies of intelligent substation, the accuracy of time synchronization plays an important role in the information collecting, fault analyzing, detection controlling. The IEEE 1588 time synchronization protocol enables the accuracy of sub-microsecond, and plays an important role in the packet-based network synchronization mechanism, which becomes the ideal choice to realize the accurate network time synchronization of substation. In this paper, the realization mechanism of IEEE 1588 protocol is introduced first, and on that basis, the main accuracy influencing factors of the protocol are analyzed. Aiming at the influencing factors such as the time offset between master and slave clock, the network delay caused by the packet line up mechanism, the switch and generating position of time stamp, the specific methods to reduce or eliminate the influence and further improve the synchronization accuracy are proposed. The research results could provide theory references for the accuracy improving of IEEE 1588 time synchronization protocol.

Keywords — IEEE 1588, time synchronization, accuracy analyzing, improving methods.

I. INTRODUCTION

With the gradual and further research of IEC61850 standard, the intelligent substation has become the development of substation automation technology. Different from the electromagnetic voltage and current transformers used in Process Level in traditional substation, the devices in intelligent substation process level are replaced by electronic voltage and current transformers, which has put the sampling link forward and the information are picked up from the sampling devices and transmitted to emerging unit, which causes the problem of sampling synchronization. To build a centralized and accurate time standard and synchronize all the nodes in the substation, is an essential guarantee and premise to maintain the substation safety, steady and economic operation^[1].

For distributed network time synchronization, there have been many mature methods such as NTP(network time protocol) and SNTP(simple network time protocol), and the latter is the simplified standard of the former. The IEC 61850 standard divides the synchronization accuracy into 5 classes(T1-T5)^[2], in certain network structure the synchronization accuracy of NTP can achieve T1 class(1ms), while its wide field synchronization error is 10~100ms. Several synchronization technologies have been developed in last decades such as IRIG-B, LORAN-C, NTP, GPS-based synchronization and SyncE. However, they

are not suitable for application fields where a precise time system is required with low costs. GPS(Global Positioning System) is used a lot in substation automation system and it synchronizes the nodes using impulse signal through cable connections, which has the advantage of high accuracy and low cost, but it requires that cable connection and that does not coincide with the trend of intelligent substation^[3]. With Precision Time Protocol (PTP), sub-microsecond accuracy can be reached with minimal network, computing and hardware resource requirements. For all that, PTP as defined in the IEEE 1588 standard is becoming the most feasible solution for many applications where a precise time synchronization is required. The IEEE 1588 protocol released in 2002 is a high precision time protocol used for measuring and automation, and it achieves the accuracy of sub-microsecond^[4] which satisfies the need of T5 class for process level measurement. The sending mechanism of IEEE 1588 protocol is based on UDP/IP, it adds time stamp with hardware and does not need extra cable connection, which makes it especially suitable for internet application.

In view of the trend that IEEE 1588 protocol is to become the main method for digital substation synchronization, the principle of its time synchronization is introduced first in this paper. On that basis, the main influencing factors of IEEE 1588 protocol synchronization accuracy are studied and the effective methods to improve the accuracy are proposed aiming at each influencing factor. The research results are positive references to promote the IEEE 1588 protocol synchronization accuracy.

II. PRINCIPLE OF IEEE 1588 PROTOCOL

The time synchronization of IEEE 1588 protocol is achieved by send message between master and slave clocks. The clocks in the network are divided into master and slave clocks^[5], while the master clock is determined by comparing the clock quality supplied by each PTP port. When the master clock is determined, the slave clock is revised by computing the offset between master and slave clocks and the network delay, the realization mechanism is shown in Fig. 1.

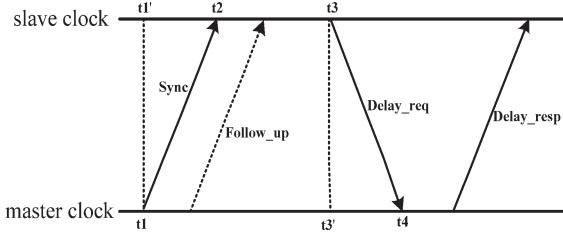


Fig. 1 Principle of IEEE 1588 Protocol

The specific steps are as follows:

Step 1: at the time of t_1 (based on master clock), the master clock send periodic Sync message to slave clock. Assume that the local time of slave clock when the message is sent is t_1' , and the time when the message is received is t_2 ;

Step 2: the master clock sends Follow_up message to slave clock, which contains the accurate time of t_1 when the Sync message is sent. The slave clock marks the time stamp when it receives Follow_up message;

Step 3: at the time of t_3 (based on slave clock), the slave clock send Delay_req message to master clock by unicast transmission, and marks the sending time stamp. Assume that the local time of master clock is t_3' when the Delay_req message is sent, local time of master clock is t_4 when the Delay_req message is received;

Step 4: the master clock sends Delay_resp message to slave clock, and the message contains the time stamp when the master clock receives Delay_req message.

Therefore, the slave clock obtains four time stamps: t_1, t_2, t_3, t_4 . Suppose that the time offset between master and slave clock is constant, and the transmission time delays from the message being sent to received are equal, and they are named t_{offset} 、 t_{delay} respectively.

From the analysis above we can obtain that:

$$t_{\text{offset}} = t_1' - t_1 = t_3 - t_3' \quad (1)$$

$$t_{\text{delay}} = t_2 - t_1' = t_4 - t_3' \quad (2)$$

The sum and difference of the equations above are as follows:

$$\begin{cases} t_{\text{offset}} + t_{\text{delay}} = t_2 - t_1 \\ t_{\text{offset}} - t_{\text{delay}} = t_3 - t_4 \end{cases} \quad (3)$$

Further, the offset between master and slave clock and the transmission time delays from the message being sent to received can be obtained from the equation above:

$$\begin{cases} t_{\text{offset}} = \frac{(t_2 - t_1) + (t_3 - t_4)}{2} \\ t_{\text{delay}} = \frac{(t_2 - t_1) - (t_3 - t_4)}{2} \end{cases} \quad (4)$$

The equation (4) indicates that as long as the time stamps t_1, t_2, t_3, t_4 are obtained, the offset and time delay can be calculated using equation (4), and then the

time compensation can be made to synchronize the time master and slave clock.

III. THE INFLUENCING FACTORS OF SYNCHRONIZATION ACCURACY

From the model and assumption aforementioned, we can see that the influencing factors of synchronization accuracy mainly includes the steady of the time offset between master and slave clock, the symmetry of the transmission time delay and the accuracy of the time when adding stamp. These influencing factors will be analyzed to improve the synchronization accuracy of IEEE 1588 protocol.

A. The time offset between master and slave clock

Generally, as the standard clock in the whole network, GPS、Beidou satellite positioning system and atomic clock are usually adopted as master clock^[6]. The synchronization error of master clock is usually within dozens of nanoseconds, and its influence on the synchronization accuracy is small. Comparatively, the slave clock is usually quartz oscillator, whose accuracy is influenced by manufacture techniques, temperature, and time aging, thus resulting in error accumulating. The frequency adjustment process is responsible for adjusting the slave clock the same speed as in the master by sending a continuous flow of Sync messages from master to slave. Since oscillators may slightly change due to environmental factors for example, Sync messages are continuously sent at a constant rate and the slave clock is controlled by a system that accelerates or slows the clock period. The temperature error index of a typical quartz oscillator is $1 \times 10^{-6} \text{ s}/^\circ\text{C}$, while the default transmission interval of Sync message is 2s^[7], so the synchronization error caused by clock oscillating within one message interval is 2us when the temperature changes 1°C . In the link circuit of IEEE 1588 synchronization, the master clock is the upstream of the link, and its oscillating accuracy will influence the synchronization of the whole system.

B. The time delay of network transmission

In the model assumption the transmission time delays from the message being sent to received are considered to be equal, while actually they are not the same due to the different network loads, the asymmetric transmission paths and other factors^[8]. The network delay mainly includes several parts as follows:

- 1). message sending time delay T_0

Message sending time delay is the time from the first to the last bit of the message being sent. It is proportional to the length of the message (FS), and reciprocal to the sending speed(BR):

$$T_0 = FS / BR \quad (5)$$

Assume that the length of the message is 60B, the message sending time delay for 100M and 1000M sending speed switch are respectively as follows:

$$T_0(100M) = 60 \times 8bit / (100 \times 10^6 bit/s) = 4.8\mu s \quad (6)$$

$$T_0(1000M) = 60 \times 8bit / (1000 \times 10^6 bit/s) = 0.48\mu s \quad (7)$$

2). inherent time delay of the switch T_1

The message transmission passes through the storage of the circuit hardware, retransmission MAC address, virtual local network VLAN and the processing and conversion of other logical functions. These processes will inevitable delay the information sending. 《The Technology Standard of Network Switch-qwd429-2010》 requires that the inherent time delay of the switch should be less than 10us when sending all kinds of message. Currently this index is less than 4us in intelligent substation.

3). transmission time delay in the line T_1

When the message transmits in the optical line, its speed is nearly two-thirds the speed of light. For short distances optical line, the transmission time delay can be ignored. For example, when the optical line is 100m, the transmission time delay is calculated as:

$$T_2(100m) = 100m / (3 \times 10^8 m/s \times 2/3) = 0.5\mu s \quad (8)$$

Therefore, the influences of short distance optical line on synchronization accuracy can be omitted.

4). the packet line up mechanism delay T_3

In the broadcast Ethernet transmission mechanism, the message transmission usually encounters frame conflict. In order to eliminate such phenomenon, the packet line up mechanism is adopted to storage the messages first and then send them in line. However, the line up mechanism is influenced by the length of the packet, network flow and other factors, which results in the uncertainty of transmission delay. The line up mechanism is an important reason for the jitter of network delay.

5). the number of layers of the switch

The adding of each switch layer will lead to the increase of data transmission link, thus increasing the network transmission time delay.

C. The accuracy of time stamp

When the master clock sends the Sync message, the slave clock marks the arrival of the Sync message with its local time. Then the slave clock compares it with the actual Sync transmission time stamp in the master clock's Follow_up message. The difference between the two time stamps represents the sum of the offset of the slave and the message transmission delay. The second set of messages is necessary to account for variations in network delays. The slave clock then marks the time stamp when a Delay_req message is sent. The master clock receives the arrival of the delay request message and then sends a Delay_resp message with the delay

request arrival timestamp. The difference between the timestamps is the slave-to-master delay. As shown in equation (3) and (4), the accuracy of the time stamp will directly influence the synchronization accuracy of the whole internet protocol. In the realization of PTP system, the accuracy of time stamp depends on its generating process^[9]. Fig 2. Illustrates the two generating positions of time stamp

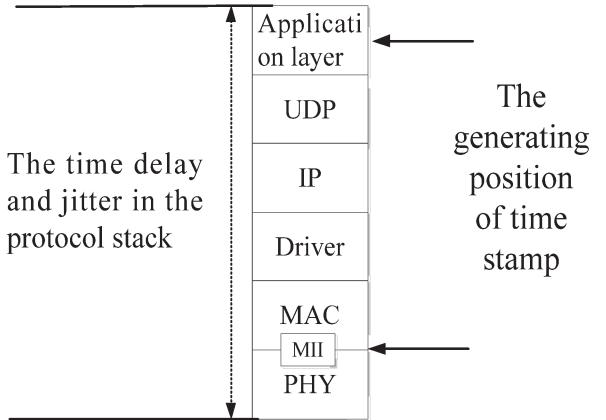


Fig 2. The generating position of time stamp

In the figure above, if the time stamp is generated and identified in application layer, the synchronization message including application layer time stamp will be packed through UDP, and then the data will be added prefix and suffix to generate IP packet, finally sent out to the switch through the physical ports. The advantage of the such method is that it can be realized by software and greatly reduce the cost of the system. However, it also inevitably involves the time delay and jitter of the stack, and further influences the synchronization accuracy of the whole system. To maximize the synchronization accuracy, the time stamps must be generated at the point of minimum jitter. Network protocol stack jitter is known to be about 3 ms, while it is too large to permit sub-microsecond timing^[10]. The more accurate method is to detect the synchronization message by hardware detecting, and add the time stamp at the MII(Media Independent Interface) between MAC layer and PHY layers. This position is the most close to the entrance of data packet and the jitter time is minimized to nanosecond level, and enormously improves the synchronization accuracy. But this method can only be realized by hardware system and costs more than software method^[11].

IV. MEASURES TO IMPROVE THE SYNCHRONIZATION ACCURACY

In section III the influencing factors of IEEE 1588 protocol has been discussed and analyzed. The specific measures to reduce the synchronization error aiming at each influencing factor will be given as follows:

1. Aiming at the time offset between master and slave clock, time compensation(according to the timekeeping difference between master and slave clock, the timing error of slave clock can be revised by the pulse per second of master clock) can be made to reduce the timing difference between them within an synchronization message interval. In addition, the message interval can be also shortened to reduce the accumulated timing error if the network flow allows. Moreover, the high accurate quartz oscillator(such as temperature constant) can be chosen as the slave clock to guarantee the coincidence of timekeeping between master and slave clock. It should be noted that the high accurate oscillators are usually costly. Therefore, compromise should be made between the synchronization message interval, the steady and price of the oscillator, the compensation technology of the oscillating under the requirement of synchronization accuracy.

2. For the transmission time delay of the network, faster transmission speed switch can be chosen to transmit the synchronization message or reduce the switch layer reasonably. Since the line up mechanism is the major reason for the network jitter and delay, the data priority can be set to send the synchronization message at the highest priority, so that the message can be stored and processed earliest. Besides, a novel method named “boundary clock” can be introduced to reduce the time delay. The schematic diagram of boundary clock is shown in Fig. 3. A boundary clock (BC) is an IEEE 1588 component that allows the synchronization of IEEE 1588 clocks across subnets defined by a router or bridges that blocks the transmission of all PTP messages. A BC serves to eliminate the large fluctuations in communication latency typically generated by bridges. To realize time synchronization with PTP for a line topology the BC must be used. The oscillator of the local clock within a BC will be regulated by the PTP slave functionality. The corrected local clock of the BC will be used as the master clock for the next network segment. This procedure will be repeated until reaching the time client. In this way a cascade of control loops will be generated. Chains of control loops tend to be unstable. Because of the importance of the line topology at the field level of industrial automation system it is necessary to examine a further synchronization element beside the already standardised IEEE 1588 synchronization elements, which we call a Bypass Clock.

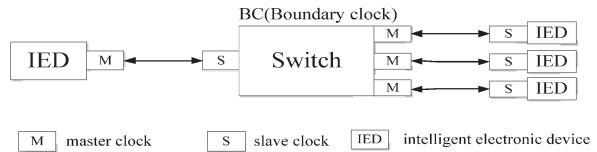


Fig. 3 Schematic diagram of boundary clock in the network

3. In order to improve the time stamp generating accuracy, the time stamp should be generated by hardware and close to the physical layer, so that it could precisely reflect the transmission time of the synchronization message, and then the stamp will be added to the following message. In general, the most accessible point of minimum jitter is the interface between the physical and the MAC layers. Meanwhile, in the realization of the system, the clock regaining and interference suppression circuit functions can be added to achieve higher synchronization accuracy.

V. EXPERIMENT

To examine the synchronization accuracy of IEEE 1588 protocol, the experiment of the protocol accuracy was carried out and the schematic diagram was shown in Fig. 4. When the data is transmitted in SV netting mode, the synchronization pulse is uploaded to MU(merging unit) via the switch. By comparing the time between master clock and the rising edge of MU, the time skewing can be tested and further the synchronization accuracy can be calculated.

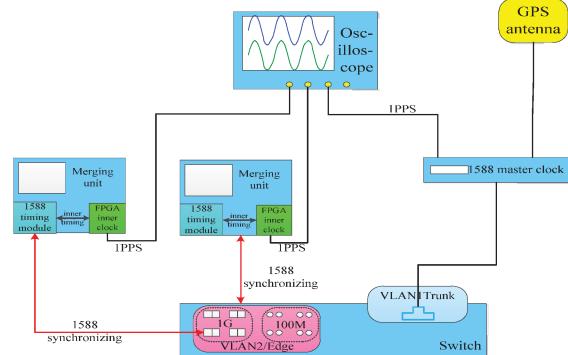


Fig. 4 Schematic diagram of synchronization accuracy test of IEEE 1588

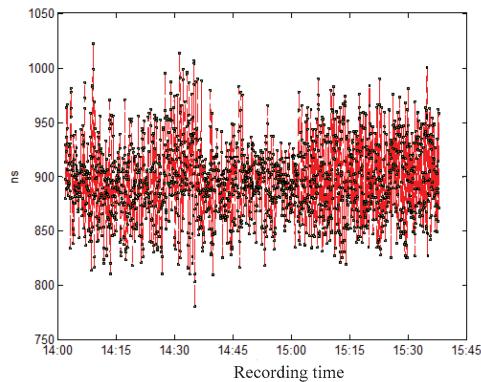


Fig. 5 Time accuracy of IEEE 1588

Fig. 5 illustrates the synchronization accuracy of IEEE 1588 protocol. As we can see, the experiment lasts two hours and the synchronization skewing is mainly between 800-1000ns, which coincides with the accuracy requirements of the protocol.

VI. CONCLUSION

As a network synchronization protocol achieving the accuracy of sub-microsecond, the IEEE 1588 protocol is of important significance to the building of intelligent substation. In this paper, the main principle of IEEE 1588 is introduced and the message transmission process is analyzed to study the influences of each factor on the synchronization accuracy. Aiming at the time offset between master and slave clock, the transmission time delay and the generating position of time stamp, their influences on the synchronization accuracy and the measures to reduce or eliminate such influences are studied. The research results provide theoretical references to the engineering application of IEEE 1588 protocol.

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