A Discussion On Chiplets

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Abstract:

Tradition SoC has now been facing huge challenges with the slow down of Moore's Law. The more complicated chip design creates problems for chip manufacturers as the yield rate of a single die has drastically reduced due to the sophisticated manufacturing process, especially during the process of lithography.Moreover, the power consumption of a single die SoC cause enormous issues for large companies who rely on computing powers. Therefore, a new concept of design, known as Chiplets design, is introduced by researchers and are widely investigated by institutes and applied by many SoC design companies along with chip manufacturers.The advantage of production and design motivates many innovations on such approach, but it still faces practical problems that need to be addressed if further applications are to be anticipated in the next decade with the development of semiconductor materials. In this paper, the chiplets integration topology will be discussed with the focus on one specific paper and some other papers will also be referenced to demonstrate the development of chiplets technology and its current challenges.

Literature review:

In this paper, the article "Chiplet Heterogeneous Integration Technology-Status and Challenges"[1] will be heavily analyzed. Firstly, it provides the background as this paper mentioned in the abstraction section that the compelling reasons for the development of Chiplets

design are the slowdown of Moore's Law and the cost of manufacturing of the sophisticated design.The traditional Soc design will soon reach its limits as the scale of the chip is approaching 1nm, which would cause the quantum tunnel effect to happen. What's more, The complicated design requires more transistors to be built in a small area that would trigger the possible problem of defection on die or unpredictable power consumption.Any defection on a single die would hugely slow down the production time line, and it will cause big financial burdens for companies that such problem will have potentials to bankrupt companies.Hence, many chip design giants, such as AMD, have already introduced the chiplets design methodology in their products and such design has swiftly taking over the market.

To clearly illustrate the chiplets design, one paper[2] shows the basic idea of it.

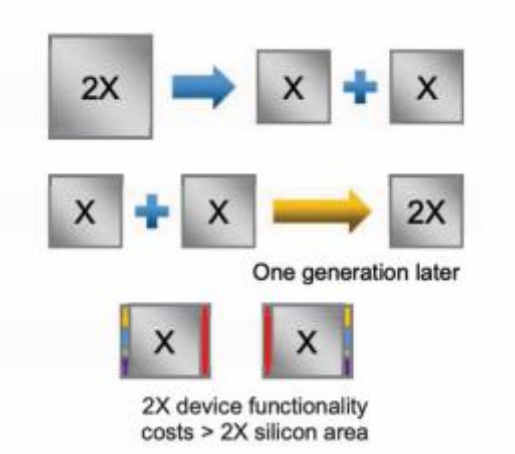

Figure 1..G. H. Loh, S. Naffziger, and K. Lepak, "Understanding Chiplets Today to Anticipate Future Integration Opportunities and Limits," in *2021 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Grenoble, France: IEEE, Feb. 2021, pp. 142–145. doi: 10.23919/DATE51398.2021.9474021.

The main idea of chiplets design is to use the methodology in coding as "divide and conquer". That is to divide one single monolithic die into smaller pieces and to achieve the

functionalities individually by using a common central unit which is integrated on a PCB board.Secondly, the authors assert that one of the problems needs to be addressed for chiplets design is that EDA tools and design-related ecological system need to have a standard, because it will prevent unregulated development and create a guideline for future developers and researchers. The paper address the advantages of chiplets design in several ways such technology advancement, development cost of chiplets design and business enhancement.

But this paper also addresses challenges that need to be solved. One of the main problems is the universal standard for all chiplets design related entities, as the world should not see unregulated and unordered development of chiplets design, because it will largely waste resources and drag down any improvements and innovations on such technology.Secondly, the interface interconnecting each unit must be reliable. Since chiplets design utilizes multiple cores built on boards, the common central unit which controls the in flow and out flow of data must be able to coordinate each sub unit.Any flaws in the central control unit will destroy the reliability of data stored in sub units and the entire design will be thrown out.Lastly, the packaging technology needs to be improved as chiplets design contains several units and it would be a challenge to put all units together.

Analysis of ChatGPT outcome:

After asking ChatGPT to write a paper about chiplets design, some key outcomes have been highlighted. ChatGPT points out almost every feature that the paper has pointed out. The advantages of chiplets design are the scalability , cost, and yield rates, while the challenges are standardization,power consumption and interconnect capabilities.ChatGPT also points out the

key technologies behind the chiplets design,such as the heterogeneous integration,packaging and assembly and interconnection technologies. It is easy to conclude that the paper in the literature review section provides a great scope of chiplets design.Lastly in the paper, ChatGPT gives out examples on the applications of chiplets design on building data center and enhancing cloud computing capabilities, along with producing more complicated consumer and commercial oriented products.

Proposal of Chiplets Design:

1. Focus on enhancing the computing capabilities. Commercial oriented design should be the priority of such design. Consumers don't typically need such design since they won't need such powerful computing powers, but for commercial users or institution users, chiplets design would be a great approach for them to save money on power consumption and annual costs on updating equipment.
2. Companies and research institutions and governments should form an alliance on such design. This alliance should write certain regulations to pave the guidelines for developers ,manufacturing and design companies to conduct such design. Commercial users rely on steady and reliable products that are compatible with older version of design.Therefore initial standards would be vital for the development of Chiplets design.
3. Chiplets design should be an open source project to attract more developers and researchers so that the ecology system would be significant prevailing around the world and resources won't be wasted on building different framework for chiplets design.A universal framework would be ideal for both users and developers.

4. Manufacturers should focus on reducing the production cost of chiplets design so that the development of such design won't be dragged down by the cost and the development of newer version would be swift.

Reference:

[1]T. Li, J. Hou, J. Yan, R. Liu, H. Yang, and Z. Sun, "Chiplet Heterogeneous Integration Technology—Status and Challenges," *Electronics*, vol. 9, no. 4, p. 670, Apr. 2020, doi: 10.3390/electronics9040670.

[2]G. H. Loh, S. Naffziger, and K. Lepak, "Understanding Chiplets Today to Anticipate Future Integration Opportunities and Limits," in *2021 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Grenoble, France: IEEE, Feb. 2021, pp. 142–145. doi: 10.23919/DATE51398.2021.9474021.