Shizhe Yang

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EDUCATIONAL BACKGROUND

Case Western Reserve University 08/2017 – 05/2021

Major: Electrical Engineering

Relevant Coursework: *Electronic Circuits; Semiconductor Electronic Devices; Solid State Electronics I&II; Electronic Analysis& Digital Design; Intro Circuits and Instruments; Integrated Circuits/Electronic Devices; Computer Organization and Architecture;Applied Circuit Design; etc.*

Boston University 09/2021 – 01/2024

Major: Electrical Engineering

Relevant Coursework: *EC500L6: Plasma Engineering and Technologies;EC551:Advanced Verilog EC575:Semiconductor Devices;EC571:VLSI Design;EC605:Computer Engineering Fundamentals;EC574:Physics of Semiconductor Materials;EC578 Fabrication of Integrated Circuits;EC504:Advanced Data Structure;EC500:Principle of Software;*

ACADEMIC EXPERIENCE

Teaching Assistant at Case Western Reserve University Fall 2020 - Spring 2021

Undergraduate Student TA

- For course ENGR210 (Introduction to Circuits and Instruments)

The Design of a Real-time Tracking and Tracing System Based on RFID Fall 2020

Team Leader

- Led a team of 3 to design a tracking and tracing system to monitor people and reduce the spread of COVID-19
- Designed the exterior of the wristband;Studied its relevant interior digital design.
- Designed the functions of the RFID chips, including the record of people's movements, body temperature, etc.
- Ran tests on the functionality of RFID, signal receiver, locating system, data transmitting system, etc.

Fabrication of Integrated Circuits Fall 2023

Student

- Studied and designed a circuit and apply fabrication steps on a wafer.CAD tool used for layout design.
- Full hands on experiment of photoresist coating,post baking,BOE etching,diffusion and deposition,wire bonding.
- Post examination and cleaning after each process,such as photoresist removing,etc.

Chiplet Design Research Fall 2023

Student Under the advisement of Professor Alshaykh

- Studied Chiplets Design.Explored VLSI design and chiplet related CPU,GPU architectures ,pip-lining,etc.
- Research on development of Chiplet Designs, especially in performance,power,and architectures.
- Using gem5 for simulation,written with C++ and Python.

Advanced Verilog Design(FPGA) Fall 2023

Student

- Using FPGA board to create a Enigma machine. Verilog and Python are used on FPGA board.
- Conduct timing analysis and design verification using Xilinx simulation and RLT analysis tools.
- Using Java to create a program for algebra logic synthesis.

RESEARCH EXPERIENCE

The Design of a Wearable Health Monitor Fall 2020-Spring 2021

Researcher under the advisement of Professor Spiegel

- Studied and designed a health monitor to monitor people's heart rate, blood oxygen, respiratory rate, etc.
- Using Multisim to draft preliminary circuit layout.
- Collected data by monitoring people's health conditions and run simulations to test functionalities.

- Use Matlab for simulation.Explored and applied Machine learning techniques.
- Paper published.

Visiting Researcher, Boston University- NISLAB July 2024 - Present

- Project GenSync - a framework written with C++ for synchronizing data across multiple devices

PUBLICATIONS

1.Multi-parameter Health Monitor with Alarm System based on Machine Learning Techniques. *Frontiers in Science and Engineering,Volume 1 Issue 7 ,Pp. 158-165, October 2021.https://doi.org/10.29556/FSE.202110_1(7).0024*

CLUB EXPERIENCE

Flying Club of CWRU 11/2020 – Present

Member

- Participated in club meetings and training regularly; attended flying lectures; studied the knowledge of aircraft
- Held promotional events to attract and recruit new members; studied pilot operation in simulated aircraft cabin
- Student pilot with more than 30 hours time of flight;

Club Soccer of CWRU 2017 – 2021

Member

HONORS& AWARDS

- Dean's List Fall 2017
- Dean's List Spring 2020
- Best Project Award -Chiplets Design Fall 2023

INTERESTS& SKILLS

Languages: Mandarin (Native); English (Fluent);French(Basic)

Programming Language ,Software and Skills:

Java;Verilog:XilinxVivado;Multisim;Ltspice;MatLab;Cadence;C,C++;Python;Assembly:RISC-V,MIPS.Modelsim;VLSI Design;Digital Design;SystemVerilog;

Others: Aviation; Soccer;