



LAB - 05

陳培殷

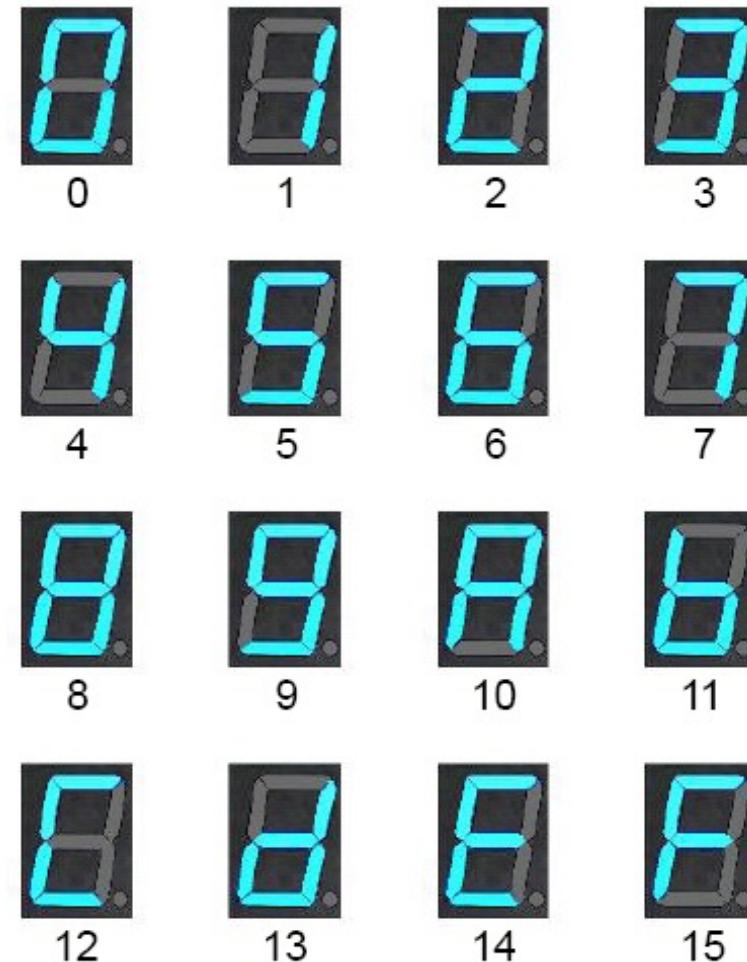
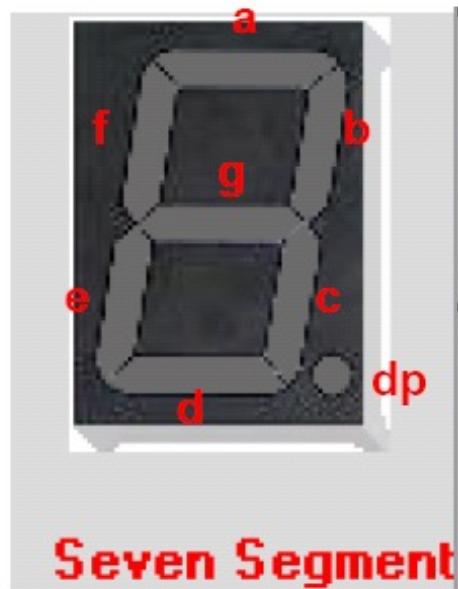
國立成功大學 資訊工程系



Outline

- Video preview for 晶片實現+HDL介紹(Parts I~V)
- Seven segment display
- Lab I – 學號顯示器
- Lab II – 3-bit Adder
- Appendix

Seven-segment display (1/3)



Seven-segment display (2/3)

- 0 is on, 1 is off
- dp is useless in DE0-CV board

- Ex:  out=7'b1000000;

g=1

- Ex:  out=7'b0010010;

b=1, e=1

Seven-segment display (3/3)

- Assign out to seven segment digit pin of FPGA
 - Take seven segment digit 0 as example

Signal Name	FPGA Pin No.	Description	Signal Assigned
HEX00	PIN_U21	Seven Segment Digit 0[0]	out[0]
HEX01	PIN_V21	Seven Segment Digit 0[1]	out[1]
HEX02	PIN_W22	Seven Segment Digit 0[2]	out[2]
HEX03	PIN_W21	Seven Segment Digit 0[3]	out[3]
HEX04	PIN_Y22	Seven Segment Digit 0[4]	out[4]
HEX05	PIN_Y21	Seven Segment Digit 0[5]	out[5]
HEX06	PIN_AA22	Seven Segment Digit 0[6]	out[6]

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- **Lab I – 學號顯示器**
- **Lab II – 3-bit Adder**
- Appendix

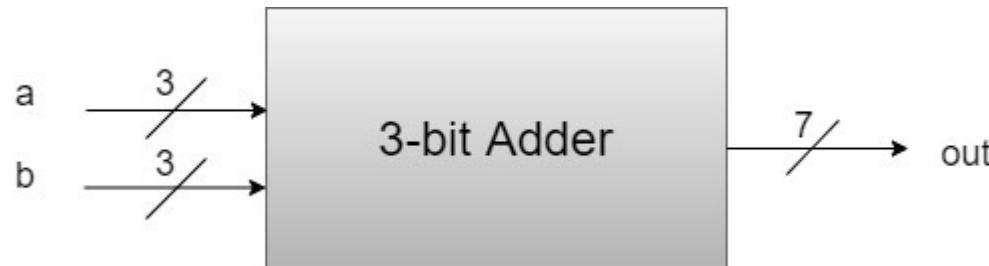
Lab I 學號顯示器

- 設計一個學號顯示器電路，顯示學號的後三碼
- 輸出21bits (使用三個七段顯示器，每個七段顯示器需用7bits控制亮暗)
HEX26~HEX20, HEX16~HEX10, HEX06~HEX00
- Ex: 學號F12345678，七段顯示器顯示678



Lab II – 3-bit Adder

- 設計一3-bit無號數加法器，輸入兩個3 bits數字，以七段顯示器顯示加法運算結果(16進制) HEX06~HEX00
- 3 bits加法和的大小在0~15之間，使用0~9、a~f表示
- Input: a(3 bits)、b(3 bits)
- Output: out(7 bits)



Notice for Lab II

■ 七段顯示器裝置模擬

- EX: $a = 0, b = 1$



- 七段顯示器顯示1

- EX: $a = 3, b = 4$



- 七段顯示器顯示7

- EX: $a = 7, b = 7$



- 七段顯示器顯示E

Notice

- 請勿命名中文資料夾
- Device family 請確認與 FPGA Chip 符合 (**5CEFA4F23C7**)
- Top module name & Project name 需要一致

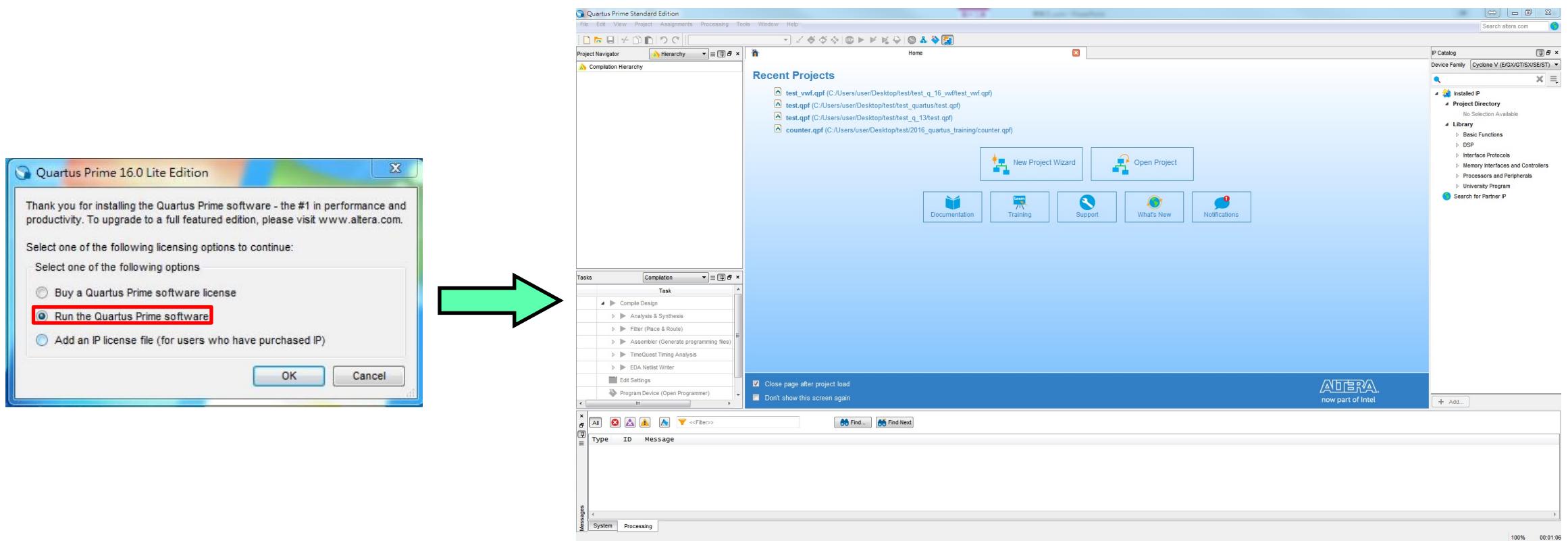
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Quartus II Tutorial (1/10)

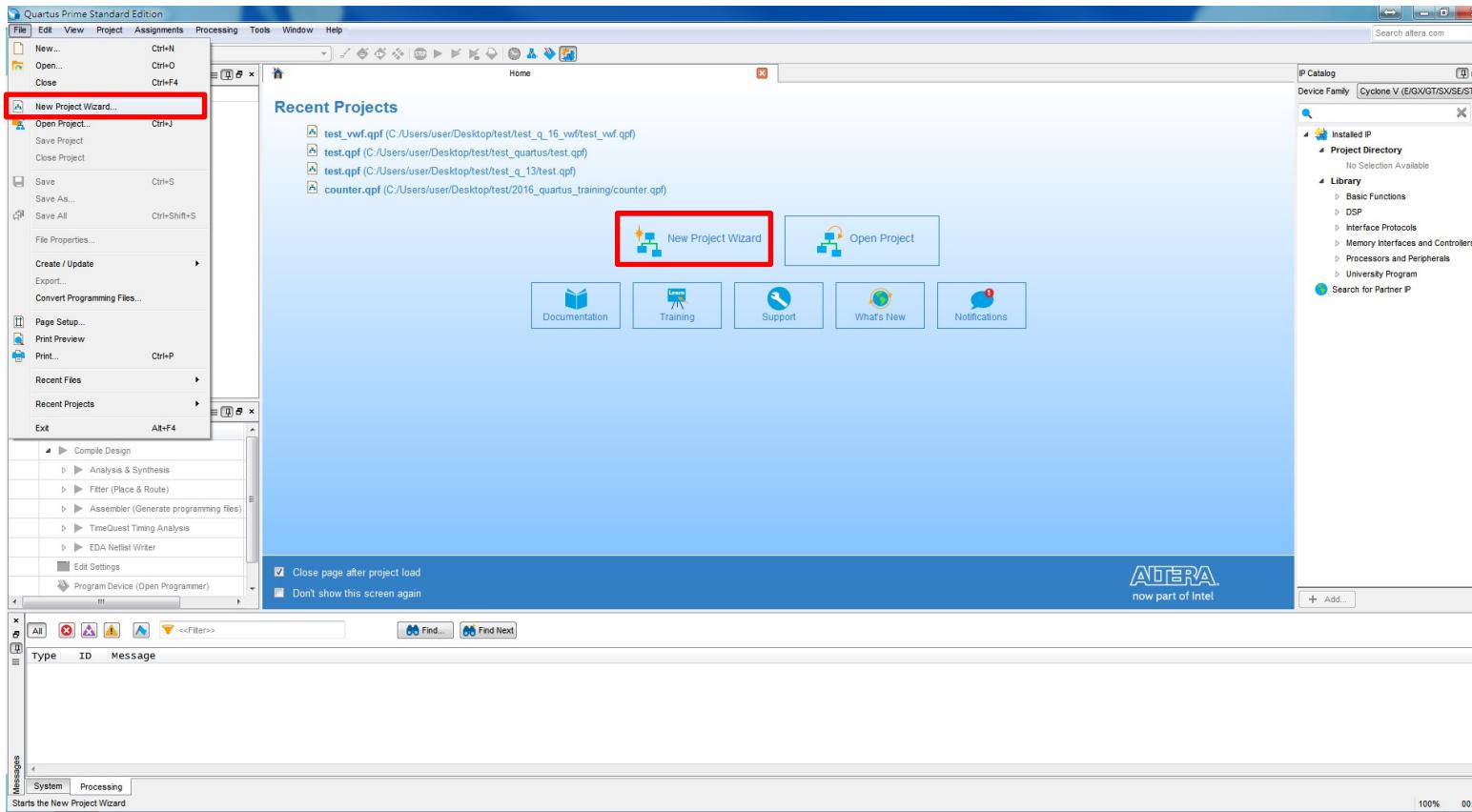
■ Getting Started –

- Start the Quartus II software



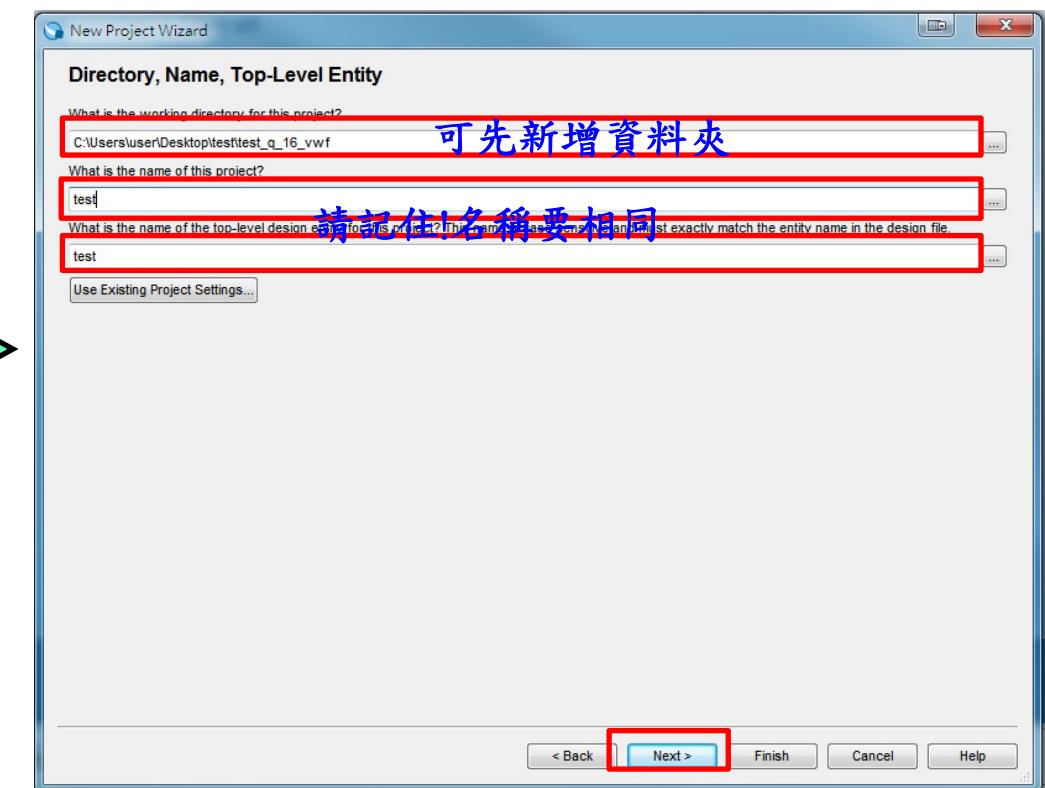
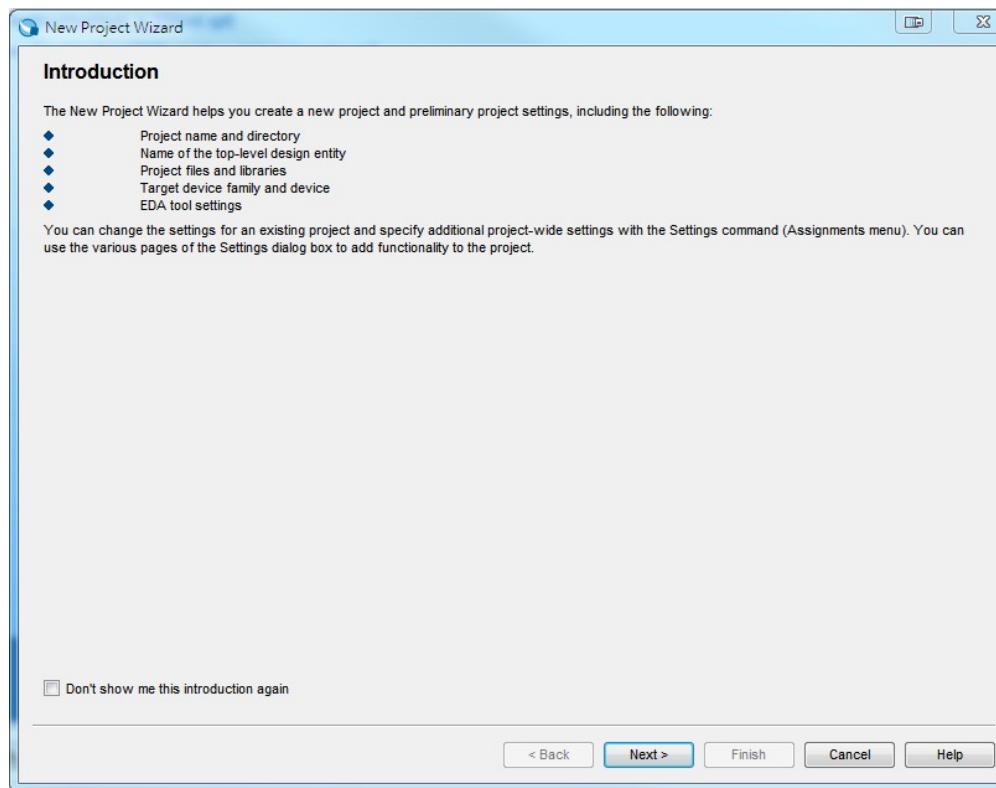
Quartus II Tutorial (2/10)

- Create a New Project –
 - Open New Project Wizard (File → New Project Wizard...)



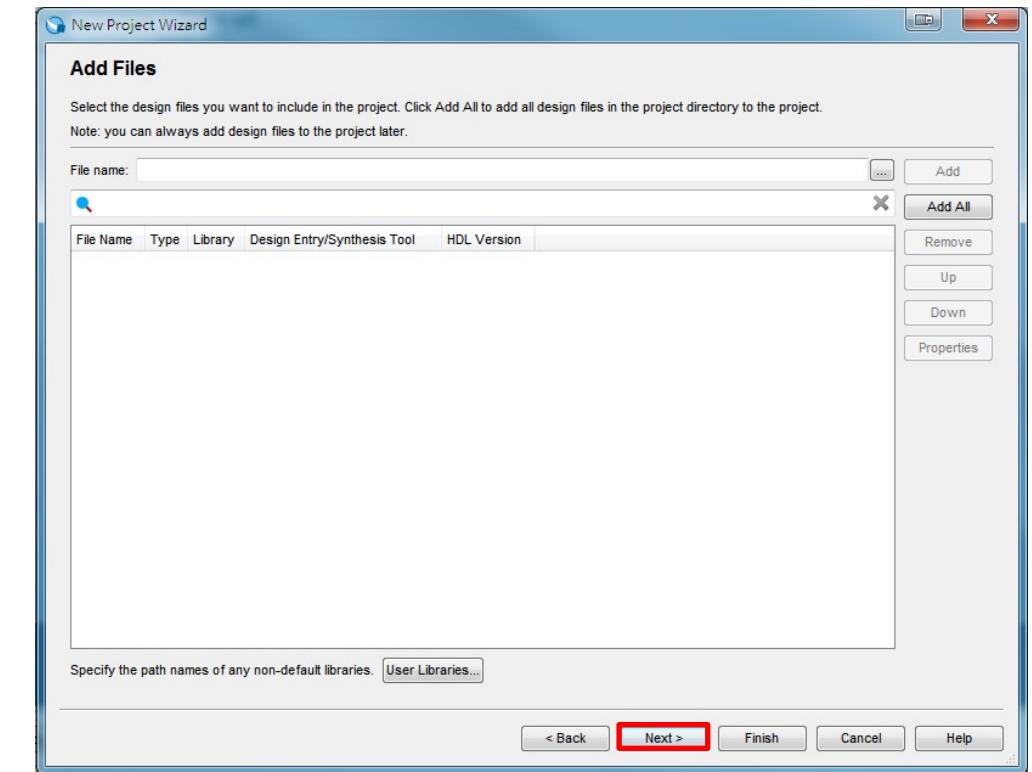
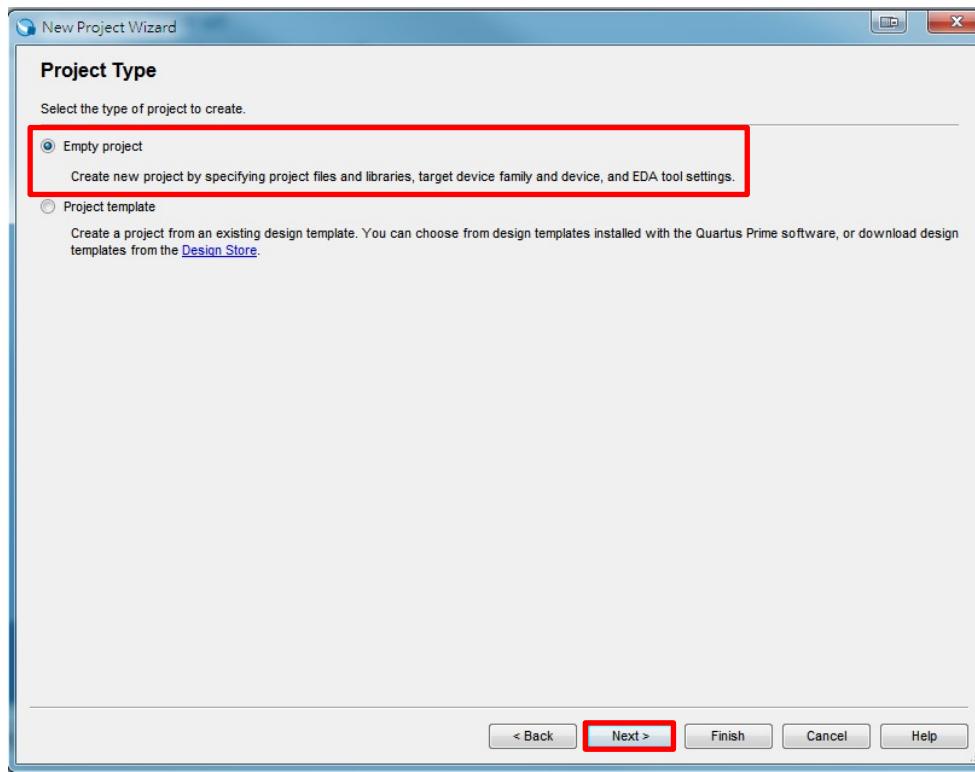
Quartus II Tutorial (3/10)

■ Specify the working directory and the name of the project



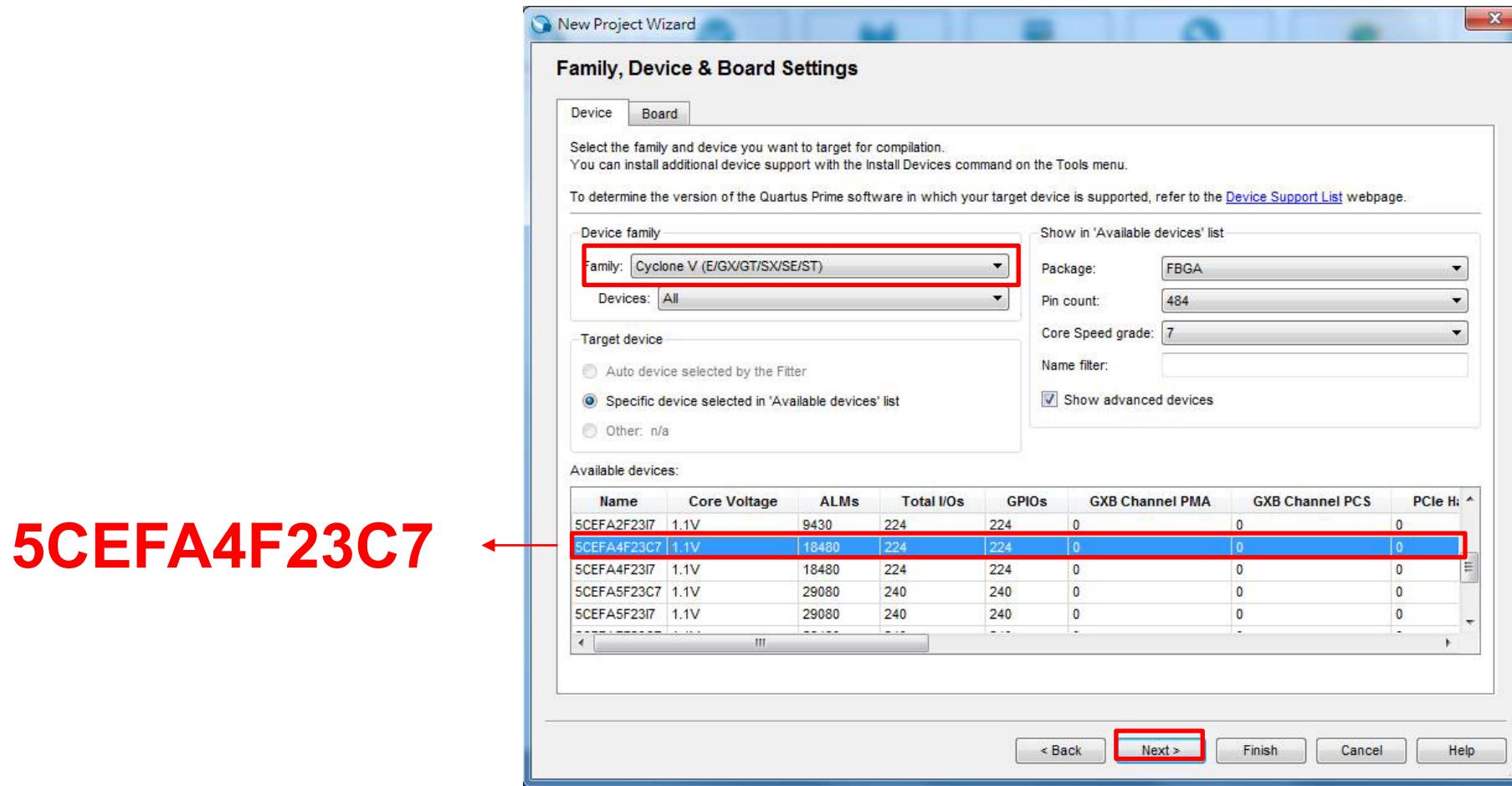
Quartus II Tutorial (4/10)

- Select “Empty project”. Then, click “Next”.
- Select design files. Or click “Next” to skip this step.



Quartus II Tutorial (5/10)

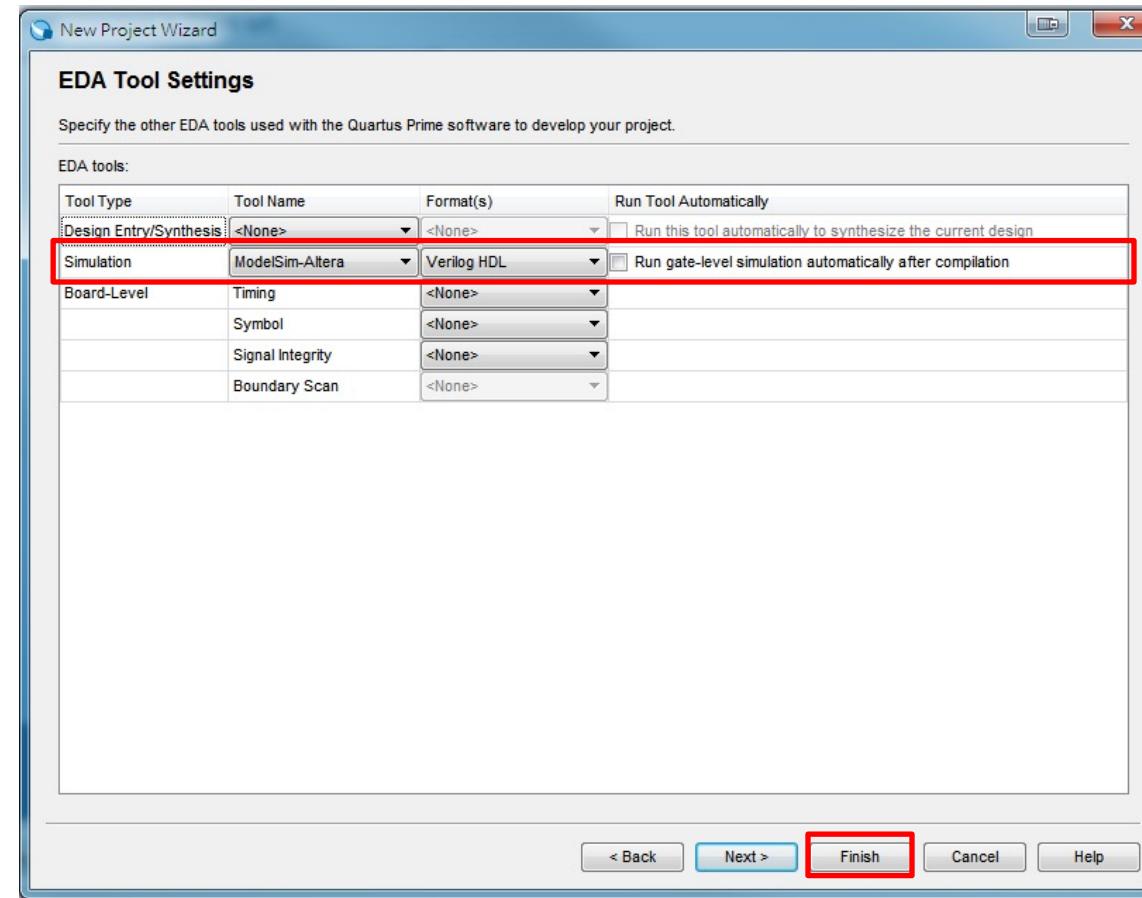
- Specify device settings - (DE0-CV Device family are used). Click “Next.”



5CEFA4F23C7

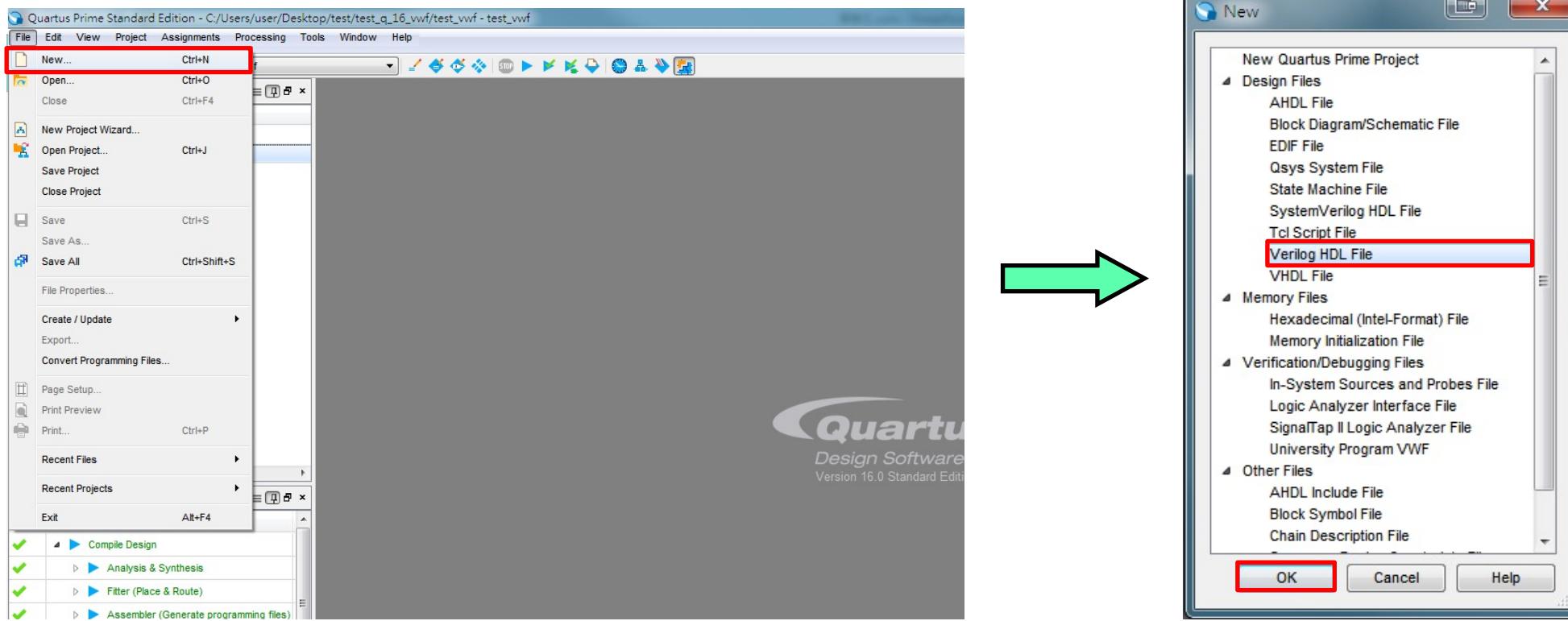
Quartus II Tutorial (6/10)

- Specify EDA Tool – (**Modelsim-Altera** is selected for simulation). Click “Finish.”



Quartus II Tutorial (7/10)

- Edit a new file by opening a Verilog HDL file
 - (File → New → **Verilog HDL File** → OK)



Quartus II Tutorial (8/10)

■ Write Verilog code

Top module name 一定要跟 Project name 相同 !!

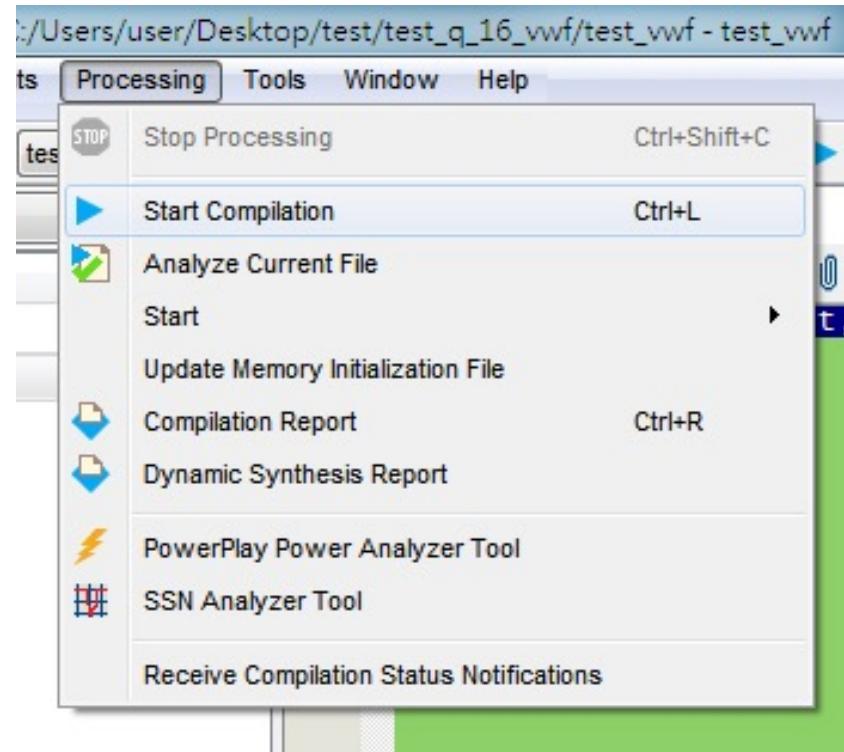
```
1: //File Name : Half_Adder.v
2: module Half_Adder(a, b, sum, carry);
3:   input a, b;
4:   output sum, carry;
5:
6:   assign sum = a ^ b;
7:   assign carry = a & b;
8:
9: endmodule
```

輸入(input)		輸出(output)	
被加數(a)	加數(b)	和(sum)	進位(carry)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



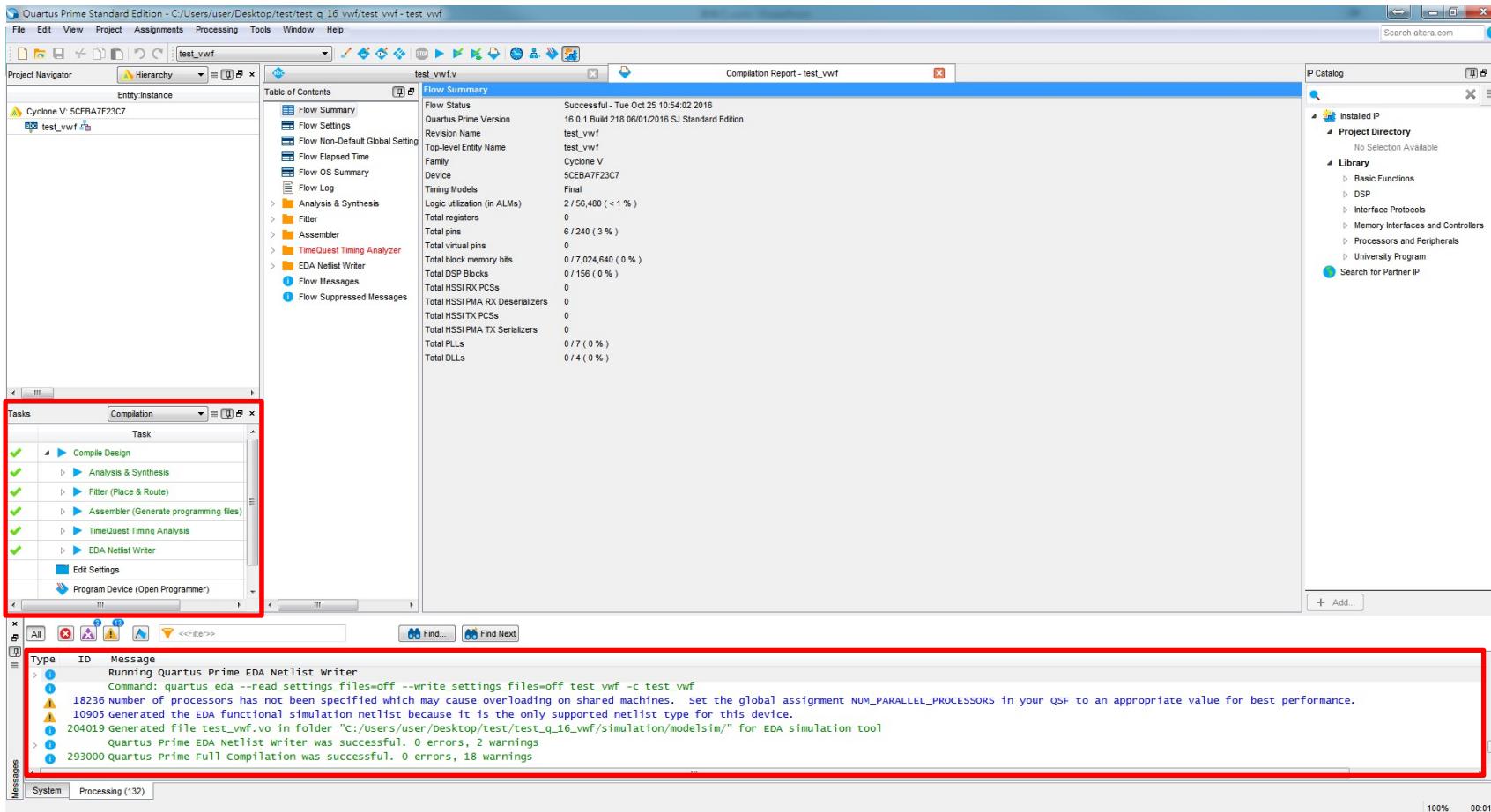
Quartus II Tutorial (9/10)

- Compiling the Designed Circuit (synthesis 合成)
 - (Processing → Start Compilation)



Quartus II Tutorial (10/10)

■ Successful compilation

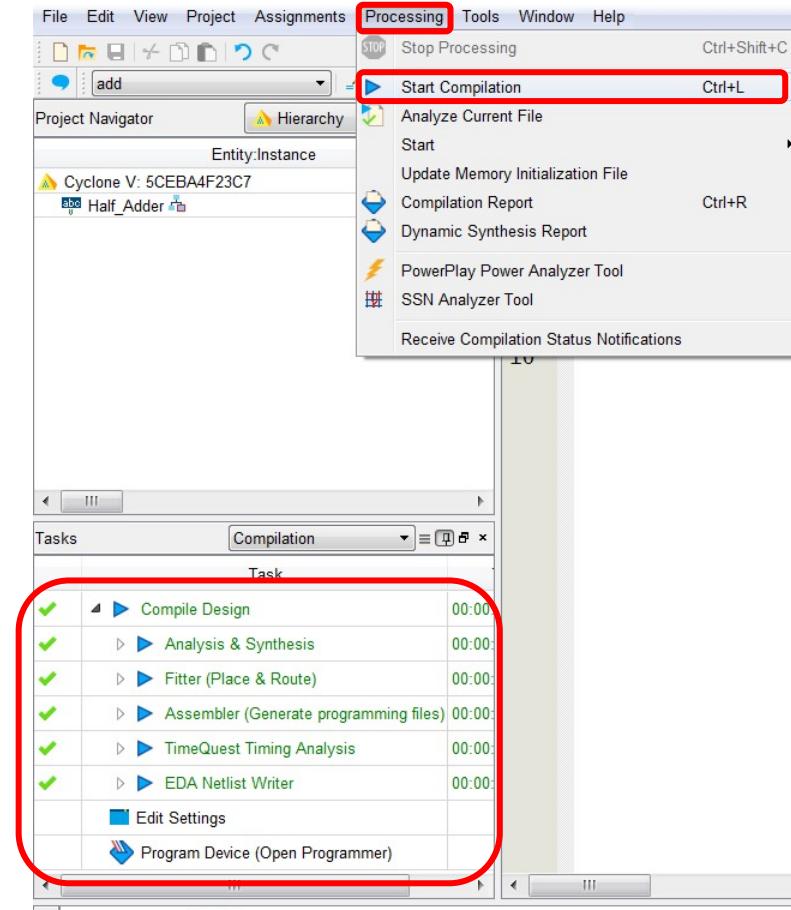


Programming DE0-CV (1/13)

```
1 module Half_Adder(a, b, sum, carry);
2   input a,b;
3   output sum, carry;
4   assign sum = a ^ b;
5   assign carry = a & b;
6 endmodule
```

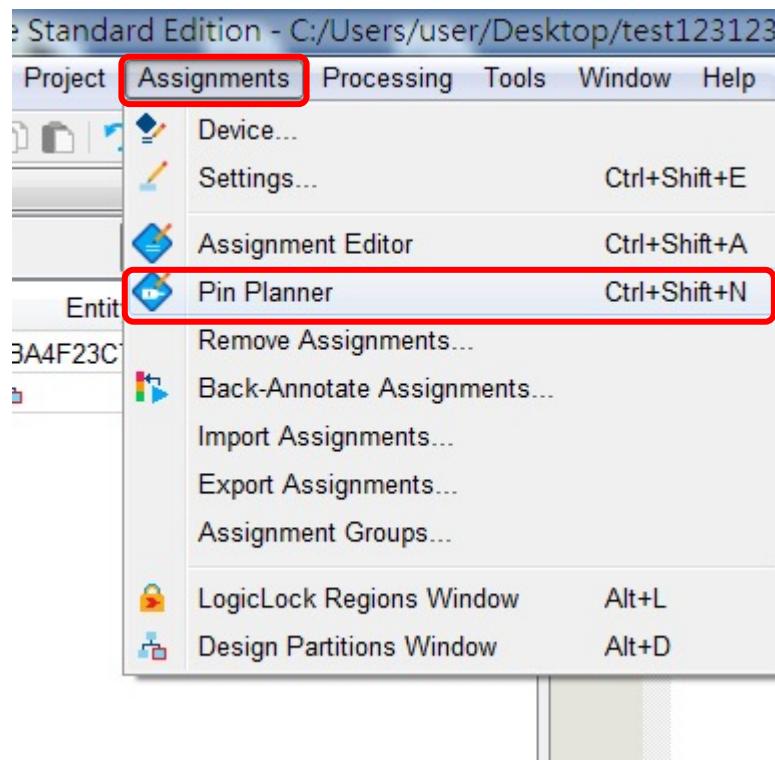
Programming DE0-CV (2/13)

■ Start compilation



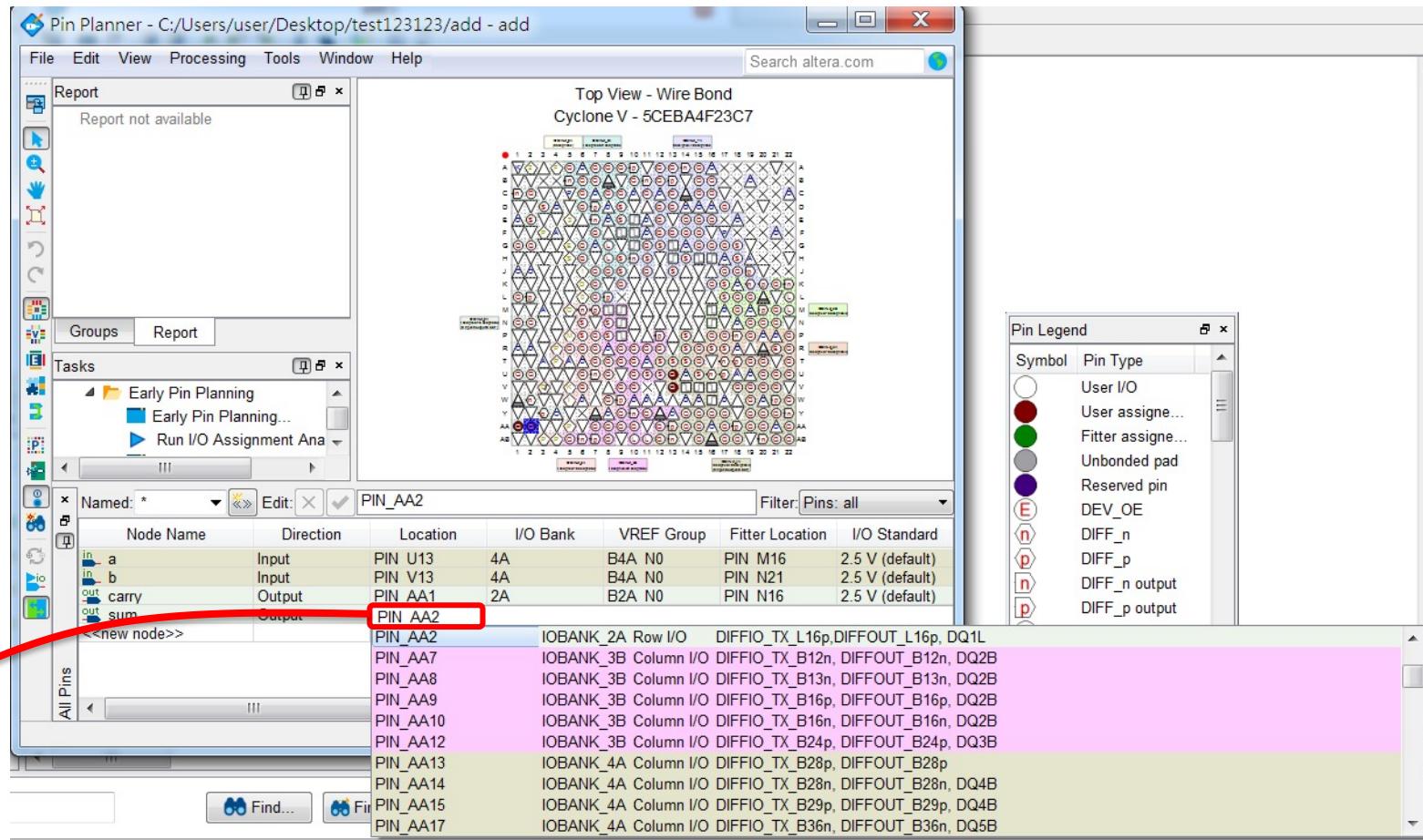
Programming DE0-CV (3/13)

■ Open Pin Planner



Programming DE0-CV (4/13)

■ Pin assignment



Double click

Programming DE0-CV (5/13)

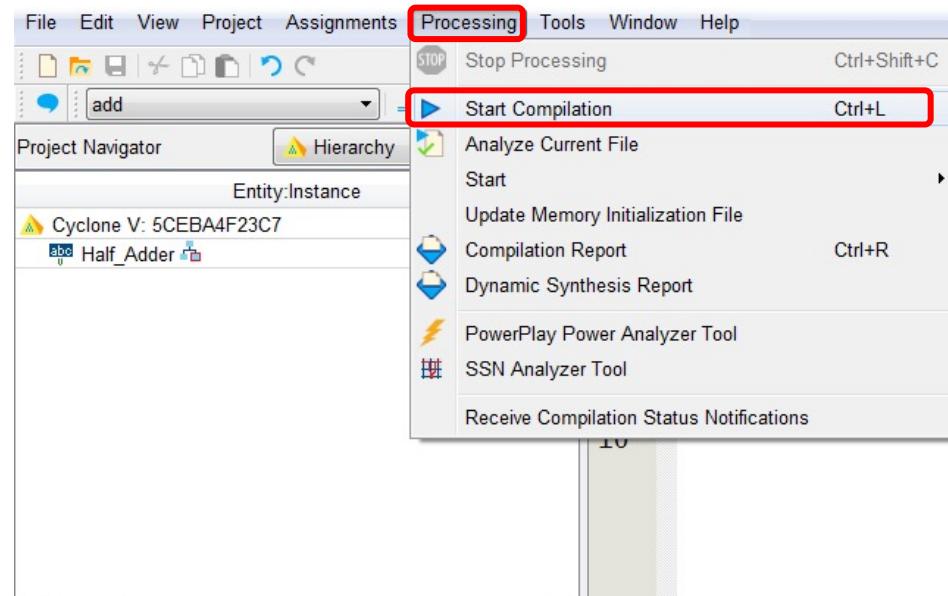
- Assign pin location to all inputs and outputs

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard
in a	Input	PIN U13 SW0	4A	B4A N0	PIN M16	2.5 V (default)
in b	Input	PIN V13 SW1	4A	B4A N0	PIN N21	2.5 V (default)
out carry	Output	PIN AA1 LED1	2A	B2A N0	PIN N16	2.5 V (default)
out sum	Output	PIN AA2 LED0				

- Please refer to DE0_pin.xls for pin location assignment

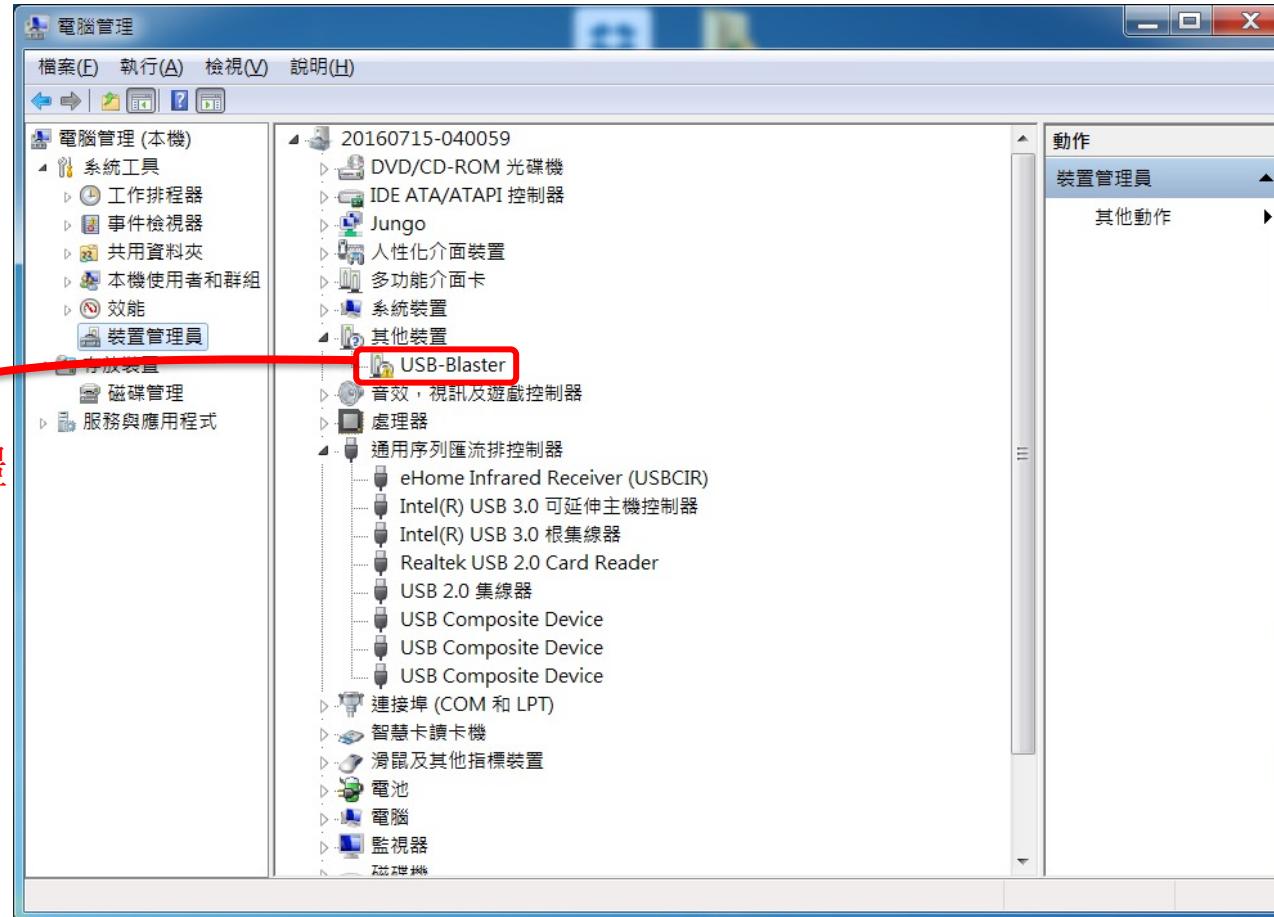
Programming DE0-CV (6/13)

■ Start compilation

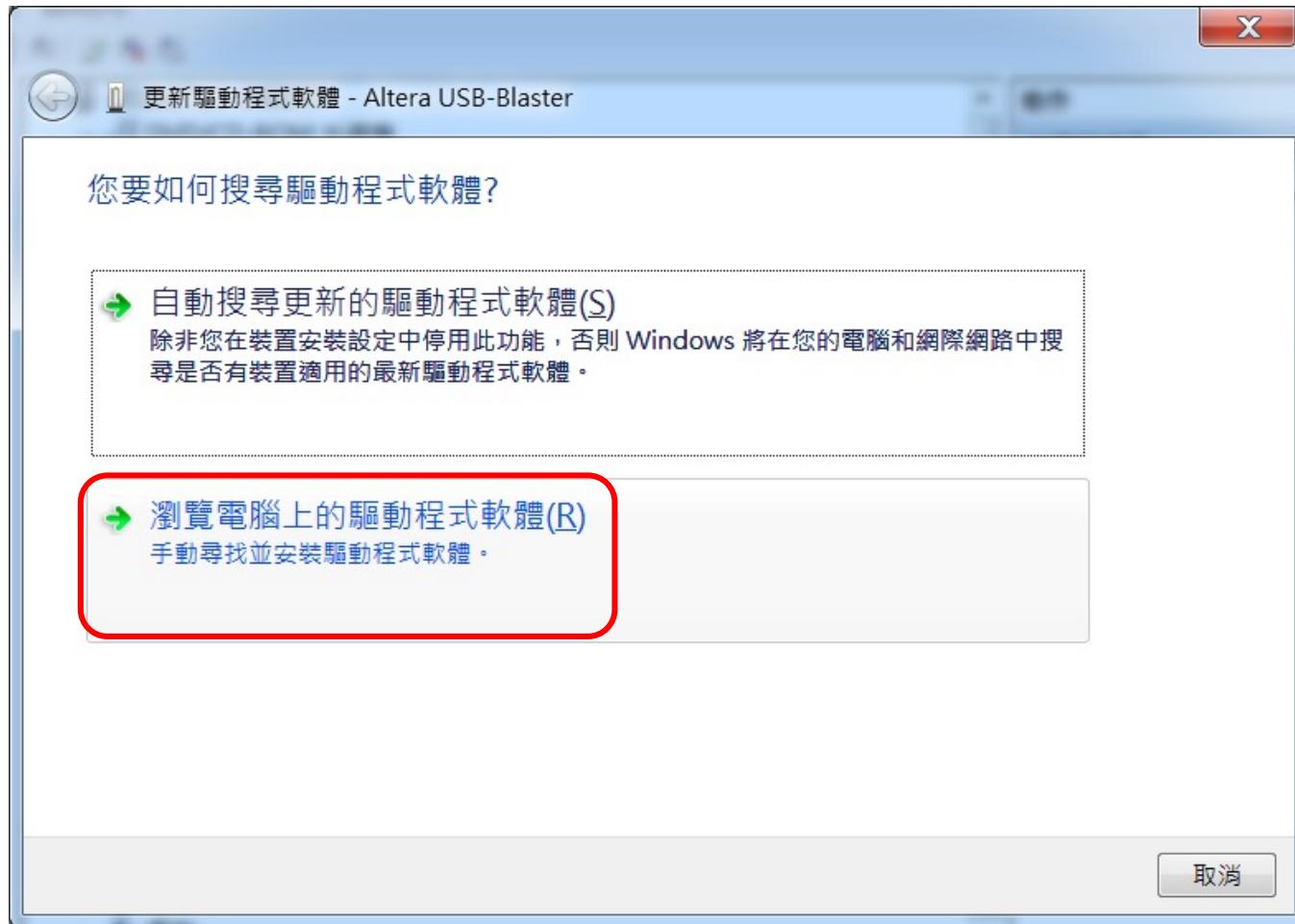


Programming DE0-CV (7/13)

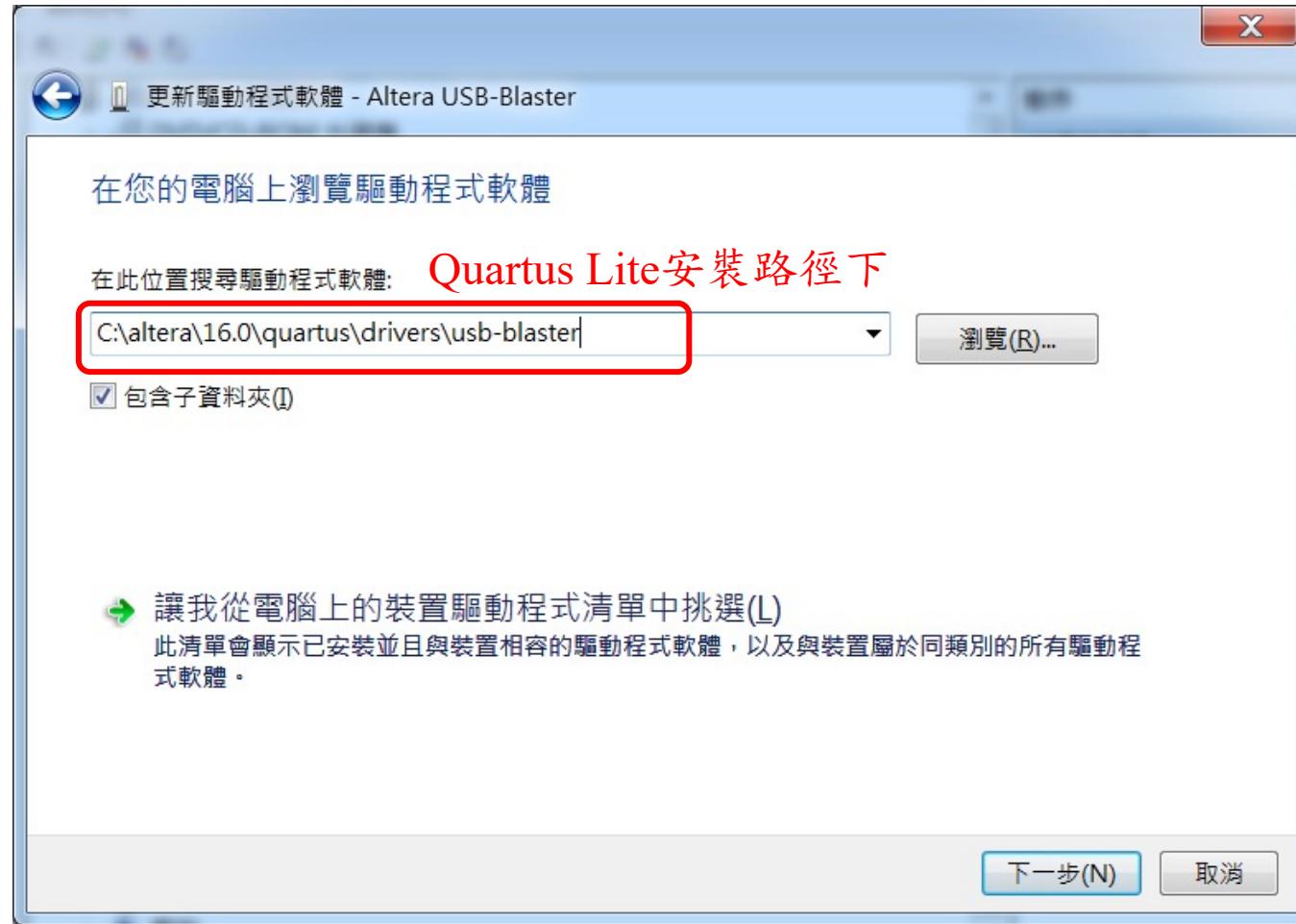
右鍵選更新驅動程式軟體



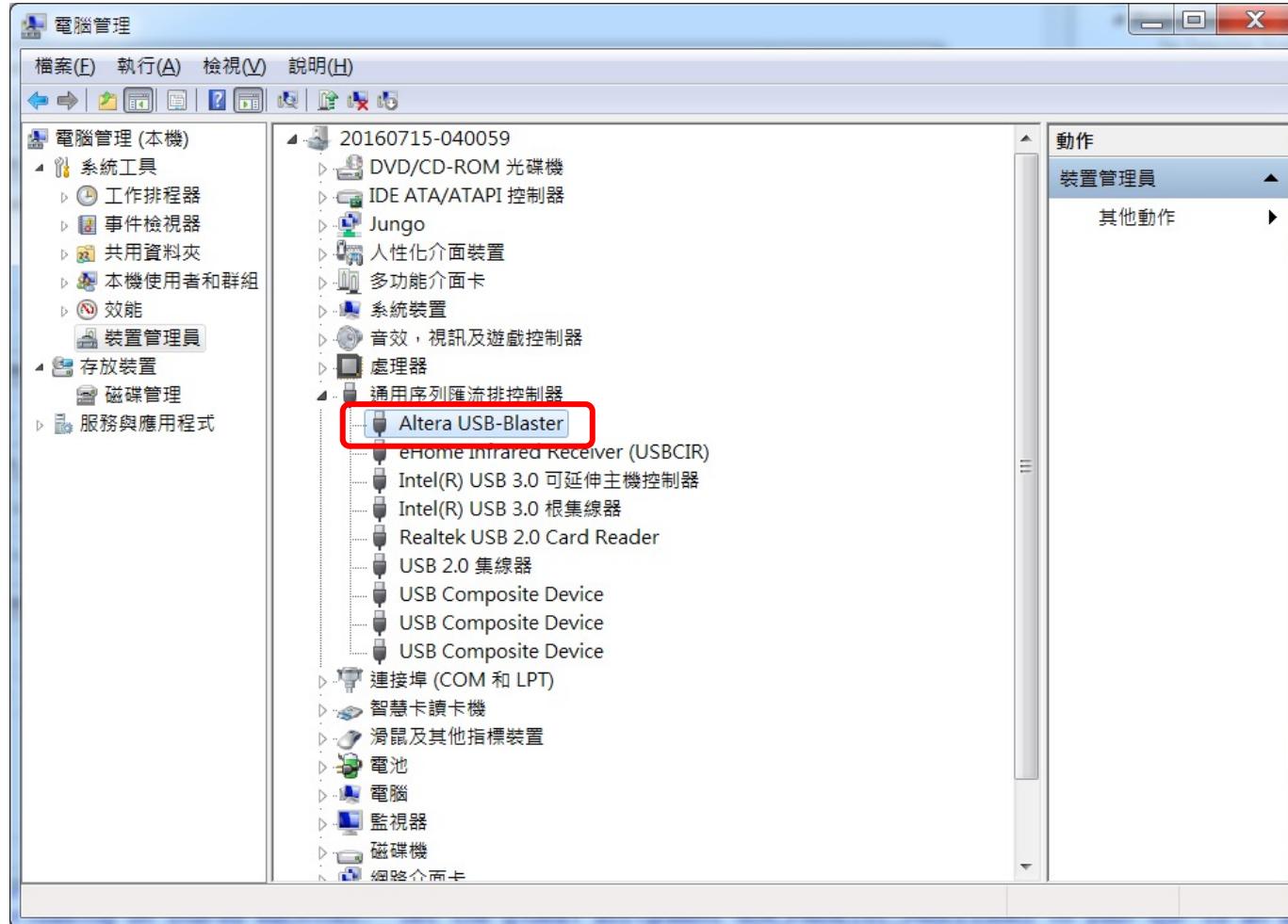
Programming DE0-CV (8/13)



Programming DE0-CV (9/13)

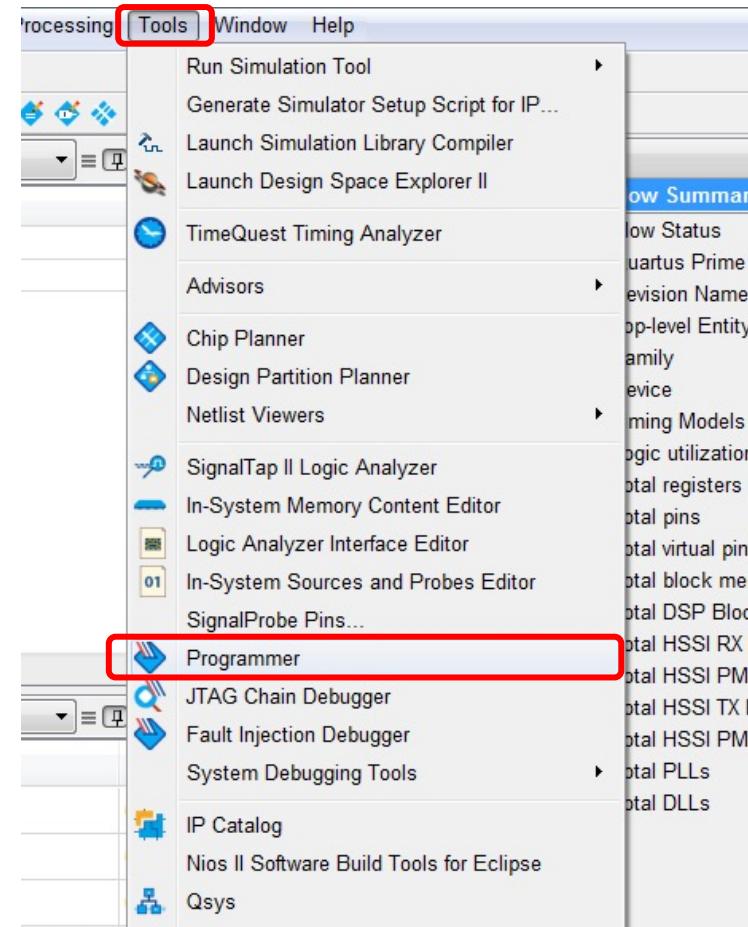


Programming DE0-CV (10/13)



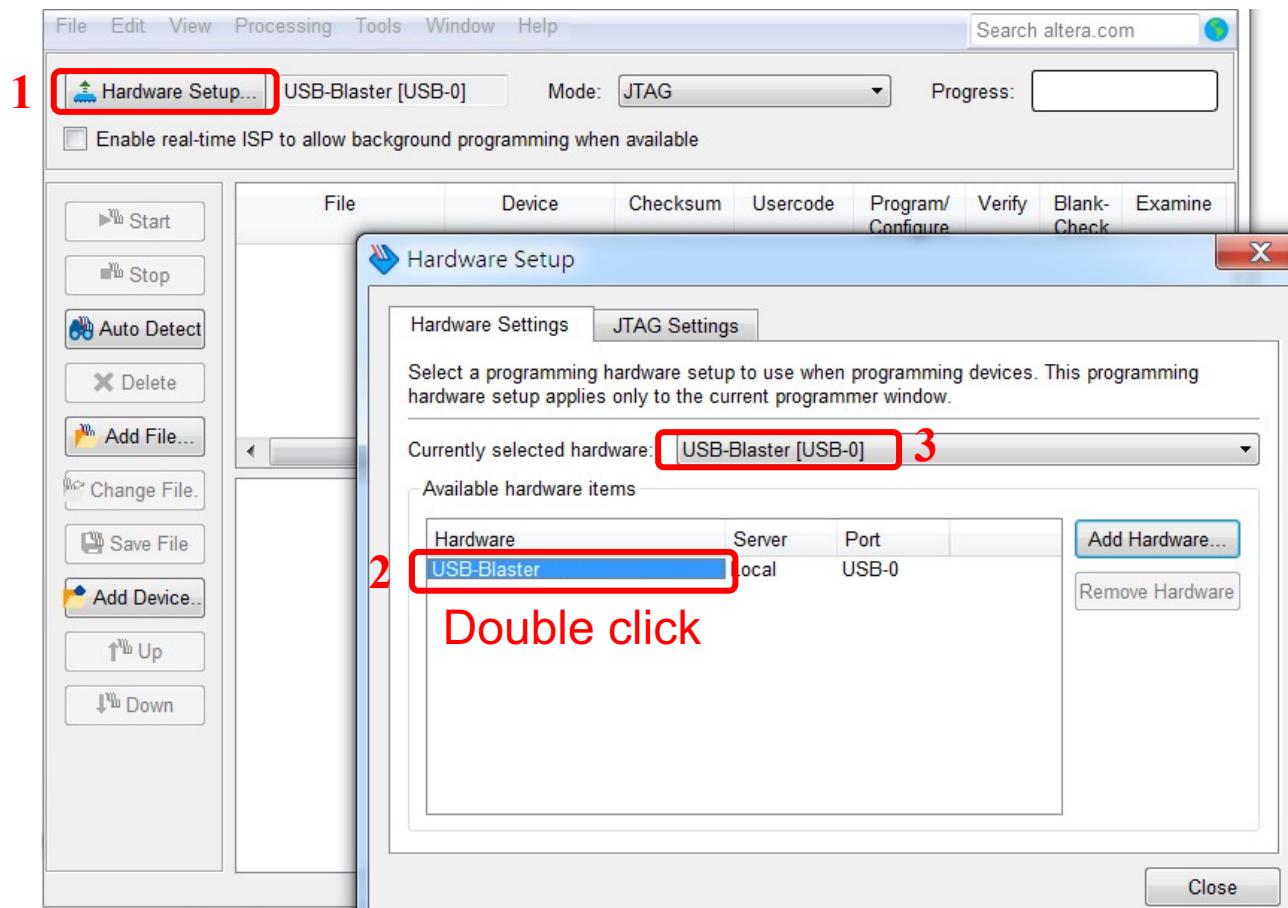
Programming DE0-CV (11/13)

■ Programming device



Programming DE0-CV (12/13)

■ Hardware setup: add USB-Blaster



Programming DE0-CV (13/13)

■ Programming device

