



LAB - 04

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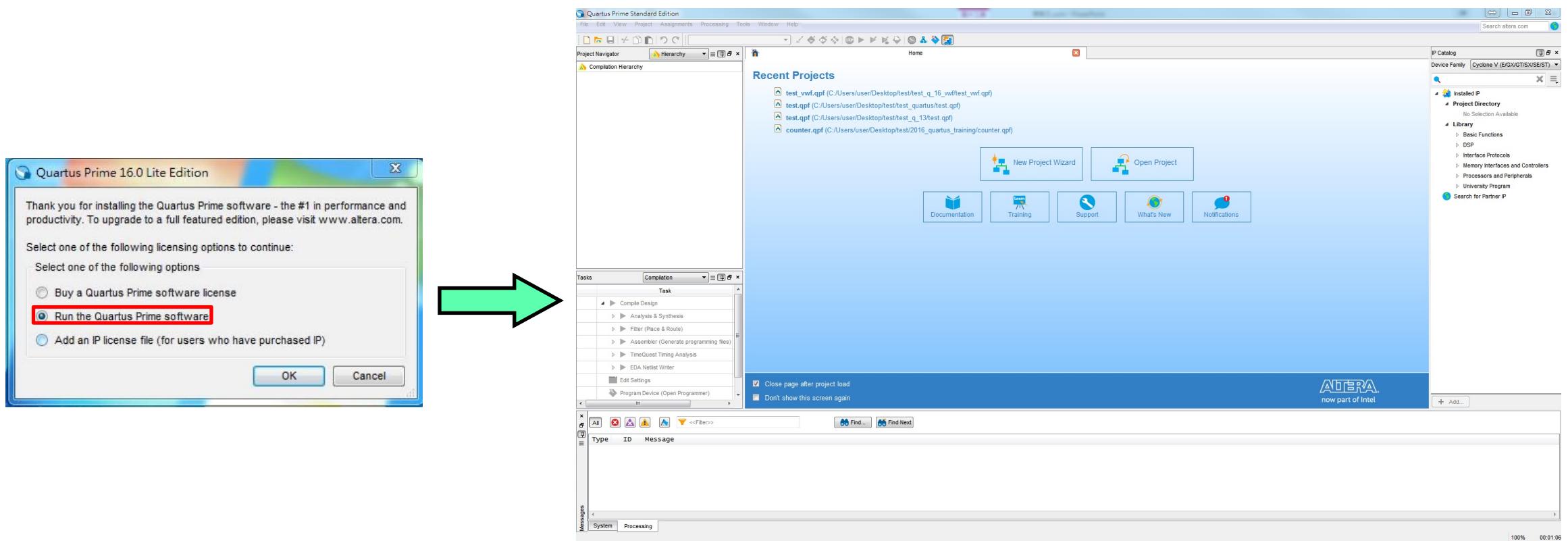
Outline

- Video preview for 晶片實現+HDL介紹(Parts II~IV)
- Quartus II tutorial
- Introduction to DE0-CV
- Programming DE0-CV
- Lab I – adder-subtractor to DE0-CV
- Lab II – encoder to DE0-CV

Quartus II Tutorial (1/10)

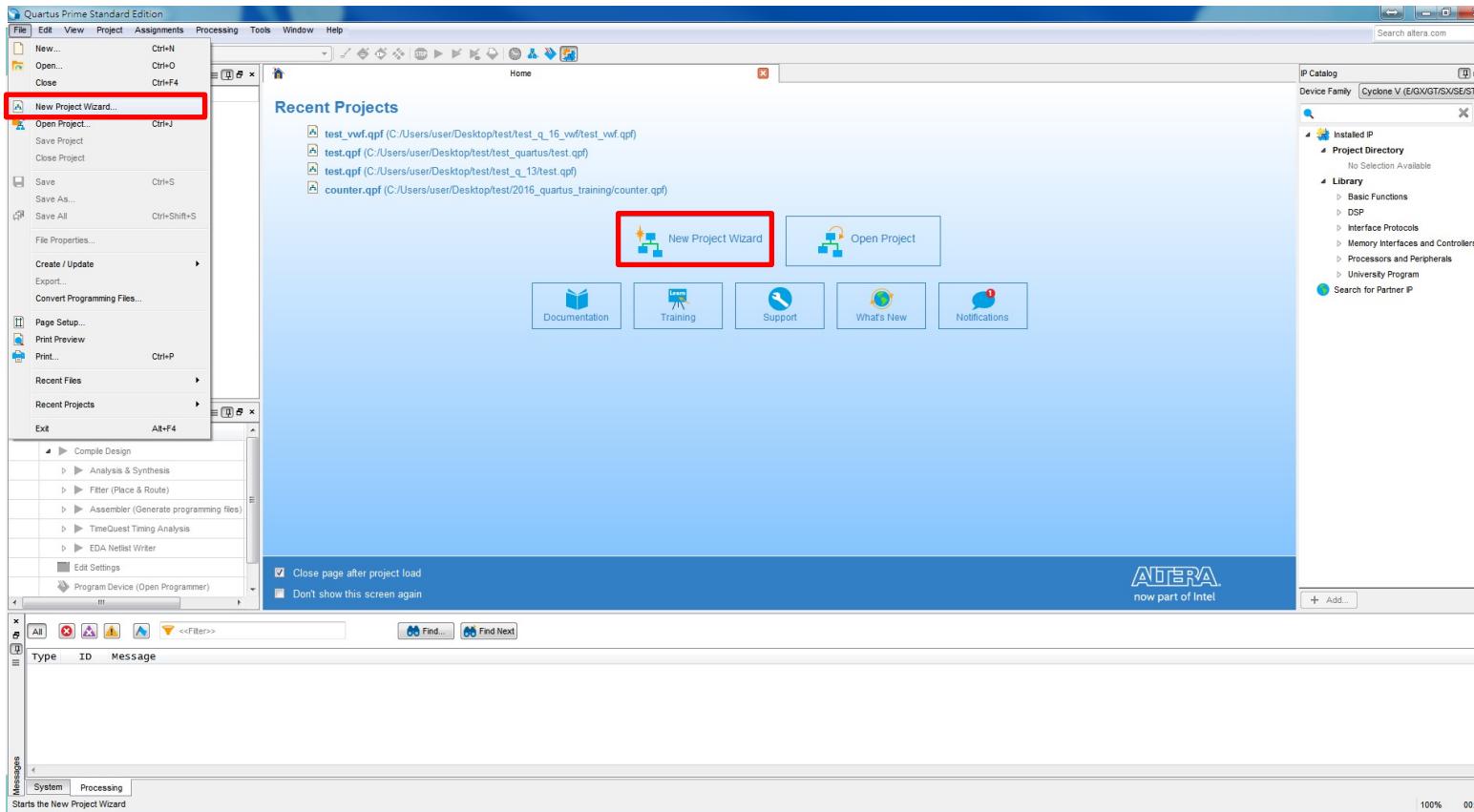
■ Getting Started –

- Start the Quartus II software



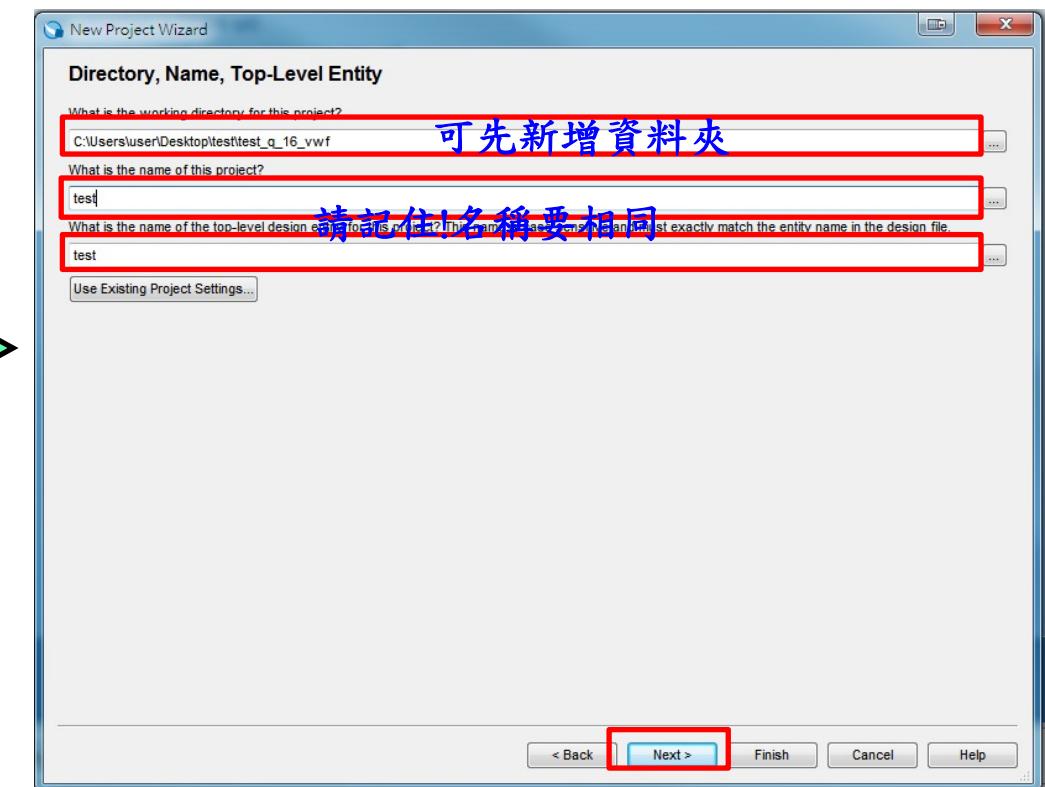
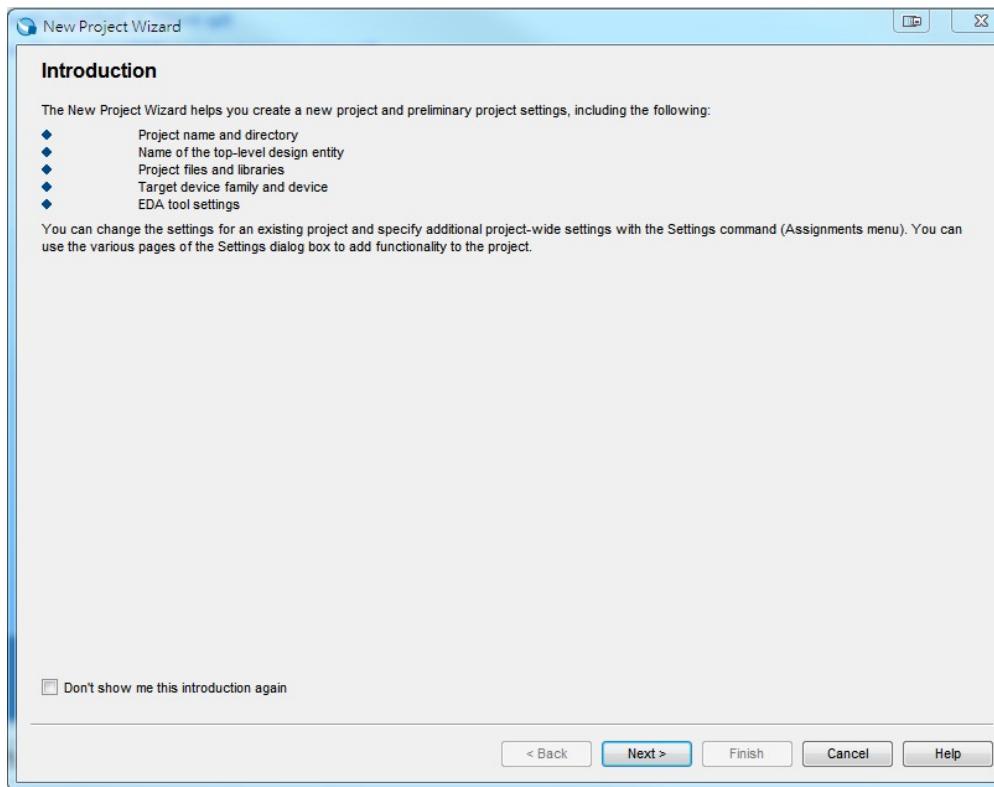
Quartus II Tutorial (2/10)

- Create a New Project –
 - Open New Project Wizard (File → New Project Wizard...)



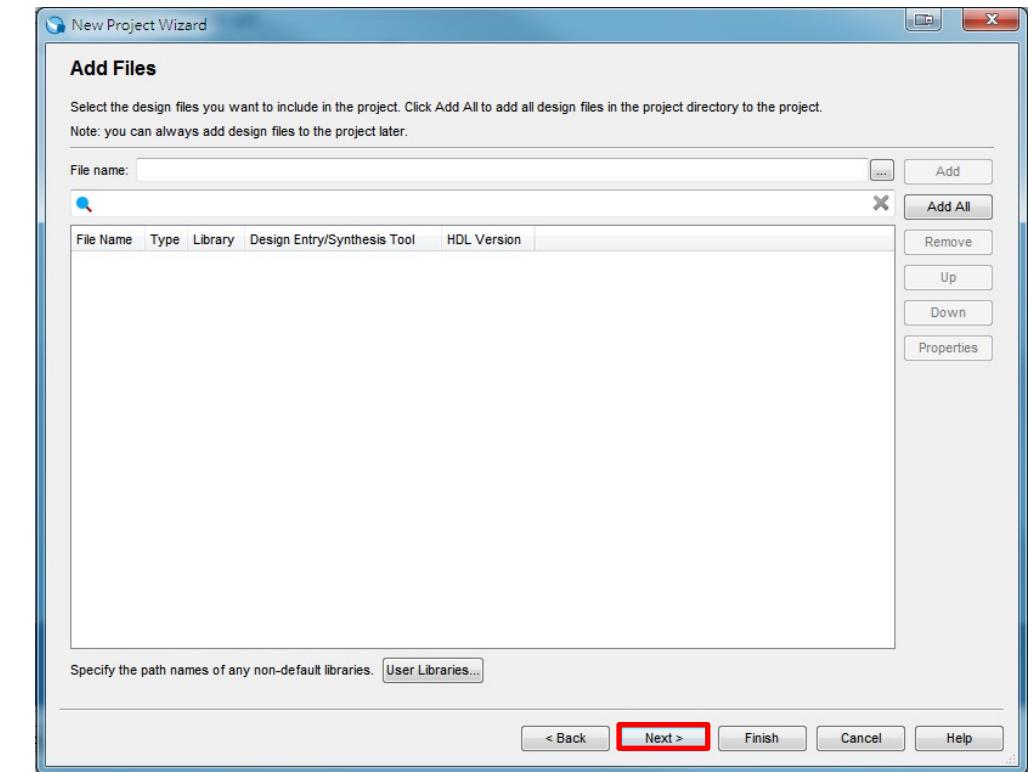
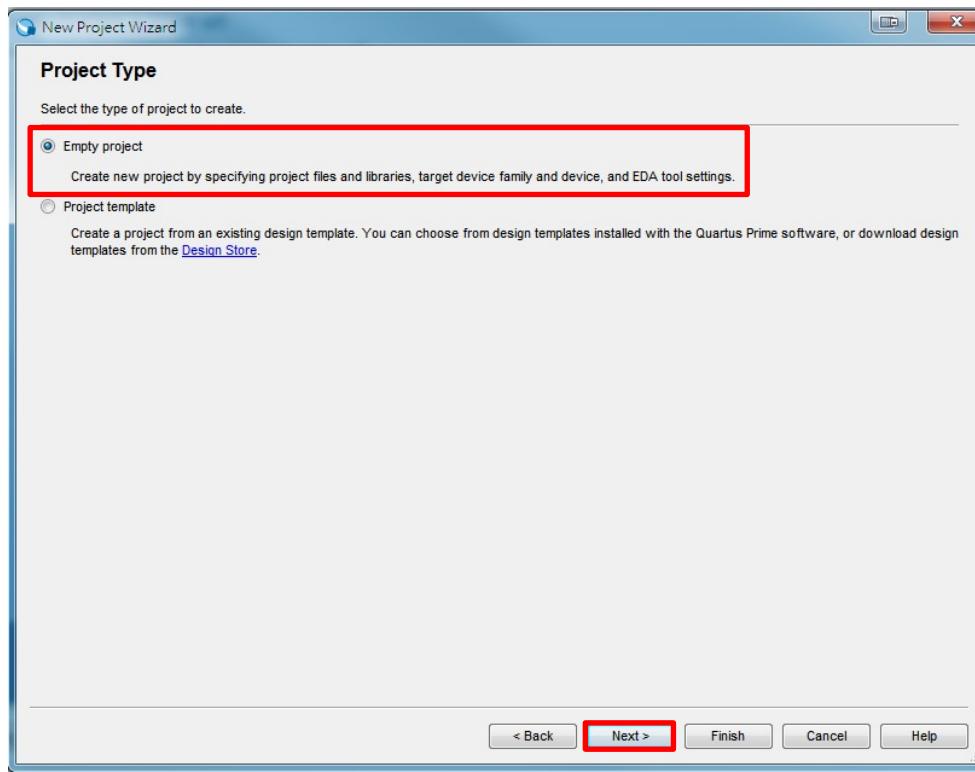
Quartus II Tutorial (3/10)

■ Specify the working directory and the name of the project



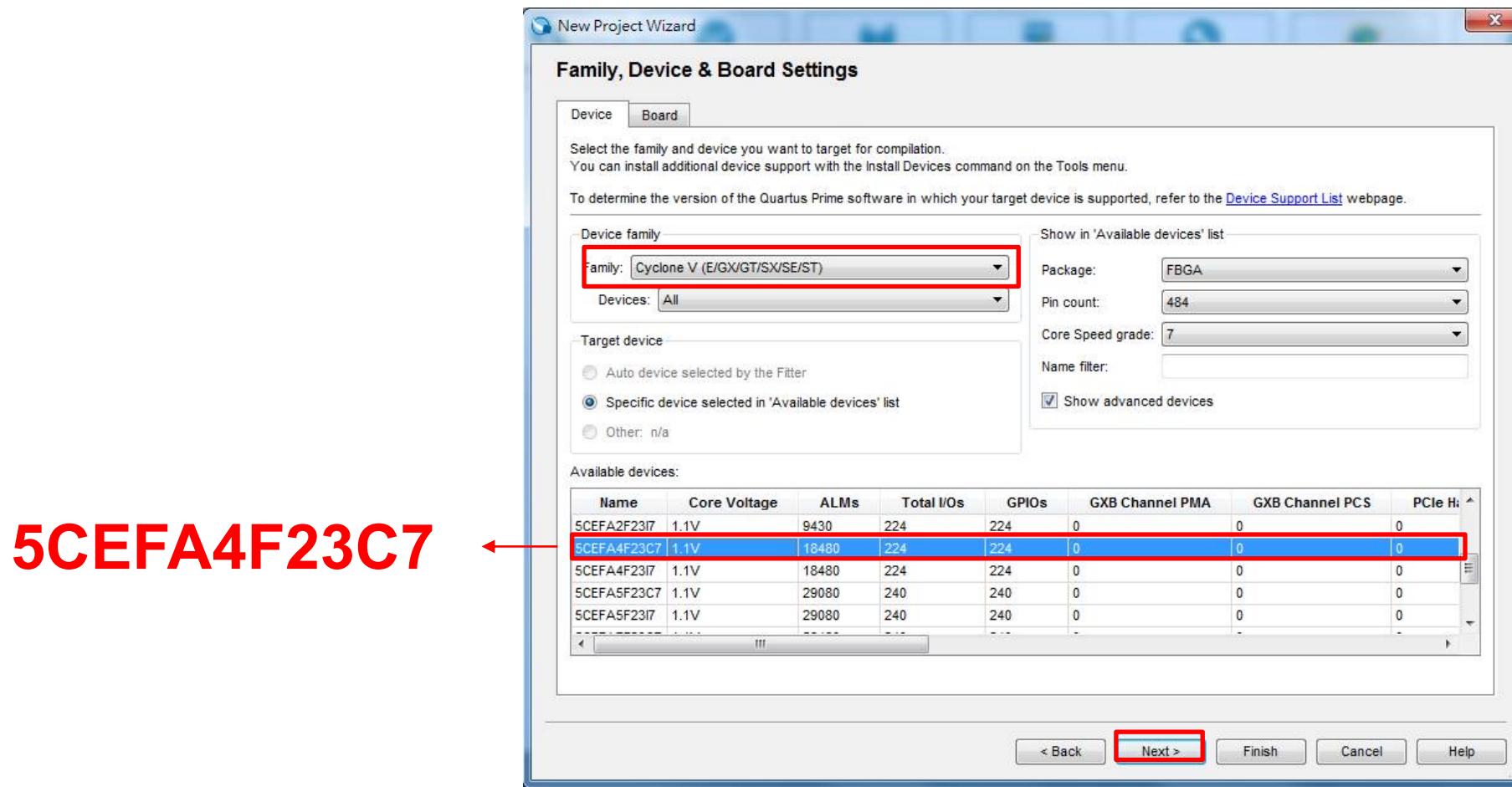
Quartus II Tutorial (4/10)

- Select “Empty project”. Then, click “Next”.
- Select design files. Or click “Next” to skip this step.



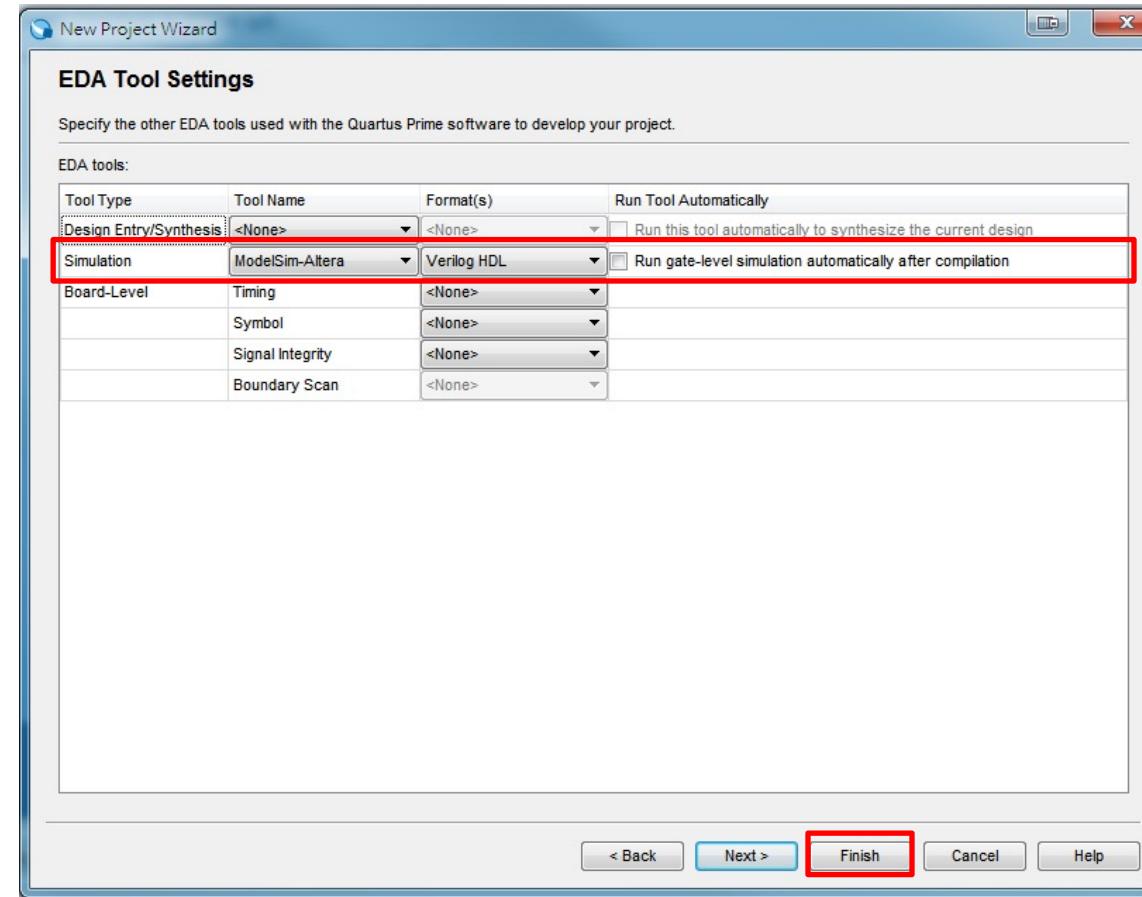
Quartus II Tutorial (5/10)

- Specify device settings - (DE0-CV Device family are used). Click “Next.”



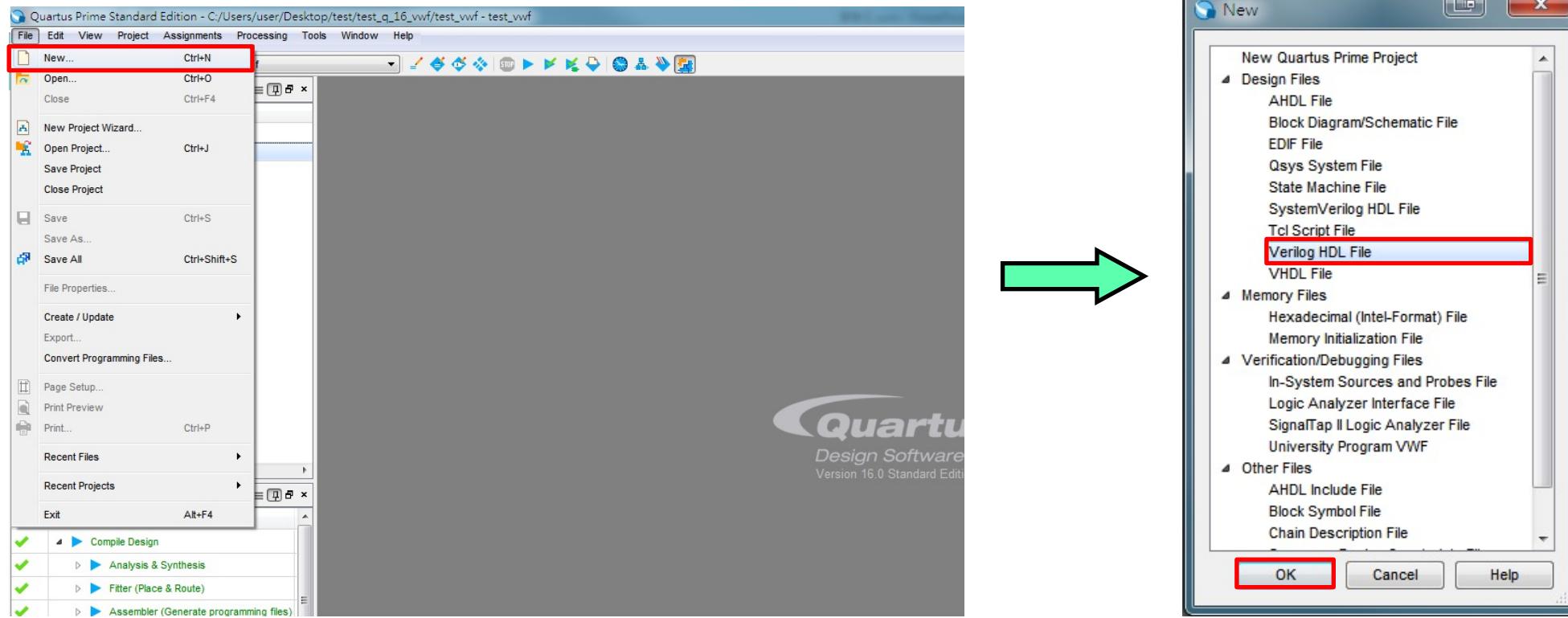
Quartus II Tutorial (6/10)

- Specify EDA Tool – (**Modelsim-Altera** is selected for simulation). Click “Finish.”



Quartus II Tutorial (7/10)

- Edit a new file by opening a Verilog HDL file
 - (File → New → **Verilog HDL File** → OK)



Quartus II Tutorial (8/10)

■ Write Verilog code

Top module name 一定要跟 Project name 相同 !!

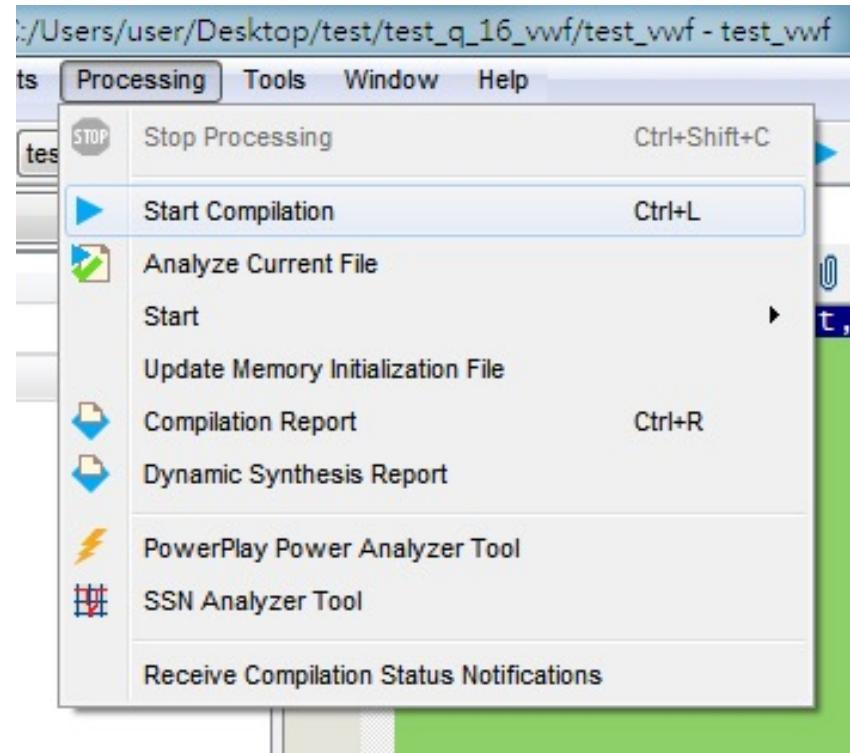
```
1: //File Name : Half_Adder.v
2: module Half_Adder(a, b, sum, carry);
3:   input a, b;
4:   output sum, carry;
5:
6:   assign sum = a ^ b;
7:   assign carry = a & b;
8:
9: endmodule
```

輸入(input)		輸出(output)	
被加數(a)	加數(b)	和(sum)	進位(carry)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



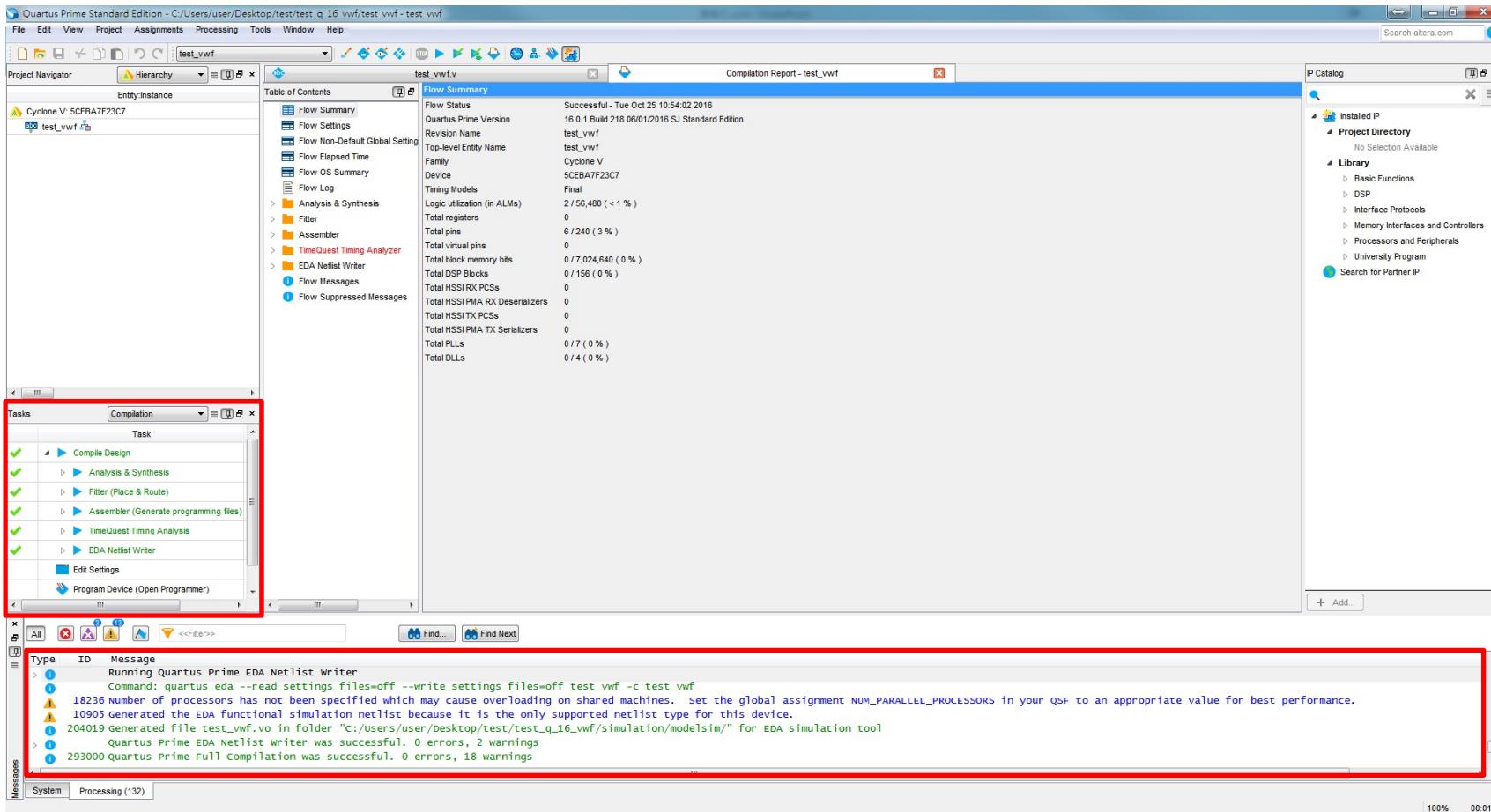
Quartus II Tutorial (9/10)

- Compiling the Designed Circuit (synthesis 合成)
 - (Processing → Start Compilation)



Quartus II Tutorial (10/10)

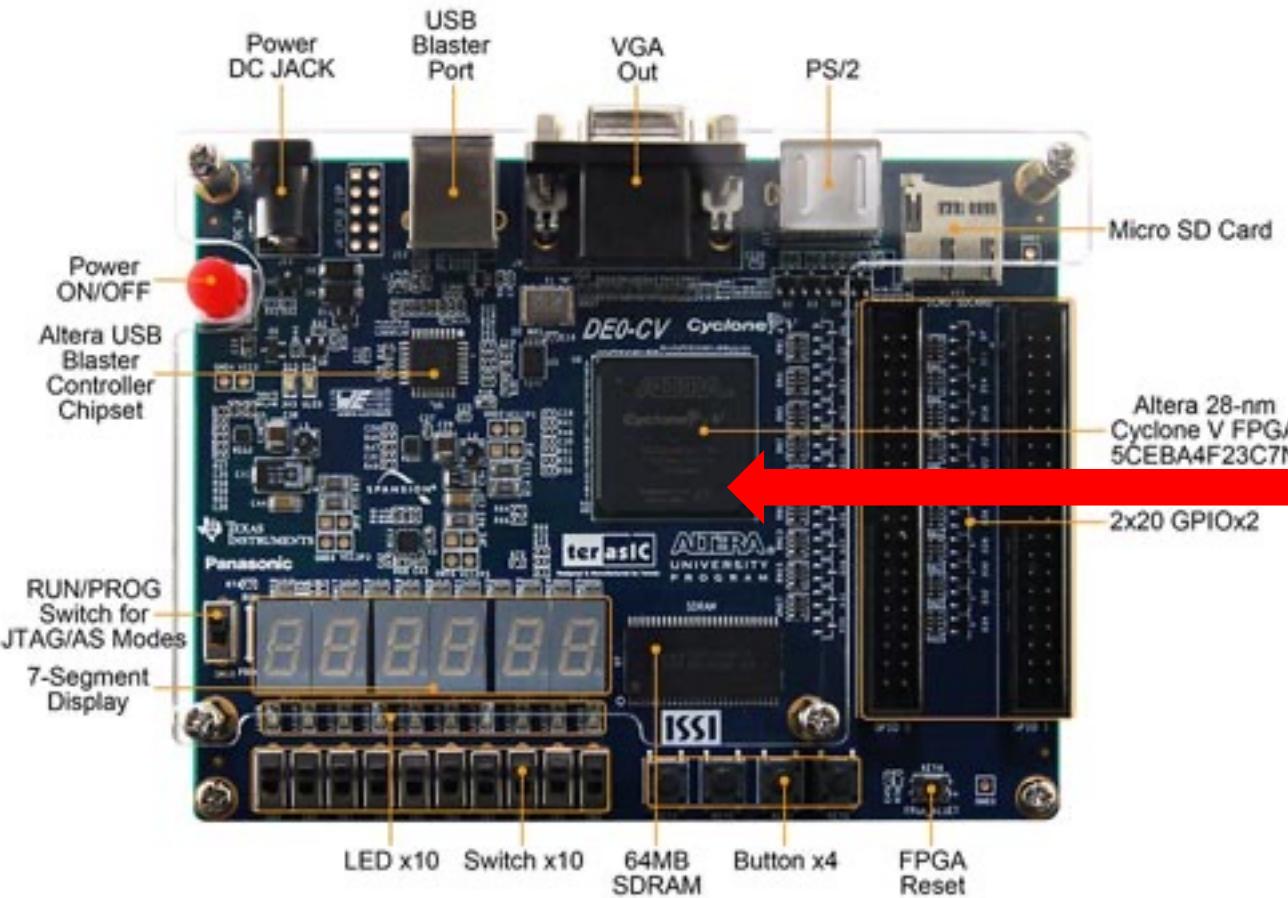
■ Successful compilation



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- **Introduction to DE0-CV**
- Programming DE0-CV
- Lab I – adder-subtractor to DE0-CV
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Introduction to DE0-CV(1/3)

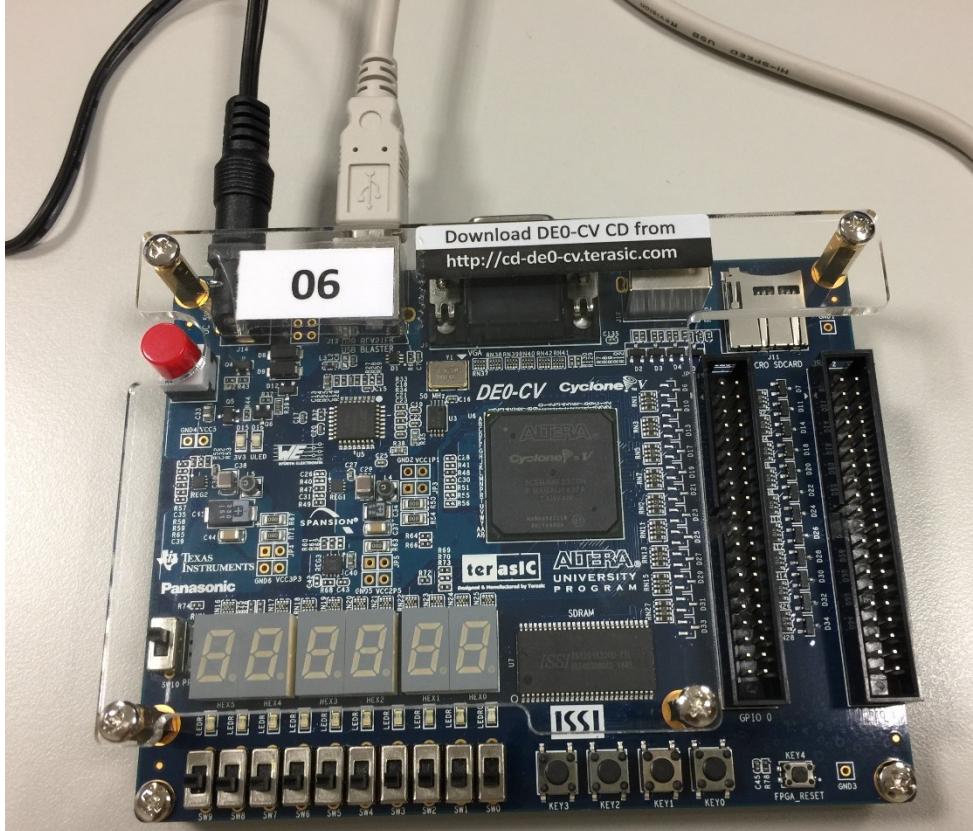


1. DE0-CV is a FPGA simulation board used to simulate the user-defined circuit.
2. You can program your circuit into the FPGA in the board for simulation.

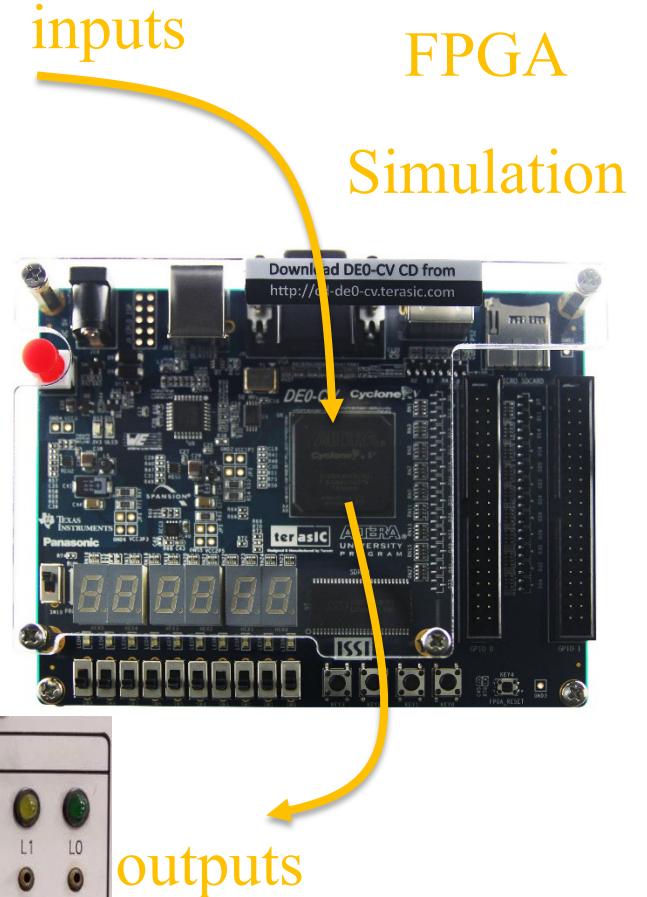
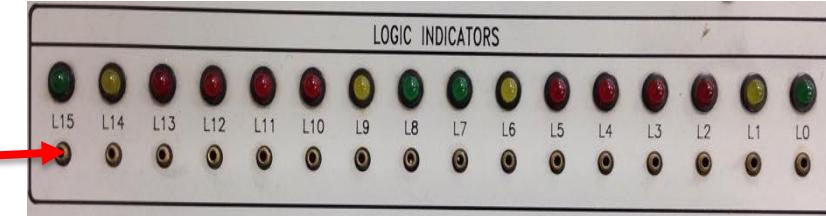
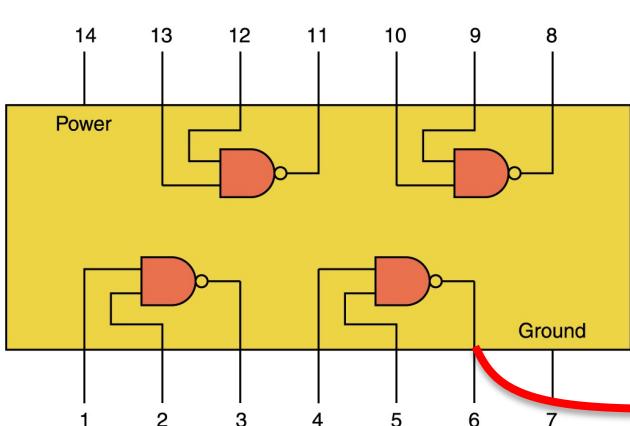
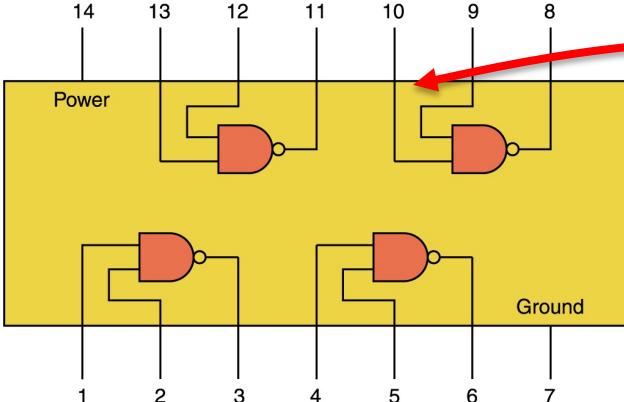
User-defined circuit

Introduction to DE0-CV (2/3)

電源 USB



Introduction to DE0-CV (3/3)



Outline

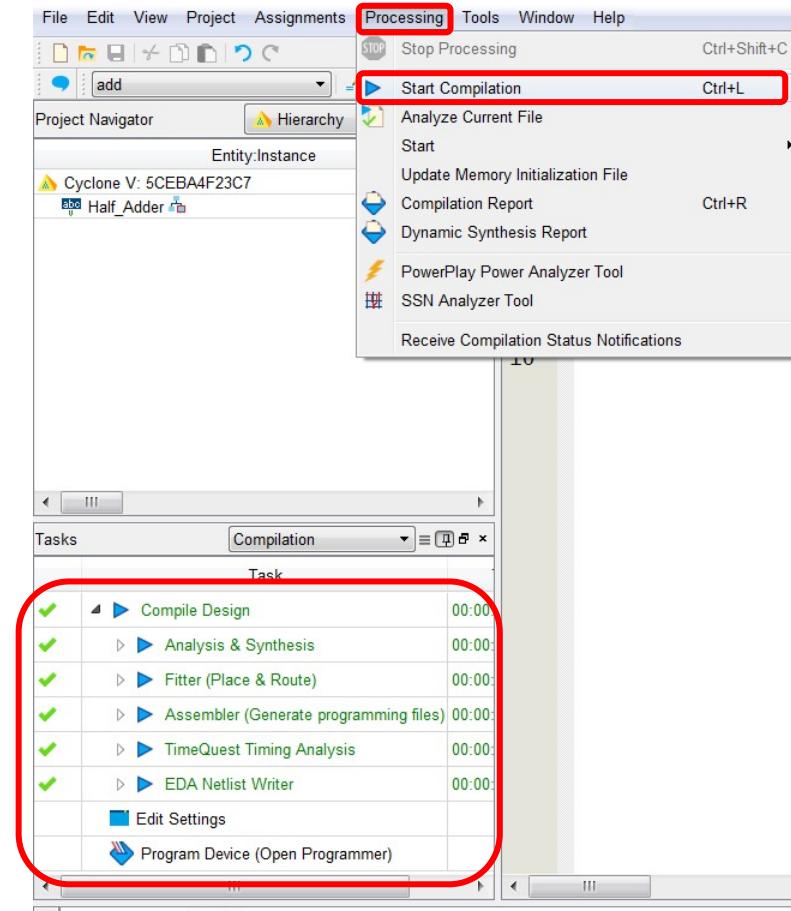
- Video preview for 晶片實現+HDL介紹(Parts II~IV)
- Quartus II tutorial
- Introduction to DE0-CV
- **Programming DE0-CV**
- Lab I – adder-subtractor to DE0-CV
- Lab II – encoder to DE0-CV

Programming DE0-CV (1/13)

```
1 module Half_Adder(a, b, sum, carry);
2   input a,b;
3   output sum, carry;
4   and(carry,a,b);
5   xor(sum,a,b);
6
7 endmodule
```

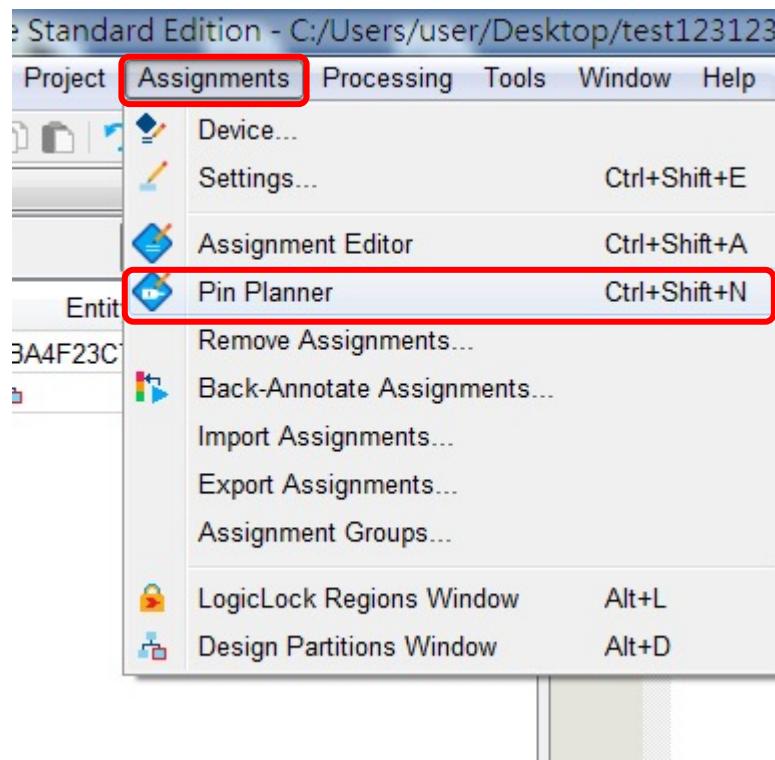
Programming DE0-CV (2/13)

■ Start compilation



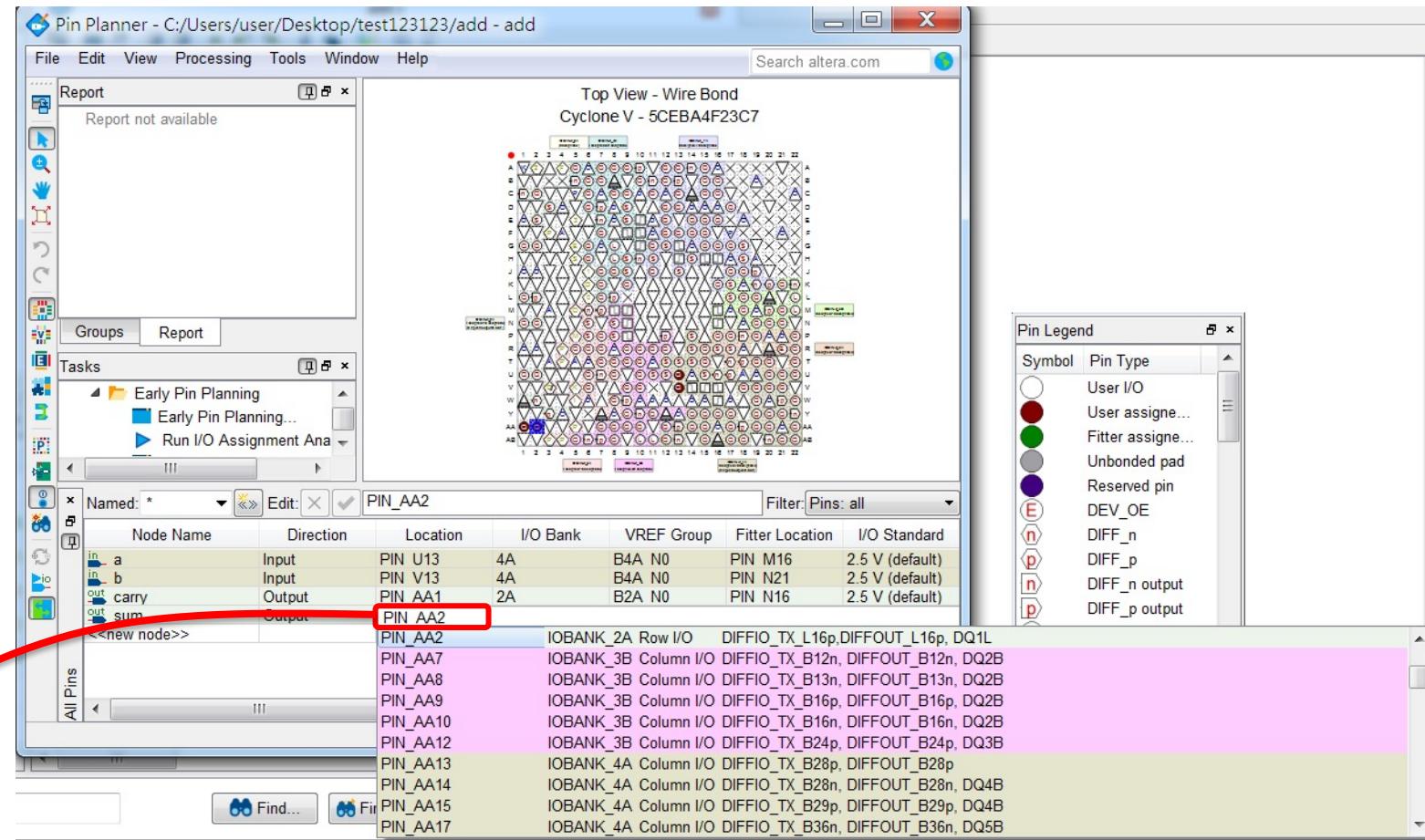
Programming DE0-CV (3/13)

■ Open Pin Planner



Programming DE0-CV (4/13)

■ Pin assignment



Double click

Programming DE0-CV (5/13)

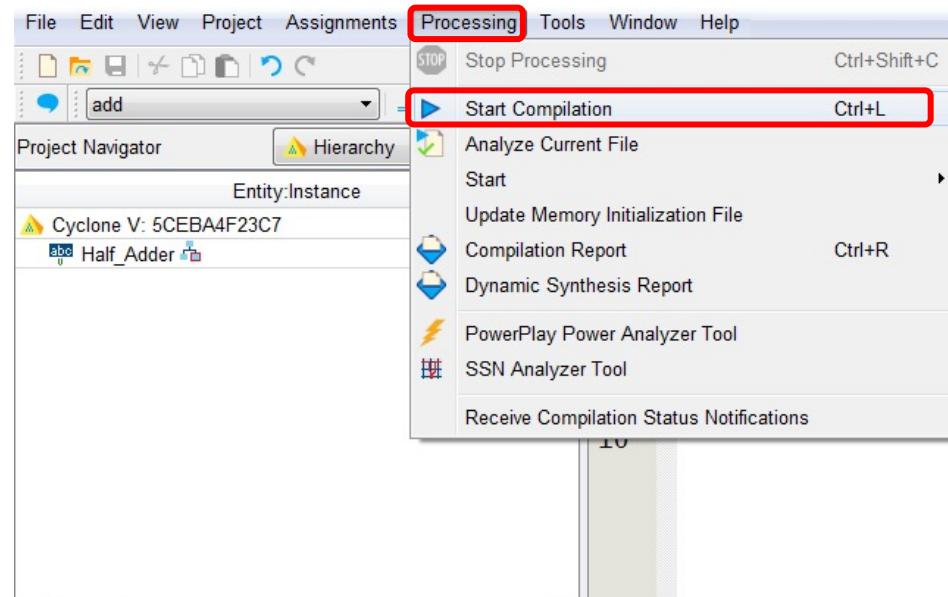
- Assign pin location to all inputs and outputs

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard
in a	Input	PIN U13 SW0	4A	B4A N0	PIN M16	2.5 V (default)
in b	Input	PIN V13 SW1	4A	B4A N0	PIN N21	2.5 V (default)
out carry	Output	PIN AA1 LED1	2A	B2A N0	PIN N16	2.5 V (default)
out sum	Output	PIN AA2 LED0				

- Please refer to DE0_pin.xls for pin location assignment

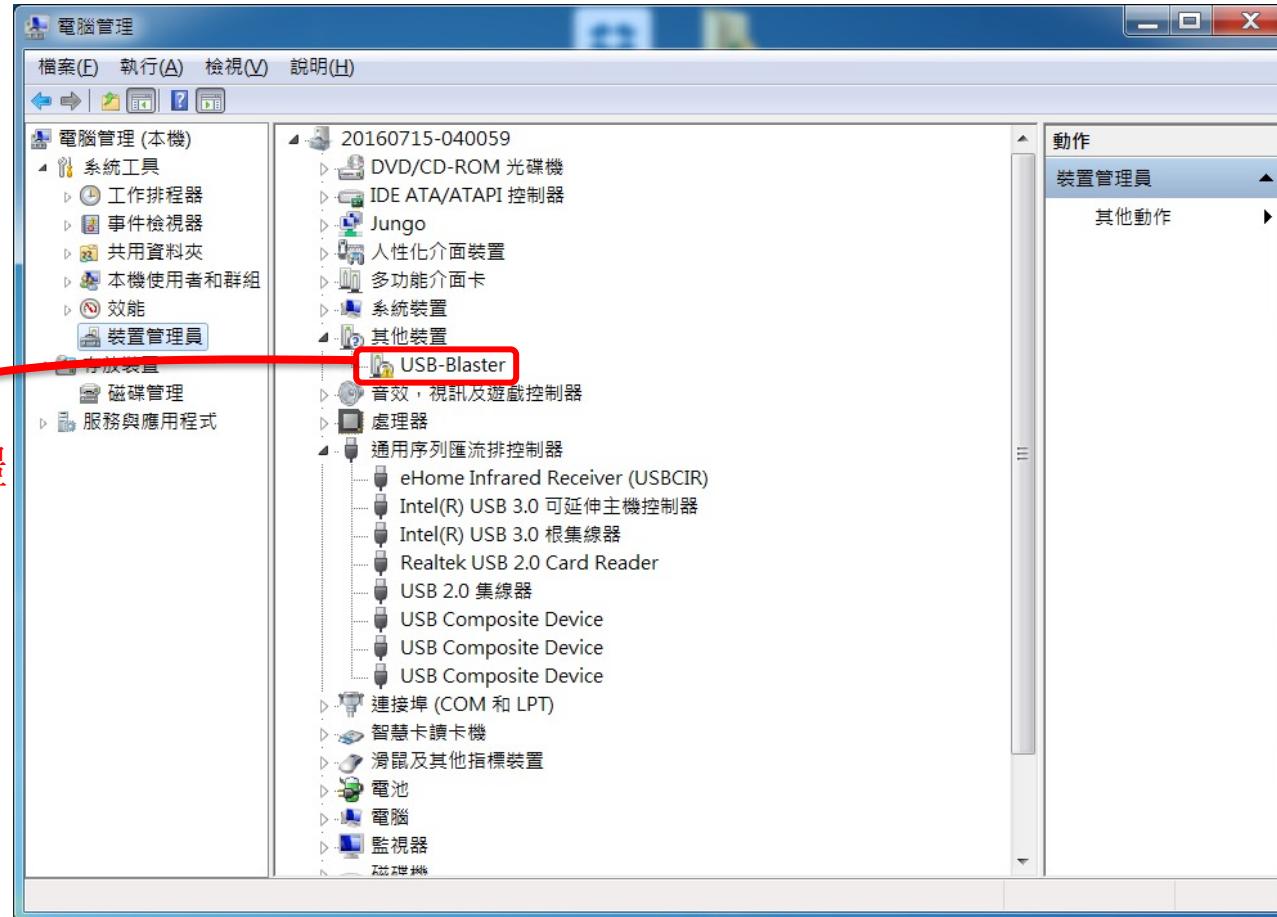
Programming DE0-CV (6/13)

■ Start compilation

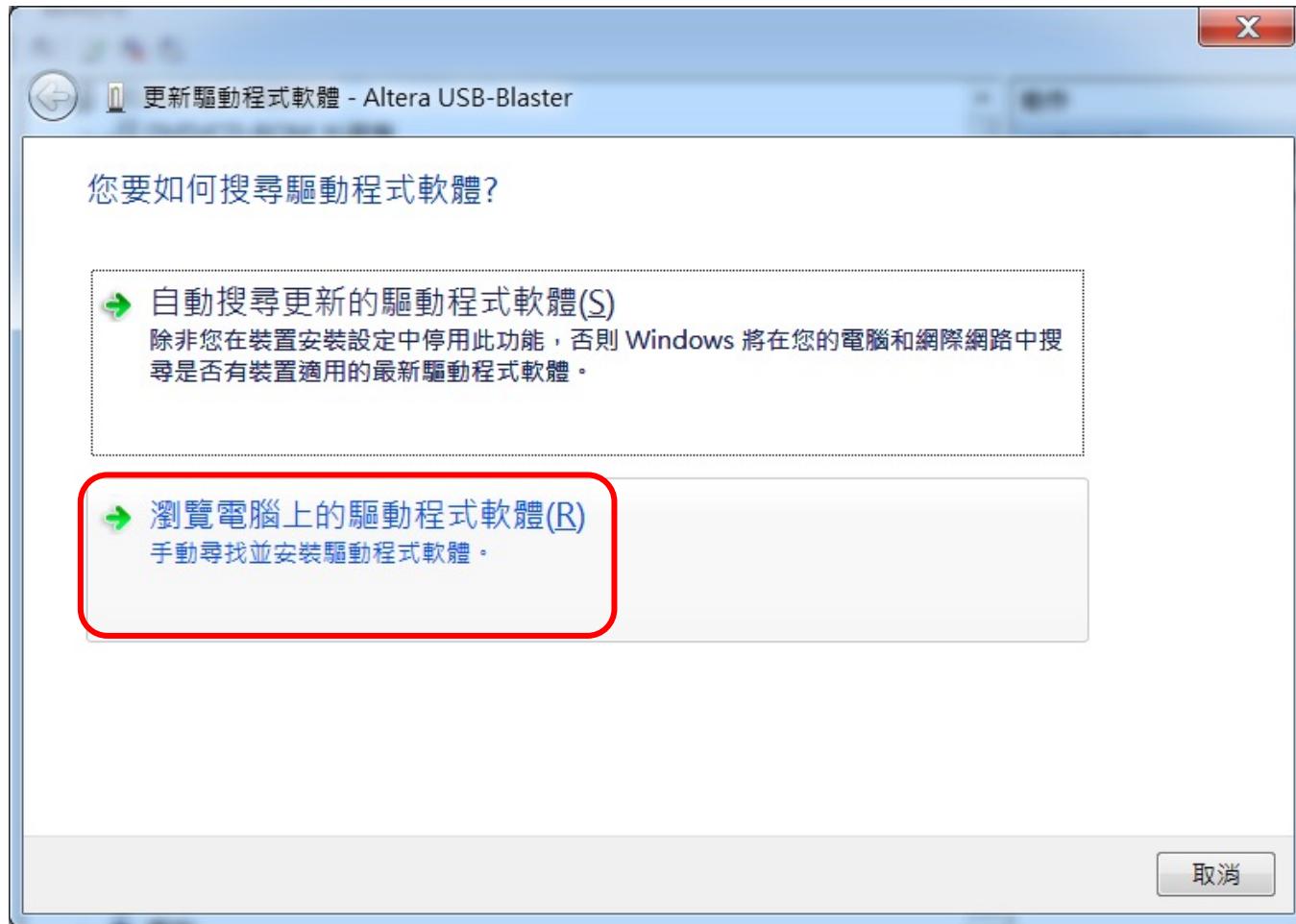


Programming DE0-CV (7/13)

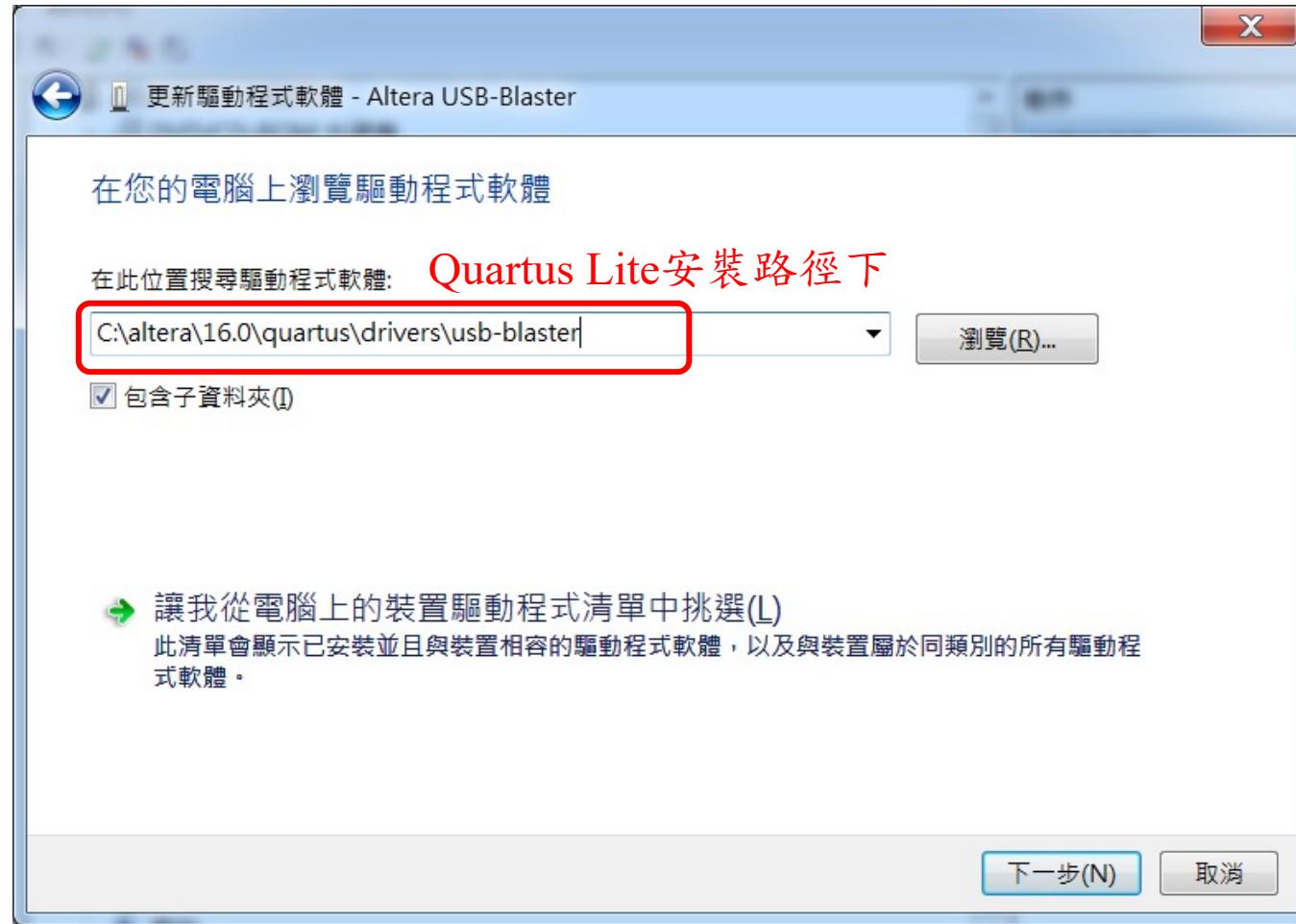
右鍵選更新驅動程式軟體



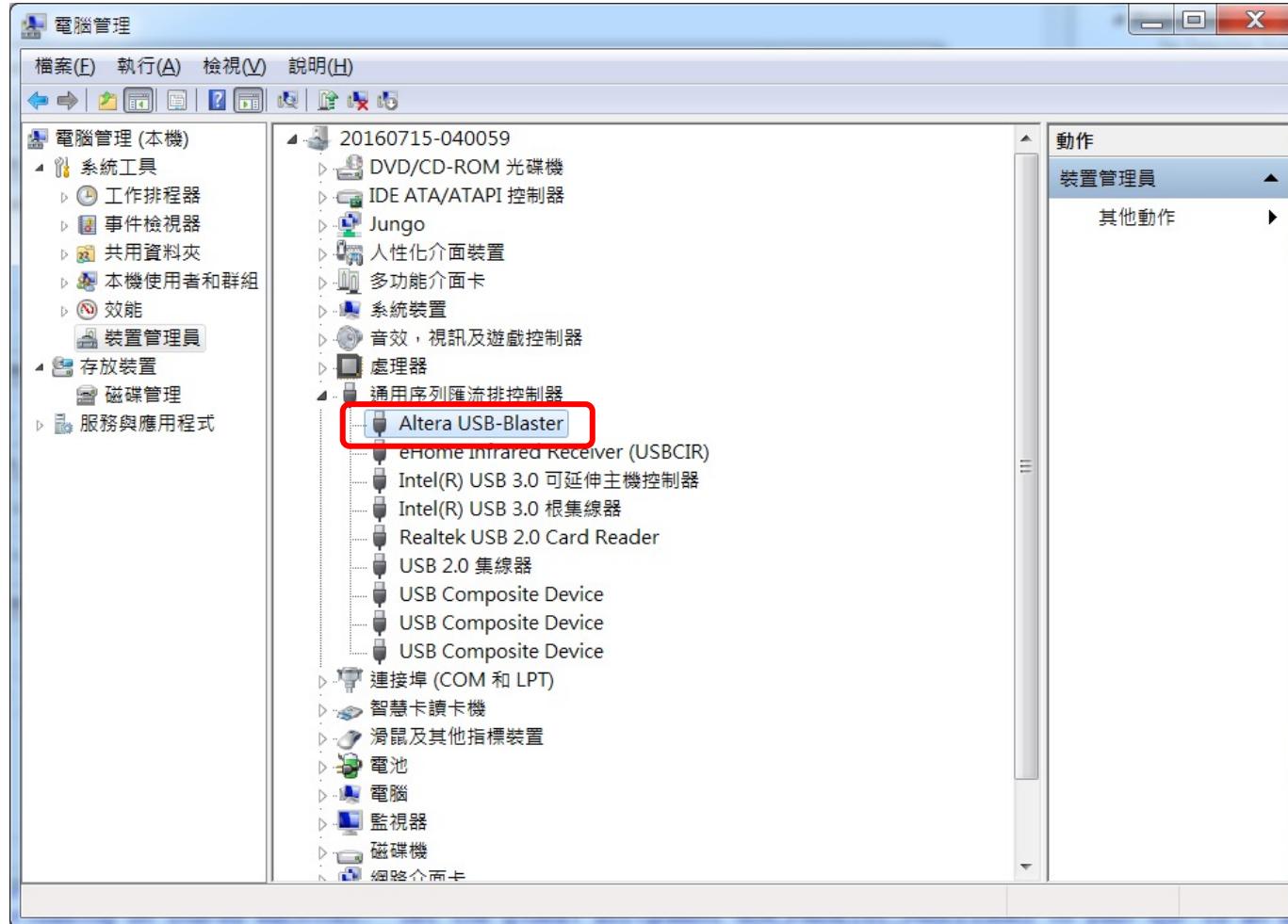
Programming DE0-CV (8/13)



Programming DE0-CV (9/13)

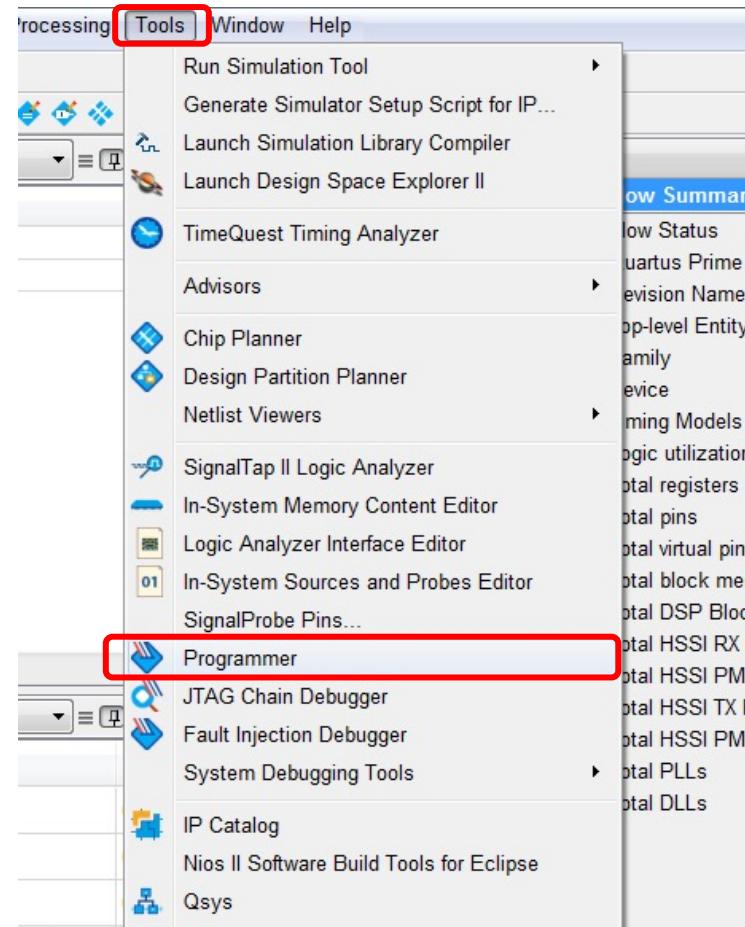


Programming DE0-CV (10/13)



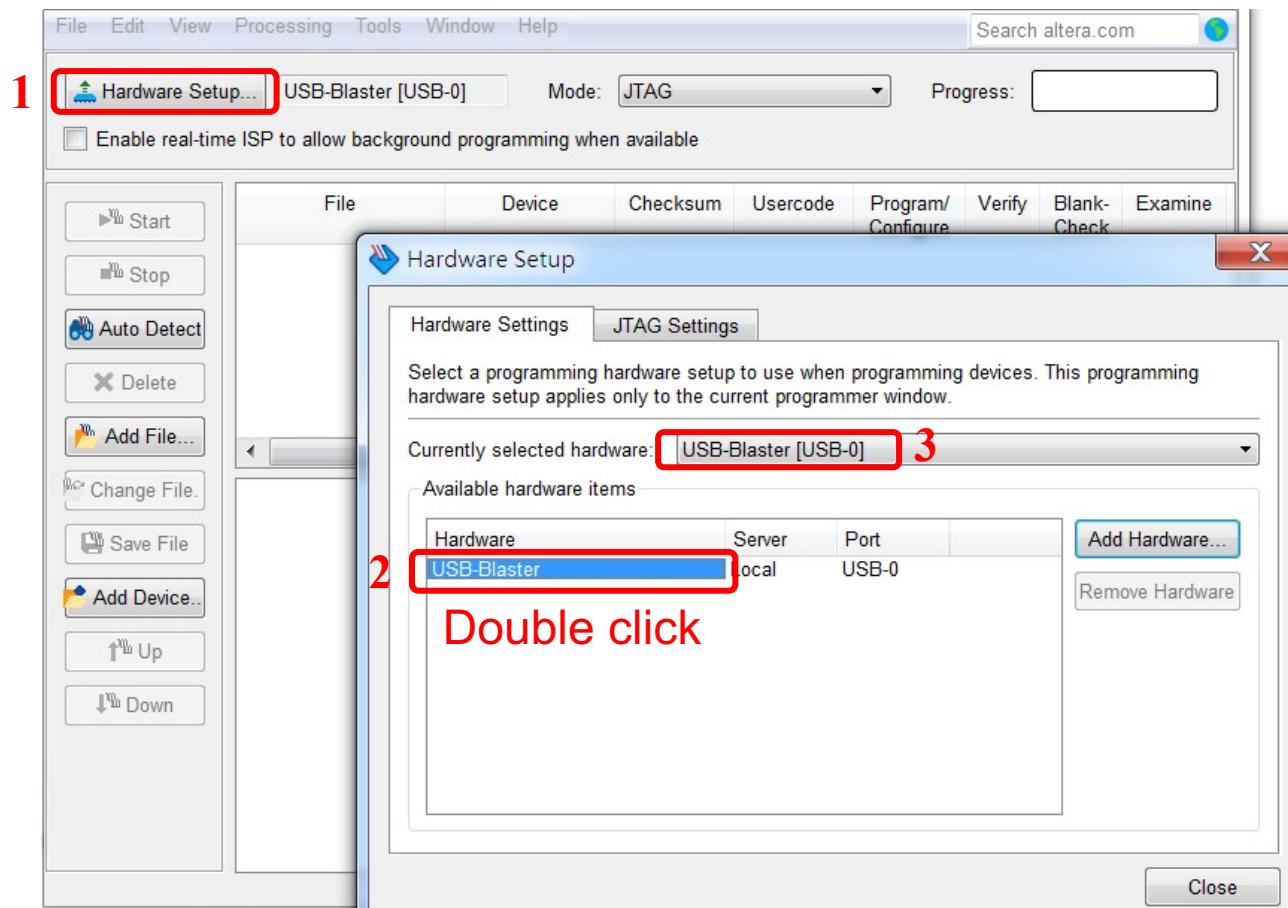
Programming DE0-CV (11/13)

■ Programming device



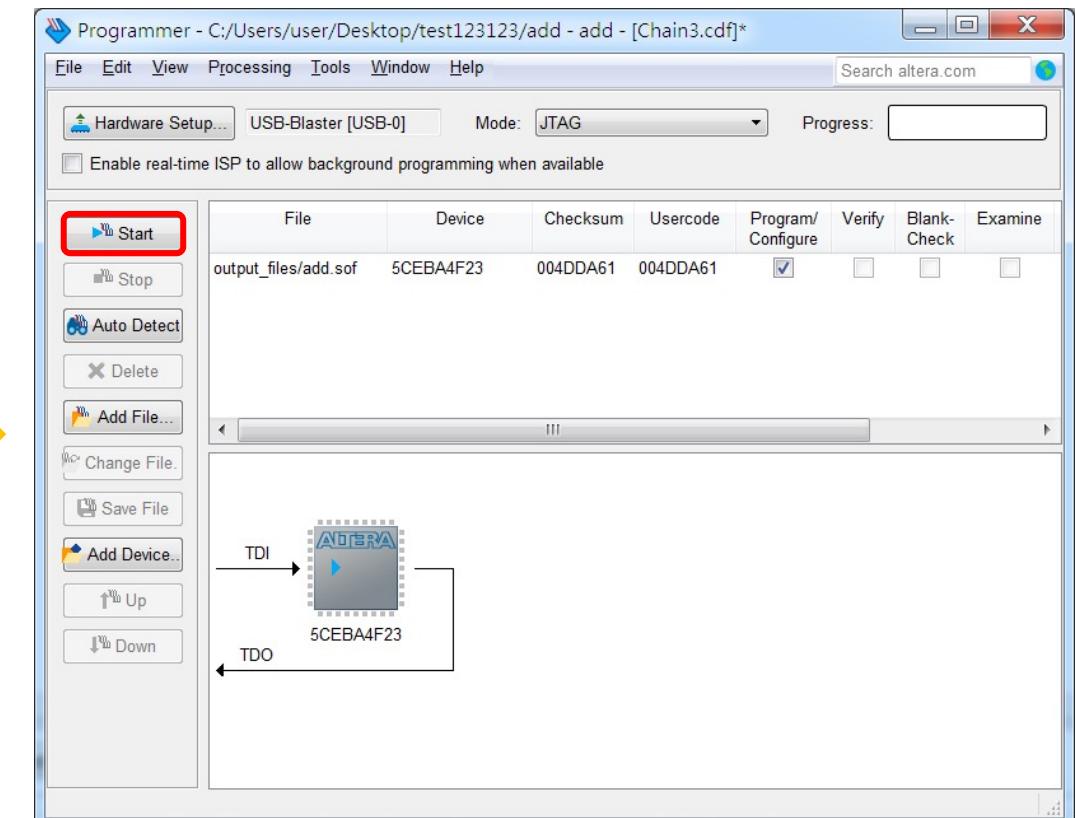
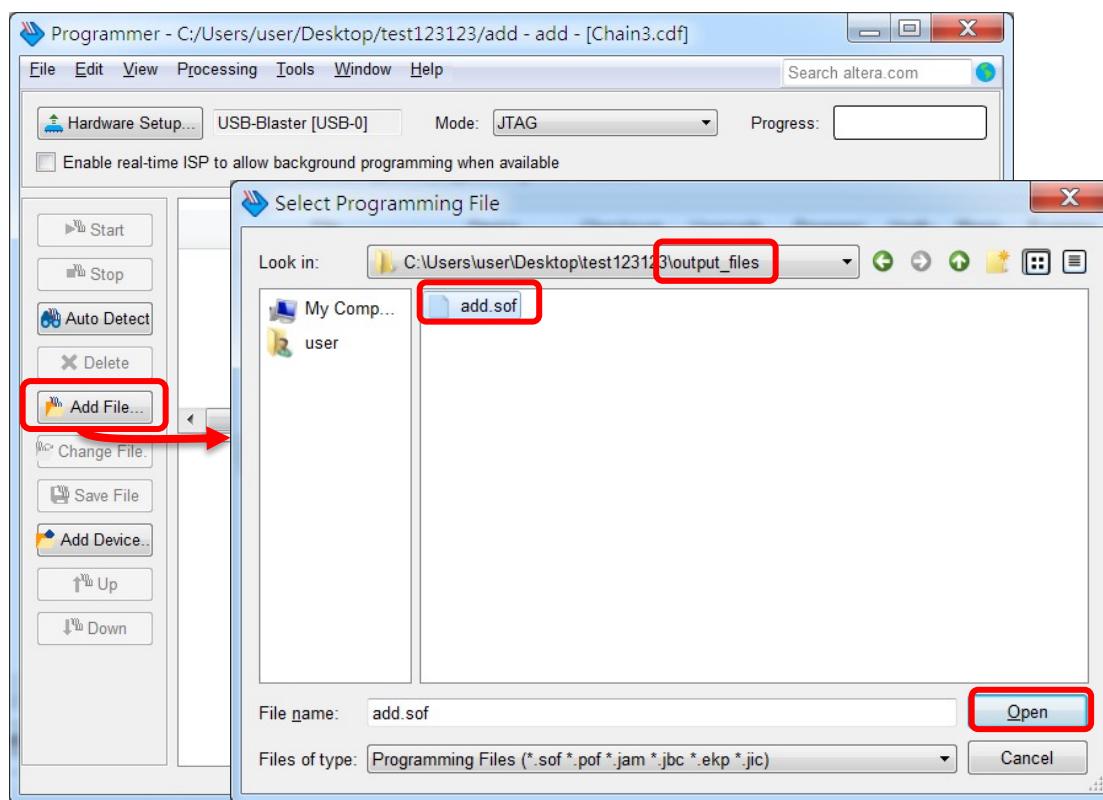
Programming DE0-CV (12/13)

■ Hardware setup: add USB-Blaster



Programming DE0-CV (13/13)

■ Programming device

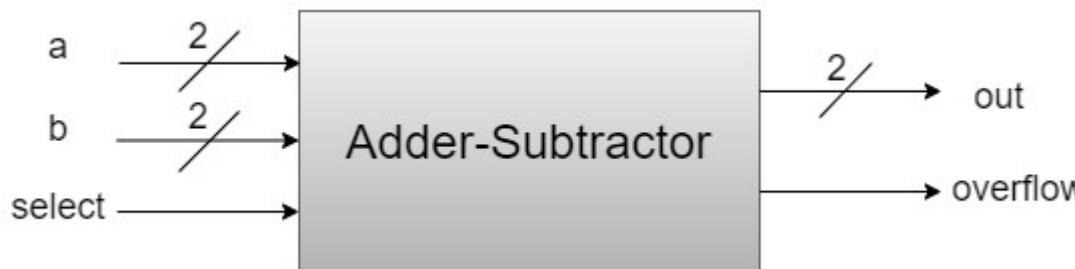


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Lab I -- Adder-Subtractor to DE0-CV

- 請設計一 2-bit 無號數加減法器，並燒錄至DE0-CV開發板
 - Input: a(2 bits)、b(2 bits)、select(1 bit)
 - Output: out(2 bits)、overflow(1 bit)
- 無號數加減法器藉由選擇(select)訊號決定進行加法或減法運算
 - select訊號為1時，out輸出 $a + b$
 - select訊號為0時，out輸出 $a - b$
 - 溢位(overflow)訊號用來表示有無進位或借位



Lab I -- Adder-Subtractor to DE0-CV

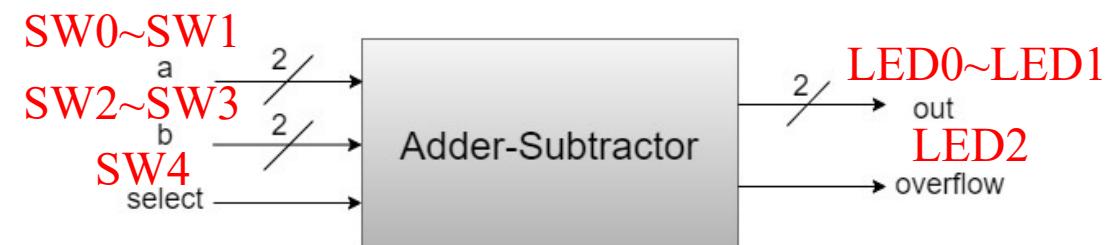
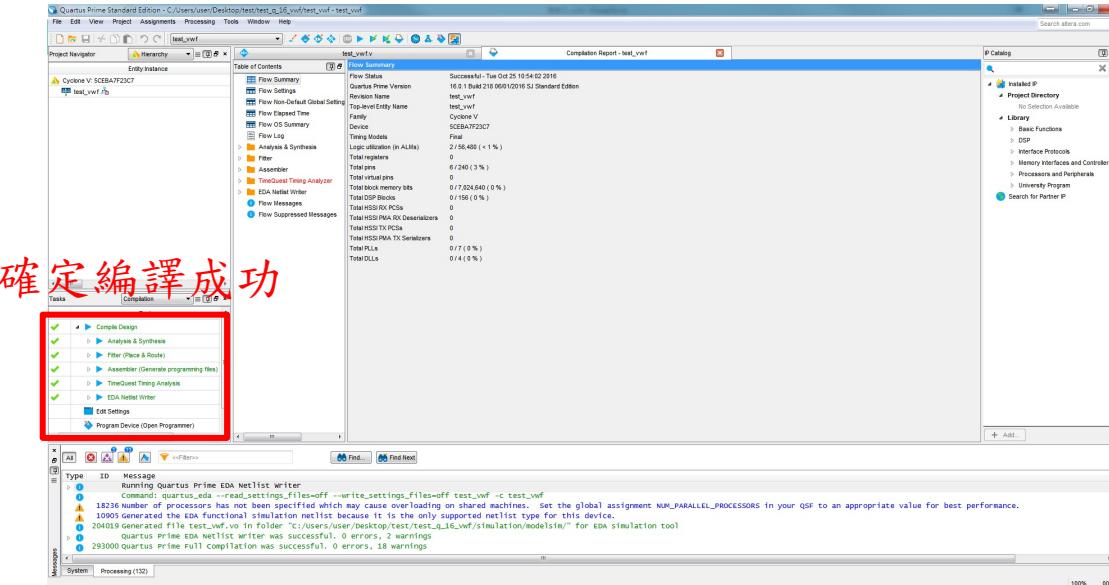
■ Hint:

- 可利用三元運算子或behavior description 中的if-else語法來依照select訊號完成電路
- 可使用concatenation來簡化運算
- 電路運作模式參考1-bit 加減法器之真值表

輸入 (input)			輸出 (output)	
被加減數 (a)	加減數 (b)	選擇 (select)	和 / 差 (out)	溢位 (overflow)
0	0	0	0	0
0	0	1	0	0
0	1	0	1	1
0	1	1	1	0
1	0	0	1	0
1	0	1	1	0
1	1	0	0	0
1	1	1	0	1

Lab I -- Adder-Subtractor to DE0-CV

- 完成verilog電路設計後，需先確認其在Quartus可順利編譯，再將其燒錄至DE0-CV開發板進行驗證
- 使用Switch(SW0~SW4)控制input訊號，使用LED(LED0~LED2)表示output



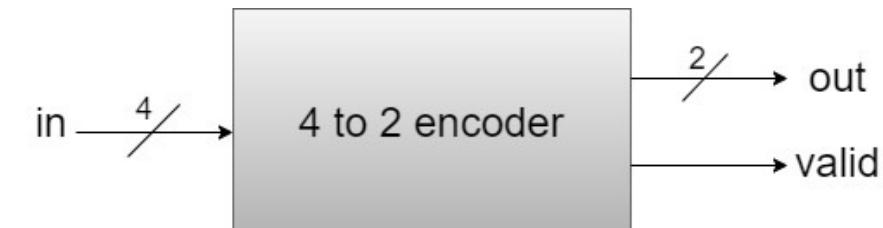
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Lab II -- encoder to DE0-CV

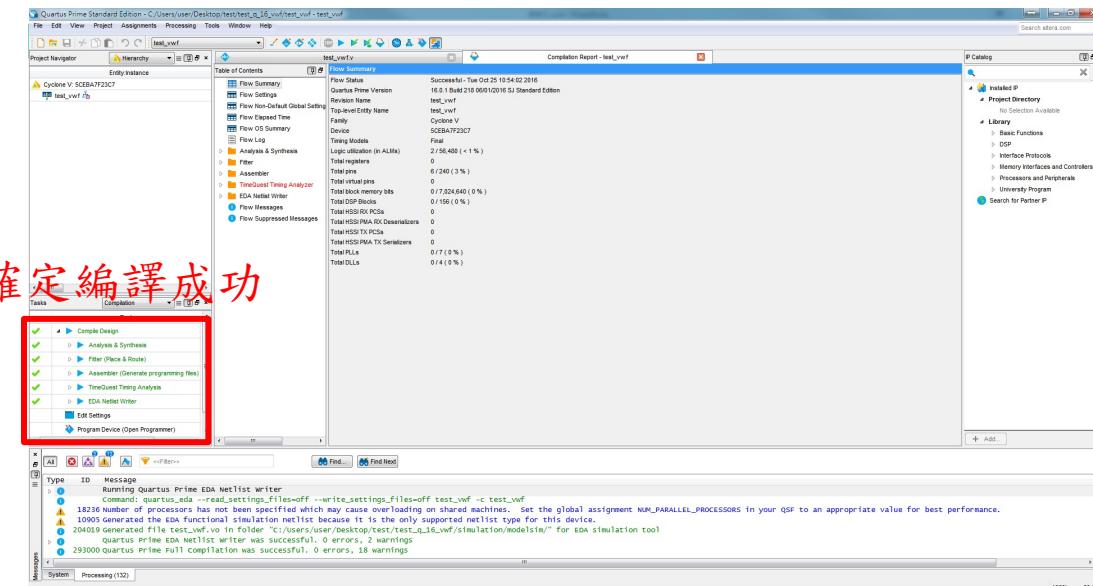
- 請設計一4對2編碼器(4 to 2 encoder)
- 編碼器可以將 2^n 個輸入訊號轉換成n位元輸出訊號，假設有m個輸入與n個輸出，則稱為m對n編碼器
- Hint: 可使用behavior description之case語法實作

輸入(input)				輸出(output)		
in[3]	in[2]	in[1]	in[0]	valid	out[1]	out[0]
0	0	0	1	1	0	0
0	0	1	0	1	0	1
0	1	0	0	1	1	0
1	0	0	0	1	1	1
其餘的輸入情況				0	0	0

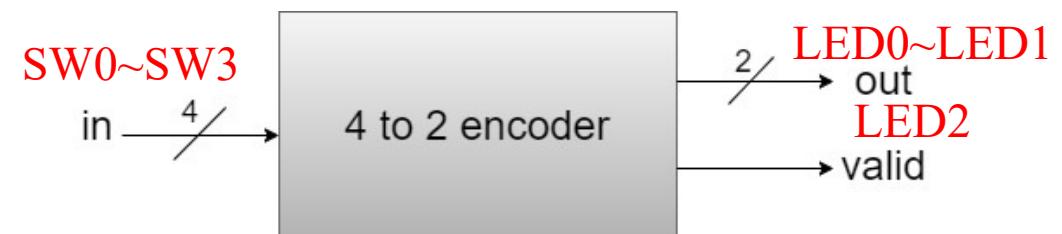


Lab II -- encoder to DE0-CV

- 完成verilog電路設計後，需先確認其在Quartus可順利編譯，再將其燒錄至DE0-CV開發板進行驗證
- 使用Switch(SW0~SW3)控制input訊號，使用LED(LED0~LED2)表示output



確定編譯成功



Notice

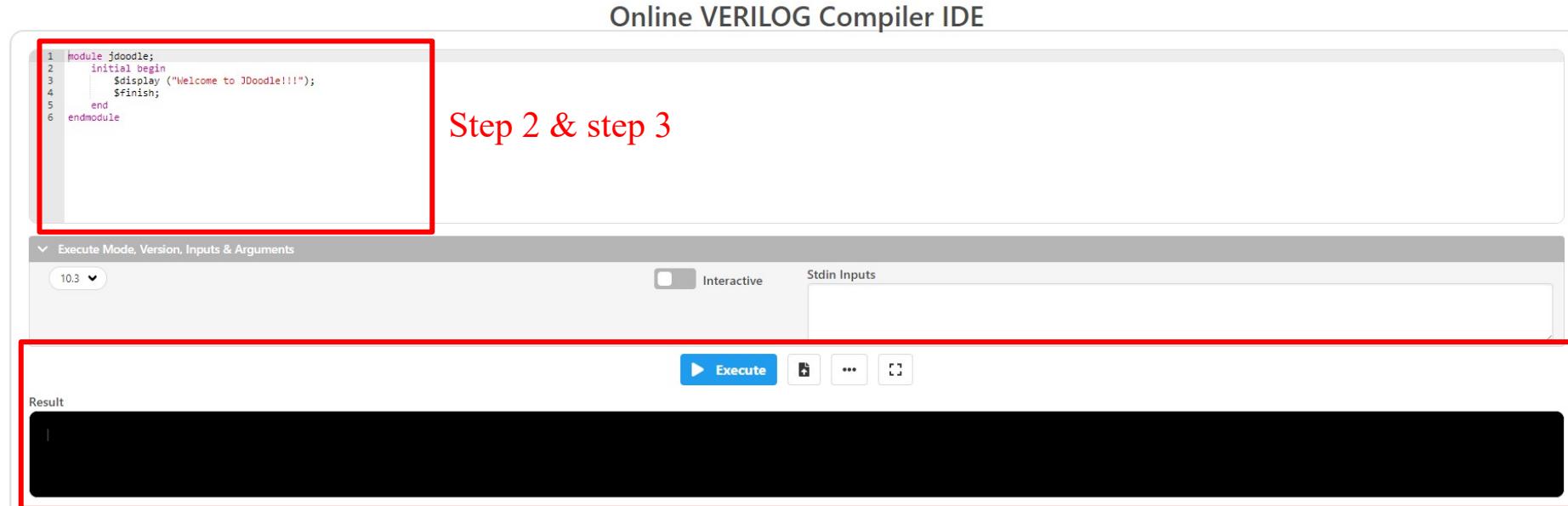
- 請勿命名中文資料夾
- Device family 請確認與 FPGA Chip 符合 (**5CEBA4F23C7**)
- Top module name & Project name 需要一致

Appendix

■ 為了幫助同學驗證程式是否正確，moodle上有提供testbench

■ 驗證方式：

- Step 1: 前往verilog線上模擬網站: <https://www.jdoodle.com/execute-verilog-online/>
- Step 2: 將moodle上的testbench code整段貼上
- Step 3: 修改adder_subtractor/encoder module
- Step 4: 按下Execute按鈕，確認模擬結果是否正確



Appendix

■ Lab 4-1 模擬結果

Result

CPU Time: 0.00 sec(s), Memory: 7248 kilobyte(s)

```
a = 0, b = 0, select = 1; a + b = 0, no overflow
a = 1, b = 1, select = 1; a + b = 2, no overflow
a = 3, b = 1, select = 1; a + b = 0, overflow
a = 0, b = 1, select = 0; a - b = 3, overflow
a = 2, b = 2, select = 0; a - b = 0, no overflow
a = 1, b = 3, select = 0; a - b = 2, overflow
```

Appendix

■ Lab 4-2 模擬結果

Result

CPU Time: 0.00 sec(s), Memory: 7156 kilobyte(s)

```
in = 0001; Output is valid, out = 00
in = 0010; Output is valid, out = 01
in = 0100; Output is valid, out = 10
in = 1000; Output is valid, out = 11
in = 0000; Output is not valid, out = 00
in = 1111; Output is not valid, out = 00
```