Project

Circuits and Systems for Radio-Frequency

Design of an RF-CMOS front-end for a Low Data Rate Digital Receiver

October 2024
Version 1.0

1- Introduction

Starting from a reference architecture associated with a Zero or Low-IF RF receiver, depicted in Fig. 1, the project has the objective to design and simulate a complete RF front-end (RFFE), using a 65nm CMOS technology.

The design of the complete receiver is a complex task that should start by gathering all the required specifications ranging from application/system level up to electronic components and circuits.

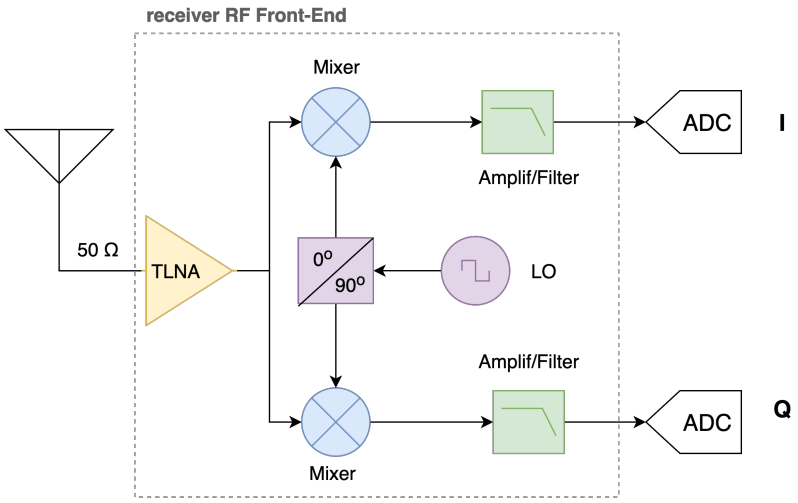

Figure 1- Simplified block diagram of a Direct and Low-IF Conversion Receiver.

Based on the collected specifications, the next step of the design is to select the architecture, between the Zero-IF or low-IF. Then the requirements for each building block of the RF Front-End are determined to allow the sizing of each circuit, which should be selected previously.

The project of the RFFE involves the design of several building blocks, namely:

- Low-noise amplifier: the inductive degenerated common source topology can achieve very low noise figures;
- Mixer: use a current-driven passive mixer;
- Baseband or Low-IF low-pass (or bandpass) filter;
- Baseband or Low-IF amplifier: dependent on the level of amplification incorporated (or not) in the low-pass filter;
- Local Oscillator (LO) with drivers:
    - For the groups with two students: assume that the oscillator is ideal and it is only needed to design the LO output drivers.
    - For the groups with three elements: design the oscillator with output drivers and phases generator.

2- Specifications / design requirements

- TX power : 0 dBm
- Distance : 40 m
- Modulation: FSK/ASK, 40kbps and BER=10e-4
- Battery : 2000 mAh
    - Autonomy: 30 days considering 10% node operation. When in operating mode, the RF front-end part is active 40% of the time.
- ISM/MICS/WTMS bands: each group selects one center frequency.
- Narrowband
- Technology: CMOS 65 nm
- Inductors, resistors, and capacitors from the 65 nm design kit
    - Consider an approximate model of the on-chip inductor with parasitic capacitances; CP of 10 fF; also, consider an on-chip inductor quality factor of 7. You can fine-tune these values by checking the 65 nm design kit;
    - Due to area constraints, limit the total inductance;
    - On-chip capacitor with a bottom-plate parasitic capacitance of 4%.
- if Low-IF architecture, then IF should be <=10MHz
- VDD = from 0.7 to 1.2 V
- Zo=50 Ω
- P1dB > -10 dBm
- IIP3 >= -16 dBm
- IIP2 >= 10 dBm

3- Design and Validation

65 nm CMOS technology Design and simulation process

The design process should include the determination of the circuit equations (or design tables) from which the device sizes are calculated (e.g., W, L, capacitance, inductance, resistance). The operation and performance achieved by the designed circuits should be confirmed through SpectreRF (Cadence) simulation using BSIM V4 transistor models. Also, the transistors that must process RF signals should be the ones with RF transistor layout (check 65nm component library).

The SpectreRF simulator from Cadence design framework includes the Periodic Steady State (PSS) analysis which is capable to simulate efficiently time-variants circuits. It is expected that the following simulation be performed:

- Distortion, non-linear
- noise simulation (e.g., through PNOISE option)
- PVT simulation for one or more building blocks. (optional: Monte-Carlo)

Create a set of “testbenches” to simulate the behavior of your design under various conditions and input stimuli. A test bench serves as an environment or simulation setup in which you can verify the functionality and performance of your electronic designs.

The final report should address a deep and detailed analysis and description, including the theoretical background, the design and the simulation of the RF Front-End. As a general indication, the report should include, clearly:

- Specifications and requirements for each building block, namely, in terms of Noise, Linearity, Sensitivity, Power consumption, and estimated chip area, among others;
- Detailed theoretical analysis of the system and building blocks, including noise analysis, linearity analysis (1dB compression point, IIP2, and IIP3)
- If applicable, high-level simulations (Octave, scilab, Python, etc);
- Electrical simulations using realistic models of the components;
- Include a comparative analysis between theoretical and simulation results.
- As general requirement, include PVT and (Monte Carlo, optional) simulation for one or more building blocks.

Besides the general indications given above, the following list of topics/information should be considered (note: for most of the items it is expected that the content of the report includes detailed theoretical analysis and simulations)

For the LNA

- Type of topology:
  - A Common source (CS) is suggested but a common gate (CG) can also be chosen
- Region of operation of the transconductor
  - Weak, moderate or Strong Inversion
- Type of input:
  - single ended or differential
- Type of output:
  - single ended or differential
  - voltage or current mode
- Noise figure
- Voltage Gain
- Input matching
  - 50 Ω? Level of S11 (level of matching)
- Power consumption
- 1 dB compression point
- Linearity: IIP3 and IIP2,
- Estimated area

For Mixer (including the TIA)

- Type of topology/operation:
  - Passive: current-mode; (preferentially)
  - (if adequately justified, an active mixer can be selected)

- Conversion Gain;
- Linearity: IIP3 and IIP2;
- Noise analysis;
- For the TIA:
    - Incorporate a first-order filter
- A clear indication should be given for the requirements of the buffers which drive the mixer switches;
- Power consumption;
- Estimated area.

For Local Oscillator

- For the groups with 2 students
    - ideal oscillator
    - design the output drivers
- For the groups with 3 students
        - Design the oscillator.
        - Type of topology/operation: Ring oscillator or LC oscillator
    - Design the output drivers
- Estimated area

For IF/BB amplifiers, filters, …

- Gain
- Bandwidth;
- Filter order
- Linearity analysis
- Noise analysis
- Gain programmability (optional);
- Operation region of the transistors;
    - Weak, moderate or Strong Inversion;
- Power consumption and estimated area;
- This stage can be implemented as a cascade structure;

For the full front-end receiver

The full RF front-end should be simulated as a complete and unique system block:

- Gain of the full RF front-end;
- Total noise figure and verify if it is compliant with the initial requirements;
- 1 dB compression point, P1dB;
- Linearity: IIP3 and IIP2;
- Total power consumption.
- Use an adequate input signal type and dynamic range to test the complete RF front-end.

The list items are a set of results that should be included in the report. However, additional characterization and analysis will be positively graded and strongly recommended.

4- LNA Layout (optional)

Proceed with the layout of the LNA, including real inductors available from the process design kit.

5- Evaluation

The complete RF Front-End should be designed and simulated. The final report should be delivered by the end of the semester (check dates on moodle). The project evaluation includes:

- Final report, calculation files (octave, excel, python, etc.) and design database
- Presentation, Q&A session (both in group and individually)

Classification options:

Option A: Up to 17.3: single ended version of the receiver.

Option B: Up to 20: (fully) differential version of the receiver, including I/Q mixer and LNA layout.