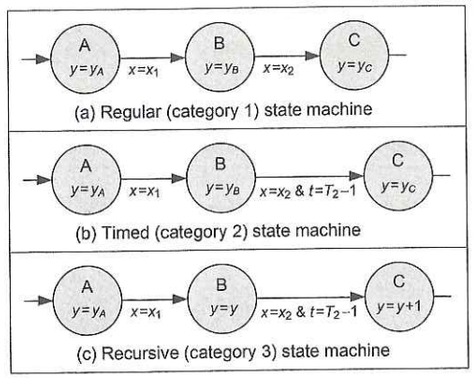


Figure 8.1
State machine categories (from a hardware perspective).

2) The state machine type (Moore or Mealy).

It is important to recall, however, that regardless of the machine category and type, the state transition diagram must fulfill three fundamental requisites (seen in section 1.3):

1) It must include all possible system states.
2) All state transition conditions must be specified (unless a transition is unconditional) and must be truly complementary.
3) The list of outputs must be exactly the same in all states (standard architecture).

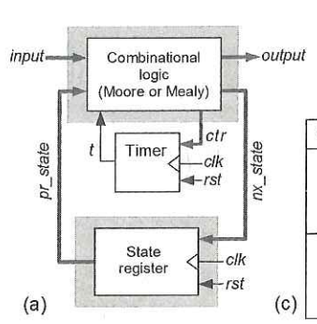
8.2 Architectures for Timed (Category 2) Machines

The general architecture for category 2 machines is summarized in figure 8.2a. This representation follows the style of figures 3.1b and 3.1d, but the style of figures 3.1a and 3.1c could be used equivalently. The output register (figure 8.2b) is still optional, but the timer (in figure 8.2a) is compulsory.

Note that the timer operates as an auxiliary circuit, producing the signal *t*, needed by the state machine. However, the FSM itself is responsible for controlling the timer, as represented symbolically by the control signal *ctr* in the figure. In other words, the machine is who decides when the timer should run or stop and when it should be zeroed.

The four possible constructions, listed in figure 8.2c, are summarized below.

Timed Moore machine: The circuit of figure 8.2a is used with the input (if it exists) connected only to the logic block for the next state, as in figure 5.2a. Consequently, it behaves exactly as a pure Moore machine, just with an auxiliary timer operating as



Construction	Resulting category 1 circuit	Behavior
(a) only	Timed Moore machine (preferred)	Order-1 synchronous
	Timed Mealy machine	Asynchronous
(a) + (b)	Out-registered (pipelined) timed Moore machine	Order-2 synchronous
	Out-registered (pipelined) timed Mealy machine	Order-1 synchronous

Figure 8.2
Timed (category 2) state machine architectures. (a) Moore or Mealy type (depending on input connections). (b) Optional output register. (c) Resulting circuits.

an extra input. Because the output depends only on the state in which the machine is, this circuit is synchronous (see details in section 3.5). Because modern designs are generally synchronous, this option is preferred over any other timed implementation whenever the application permits.

Timed Mealy machine: Again, the circuit of figure 8.2a is used, but this time with the input connected to both logic blocks (for output and for next state), as in figure 5.2b. Consequently, it behaves exactly as a pure Mealy machine, just with an auxiliary timer operating as an extra input. Because the input–output transfer is asynchronous, this machine can have more than one output value for the same state (see details in section 3.5).

Out-registered (pipelined) timed Moore machine: The extra register of figure 8.2b is connected to the output of the timed Moore machine. As seen in sections 2.5 and 2.6, two fundamental reasons for doing so are glitch removal and pipelined construction. The new output will be one or one-half of a clock cycle (depending on the selected clock edge) behind the original output. The resulting circuit is order-2 synchronous because the original Moore machine was already a registered circuit (in other words, the input–output transfer occurs after two clock edges—see details in section 3.5). If in a given application this extra register is needed but its consequent extra delay is not acceptable, the next alternative can be considered.

Out-registered (pipelined) timed Mealy machine: The extra register of figure 8.2b is connected to the output of the timed Mealy machine. The reasons for doing so are the same as for Moore machines. The resulting circuit is order-1 synchronous because the input–output relationship in the original Mealy machine can be asynchronous. Consequently, the overall behavior (with the output register included) is similar to that of a timed Moore machine without the output register (see details in section 3.5).