Some slides from:
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(EMB3 course 2014)

Robot electronics 2017
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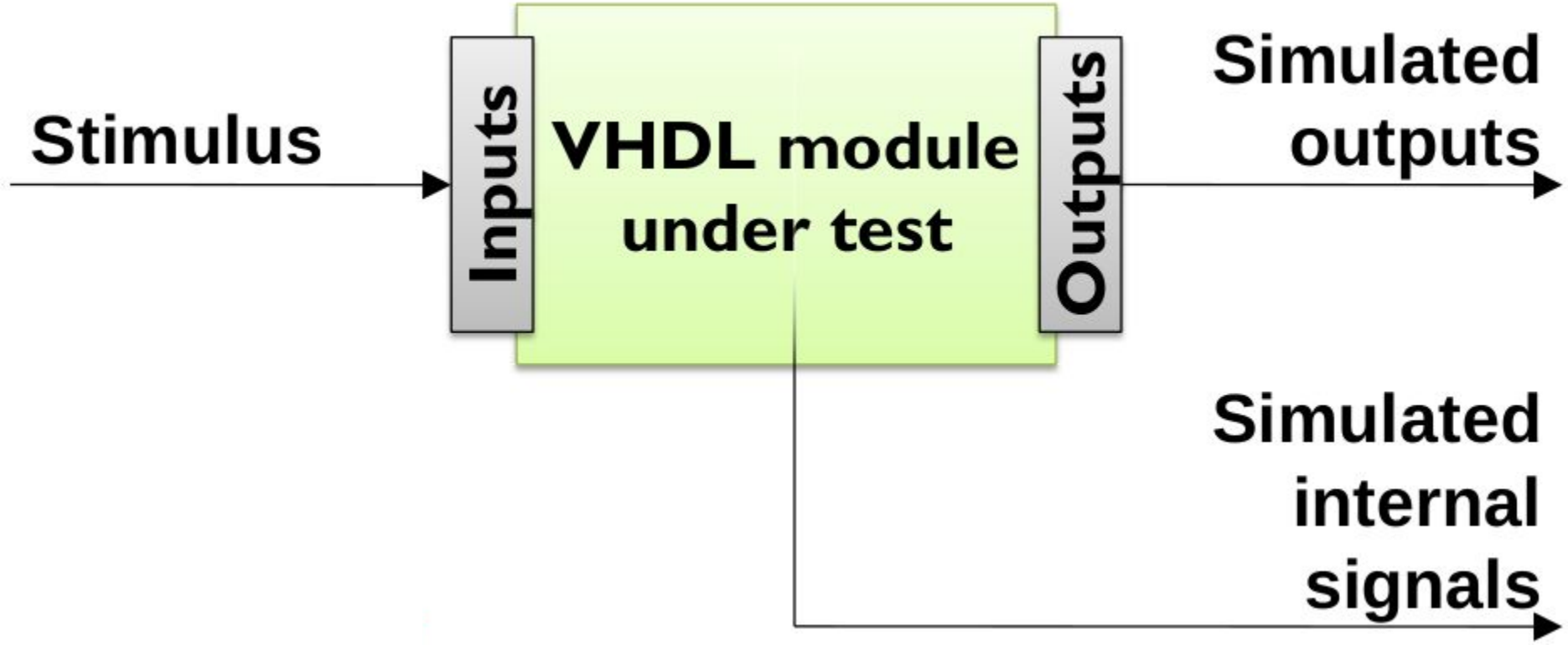
Simulation


Stimulus
Inputs
VHDL module under test
Outputs
Simulated outputs
Simulated internal signals

Creating stimulus

- Manually inside the simulator
- Scripted

- Testbench
  - Basically an extra VHDL module

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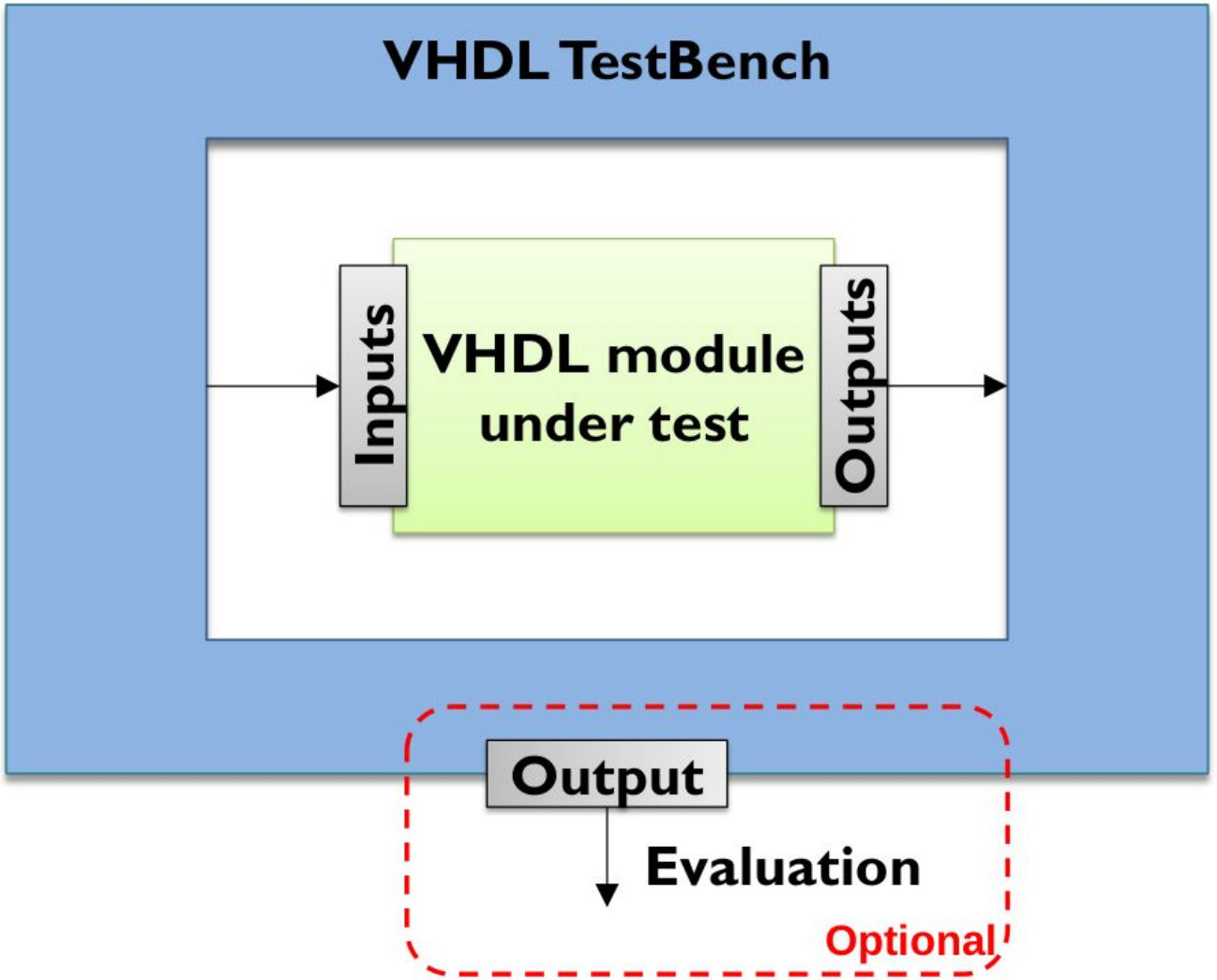
Simulation



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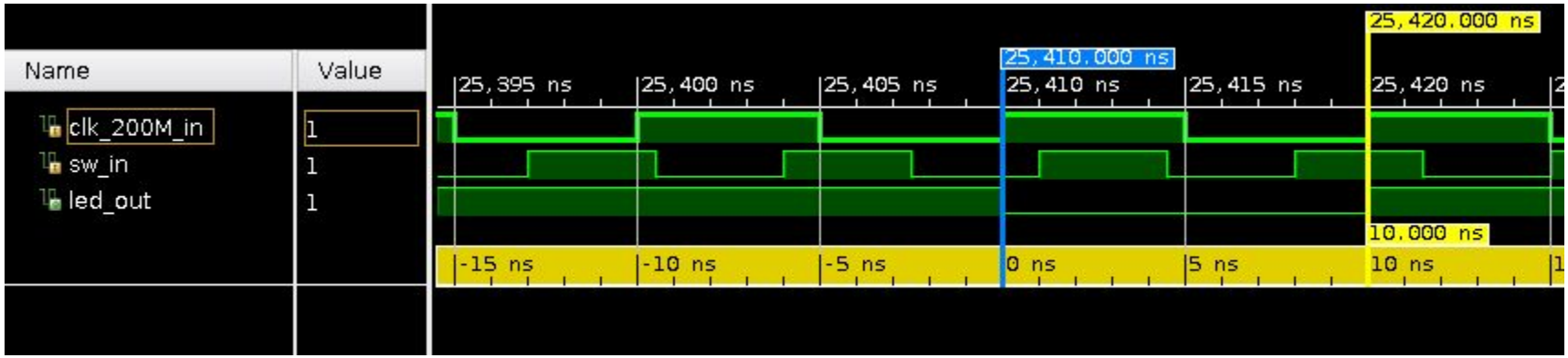
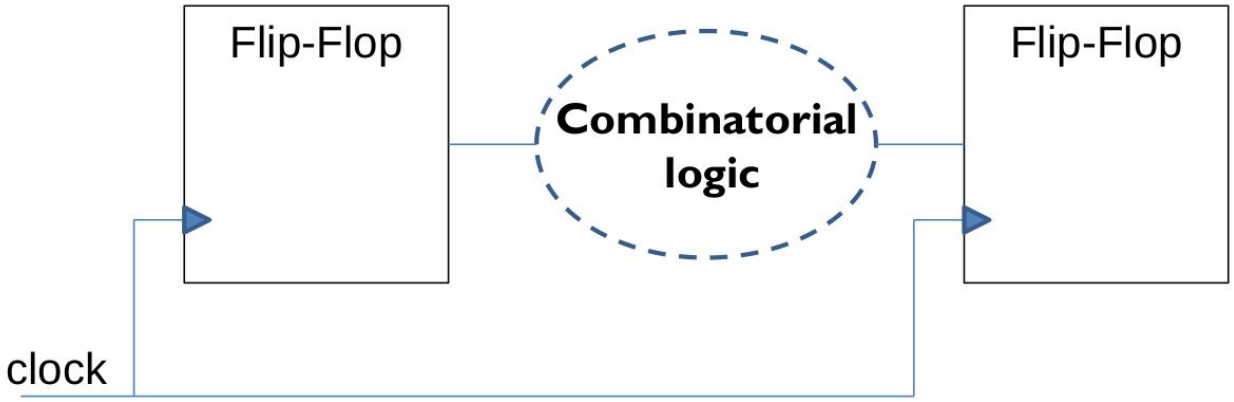
Why simulation?

- Create testbenches for all modules
- Create testbenches based on requirement specification
- Cover all special cases
- Run tests whenever a module is modified
- Good investment of time, especially in medium to large projects



Overall design guidelines

- Timing
  - Maximum frequency
  - Critical path
  - Automatic calculation



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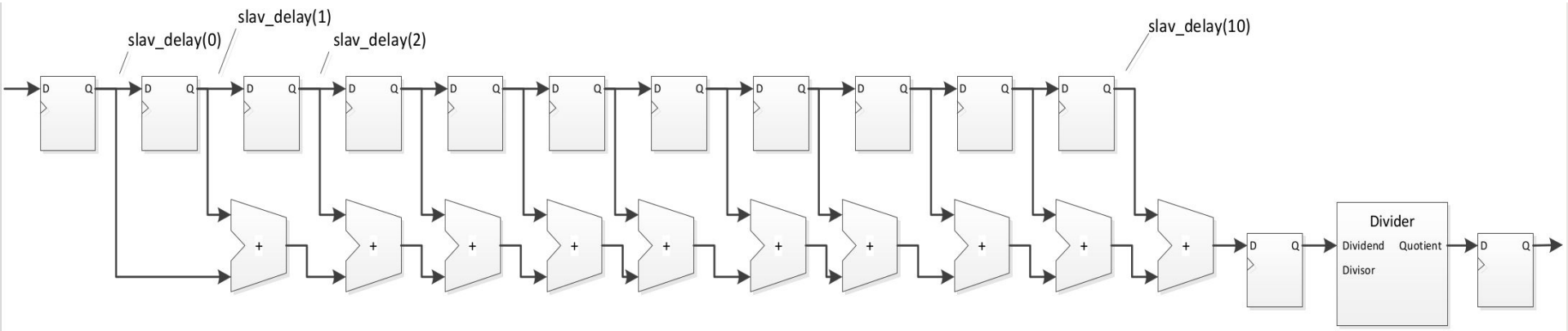
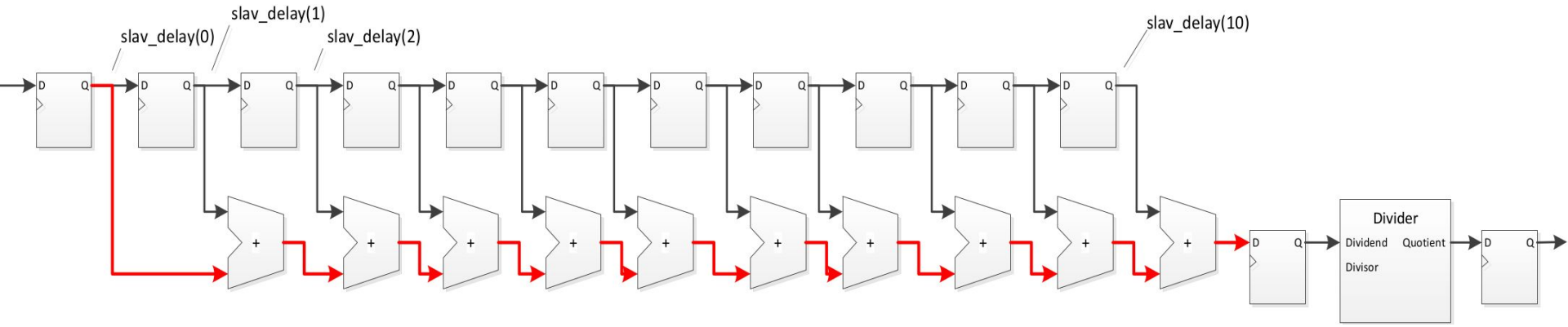
Overall design guidelines

Sliding average filter
Divisor 11



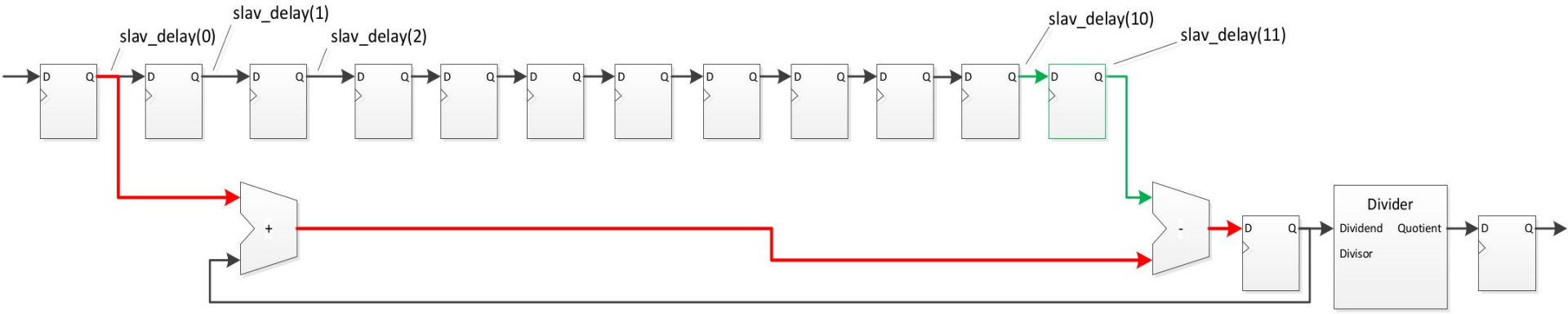
Overall design guidelines

Sliding average filter
Divisor 11



Overall design guidelines

Improved sliding average filter
Divisor 11



Implemented on Spartan 6

Average filter implementation:

- Slice count: 87
- Slice Register count: 475 (MAP: 404)
- Slice LUT count: 214 (MAP: 270)
- Maximum frequency: 147.009 MHz
- Latency: 19 clock periods

Improved Average filter implementation:

- Slice count: 75
- Slice Register count: 424 (MAP: 318)
- Slice LUT count: 145 (MAP: 206)
- Maximum frequency: 409.752MHz
- Latency: 19 clock periods

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