Theoretical and Experimental Behavior of Synchronizers Operating in the Metastable Region

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Abstract—**The interaction problem between asynchronous logic elements is formulated with emphasis on the synchronizer. A detailed analytic treatment of the binary flip-flop action in the metastable region is presented. The principle result is to predict, in a probabilistic manner, the time necessary to move from the metastable point to one of the stable boundaries. The effects of circuit time constant and circuit noise are discussed in detail. Theoretical results are correlated with laboratory measurements and suggestions for acceptable probability of error performance are given.**

Index Terms—**Asynchronous fundamental mode input changes, asynchronous interactions, binary switching time, flip-flop metastable region, glitch, interrupt failure, probabilistic behavior of flip-flops, synchronizer failures.**

I. INTRODUCTION

THE CENTRAL PROCESSORS of most digital computers operate within a time frame specified by a master clock. Such clocked sequential circuits commonly are synthesized in the pulse mode since this makes the design quite straightforward, is easy to implement, and normally produces reliable operation. In particular, a key ingredient in this design technique is the ability to easily manage the delay that is inherent in every logic family. In contrast, using fundamental mode synthesis, the physical circuit delays, which are always present, can cause several internal variables to be simultaneously unstable. If the final state of the circuit depends on the order in which the internal variables stabilize, unreliable circuit operation will result. Pulse mode operation cannot produce such conditions since only single variable changes are allowed.

Nearly all clocked central processors must, however, interact with various peripheral devices, such as remote terminals, teletypes, and console switches. These subsystems do not operate in the time frame of the master clock and therefore their interactions with a central processor are asynchronous. The exchange of information across this interface presents serious design challenges and is usually handled by employing a so-called "synchronizer" whose purpose is to provide reliable communication of data. The basic form for the synthronizer is indicated in Fig. 1, and similar configurations can be found in most digital machines.

The central processor interrogates the external line by generating a clock pulse which is gated with the external level. Since the arrival times of the pulse and level are asynchronous, the output of gate G_1 may be a misshapen pulse. A flip-flop is normally incorporated in the circuit in an attempt to correct for such misshapen or "runt" pulses. The assumption is thus made that the flip-flop will be in a stable state at a specified time after the trigger pulse is applied, even if the pulse is misshapen. A delayed clock pulse is then gated by the flip-flop output to produce, in this example, an interrupt signal to the central processor.

This assumption of guaranteed flip-flop stability in a specified time is not always valid and the use of settling time based on either the manufacturer's specifications or the behavior for a few experimental observations may be incorrect. Catt [2] has shown qualitatively that for certain trigger pulse energy levels a *metastable* state is maintained for an indeterminate period of time. Chaney and Littlefield [3] have measured the metastable action of some integrated circuit flip-flops and a photograph from their experimental studies is reproduced in Fig. 2. Each trace represents the output voltage of the bistable versus time for one trigger pulse. Note that the trigger pulse drives the output to a semistable or metastable voltage and at some *random* time later, the output voltage finally leaves the metastable point and reaches one of the two stable states (that is a "0" or a "1"). As a result of this uncertain flip-flop action, indicated by signal Q in Fig. 1, the gating of the delayed clock pulse with Q produces an interrupt pulse to the central processor that is of questionable shape. The response of the computer to this misshapen signal may yield a system failure since such signals can cause a state change fault in the central processor. Recently Chaney and Molnar [12] have provided additional experimental evidence of these failure modes.

Such failures are extremely serious when highly reliable systems having many interactions with external nonsynchronized equipment must be constructed. One of the authors (Couranz) is working on system designs contain-

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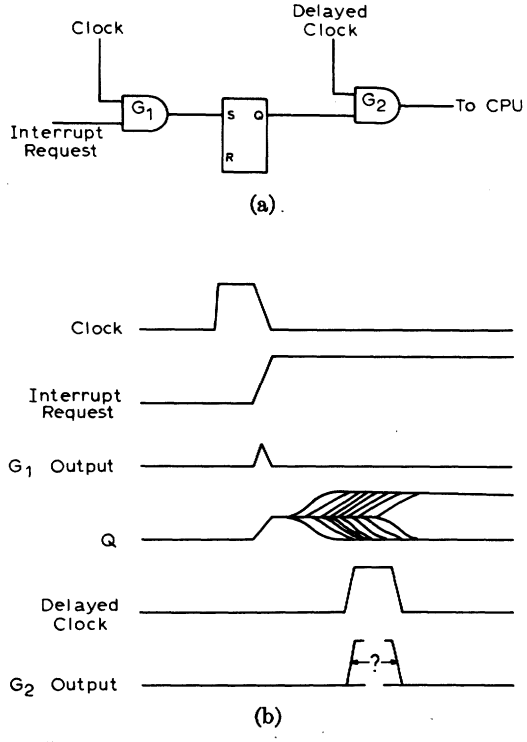

Fig. 1. Synchronizer circuit. (a) Logic diagram and (b) typical waveforms.

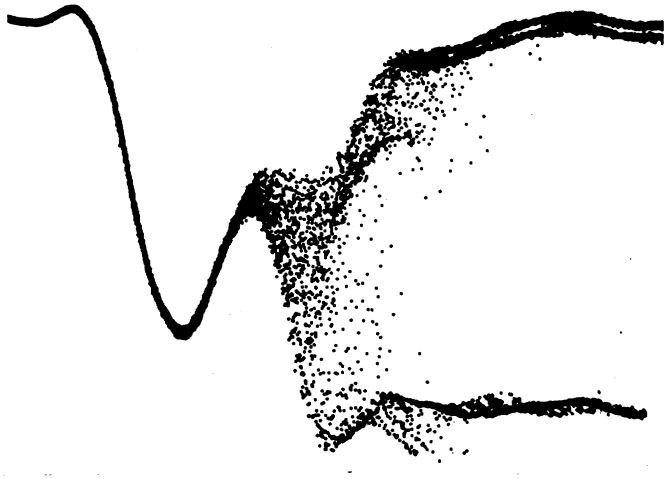

Fig. 2. Photographs from a sampling oscilloscope of flip-flop output voltage with triggering adjusted to cause entrance into the metastable region.

ing a two-port, 150-ns memory shared between two processors. There are about two access requests every 300 ns, thus in every second there are nearly 3.3×10^6 asynchronous interactions. This produces an hourly rate of over 10^{10}. The tendency of designers to ignore these interaction failure modes based on their small probability of occurance must be reexamined as such interaction rates increase. Furthermore, the emphasis on fail-safe design in both hardware and software, as typified in space operations and nuclear power plant monitoring, must include some analysis of these problems.

It should be emphasized, too, that these interaction difficulties are not limited to clocked systems. Completely asynchronous computers, as reported by Clark *et al.* [4] often involve similar problems. For example, consider the case where two processors need to access the same memory and an *interlock* is to be employed, Fig. 3. Assuming fundamental mode operation, let x_1 and x_2 be the signals that call on the common memory. The interlock mediates the requests, so that, upon receipt of x_1 or x_2, a single call, Z_3, is generated by the interlock and this activates the memory. If a second call is received during the period that the memory is active, it must be held for action when the memory is free. Upon completion of the memory access a control signal, x_3, is sent to the interlock, and in turn, a return, Z_1 or Z_2, is provided to the appropriate processor. The primitive flow table for this task is shown Table I.

There are two sequences of interest in the table, each dealing with the simultaneous arrival of x_1 and x_2. Let the initial condition consist of $x_1x_2x_3 = 000$ and let x_1 occur followed by x_2; the solid line traces the circuit operating point to the final state denoted by ⑧. Next let x_2 occur followed by x_1; then ⑨ is the final state. Inspection of the flow table shows that the inputs and outputs to the interlock are equal in both states ⑧ and ⑨, but ⑧ and ⑨ must be distinguishable. Therefore, an internal memory device is necessary to separate the two states. Since the two main sequences operate asynchronously, calls on the memory may occur in rapid succession. But there is some delay in circuit response to the calls and an internal variable may be changing during the period in which the second call is received. The analysis techniques developed by Huffman require that the inputs of the sequential circuit are controlled such that they never change unless the internal state has stabilized. Therefore, normal sequential circuit synthesis techniques cannot be employed for the design of this interlock. Recently, there have been a number of analytical treatments of this unrestricted input change problem [8]–[10]; however, careful examination reveals that every proposed solution requires some constraint on arrival times. It appears that such "knife edge" decision making may well be a fundamental circuit design problem that has been grossly neglected [11].

Examination of the synchronizer or interlock indicates that the success or failure of such a control element is dependent on the operation of a memory device, usually a flip-flop, to reach a completely stable state within a specified time interval. When the circuit operation is such that trigger pulses supplied to the flip-flop are of adequate amplitude and duration, the switching time can be accurately defined. In the case of the synchronizer, however, a possibility exists that the trigger pulse will be misshapen and cause random switching times. The problems of the interlock may be compared to that of the synchronizer if the existing internal state replaces the interrupt level. If two input signals are supplied to the interlock in rapid succession, the internal state may be in the process of changing when the second input, which is comparable to the clock, arrives. Again, a misshapen pulse may occur

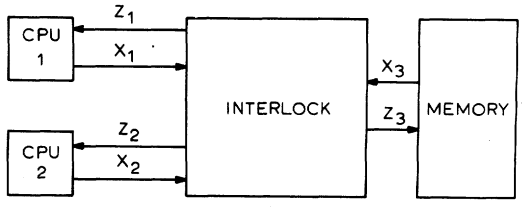

Fig. 3. Use of an interlock to mediate requests on common memory.

TABLE I
PRIMITIVE FLOW TABLE FOR INTERLOCK

$X_1X_2X_3$ 000	001	011	010	110	111	101	100	$Z_1Z_2Z_3$
(1)	–	–	5	8	–	–	2	000
–	–	–	–	8	20	3	(2)	001
–	4	12	–	–	20	(3)	–	101
1	(4)	12	5	–	–	–	–	100
–	–	6	(5)	9	11	–	–	001
–	7	(6)	–	–	11	14	–	011
1	(7)	–	–	–	–	13	2	010
–	–	–	–	(8)	20	–	–	001
–	–	17	16	10	(20)	–	–	100
18	–	–	16	(10)	–	–	15	110
–	–	–	–	10	(11)	14	15	010
–	–	(12)	5	–	–	–	–	100
–	–	–	–	–	–	(13)	2	010
–	–	–	–	–	–	(14)	15	010
19	4	–	–	–	–	3	(15)	111
18	7	6	(16)	–	–	–	–	111
–	–	(17)	16	–	–	–	–	100
(18)	7	–	–	–	–	–	–	111
(19)	4	–	–	–	–	–	–	111
–	–	–	–	(9)	11	–	–	001

in the circuitry which determines the internal state and the switching time may be irregular-causing errors in other circuits which use the internal state as a gating function.

A detailed analytic treatment of the binary flip-flop action in the metastable region is thus needed in order to 1) understand and predict in a mathematical manner the circuit performance and 2) aid the computer circuit designer in constructing devices for reliable communication between asynchronous systems. The work presented here develops a mathematical technique that can be used for determining the time spent in the metastable region and these computations are verified with data obtained from laboratory measurements. The principle result is to predict, in a probabilistic manner, the time necessary to move from the metastable point to one of the stable points. The effects of circuit time constants and circuit noise play an important role in these determinations and are discussed in some detail.

II. CIRCUIT MODEL

Since there are many flip-flop circuits in common use, it is necessary to select a model that can be easily applied to a variety of binary devices. Probably the most common

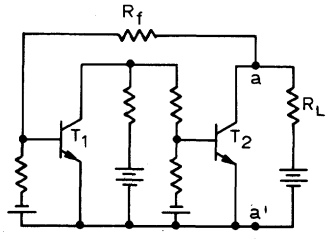

Fig. 4. Eccles–Jordan flip-flop showing feedback loop.

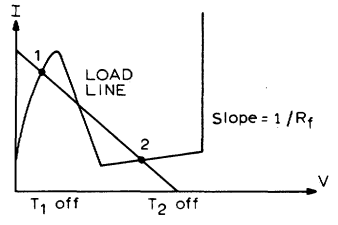

Fig. 5. Voltage–current characteristic of flip-flop measured at terminals a-a' of Fig. 4.

circuit is the Eccles–Jordan bistable, as indicated in Fig. 4. The two transistors provide amplification to produce a negative resistance in the closed loop system. The composite V-I profile [5] at terminals $a - a'$ is shown in Fig. 5 along with the load line defined by the circuit resistor R_L. If the effects of reactive elements, such as transistor junction capacitances, are included [6] the equivalent admittance at terminals $a - a'$ can be determined as

$$Y_{a-a'} = \frac{1 - K_1}{R_f} + j\frac{2K_2\omega}{R_f} \tag{1}$$

where ω is the radian frequency variable, K_1 and K_2 are positive constants, and R_f is the feedback resistor. It should be noted that for the case of interest, K_1 is greater than 1, and the effective resistance is therefore negative. Thus, during the time interval the operating point is in the negative resistance region, the binary can be represented to a first approximation as a parallel RC circuit, where

$$R_n = \frac{R_f}{1 - K_1} \qquad C = \frac{2K_2}{R_f}. \tag{2}$$

Since the circuit operation is linear in the region surrounding the intersection of the load line and the negative resistance section of the V-I characteristic, superposition may be applied to obtain the equivalent noise current source, I_n, at the output terminals. If the transfer function relating a specific noise source, I_k, to the output current is $H_k(j\omega)$, then by superposition [6]

$$S_{I_{noise}}(\omega) = \sum_{k=1}^{m} |H_k(j\omega)|^2 S_{I_k}(\omega) \tag{3}$$

where S is the transform operator and m is the number of noise sources of interest. The composite of all the noise sources in the circuit can then be represented by a *single* noise current source in parallel with an RC network.

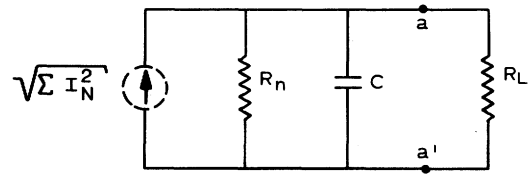

Fig. 6. Model for the Eccles–Jordan circuit around the metastable point including noise source.

This circuit, Fig. 6, is valid in the negative resistance region just surrounding the metastable point.

III. PROBABILITY OF ESCAPE FROM THE METASTABLE REGION

The probability of reaching one of the two totally stable states can now be determined. Reaching a stable state from the region just surrounding the metastable point depends on 1) the initial offset voltage and 2) the circuit noise. The degree to which noise affects the circuit response is dependent on the magnitude of the offset from the metastable point. The negative resistance region of most circuits have widths greater than 100 mV while circuit noise is normally in the tens of microvolts. Once the output voltage exceeds several millivolts, the time to reach a stable point will be largely independent of the effects of noise. The transition may, therefore, be assumed to be a two-part process as shown in Fig. 7. The first transition consists of the movement of the output voltage from its initial condition to an output level at which noise has an insignificant influence. These voltage levels are defined as the upper and lower boundary voltages, V_{UB} and V_{LB}, respectively. Since they are symmetric around the metastable point, they will be referred to as V_B. The actual value of the boundaries are functions of the circuit noise and in the following discussion will often be represented as $K\sigma(\Delta t)$ where K is a constant and $\sigma(\Delta t)$ is the standard deviation of the noise source voltage per unit time increment. The second part of the process is a movement to one of the stable points. Since this latter transition is deterministic, emphasis will be placed on evaluating the probability, $P(|v| \geq V_B \mid t)$, that the circuit opeating point has reached the boundary of the region in which noise has a significant effect. One of our colleagues, M. Hurtado, has recently proved that 1) regions of metastability do exist in this type of flip-flop circuit, 2) if a circuit is placed within such a metastable region, then in the absence of external signals or noise, the circuit will remain there indefinitely without exiting to a stable region (i.e., the "0" or "1" state), and 3) in the absence of any signal input then the only factor that may move the circuit from this metastable region is noise. These results will be published shortly [13] and underly the analysis presented here.

The ac equivalent circuit of the flip-flop model in the linearized negative resistance region is shown in Fig. 8. The load resistor, R_L, and the effective negative resistance, R_n, are combined into $-R$. Writing Kirchhoff's current difference equation for the circuit yields

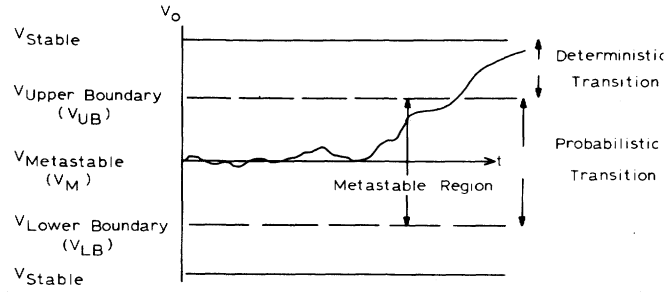

Fig. 7. Definition of the transition regions between the metastable state and the stable states.

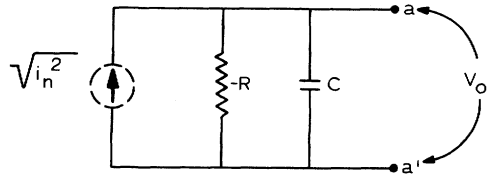

Fig. 8. Equivalent circuit for the noise model.

$$C\frac{V_{oi+1}-V_{oi}}{\Delta t}-\frac{V_{oi}}{R}\approx I_n \tag{4}$$

where I_n is a normally distributed random variable with zero mean, V_{oi} is the output voltage at time t_i, and V_{oi+1} is the output voltage at time $t_i + \Delta t$. Solving for V_{oi+1} gives

$$V_{oi+1}\approx \underbrace{\frac{V_{oi}(RC+\Delta t)}{RC}}_{\text{I}}+\underbrace{\frac{I_n\,\Delta t}{C}}_{\text{II}}. \tag{5}$$

The first term specifies the *deterministic* circuit response—sometimes referred to as drift. The second term is the *uncertainty* in the output voltage after Δt due to the effects of noise. Thus, the output voltage at $t_i + \Delta t$ is a function of the initial voltage at t_i and the amount of charge supplied to the capacitor during the interval Δt. Although (5) may be solved by simulating the random current and using numerical integration, this does not directly yield the probability distribution per unit voltage $p_{V_o}(V,t)$ between the boundary voltages. To compute this distribution directly requires a significant expenditure of computer time. For this reason an alternative technique, based on the fast Fourier transform, was developed.

A. Fourier Transform Solution

The probability density function of interest is $P_{V_{on}}(V)$ which is the composite of both $p_{Vo}(V)$, the distribution due to drift effects, and $p_{Vn}(V)$, the distribution due to noise effects.

Let the output voltage range be subdivided into N total increments, with a specific increment, j, being ΔV_j long. Then just after the trigger pulse disappears, the output voltage is known to be within the bounds of ΔV_j with a probability of 1. The probability of the occupancy of any other increment by the output voltage is zero. As a result, the probability density function of the output voltage is given by

$$p_{V_o}(\Delta V_k, t=0)\begin{cases}1.0/\text{V} & \text{for } k=j\\ 0 & \text{for } k\neq j.\end{cases} \tag{6}$$

First the deterministic effects will be considered, as specified by the first term of (5). After Δt seconds the output voltage will have changed but will still be found in ΔV_j. The size of the increment will, however, have increased, as denoted in Fig. 9(a). Assuming that the upper boundary of increment ΔV_j was at $V_j + \Delta V/2$ and the lower boundary at $V_j - \Delta V/2$ then

$$\Delta V(t+\Delta t)=(V_j+\Delta V/2)\exp(\Delta t/RC)-(V_j-\Delta V/2)\exp(\Delta t/RC) \tag{7}$$

which reduces to

$$\frac{\Delta V(t+\Delta t)}{V(t)}=\exp(\Delta t/RC). \tag{8}$$

Also the magnitude of the probability density function within ΔV_j must be multiplied by $\exp(-\Delta t/RC)$ to maintain a total probability of unity over the voltage increment. Since it is desirable to maintain a constant increment size during the entire computation, the expanded voltage range at $t + \Delta t$ must be scaled so that the basic $\Delta V(t)$ is reestablished for the next interval as shown in Fig. 9(b).

The second step is to superimpose the effects of noise on the output voltage. The circuit noise is known to be normally distributed with a zero mean and, from (5), this produces a deviation from the zero noise condition by a value proportional to the noise current during the interval multiplied by the interval length. For small Δt the noise current can be assumed constant and the probability density may be computed in discrete form along the quantized voltage axis. If the output voltage is known to be in the kth interval with a probability $p_{V_o}(\Delta V_k)\Delta V$ and the noise voltage is known to be within the jth interval with a probability of $p_{V_n}(\Delta V_j)\Delta V$ (Fig. 10), then the probability density function of the voltage sum is

$$p_{V_{on}}(\Delta V)=\sum_{j=-\infty}^{\infty}p_{V_o}(\Delta V-V_j)p_{V_n}(\Delta V_j) \tag{9}$$

where

$$V=V_k+V_j.$$

For the general case, the probability of finding the output voltage in a specified V is found as indicated in Fig. 11. Let $p_{V_o}(V_1)dV_1$ be the probability that the value of V_o lies in the interval dV_1 at V_1 and let $p_{V_n}(V_2)dV_2$ be the probability that V_n, the noise voltage component, lies in dV_2 at V_2. Since V_1 and V_2 are independent, the output voltage probability density function, $p_{V_{on}}(V,V_1)$, which includes noise, is given by

$$p_{V_{on}}(V,V_1)=p_{V_o}(V_1)p_{V_n}(V-V_1)dV_1. \tag{10}$$

Then integrating over all V yields the desired probability

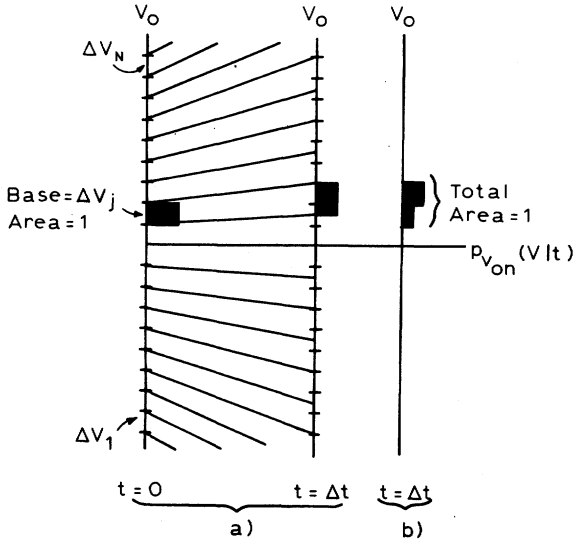

Fig. 9. Subdivision of the output voltage range illustrating (a) the distribution drift and (b) the grid correction.

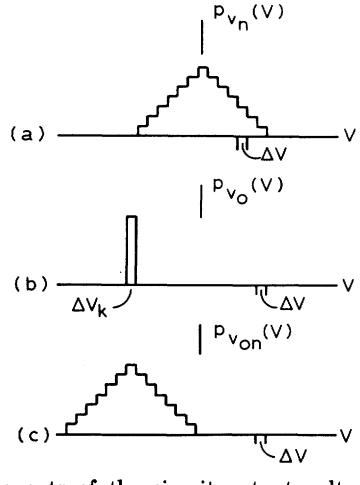

Fig. 10. Components of the circuit output voltage distribution. (a) Noise voltage distribution. (b) Deterministic (or drift) voltage distribution. (c) Composite distribution.

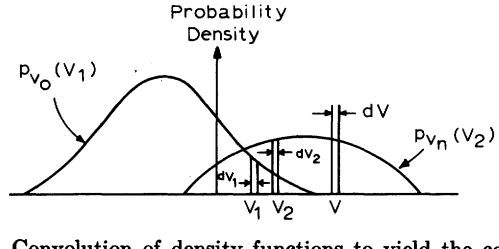

Fig. 11. Convolution of density functions to yield the composite distribution.

density function

$$p_{V_{on}}(V) = \int_{-\infty}^{\infty} p_{V_o}(V_1)p_{V_n}(V - V_1)dv_1. \quad (11)$$

In order to guarantee computational accuracy, many small voltage sections are necessary and this requires prohibitive computation time if the integral is replaced by a sum. Fortunately, (11) represents a convolution operation and may be economically evaluated by the application of Fourier transform techniques. Defining F as the Fourier operation, (11) can be expressed as

$$p_{V_{on}}(V) = F^{-1}\{F[p_{V_o}(V)]F[p_{V_n}(V)]\}. \quad (12)$$

Since $p_{V_o}(V)$ is known at $t = 0$ and $p_{V_n}(V)$ can be computed from circuit characteristics, it is only necessary to obtain their Fourier transforms, multiply the transform arrays, and take the inverse transform to obtain the output voltage distribution which includes the effects of noise during the interval Δt. The drift and noise effects must now be combined to determine the output voltage probability density distribution as a function of time. Starting with the initial condition of the circuit just after triggering, the drift is computed to obtain the circuit output voltage at $t = \Delta t$. The circuit noise component is then superimposed, and this yields the probability distribution of the output voltage after time Δt. This process is repeated to obtain the distribution at $t = N\Delta t$.

Assuming that the output voltage density function at time t, $p_{V_{on}}(V/T)$, has been evaluated, the probability of exceeding one of the boundary regions can be obtained by summing the probabilities indicated by the sectors outside the boundary. This sum is the probability of escape per unit time, $p_E(t)$. The distribution $p_{V_{on}}(V/t)$ is restricted in that once the operating point, as indicated by the output voltage, exceeds a boundary, it cannot reenter the metastable area. To satisfy this constraint, $p_{V_{on}}(V \mid t)$ is set to zero in the region exceeding either boundary voltage. Then, as the distribution expands due to drift and circuit noise during each time interval, the integral of $p_{V_{on}}(V \mid t)$ over the metastable region is the probability that the operating point has never crossed a boundary. Although the distribution expands across the boundary during each time interval, the probability of not escaping decreases with time but never reaches zero until $t = \infty$. The numerical solution of (12) was performed using circuit values (RC time constants and noise standard deviations) that were indicative of the parameters encountered in the experimental phases of the work to be described later. These parameters are summarized in Table II.

B. Voltage Distributions for Zero Offset Conditions

Using the procedure described above, and the data from Table II, a series of computations were performed. Fig. 12(a) shows the computed voltage probability distribution for circuit configuration 1 with an initial offset voltage of zero. This yields a drift over the first Δt of zero. The distribution due to circuit noise is shown superimposed on the output voltage after 1 ns. For times of 5, 10, and 15 ns, drift also produces spreading.

The situation in which the boundaries were set at $20\sigma(\Delta t)$ was evaluated and the probability density function of escape, $p_E(t)$, is shown in Fig. 12(b).

To further evaluate the effects of noise in the circuit operation, $p_E(t)$ was computed for RC values of 11, 22, and 44 ns with zero offset initial conditions. First, the value of the circuit noise voltage distribution was varied

TABLE II
CIRCUIT PARAMETERS USED IN THEORETICAL AND EXPERIMENTAL COMPUTATIONS

CIRCUIT	TIME CONSTANT (NANOSECONDS)	NOISE VOLTAGE STANDARD DEVIATION, $\sigma(\Delta t)$ (MICROVOLTS)	COMPONENT
1	44	1.2	TD710
2	44	0.7	TD712
3	22	1.4	TD712

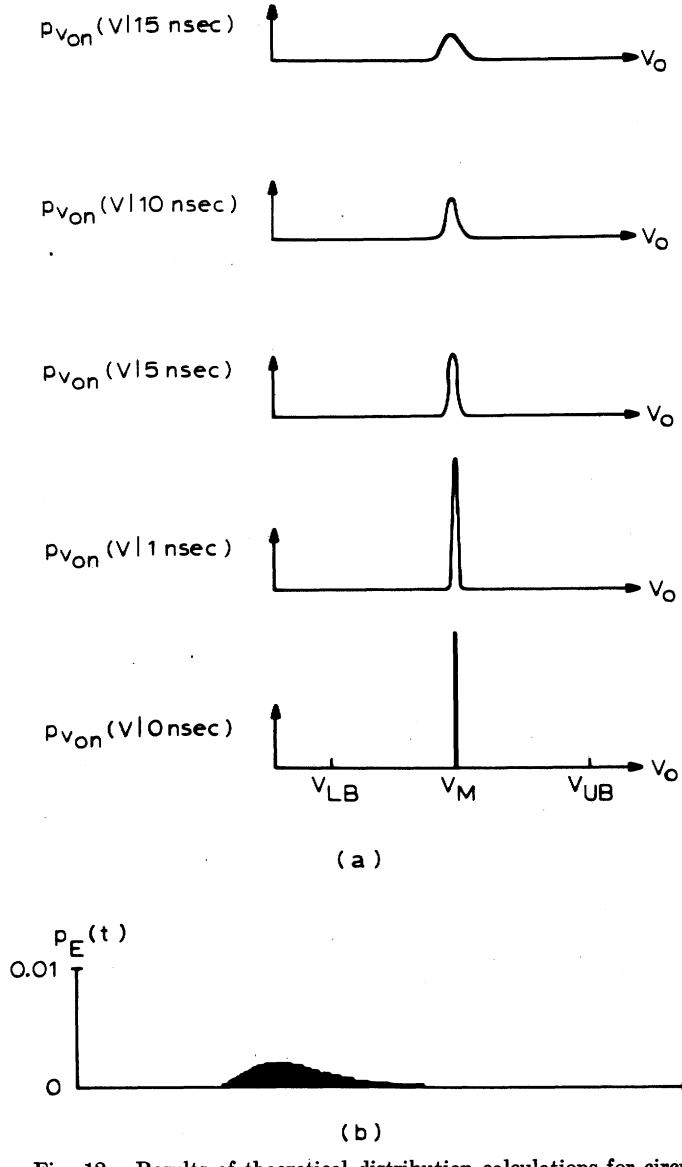

Fig. 12. Results of theoretical distribution calculations for circuit with RC = 44 ns, zero offset and $\sigma(\Delta t)$ = 1.2 μV, and boundaries at 20 $\sigma(\Delta t)$. (a) $p_{V_{on}}(V \mid t)$. (b) $p_E(t)$.

such that, for the three time constants, the noise voltage standard deviations would be multiples (1, 2, and 4) of the values indicated in Table II. In addition, the position of the boundary, V_B, for each evaluation was adjusted such that $V_B/\sigma(\Delta t)$ was a constant. The results for the case of a 44-ns time constant are shown in Fig. 13(a) from which it is clear that $p_E(t)$ is not altered by the different noise levels. The result of holding V_B constant and varying $\sigma(\Delta t)$, again with a 44-ns time constant, is shown in Fig. 13(b), which demonstrates that for a zero offset initial condition, the time for the mean of $p_E(t)$ to reach the boundary is a function of the ratio $V_B/\sigma(\Delta t)$. This mean of $p_E(t)$ is the *mean first passage time* and its variation with time constant and $V_B/\sigma(\Delta t)$ ratio is de-

picted in Fig. 14. Observe that the time at which the mean occurs is a function of both of these variables.

Since there is no change in $p_E(t)$ if $V_B/\sigma(\Delta t)$ is maintained constant, it is possible to evaluate the probability density of escape for other values of V_B and $\sigma(\Delta t)$. If a reference value of $p_E(t)$ is computed with $V_B/\sigma(\Delta t)$ chosen such that once the circuit output voltage reaches the boundary the response is essentially deterministic, $p_E(t)$ can be time scaled for any desired value of $V_B/\sigma(\Delta t)$.

C. Voltage Distributions Under Conditions of Initial Offset

The modification with time of the output voltage probability density function when the initial offset voltage is varied is depicted in Fig. 15. Fig. 15 consists of a time sequence of the distribution for a circuit with a time constant of 11 ns and an initial offset of $0.25V_B$. As the distribution spreads out along the base line, the mean moves toward the positive boundary. Upon reaching the boundary at 14 ns, that portion of the distribution that has exceeded the boundary is no longer of interest. Finally, at 20 ns, only an extremely small probability remains that the output voltage is less than the boundary voltage.

An attempt was made to describe the response as a function of noise level and time constant, but a satisfactory correlation of these variables and the data could not be obtained. This is due largely to the size of the voltage increments, ΔV, which limit the accuracy of the calculations. To obtain such a correlation, the number of increments should be expanded to allow for smaller values of ΔV without greatly restricting the overall voltage range of the computations.

D. Response to a Uniform Distribution of Initial Condition Voltages

If it is assumed that the circuit output voltage just after triggering is uniformly distributed between the two boundary voltages, the probability of exceeding the metastable region as a function of time, for the case of no circuit noise, can be computed. Since the process is completely deterministic, the probability that the boundary voltage has been exceeded is merely

$$p_{V_B}(t) = 1 - \exp(-t/RC). \tag{13}$$

This means that the probability density function is given by

$$p_{V_B}(t) = RC \exp(-t/RC). \tag{14}$$

Evaluating $p_E(t)$ for two time constants, circuit noise nonzero, and uniform initial distribution, yields the data illustrated in Fig. 16. These results are identical to those derived for the case where circuit noise was zero. This may at first seem to conflict with the data presented in Fig. 17. But consider an ensemble of flip-flops whose output states are uniformly distributed across the metastable region. During the transition to a stable state (0 − 1), the output voltage changes exponentially while it is in the linear negative resistance region. For each noise contribution which moves a given flip-flop from one exponential trajectory that is closer to (farther away from) a stable point, there will be, on the average, a compensating noise signal which tends to move the output of another flip-flop further away (closer to) the intersection of the load line and the negative resistance line. Since the initial distribution was uniform, the noise effect will, on the average, not change the result.

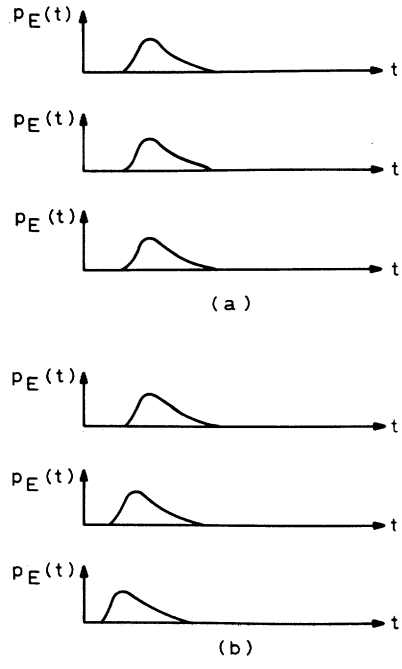

Fig. 13. Variation of $p_E(t)$ as a function of V_B and $\sigma(\Delta t)$. (a) Values of $\sigma(\Delta t)$ equal to 1.2 μV, 2.4 μV, and 4.8 μV, for the upper, middle, and lower plots, respectively. (b) Plots for $V_B/\sigma(\Delta t)$ equal to 80, 40, and 20 for the upper, middle, and lower plots, respectively. Time constant for both parts is 44 ns.

In conclusion, then, for the cases discussed here, the probability density function of escape is

$$p_E(t) = \frac{1}{RC} \exp(-t/RC) \tag{15}$$

while the probability of escape from the metastable region then becomes

$$p_E(t) = 1 - \exp(-t/RC). \tag{16}$$

IV. EXPERIMENTAL EVALUATION OF THE PROBABILITY OF ESCAPE

Verification of these theoretical results using laboratory experiments is very desirable. In order to more accurately control circuit parameters, a tunnel diode was employed as the negative resistance device in a simple bistable design. The use of a more complex circuit would not have added to the analysis since any such circuit may be reduced to one equivalent to the tunnel diode design in the region of interest (5). This test circuit is depicted in Fig. 18 and the corresponding *V-I* characteristic is illustrated in Fig. 18 (b). The tunnel diode has a model very close to that of the first order approximation of the two transistor flip-flop circuit previously discussed, see Fig. 6. The tunnel

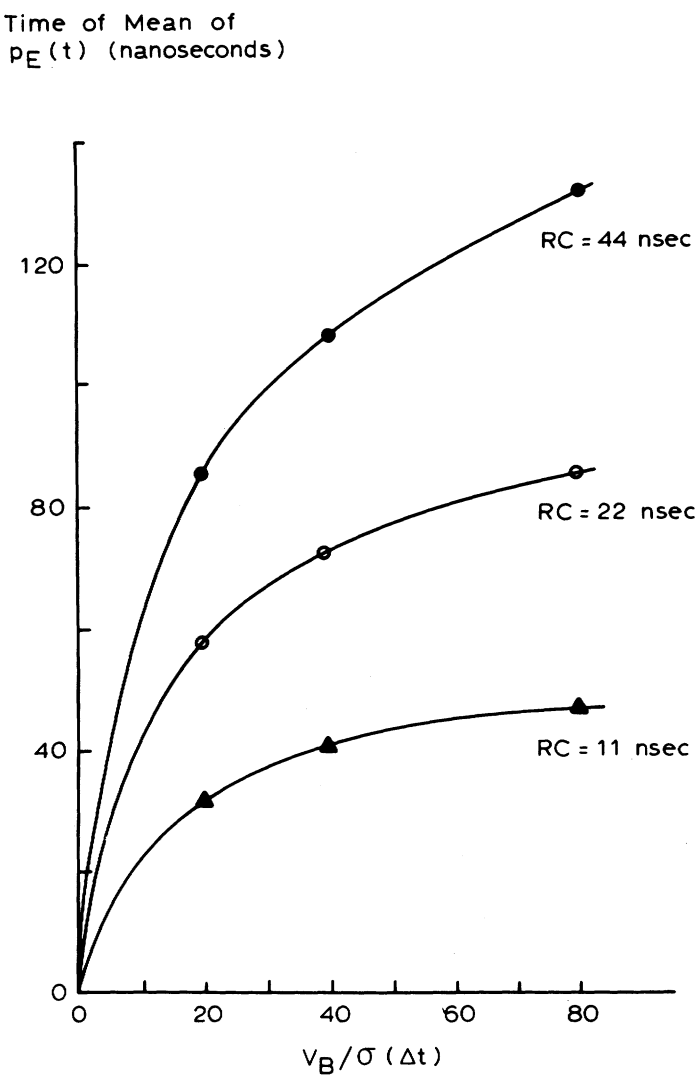

Fig. 14. Mean first passage time as a function of $V_B/\sigma(\Delta t)$.

diodes used in the experiment were the TD710 and the TD712 which had peak currents of 0.5 mA and 1 mA and junction capacitances of 5 and 10 pF, respectively. The sum of the diode junction and stray capacitance is indicated by C_T in Fig. 18. A swamping capacitor, C_S, was added to the circuit for two reasons. First, the junction capacitances are on the order of stray circuit capacitance and these would be variable throughout the experiment. As a result, the time constant, RC, would be uncertain. Secondly, the switching time for the circuit is in the nanosecond range. For trigger voltages that would produce a total supply current in the order of the peak current, the switching time for the given devices would be approximately 4 ns. The sample gate width for the sampling oscilloscope utilized for voltage measurements was 0.35 ns and the jitter on the oscilloscope sampling gate was on the order of 0.1 ns. This would make the sampling time of the measuring system questionable with respect to the short switching time of the tunnel diode circuit. Thus, the addition of the swamping capacitor to slow the circuit response yielded a stable value for RC (where $C = C_T + C_S$) and

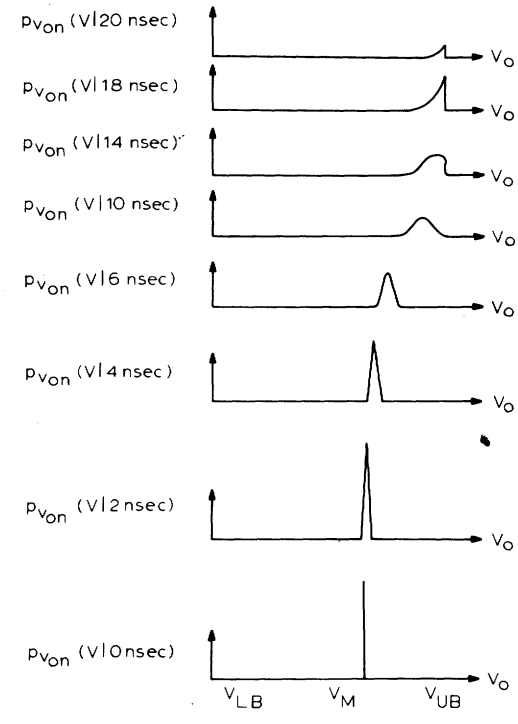

Fig. 15. Variation of pv_{on} with time for a time constant of 11 ns and a 10 μV initial offset.

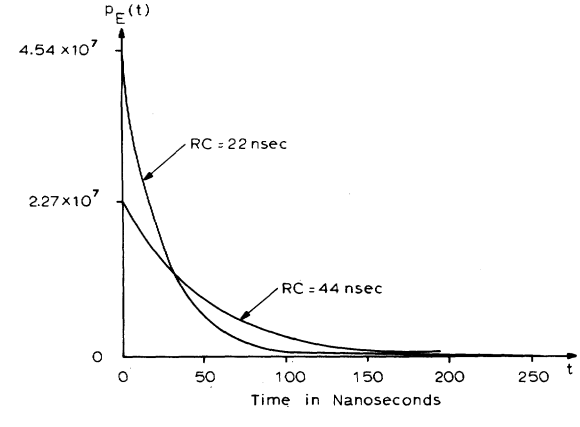

Fig. 16. Computed value of $p_E(t)$ for time constants of 22 and 44 ns and a uniform initial condition distribution. Metastable region is ± 38.4 μV.

decreased the measurement error due to jitter. Finally, since the negative resistance region for tunnel diodes is linear in a 50-mV wide region, the test boundaries were set at ± 25 mV surrounding the metastable point which, in turn, was at the center of this linear region.

A. *Instrumentation*

The instrumentation used to obtain the probability density function of escape was largely dictated by the uncertainty of voltages in the circuit. Because of circuit noise, the initial condition voltage cannot be specified exactly. Thus, it was necessary to generate a known distribution of initial offset voltages and then determine the circuit response. Due to the ease of implementation, a uniform distribution of initial condition voltages was used.

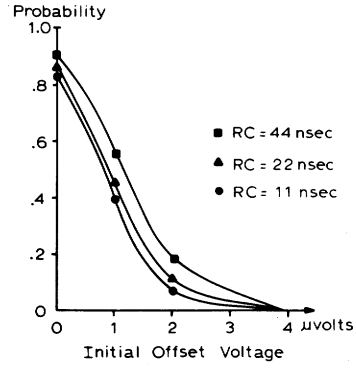

Fig. 17. Probability of output voltage, V_o, crossing V_m as a function of initial offset voltage.

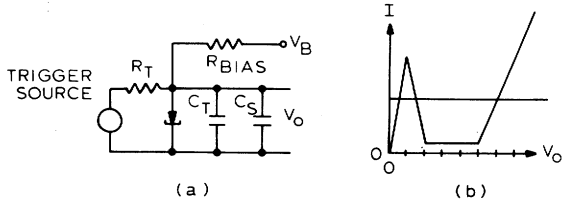

Fig. 18. Basic tunnel diode flip-flop and linearized V-I characteristic.

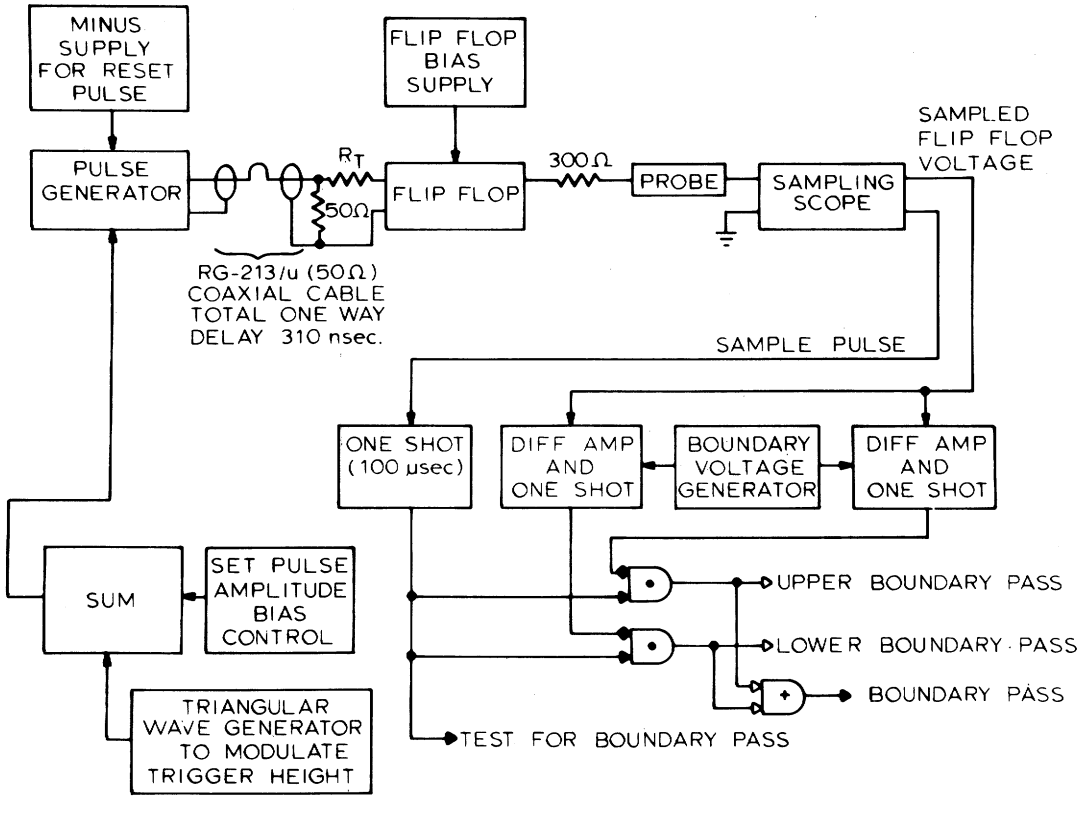

Fig. 19. Block diagram of instrumentation used in experimental tests.

This distribution was produced by amplitude modulating the trigger pulse with a triangular waveform.

Detection of a boundary crossing was accomplished by comparing the flip-flop output voltage for each sample with a reference level, at specified time intervals after triggering, Fig. 19. The sample voltage (obtained from a sample and hold circuit in the oscilloscope) and the reference level were applied to the alternate inputs of a high gain differential amplifier. If the sample voltage exceeded the threshold level, the amplifier output switched and the resulting signal was used as the assertion level to an AND gate. Each time a sample was taken this assertion

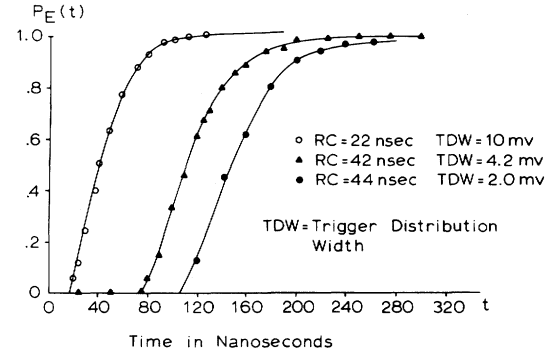

Fig. 20. Experimental results for the probability of escape for several tunnel diode flip-flop circuits.

level was tested by generating appropriate pulses based on the "sample taken" pulse from the oscilloscope. The "sample taken" pulse was also used to trigger a 100 μs one-shot whose output was gated with the signal from the upper and lower boundary level voltage comparators. The results of the boundary checks were then ORed together. A ratio of the number of successful tests of boundary passage to the total number of circuit triggers, with the sample being taken at a specified time after the end of the trigger pulse, yields the probability of boundary passage at that point in time. A counter performs the ratio computation.

After establishing the uniform distribution of initial conditions, $p_E(t)$ was evaluated by measuring the circuit output voltage at specified time intervals after the completion of the trigger pulse. These measurements, taken with a sampling oscilloscope, were compared with the ± 25 mV boundary lines. The ratio of the number of samples found to be outside the bounded region to the total number of samples taken at each time period is the probability of escape, $p_E(t)$.

B. The Escape Probability Density of Three-Flip-Flops

Circuits with the characteristics listed in Table II were constructed and the probability of escape from a ± 25 mV band surrounding the metastable point was experimentally determined. Fig. 20 indicates the probability of escape for each circuit as a function of time. Each data point is the result of 100 000 samples of the output voltage. The results agree quite well with the theoretical computations. The distribution was restricted to a range much less than the ± 25 mV boundary voltages and this caused the delay in exceeding the threshold. Although it is desirable to minimize the width of the distribution so that the number of points close to V_M are large, this condition must be balanced against the drift in the position of the distribution due to changes during the sampling period in 1) the bus and trigger sources and 2) the modulator. The width of the resultant distribution can readily be determined from the data, since, for the purposes of this calculation, the results are deterministic. The width of the trigger distribution for each of the tested diodes is also indicated by the breakpoints in Fig. 20.

The major limitation of this testing scheme is the problem of generating a large number of samples in the critical voltage range. For a time constant of 44 ns and the associated noise level, noise appears to have a relatively large bearing on the escape time for voltages out to about 3 μV. From a total sample population of 100 000 the number of samples that can be expected inside the 3 μV region for each run is about 36 while in a 38.4 μV region about 914 samples would be expected. Therefore, without raising the total samples per point by several orders of magnitude, it is difficult to say that the data taken from the test circuit matches the results throughout the *entire* test range. Increasing the number of samples is somewhat difficult since the measurement time for 100 000 samples, not including distribution positioning, is approximately 5 min.

V. CONCLUSIONS

Synchronizers, interlocks, and other similar elements which are employed to control the interaction of asynchronous signals normally use flip-flops to resolve state change uncertainties. These flip-flops are basically negative resistance devices and may be approximated by a parallel combination of a resistor and a capacitor. When this equivalent circuit is used, along with the appropriate noise voltage sources, it is possible to derive $p_E(t)$, the probability density of escape from the metastable point. Fourier transform techniques can then be applied to evaluate the effects of noise on the circuit output voltage. In this method, the metastable region is subdivided into voltage increments, ΔV. The voltage range for each increment has an upper bound which must be chosen such that the noise voltage density distribution can be accurately represented. As shown by Figs. 13–17, the region in which noise has a significant effect is limited to offset voltages much less than the imposed boundaries. Based on this data, the noise effect region can be reduced by decreasing the circuit time constant.

For an initial condition offset voltage of zero the mean time of escape from the metastable region by the output voltage is a function of the ratio of boundary voltage, V_B to the circuit noise level as indicated by $\sigma(\Delta t)$, the standard deviation of the noise voltage developed per unit time

interval. If this ratio is large, the shape of $p_E(t)$ is, to a first-order approximation, only a function of the time constant, RC. Thus, only the position of $p_E(t)$ in time is changed by varying the ratio.

As the initial offset voltage is increased from zero, the time of occurrence of the mean of $p_E(t)$ approaches that of the deterministic transition of the offset voltage to the boundary in the case where circuit noise is zero. For offsets greater than $10\sigma(\Delta t)$, the time of occurrence of the mean is essentially the same as the deterministic offset voltage transition time.

For the special case of a uniform distribution of circuit initial offset voltage, the probability of the output voltage being found outside the metastable region is given by the simple relation

$$p_E(t) = 1 - \exp(-t/RC). \tag{17}$$

This probability is the same as that obtained if the circuit response is evaluated assuming a noise-free operation.

The laboratory test data obtained from tunnel diode flip-flops, as shown in Fig. 20, compare favorably with the integral of the data obtained from the computer solution of the circuit output voltage probability density function as shown in Fig. 17. This indicates that the mathematical model closely approximates the physical circuit response. It should be recalled, however, that the number of data points obtained from circuit voltages within ± 100 μV of the metastable voltage just after triggering is limited. Since the accuracy of measurement is dependent on the sample size, it is not possible to completely substantiate the calculated data from the laboratory tests in this low offset region.

Also, the advantage of the Fourier transform method in the calculation of the output voltage probability density function, $p_{V_{out}}(V)$ after each step in time should not be overlooked. The application of this technique to other random process problems, such as switching jitter or oscillator starting, appears reasonable.

Application of Results

This analysis can be directly applied to the design of synchronizers and interlocks. For example, suppose it is desired to sample the binary state of an external line in a clocked system and a basic synchronizer circuit, such as the one shown in Fig. 1, is to be designed for this purpose. Assume that the circuit components are known and an acceptable probability of error (APE) selected. Then the appropriate delay time, t_d, that should be used between the excitation of the flip-flop and the sampling of its output can be obtained. If the intial condition distribution is uniform, the time t_{APE}, to reach an acceptable error probability at the boundary voltage is given as

$$t_{APE} = \frac{-\ln(APE)}{RC} \tag{18}$$

where APE is

$$APE = 1 - P_E(t). \tag{19}$$

The total delay time, t_d, is then merely t_{APE} plus the deterministic response time, t_r, of the circuit. This latter time is the time necessary to move from one of the established boundary voltages to its associated stable state. Thus, $t_d = t_{APE} + t_r$.

If the initial condition distribution is unknown, it may be necessary to use one of the numerical methods to determine $p_E(t)$ for the case of an exact metastable point initial condition for each trigger. The results of this worst case analysis will yield t_{APE}.

This "trigger and wait" approach has been employed in various computer synchronizers and typically uses components from the same family as the rest of the machine. As a consequence, valuable computer cycles are lost in obtaining an acceptable probability of error. A better solution, for most practical applications, would be the selection of a device having an RC time constant an order of magnitude lower than the logic family of the central processing unit. One obvious candidate would be the tunnel diode.

An alternate method, suggested by Chaney and Littlefield [7] employs differential amplifiers to determine the stability of the flip-flop response. Their technique assumes that once the output voltage has passed through a threshold voltage toward a stable state, it will continue on to a stable state with unit probability. The data obtained here on the probability of the output reaching the metastable voltage as a function of initial offset indicate that for any set of defined boundaries there is a nonzero probability that the output voltage may *reenter* the metastable region. Again, however, if the circuit noise characteristics and time constant are known, the numerical techniques presented here can be employed to set the threshold levels of the state sensor circuit for an acceptable error.

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On the Quantitative Evaluation of Edge Detection Schemes and Their Comparison with Human Performance

JERRY R. FRAM AND EDWARD S. DEUTSCH, MEMBER, IEEE

***Abstract*—A technique for the quantitative evaluation of edge detection schemes is presented. It is used to assess the performance of three such schemes using a specially-generated set of images containing noise. The ability of human subjects to distinguish the edges in the presence of noise is also measured and compared with that of the edge detection schemes. The edge detection schemes are used on a high-resolution satellite photograph with varying degrees of noise added in order to relate the quantitative comparison to real-life imagery.**

***Index Terms*—Edge detection schemes, image processing, quantitative evaluation.**

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I. INTRODUCTION

ONE of the fundamental problems in the area of image processing is the location of boundaries of objects within an image. While a considerable number of edge detection schemes have been devised towards this end no comprehensive attempt has been made to compare the various schemes available. Such a comparison is necessary in order to establish the performance limitations of each scheme under the various conditions encountered. While the work reported here is only a first step in this important direction, it forms a groundwork for the long needed overall evaluation.

Characteristics of edge detection schemes, which should be investigated for comparative purposes include the following; edge orientation biases, edge detection in the presence of noise, range in scale of edge detectability,