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# Latch (electronics)

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In electronics, a **latch** is a kind of **bistable multivibrator**, an electronic circuit which has two stable states and thereby can store one bit of information. Today the word is mainly used for simple *transparent* storage elements, while slightly more advanced *non-transparent* (or *clocked*) devices are described as **flip-flops**. Informally, as this distinction is quite new, the two words are sometimes used interchangeably.

A circuit incorporating latches has state; its output may depend not only on its current input, but also on its previous inputs. Such a circuit is described as sequential logic.

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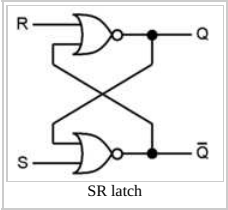
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## Simple set-reset latches

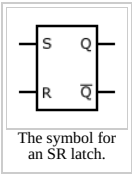
### SR latch

When using static gates as building blocks, the most fundamental latch is the simple *SR latch* (or simple *SR flip-flop*), where S and R stand for *set* and *reset*. It can be constructed from a pair of cross-coupled NOR (negative OR) logic gates. The stored bit is present on the output marked Q.

Normally, in storage mode, the S and R inputs are both low, and feedback maintains the Q and Q̄ outputs in a constant state, with Q̄ the complement of Q. If S (*Set*) is pulsed high while R is held low, then the Q output is forced high, and stays high when S returns low; similarly, if R (*Reset*) is pulsed high while S is held low, then the Q output is forced low, and stays low when R returns low.



SR latch operation		
S	R	Action
0	0	Keep state
0	1	Q = 0
1	0	Q = 1
1	1	Restricted combination



The symbol for an SR latch.

The R = S = 1 combination is called a **restricted combination** because, as both NOR gates then output zeros, it breaks the logical equation 



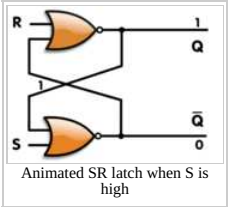
Q
=
¬
Q
¯


{\displaystyle Q=\not Q\,\!}

. The combination is also inappropriate in circuits where *both* inputs may go low *simultaneously* (i.e. a transition from *restricted* to *keep*). The output would lock at either 1 or 0 depending on the propagation time relations between the gates (a race condition). In certain implementations, it could also lead to longer ringings (damped oscillations) before the output settles, and thereby result in undetermined values (errors) in high-frequency digital circuits. This condition is therefore sometimes avoided.

To overcome the restricted combination, one can add gates to the inputs that would convert (S,R) = (1,1) to one of non-restricted combinations. That can be:

- Q = 1 (1,0) — referred to as an *S-latch*
- Q = 0 (0,1) — referred to as an *R-latch*
- Keep state (0,0) — referred to as an *E-latch*

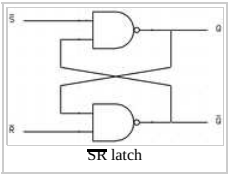


Animated SR latch when S is high

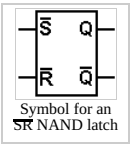
Characteristic: Q+ = R'Q + R'S or Q+ = R'Q + S see [1] ([http://books.google.com/books?id=4sX9fTGRo7QC&pg=PA344&lpg=PA344&dq=sr+characteristic+latch+equation&source=web&ots=9WdHN5uzTF&sig=ewGWuNX8g\\_4KozJuL5VyASz](http://books.google.com/books?id=4sX9fTGRo7QC&pg=PA344&lpg=PA344&dq=sr+characteristic+latch+equation&source=web&ots=9WdHN5uzTF&sig=ewGWuNX8g_4KozJuL5VyASz))

### SR NAND latch

This is a variety of the simple SR latch built with NAND (negative AND) logic gates. *Set* and *reset* now become active low signals, denoted 
S
¯
 and 
R
¯
 respectively. Otherwise, operation is identical to that of the SR latch. Historically, **SR**-latches have been predominant despite the notational inconvenience of active-low inputs. This is because NAND gates are cheaper to produce than NOR gates in the diode-transistor logic (DTL) and transistor-transistor logic (TTL) families, which were the basis of early integrated circuits before the complementary metal–oxide semiconductor (CMOS) family attained wide-spread use. Since the 1970's and still as of 2007, most integrated circuits are built using CMOS technology, where NAND gates are also preferred.



SR latch operation		
<span> S ¯<!-- ¯ --> </span>	<span> R ¯<!-- ¯ --> </span>	Action
0	0	Restricted combination
0	1	Q = 1
1	0	Q = 0
1	1	Keep state



Symbol for an SR NAND latch

### Gated latches

## Gated SR latch

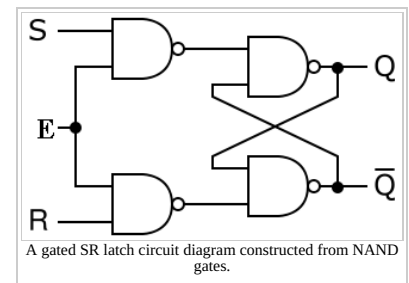
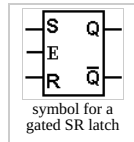
A *Synchronous SR latch* (sometimes *clocked SR flip-flop*) can be made by adding a second level of NAND gates to the inverted SR latch (or a second level of NOR gates to the direct SR latch). The extra gates further invert the inputs so the simple **SR** latch becomes a gated SR latch (and a simple SR latch would transform into a gated **SR** latch with inverted enable).

With **E** high (*enable* true), the signals can pass through the input gates to the encapsulated latch; all signal combinations except for (0,0) = *hold* then immediately reproduce on the ( $Q, \bar{Q}$ ) output, i.e. the latch is *transparent*.\*

With **E** low (*enable* false) the latch is *closed* and remains in the state it was left the last time **E** was high.

The *enable* input is sometimes a clock signal, but more often a read or write strobe.

Gated SR latch operation	
E	Action
0	No action (keep state)
1	The same as non-clocked SR latch



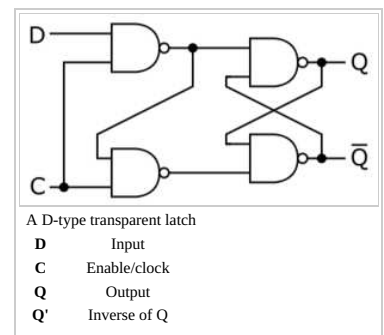
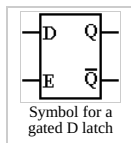
\* Note that, with several transparent latches following each other, the signal would propagate through all of them.

## Gated D-latch

This latch is closely related to the gated SR latch and can be similarly constructed. It is also known as *transparent latch*, *data latch*, or simply *gated latch*. It has a *data* input and an *enable* signal (sometimes named *clock*, or *control*). The word *transparent* comes from the fact that, when the enable input is on, the signal would propagate directly through the circuit, from the input D to the output Q.

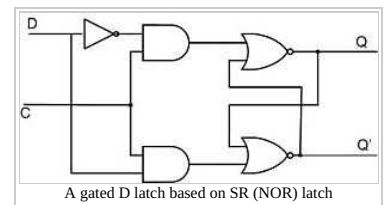
Transparent latches are typically used as I/O ports or in asynchronous systems.\* They are available as integrated circuits, usually with multiple latches per circuit. For example, 74HC75 is a quadruple transparent latch in the ubiquitous 7400 series.

D-latch truth table			
E/C	D	Q <sub>next</sub>	Comment
0	X	Q <sub>prev</sub>	No change
1	0	0	Reset
1	1	1	Set



The truth table shows that when the enable/clock input is 0, the D input has no effect on the output. When E/C is high, the output equals D.

\* Transparent latches are also sometimes used in synchronous two-phase systems (for reduced transistor count); however, in single-phase synchronous systems with direct feedback, master-slave devices (often edge-triggered) must be used to avoid analog oscillations.



## Gated Toggle latch

This is another synchronous SR latch that toggles the previous output. If the toggle (T) input is high, the T latch (well known as T flip-flop) changes state ("toggles") whenever the clock input is strobed. If the T input is low, it holds the previous value. Characteristic equation is;  $Q_{next} = T \oplus Q_{pre}$ , where  $Q_{next}$  is the next state and  $Q_{pre}$  is the previous state.

T	Q <sub>prev</sub>	Q <sub>next</sub>	Comment
0	0	0	Hold state
0	1	1	Hold state
1	0	1	Toggle state
1	1	0	Toggle state

A T flip-flop can also be built using a JK flip-flop (J & K pins are connected together and act as T) or D flip-flop (T input and  $Q_{previous}$  is connected to the D input through a XOR gate).

## JK latch

The **JK latch** follows the following state table:

JK Flip-Flop truth table			
J	K	Q <sub>next</sub>	Comment
0	0	Q <sub>prev</sub>	No change
0	1	0	Reset
1	0	1	Set
1	1	$\bar{Q}_{prev}$	Toggle

□

## See also

- Flip-flop
- Logic gate

## References

- Hwang, Enoch (2006). *Digital Logic and Microprocessor Design with VHDL*. Thomson. ISBN 0-534-46593-5.
- Fundamentals of Digital Logic by Brown and Vranesic
- S.P.Vingron: 'Switching Theory. Insight through Predicate Logic.' Springer Verlag, 2003. ISBN 3-540-40343-4 — extensively covers the theory of latches
- Parallel Port Output expanding with Latches (<http://www.globu.net/pp/english/pp/>)

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