EMB1 fall 2018
Final project
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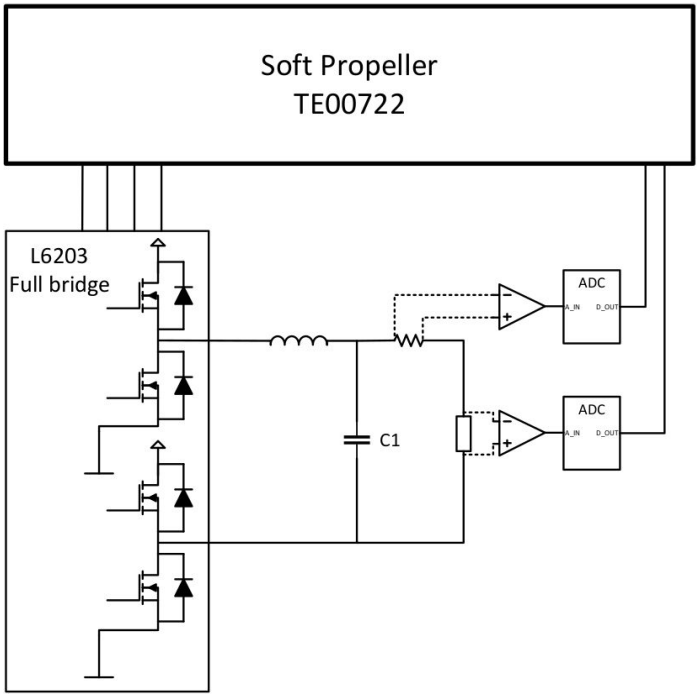
Final project

Materials

- Full bridge L6203 or other integrated bridge
- Load: Power resistor and/or electromagnet ..e.g. RS part no. SD0837
- Trenz TE0722 "Soft Propeller" with Xilinx Zynq-7010
- Trenz TE0790 XMOD FTDI JTAG Adapter
- ADC Ads7885
- Differential amplifier
- Inductor 50µH
- Capacitor
- Capacitors for decoupling, wires, Stripboard (rs: 433-832).

Project description



The control loop should be able to control current and voltage

- Adjustable constant level.
- Triangular waveform (option).
- Square waveform (option).
- Sinus waveform.

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Using a differential amplifier and ADC, the FPGA can sample the voltage across the load: V(t), and the current through the load: I(t). Using feedback, e.g. a P, PI- or PID-regulator, the system can regulate the PWM to produce a specific load-voltage and/or -current.

Rather than creating a constant voltage or current, the system should work as a signal generator, creating a sinusoid load-voltage or current, where frequency, amplitude and offset should be controlled from a PC. When working as a sinusoidal voltage signal generator, the FPGA should control the load voltage as: V(t) = A*cos(2*pi*t*f)+D, where A is the amplitude, f the frequency and D the offset. When working as a current generator the current should be controlled so: I(t)=A*cos(2*pi*t*f)+D. Given the practical limits of the power components, we accept Amax=12V and Imax=0.5A, but we encourage you to explore and document the practical voltage and current limits, and perhaps exceed our suggestion if possible.

You can use e.g. a lookup-table in the form of a predefined ROM/ARRAY to produce sinusoid approximations in VHDL. You are also encouraged to add other waveforms such as triangle and square when you have mastered the sinusoid generator.

The sinusoid frequency will be limited by practical considerations like balances between maximum switching frequency, power-filter bandwidth and acceptable ripple noise in the output signal. We encourage you to explore these limits and try to optimize the compromise between various limiting factors in order to support high frequency sinusoids, with minimal distortion/noise. You may for instance present us with different designs, each optimizing one parameter or compromise between parameters, e.g. a design for high quality and a different design for high frequency. Or design that is a good compromise between both.

You are free to use PWM, sigma/delta, a combination or perhaps other switching schemes to optimize your design, as you see fit.

Using a resistor as load, current and voltage will be proportional to each other. When your system is set to work as a voltage generator, demonstrate that it will produce the requested V(t), independent of the resistor value, down to the smallest resistor that does not cause you to exceed the maximum current limit of your transistors and/or inductor. When the system is in current mode, document that it will produce the requested I(t), independent of resistance, up to the largest resistor that will allow the current at the maximum voltage restriction.

In inductive loads, current and voltage are not in phase, and it is more demanding for the system to produce a specified V(t) or I(t). Using an electromagnet as a combined inductive and resistive load, document how well the system is able to produce V(t) and I(t). You may connect multiple electromagnets in series or add a power resistor to change the inductance and/or resistance of the load.

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Implementation methodology:

1. Configure one half-bridge as a constant connection to ground and use the other half-bridge generate waveforms. This will create only positive voltages/current across/through load.
2. Use both sides of the full bridge to create bi-polar waveforms so the voltage/current can be negative or positive (Option).

Hand-in

All VHD file (except Unity) should be uploaded in a zip-file along with a journal. Journals longer than 20 pages will not be accepted. The journal should as a minimum include the following:

- A block diagram showing vhdl modules and signal connections.
- Views and description of simulated modules (min. three modules). The simulation should cover all special cases.
- State diagram of at least one FSM from the implemented code.
- A diagram showing the electronics in the project.
- A picture of the physical setup.
- Documentation of V(t) and I(t) quality at relevant combinations of frequency, amplitudes and load, to document the agility and quality of your solution.
  Quality is the accuracy of the produced waveform in relation to the requested, and can be discussed in terms of e.g:
    - Ripple noise (switch noise that is not entirely removed by RL filter)
    - Amplitude error
    - Phase error
    - Distortion (e.g. due to imperfect regulation)
    - Perhaps other phenomenon/classifications

Hand in to discussion board on blackboard, date will be informed ASAP.