2008 Signal Integrity Seminars

taught by Dr. Howard Johnson

High- Speed Digital Design	Rochester, NY September 29 - 30 San Jose, CA October 27 - 28
Advanced High-Speed Signal Propagation	San Jose, CA October 29 - 30
High-Speed Noise and Grounding	San Jose, CA November 3 - 4

Inducing Metastability

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----------(QUESTION)----------

[EDITOR'S NOTE: In Vol.3 Issue 15, Howard Johnson discussed the general topic of "Metastability in Flip Flops."]

INDUCED METASTABILITY

Trent Shipley writes:

What if I *WANT* to induce the metastable state in a flip-flop?

Reasons:

--Laboratory investigation of the metastable phenomenon in flip-flops

--Demonstration of quantum principles in introductory physics lab

--Development of solid-state random number generators

--Use of random number generator circuitry to produce multi-latches with mutually entangled metastable states from which one could build solid- state quantum ALUs

----------(REPLY FROM DR. JOHNSON)----------

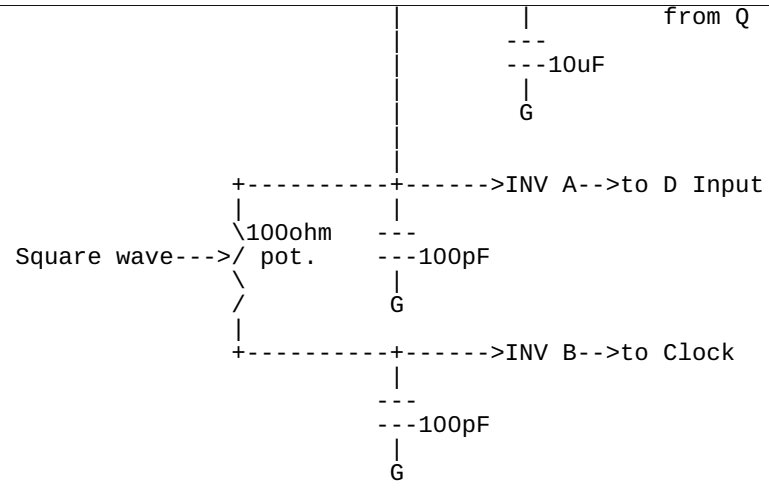
Thanks for your interest in High-Speed Digital Design.

The simple setup described below easily generates massive numbers of metastable events. The complete circuit appears on page 121 of my book, "High-Speed Digital Design: A Handbook of Black Magic". The circuit comprises one ordinary flip-flop into which I feed a D input, reset, and clock. An oscilloscope monitors the clock and Q output.

The input signals are repetitive with a cycle time of 1 microsecond. Each cycle I first reset the flip- flop, then release the reset, all while holding both clock and data low. Next, the circuit applies rising edges to both clock and data, in quick succession, with an adjustable skew. If the data edge arrives sufficiently early (compared to the clock) the flip-flip will latch a one. If the data edge arrives too late, the flip-flop will latch a zero. If the data edge arrives just at the wrong moment (violating the prescribed setup and hold times) the flip-flop will go metastable, producing a late output transition at the Q output.

The skew adjustment is done in a very simple manner, as depicted below. I start with one square- wave signal (at 1 MHz). This signal is fed to the center-tap of a 100-ohm, ten-turn potentiometer. Each leg of the potentiometer feeds a 100-pF capacitor, which in turn feeds a buffer gate (an inverter, INV A or INV B on the diagram) that squares up the resulting slightly-delayed signal.

+--------+----- <--Feedback



(The symbol "G" means "ground").

With the potentiometer set to mid-scale you will get equal delays in both legs (100pF x 50 ohms = 5 ns). When the potentiometer is offset to one side you get more or less delay on the two sides, producing a fixed amount of skew. With this setup I can set a predictable (and measurable) amount of data-to-clock skew ranging from -5 ns to +5 ns.

Now, here comes the tricky part. The metastable window on a flip-flop is extremely narrow, perhaps only a few picoseconds wide. Furthermore, it drifts with time, temperature, power supply voltage, and other factors. Once you set the potentiometer to create a lot of metastable events, drift in the flip-flop's metastable window will soon cause the circuit to fall off the metastable cusp, and the circuit will return to normal operation. You have to keep chasing the metastable window around if you want to observe events over a long period of time.

The algorithm for chasing the window is quite simple: if the flip-flop is reliably producing zeros, the data waveform is too early. If it is producing ones, the data waveform is too late. In other words, by looking at the output waveform (specifically, you need only look at the *average value* of the output waveform), you can tell which way to adjust the skew. What's really cool about my circuit is that I have added a feedback loop to automatically track drift in the metastable window.

My feedback circuit is beautifully simple. From the Q output I connect through a 1K resistor R1 to a 10 uF capacitor. The other side of the capacitor hooks to ground. This configuration makes a low-pass filter, with a time constant of about 10 ms. The voltage on the capacitor therefore tracks the *average* voltage on the Q output, averaged over the last 10,000 cycles.

I then feed the voltage on the capacitor through a second 1K resistor R2 to the input of the inverter marked "INV A" on the diagram, which serves as the data buffer. Remember this inverter is driven by an impedance of roughly 50 ohms from the potentiometer. Resistor R2 functions as a DC offset adjustment for the data signal coming out of the potentiometer. When Q is mostly ones, R2 delivers positive current towards the potentiometer, lifting the input to the inverter, causing negative-going edges (which will result in positive-going edges observed at the flip-flop) to be *slightly* delayed. The delay is just enough to cause the flip- flop to begin sampling more zeros.

Noise present within the circuit prevents me from setting the data-clock skew accurately enough to produce repeatable metastable delays much larger than about 5x the normal clk-Q interval, however, it does permit me to *observe* plenty of those very rare events using a digital scope with infinite- persistence. The feedback circuit keeps the data- clock timing centered around the metastable window long enough for me to count literally millions of metastable events.

Best Regards,
Dr. Howard Johnson

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