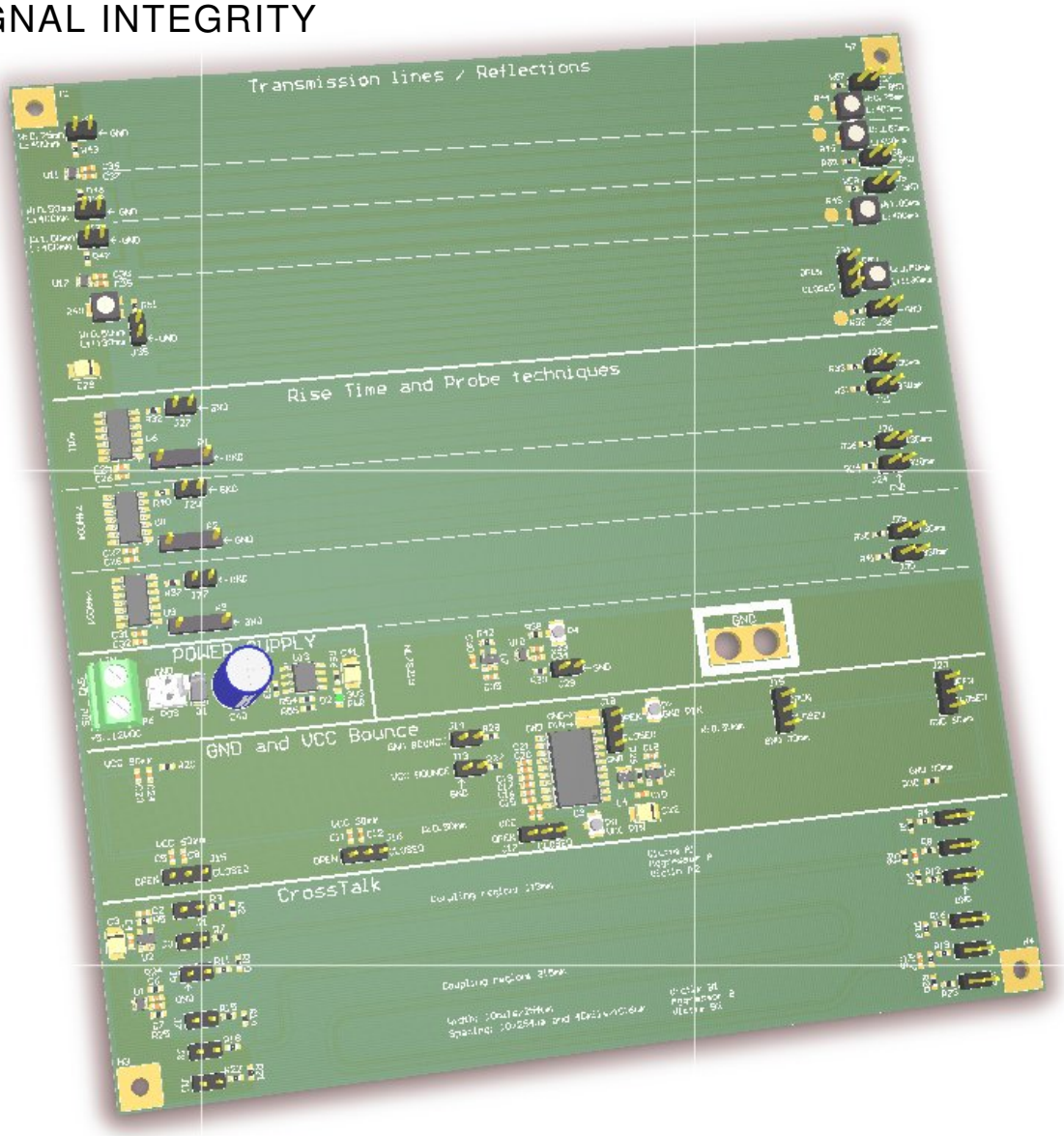
LABORATORY MANUAL FOR HIGHSPEED TEST PCB

SIGNAL INTEGRITY



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Whenever we attempt to get a computer to interact with the physical world, we use electrical signals, to represent and transmit information between the physical world and — ultimately — the software running on the computer. Unfortunately, signals can be distorted and interfered with, by the very electronics we design to handle them, as well as by external sources. As these phenomenons are often ignored in conventional electronics courses, many educational, research and commercial projects have experienced delays, problems or even failure, due to unforeseen problems with signal integrity.

This project aim at teaching students the basic theory behind signals, signal transmission and the major sources of distortion and interference, and how to maintain a signals purity of essence.

This documentation has been adapted from use in a dedicated 5ECTS signal integrity course, to use in a few introductory lab exercises.

"In theory, theory and practice are the same thing.
In practice, they are not!"

HTTP://WWW.SDU.DK

First printing,

Typeset using LaTeX

This document is a work in progress. At it's current state, it supply the minimum information necessary to perform exercises with the PCB. Ambitious students are urged to seek supplementary information about signal integrity from lectures, lab supervision, and external literature. Useful information about theoretical calculations can be found in [1], which also recommend further literature.

Cover image: 3D rendering of the test-PCB used in the exercises

1. Overall board description

This board is designed to demonstrate some of the basic issues and design techniques associated with single ended logic design.

It is highly recommended, that students are familiar with basic electronic and logic design techniques and components, at a level consistent with http://www.ti.com/lit/an/sdya009c/sdya009c.pdf

1.0.1. Power supply

The power supply is documented in [2, Page 2].

The board is supplied with a $5V$ to $12V$ DC voltage, connected to either the screw terminal, or the 2-pin Molex connector, marked "Power supply". The board is protected from reverse polarity by diode D1. The linear regulator U13 provide a regulated 3.3V supply, from the input voltage.

2. Rise times and probes

This exercise will illustrate the difference in rise- and fall times of different logic families, and how they impact our ability to measure the signals reliably with different types of probes.

2.1. Circuit description

The sub-circuit for this exercise is documented in detail in [2, Page 3].

A 12kHz square wave generator (U7) drive the inputs of 4 different simple logic IC's, that simply act as buffers for the square-wave signal. The IC's are:

U6: 4011 quad CMOS NAND gates. The 4000 family was the first family of CMOS logic IC's avialable. They date back to 1968[1] and are amazingly still produced. The primitive silicon production techniques of 1968, caused low transition speeds and high output impedance, which are maintained in modern copies, for backward compatibility.

U8: 74HC04 hex invertes. Starting out with NPN and PNP bipolar transisitors (74 series), later evolving into Shottky Bipolar transisors (74LS series), The 74HC series (HC=High Speed CMOS) branch of the 74 logic series, originated in the 1980'ies, as a much faster and powerful alternative to the 4000 series of CMOS based logic gates.

U9: 74AC04 hex inverters. The 74AC (AC=advanced CMOS) take advantage of better manufacturing techniques, to increase speed, compared to the earlier 74HC series.

U10: nc7sz19 Decoder/Demux. From the "TinyLogic" series, this ultra highspeed decoder, is a good example of one of the fastest logic IC's using single-ended output signals.

The outputs of all 4 different IC's are used to exemplify how digital signals can be measured in realistic circumstances.

As the nc7sz19 only has 2 outputs, they are demonstrated only with highspeed measuring points, while 4 outputs from each of the other types are used to illustrate different measurement techniques/circumstances:

[1] Yes, approximately 50 years ago!

- Direct measurement with normal oscilloscope probe, close to IC.
- Measurement with 1:21 high-speed pinheader probe close to IC
- Measurement with 1:21 high-speed pinheader probe 130mm from IC
- Measurement with 1:21 high-speed pinheader probe 330mm from IC

The nc7sz19 is demonstrated with the same 1:21 high-speed pinheader probe (close to the IC) used for the other 3 IC's, supplemented with a 1:21 high-speed coaxial probe for reference.

Note that the 1:21 probe has an impedance of 1005Ω, which will overload the output of the 4011 IC, and severely distort it's signal. It was a design error to use this probe type for the 4011, and it will be corrected in later revisions.

2.2. Preparation

Find and study the data sheets for the 4 IC's. The 4011, 74HC04 and 74AC04 have multiple manufacturers. The differences between these are minute, so for this exercise, it is not important which manufacturers data sheet you use.

Note that transition time and/or rise-fall times are not specified accurately, or not specified at all, as they depend on the load placed on the IC output.

The output impedance is not specified either, but the DC output resistance can be inferred from information about output voltage vs. output current.

Use the data sheets to estimate transition times and output resistances as best you can.

2.2.1. IBIS files

Modern electronic design can not rely on rough estimates and rules of thumb. Therefore, manufactures provide detailed mathematical (IBIS) models for their components, that can be simulated numerically, in order to evaluate their performance with specific loads and designs.

You can read more about IBIS here: http://www.ti.com/lit/an/szza034/szza034.pdf

Locate, download and study the IBIS file for the nc7sz19.

The IBIS file contain a detailed $v(t)$ specification for the output voltage of an unloaded output (representing the fastest possible transition times). Copy this into a mathematics program e.g. octave or matlab, plot it and determine the $10-90\%$rise and fall times of the device.

2.2.2. Probes and highspeed

Read the description of 3 common probe configurations at http://www.sigcon.com/Pubs/straight/probes.htm

Normal probes are similar to the first configuration. We can not afford the active probes described as the second configuration, but it is very easy to manufacture the 3. type configuration, which we use as high-speed probe for this exercise.

Study the circuit diagram for the test board, and note that the $1k\Omega$ resistors are placed in circuit on the PCB, so only the 50Ω coaxial cable is necessary. This is connected using a low-cost 2-pin pinheader.

2.3. Lab exercise

2.3.1. Normal probes

Start by using an ordinary 1:10 oscilloscope probe. Note the input impedance specified on the oscilloscope. Remember to note both the resistive part and the capacitive part.

Use the double hole in the test PCB to connect the GND wire from he probe to the groundplane of the PCB.

Measure and document the rising and falling edges of the 4011, 74HC04 and 74AC04 at the test points connected directly to IC output pins.

2.3.2. Normal probes with short grounds

Unmount the GND wire from the probe. Measure it's length, and estimate it's contribution to self inductance.

Note that the test points have been designed to enable the probe tip to touch the test point, while the GND-ring next to the tip touches a GND pin.

Use this feature to simultaneous connect the probe input and GND to the test point signal and GND, and remeasure and document the rising and falling edges.

2.3.3. 1:21 High speed probe

Configure the oscilloscope input for 50Ω input impedance, and connect a 50Ω coaxial cable with pin-header to the input.

Use the designated high-speed test points, to remeasure and re-document the rising and falling edges of the 4011, 74HC04, 74AC04 as well as the. nc7sz19.

Note the oscilloscope bandwidth

Reflect on the bandwidth required to measure the expected transition times for each of the IC types, and estimate how fast transition-times the scope you have actually support.

Go to the LAB supervisor and document the rising and falling edges of the nc7sz19 transitions, using a 2GHz bandwidth oscilloscope.

3. Reflections on transmission lines

This exercise will illustrate the practical aspects of reflections on PCB-trace transmission lines, for various geometries, and various types of termination.

3.1. Circuit description

The sub-circuit for this exercise is documented in detail in [2, Page 4].

It consist of 4 microstriplines, driven by individual outputs from 2 nl17sz19 IC's, which is one of the fastest single-ended output types in our inventory. [3]

The PCB is manufactured in 3 different thicknesses: 1.6mm, 0.8mm and 0.5mm. The micro-stripline geometry is quite different between the two thicknesses, and so are L', C', Z_0. It is left as an exercise to the students to calculate these parameters, using the formulas or tables in [1], the calculation tools in simulation programs like *Qucs* or a field-solver like ATLC.

Number	**Length** *[mm]*	**Width** *[mm]*
1	*400*	*0.25*
2	*400*	*0.50*
3	*400*	*1.00*
4	*1130*	*0.50*

Each of the 4 transmission lines have a $1k\Omega$ 1:21 pin-header test-point in either end, allowing students to make high bandwidth measurements with a 50Ω coaxial cable, connected to a 50Ω oscilloscope input. Apart from trace width, the circuits for line 1-3 are identical, while the circuit for line 4 has a few extra features.

3.2. Termination

The lines: 1-4 are all end-terminated with a 500Ω variable resistor, that allow students to adjust the termination impedance in the range $[0\Omega; 500\Omega]$. By adjusting the termination, while simultaneously monitoring the reflections on the line, the termination can be adjusted to match the line impedance. The resistance of the 500Ω variable resistor, can then be measured by an external ohm-meter, by powering off the PCB.

Line 4 is special, as it is configured for both source- (R49) and end-termination (R50), with identical 500Ω variable resistors. Additionally, the end termination can be disconnected, by removing the jumper: J34. For end-termination experiments, connect J34 and set $R49 = 0\Omega$. For source termination experiments, disconnect J34.

3.3. Preparation

- Verify the PCB thickness
- Assuming FR4 material, with $\epsilon_r \simeq 4$, use a field solver, formulas or tables, to estimate the characteristic impedance: Z_0, the propagation velocity and the line propagation delay t_p, for all the 4 lines, for both thicknesses. Ambitions students are also welcome to determine the distributed capacitance and inductance: L', C'.
- To simplify the exercise, we can assume the $10 - 90\%$ rise time of the nl17sz19 outputs to be $400ps$, and it's output impedance $Z_o = R_o = 12\Omega$ Ambitious students should study the nl17sz19 data sheet and particularly it's IBIS file, in order to understand how output impedance, rise- and fall-times can be calculated or estimated with better accuracy, taking into account the manufacturers detailed information about the driver, as well as it's output impedance.
- Calculate the reflection coefficients at the near and far end of the traces, using the nl17sz19 output impedance, and the maximum setting of $R = 500\Omega$ of the far end termination.
- Estimate the electrical length of the signal on the various traces.
- Are the traces "long" or "short" compared to the signal?
- (Optional) set up a qucs simulation of the system, using a file based generator, and simulate the various transmission lines.

3.4. LAB work

- For each of the board thicknesses:

- For each of the traces 1-3
  - Verify that the reflections appear as expected in both the far-end and near end of the line, at various settings of the end termination R_E, including $R_E = 0\Omega$ and $R_E = 500\Omega$.
  - Adjust R_E to give minimal reflections (ideally no reflection), disconnect power, and measure R_E with an ohmmeter.
  - Compare R_E for minimal reflections, with the theoretical Z_0 of the trace.
  - Document and comment selected situations from the above steps.
- For trace 4
  - Set the source termination $R_S = 0$ and connect the jumper J34, so the trace is configured for end-termination.
  - Repeat the steps for trace 1-3.
  - Do there appear to be signal loss, on this $1.13m$ long trace?
  - Document/comment relevant data associated with long traces.
  - Configure the line for source termination, by disconnecting J34.
  - Verify, that reflections appear as expected in both ends, for various settings of R_S, including $R_S = 0$, $R_S = 500\Omega$.
  - Adjust R_S to give minimal source reflection. Document the reflections in either end.
  - Disconnect power, and measure R_S. Check if $R_o + R_S$ match the theoretical Z_0 of the trace.
  - Attempt to measure the signal at the middle of the line, and document/comment what you see.

4. Ground bounce and decoupling

Most IC's we use, have single-ended inputs and outputs, that rely on controlling the output voltage, or sampling the input voltage, in relation to the common voltage reference of $0V$ or GND. In order to do this, they must be supplied with a well defined and stable supply voltage, and there must not be significant voltage differences across the network connecting the common $0V$ or GND points on the different IC's in the circuit.

As we become aware of the parasitic self inductance and capacitance lurking in our circuits, we have to realize that this is not at all an easy task, when transition times become short.

4.1. Circuit description

The sub-circuit for this exercise is documented in detail in [2, Page 5]

The circuit is designed to study the performance of a single IC: U3, which is a 74AC574 octal D-flip-flop. U3 contain 8 D-flip-flops, that share their CLK input, but have separate data inputs and outputs.

6 of the flip-flops — number 0 to 5 — are configured to change simultaneously between 1 and 0 with a repetition frequency of $f_r \simeq 6kHz$. Their outputs are loaded with the maximum capacitive load allowed by the datasheet, in order to draw maximum current from the IC's outputs when their output change state. This will in term create high currents in the IC's supply network: VDD and GND.

2 of the flip-flops are configured to maintain a state of 1 and 0 — number 6 and 7 respectively. Their outputs are connected directly to individual $1:21$ probe connectors, allowing us to monitor the voltage on those pins, as the 6 output changes state.

As the output stage of the IC are transistors, connecting the output pins directly to the IC's internal VDD and GND network, the voltage on O6 and O7, is actually very close to the IC's internal VDD and GND voltages, allowing us an insight into the internal voltages of the IC during switching.

Ideally, the voltage on O6 should remain stable at $3.3V$, and the voltage on O7 at $0V$. However, due to nonzero impedances in the internal wiring of the IC, it's pins, and the external wiring of the PCB, the IC's internal supply voltages may stray from the ideal. So much so, that it may fail to produce valid output levels.

The PCB is designed to experiment with different length PCB traces connecting the IC's GND pin to PCB ground. This is done by placing jumpers at one of 3 possible locations, or by soldering/unsoldering a via.

It is also designed to decouple the VCC network with capacitors placed different distances along a PCB trace, from the IC VCC terminal, in the same fashion.

4.2. Preparation

Locate and download the data sheet of U3. For instance: http://www.ti.com/lit/ds/symlink/cd74ac574.pdf

Find the power dissipation capacitance: C_{PD} of U3.

You can read more about IC power dissipation in http://www.ti.com/lit/an/scaa035b/scaa035b.pdf

Study and understand the circuit diagram, as well as the PCB layout implementing it.

A transition from $0V$ to $3.3V$ or vice versa, will charge the load capacitor, as well as the intenal capacitance of the IC, with a charge of $Q = V\,C$ The change in charge is also known as current: $I = dQ/dt$.

Charging a capacitance in a specific amount of time: ΔT, will thus require a current pulse with width: ΔT and area of Q

Assume a triangular current pulse with $\Delta T = 2ns$ and area of: $Q = 3.3V(C_{load} + C_{PD})$

Sketch $V(t)$ and $I(t)$ for rising and falling edges.

Estimate the currents rate of change: dI/dt during current pulses.

If the current should flow through a self inductance: L, the self inductance will cause a voltage drop of: $\Delta V = L\frac{dI}{dt}$

How much self inductance will it take in the supply network to cause a voltage drop, that will violate the IC's specification for minumum supply voltage?

How much self inductance is allowed if the transition time: $\Delta T = 1ns$ or $\Delta T = 500ps$

4.3. Lab work

A. 4011 NAND gate

This chapter is yet incomplete - refer to proper data sheet and information given in class

At 5V supply, the transition times can be expected to be $t_r \simeq 100 - 200ns$. The output impedance can be roughly estimated to $R_o \simeq 800\Omega$

The very high output impedance make the actual transition time highly dependent on the load.

B. 74HC04 Inverter

This chapter is yet incomplete - refer to proper data sheet and information given in class

At 5V supply, it can be assumed to have transition times of $t_r \simeq 4 - 8ns$ and output impedance of $R_o \simeq 75\Omega$

The high output impedance make the transition time quite dependent on the load.

C. 74AC04 Inverter

This chapter is yet incomplete - refer to proper data sheet, IBIS model and information given in class

At 5V supply, it can be expected to have transition times of $t_r \simeq 1 - 2ns$ and output impedance of $R_o \simeq 20\Omega$

D. nc7sz19 Decoder

This chapter is yet incomplete - refer to proper data sheet, IBIS model and information given in class

A simple estimation of it's output impedance is $Z_o \simeq 12\Omega$

A simple estimation of it's rise- and fall-times are: $t_r \simeq t_f \simeq 400ps$

E. Wish-list for next version

A test point for measuring the signal in the middle of the 1.13 meter long line.

Bibliography

[1] A. S. Sørensen, "Notes for high speed electronics," notes for this course.

[2] C. Albertsen, "Documentation of emb2 test pcb," Mærsk Instituttet, Tech. Rep., Feb. 2013.

[3] Fairchild, "Ibis model of nc7sz19," Mar. 2001.