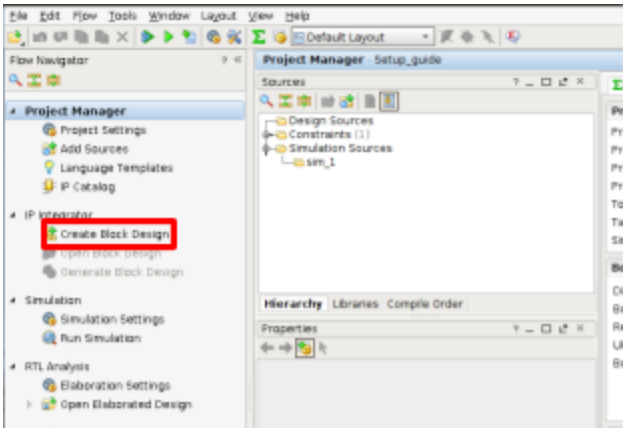
Create project template

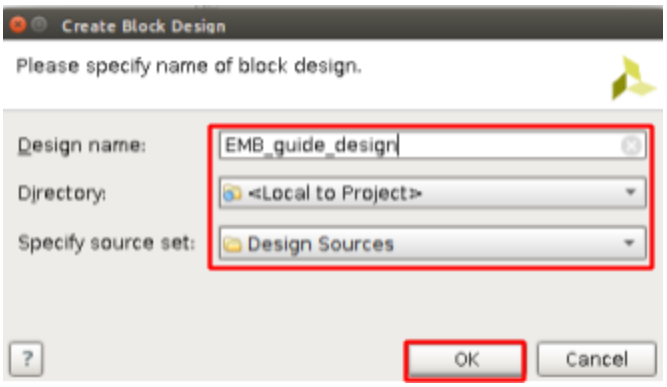
This guide demonstrates how to setup a simple project in Vivado. Before following this guide create a project like in the guide for setup project without source files.

1) Follow the “Vivado_setup_project.pdf” guide to setup a project

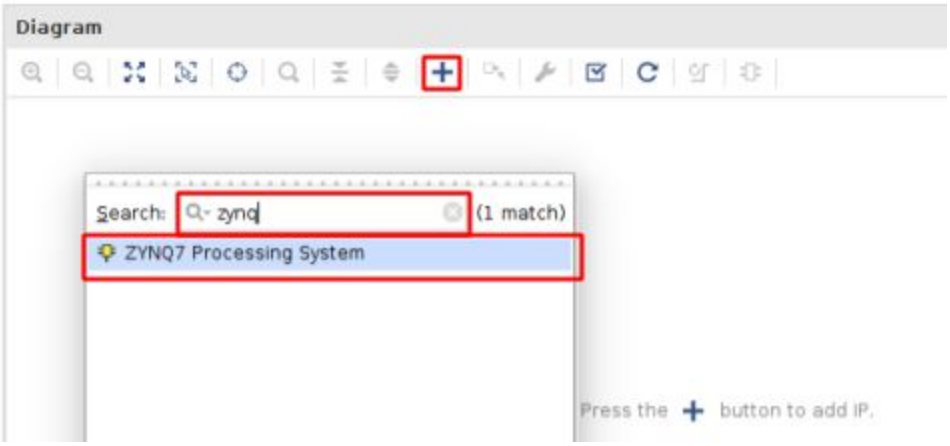
2) From the “Project manager” window press “Create Block design”



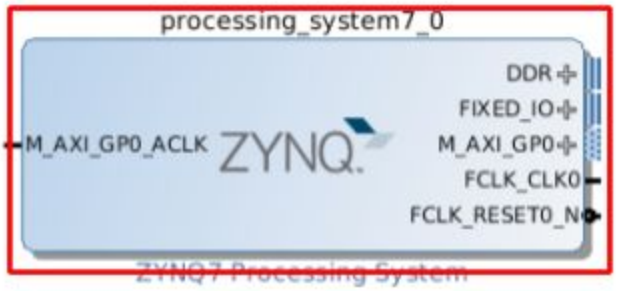
3) Enter a design name and chose directory and source set as shown below. Vivado opens a window called “Diagram”.



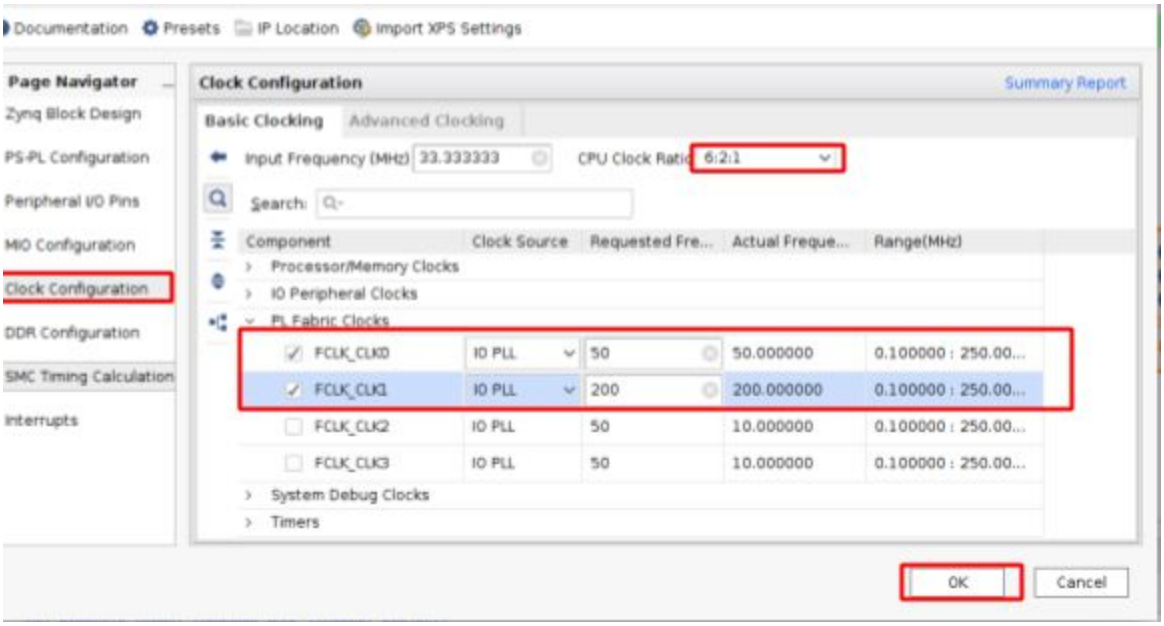
4) In the toolbar under “IP integrator” select “Open Block Design”. Click on the + sign and type “zynq”, select the “ZYNQ7 Processing System”



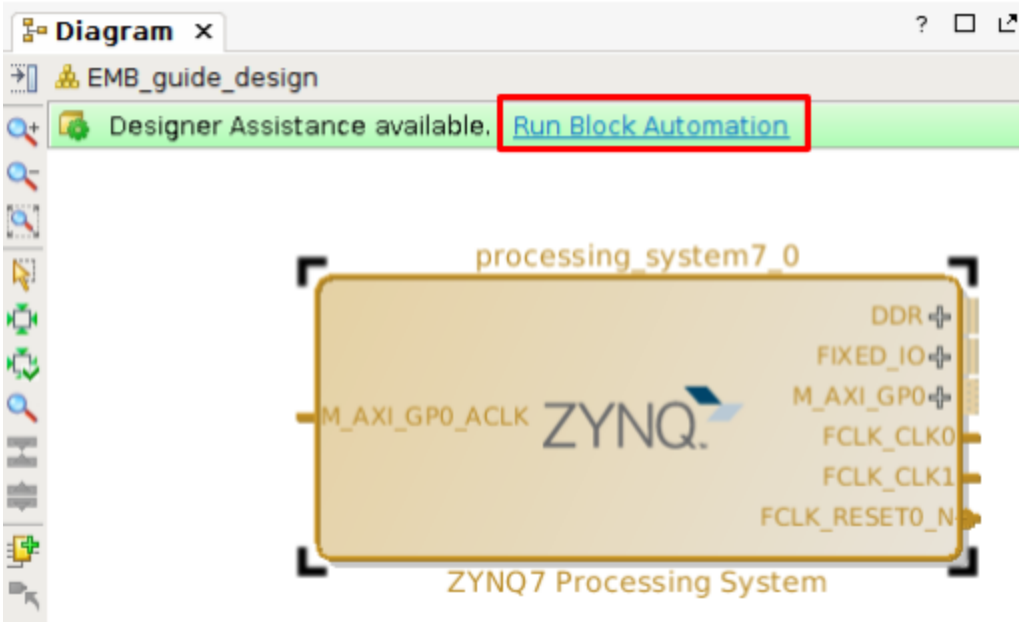
5) Double click on the ZYNQ IP in the “Diagram”



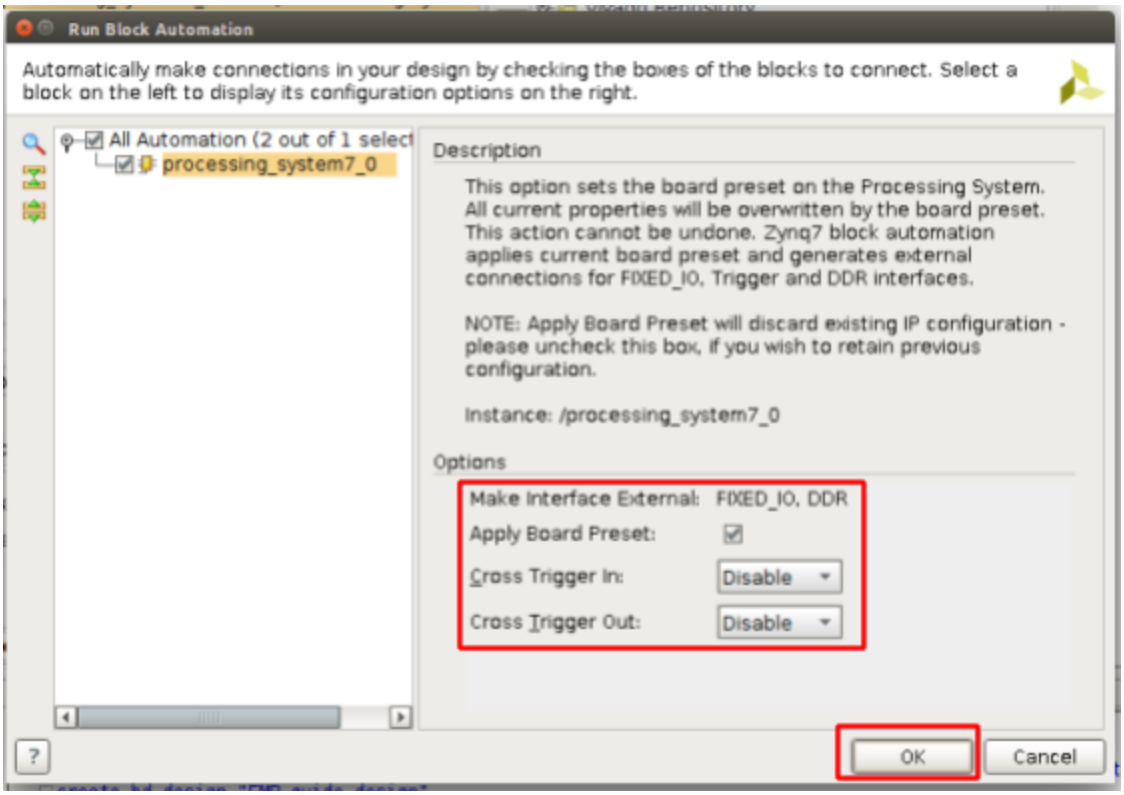
6) In the IP wizard go to “Clock Configuration” and setup the “PL Fabric Clocks” as shown in the images below



7) Click on the “Run Block Automation” in top of the “Diagram” window

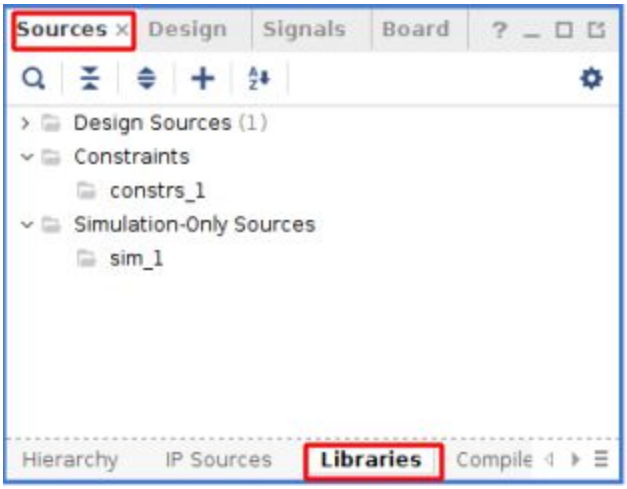


8) Make sure you have the options as shown below before clicking “OK”. You should now see the DDR and FIXED_IO attached to the ZYNQ IP.



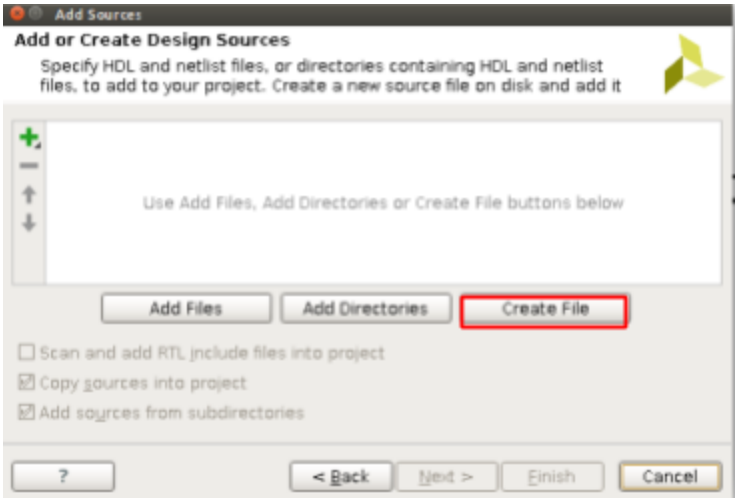
9) In the window Sources->Libraries (see below) right click and select “Add Sources...”

and the add wizard shows up

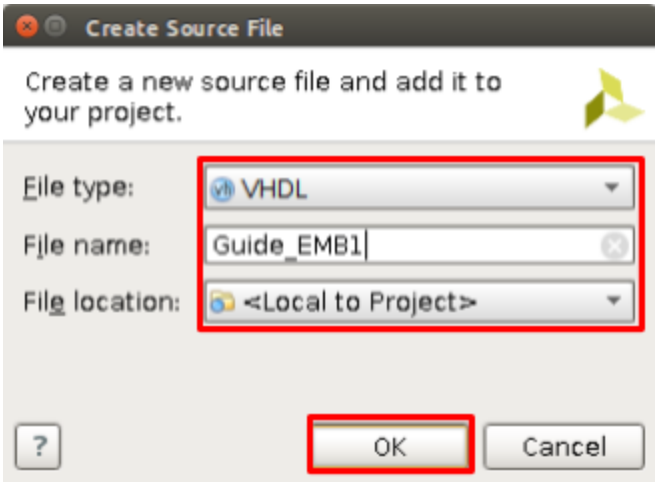


10) Select “Add or create design sources” and click “next”

11) Click “Create file”

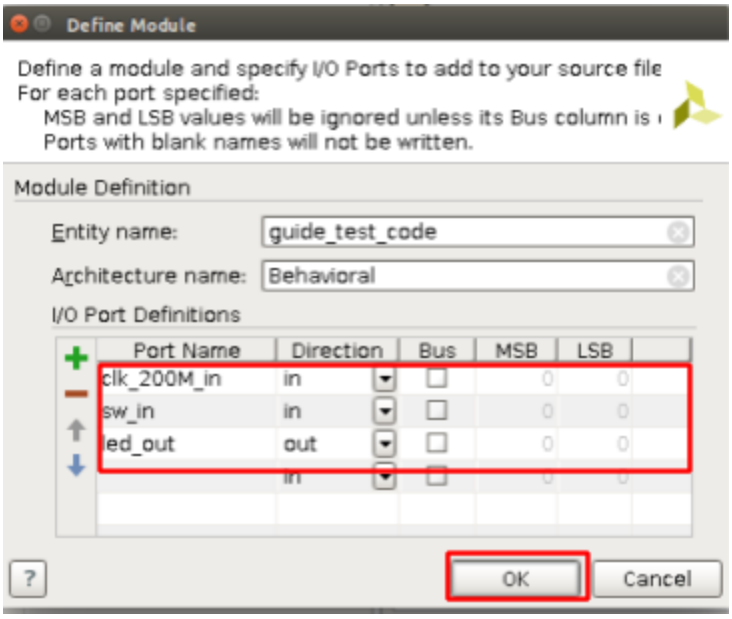


12) Select “VHDL” file type, some file name and “Local to Project”



13) In the “Add Sources” window click “Finish”

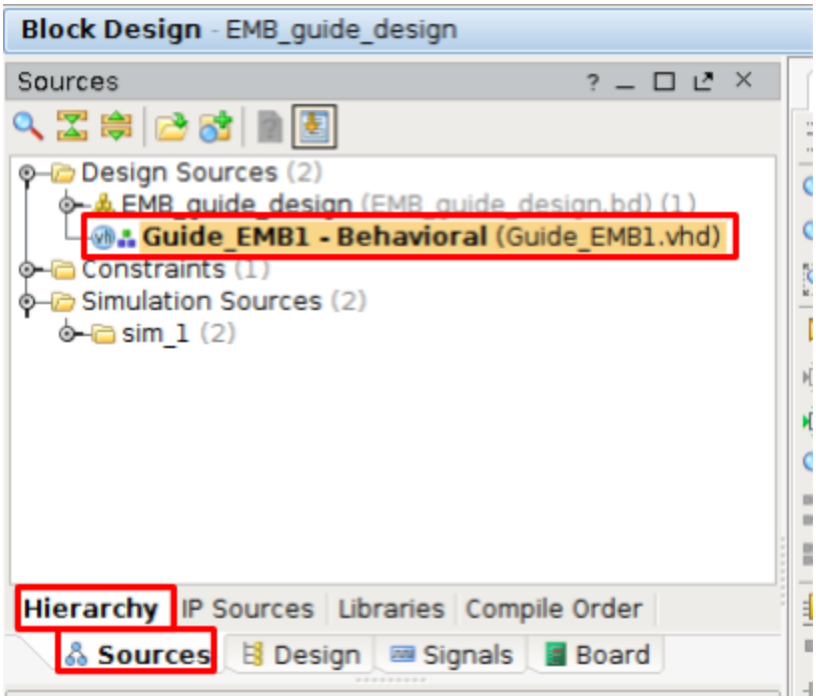
14) If you already know which input and output you want for the module then you can add them in the window(see below). If not then you can add them manually later. Click “OK” when you are done defining your ports.



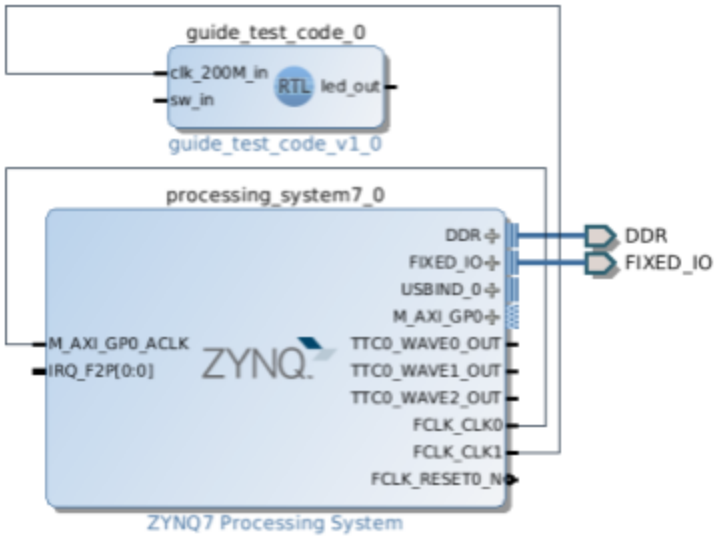
15) Now a .vhd appears under Design Sources->VHDL->xil_defaultlib. Open the file and add some very simple code like in the image below and save the file

```
34 entity guide_test_code is
35     Port
36     (
37         clk_200M_in  : in STD_LOGIC;
38         sw_in        : in STD_LOGIC;
39         led_out      : out STD_LOGIC
40     );
41 end guide_test_code;
42
43 architecture Behavioral of guide_test_code is
44
45 begin
46
47 ----------------------------------------------------------------
48 -- Very simple code
49 ----------------------------------------------------------------
50 sync_proc: process(clk_200M_in, sw_in)
51 begin
52     if rising_edge(clk_200M_in) then
53         led_out <= sw_in;
54     end if;
55 end process sync_proc;
56
57 end Behavioral;
```

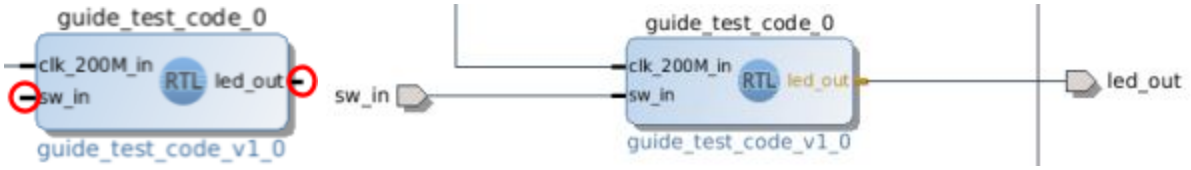
16) Go to the window “Sources” and “Hierarchy” right click on the .vhd file you created and select “Add Module to Block Design” and the module will appear in the “Diagram”



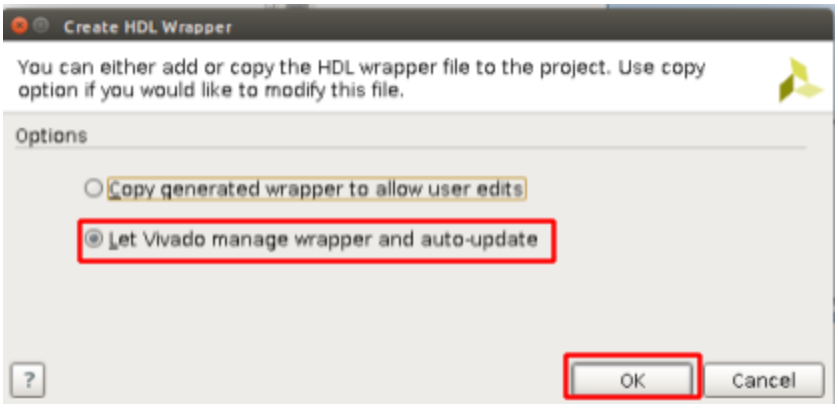
17) Connect the clk “FCLK_CLK0” to the AXI clk on the input of the ZYNQ IP and the “FCLK_CLK1” to your new block as shown in the image below.



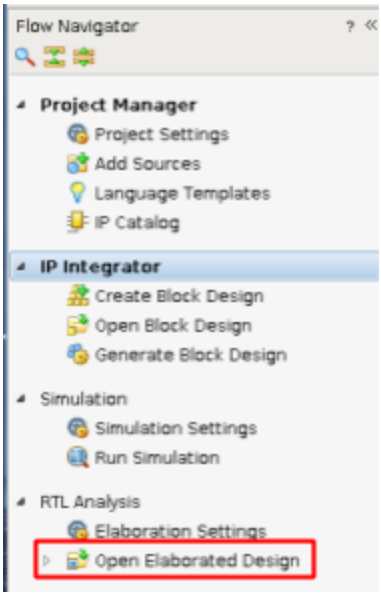
18) Right click on the in- and outputs of you vhdl module (one at a time) and select “make external”



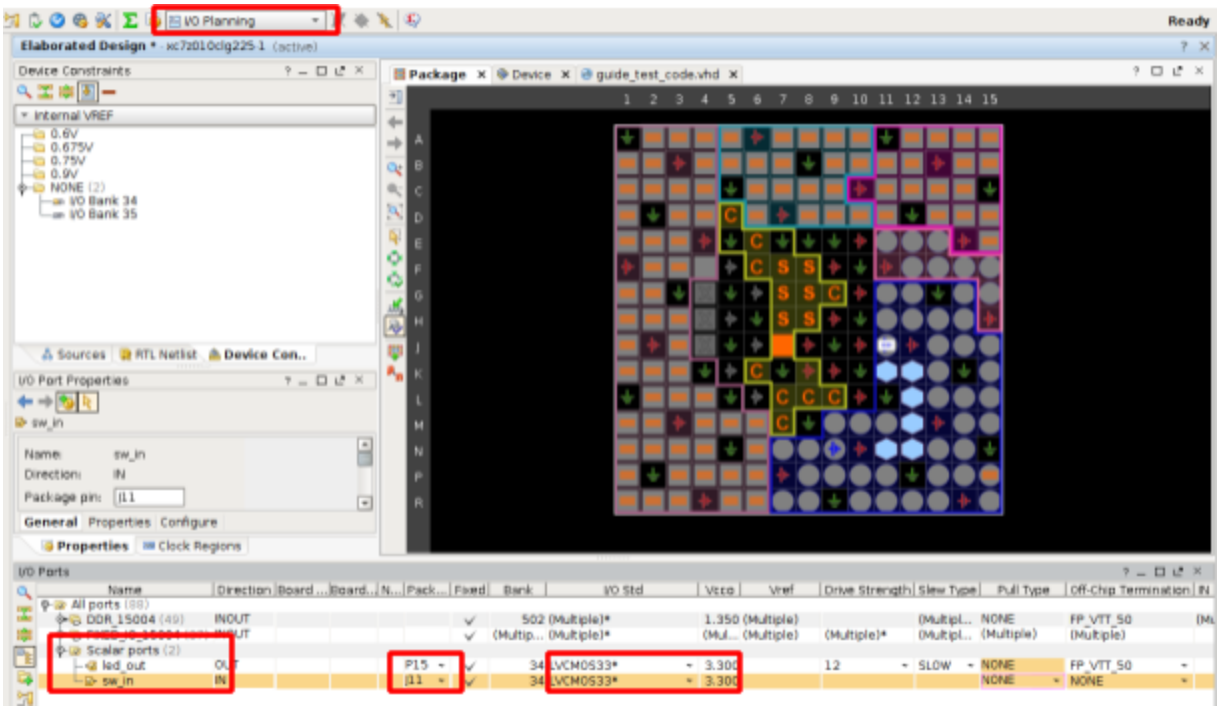
19) Right click on the block design file “EMB_guide_design” or what you called it and select “Create HDL Wrapper”. In the wizard select as shown in the image below and click “OK”



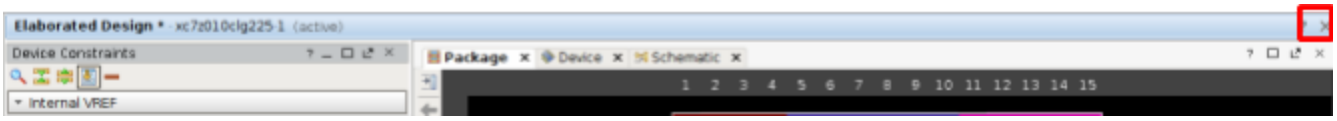
20) In the Flow Navigator under RTL Analysis click on “Open Elaborated Design” and select “OK” in the window that pops up and just ignore the critical warnings in the next window.

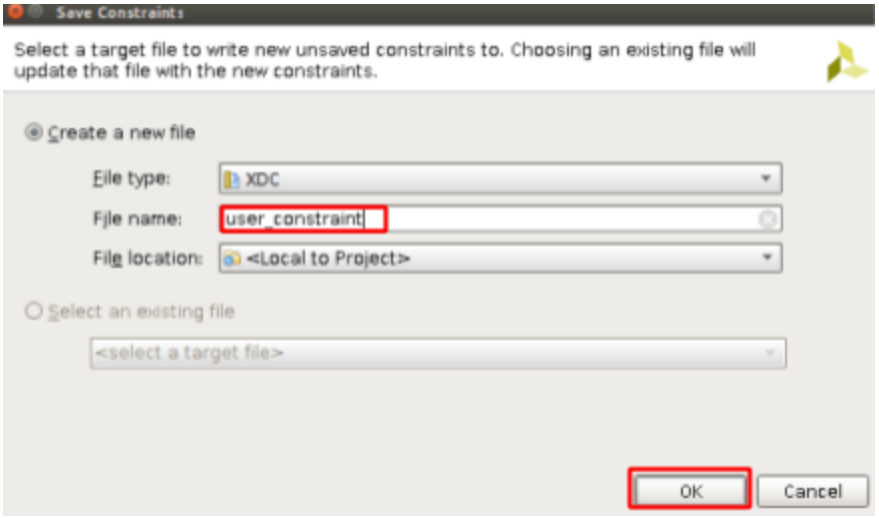


21) Change the window to I/O Planning and setup the physical in- and output ports for your project. Use the pin header file from Blackboard to figure out which ports you want to use. Since we are using 3.3V port set “I/O Std” to “LVCMOS33* and chose the “Pull Type” that fits your hardware design.



22) Close the “Elaborated Design” window press “OK” to close and “Yes” to save. Choose a filename for you constraint file and click “OK”





23) Your first project is done and ready be used in simulation or to program into the FPGA.