

CD4001B, CD4002B, CD4025B Types

CMOS NOR Gates

High-Voltage Types (20-Volt Rating)

Quad 2 Input – CD4001B

Dual 4 Input – CD4002B

Triple 3 Input – CD4025B

CD4001B, CD4002B, and CD4025B
 NOR gates provide the system designer with direct implementation of the NOR function and supplement the existing family of CMOS gates. All inputs and outputs are buffered.

The CD4001B, CD4002B, and CD4025B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

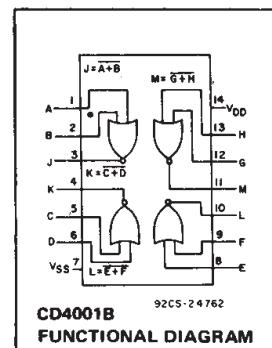
STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS	
	V_O (V)	V_{IN} (V)	V_{DD} (V)	+25				Min.	Typ.	Max.		
				-55	-40	+85	+125					
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA	
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5		
	–	0,15	15	1	1	30	30	–	0.01	1		
	–	0,20	20	5	5	150	150	–	0.02	5		
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA	
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–		
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–		
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	–	mA	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–		
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	–		
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	–		
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V	
	–	0,10	10	0.05				–	0	0.05		
	–	0,15	15	0.05				–	0	0.05		
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	V	
	–	0,10	10	9.95				9.95	10	–		
	–	0,15	15	14.95				14.95	15	–		
Input Low Voltage, V_{IL} Max.	0,5,4,5	–	5	1.5				–	–	1.5	V	
	1,9	–	10	3				–	–	3		
	1,5,13,5	–	15	4				–	–	4		
Input High Voltage, V_{IH} Min.	0,5	–	5	3.5				3.5	–	–	V	
	1	–	10	7				7	–	–		
	1,5	–	15	11				11	–	–		
Input Current I_{IN} Max.		0,18	18	±0,1	±0,1	±1	±1	–	±10 ⁻⁵	±0,1	μA	

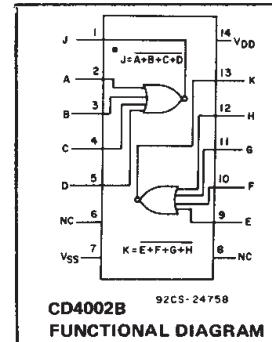
Features:

- Propagation delay time = 60 ns (typ.) at $C_L = 50 \text{ pF}$, $V_{DD} = 10 \text{ V}$
- Buffered inputs and outputs
- Standardized symmetrical output characteristics
- 100% tested for maximum quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 - 1 V at $V_{DD} = 5 \text{ V}$
 - 2 V at $V_{DD} = 10 \text{ V}$
 - 2.5 V at $V_{DD} = 15 \text{ V}$
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of "B" Series CMOS Devices"

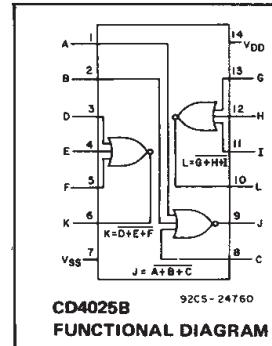
1 V at $V_{DD} = 5 \text{ V}$
 2 V at $V_{DD} = 10 \text{ V}$
 2.5 V at $V_{DD} = 15 \text{ V}$



CD4001B
FUNCTIONAL DIAGRAM



CD4002B
FUNCTIONAL DIAGRAM



CD4025B
FUNCTIONAL DIAGRAM

CD4001B, CD4002B, CD4025B Types

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT $\pm 10\text{mA}$

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearity at 12mW/ $^\circ\text{C}$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55 $^\circ\text{C}$ to $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg}) -65 $^\circ\text{C}$ to $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch (1.59 \pm 0.79mm) from case for 10s max $+265^\circ\text{C}$

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	ALL TYPES LIMITS		UNITS
		V_{DD} VOLTS	TYP.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	125	ns
		10	60	
		15	45	
Transition Time, t_{THL}, t_{TLH}		5	100	ns
		10	50	
		15	40	
Input Capacitance, C_{IN}	Any Input	5	7.5	pF

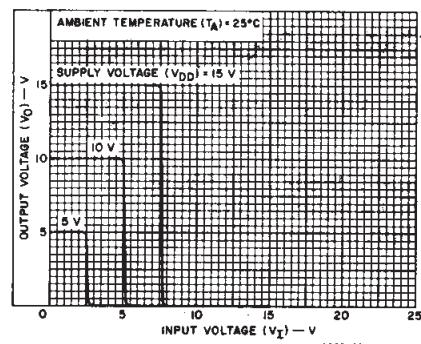


Fig. 1 – Typical voltage transfer characteristics.

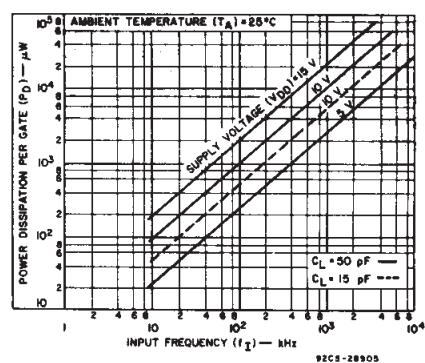


Fig. 2 – Typical power dissipation vs. frequency.

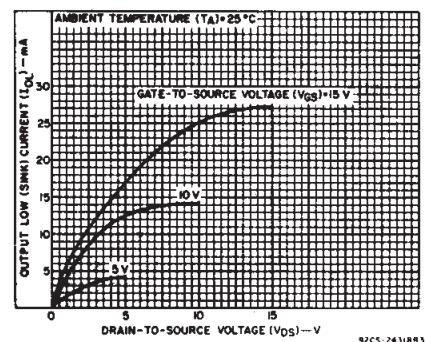


Fig. 3 – Typical output low (sink) current characteristics.

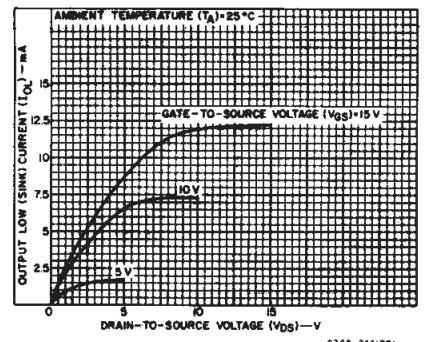
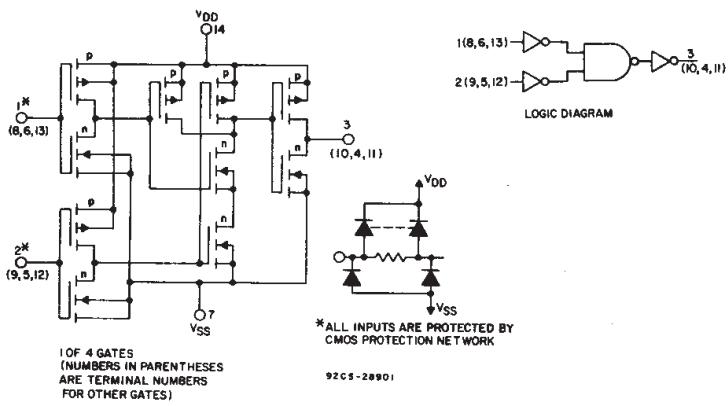
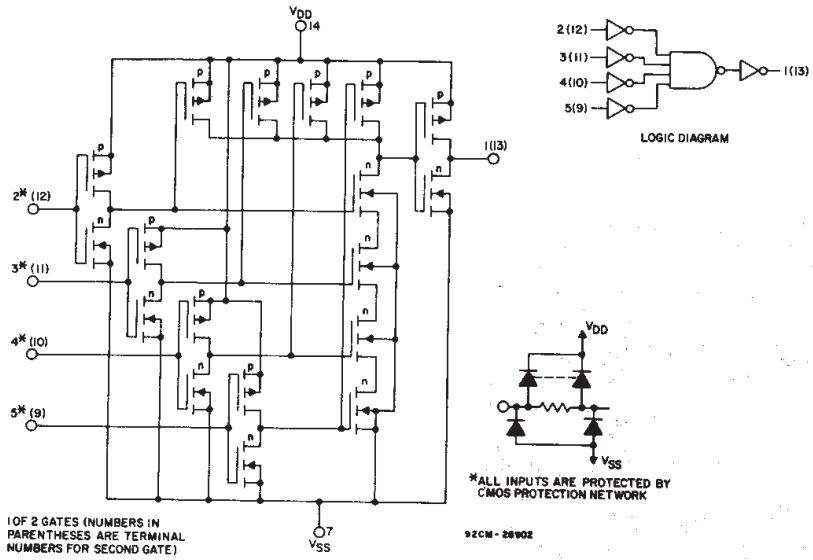
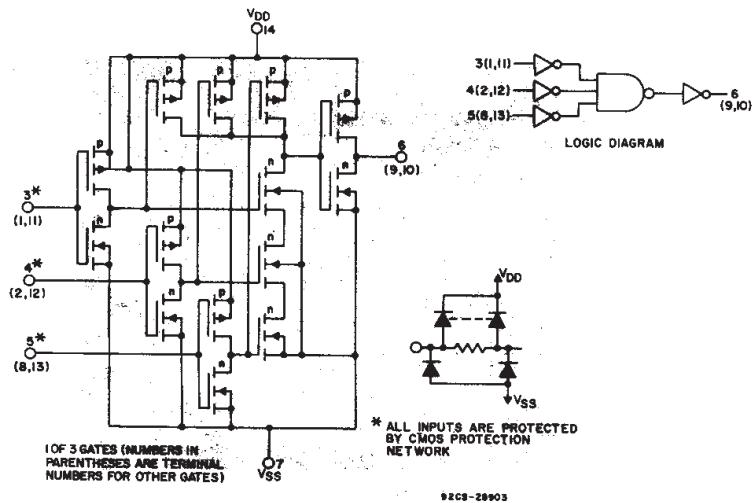
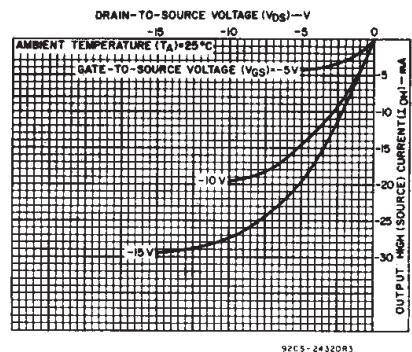
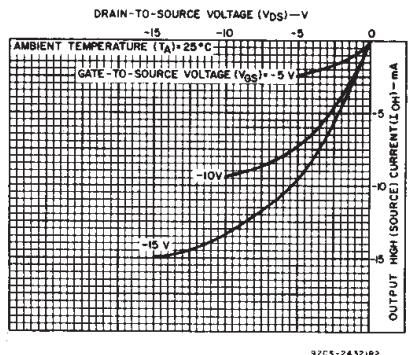
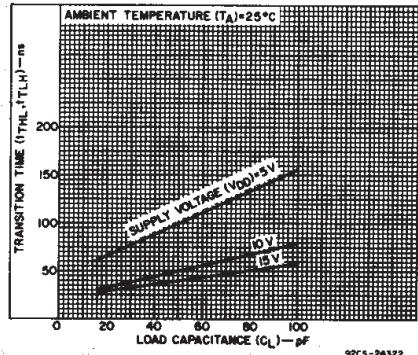
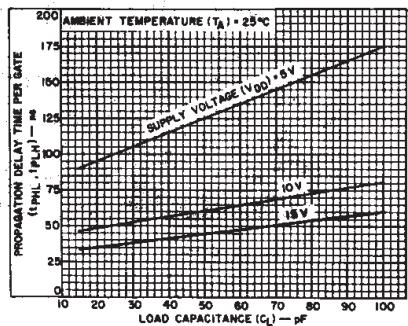


Fig. 4 – Minimum output low (sink) current characteristics.

CD4001B, CD4002B, CD4025B Types

Fig. 5 – Schematic and logic diagrams for CD4001B.

Fig. 6 – Schematic and logic diagrams for CD4002B.

Fig. 7 – Schematic and logic diagrams for CD4025B.

Fig. 8 – Typical output high (source) current characteristics.

Fig. 9 – Minimum output high (source) current characteristics.

Fig. 10 – Typical transition time vs. load capacitance.

Fig. 11 – Typical propagation delay time vs. load capacitance.

CD4001B, CD4002B, CD4025B Types

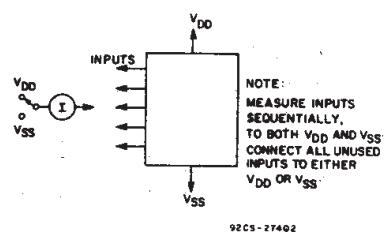


Fig. 13 – Input leakage current test circuit.

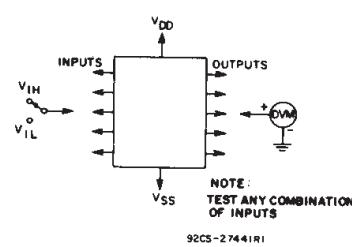


Fig. 14 – Input-voltage test circuit.

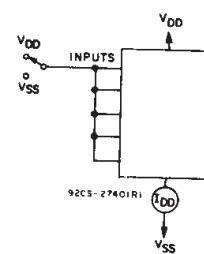
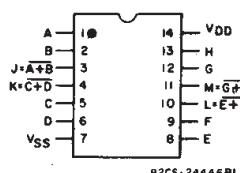
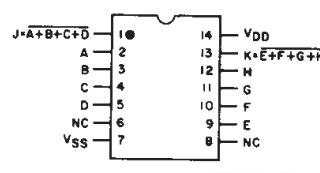


Fig. 15 – Quiescent-device current test circuit.

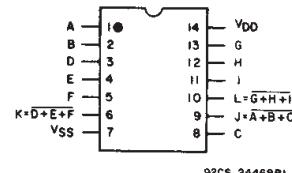
TERMINAL ASSIGNMENTS (TOP VIEW)



CD4001B

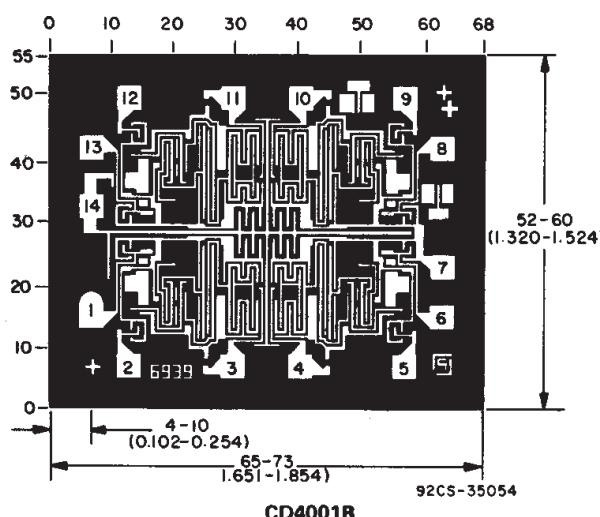


NC = NO CONNECTION

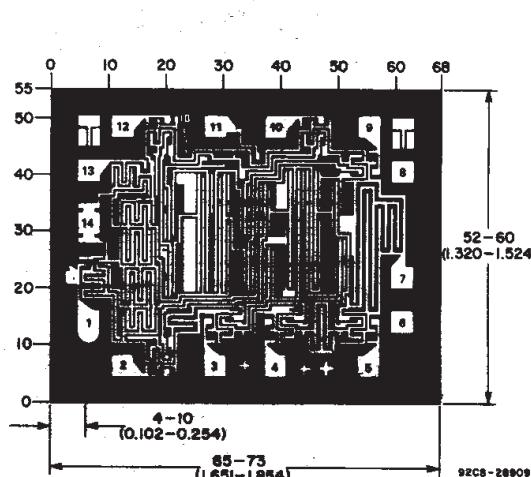


CD4025B

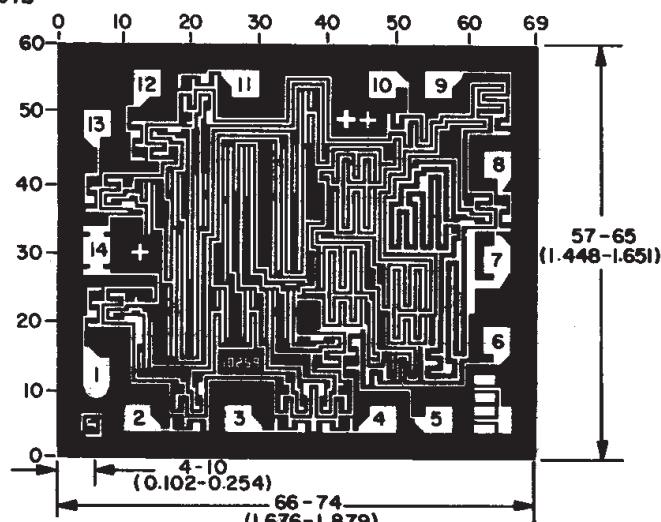
Chip Dimensions and Pad Layouts



CD4001B



CD4002B



CD4025B

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
7704403CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	7704403CA CD4002BF3A	Samples
89263AKB3T	OBsolete	CFP	WR	16		TBD	Call TI	Call TI	-55 to 125		
CD4001BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4001BE	Samples
CD4001BEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4001BE	Samples
CD4001BF	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4001BF	Samples
CD4001BF3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4001BF3A	Samples
CD4001BF3AS2534	OBsolete	CDIP	J	14		TBD	Call TI	Call TI			
CD4001BM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4001BM	Samples
CD4001BM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4001BM	Samples
CD4001BM96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4001BM	Samples
CD4001BM96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4001BM	Samples
CD4001BMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4001BM	Samples
CD4001BMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4001BM	Samples
CD4001BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4001B	Samples
CD4001BNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4001B	Samples
CD4001BPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM001B	Samples
CD4001BPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM001B	Samples
CD4001BPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM001B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4002BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4002BE	Samples
CD4002BEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4002BE	Samples
CD4002BF	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4002BF	Samples
CD4002BF3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	7704403CA CD4002BF3A	Samples
CD4002BM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4002BM	Samples
CD4002BM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4002BM	Samples
CD4002BMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4002BM	Samples
CD4002BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4002B	Samples
CD4002BNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4002B	Samples
CD4002BNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4002B	Samples
CD4002BPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM002B	Samples
CD4002BPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM002B	Samples
CD4002BPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM002B	Samples
CD4025BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4025BE	Samples
CD4025BEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4025BE	Samples
CD4025BF	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4025BF	Samples
CD4025BF3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4025BF3A	Samples
CD4025BM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4025BM	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4025BM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4025BM	Samples
CD4025BMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4025BM	Samples
CD4025BMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4025BM	Samples
CD4025BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4025B	Samples
CD4025BNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4025B	Samples
CD4025BPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM025B	Samples
CD4025BPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM025B	Samples
JM38510/05252BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/05252BCA	Samples
JM38510/05254BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/05254BCA	Samples
M38510/05252BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/05252BCA	Samples
M38510/05254BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/05254BCA	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.



www.ti.com

PACKAGE OPTION ADDENDUM

24-Aug-2014

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4001B, CD4001B-MIL, CD4002B, CD4002B-MIL, CD4025B, CD4025B-MIL :

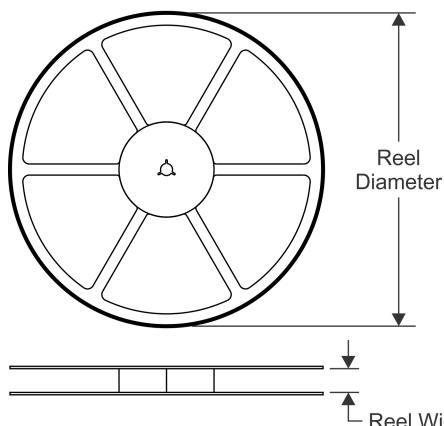
- Catalog: [CD4001B](#), [CD4002B](#), [CD4025B](#)
- Military: [CD4001B-MIL](#), [CD4002B-MIL](#), [CD4025B-MIL](#)

NOTE: Qualified Version Definitions:

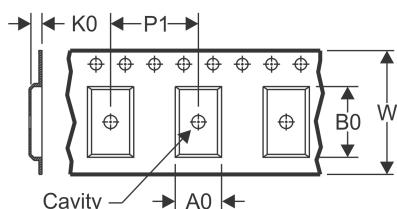
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

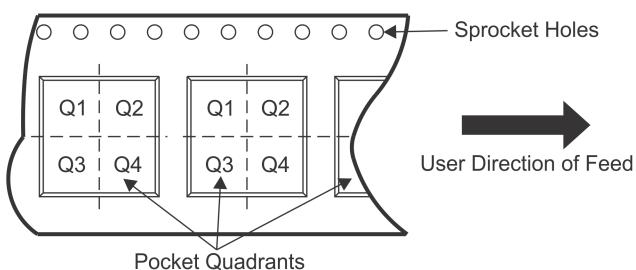


TAPE DIMENSIONS



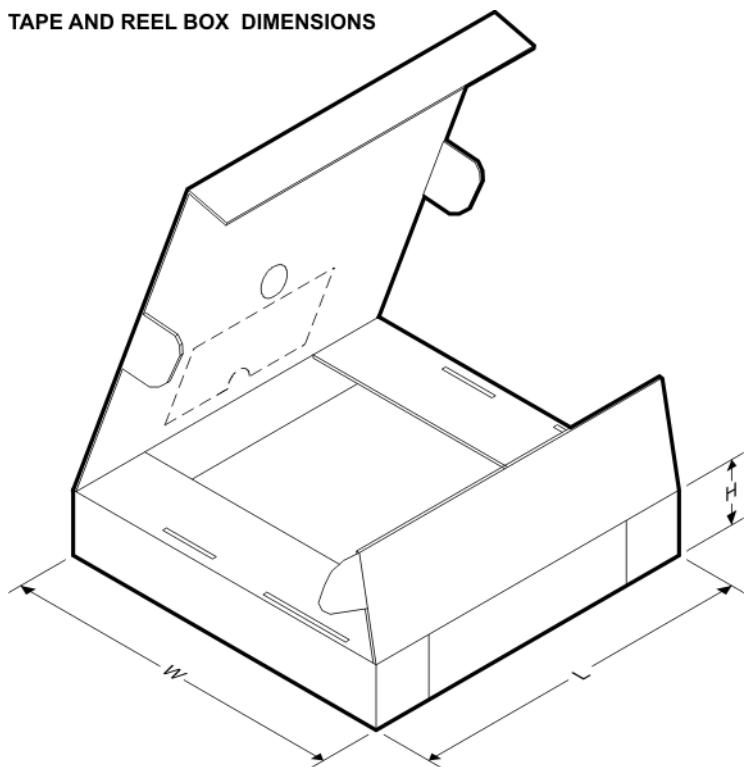
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4001BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4001BMT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4001BNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4001BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4002BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4002BNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4002BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4025BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4025BMT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4025BNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


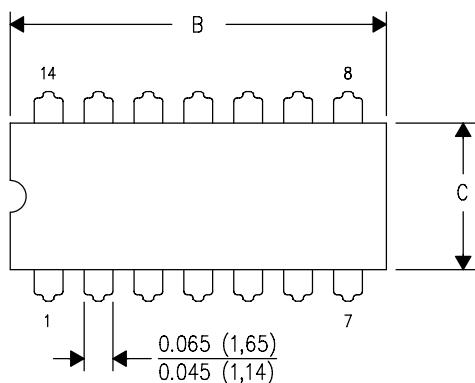
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4001BM96	SOIC	D	14	2500	367.0	367.0	38.0
CD4001BMT	SOIC	D	14	250	367.0	367.0	38.0
CD4001BNSR	SO	NS	14	2000	367.0	367.0	38.0
CD4001BPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
CD4002BM96	SOIC	D	14	2500	367.0	367.0	38.0
CD4002BNSR	SO	NS	14	2000	367.0	367.0	38.0
CD4002BPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
CD4025BM96	SOIC	D	14	2500	367.0	367.0	38.0
CD4025BMT	SOIC	D	14	250	367.0	367.0	38.0
CD4025BNSR	SO	NS	14	2000	367.0	367.0	38.0

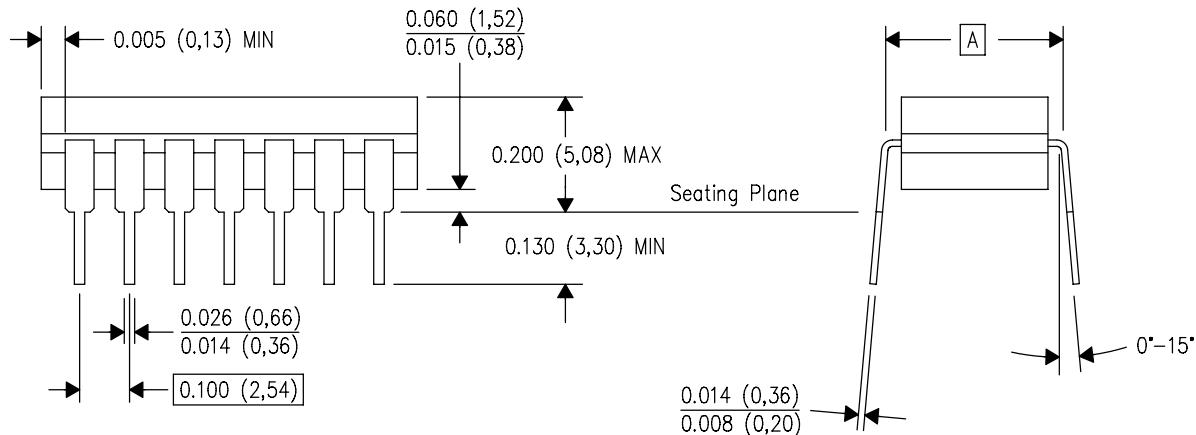
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS **\nDIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

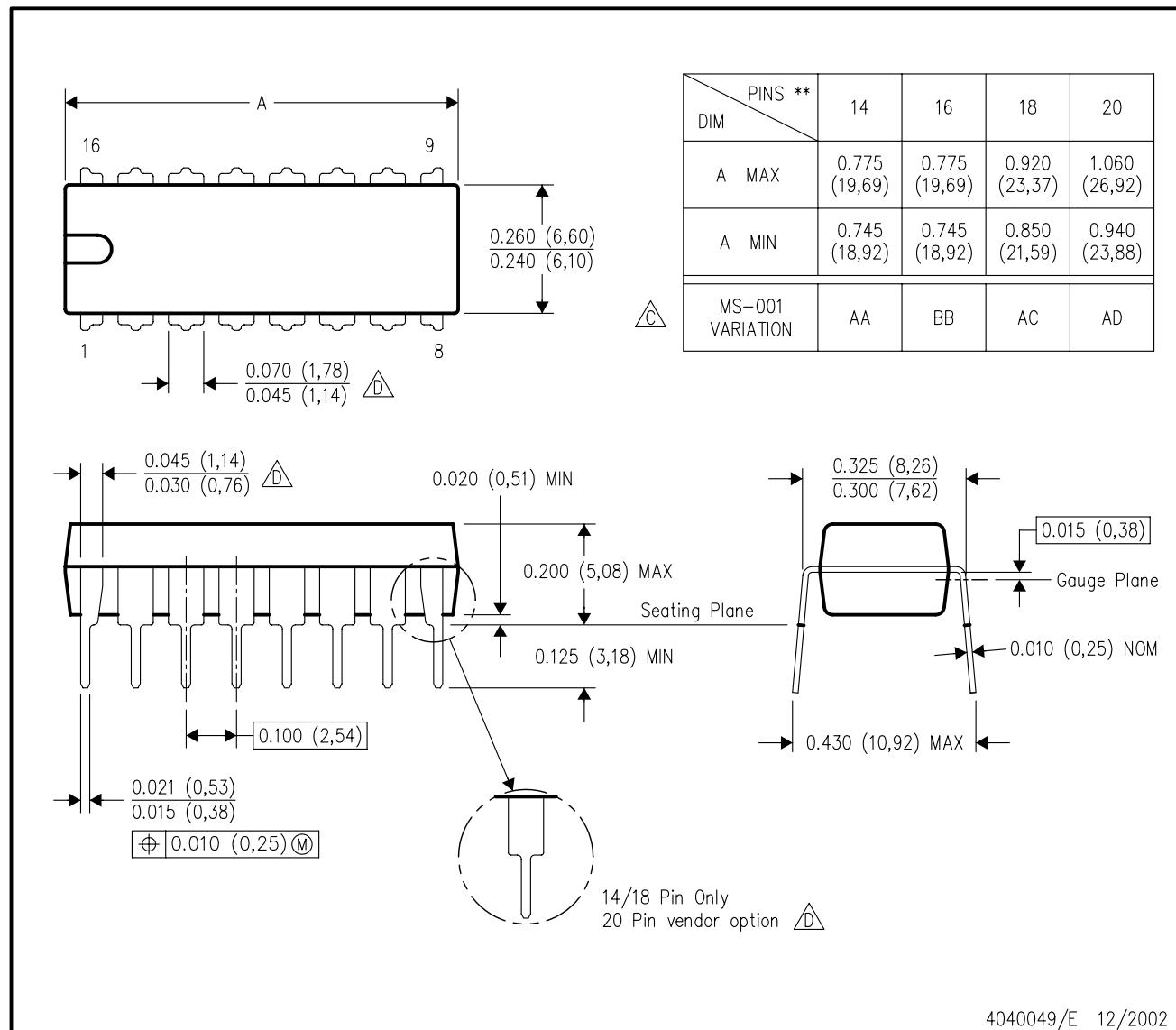
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MECHANICAL DATA

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

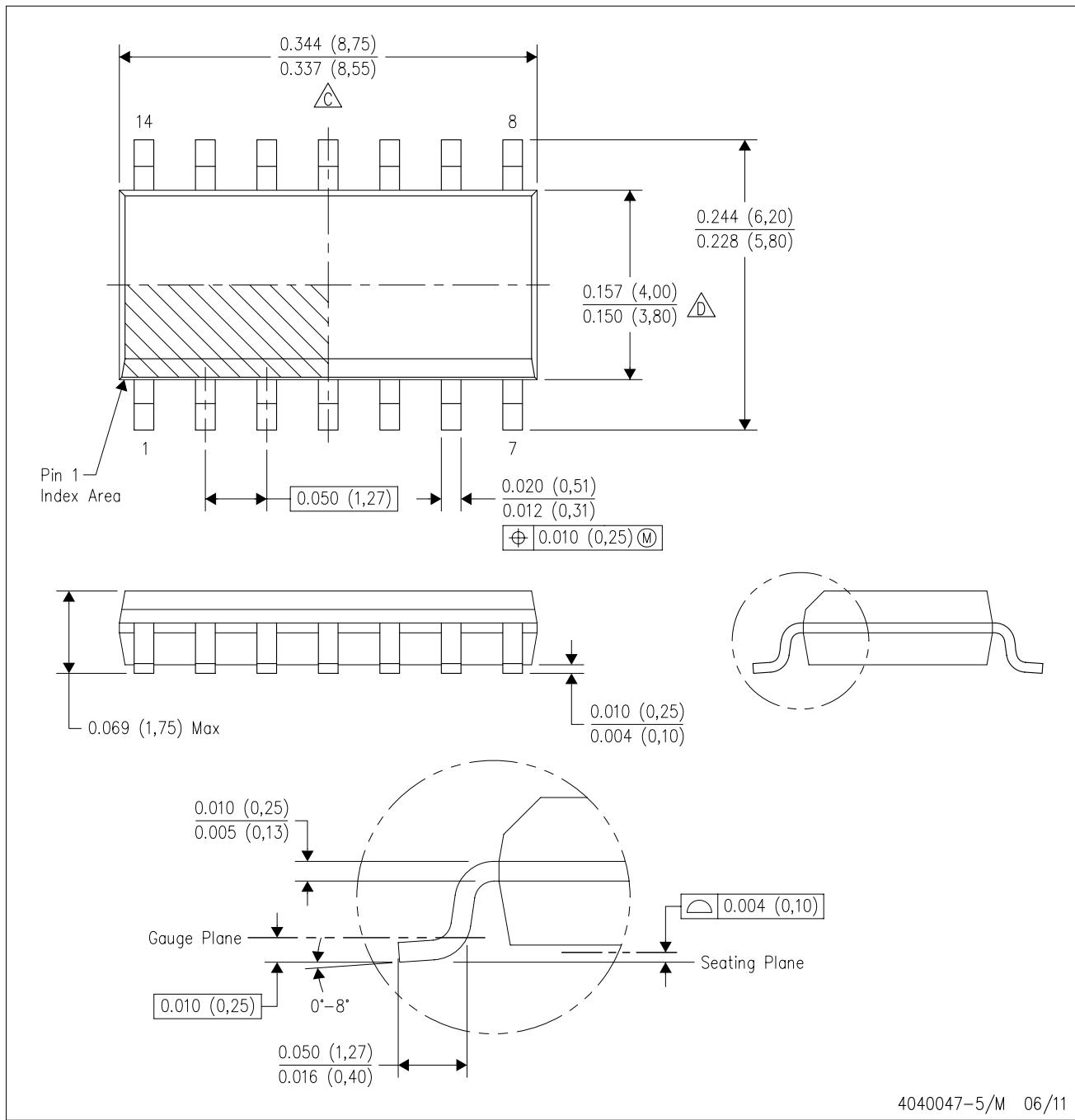
 Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

 The 20-pin end lead shoulder width is a vendor option – either half or full width.

 The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

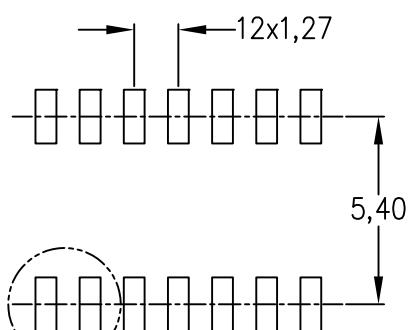
E. Reference JEDEC MS-012 variation AB.

LAND PATTERN DATA

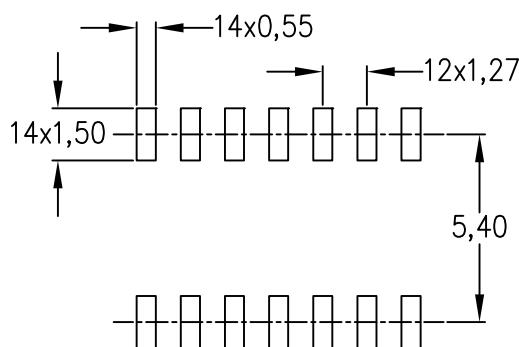
D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

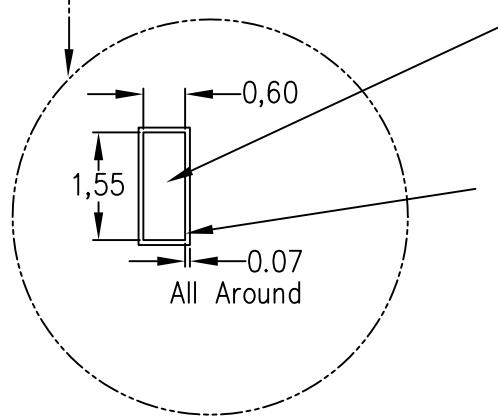
Example Board Layout
(Note C)



Stencil Openings
(Note D)



Example
Non Soldermask Defined Pad



Example
Pad Geometry
(See Note C)

Example
Solder Mask Opening
(See Note E)

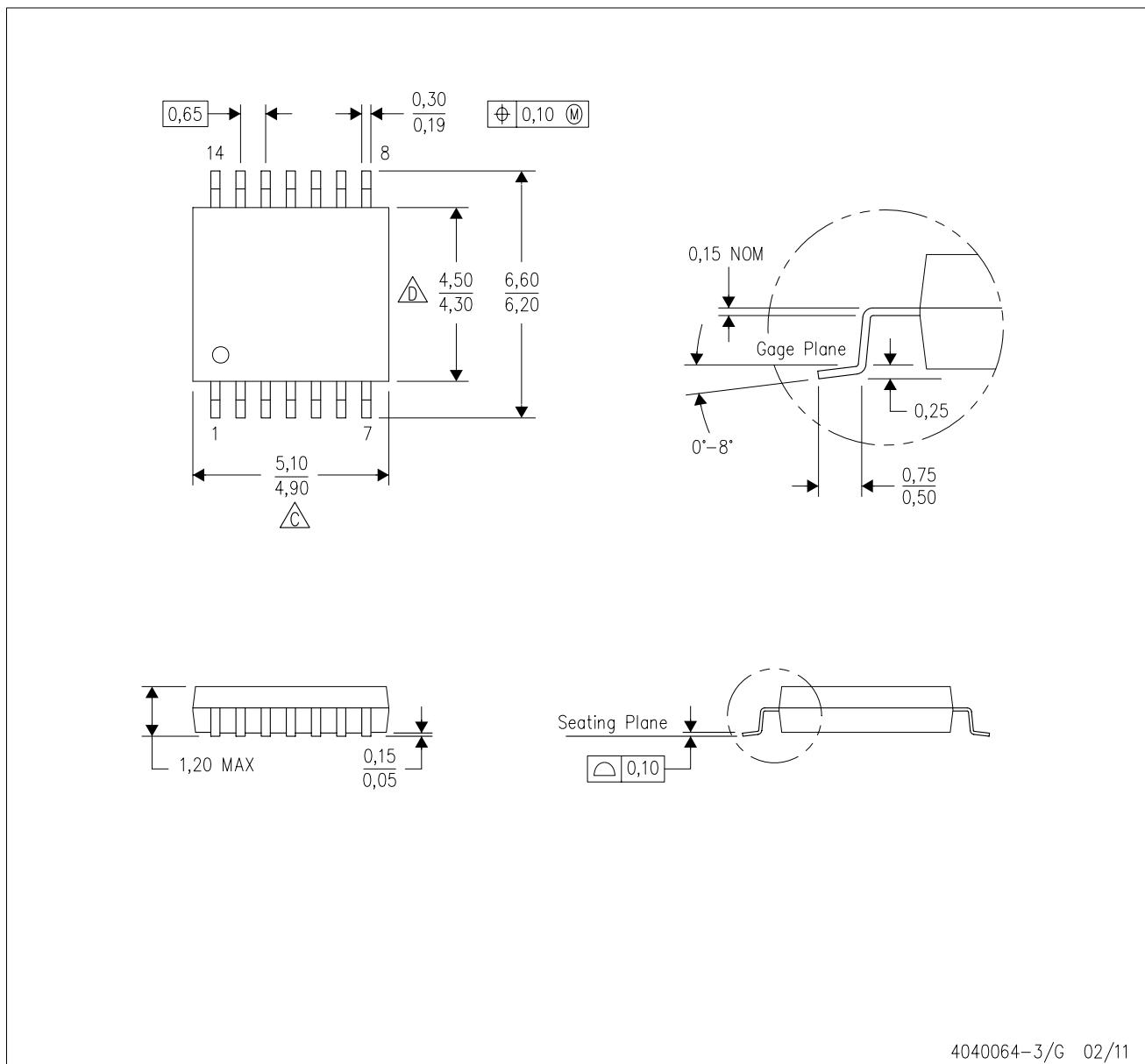
4211283-3/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

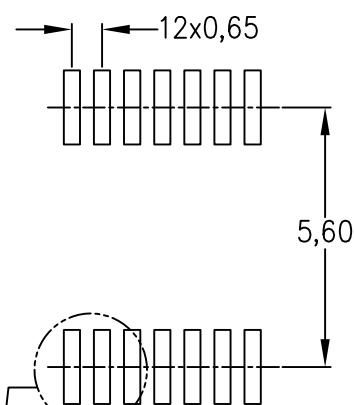
E. Falls within JEDEC MO-153

LAND PATTERN DATA

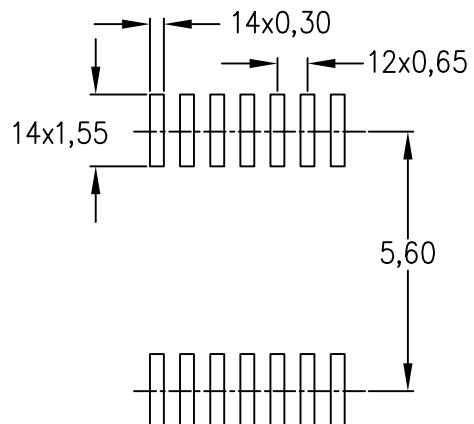
PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

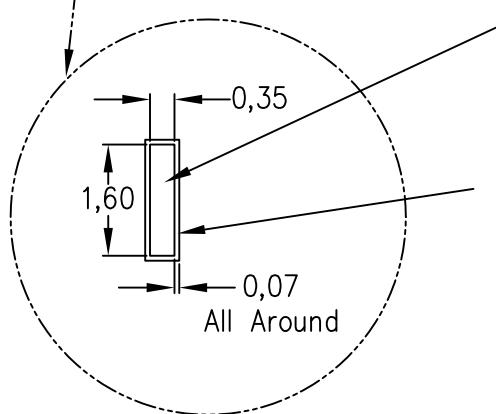
Example Board Layout
(Note C)



Stencil Openings
(Note D)



Example
Non Soldermask Defined Pad



Example
Pad Geometry
(See Note C)

Example
Solder Mask Opening
(See Note E)

4211284-2/G 08/15

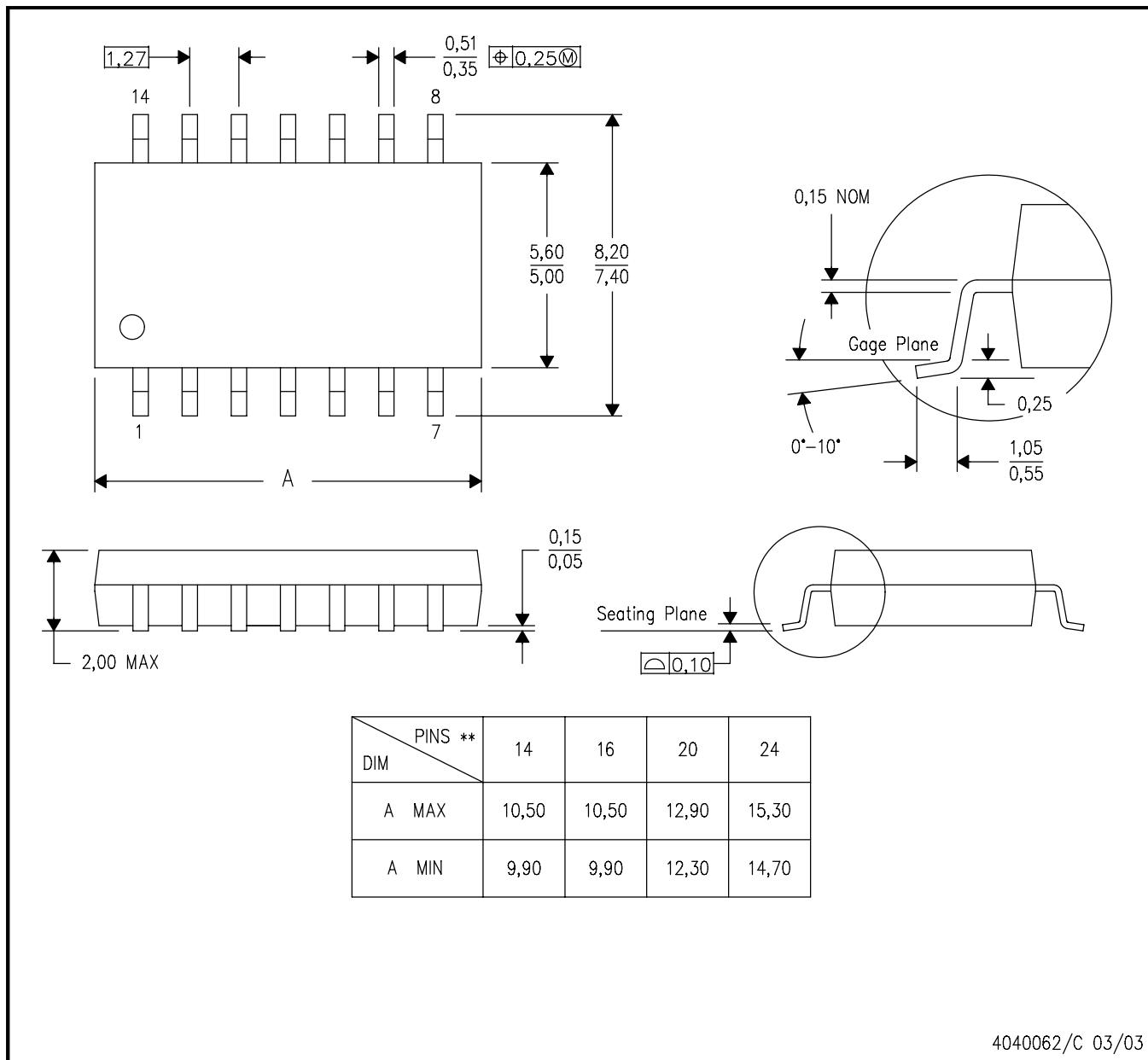
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)**

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products	Applications		
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com	TI E2E Community	
OMAP Applications Processors	www.ti.com/omap	e2e.ti.com	
Wireless Connectivity	www.ti.com/wirelessconnectivity		