CHAPTER 6 - CMOS OPERATIONAL AMPLIFIERS

Chapter Outline

Goal

Understand the analysis, design, and measurement of simple CMOS op amps

Design Hierarchy

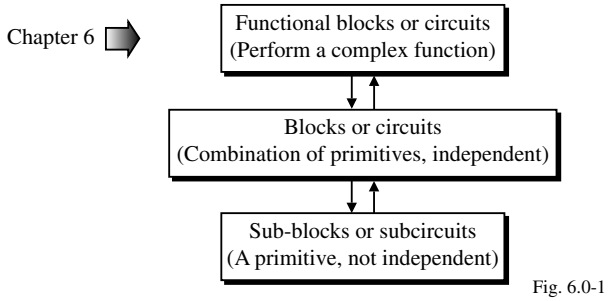


Fig. 6.0-1

The op amps of this chapter are unbuffered and are OTAs but we will use the generic term “op amp”.

SECTION 6.1 - DESIGN OF CMOS OPERATIONAL AMPLIFIERS

High-Level Viewpoint of an Op Amp

Block diagram of a general, two-stage op amp:

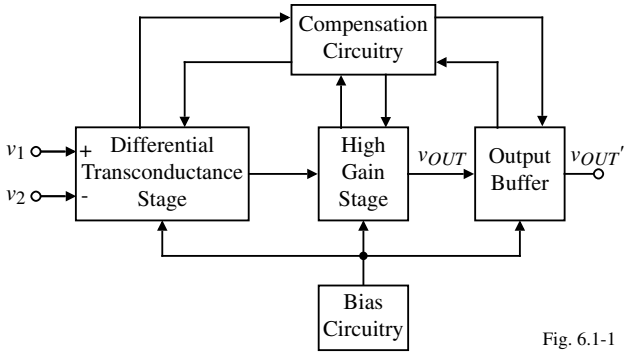


Fig. 6.1-1

- Differential transconductance stage:

  Forms the input and sometimes provides the differential-to-single ended conversion.
- High gain stage:

  Provides the voltage gain required by the op amp together with the input stage.
- Output buffer:

  Used if the op amp must drive a low resistance.
- Compensation:

  Necessary to keep the op amp stable when resistive negative feedback is applied.

Ideal Op Amp

Symbol:

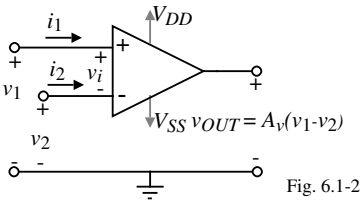


Fig. 6.1-2

Null port:

If the differential gain of the op amp is large enough then input terminal pair becomes a null port.

A null port is a pair of terminals where the voltage is zero and the current is zero.

I.e.,

$v_1 - v_2 = v_i = 0$

and

$i_1 = 0$ and $i_2 = 0$

Therefore, ideal op amps can be analyzed by assuming the differential input voltage is zero and that no current flows into or out of the differential inputs.

General Configuration of the Op Amp as a Voltage Amplifier

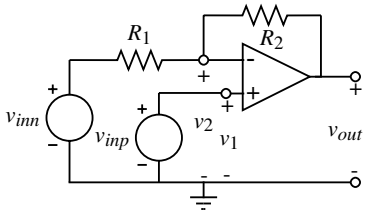


Fig. 6.1-3

Noninverting voltage amplifier:

$$v_{inn} = 0 \quad \Rightarrow \quad v_{out} = \left(\frac{R_1+R_2}{R_1}\right) v_{inp}$$

Inverting voltage amplifier:

$$v_{inp} = 0 \quad \Rightarrow \quad v_{out} = -\left(\frac{R_2}{R_1}\right) v_{inn}$$

Example 6.1-1 - Simplified Analysis of an Op Amp Circuit

The circuit shown below is an inverting voltage amplifier using an op amp. Find the voltage transfer function, v_{out}/v_{in}.

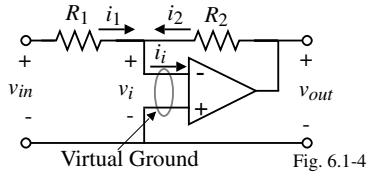


Fig. 6.1-4

Solution

If the differential voltage gain, A_v, is large enough, then the negative feedback path through R_2 will cause the voltage v_i and the current i_i shown on Fig. 6.1-4 to both be zero. Note that the null port becomes the familiar *virtual ground* if one of the op amp input terminals is on ground. If this is the case, then we can write that

$$i_1 = \frac{v_{in}}{R_1}$$

and

$$i_2 = \frac{v_{out}}{R_2}$$

Since, $i_i = 0$, then $i_1 + i_2 = 0$ giving the desired result as

$$\frac{v_{out}}{v_{in}} = -\frac{R_2}{R_1}.$$

Linear and Static Characterization of the Op Amp

A model for a nonideal op amp that includes some of the linear, static nonidealities:

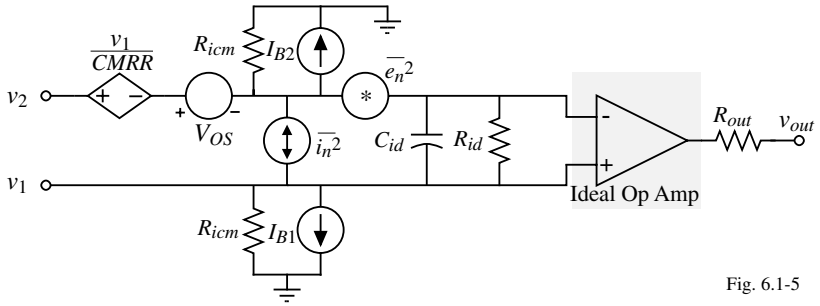


Fig. 6.1-5

where

R_{id} = differential input resistance

C_{id} = differential input capacitance

R_{icm} = common mode input resistance

V_{OS} = input-offset voltage

I_{B1} and I_{B2} = differential input-bias currents

I_{OS} = input-offset current ($I_{OS} = I_{B1}$-I_{B2})

CMRR = common-mode rejection ratio

$\overline{e}_n^2$ = voltage-noise spectral density (mean-square volts/Hertz)

$\overline{i}_n^2$ = current-noise spectral density (mean-square amps/Hertz)

Linear and Dynamic Characteristics of the Op Amp

Differential and common-mode frequency response:

$$V_{out}(s) = A_v(s)[V_1(s) - V_2(s)] \pm A_c(s)\left(\frac{V_1(s)+V_2(s)}{2}\right)$$

Differential-frequency response:

$$A_v(s) = \frac{A_{v0}}{\left(\frac{s}{p_1} - 1\right)\left(\frac{s}{p_2} - 1\right)\left(\frac{s}{p_3} - 1\right)\cdots}$$

where $p_1, p_2, p_3, \cdots$ are the poles of the differential-frequency response.

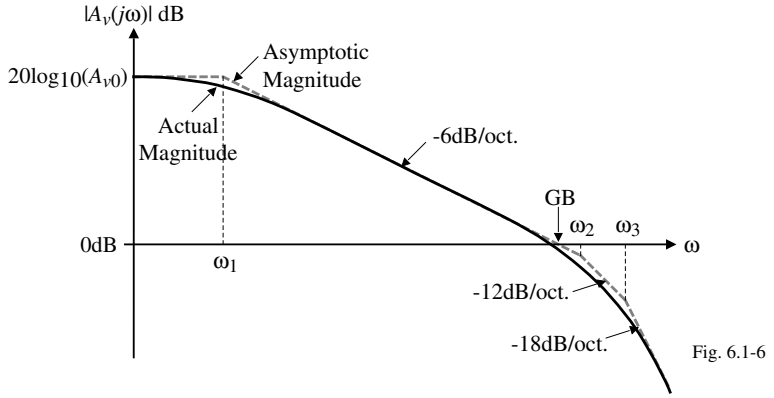


Fig. 6.1-6

Other Characteristics of the Op Amp

Power supply rejection ratio (*PSRR*):

$$PSRR = \frac{\Delta V_{DD}}{\Delta V_{\text{OUT}}} A_v(s) = \frac{V_o/V_{\text{in}}\ (V_{dd} = 0)}{V_o/V_{dd}\ (V_{\text{in}} = 0)}$$

Input common mode range (*ICMR*):

ICMR = the voltage range over which the input common-mode signal can vary without influence the differential performance

Slew rate (*SR*):

SR = output voltage rate limit of the op amp

Settling time (T_s):

T_s = time needed for the output of the op amp to reach a final value to with a predetermined tolerance when excited by a small signal. (SR is large signal excitation)

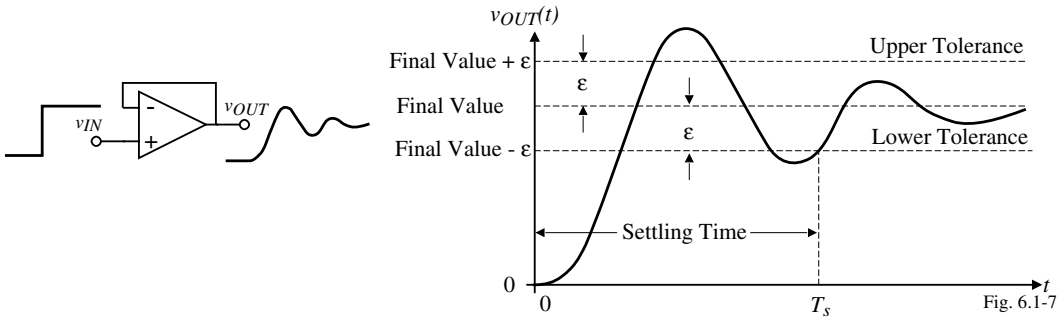


Fig. 6.1-7

Classification of CMOS Op Amps

Categorization of op amps:

Conversion	Hierarchy
Voltage to Current	Classic Differential Amplifier; Modified Differential Amplifier
Current to Voltage	Differential-to-single ended Load (Current Mirror); Source/Sink Current Loads; MOS Diode Load
Voltage to Current	Transconductance Grounded Gate; Transconductance Grounded Source
Current to Voltage	Class A (Source or Sink Load); Class B (Push-Pull)

First Voltage Stage; Current Stage; Second Voltage Stage

Table 6.1-1

Two-Stage CMOS Op Amp

Classical two-stage CMOS op amp broken into voltage-to-current and current-to-voltage stages:

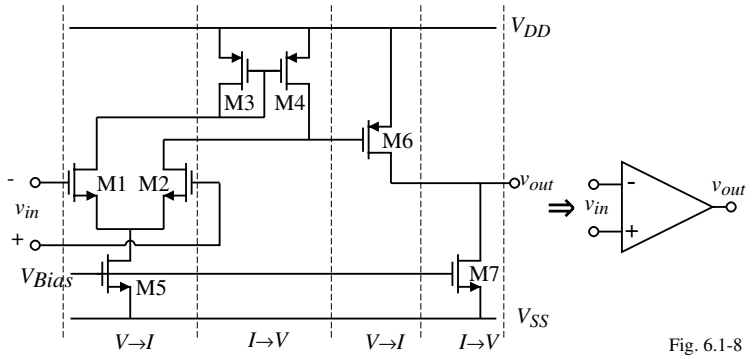


Fig. 6.1-8

Folded Cascode CMOS Op Amp

Folded cascode CMOS op amp broken into stages.

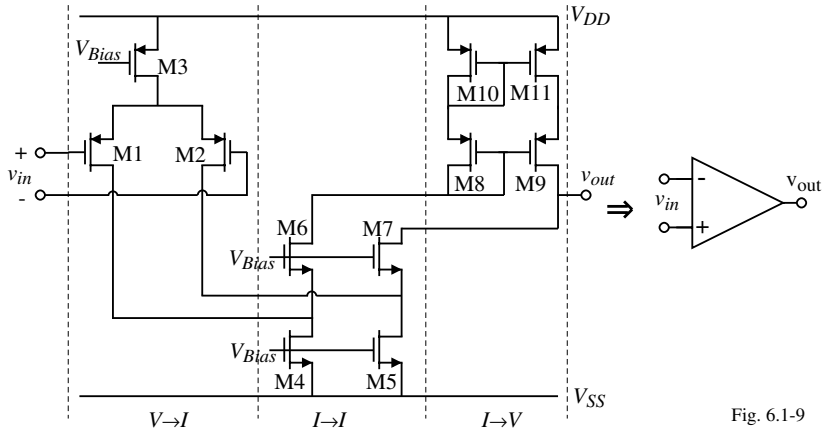


Fig. 6.1-9

Design of CMOS Op Amps

Steps:

1.) Choosing or creating the basic structure of the op amp.

This step generally is defined by a schematic showing the various transistors and their interconnections.

Generally this diagram does not change throughout the remaining portion of the design unless the specifications cannot be met and then a new or modified structure must be developed.

2.) Selection of the dc currents and transistor sizes.

Most of the effort of design is in this category.

Simulators are used to aid the designer in this phase (it is important that the design NOT use the simulator to do design). The general performance of the circuit should be known a priori.

3.) Physical implementation of the design.

Layout of the transistors

Floorplanning the connections, pin-outs, power supply buses and grounds

Extraction of the physical parasitics and resimulation

Verification that the layout is a physical representation of the circuit.

4.) Fabrication

Done by others (take a vacation)

5.) Measurement

Verification of the specifications

Modification of the design as necessary

Boundary Conditions and Requirements for CMOS Op Amps

Boundary conditions:

1. Process specification (V_T, K', C_{ox}, etc.)
2. Supply voltage and range
3. Supply current and range
4. Operating temperature and range

Requirements:

1. Gain
2. Gain bandwidth
3. Settling time
4. Slew rate
5. Common-mode input range, *ICMR*
6. Common-mode rejection ratio, *CMRR*
7. Power-supply rejection ratio, *PSRR*
8. Output-voltage swing
9. Output resistance
10. Offset
11. Noise
12. Layout area

Specifications for a Typical Unbuffered CMOS Op Amp

Boundary Conditions	Requirement
Process Specification	See Tables 3.1-1 and 3.1-2
Supply Voltage	±2.5 V ±10%
Supply Current	100 μA
Temperature Range	0 to 70°C
Specifications	
Gain	≥ 70 dB
Gainbandwidth	≥ 5 MHz
Settling Time	≤ 1 μsec
Slew Rate	≥ 5 V/μsec
Input *CMR*	≥ ±1.5 V
CMRR	≥ 60 dB
PSRR	≥ 60 dB
Output Swing	≥ ±1.5 V
Output Resistance	N/A, capacitive load only
Offset	≤ ±10 mV
Noise	≤ 100nV/$\sqrt{\text{Hz}}$ at 1KHz
Layout Area	≤ 10,000 min. channel length^2

Some Practical Thoughts on Op Amp Design

1.) Decide upon a suitable topology.
- Experience is a great help
- The topology should be the one capable of meeting most of the specifications
- Try to avoid "inventing" a new topology but start with an existing topology

2.) Determine the type of compensation needed to meet the specifications.
- Consider the load and stability requirements
- Use some form of Miller compensation or a self-compensated approach (shown later)

3.) Design device sizes for proper dc, ac, and transient performance.
- This begins with hand calculations based upon approximate design equations.
- Compensation components are also sized in this step of the procedure.
- After each device is sized by hand, a circuit simulator is used to fine tune the design.[†]

Two basic steps of design:

1.) "First-cut" - this step is to use hand calculations to propose a design that has potential of satisfying the specifications. Design robustness is developed in this step.

2.) Optimization - this step uses the computer to refine and optimize the design.

[†] A useful rule in analog design is: (Use of a simulator)x(Common sense) = Constant. Do not use a simulator for design but for optimization.

SECTION 6.2 - COMPENSATION OF OP AMPS

Compensation

Objective

Objective of compensation is to achieve stable operation when negative feedback is applied around the op amp.

Types of Compensation

1. Miller - Use of a capacitor feeding back around a high-gain, inverting stage.
   - Miller capacitor only
   - Miller capacitor with an unity-gain buffer to block the forward path through the compensation capacitor. Can eliminate the RHP zero.
   - Miller with a nulling resistor. Similar to Miller but with an added series resistance to gain control over the RHP zero.
2. Self compensating - Load capacitor compensates the op amp (later).
3. Feedforward - Bypassing a positive gain amplifier resulting in phase lead. Gain can be less than unity.

Single-Loop, Negative Feedback Systems

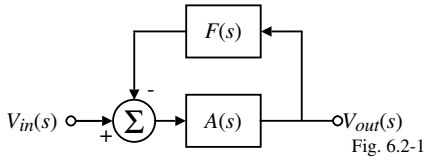


Fig. 6.2-1

$A(s)$ = amplifier gain (normally the differential-mode voltage gain of the op amp)

$F(s)$ = transfer function of the external feedback from the output of the op amp back to the input.

Definitions:

- Open-loop gain = $L(s) = -A(s)F(s)$
- Closed-loop gain = $\frac{V_{out}(s)}{V_{in}(s)} = \frac{A(s)}{1+A(s)F(s)}$

Stability Requirements:

The requirements for stability for a single-loop, negative feedback system is,

$$|A(j\omega_{0^\circ})F(j\omega_{0^\circ})| = |L(j\omega_{0^\circ})| < 1$$

where ω_{0° is defined as

$$\text{Arg}[-A(j\omega_{0^\circ})F(j\omega_{0^\circ})] = \text{Arg}[L(j\omega_{0^\circ})] = 0^\circ$$

Another convenient way to express this requirement is

$$\text{Arg}[-A(j\omega_{0dB})F(j\omega_{0dB})] = \text{Arg}[L(j\omega_{0dB})] > 0^\circ$$

where ω_{0dB} is defined as

$$|A(j\omega_{0dB})F(j\omega_{0dB})| = |L(j\omega_{0dB})| = 1$$

Illustration of the Stability Requirement using Bode Plots

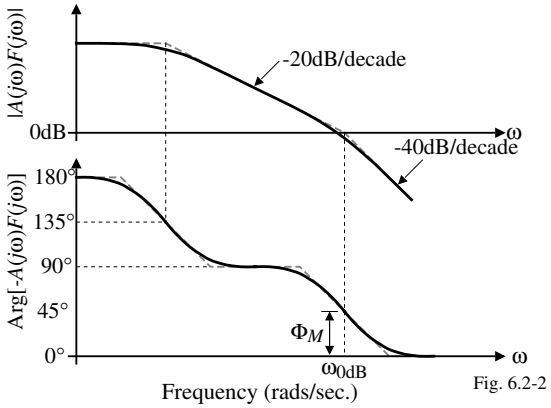


Fig. 6.2-2

A measure of stability is given by the phase when $|A(j\omega)F(j\omega)| = 1$. This phase is called *phase margin*.

$$\text{Phase margin} = \Phi_M = \text{Arg}[-A(j\omega_{0dB})F(j\omega_{0dB})] = \text{Arg}[L(j\omega_{0dB})]$$

Why Do We Want Good Stability?

Consider the step response of second-order system which closely models the closed-loop gain of the op amp.

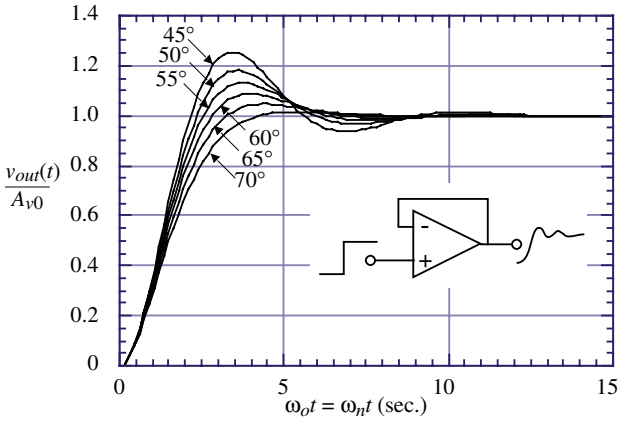


Fig. 6.2-3

A "good" step response is one that quickly reaches its final value.

Therefore, we see that phase margin should be at least 45° and preferably 60° or larger.

(A good rule of thumb for satisfactory stability is that there should be less than three rings.)

Note that good stability is not necessarily the quickest risetime.

The Frequency Response of the Two-Stage Op Amp

Without any compensation, the two-stage op amp can be modeled as shown below.

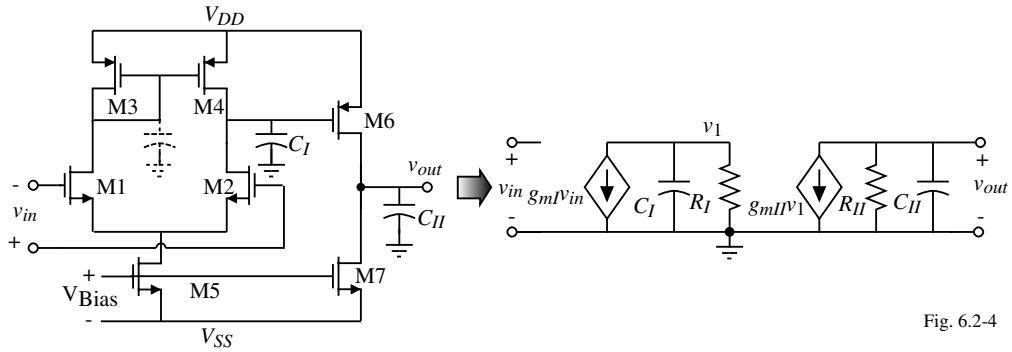


Fig. 6.2-4

The locations for the two poles are given by the following equations

$$p'_1 = \frac{-1}{R_I C_I}$$

and

$$p'_2 = \frac{-1}{R_{II} C_{II}}$$

where R_I (R_{II}) is the resistance to ground seen from the output of the first (second) stage and C_I (C_{II}) is the capacitance to ground seen from the output of the first (second) stage.

Frequency Response of the Op Amp

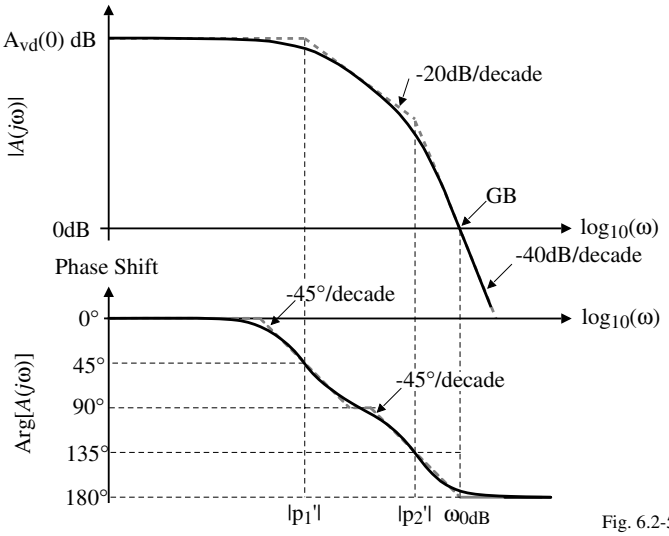


Fig. 6.2-5

Note that the op amp experiences 180° phase shift which will cause poor phase margin in a negative feedback application.

Loop Gain of an Uncompensated Op Amp with Negative Feedback of $F(s) = 1$ [$L(s) = -A(s)$]

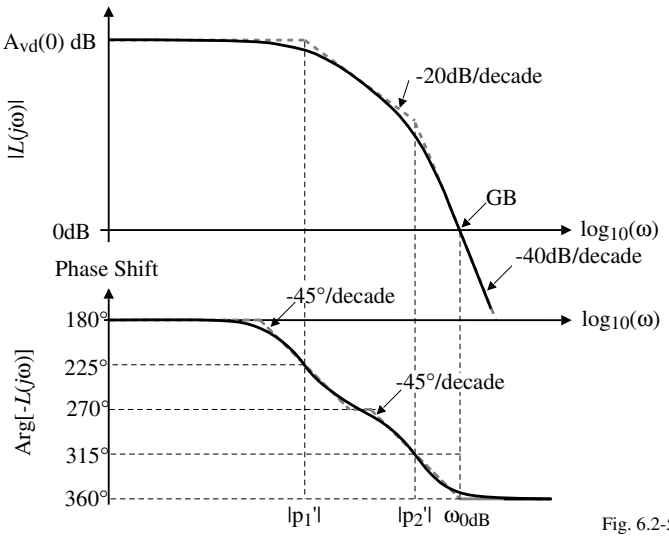


Fig. 6.2-5

Note that the phase margin is much less than 45°.

Therefore, the op amp must be compensated before using it in a closed-loop configuration.

Miller Compensation of the Two-Stage Op Amp

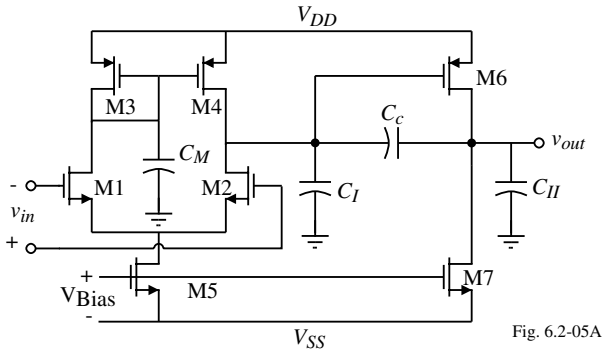


Fig. 6.2-05A

The various capacitors are:

C_c = accomplishes the Miller compensation

C_M = capacitance associated with the first-stage mirror (mirror pole)

C_I = output capacitance to ground of the first-stage

C_{II} = output capacitance to ground of the second-stage

Simplification of the Two-Stage, Small-Signal Frequency Response Model

1.) Assume that $g_{m3} >> g_{ds3} + g_{ds1}$.

2.) Assume that $\frac{g_{m3}}{C_M} >> GB$

Therefore,

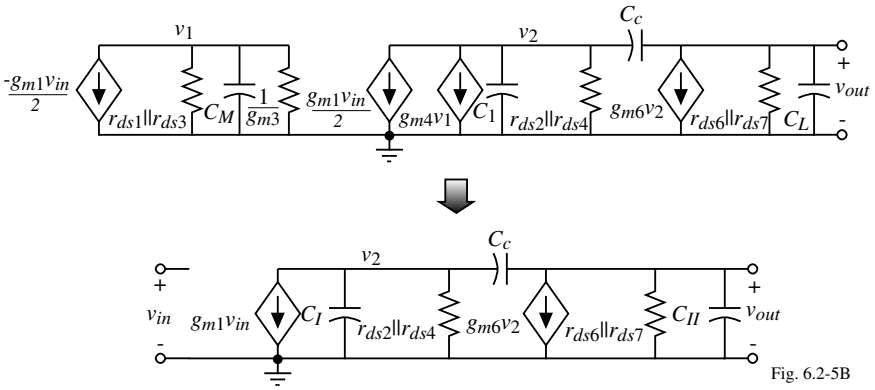


Fig. 6.2-5B

General Two-Stage Frequency Response Analysis

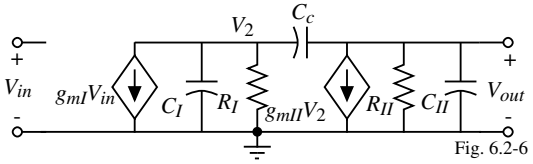


Fig. 6.2-6

where

$g_{mI} = g_{m1} = g_{m2}$, $R_I = r_{ds2}||r_{ds4}$, $C_I = C_1$

and

$g_{mII} = g_{m6}$, $R_{II} = r_{ds6}||r_{ds7}$, $C_{II} = C_2 = C_L$

Nodal Equations:

$$-g_{mI}V_{in} = [G_I + s(C_I + C_c)]V_2 - [sC_c]V_{out} \quad \text{and} \quad 0 = [g_{mII} - sC_c]V_2 + [G_{II} + sC_{II} + sC_c]V_{out}$$

Solving using Cramer's rule gives,

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{g_{mI}(g_{mII} - sC_c)}{G_IG_{II} + s[G_{II}(C_I+C_{II}) + G_I(C_{II}+C_c) + g_{mII}C_c] + s^2[C_IC_{II} + C_cC_I + C_cC_{II}]}$$

$$= \frac{A_o[1 - s(C_c/g_{mII})]}{1 + s[R_I(C_I+C_{II}) + R_{II}(C_2+C_c) + g_{mII}R_IR_{II}C_c] + s^2[R_IR_{II}(C_IC_{II} + C_cC_I + C_cC_{II})]}$$

where, $A_o = g_{mI}g_{mII}R_IR_{II}$

In general, $D(s) = \left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right) = 1 - s\left(\frac{1}{p_1} + \frac{1}{p_2}\right) + \frac{s^2}{p_1p_2} \rightarrow D(s) \approx 1 - \frac{s}{p_1} + \frac{s^2}{p_1p_2}$, if $|p_2| >> |p_1|$

$\therefore$ $\boxed{p_1 = \frac{-1}{R_I(C_I+C_{II}) + R_{II}(C_{II}+C_c) + g_{mII}R_IR_{II}C_c} \approx \frac{-1}{g_{mII}R_IR_{II}C_c}}$, $\boxed{z = \frac{g_{mII}}{C_c}}$

$\boxed{p_2 = \frac{-[R_I(C_I+C_{II}) + R_{II}(C_{II}+C_c) + g_{mII}R_IR_{II}C_c]}{R_IR_{II}(C_IC_{II} + C_cC_I + C_cC_{II})} \approx \frac{-g_{mII}C_c}{C_IC_{II} + C_cC_I + C_cC_{II}} \approx \frac{-g_{mII}}{C_{II}}}$ where $C_{II} > C_c > C_I$.

Summary of Results for Miller Compensation of the Two-Stage Op Amp

There are three roots of importance:

1.) Right-half plane zero:

$$z = \frac{g_{mII}}{C_c} = \frac{g_{m6}}{C_c}$$

This root is very undesirable because it boosts the loop magnitude while decreasing the phase.

2.) Dominant left-half plane pole (the Miller pole):

$$p_1 \approx \frac{-1}{g_{mII}R_IR_{II}C_c} = \frac{-(g_{ds2}+g_{ds4})(g_{ds6}+g_{ds7})}{g_{m6}C_c}$$

This root accomplishes the desired compensation.

3.) Left-half plane output pole:

$$p_2 \approx \frac{-g_{mII}}{C_{II}} \approx \frac{-g_{m6}}{C_L}$$

This pole must be beyond the unity-gainbandwidth or the phase margin will not be satisfied.

Root locus plot of the Miller compensation:

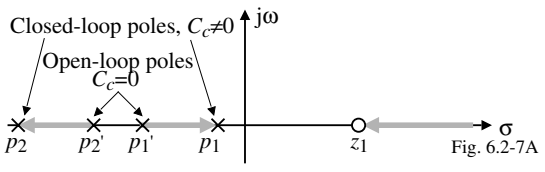


Fig. 6.2-7A

Compensated Open-Loop Frequency Response of the Two-Stage Op Amp

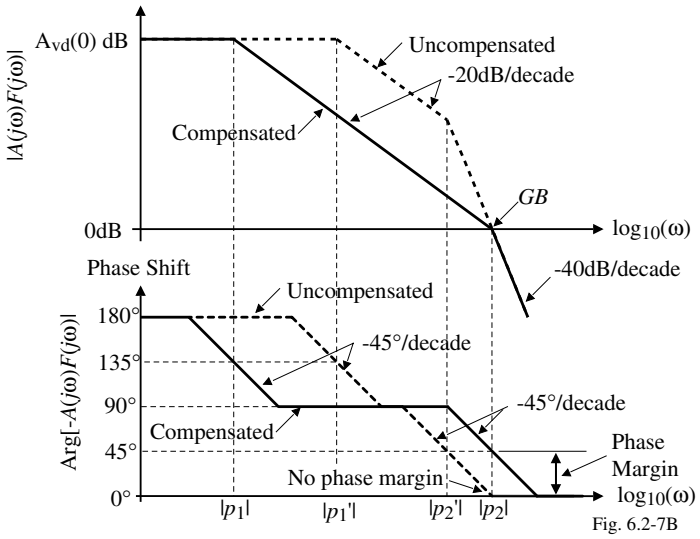


Fig. 6.2-7B

Note that the unity-gainbandwidth, *GB*, is

$$GB = A_{vd}(0)\cdot|p_1| = (g_{mI}g_{mII}R_IR_{II})\frac{1}{g_{mII}R_IR_{II}C_c} = \frac{g_{mI}}{C_c} = \frac{g_{m1}}{C_c} = \frac{g_{m2}}{C_c}$$

Conceptually, where do these roots come from?

1.) The Miller pole:

$$|p_1| \approx \frac{1}{R_I(g_{m6}R_{II}C_c)}$$

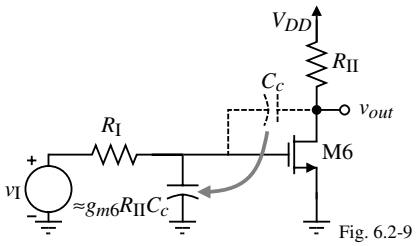


Fig. 6.2-9

2.) The left-half plane output pole:

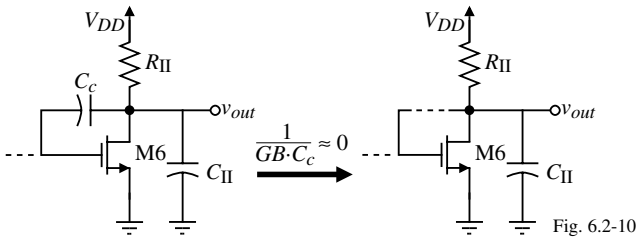


Fig. 6.2-10

$$|p_2| \approx \frac{g_{m6}}{C_{II}}$$

3.) Right-half plane zero (*Zeros always arise from multiple paths from the input to output*):

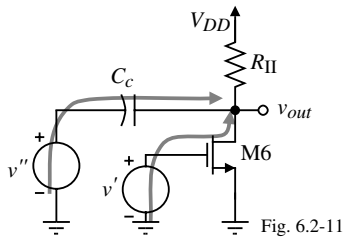


Fig. 6.2-11

$$v_{out} = \left(\frac{-g_{m6}R_{II}(1/sC_c)}{R_{II}+1/sC_c}\right)v' + \left(\frac{R_{II}}{R_{II}+1/sC_c}\right)v'' = \frac{-R_{II}\left(\frac{g_{m6}}{sC_c}-1\right)}{D(s)}v$$

where $v = v' = v''$.

Influence of the Mirror Pole

Up to this point, we have neglected the influence of the pole, p_3, associated with the current mirror of the input stage. If $|p_2| \approx |p_3|$, we have problems in compensation. This pole is given approximately as

$$p_3 \approx \frac{-g_{m3}}{C_M}$$

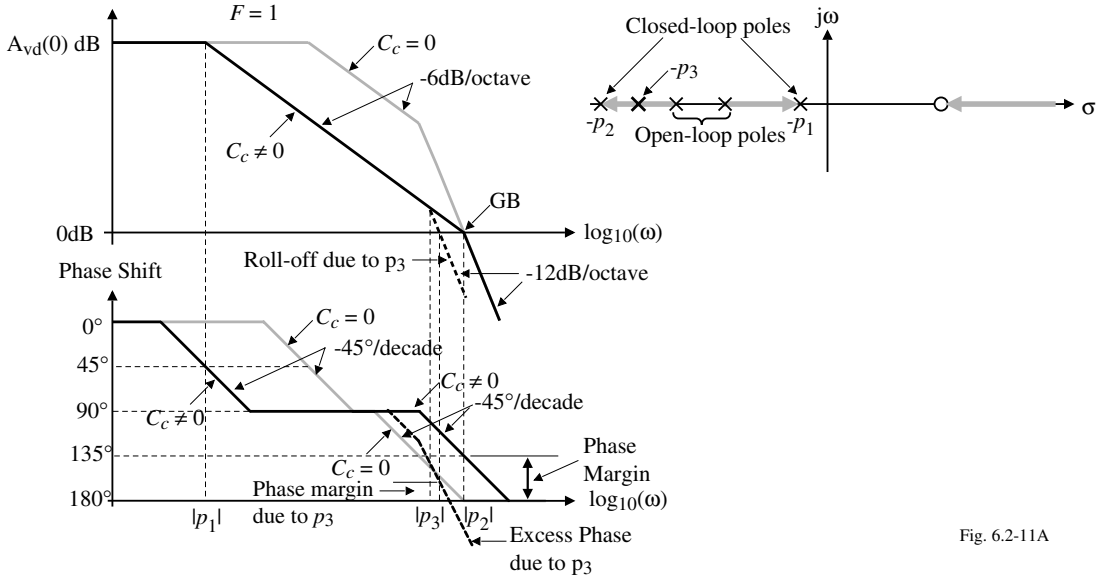


Fig. 6.2-11A

Summary of the Conditions for Stability of the Two-Stage Op Amp

• Unity-gainbandwith is given as:

$$GB = A_v(0)\cdot|p_1| = (g_{mI}g_{mII}R_IR_{II})\cdot\left(\frac{1}{g_{mII}R_IR_{II}C_c}\right) = \frac{g_{mI}}{C_c} = (g_{m1}g_{m2}R_1R_2)\cdot\left(\frac{1}{g_{m2}R_1R_2C_c}\right) = \frac{g_{m1}}{C_c}$$

• The requirement for 45° phase margin is:

$$\pm 180° - \text{Arg}[AF] = \pm 180° - \tan^{-1}\left(\frac{\omega}{|p_1|}\right) - \tan^{-1}\left(\frac{\omega}{|p_2|}\right) - \tan^{-1}\left(\frac{\omega}{z}\right) = 45°$$

Let $\omega = GB$ and assume that $z \geq 10GB$, therefore we get,

$$\pm 180° - \tan^{-1}\left(\frac{GB}{|p_1|}\right) - \tan^{-1}\left(\frac{GB}{|p_2|}\right) - \tan^{-1}\left(\frac{GB}{z}\right) = 45°$$

$$135° \approx \tan^{-1}(A_v(0)) + \tan^{-1}\left(\frac{GB}{|p_2|}\right) + \tan^{-1}(0.1) = 90° + \tan^{-1}\left(\frac{GB}{|p_2|}\right) + 5.7°$$

$$39.3° \approx \tan^{-1}\left(\frac{GB}{|p_2|}\right) \Rightarrow \frac{GB}{|p_2|} = 0.818 \Rightarrow \boxed{|p_2| \geq 1.22GB}$$

• The requirement for 60° phase margin:

$$\boxed{|p_2| \geq 2.2GB \text{ if } z \geq 10GB}$$

• If 60° phase margin is required, then the following relationships apply:

$$\frac{g_{m6}}{C_c} > \frac{10g_{m1}}{C_c} \Rightarrow \boxed{g_{m6} > 10g_{m1}} \quad \text{and} \quad \frac{g_{m6}}{C_2} > \frac{2.2g_{m1}}{C_c} \Rightarrow \boxed{C_c > 0.22C_2}$$

Controlling the Right-Half Plane Zero

Why is the RHP zero a problem?

Because it boosts the magnitude but lags the phase - the worst possible combination for stability.

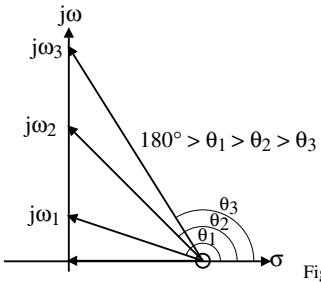


Fig. 6.2-11B

Solution of the problem:

If zeros are caused by two paths to the output, then eliminate one of the paths.

Use of Buffer to Eliminate the Feedforward Path through the Miller Capacitor

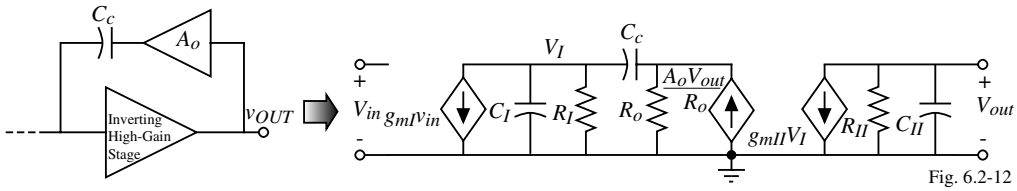


Fig. 6.2-12

If R_o of the buffer is zero, then the transfer function is given by the following equation,

$$\frac{V_o(s)}{V_{in}(s)} = \frac{(g_{mI})(g_{mII})(R_I)(R_{II})}{1 + s[R_IC_I + R_{II}C_{II} + R_IC_c + g_{mII}R_IR_{II}C_c] + s^2[R_IR_{II}C_{II}(C_I + C_c)]}$$

Using the technique as before to approximate p_1 and p_2 results in the following

$$p_1 \cong \frac{-1}{R_IC_I + R_{II}C_{II} + R_IC_c + g_{mII}R_IR_{II}C_c} \cong \frac{-1}{g_{mII}R_IR_{II}C_c}$$

and

$$p_2 \cong \frac{-g_{mII}C_c}{C_{II}(C_I + C_c)}$$

Comments:

Poles are approximately what they were before with the zero removed.

For 45° phase margin, $|p_2|$ must be greater than GB

For 60° phase margin, $|p_2|$ must be greater than $1.73GB$

Use of Buffer with Finite Output Resistance to Eliminate the RHP Zero

It can be shown that if the output resistance of the buffer amplifier, R_o, is not neglected that a third pole occurs at,

$$p_4 \cong \frac{-1}{R_o[C_IC_c/(C_I + C_c)]}$$

and a LHP zero at

$$z_2 \cong \frac{-1}{R_oC_c}$$

Closer examination shows that if a resistor, called a *nulling resistor*, is placed in series with C_c that the RHP zero can be eliminated or moved to the LHP.

Use of Nulling Resistor to Eliminate the RHP Zero (or turn it into a LHP zero)[†]

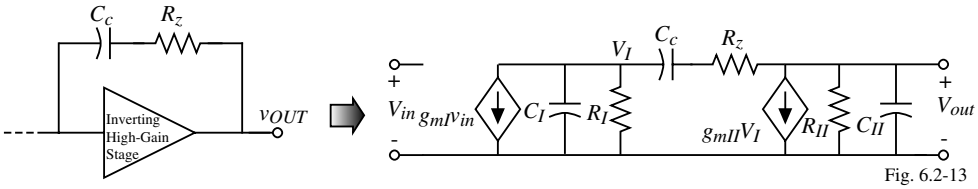


Fig. 6.2-13

Nodal equations:

$$g_{mI}V_{\text{in}} + \frac{V_I}{R_I} + sC_IV_I + \left(\frac{sC_c}{1 + sC_cR_z}\right)(V_I - V_{out}) = 0$$

$$g_{mII}V_I + \frac{V_o}{R_{II}} + sC_{II}V_{out} + \left(\frac{sC_c}{1 + sC_cR_z}\right)(V_{out} - V_I) = 0$$

Solution:

$$\frac{V_{out}(s)}{V_{\text{in}}(s)} = \frac{a\{1 - s[(C_c/g_{mII}) - R_zC_c]\}}{1 + bs + cs^2 + ds^3}$$

where

$$a = g_{mI}g_{mII}R_IR_{II}$$

$$b = (C_{II} + C_c)R_{II} + (C_I + C_c)R_I + g_{mII}R_IR_{II}C_c + R_zC_c$$

$$c = [R_IR_{II}(C_IC_{II} + C_cC_I + C_cC_{II}) + R_zC_c(R_IC_I + R_{II}C_{II})]$$

$$d = R_IR_{II}R_zC_IC_{II}C_c$$

[†] William J. Parrish, "An Ion Implanted CMOS Amplifier for High Performance Active Filters", Ph.D. Dissertation, 1976, Univ. of Calif., Santa Barbara, CA.

Use of Nulling Resistor to Eliminate the RHP - Continued

If R_z is assumed to be less than R_I or R_{II} and the poles widely spaced, then the roots of the above transfer function can be approximated as

$$p_1 \cong \frac{-1}{(1 + g_{mII}R_{II})R_IC_c} \cong \frac{-1}{g_{mII}R_{II}R_IC_c}$$

$$p_2 \cong \frac{-g_{mII}C_c}{C_IC_{II} + C_cC_I + C_cC_{II}} \cong \frac{-g_{mII}}{C_{II}}$$

$$p_4 = \frac{-1}{R_zC_I}$$

and

$$z_1 = \frac{1}{C_c(1/g_{mII} - R_z)}$$

Note that the zero can be placed anywhere on the real axis.

Conceptual Illustration of the Nulling Resistor Approach

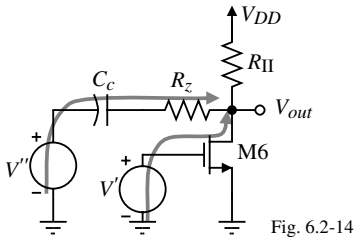


Fig. 6.2-14

The output voltage, V_{out}, can be written as

$$V_{out} = \frac{-g_{m6}R_{II}\left(R_z + \frac{1}{sC_c}\right)}{R_{II} + R_z + \frac{1}{sC_c}} V' + \frac{R_{II}}{R_{II} + R_z + \frac{1}{sC_c}} V'' = \frac{-R_{II}\left[g_{m6}R_z + \frac{g_{m6}}{sC_c} - 1\right]}{D(s)}$$

Setting the numerator equal to zero and assuming $g_{m6} = g_{mII}$ gives,

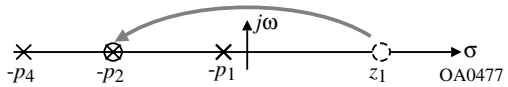
$$z_1 = \frac{1}{C_c(1/g_{mII} - R_z)}$$

A Design Procedure that Allows the RHP Zero to Cancel the Output Pole, p_2

We desire that $z_1 = p_2$ in terms of the previous notation.

Therefore,

$$\frac{1}{C_c(1/g_{mII} - R_z)} = \frac{-g_{mII}}{C_{II}}$$



The value of R_z can be found as

$$R_z = \left(\frac{C_c + C_{II}}{C_c}\right)(1/g_{mII})$$

With p_2 canceled, the remaining roots are p_1 and p_4(the pole due to R_z) . For unity-gain stability, all that is required is that

$$|p_4| > A_v(0)|p_1| = \frac{A_v(0)}{g_{mII}R_{II}R_IC_c} = \frac{g_{mI}}{C_c}$$

and

$$(1/R_zC_I) > (g_{mI}/C_c) = GB$$

Substituting R_z into the above inequality and assuming $C_{II} >> C_c$ results in

$$C_c > \sqrt{\frac{g_{mI}}{g_{mII}} C_IC_{II}}$$

This procedure gives excellent stability for a fixed value of C_{II} ($\approx C_L$).

Unfortunately, as C_L changes, p_2 changes and the zero must be readjusted to cancel p_2.

Increasing the Magnitude of the Output Pole[†]

The magnitude of the output pole , p_2, can be increased by introducing gain in the Miller capacitor feedback path. For example,

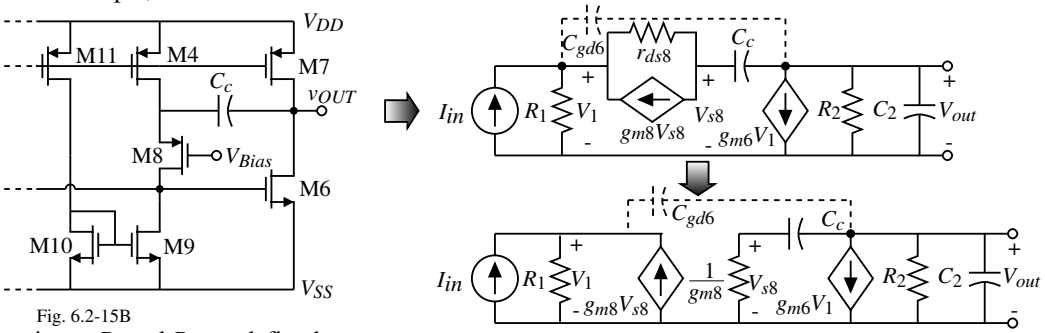


Fig. 6.2-15B

The resistors R_1 and R_2 are defined as

$$R_1 = \frac{1}{g_{ds2} + g_{ds4} + g_{ds9}} \quad \text{and} \quad R_2 = \frac{1}{g_{ds6} + g_{ds7}}$$

where transistors M2 and M4 are the output transistors of the first stage.

Nodal equations:

$$I_{in} = G_1V_1 - g_{m8}V_{s8} = G_1V_1 - \left(\frac{g_{m8}sC_c}{g_{m8} + sC_c}\right)V_{out} \quad \text{and} \quad 0 = g_{m6}V_1 + \left[G_2 + sC_2 + \frac{g_{m8}sC_c}{g_{m8} + sC_c}\right]V_{out}$$

[†] B.K. Ahuja, "An Improved Frequency Compensation Technique for CMOS Operational Amplifiers," *IEEE J. of Solid-State Circuits*, Vol. SC-18, No. 6 (Dec. 1983) pp. 629-633.

Increasing the Magnitude of the Output Pole - Continued

Solving for the transfer function V_{out}/I_{in} gives,

$$\frac{V_{out}}{I_{in}} = \left(\frac{-g_{m6}}{G_1G_2}\right)\left[\frac{\left(1+\frac{sC_c}{g_{m8}}\right)}{1+s\left[\frac{C_c}{g_{m8}}+\frac{C_2}{G_2}+\frac{C_c}{G_2}+\frac{g_{m6}C_c}{G_1G_2}\right]+s^2\left(\frac{C_cC_2}{g_{m8}G_2}\right)}\right]$$

Using the approximate method of solving for the roots of the denominator illustrated earlier gives

$$p_1 = \frac{-1}{\frac{C_c}{g_{m8}}+\frac{C_c}{G_2}+\frac{C_2}{G_2}+\frac{g_{m6}C_c}{G_1G_2}} \approx \frac{-6}{g_{m6}r_{ds}^2C_c}$$

and

$$p_2 \approx \frac{-\frac{g_{m6}r_{ds}^2C_c}{6}}{\frac{C_cC_2}{g_{m8}G_2}} = \frac{g_{m8}r_{ds}^2G_2}{6}\left(\frac{g_{m6}}{C_2}\right) = \left(\frac{g_{m8}r_{ds}}{3}\right)|p_2'|$$

where all the various channel resistance have been assumed to equal r_{ds} and p_2' is the output pole for normal Miller compensation.

Result:

Dominant pole is approximately the same and the output pole is increased by roughly $g_m r_{ds}$.

Increasing the Magnitude of the Output Pole - Continued

In addition there is a LHP zero at $-g_{m8}/sC_c$ and a RHP zero due to C_{gd6} (shown dashed in the model on Page 6.2-23) at g_{m6}/C_{gd6}.

Roots are:

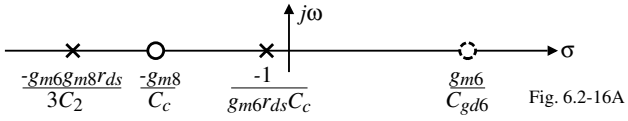


Fig. 6.2-16A

Concept Behind the Increasing of the Magnitude of the Output Pole

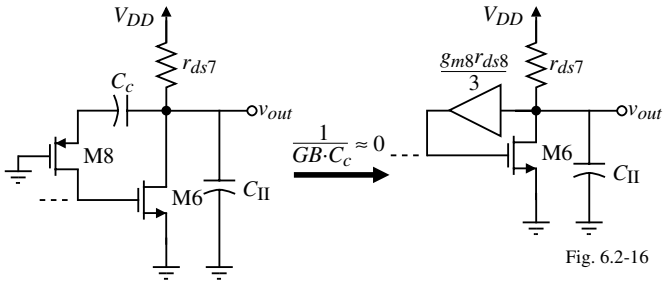


Fig. 6.2-16

$$R_{out} = r_{ds7} \| \left(\frac{3}{g_{m6} g_{m8} r_{ds8}} \right) \approx \frac{3}{g_{m6} g_{m8} r_{ds8}}$$

Therefore, the output pole is approximately,

$$|p_2| \approx \frac{g_{m6} g_{m8} r_{ds8}}{3 C_{II}}$$

Feedforward Compensation

Use two parallel paths to achieve a LHP zero for lead compensation purposes.

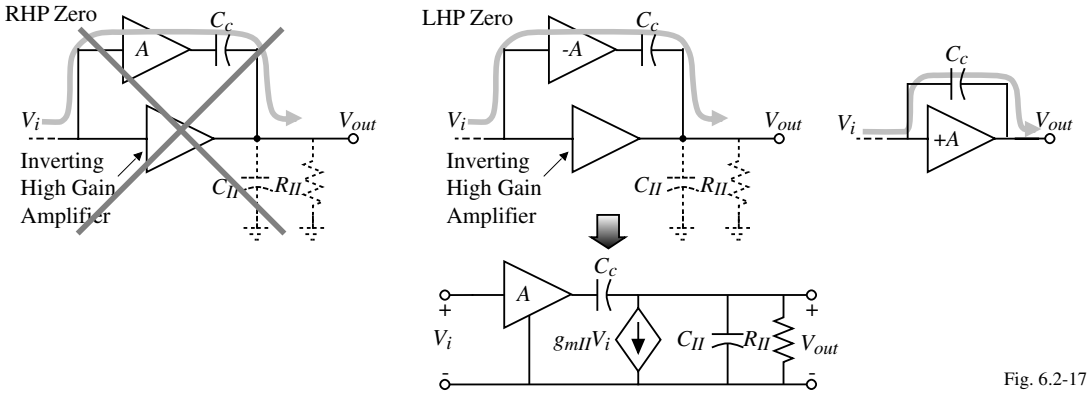


Fig. 6.2-17

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{AC_c}{C_c + C_{II}} \left(\frac{s + g_{mII}/AC_c}{s + 1/[R_{II}(C_c + C_{II})]} \right)$$

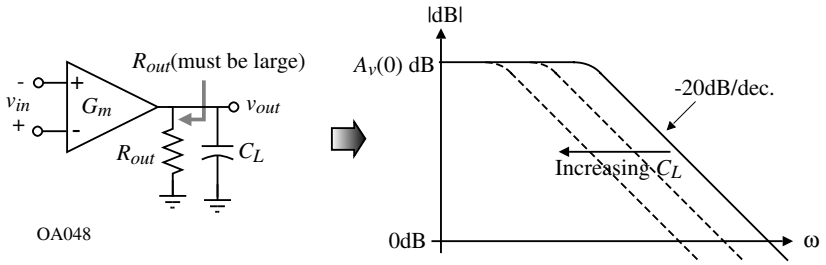
To use the LHP zero for compensation, a compromise must be observed.

- Placing the zero below *GB* will lead to boosting of the loop gain which could deteriorate the phase margin.
- Placing the zero above *GB* will have less influence on the leading phase caused by the zero.

Note that a source follower is a good candidate for the use of feedforward.

Self-Compensated Op Amps

Self compensation occurs when the load capacitor is the compensation capacitor (can never be unstable for resistive feedback)



Voltage gain:

$$\frac{v_{out}}{v_{in}} = A_v(0) = G_m R_{out}$$

Dominant pole:

$$p_1 = \frac{-1}{R_{out}C_L}$$

Unity-gainbandwidth:

$$GB = A_v(0)\cdot|p_1| = \frac{G_m}{C_L}$$

Stability:

Large load capacitors simply reduce the GB and the phase is 90° at the unity gain frequency

Slew Rate of a Two-Stage Op Amp

Remember that slew rate occurs when currents flowing in a capacitor become limited and is given as

$$I_{lim} = C\frac{dv_C}{dt}$$ where v_C is the voltage across the capacitor C.

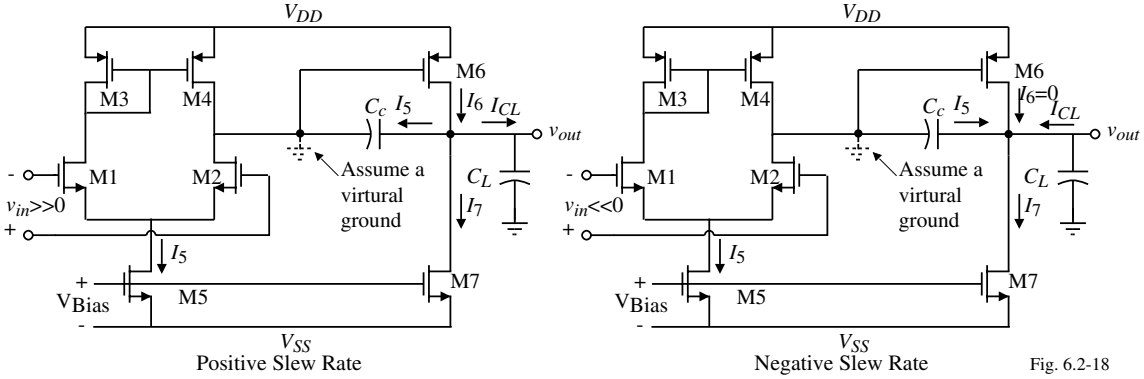


Fig. 6.2-18

$$SR^+ = \min\left[\frac{I_5}{C_c}, \frac{I_6-I_5-I_7}{C_L}\right] = \frac{I_5}{C_c} \text{ because } I_6 >> I_5$$

$$SR^- = \min\left[\frac{I_5}{C_c}, \frac{I_7-I_5}{C_L}\right] = \frac{I_5}{C_c} \text{ if } I_7 >> I_5.$$

Therefore, if C_L is not too large and if I_7 is significantly greater than I_5, then the slew rate of the two-stage op amp should be,

$$SR = \frac{I_5}{C_c}$$

SECTION 6.3 - TWO-STAGE OP AMP DESIGN

Unbuffered, Two-Stage CMOS Op Amp

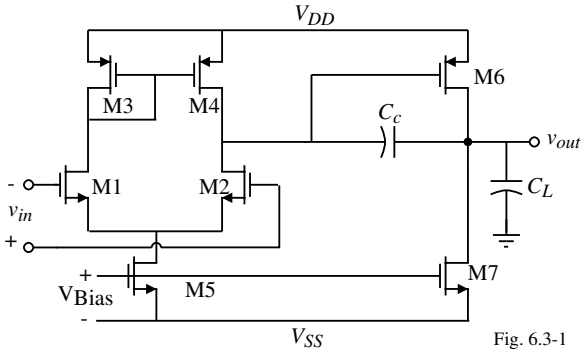


Fig. 6.3-1

Notation:

$$S_i = \frac{W_i}{L_i} = W/L \text{ of the ith transistor}$$

DC Balance Conditions for the Two-Stage Op Amp

For best performance, keep all transistors in saturation.

M4 is the only transistor that cannot be forced into saturation by internal connections or external voltages.

Therefore, we develop conditions to force M4 to be in saturation.

1.) First *assume* that $V_{SG4} = V_{SG6}$. This will cause "proper mirroring" in the M3-M4 mirror. Also, the gate and drain of M4 are at the same potential so that M4 is "guaranteed" to be in saturation.

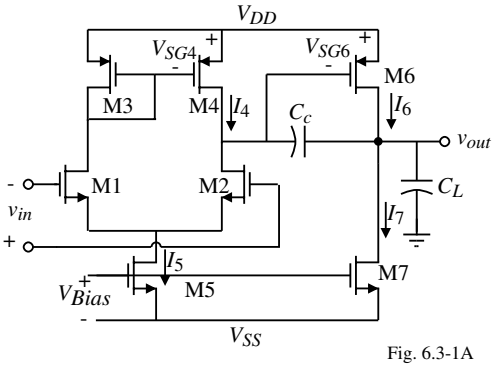


Fig. 6.3-1A

2.) *If* $V_{SG4} = V_{SG6}$, then $I_6 = \left(\frac{S_6}{S_4}\right) I_4$

3.) However, $I_7 = \left(\frac{S_7}{S_5}\right) I_5 = \left(\frac{S_7}{S_5}\right)(2I_4)$

4.) For balance, I_6 must equal $I_7 \Rightarrow \boxed{\frac{S_6}{S_4} = \frac{2S_7}{S_5}}$ which is called the "balance conditions"

5.) So if the balance conditions are satisfied, then $V_{DG4} = 0$ and M4 is saturated.

Design Relationships for the Two-Stage Op Amp

Slew rate $SR = \frac{I_5}{C_c}$ (Assuming $I_7 >> I_5$ and $C_L > C_c$)

First-stage gain $A_{v1} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{2g_{m1}}{I_5(\lambda_2 + \lambda_4)}$

Second-stage gain $A_{v2} = \frac{g_{m6}}{g_{ds6} + g_{ds7}} = \frac{g_{m6}}{I_6(\lambda_6 + \lambda_7)}$

Gain-bandwidth $GB = \frac{g_{m1}}{C_c}$

Output pole $p_2 = \frac{-g_{m6}}{C_L}$

RHP zero $z_1 = \frac{g_{m6}}{C_c}$

60° phase margin requires that $g_{m6} = 2.2g_{m2}(C_L/C_c)$ if all other roots are ≥ $10GB$.

Positive ICMR $V_{\text{in(max)}} = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{T03}|_{(\max)} + V_{T1(\min)})$

Negative ICMR $V_{\text{in(min)}} = V_{SS} + \sqrt{\frac{I_5}{\beta_1}} + V_{T1(\max)} + V_{DS5}(\text{sat})$

Saturation voltage $V_{DS}(\text{sat}) = \sqrt{\frac{2I_{DS}}{\beta}}$

It is assumed that all transistors are in saturation for the above relationships.

Op Amp Specifications

The following design procedure assumes that specifications for the following parameters are given.

1. Gain at dc, $A_v(0)$
2. Gain-bandwidth, GB
3. Phase margin (or settling time)
4. Input common-mode range, ICMR
5. Load Capacitance, C_L
6. Slew-rate, SR
7. Output voltage swing
8. Power dissipation, P_{diss}

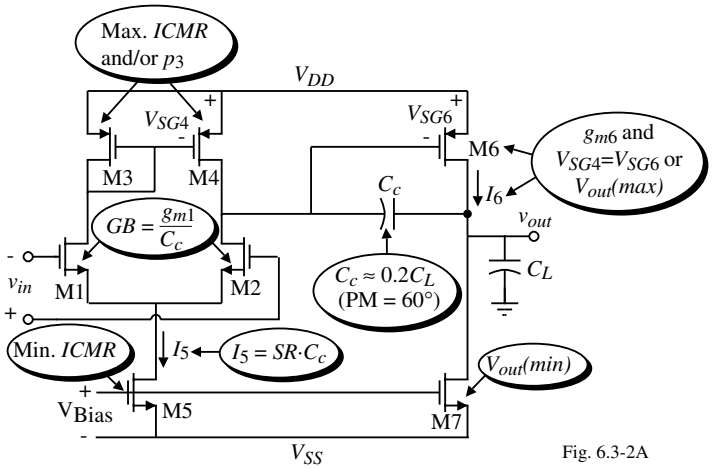


Fig. 6.3-2A

Unbuffered Op Amp Design Procedure

This design procedure assumes that the gain at dc (A_v), unity gain bandwidth (GB), input common mode range (V_{in}(min) and V_{in}(max)), load capacitance (C_L), slew rate (SR), settling time (T_s), output voltage swing (V_{out}(max) and V_{out}(min)), and power dissipation (P_{diss}) are given. Choose the smallest device length which will keep the channel modulation parameter constant and give good matching for current mirrors.

1. From the desired phase margin, choose the minimum value for C_c, i.e. for a 60° phase margin we use the following relationship. This assumes that $z \geq 10GB$.

   $$C_c > 0.22C_L$$

2. Determine the minimum value for the "tail current" (I_5) from the largest of the two values.

   $$I_5 = SR \cdot C_c \qquad \text{or} \qquad I_5 \cong 10\left(\frac{V_{DD} + |V_{SS}|}{2 \cdot T_s}\right)$$

3. Design for S_3 from the maximum input voltage specification.

   $$S_3 = \frac{2I_3}{K'_3[V_{DD} - V_{in}(\max) - |V_{T03}|(\max) + V_{T1}(\min)]^2} \geq 1$$

4. Verify that the pole of M3 due to C_{gs3} and C_{gs4} (=$0.67W_3L_3C_{ox}$) will not be dominant by assuming it to be greater than 10 GB

   $$\frac{g_{m3}}{2C_{gs3}} > 10GB.$$

5. Design for S_1 (S_2) to achieve the desired GB.

   $$g_{m1} = GB \cdot C_c \Rightarrow S_1 = S_2 = \frac{g_{m1}}{K'_1 I_5}$$

Unbuffered Op Amp Design Procedure - Continued

6. Design for S_5 from the minimum input voltage. First calculate V_{DS5}(sat) then find S_5.

   $$V_{DS5}(\text{sat}) = V_{in}(\min) - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1}(\max) \geq 100 \text{ mV} \rightarrow \qquad S_5 = \frac{2I_5}{K'_5[V_{DS5}(\text{sat})]^2}$$

7. Find S_6 by letting the second pole (p_2) be equal to 2.2 times GB and assuming that $V_{SG4} = V_{SG6}$.

   $$g_{m6} = 2.2g_{m2}(C_L/C_c) \qquad \rightarrow \qquad S_6 = S_4\frac{g_{m6}}{g_{m4}}$$

8. Calculate I_6 from

   $$I_6 = \frac{g_{m6}^2}{2K'_6 S_6}$$

Check to make sure that S_6 satisfies the V_{out}(max) requirement and adjust as necessary.

9. Design S_7 to achieve the desired current ratios between I_5 and I_6.

   $S_7 = (I_6/I_5)S_5$ (Check the minimum output voltage requirements)

10. Check gain and power dissipation specifications.

    $$A_v = \frac{2g_{m2}g_{m6}}{I_5(\lambda_2 + \lambda_3)I_6(\lambda_6 + \lambda_7)} \qquad P_{diss} = (I_5 + I_6)(V_{DD} + |V_{SS}|)$$

11. If the gain specification is not met, then the currents, I_5 and I_6, can be decreased or the W/L ratios of M2 and/or M6 increased. The previous calculations must be rechecked to insure that they are satisfied. If the power dissipation is too high, then one can only reduce the currents I_5 and I_6. Reduction of currents will probably necessitate increase of some of the W/L ratios in order to satisfy input and output swings.

12. Simulate the circuit to check to see that all specifications are met.

Example 6.3-1 - Design of a Two-Stage Op Amp

Using the material and device parameters given in Tables 3.1-2 and 3.2-1, design an amplifier similar to that shown in Fig. 6.3-1 that meets the following specifications. Assume the channel length is to be 1μm.

$A_v > 5000$V/V $V_{DD} = 2.5$V $V_{SS} = -2.5$V 60° phase margin
$GB = 5$MHz $C_L = 10$pF $SR > 10$V/μs
V_{out} range = ±2V $ICMR = -1$ to 2V $P_{diss} \leq 2$mW

Solution

1.) The first step is to calculate the minimum value of the compensation capacitor C_c, which is

$$C_c > (2.2/10)(10\text{ pF}) = 2.2\text{ pF}$$

2.) Choose C_c as 3pF. Using the slew-rate specification and C_c calculate I_5.

$$I_5 = (3\text{x}10^{-12})(10\text{ x }10^6) = 30\ \mu\text{A}$$

3.) Next calculate $(W/L)_3$ using ICMR requirements.

$$(W/L)_3 = \frac{30\text{ x }10^{-6}}{(50\text{x}10^{-6})[2.5 - 2 - 0.85 + 0.55]^2} = 15 \quad \rightarrow \quad \boxed{(W/L)_3 = (W/L)_4 = 15}$$

4.) Now we can check the value of the mirror pole, p_3, to make sure that it is in fact greater than $10GB$. Assume the $C_{ox} = 0.4$fF/μm^2. The mirror pole can be found as

$$p_3 \approx \frac{-g_{m3}}{2C_{gs3}} = \frac{-\sqrt{2K'_pS_3I_3}}{2(0.667)W_3L_3C_{ox}} = 2.81\text{x}10^9\text{(rads/sec)}$$

or 448 MHz. Thus, p_3, is not of concern in this design because $p_3 >> 10GB$.

Example 6.3-1 - Continued

5.) The next step in the design is to calculate g_{m1} to get

$$g_{m1} = (5\text{x}10^6)(2\pi)(3\text{x}10^{-12}) = 94.25\mu\text{S}$$

Therefore, $(W/L)_1$ is

$$(W/L)_1 = (W/L)_2 = \frac{g_{m1}^2}{2K'_NI_1} = \frac{(94.25)^2}{2\cdot110\cdot15} = 2.79 \approx 3.0 \Rightarrow \quad \boxed{(W/L)_1 = (W/L)_2 = 3}$$

6.) Next calculate V_{DS5},

$$V_{DS5} = (-1) - (-2.5) - \sqrt{\frac{30\text{x}10^{-6}}{110\text{x}10^{-6}\cdot3}} - .85 = 0.35\text{V}$$

Using V_{DS5} calculate $(W/L)_5$ from the saturation relationship.

$$(W/L)_5 = \frac{2(30\text{ x }10^{-6})}{(110\text{ x }10^{-6})(0.35)^2} = 4.49 \approx 4.5 \quad \rightarrow \quad \boxed{(W/L)_5 = 4.5}$$

7.) For 60° phase margin, we know that

$$g_{m6} \geq 10g_{m1} \geq 942.5\mu\text{S}$$

Assuming that $g_{m6} = 942.5\mu$S and knowing that $g_{m4} = 150\mu$S, we calculate $(W/L)_6$ as

$$(W/L)_6 = 15\,\frac{942.5\text{ x }10^{-6}}{(150\text{ x }10^{-6})} = 94.25 \approx 94$$

Example 6.3-1 - Continued

8.) Calculate I_6 using the small-signal g_m expression: $I_6 = \frac{(942.5 \text{ x } 10^{-6})^2}{(2)(50 \text{ x } 10^{-6})(94)} = 94.5\mu A \approx 95\mu A$

If we calculate $(W/L)_6$ based on V_{out}(max), the value is approximately 15. Since 94 exceeds the specification and maintains better phase margin, we will stay with $(W/L)_6 = 94$ and $I_6 = 95\mu A$.

With $I_6 = 95\mu A$ the power dissipation is

$$P_{diss} = 5V \cdot (30\mu A + 95\mu A) = 0.625mW.$$

9.) Finally, calculate $(W/L)_7$

$$(W/L)_7 = 4.5\left(\frac{95 \text{ x } 10^{-6}}{30 \text{ x } 10^{-6}}\right) = 14.25 \approx 14 \quad \rightarrow \quad \boxed{(W/L)_7 = 14}$$

Let us check the V_{out}(min) specification although the W/L of M7 is so large that this is probably not necessary. The value of V_{out}(min) is

$$V_{out}(\text{min}) = V_{DS7}(\text{sat}) = \sqrt{\frac{2 \cdot 95}{110 \cdot 14}} = 0.351V$$

which is less than required. At this point, the first-cut design is complete.

10.) Now check to see that the gain specification has been met

$$A_v = \frac{(94.25 \text{ x } 10^{-6})(942.5 \text{ x } 10^{-6})}{15 \text{ x } 10^{-6}(.04 + .05)95 \text{ x } 10^{-6}(.04 + .05)} = 7{,}696V/V$$

which meets specifications. An easy way to increase the gain would be to increase the W and L values by a factor of two which because of the decreased value of λ would multiply the above gain by a factor of 20.

Example 6.3-1 - Continued

The final step in the hand design is to establish true electrical widths and lengths based upon ΔL and ΔW variations. In this example ΔL will be due to lateral diffusion only. Unless otherwise noted, ΔW will not be taken into account. All dimensions will be rounded to integer values. Assume that ΔL = 0.2μm. Therefore, we have

$W_1 = W_2 = 3(1 - 0.4) = 1.8\ \mu m \approx 2\mu m$
$W_3 = W_4 = 15(1 - 0.4) = 9\mu m$
$W_5 = 4.5(1 - 0.4) = 2.7\mu m \approx 3\mu m$
$W_6 = 94(1 - 0.4) = 56.4\mu m \approx 56\mu m$
$W_7 = 14(1 - 0.4) = 8.4 \approx 8\mu m$

The figure below shows the results of the first-cut design. The W/L ratios shown do not account for the lateral diffusion discussed above. The next phase requires simulation.

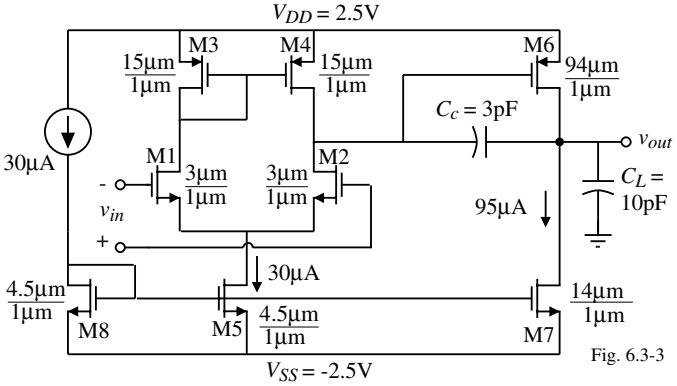


Fig. 6.3-3

