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CSC 137  
HW 4.

## Chap 4

#4.7

$$\text{Setup time } (T_{st}) = 0.1 \text{ ns}$$

$$\text{Hold time } (T_{cq-\max}) = 0.1 \text{ ns}$$

$$\text{Maximum propagation delay } (T_{pd-\max}) = 0.3 \text{ ns}$$

$$T = T_{st} + T_{cq-\max} + T_{pd-\max} = (0.1 + 0.1 + 0.3) \text{ ns} \\ = 0.5 \text{ ns}$$

Maximum clock frequency:

$$f = \frac{1}{T} = \frac{1}{0.5 \text{ ns}} = 2 \text{ Hz}$$

## Chap 4

# 4.8

HDR model:

```
module dfliptlop
(
    input D, CLK, -reset, -preset,
    output Q, Q-BAR
);
    assign Q-BAR = ~Q;
    nand U1 (X, D, CLK);
    nand U2 (Y, X, CLK);
    nand U3 (Q, Q-BAR, X);
    nand U4 (Q-BAR, Q, Y);
endmodule
```

Test-bench:

```
`include "dfliptlop.v"
module testdfliptlop();
```

```
    reg D, CLK, -reset, -preset;
    wire Q, Q-BAR;
```

```
    initial begin
```

```
        $monitor(" CLK = %b -reset = %b -preset = %b D = %b Q = %b Q-BAR = %b",
            CLK, -reset, -preset, D, Q, Q-BAR);
```

```
        CLK = 0; -reset = 1; -preset = 1;
```

```
        #1 -reset = 0;
```

```
        #1 -preset = 1;
```

```
        #1 D = 1;
```

```
        #1 CLK = 1;
```

```
        #1 D = 0
```

```
        #10 $finish;
```

```
    end
endmodule
```

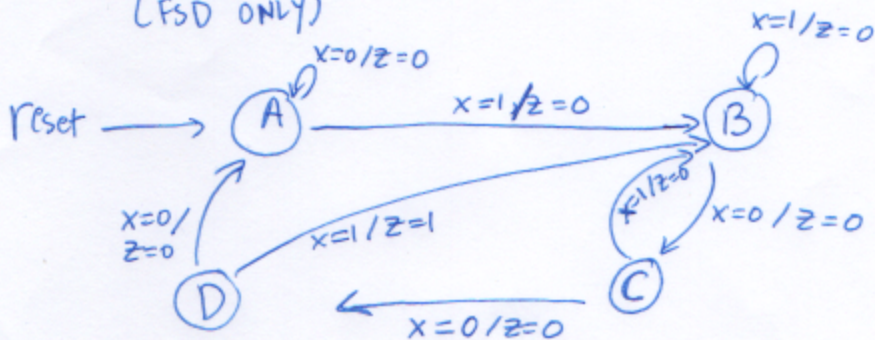


# Chap 5

#5.11

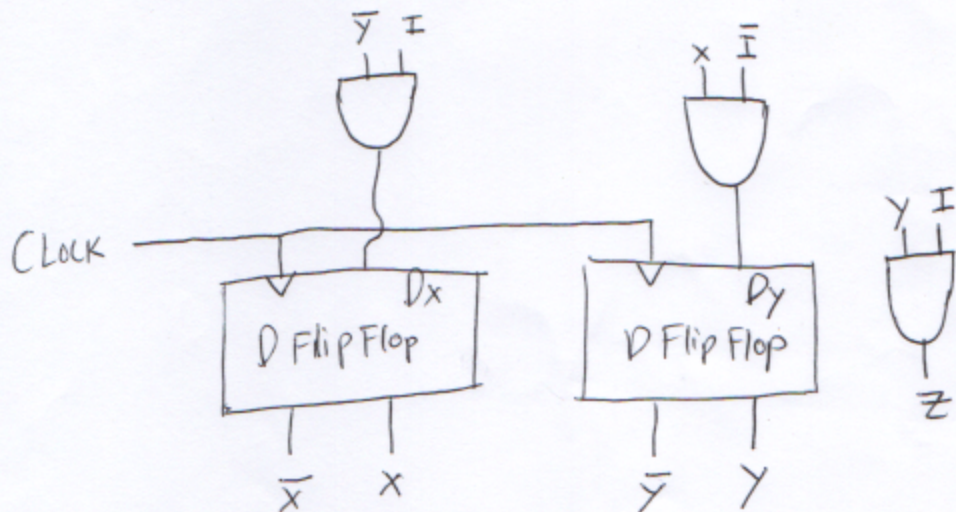
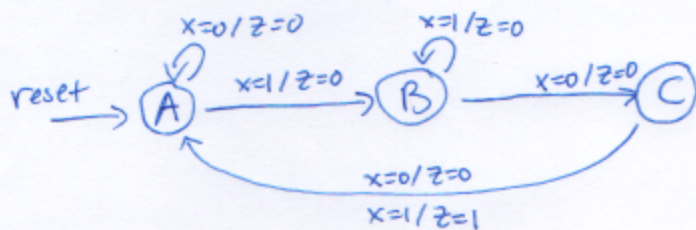
Design a Mealy sequence recognizer that detects the overlapping sequence "001".

(FSD ONLY)



#5.9

Mealy sequence recognizer that detects the nonoverlapping "101"



# Chap 5

#5.21 Design a mod 4 up/down counter

$m=0$  up counter  $0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 6 \rightarrow 7$

$m=1$  down counter  $7 \rightarrow 6 \rightarrow 5 \rightarrow 4 \rightarrow 3 \rightarrow 2 \rightarrow 1 \rightarrow 0$

We need 4 D FlipFlops, AND gates, OR gates

