



程序的性能优化

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提纲

- 概述
- 常用的优化技术
 - 代码移动/预算算
 - 减小强度
 - 共享相同子表达式
 - 示例：冒泡排序
- 优化的阻碍
 - 函数调用
 - 内存别名
- 指令级并行
- 处理条件判断



关于性能

- *There's more to performance than asymptotic complexity*
(复杂度)
- Constant factors matter too!
 - Easily see 10:1 performance range depending on **how code is written**
 - Must optimize at multiple levels:
 - 算法、数据类型、函数、循环
- Must understand system to optimize performance
 - How programs are compiled and executed, 编译
 - How modern processors + memory systems operate, 架构+存储
 - How to measure program performance and identify bottlenecks, 瓶颈分析
 - How to improve performance without destroying code modularity and generality, 模块化和通用性



优化编译器

- Provide efficient mapping of program to machine
 - register allocation 寄存器分配
 - code selection and ordering (scheduling) 代码选择和调度
 - dead code elimination 消除无效代码
 - eliminating minor inefficiencies 消除低效代码
- Don't (usually) improve asymptotic efficiency
 - up to programmer to select best overall algorithm
 - big-O savings are (often) more important than constant factors
 - but constant factors also matter
- Have difficulty overcoming “optimization blockers”
 - potential memory aliasing
 - potential procedure side-effects



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Generally Useful Optimizations

- Optimizations that you or the compiler should do regardless of processor / compiler
- 代码移动 Code Motion
 - Reduce frequency with which computation performed
 - If it will always produce same result
 - Especially moving code out of loop

```
void set_row(double *a, double *b,
    long i, long n)
{
    long j;
    for (j = 0; j < n; j++)
        a[n*i+j] = b[j];
}
```



```
long j;
int ni = n*i;
for (j = 0; j < n; j++)
    a[ni+j] = b[j];
```



Compiler-Generated Code Motion (-O1)

```
void set_row(double *a, double *b,
    long i, long n)
{
    long j;
    for (j = 0; j < n; j++)
        a[n*i+j] = b[j];
}
```

```
long j;
long ni = n*i;
double *rowp = a+ni;
for (j = 0; j < n; j++)
    *rowp++ = b[j];
```

```
set_row:
    testq    %rcx, %rcx
    jle     .L1
    imulq    %rcx, %rdx
    leaq     (%rdi,%rdx,8), %rdx
    movl     $0, %eax
.L3:
    movsd    (%rsi,%rax,8), %xmm0
    movsd    %xmm0, (%rdx,%rax,8)
    addq     $1, %rax
    cmpq     %rcx, %rax
    jne     .L3
.L1:
    rep ; ret
```

Test n
If 0, goto done
ni = n*i
rowp = A + ni*8
j = 0
loop:
t = b[j]
M[A+ni*8 + j*8] = t
j++
j:n
if !=, goto loop
done:



Reduction in Strength

- Replace costly operation with simpler one
- Shift, add instead of multiply or divide

$16 * x \rightarrow x << 4$

- Utility machine dependent
- Depends on cost of multiply or divide instruction
 - On Intel Nehalem, integer multiply requires 3 CPU cycles
- Recognize sequence of products

```
for (i = 0; i < n; i++) {  
    int ni = n*i;  
    for (j = 0; j < n; j++)  
        a[ni + j] = b[j];  
}
```



```
int ni = 0;  
for (i = 0; i < n; i++) {  
    for (j = 0; j < n; j++)  
        a[ni + j] = b[j];  
    ni += n;  
}
```



Share Common Subexpressions

- Reuse portions of expressions
- GCC will do this with -O1

```
/* Sum neighbors of i,j */
up =    val[(i-1)*n + j];
down =   val[(i+1)*n + j];
left =   val[i*n      + j-1];
right =  val[i*n      + j+1];
sum = up + down + left + right;
```

```
long inj = i*n + j;
up =    val[inj - n];
down =   val[inj + n];
left =   val[inj - 1];
right =  val[inj + 1];
sum = up + down + left + right;
```

3 multiplications: $i*n$, $(i-1)*n$, $(i+1)*n$

1 multiplication: $i*n$

```
leaq    1(%rsi), %rax # i+1
leaq    -1(%rsi), %r8  # i-1
imulq   %rcx, %rsi   # i*n
imulq   %rcx, %rax   # (i+1)*n
imulq   %rcx, %r8    # (i-1)*n
addq    %rdx, %rsi   # i*n+j
addq    %rdx, %rax   # (i+1)*n+j
addq    %rdx, %r8    # (i-1)*n+j
...
```

```
imulq   %rcx, %rsi   # i*n
addq    %rdx, %rsi   # i*n+j
movq    %rsi, %rax   # i*n+j
subq    %rcx, %rax   # i*n+j-n
leaq    (%rsi,%rcx), %rcx # i*n+j+n
...
```



Bubblesort

比较遍数

数据	1	2	3	4
587	-632	-632	-632	-632
-632	587	234	-34	-34
777	234	-34	234	234
234	-34	587	587	587
-34	777	777	777	777

从小到大排序



Optimization Example: Bubblesort

- **Bubblesort program that sorts an array **A** that is allocated in static storage:**
 - an element of **A** requires **four bytes** of a byte-addressed machine
 - elements of **A** are numbered **1** through **n** (**n** is a variable)
 - **A[j]** is in location **&A+4*(j-1)**

```
for (i = n-1; i >= 1; i--) {  
    for (j = 1; j <= i; j++)  
        if (A[j] > A[j+1]) {  
            temp = A[j];  
            A[j] = A[j+1];  
            A[j+1] = temp;  
        }  
}
```



Translated (Pseudo) Code

```
i := n-1
L5: if i<1 goto L1
j := 1
L4: if j>i goto L2
t1 := j-1
t2 := 4*t1
t3 := A[t2]    // A[j]
t4 := j+1
t5 := t4-1
t6 := 4*t5
t7 := A[t6]    // A[j+1]
if t3<=t7 goto L3

for (i = n-1; i >= 1; i--) {
    for (j = 1; j <= i; j++) {
        if (A[j] > A[j+1]) {
            temp = A[j];
            A[j] = A[j+1];
            A[j+1] = temp;
        }
    }
}
```

```
t8 := j-1
t9 := 4*t8
temp := A[t9]    // temp:=A[j]
t10 := j+1
t11 := t10-1
t12 := 4*t11
t13 := A[t12]    // A[j+1]
t14 := j-1
t15 := 4*t14
A[t15] := t13    // A[j]:=A[j+1]
t16 := j+1
t17 := t16-1
t18 := 4*t17
A[t18]:=temp    // A[j+1]:=temp
L3: j := j+1
    goto L4
L2: i := i-1
    goto L5
L1:
```

Instructions
29 in outer loop
25 in inner loop



Redundancy in Address Calculation

```
i := n-1  
L5: if i<1 goto L1  
j := 1  
L4: if j>i goto L2  
t1 := j-1  
t2 := 4*t1  
t3 := A[t2] // A[j]  
t4 := j+1  
t5 := t4-1  
t6 := 4*t5  
t7 := A[t6] // A[j+1]  
if t3<=t7 goto L3
```

```
t8 := j-1  
t9 := 4*t8  
temp := A[t9] // temp:=A[j]  
t10 := j+1  
t11 := t10-1  
t12 := 4*t11  
t13 := A[t12] // A[j+1]  
t14 := j-1  
t15 := 4*t14  
A[t15] := t13 // A[j]:=A[j+1]  
t16 := j+1  
t17 := t16-1  
t18 := 4*t17  
A[t18] := temp // A[j+1]:=temp  
L3: j := j+1  
     goto L4  
L2: i := i-1  
     goto L5  
L1:
```



Redundancy Removed

```
i := n-1  
L5: if i<1 goto L1  
     j := 1  
L4: if j>i goto L2  
     t1 := j-1  
     t2 := 4*t1  
     t3 := A[t2]      // A[j]  
     t6 := 4*j  
     t7 := A[t6]      // A[j+1]  
     if t3<=t7 goto L3  
          t8 :=j-1  
          t9 := 4*t8  
          temp := A[t9]    // temp:=A[j]  
          t12 := 4*j  
          t13 := A[t12]    // A[j+1]  
          A[t9]:= t13    // A[j]:=A[j+1]  
          A[t12]:=temp   // A[j+1]:=temp  
L3:  j := j+1  
      goto L4  
L2:  i := i-1  
      goto L5  
L1:
```

Instructions
20 in outer loop
16 in inner loop



More Redundancy

```
i := n-1  
L5: if i<1 goto L1  
     j := 1  
L4: if j>i goto L2  
     t1 := j-1  
     t2 := 4*t1  
     t3 := A[t2]      // A[j]  
     t6 := 4*j  
     t7 := A[t6]      // A[j+1]  
     if t3<=t7 goto L3
```

```
t8 :=j-1  
t9 := 4*t8  
temp := A[t9] // temp:=A[j]  
t12 := 4*j  
t13 := A[t12] // A[j+1]  
A[t9]:= t13 // A[j]:=A[j+1]  
A[t12]:=temp // A[j+1]:=temp  
L3: j := j+1  
    goto L4  
L2: i := i-1  
    goto L5  
L1:
```



Redundancy Removed

```
i := n-1
L5: if i<1 goto L1
      j := 1
      L4: if j>i goto L2
            t1 := j-1
            t2 := 4*t1
            t3 := A[t2]    // old_A[j]
            t6 := 4*j
            t7 := A[t6]    // A[j+1]
            if t3<=t7 goto L3
            A[t2] := t7   // A[j]:=A[j+1]
            A[t6] := t3   // A[j+1]:=old_A[j]
      L3: j := j+1
          goto L4
      L2: i := i-1
          goto L5
      L1:
```

Instructions

15 in outer loop
11 in inner loop



Redundancy in Loops

```
i := n-1  
L5: if i<1 goto L1  
  
L4: if j>i goto L2  
    t1 := j-1  
    t2 := 4*t1  
  
    t3 := A[t2]      // A[j]  
    t6 := 4*j  
  
    t7 := A[t6]      // A[j+1]  
  
    if t3<=t7 goto L3  
    A[t2] := t7  
    A[t6] := t3  
  
L3: j := j+1  
    goto L4  
  
L2: i := i-1  
    goto L5  
  
L1:
```



Redundancy Eliminated

```
i := n-1  
L5: if i<1 goto L1  
  
    j := 1  
  
L4: if j>i goto L2  
    t1 := j-1  
  
    t2 := 4*t1  
  
    t3 := A[t2]      // A[j]  
  
    t6 := 4*j  
  
    t7 := A[t6]      // A[j+1]  
  
    if t3<=t7 goto L3  
    A[t2] := t7  
    A[t6] := t3  
  
L3:  j := j+1  
      goto L4  
  
L2:  i := i-1  
      goto L5  
  
L1:
```

```
i := n-1  
L5: if i<1 goto L1  
  
    t2 := 0  
    t6 := 4  
    t19 := 4*i  
  
L4: if t6>t19 goto L2  
    t3 := A[t2]  
    t7 := A[t6]  
    if t3<=t7 goto L3  
    A[t2] := t7  
    A[t6] := t3  
  
L3:  t2 := t2+4  
    t6 := t6+4  
    goto L4  
  
L2:  i := i-1  
    goto L5  
  
L1:
```



Final Pseudo Code

```
i := n-1  
L5: if i<1 goto L1  
    t2 := 0  
    t6 := 4  
    t19 := i << 2  
  
L4: if t6>t19 goto L2  
    t3 := A[t2]  
    t7 := A[t6]  
    if t3<=t7 goto L3  
    A[t2] := t7  
    A[t6] := t3  
  
L3: t2 := t2+4  
    t6 := t6+4  
    goto L4  
  
L2: i := i-1  
    goto L5  
  
L1:
```

**Instruction Count
Before Optimizations**
29 in outer loop
25 in inner loop

**Instruction Count
After Optimizations**
15 in outer loop
9 in inner loop

- These were **Machine-Independent Optimizations**.
- Will be followed by **Machine-Dependent Optimizations**, including allocating temporaries to registers, converting to assembly code



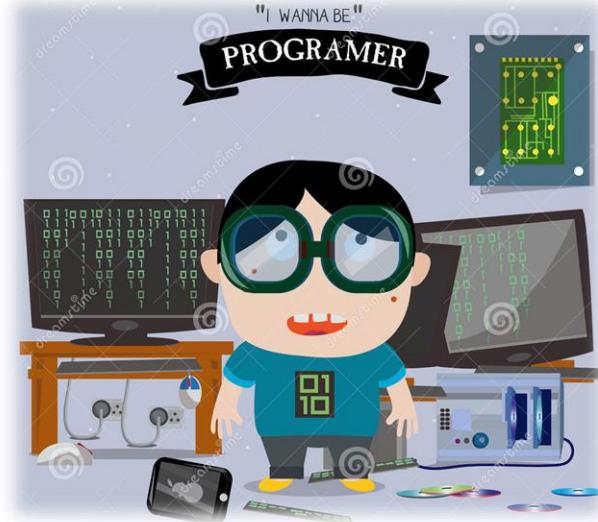
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优化编译器的能力和局限性

- GCC胜任基本的优化，不适合执行激进的变换
- GCC程序员需要强化代码优化，以简化编译器生成高效代码任务的方式编写程序



GCC-conscious programming



编译器优化的能力和局限性

- 优化行为受到基本的约束
 - 不能改变程序行为
 - 除非程序使用非标准语言功能时
 - 通常会阻止它进行仅影响特殊条件下行为的优化
- 对程序员来说可能很明显的行为可能会被语言和编码风格混淆
 - e.g., Data ranges may be more limited than variable types suggest 例如，数据范围可能比变量类型的建议范围更有限
- 大多数分析仅在程序内执行
 - 在大多数情况下，整个程序分析的成本太高
 - 较新版本的 GCC 在单个文件中执行过程间分析
 - 但是，不是在不同文件中的代码之间
- 大多数分析仅基于静态信息
 - 编译器难以预测运行时输入
- 如有疑问，编译器必须是保守的



Optimization Blocker #1: Procedure Calls

- Procedure to Convert String to Lower Case

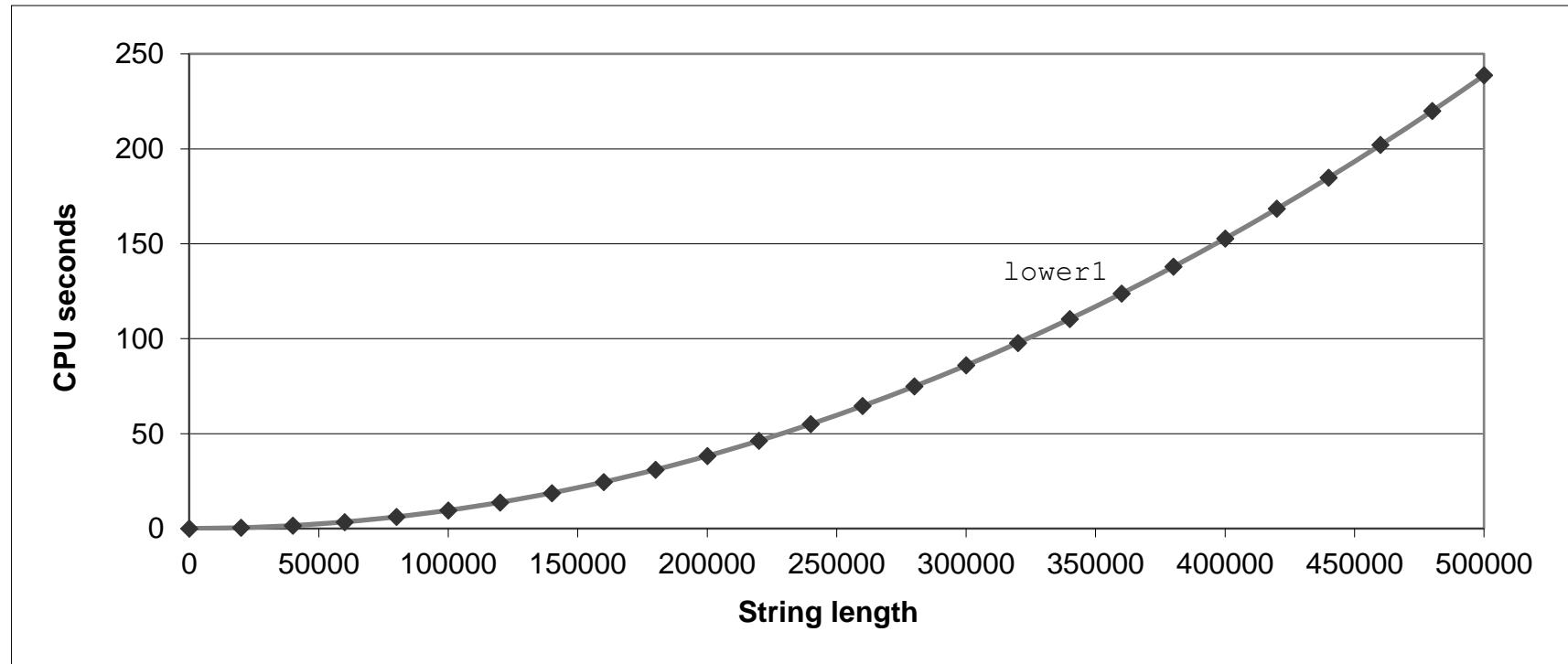
```
void lower(char *s)
{
    size_t i;
    for (i = 0; i < strlen(s); i++)
        if (s[i] >= 'A' && s[i] <= 'Z')
            s[i] -= ('A' - 'a');
}
```

- Extracted from 213 lab submissions, Fall, 1998



Lower Case Conversion Performance

- Time quadruples when double string length
- Quadratic performance





Convert Loop To Goto Form

```
void lower(char *s)
{
    size_t i = 0;
    if (i >= strlen(s))
        goto done;
loop:
    if (s[i] >= 'A' && s[i] <= 'Z')
        s[i] -= ('A' - 'a');
    i++;
    if (i < strlen(s))
        goto loop;
done:
}
```

- `strlen` executed every iteration



Calling Strlen

```
/* My version of strlen */
size_t strlen(const char *s)
{
    size_t length = 0;
    while (*s != '\0') {
        s++;
        length++;
    }
    return length;
}
```

- Strlen performance
 - Only way to determine length of string is to scan its entire length, looking for null character.
- Overall performance, string of length N
 - N calls to strlen
 - Require times N, N-1, N-2, ..., 1
 - Overall O(N²) performance



Improving Performance

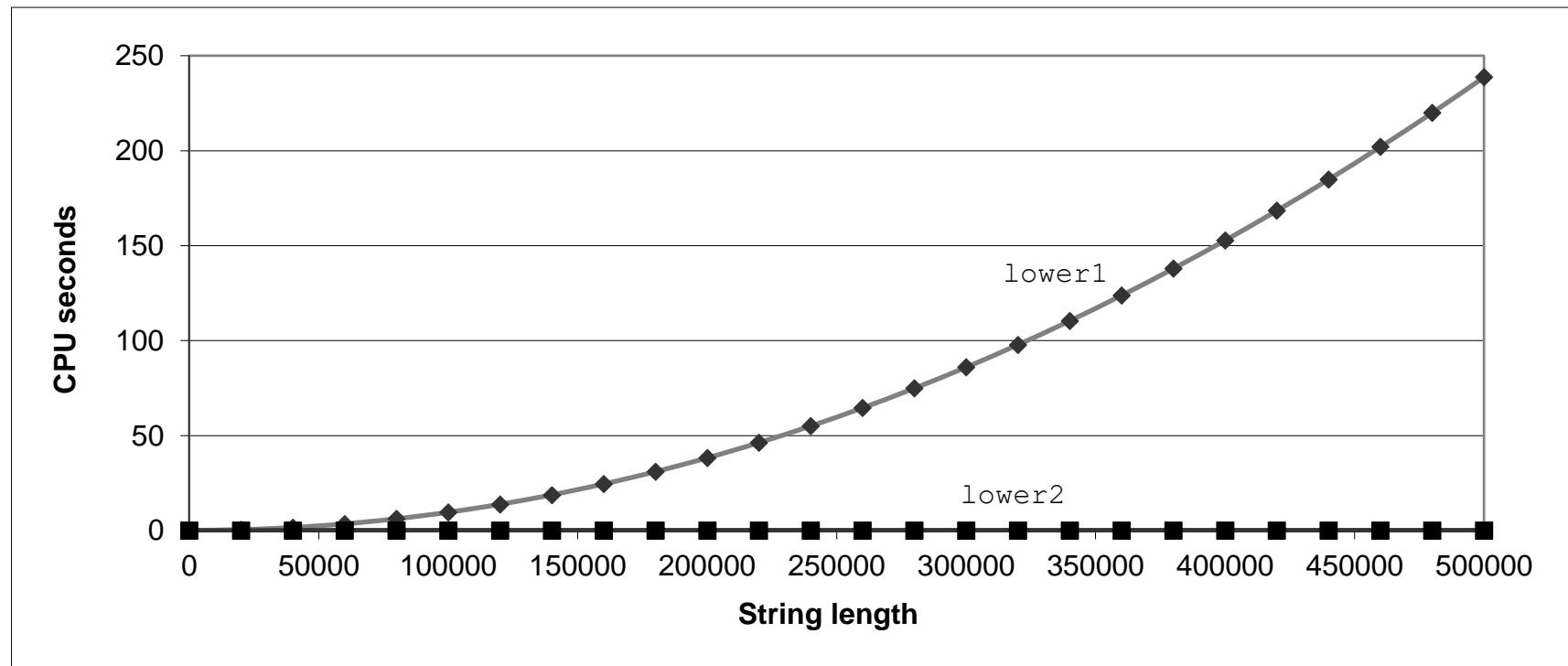
```
void lower(char *s)
{
    size_t i;
    size_t len = strlen(s);
    for (i = 0; i < len; i++)
        if (s[i] >= 'A' && s[i] <= 'Z')
            s[i] -= ('A' - 'a');
}
```

- Move call to `strlen` outside of loop
- Since result does not change from one iteration to another
- Form of code motion



Lower Case Conversion Performance

- Time doubles when double string length
- Linear performance of lower2





Optimization Blocker: Procedure Calls

- *Why couldn't compiler move strlen out of inner loop?*
 - Procedure may have side effects
 - Alters global state each time called
 - Function may not return same value for given arguments
 - Depends on other parts of global state
 - Procedure lower could interact with strlen
- **Warning:**
 - Compiler treats procedure call as a black box
 - Weak optimizations near them
- Remedies:
 - Use of inline functions
 - GCC does this with -O1
 - Within single file
 - Do your own code motion

```
size_t lencnt = 0;
size_t strlen(const char *s)
{
    size_t length = 0;
    while (*s != '\0') {
        s++; length++;
    }
    lencnt += length;
    return length;
}
```



Which one is better?

```
long f()
long func1() {
    return f() + f() + f() + f();
}

long func2() {
    return 4*f();
}
```



func1



func2

提交



Optimization Blocker: Procedure Calls

- Which one is better?

```
long f()
long func1() {
    return f()+f()+f()+f();
}

long func2() {
    return 4*f();
}
```

- ◆ 函数f()中改变counter值，调用次数不同函数返回值不同。
- ◆ func1()中f()被调用4次，函数返回值分别为0, 1, 2, 3，因此func1()返回值为 $0+1+2+3=6$;
- ◆ func2()中只调用f()一次，因此返回值为 $4*0=0$

- But if ...

```
long counter = 0;
long f () {
    return counter++;
}
```



Optimization Blocker: Procedure Calls

- 内联函数替换函数调用

- 使用inline关键字定义内联函数，编译器优化时将函数调用替换为内联函数体

```
inline long f() {
    return counter++;
}

long func1() {
    return f() + f() + f() + f();
}
```

- ◆ 通过内联函数替换掉对函数f()的四次调用
- ◆ 编译器统一func1中对全局变量counter的更新，产生优化版本funclopt();

```
Long func1in() {
    long t=counter++; //0
    t+=counter++; //1
    t+=counter++; //2
    t+=counter++; //3
    return t;
}
```

```
[nsrc@localhost ~]$ inlinefcall
inline f call:6
f call:6
```

```
Long funclopt() {
    long t=4*counter+6; //6
    counter+=4; //4
    return t;
}
```



练习题5.3

```
long min(long x,long y){  
    cmin++;  
    return x<y?x:y;  
}  
  
long max(long x,long y){  
    cmax++;  
    return x<y?y:x;  
}  
  
void incr(long *xp,long v){  
    cincr++;  
    *xp+=v;  
}  
  
long square(long x){  
    csqu++;  
    return x*x;  
}  
  
A.  
for (i=min(x,y);i<max(x,y);incr(&i,1))  
    t+=square(i);  
  
B.  
for (i=max(x,y);i>=min(x,y);incr(&i,-1))  
    t+=square(i);  
  
C.  
long low=min(x,y);  
long high=max(x,y);  
for (i=low;i<high;incr(&i,1))  
    t+=square(i);
```

改进1：使用内联函数

```
inline  
void inline_incr(long *xp,long v){  
    cincr++;  
    *xp+=v;  
}  
  
inline long inline_square(long x){  
    csqu++;  
    return x*x;  
}
```

改进2：使用宏定义

```
#define SQUA(X) (X*X)
```



Which one is better?

```
void twiddle1()
{
    *xp += *yp;
    *xp += *yp;
}

void twiddle2()
{
    *xp += 2**yp;
}
```

A

twiddle1

B

twiddle2

提交



Optimization Blocker:

- Which one is better?

```
void twiddle1()
{
    *xp += *yp;
    *xp += *yp;
}

void twiddle2()
{
    *xp += 2**yp;
}
```

- But if $xp = yp$?

```
twiddle1 result:6
twiddle2 result:6
case xp=yp
twiddle1 result:8
twiddle2 result:6
```



Memory Matters

```
/* Sum rows is of n X n matrix a
   and store in vector b */
void sum_rows1(double *a, double *b, long n) {
    long i, j;
    for (i = 0; i < n; i++) {
        b[i] = 0;
        for (j = 0; j < n; j++)
            b[i] += a[i*n + j];
    }
}
```

```
# sum_rows1 inner loop
.L4:
    movsd    (%rsi,%rax,8), %xmm0      # FP load
    addsd    (%rdi), %xmm0               # FP add
    movsd    %xmm0, (%rsi,%rax,8)       # FP store
    addq    $8, %rdi
    cmpq    %rcx, %rdi
    jne     .L4
```

- Code updates $b[i]$ on every iteration
- Why couldn't compiler optimize this away?



Memory Aliasing

```
/* Sum rows is of n X n matrix a
   and store in vector b */
void sum_rows1(double *a, double *b, long n) {
    long i, j;
    for (i = 0; i < n; i++) {
        b[i] = 0;
        for (j = 0; j < n; j++)
            b[i] += a[i*n + j];
    }
}
```

```
double A[9] =
{ 0, 1, 2,
  4, 8, 16,
  32, 64, 128};

double B[3] = A+3;

sum_rows1(A, B, 3);
```

```
double A[9] =
{ 0, 1, 2,
  3, 22, 224,
  32, 64, 128};
```

Value of B:

```
init: [4, 8, 16]
```

```
i = 0: [3, 8, 16]
```

```
i = 1: [3, 22, 16]
```

```
i = 2: [3, 22, 224]
```

- Code updates **b[i]** on every iteration
- Must consider possibility that these updates will affect program behavior



Removing Aliasing

```
/* Sum rows is of n X n matrix a
   and store in vector b */
void sum_rows2(double *a, double *b, long n) {
    long i, j;
    for (i = 0; i < n; i++) {
        double val = 0;
        for (j = 0; j < n; j++)
            val += a[i*n + j];
        b[i] = val;
    }
}
```

```
# sum_rows2 inner loop
.L10:
    addsd    (%rdi), %xmm0      # FP load + add
    addq    $8, %rdi
    cmpq    %rax, %rdi
    jne     .L10
```

- No need to store intermediate results



Optimization Blocker: Memory Aliasing

- Aliasing
 - Two different memory references specify single location
 - Easy to have happen in C
 - Since allowed to do address arithmetic
 - Direct access to storage structures
 - Get in habit of introducing local variables
 - Accumulating within loops
 - Your way of telling compiler not to check for aliasing

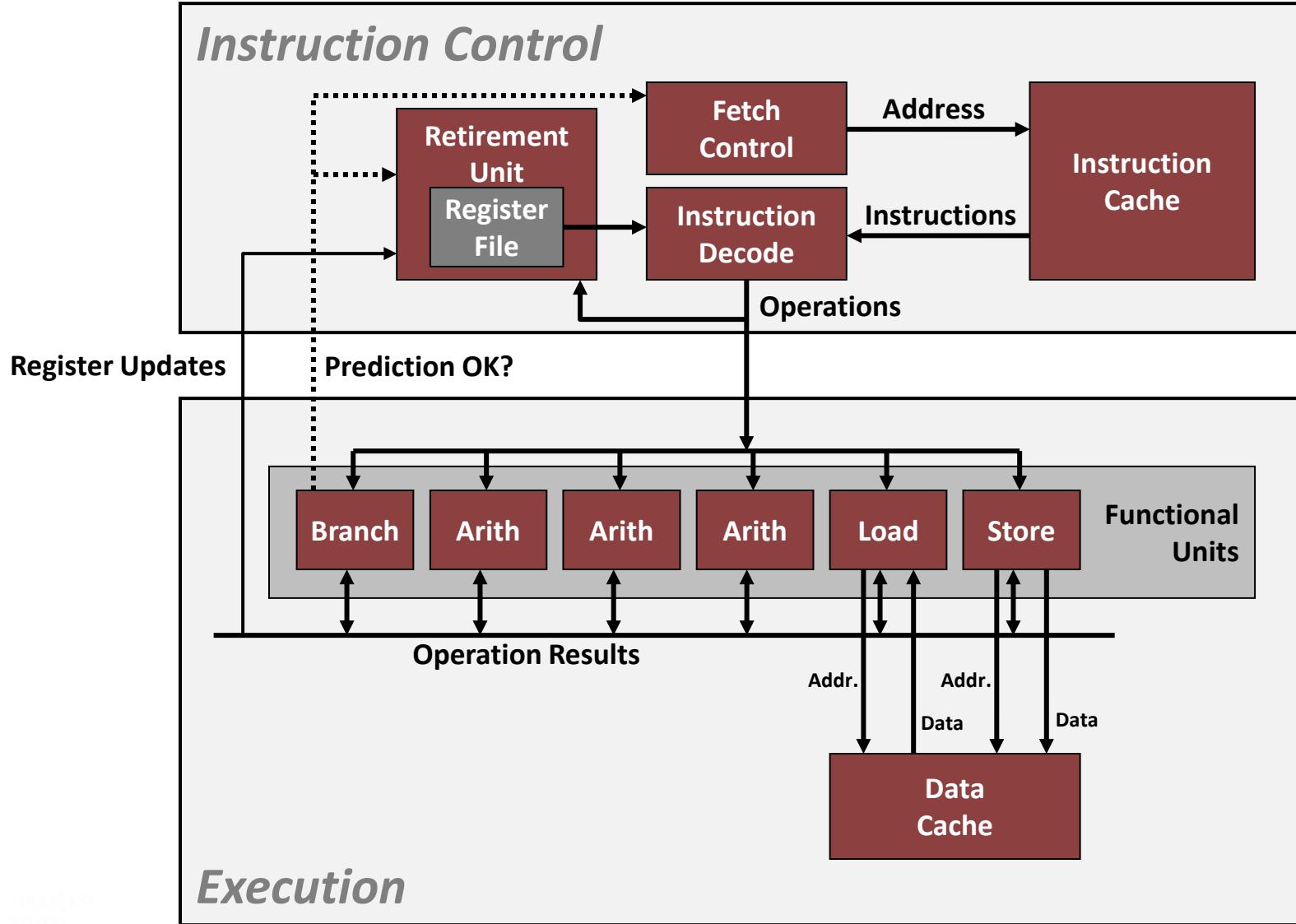


提纲

- 概述
- 常用的优化技术
 - 代码移动/预算算
 - 减小强度
 - 共享相同子表达式
 - 示例：冒泡排序
- 优化的阻碍
 - 函数调用
 - 内存别名
- 指令级并行
- 处理条件判断

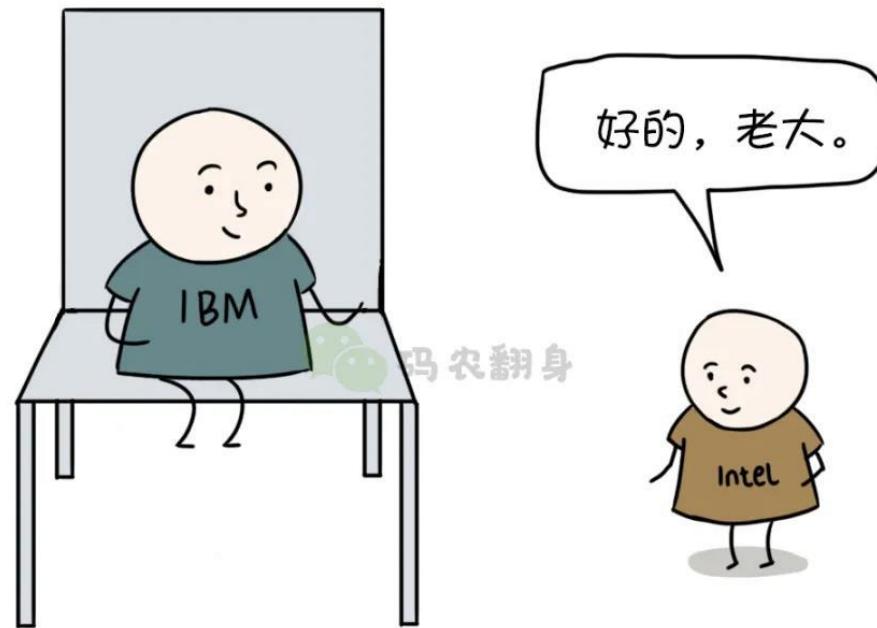


Modern CPU Design





为了防止你一家独大，必须得有第二供应商！



冯农翻身





Windows

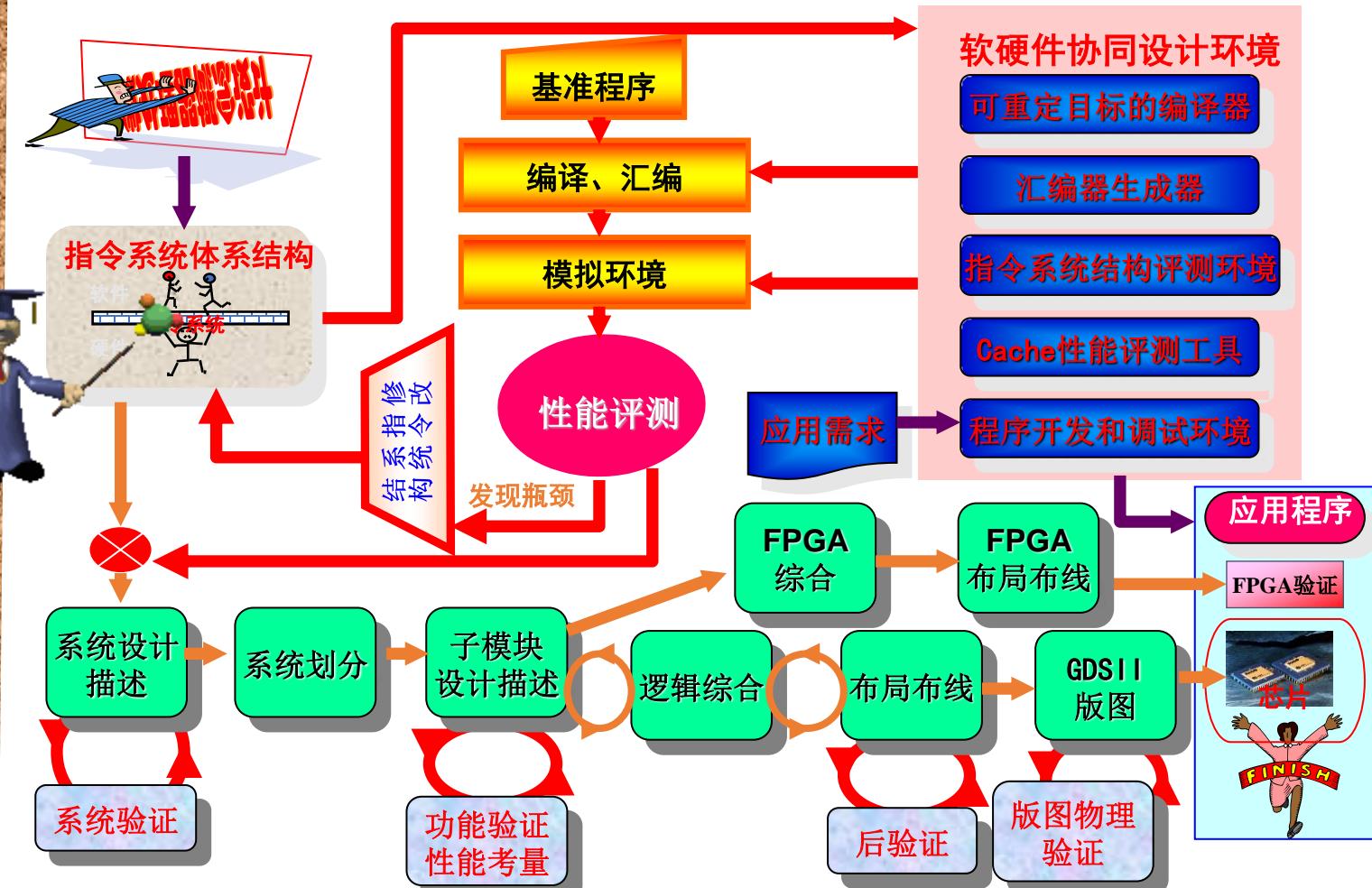
Linux

Mac

x86指令集

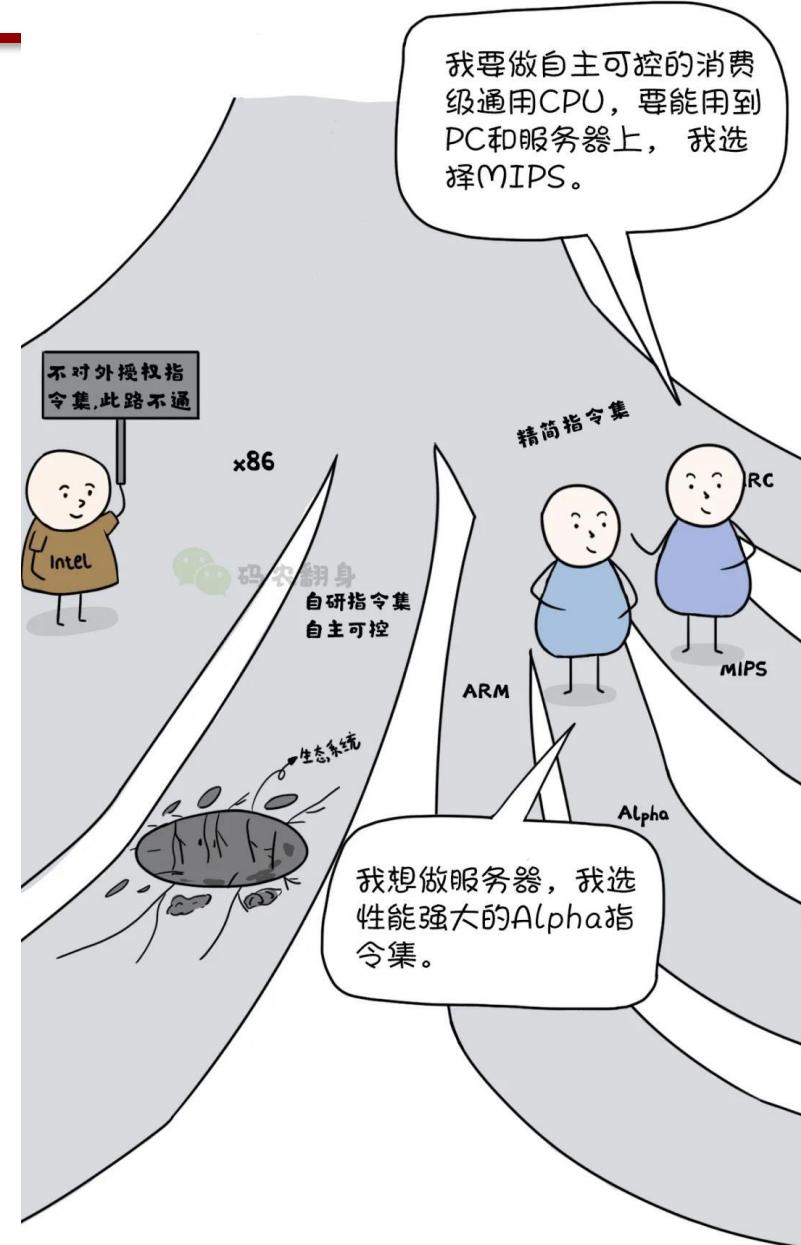
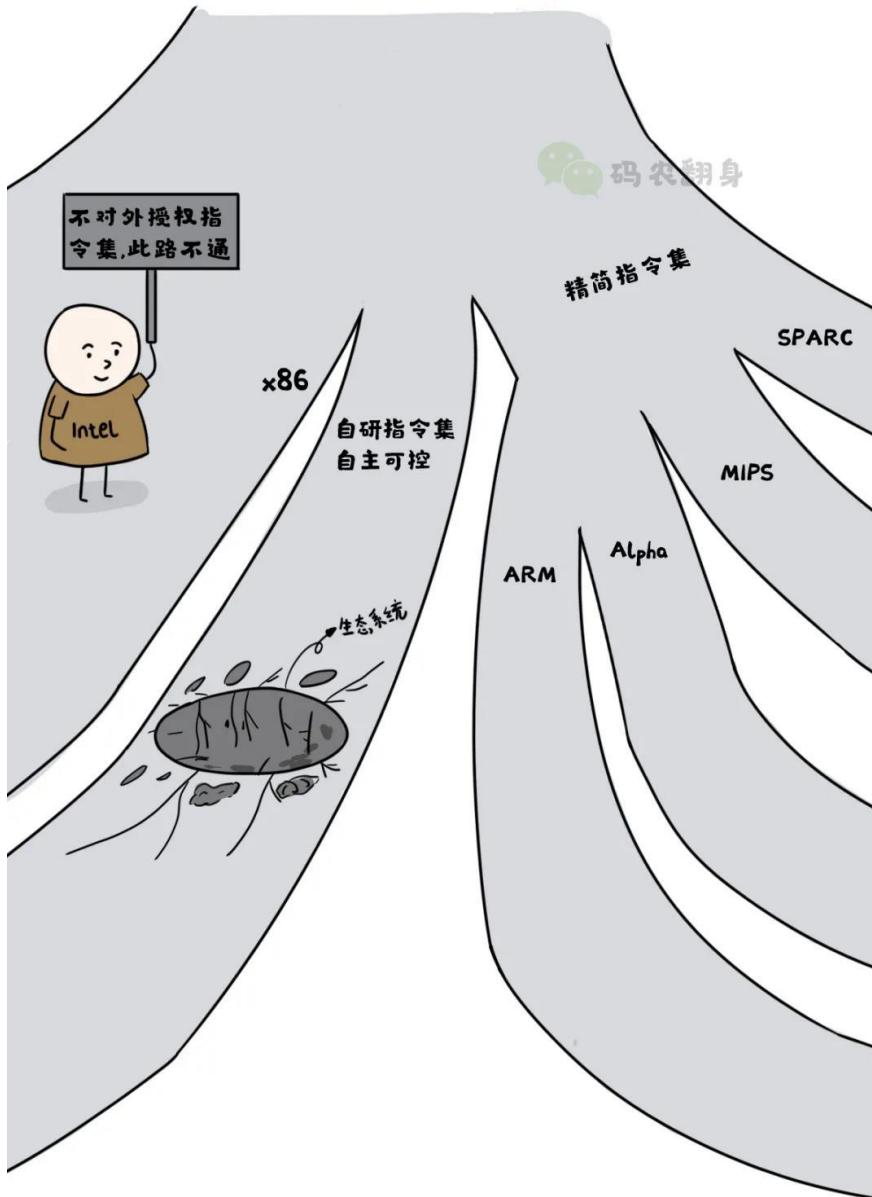
中国芯的发源地

中国第一款正向设计的自主CPU(1999)





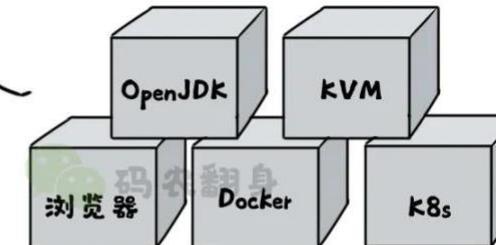
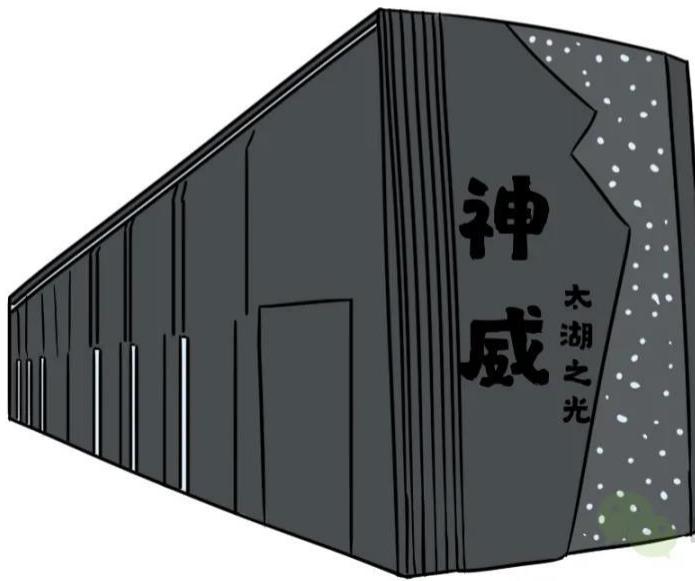
码农翻身





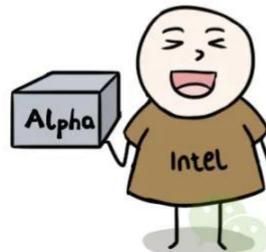
我的SW26010让太湖之光
连续4年在全球TOP500超
算排名第一！

这些产品都移植到了龙芯
平台，欢迎使用！



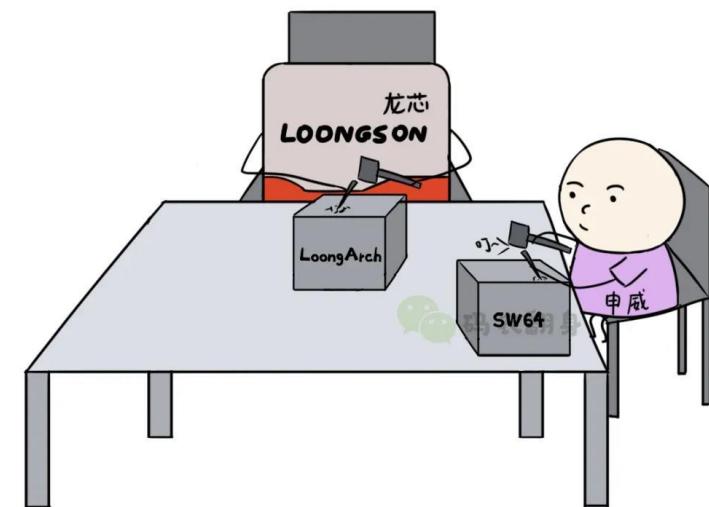


哈哈，最终还是落到了我的手中，你的寿命也到此为止了。



码农翻身

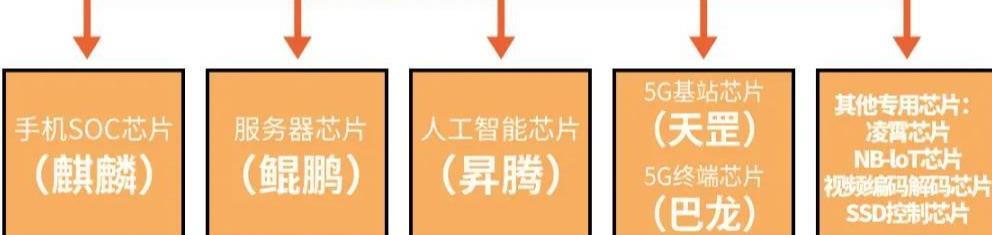
LoongArch是完全自主的指令集，可以兼容MIPS生态，融合x86/ARM指令系统的主要特点，高效支持二进制翻译。

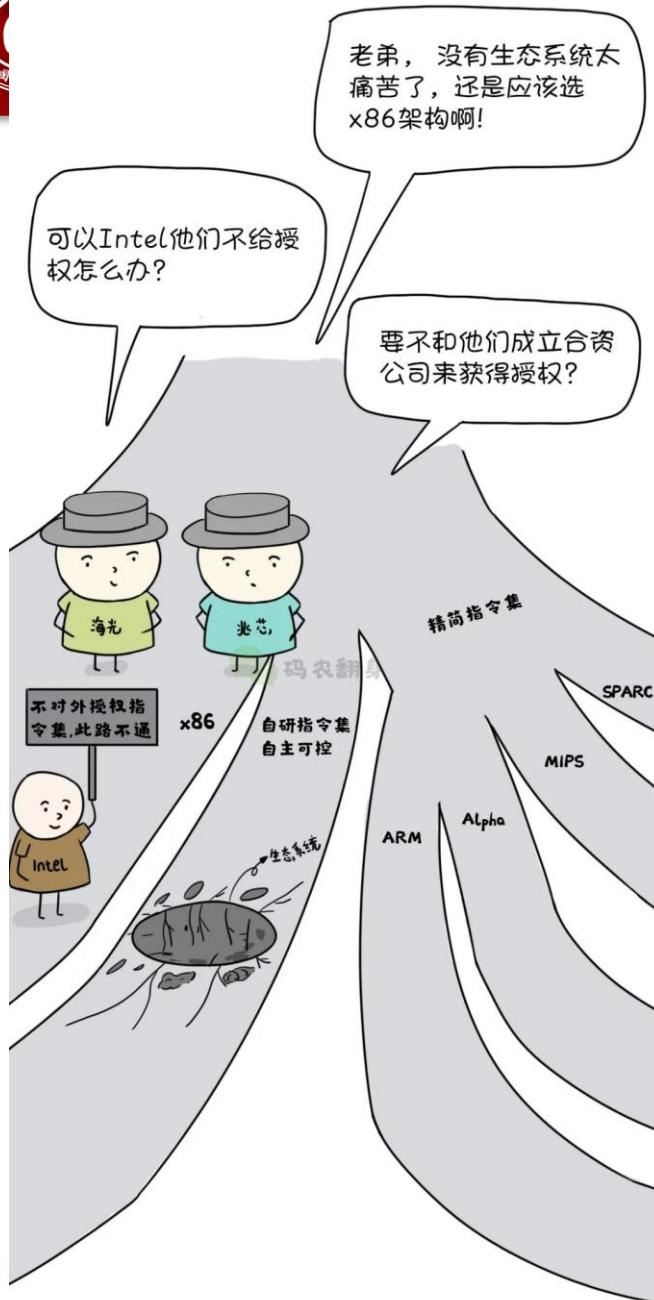


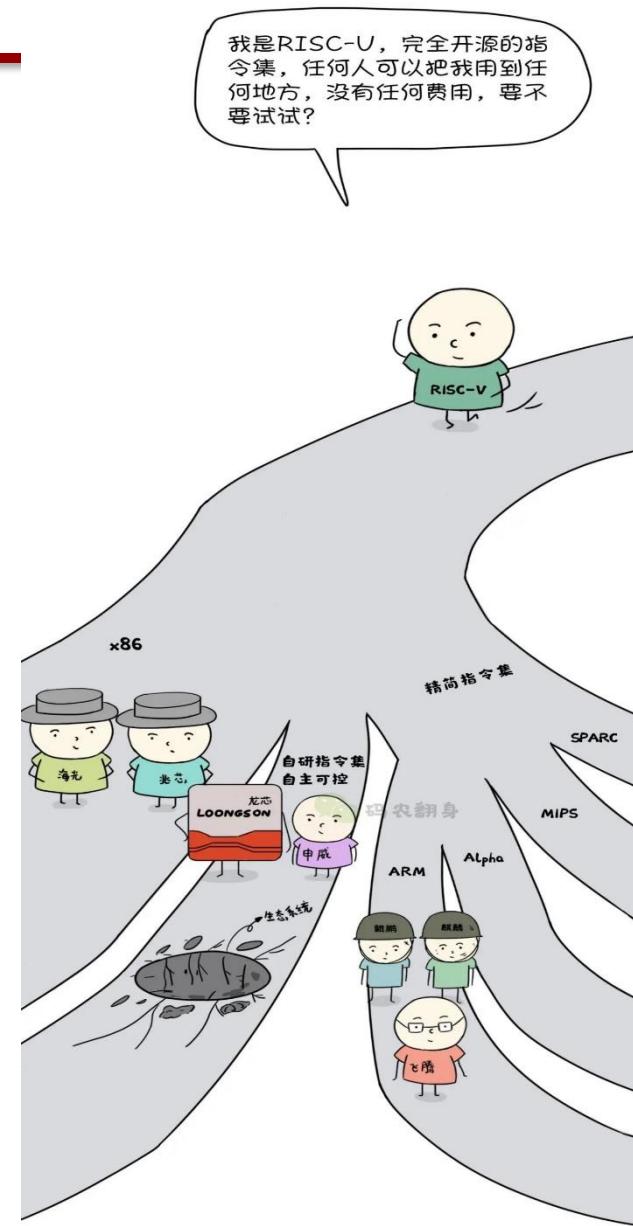
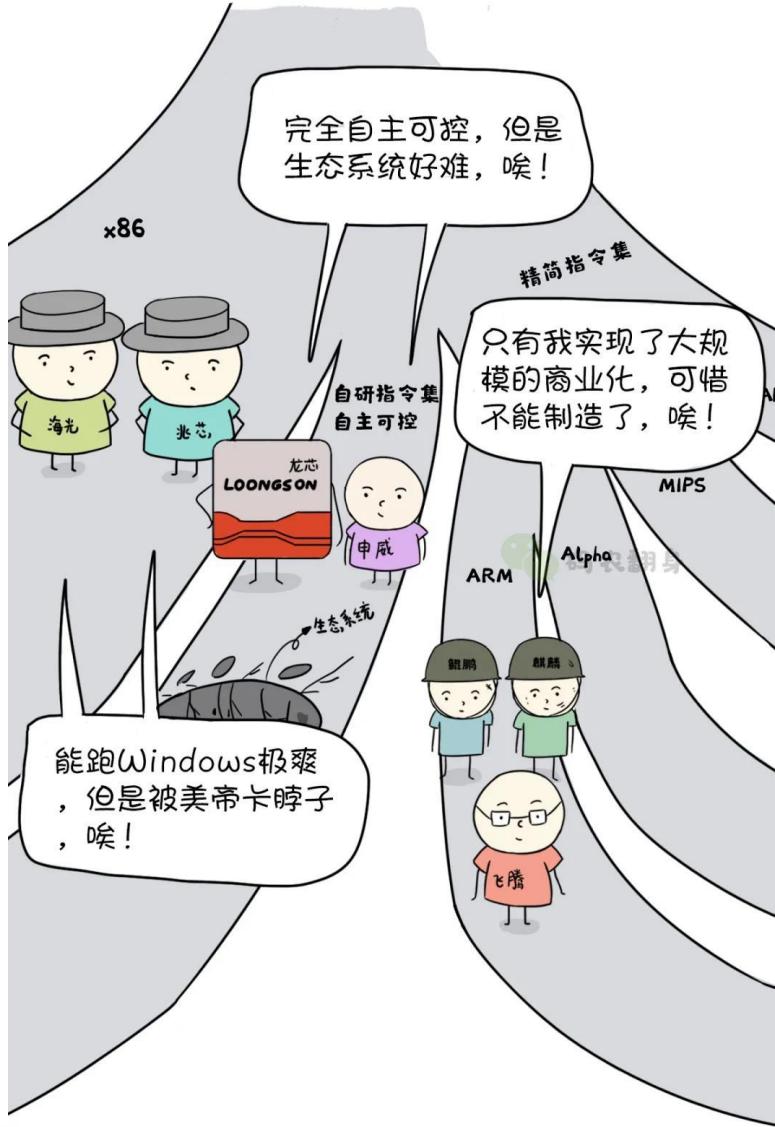
唉，兄弟，太难了，自己的指令集，软件生态又得重来了！



华为芯片全景图









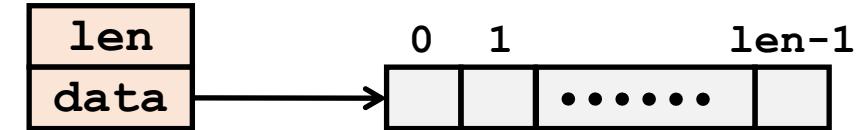
Exploiting Instruction-Level Parallelism

- Need general understanding of modern processor design
 - Hardware can execute multiple instructions in parallel
- Performance limited by data dependencies
- Simple transformations can yield dramatic performance improvement
 - Compilers often cannot make these transformations
 - Lack of associativity and distributivity in floating-point arithmetic



Data Type for Vectors

```
/* data structure for vectors */  
typedef struct{  
    size_t len;  
    data_t *data;  
} vec;
```



• Data Types

- Use different declarations for `data_t`
- `int`
- `long`
- `float`
- `double`

```
/* retrieve vector element  
and store at val */  
int get_vec_element  
(*vec v, size_t idx, data_t *val)  
{  
    if (idx >= v->len)  
        return 0;  
    *val = v->data[idx];  
    return 1;  
}
```



Benchmark Computation

```
void combine1(vec_ptr v, data_t *dest)
{
    long int i;
    *dest = IDENT;
    for (i = 0; i < vec_length(v); i++) {
        data_t val;
        get_vec_element(v, i, &val);
        *dest = *dest OP val;
    }
}
```

Compute sum or product of vector elements

- Data Types

- Use different declarations for `data_t`
- `int`
- `long`
- `float`
- `double`

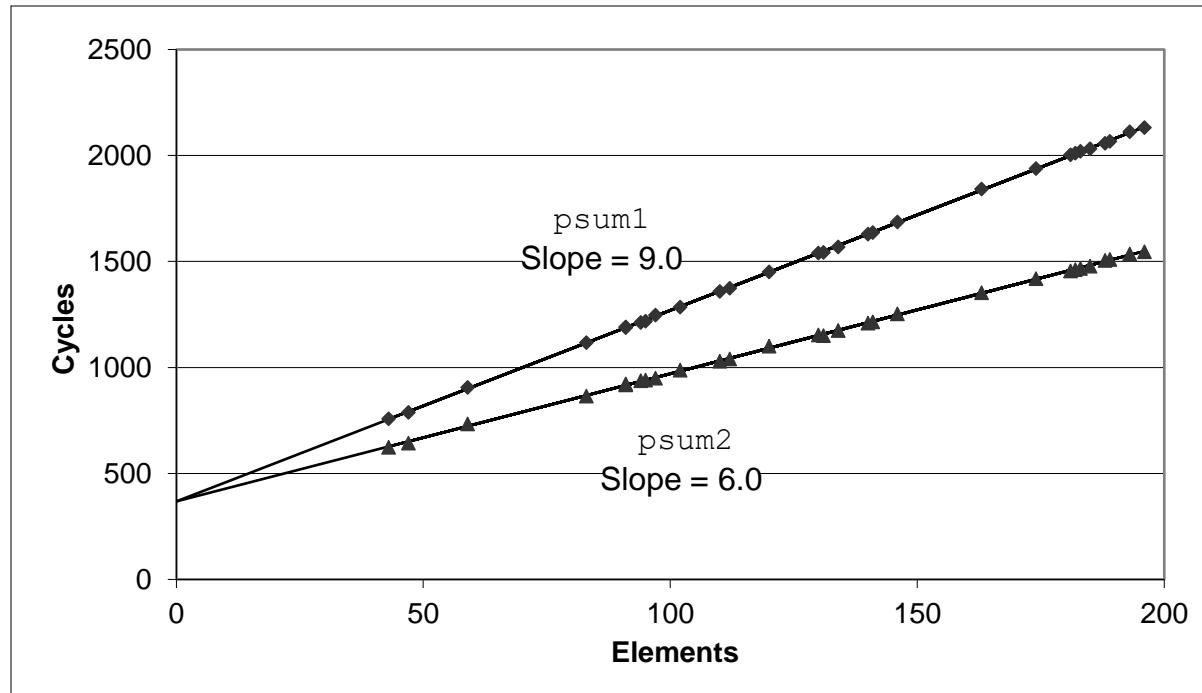
- Operations

- Use different definitions of `OP` and `IDENT`
 - `+` / `0`
 - `*` / `1`



Cycles Per Element (CPE)

- Convenient way to express performance of program that operates on vectors or lists
- Length = n
- In our case: **CPE = cycles per OP**
- $T = \text{CPE} * n + \text{Overhead}$
 - CPE is slope of line





Benchmark Performance

```
void combine1(vec_ptr v, data_t *dest)
{
    long int i;
    *dest = IDENT;
    for (i = 0; i < vec_length(v); i++) {
        data_t val;
        get_vec_element(v, i, &val);
        *dest = *dest OP val;
    }
}
```

Compute sum or product of vector elements

Method	Integer		Double FP	
Operation	Add	Mult	Add	Mult
Combine1 unoptimized	22.68	20.02	19.98	20.18
Combine1 -O1	10.12	10.12	10.17	11.14
Combine1 -O3	4.5	4.5	6	7.8

Results in CPE (cycles per element)



Basic Optimizations

```
void combine4(vec_ptr v, data_t *dest)
{
    long i;
    long length = vec_length(v);
    data_t *d = get_vec_start(v);
    data_t t = IDENT;
    for (i = 0; i < length; i++)
        t = t OP d[i];
    *dest = t;
}
```

- Move `vec_length` out of loop
- Avoid bounds check on each cycle
- Accumulate in temporary



Effect of Basic Optimizations

```
void combine4(vec_ptr v, data_t *dest)
{
    long i;
    long length = vec_length(v);
    data_t *d = get_vec_start(v);
    data_t t = IDENT;
    for (i = 0; i < length; i++)
        t = t OP d[i];
    *dest = t;
}
```

Method	Integer		Double FP	
Operation	Add	Mult	Add	Mult
Combine1 -O1	10.12	10.12	10.17	11.14
Combine4	1.27	3.01	3.01	5.01

- Eliminates sources of overhead in loop



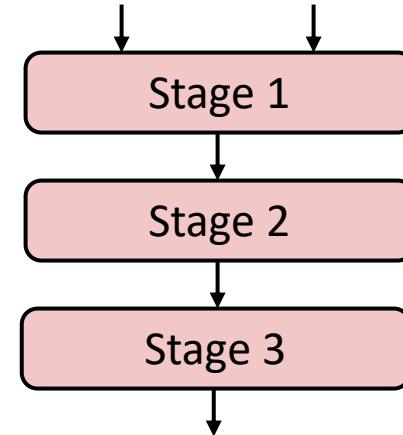
Superscalar Processor

- **Definition:** A superscalar processor can issue and execute *multiple instructions in one cycle*. The instructions are retrieved from a sequential instruction stream and are usually scheduled dynamically.
- **Benefit:** without programming effort, superscalar processor can take advantage of the *instruction level parallelism* that most programs have
 - Most modern CPUs are superscalar.
 - Intel: since Pentium (1993)



Pipelined Functional Units

```
long mult_eg(long a, long b, long c) {  
    long p1 = a*b;  
    long p2 = a*c;  
    long p3 = p1 * p2;  
    return p3;  
}
```



	Time							
	1	2	3	4	5	6	7	
Stage 1	a*b	a*c			p1*p2			
Stage 2		a*b	a*c			p1*p2		
Stage 3			a*b	a*c			p1*p2	

- Divide computation into stages
- Pass partial computations from stage to stage
- Stage i can start on new computation once values passed to $i+1$
- E.g., complete 3 multiplications in 7 cycles, even though each requires 3 cycles



Haswell CPU

- 8 Total Functional Units
- Multiple instructions can execute in parallel
 - 2 load, with address computation
 - 1 store, with address computation
 - 4 integer
 - 2 FP multiply
 - 1 FP add
 - 1 FP divide
- Some instructions take > 1 cycle, but can be pipelined

<i>Instruction</i>	<i>Latency</i>	<i>Cycles/Issue</i>
Load / Store	4	1
Integer Multiply	3	1
Integer/Long Divide	3-30	3-30
Single/Double FP Multiply	5	1
Single/Double FP Add	3	1
Single/Double FP Divide	3-15	3-15



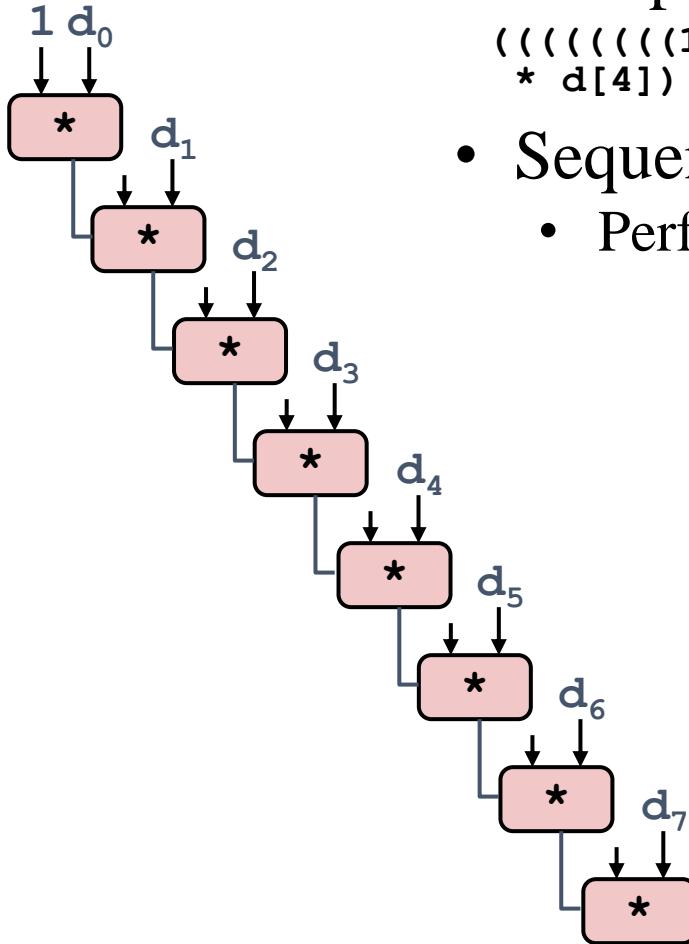
x86-64 Compilation of Combine4

- Inner Loop (Case: Integer Multiply)

```
.L519:                                # Loop:  
    imull (%rax,%rdx,4), %ecx    # t = t * d[i]  
    addq $1, %rdx                # i++  
    cmpq %rdx, %rbp              # Compare length:i  
    jg .L519                     # If >, goto Loop
```

Method	Integer		Double FP	
Operation	Add	Mult	Add	Mult
Combine4	1.27	3.01	3.01	5.01
Latency Bound	1.00	3.00	3.00	5.00

Combine4 = Serial Computation (OP = *)

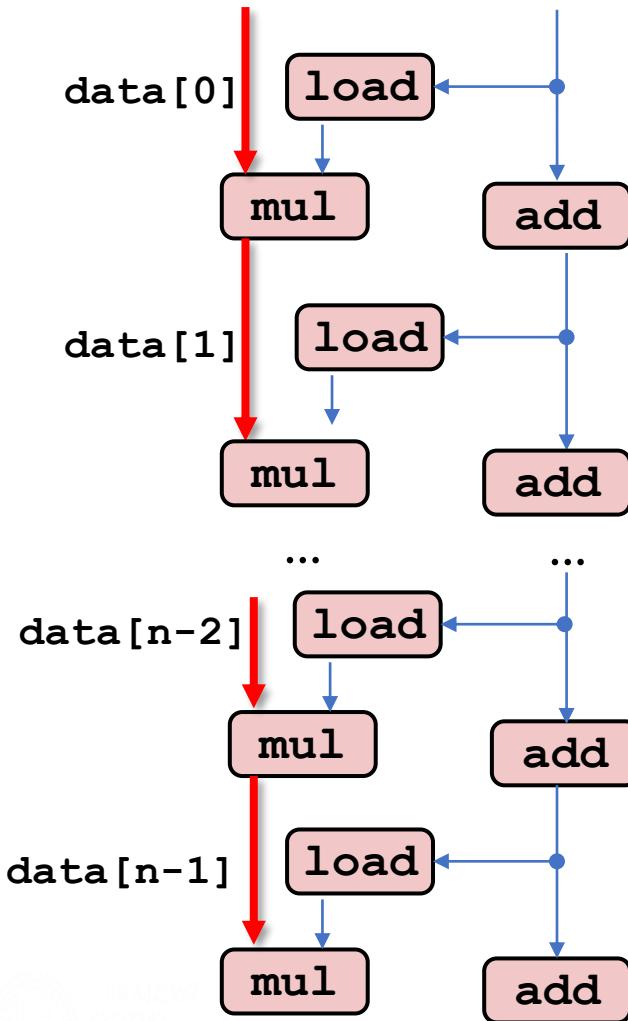


- Computation (length=8)
$$((((((1 * d[0]) * d[1]) * d[2]) * d[3]) * d[4]) * d[5]) * d[6]) * d[7])$$
- Sequential dependence
 - Performance: determined by latency of OP

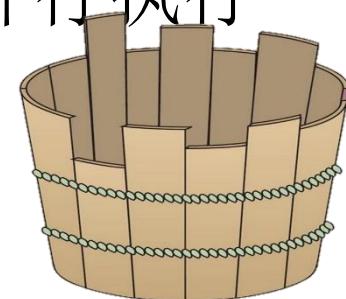


处理器操作的抽象模型

关键路径



- 函数combine4内循环的n次迭代数据流图
 - 两条数据相关链: mul和add对程序值acc和data+i的修改
 - 假设乘法延迟为5个周期，加法延迟为1个周期
 - 左边的链成为关键路径，需要 $5n$ 个周期执行
 - 右边的链需要n个周期执行，不会制约程序性能
- 浮点乘法器成为程序制约资源，其他操作与乘法器并行执行





循环展开Loop Unrolling (2x1)

```
void unroll2a_combine(vec_ptr v, data_t *dest)
{
    long length = vec_length(v);
    long limit = length-1;
    data_t *d = get_vec_start(v);
    data_t x = IDENT;
    long i;
    /* Combine 2 elements at a time */
    for (i = 0; i < limit; i+=2) {
        x = (x OP d[i]) OP d[i+1];
    }
    /* Finish any remaining elements */
    for (; i < length; i++) {
        x = x OP d[i];
    }
    *dest = x;
}
```

- Perform 2x more useful work per iteration



Effect of Loop Unrolling

Method	Integer		Double FP	
	Add	Mult	Add	Mult
Combine4	1.27	3.01	3.01	5.01
Unroll 2x1	1.01	3.01	3.01	5.01
<i>Latency Bound</i>	1.00	3.00	3.00	5.00

- Helps integer add
 - Achieves latency bound
- Others don't improve. *Why?*
 - Still sequential dependency

```
x = (x OP d[i]) OP d[i+1];
```



Loop Unrolling with Reassociation (2x1a)

```
void unroll2aa_combine(vec_ptr v, data_t *dest)
{
    long length = vec_length(v);
    long limit = length-1;
    data_t *d = get_vec_start(v);
    data_t x = IDENT;
    long i;
    /* Combine 2 elements at a time */
    for (i = 0; i < limit; i+=2) {
        x = x OP (d[i] OP d[i+1]);
    }
    /* Finish any remaining elements */
    for (; i < length; i++) {
        x = x OP d[i];
    }
    *dest = x;
}
```

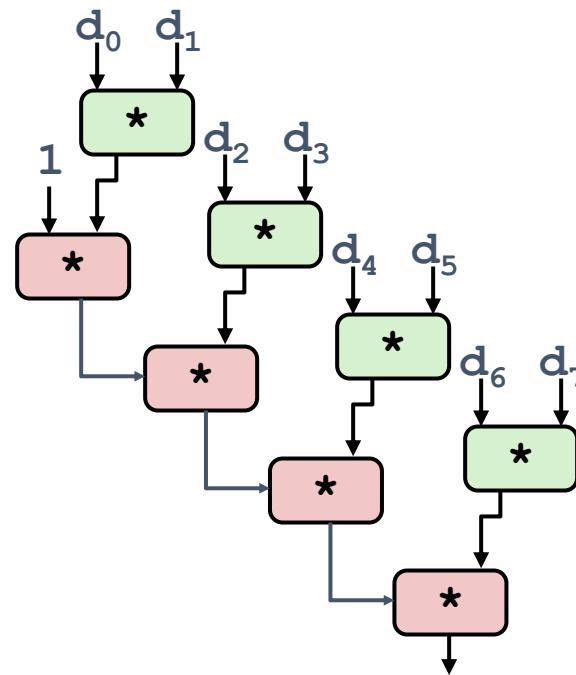
Compare to before

$x = (x \text{ OP } d[i]) \text{ OP } d[i+1];$

- Can this change the result of the computation?
- Yes, for FP. *Why?*

Reassociated Computation

```
x = x OP (d[i] OP d[i+1]);
```



- What changed:
 - Ops in the next iteration can be started early (no dependency)
- Overall Performance
 - N elements, D cycles latency/op
 - $(N/2+1)*D$ cycles:
CPE = D/2



Effect of Reassociation

Method	Integer		Double FP	
Operation	Add	Mult	Add	Mult
Combine4	1.27	3.01	3.01	5.01
Unroll 2x1	1.01	3.01	3.01	5.01
Unroll 2x1a	1.01	1.51	1.51	2.51
<i>Latency Bound</i>	1.00	3.00	3.00	5.00
<i>Throughput Bound</i>	0.50	1.00	1.00	0.50

4 func. units for int +,
2 func. units for load

2 func. units for FP *,
2 func. units for load

- Nearly 2x speedup for Int *, FP +, FP *
- Reason: Breaks sequential dependency

```
x = x OP (d[i] OP d[i+1]);
```



Loop Unrolling with Separate Accumulators (2x2)

```
void unroll2a_combine(vec_ptr v, data_t *dest)
{
    long length = vec_length(v);
    long limit = length-1;
    data_t *d = get_vec_start(v);
    data_t x0 = IDENT;
    data_t x1 = IDENT;
    long i;
    /* Combine 2 elements at a time */
    for (i = 0; i < limit; i+=2) {
        x0 = x0 OP d[i];
        x1 = x1 OP d[i+1];
    }
    /* Finish any remaining elements */
    for (; i < length; i++) {
        x0 = x0 OP d[i];
    }
    *dest = x0 OP x1;
}
```

- Different form of reassociation



Effect of Separate Accumulators

Method	Integer		Double FP	
Operation	Add	Mult	Add	Mult
Combine4	1.27	3.01	3.01	5.01
Unroll 2x1	1.01	3.01	3.01	5.01
Unroll 2x1a	1.01	1.51	1.51	2.51
Unroll 2x2	0.81	1.51	1.51	2.51
<i>Latency Bound</i>	1.00	3.00	3.00	5.00
<i>Throughput Bound</i>	0.50	1.00	1.00	0.50

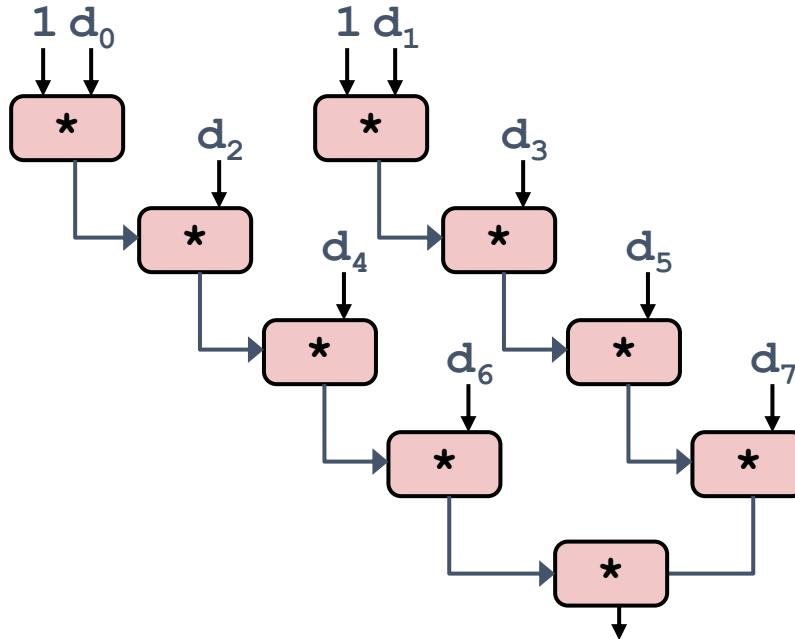
- Int + makes use of two load units

```
x0 = x0 OP d[i];  
x1 = x1 OP d[i+1];
```

- 2x speedup (over unroll2) for Int *, FP +, FP *

Separate Accumulators

```
x0 = x0 OP d[i];  
x1 = x1 OP d[i+1];
```



■ What changed:

- Two independent “streams” of operations

■ Overall Performance

- N elements, D cycles latency/op
- Should be $(N/2+1)*D$ cycles:
CPE = D/2
- CPE matches prediction!

What Now?



Unrolling & Accumulating

- Idea
 - Can unroll to any degree L
 - Can accumulate K results in parallel
 - L must be multiple of K
- Limitations
 - Diminishing returns
 - Cannot go beyond throughput limitations of execution units
 - Large overhead for short lengths
 - Finish off iterations sequentially



Unrolling & Accumulating: Double

- Case

- Intel Haswell
- Double FP Multiplication
- Latency bound: 5.00. Throughput bound: 0.50

Accumulators

FP *	Unrolling Factor L								
K	1	2	3	4	6	8	10	12	
1	5.01	5.01	5.01	5.01	5.01	5.01	5.01	5.01	
2		2.51		2.51		2.51			
3			1.67						
4				1.25		1.26			
6					0.84			0.88	
8						0.63			
10							0.51		
12								0.52	



Unrolling & Accumulating: Int +

- Case

- Intel Haswell
- Integer addition
- Latency bound: 1.00. Throughput bound: 1.00

Int +	Unrolling Factor L								
	K	1	2	3	4	6	8	10	12
1	1.27	1.01	1.01	1.01	1.01	1.01	1.01	1.01	
2		0.81			0.69		0.54		
3			0.74						
4				0.69			1.24		
6					0.56				0.56
8						0.54			
10							0.54		
12								0.56	

Accumulators



Achievable Performance

Method	Integer		Double FP	
Operation	Add	Mult	Add	Mult
Best	0.54	1.01	1.01	0.52
<i>Latency Bound</i>	1.00	3.00	3.00	5.00
<i>Throughput Bound</i>	0.50	1.00	1.00	0.50

- Limited only by throughput of functional units
- Up to 42X improvement over original, unoptimized code



Programming with AVX2

YMM Registers

- 16 total, each 32 bytes
- 32 single-byte integers



- 16 16-bit integers



- 8 32-bit integers



- 8 single-precision floats



- 4 double-precision floats



- 1 single-precision float



- 1 double-precision float

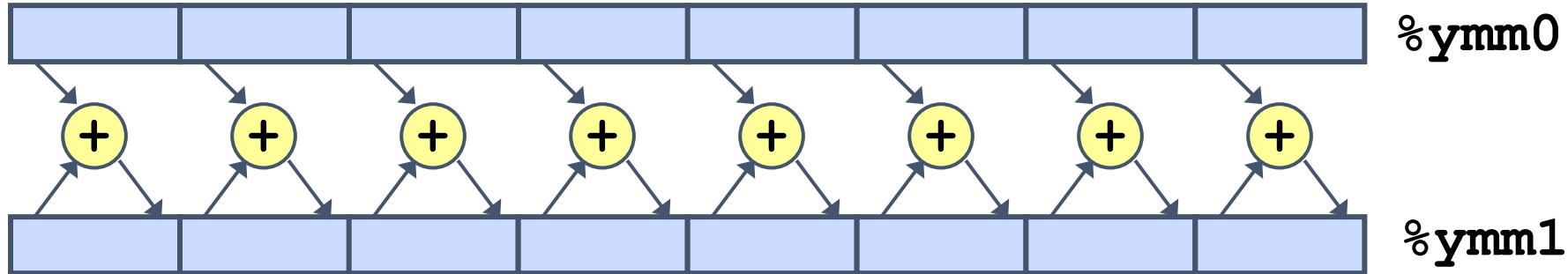




单指令多数据

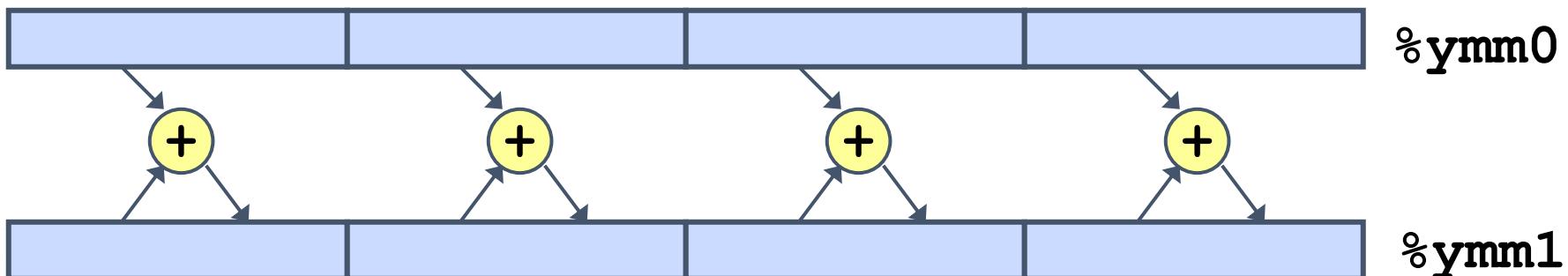
■ SIMD Operations: Single Precision

vaddsd %ymm0, %ymm1, %ymm1



■ SIMD Operations: Double Precision

vaddpd %ymm0, %ymm1, %ymm1





向量指令

Method	Integer		Double FP	
Operation	Add	Mult	Add	Mult
Scalar Best	0.54	1.01	1.01	0.52
Vector Best	0.06	0.24	0.25	0.16
<i>Latency Bound</i>	0.50	3.00	3.00	5.00
<i>Throughput Bound</i>	0.50	1.00	1.00	0.50
<i>Vec Throughput Bound</i>	0.06	0.12	0.25	0.12

- Make use of AVX Instructions
 - Parallel operations on multiple data elements
 - See Web Aside OPT:SIMD on CS:APP web page



What About Branches?

- Challenge
 - Instruction Control Unit must work well ahead of Execution Unit to generate enough operations to keep EU busy

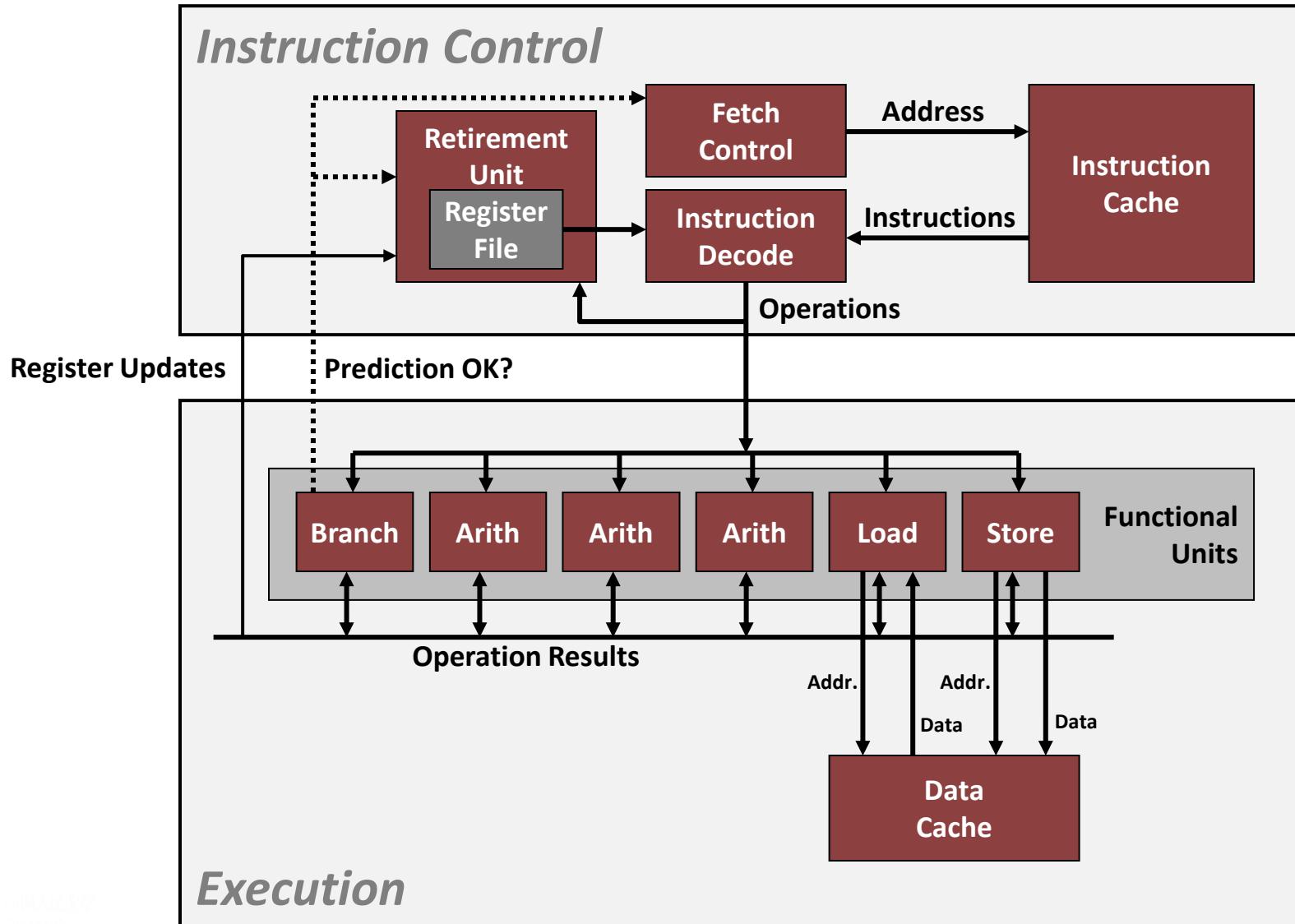
```
404663:    mov      $0x0,%eax
404668:    cmp      (%rdi),%rsi
40466b:    jge      404685
40466d:    mov      0x8(%rdi),%rax
.
.
.
404685:    repz    retq
```

} Executing
How to continue?

- When encounters conditional branch, cannot reliably determine where to continue fetching



Modern CPU Design





Branch Outcomes

- When encounter conditional branch, cannot determine where to continue fetching
 - Branch Taken: Transfer control to branch target
 - Branch Not-Taken: Continue with next instruction in sequence
- Cannot resolve until outcome determined by branch/integer unit

```
404663:    mov      $0x0,%eax
404668:    cmp      (%rdi),%rsi
40466b:    jge      404685
40466d:    mov      0x8(%rdi),%rax
.
.
.
404685:    repz    retq
```

Branch Not-Taken
Branch Taken



Branch Prediction

- Idea
 - Guess which way branch will go
 - Begin executing instructions at predicted position
 - But don't actually modify register or memory data

```
404663: mov    $0x0,%eax
404668: cmp    (%rdi),%rsi
40466b: jge    404685
40466d: mov    0x8(%rdi),%rax
```

. . .

```
404685: repz  retq
```

Predict Taken

} Begin
Execution



Branch Prediction Through Loop

```
401029: vmulsd (%rdx), %xmm0, %xmm0  
40102d: add    $0x8, %rdx  
401031: cmp    %rax, %rdx  
401034: jne    401029
```

i = 98

Assume
vector length = 100

```
401029: vmulsd (%rdx), %xmm0, %xmm0  
40102d: add    $0x8, %rdx  
401031: cmp    %rax, %rdx  
401034: jne    401029
```

i = 99

Predict Taken (OK)

```
401029: vmulsd (%rdx), %xmm0, %xmm0  
40102d: add    $0x8, %rdx  
401031: cmp    %rax, %rdx  
401034: jne    401029
```

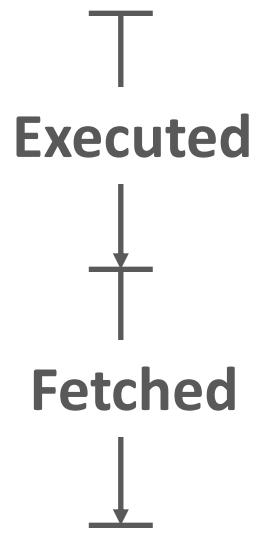
i = 100

Predict Taken
(Oops)

Read
invalid
location

```
401029: vmulsd (%rdx), %xmm0, %xmm0  
40102d: add    $0x8, %rdx  
401031: cmp    %rax, %rdx  
401034: jne    401029
```

i = 101





Branch Misprediction Invalidation

```
401029: vmulsd (%rdx), %xmm0, %xmm0  
40102d: add    $0x8, %rdx  
401031: cmp    %rax, %rdx  
401034: jne    401029      i = 98
```

Assume
vector length = 100

```
401029: vmulsd (%rdx), %xmm0, %xmm0  
40102d: add    $0x8, %rdx  
401031: cmp    %rax, %rdx  
401034: jne    401029      i = 99
```

Predict Taken (OK)

```
401029: vmulsd (%rdx), %xmm0, %xmm0  
40102d: add    $0x8, %rdx  
401031: cmp    %rax, %rdx  
401034: jne    401029      i = 100
```

Predict Taken
(Oops)

```
401029: vmulsd (%rdx), %xmm0, %xmm0  
40102d: add    $0x8, %rdx  
401031: cmp    %rax, %rdx  
401034: jne    401029      i = 101
```

Invalidate



Branch Misprediction Recovery

```
401029:  vmulsd (%rdx), %xmm0, %xmm0
40102d:  add    $0x8,%rdx
401031:  cmp    %rax,%rdx
401034:  jne    401029
401036:  jmp    401040
...
401040:  vmovsd %xmm0, (%r12)
```

i = 99

Definitely not taken

Reload
Pipeline

- Performance Cost
 - Multiple clock cycles on modern processor
 - Can be a major performance limiter



Branch Prediction Numbers

- Default behavior:
 - Backwards branches are often loops so predict taken
 - Forwards branches are often if so predict not taken
- Predictors average better than 95% accuracy
 - Most branches are already predictable.
- Bonus material:
<http://stackoverflow.com/questions/11227809/why-is-processing-a-sorted-array-faster-than-an-unsorted-array>



确信和消除性能瓶颈

程序剖析

- 程序剖析(profiling): 是程序执行时收集性能数据的分析工具，方法是运行程序的一个版本，其中插入了工具代码，以确定程序的各个部分需要多少时间
- GPROF: 给出函数执行时间和调用次数
 1. 为剖析编译和链接程序: 使用-pg选项
 - 例: `gcc -O3 -pg prefixsum.c -o prefixsum`
 2. 执行程序
 - 例: `prefixsum`
 3. 调用GPROF分析
 - 例: `gprof prefixsum`, 剖析报告显示函数执行信息

granularity: each sample hit covers 2 byte(s) for 0.15% of 6.86 seconds					
index	% time	self	children	called	name
[1]	100.0	1.38	5.48	1/1	<spontaneous>
		2.87	0.00		main [1]
		1.70	0.00		psuml [2]
		0.91	0.00		psum2 [3]
[2]	41.9	2.87	0.00	1/1	main [1]
		2.87	0.00	1	psuml [2]
		1.70	0.00	1/1	main [1]
[3]	24.8	1.70	0.00	1	psum2 [3]
		0.91	0.00	1/1	main [1]
[4]	13.2	0.91	0.00	1	psumla [4]



perf监测性能指标

- Perf是用来进行软件性能分析的工具，可以同时分析应用代码和内核，从而全面理解应用程序中的性能瓶颈。
- Perf程序剖析示例：监测rearrange程序branch与cache misses
 - 命令：perf stat -e branches -e branch-misses -e cache-misses ./rearrange

```
[nsrc@localhost ~]$ perf stat -e branches -e branch-misses -e cache-misses ./rearrange
Input length of random array a and b:1000000
Input filter ratio of array:1
numbers of 1:1000000
minmaxl cycles_per_elem:17.6
minmaxl cycles_per_elem: 2.7
predicate branching: Items:1000000, cycles_per_elem: 5.9
predicate branching: Items:1000000, cycles_per_elem: 3.9

Performance counter stats for './rearrange':

      56,337,543      branches
          613,754      branch-misses          #    1.09% of all branches
            3,327      cache-misses

  3.949698873 seconds time elapsed
```

- Perf主要监测指标：perf list

```
[nsrc@localhost ~]$ perf list
List of pre-defined events (to be used in -e):
branch-instructions OR branches           [Hardware event]
branch-misses                           [Hardware event]
bus-cycles                             [Hardware event]
cache-misses                           [Hardware event]
cache-references OR cpu/cache-references [Hardware event]
cpu-cycles OR cycles                   [Hardware event]
instructions                           [Hardware event]
ref-cycles                            [Hardware event]

alignment-faults                      [Software event]
context-switches OR cs                [Software event]
cpu-clock                            [Software event]
cpu-migrations OR migrations         [Software event]
dummy                                 [Software event]
emulation-faults                     [Software event]
major-faults                          [Software event]
minor-faults                         [Software event]
page-faults OR faults                [Software event]
task-clock                           [Software event]

L1-dcache-load-misses                 [Hardware cache event]
L1-dcache-loads                      [Hardware cache event]
L1-dcache-stores                     [Hardware cache event]
L1-icache-load-misses                [Hardware cache event]
LLC-load-misses                      [Hardware cache event]
LLC-loads                            [Hardware cache event]
LLC-store-misses                     [Hardware cache event]
LLC-stores                           [Hardware cache event]
branch-load-misses                   [Hardware cache event]
branch-loads                         [Hardware cache event]
dTLB-load-misses                     [Hardware cache event]
dTLB-loads                           [Hardware cache event]
dTLB-store-misses                   [Hardware cache event]
dTLB-stores                          [Hardware cache event]
iTLB-load-misses                     [Hardware cache event]
iTLB-loads                           [Hardware cache event]
node-load-misses                     [Hardware cache event]
node-loads                           [Hardware cache event]
node-store-misses                   [Hardware cache event]
node-stores                          [Hardware cache event]

branch-instructions OR cpu/branch-instructions/ [Kernel PMU event]
branch-misses OR cpu/branch-misses/           [Kernel PMU event]
bus-cycles OR cpu/bus-cycles/                [Kernel PMU event]
cache-misses OR cpu/cache-misses/             [Kernel PMU event]
cache-references OR cpu/cache-references/   [Kernel PMU event]
cpu-cycles OR cpu/cpu-cycles/                [Kernel PMU event]
cycles-ct OR cpu/cycles-ct/                  [Kernel PMU event]
cycles-t OR cpu/cycles-t/                   [Kernel PMU event]
```



perf监测性能指标

- Perf性能分析：监测程序性能并将其数据保存到perf.data中，使用perf report进行分析。
 - perf record和perf report可以更精确的分析一个应用，perf record可以精确到函数级别。并且在函数里面混合显示汇编语言和代码。
 - 命令：

- ```
perf record -e branches -e branch-misses -e cache-misses ./rearrange
```

```
202.112.117.222 - Xshell 4
Samples: 301 of event 'branches', Event count (approx.): 1000
Overhead Command Shared Object
32.91% rearrange rearrange
19.59% rearrange libc-2.17.so
18.09% rearrange libc-2.17.so
10.08% rearrange libc-2.17.so
5.30% rearrange rearrange
4.39% rearrange rearrange
3.34% rearrange rearrange
1.72% rearrange rearrange
1.66% rearrange rearrange
0.66% rearrange [kernel.kallsyms]
0.38% rearrange [kernel.kallsyms]
0.35% rearrange [kernel.kallsyms]
0.30% rearrange [kernel.kallsyms]
0.28% rearrange [kernel.kallsyms]
0.27% rearrange libc-2.17.so
0.26% rearrange [kernel.kallsyms]
0.09% rearrange [kernel.kallsyms]
0.09% rearrange [kernel.kallsyms]
0.09% rearrange [kernel.kallsyms]
0.08% rearrange [kernel.kallsyms]
0.08% rearrange [kernel.kallsyms]
0.00% perf [kernel.kallsyms]
? p: If you prefer Intel style assembly, try: perf annotate -M intel
已连接 202.112.117.222:2017. SSH2 xterm
? p: If you prefer Intel style assembly, try: perf annotate -M intel
已连接 202.112.117.222:2017. SSH2 xterm 72x25 20,72 1会话
? p: If you prefer Intel style assembly, try: perf annotate -M intel
已连接 202.112.117.222:2017. SSH2 xterm 72x25 19,72 1会话
CAP NUM
```

```
202.112.117.222 - Xshell 4
Samples: 265 of event 'branch-misses', Event count (approx.): 1000
Overhead Command Shared Object
82.36% rearrange rearrange [.] minmaxl
14.23% rearrange rearrange [.] main
1.07% rearrange libc-2.17.so [.]
0.84% rearrange libc-2.17.so [.]
0.38% rearrange libc-2.17.so [.]
0.29% rearrange [kernel.kallsyms] [k] rebalance_domains
0.18% rearrange [kernel.kallsyms] [k] strnlen_user
0.11% rearrange [kernel.kallsyms] [k] prepend_path
0.09% rearrange libc-2.17.so [.]
0.08% rearrange [kernel.kallsyms] [k] get_page_from_freelist
0.07% rearrange [kernel.kallsyms] [k] ktime_get_update_of
0.07% rearrange [kernel.kallsyms] [k] find_vma
0.07% rearrange [kernel.kallsyms] [k] smp_call_function_s
0.07% rearrange [kernel.kallsyms] [k] native_apic_mem_wri
0.06% rearrange [kernel.kallsyms] [k] update_cfs_rq_block
0.04% perf [kernel.kallsyms] [k] perf_event_comm_out
0.01% perf [kernel.kallsyms] [k] perf_pmu_enable
? p: If you prefer Intel style assembly, try: perf annotate -M intel
已连接 202.112.117.222:2017. SSH2 xterm
? p: If you prefer Intel style assembly, try: perf annotate -M intel
已连接 202.112.117.222:2017. SSH2 xterm 72x25 20,72 1会话
CAP NUM
```

```
202.112.117.222 - Xshell 4
Samples: 27 of event 'cache-misses', Event count (approx.): 1000
Overhead Command Shared Object
45.50% rearrange [kernel.kallsyms] [k] get_page_from_freelist
15.20% rearrange libc-2.17.so [.]
12.73% rearrange [kernel.kallsyms] [k] __mod_zone_page_state
9.67% rearrange [kernel.kallsyms] [k] clear_page_c_e
5.49% rearrange [kernel.kallsyms] [k] __rmqueue
2.94% rearrange [kernel.kallsyms] [k] page_fault
2.77% rearrange [kernel.kallsyms] [k] copy_page_rep
2.77% rearrange [kernel.kallsyms] [k] get_pageblock_flags_group
1.18% rearrange [kernel.kallsyms] [k] __list_del_entry
0.43% rearrange rearrange [.]
0.40% rearrange libc-2.17.so [.]
0.40% rearrange libc-2.17.so [.]
0.32% rearrange [kernel.kallsyms] [k] padzero
0.13% rearrange [kernel.kallsyms] [k] perf_event_aux_ctx
0.05% perf [kernel.kallsyms] [k] perf_event_aux.part.48
0.03% perf [kernel.kallsyms] [k] perf_pmu_enable
? p: If you prefer Intel style assembly, try: perf annotate -M intel
已连接 202.112.117.222:2017. SSH2 xterm
? p: If you prefer Intel style assembly, try: perf annotate -M intel
已连接 202.112.117.222:2017. SSH2 xterm 72x25 19,72 1会话
CAP NUM
```



# 代码阅读工具

hash join Project - Source Insight 4.0 - [main.c (C:\documents\...\src)]

File Edit Search Project Options Tools View Window Help

main.c (C:\documents\...\src) X

**main.c**

Symbol Name (Alt+L)

ifndef \_GNU\_SOURCE  
#ifndef \_GNU\_SOURCE  
endif  
include "cpu\_mapping.h" /\* get\_cpu\_id  
include <sched.h> /\* sched\_setaffinity  
include <stdio.h> /\* printf \*/  
include <sys/time.h> /\* gettimeofday  
include <getopt.h> /\* getopt \*/  
include <stdlib.h> /\* exit \*/  
include <string.h> /\* strcmp \*/  
include <limits.h> /\* INT\_MAX \*/  
include <sys/time.h> /\* gettimeofday  
include "rtdsch.h" /\* startTimer, stopTim  
include "no\_partitioning\_join.h" /\* no p  
include "parallel\_radix\_join.h" /\* paralle  
include "generator.h" /\* create\_relatio  
include "pj\_params.h" /\* RELATION\_P  
include "perf\_counters.h" /\* PCM\_x \*/  
include "affinity.h" /\* pthread\_attr\_seta  
include "../config.h" /\* autoconf heade  
if !defined(\_cplusplus)  
getopt  
endif  
RAND\_RANGE  
MALLOC  
algo\_t  
param\_t  
num\_part  
num\_supplier  
num\_customer  
num\_date  
num\_lineorder  
FactColumns  
DimVector  
MeasureIndex  
firstfilterflag  
M1  
M2

\* with --perfconf which specifies which hardware counters to monitor. For  
\* detailed list of hardware counters consult to "Intel 64 and IA-32  
\* Architectures Software Developer's Manual" Appendix A. For an example  
\* configuration file used in the experiments, see <b>'pcm.cfg'</b> file.  
\* Lastly, an output file name with --perfout on commandline can be specified to  
\* print out profiling results, otherwise it defaults to stdout.

\* @subsection systemparams System and Implementation Parameters

\* The join implementations need to know about the system at hand to a certain  
\* degree. For instance #CACHE\_LINE\_SIZE is required by both of the  
\* implementations. In case of no partitioning join, other implementation  
\* parameters such as bucket size or whether to pre-allocate for overflowing  
\* buckets are parametrized and can be modified in 'pj\_params.h'.  
\*

\* On the other hand, radix joins are more sensitive to system parameters and  
\* the optimal setting of parameters should be found from machine to machine to  
\* get the same results as presented in the paper. System parameters needed are  
\* #CACHE\_LINE\_SIZE, #L1\_CACHE\_SIZE and  
\* #L1\_ASSOCIATIVITY. Other implementation parameters specific to radix  
\* join are also important such as #NUM\_RADIX\_BITS  
\* which determines number of created partitions and #NUM\_PASSES which  
\* determines number of partitioning passes. Our implementations support between  
\* 1 and 2 passes and they can be configured using these parameters to find the  
\* ideal performance on a given machine.  
\*

\* @section data Generating Data Sets of Our Experiments

\* Here we briefly describe how to generate data sets used in our experiments  
\* with the command line parameters above.  
\*

\* @subsection workloadB Workload B

\* In this data set, the inner relation R and outer relation S have  $128 \times 10^6$   
\* tuples each. The tuples are 8 bytes long, consisting of 4-byte (or 32-bit)  
\* integers and a 4-byte payload. As for the data distribution, if not  
\* explicitly specified, we use relations with randomly shuffled unique keys  
\* ranging from 1 to  $128 \times 10^6$ . To generate this data set, append the following  
\* parameters to the executable  
\* <tt>mhashjoins</tt>:  
\*

\* @verbatim  
\$ ./mhashjoins [other options] --r-size=128000000 --s-size=128000000  
@endverbatim

\* \note Configure must have run without --enable-key8B.

\* @subsection workloadA Workload A

\* This data set reflects the case where the join is performed between the

Project Files X Project Symbols X

File Name (Ctrl+O)

| File Name              | Directory     | Size |
|------------------------|---------------|------|
| affinity.h             | C:\documents\ | 1    |
| barrier.h              | C:\documents\ | 2    |
| cpu_mapping.c          | C:\documents\ | 1    |
| cpu_mapping.h          | C:\documents\ |      |
| generator.c            | C:\documents\ | 19   |
| generator.h            | C:\documents\ | 3    |
| genzipf.c              | C:\documents\ | 3    |
| genzipf.h              | C:\documents\ |      |
| lock.h                 | C:\documents\ | 1    |
| main.c                 | C:\documents\ | 37   |
| Makefile               | C:\documents\ | 28   |
| mapdql_history.txt     | C:\documents\ | 10   |
| no_partitioning_join.c | C:\documents\ | 61   |
| no_partitioning_join.h | C:\documents\ | 2    |
| pj_params.h            | C:\documents\ |      |
| npi_types.h            | C:\documents\ | 1    |
| parallel_radix_join.c  | C:\documents\ | 53   |
| parallel_radix_join.h  | C:\documents\ | 2    |
| perf_counters.c        | C:\documents\ | 9    |
| perf_counters.h        | C:\documents\ | 2    |
| prj_params.h           | C:\documents\ | 2    |
| rtdsch.h               | C:\documents\ | 1    |
| task_queue.h           | C:\documents\ | 6    |
| types.h                | C:\documents\ | 1    |

Context

Line 175 Col 3 [UTF-8] INS



# Getting High Performance

- Good compiler and flags
- Don't do anything stupid
  - Watch out for hidden algorithmic inefficiencies
  - Write compiler-friendly code
    - Watch out for optimization blockers:  
procedure calls & memory references
    - Look carefully at innermost loops (where most work is done)
- Tune code for machine
  - Exploit instruction-level parallelism
  - Avoid unpredictable branches
  - Make code cache friendly (Covered later in course)



预祝同学们：  
考得都会  
蒙的都对  
新年快乐

相约2026《人工智能计算系统》