Shashwat Shrivastava

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EDUCATION

IIIT HYDERABAD
B.Tech. and M.S. by Research
Electronics and Communication
Expected Graduation: 2021
Cumulative GPA: 8.63/10

RELEVANT COURSES

Advanced Computer Architecture
Deep Neural Networks
Digital VLSI
Complex Digital System Design
Information Theory and Coding

ACHIEVEMENTS

- Dean's List-3 for semester 3.
- Dean's List-2 for semester 6.
- Dean's List-1 for semester 7.

POSITIONS

- **Teaching Assistant** for Embedded Hardware Design.
  Intro to Internet of Things
  Technology Product Entrepreneurship
  Intro to Processor Architecture
  Intro to Psychology
- **Pulsation Coordinator** 2019, an umbrella term for Electronics related events in Institute's Annual Festival, Felicity.
- **Sports Coordinator** for the year 2018-19.
- **Member IIITH Cricket Team**.

SKILLS

PROGRAMMING
Day to Day:
•C•C++•Python•Bluespec System Verilog•Matlab•Verilog•OpenCL•HLS
Familiar:
•Shell

TECHNOLOGIES
•Arduino•FPGA•Machine Learning•AWS F1 FPGA

WORK EXPERIENCE

GOOGLE SUMMER OF CODE STUDENT | ROBOCOMP
May 2019 - August 2019 | C++, Qt, OpenSceneGraph

- The aim of this project was to build an interactive robotic simulator where modifications of the environment is possible during the simulation time.

BLUESPEC INC | Research Intern
May 2018-July 2018 | Mysore, India

- Worked under Bluespec India Head, Mr. Niraj Sharma, to explore various hardware architectures for dense matrix multiplier to maximize throughput without compromising on-chip area.
- Extended the work by integrating Hardware Accelerator with RISC-V processor Piccolo Master, a 3 stage pipelined CPU.

INTEL LABS | Research Intern
Jan 2021 - June 2021 | FPGA

- Working as a research intern at Intel's Processor Architecture Lab on the software and hardware side of an FPGA accelerator for 3D image segmentation.

RESEARCH EXPERIENCE

COMPUTING SYSTEMS GROUP May 2018-Present | Hyderabad, India

- Pursuing research under Prof. Suresh Purini on accelerating image processing algorithms and Convolutional Neural Networks on FPGA.

PROJECTS

FINGERPRINT RECOGNITION ON FPGA USING INCEPTION NET | Research Project| Machine Learning| Bluespec System Verilog | OpenCL

- Building a Fingerprint Recognition System on AWS F1 FPGA where host code uses OpenCL APIs to send data to DDR Memory over PCIe. Subsequently, the RTL kernel interacts with memory through AXI4 Lite and internally uses AXI4 stream. The proposed recognition system will use Inception-v4 Net along with fingerprint domain knowledge to extract fingerprint features and subsequently perform fingerprint matching on the cloud.

OBJECT DETECTION ON FPGA | VLSI| Image Processing| Bluespec System Verilog

- Designed a fully pipelined architecture for real-time object detection on FPGA using Block-based Subtraction Method.

PUBLICATIONS

- **S. Shrivastava**, Z. Choudhury, S. Khandelwal and S. Purini, "FPGA Accelerator for Stereo Vision using Semi-Global Matching through Dependency Relaxation," 2020 30th International Conference on Field-Programmable Logic and Applications (FPL), Gothenburg, Sweden, 2020, pp. 304-309
- S. Khandelwal, Z. Choudhury, **S. Shrivastava** and S. Purini, "Accelerating Local Laplacian Filters on FPGAs," 2020 30th International Conference on Field-Programmable Logic and Applications (FPL), Gothenburg, Sweden, 2020, pp. 109-114