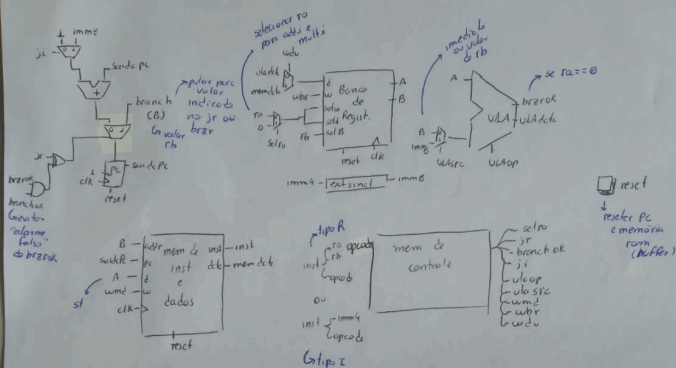
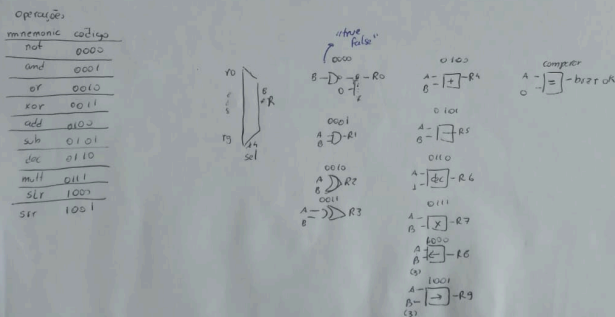


# DATAPATH DO PROCESSADOR



## DIAGRAMA DE CAIXAS ULA



## MEMORIA DE CONTROLE

opcode	mnemonic	wdu	wbr	wmd	lascr	uloop	ji	branchok	jr	sel ro
0000	brzr	0	0	0	0	0011	0	1	0	0
0001	ji	0	0	0	1	0100	1	0	0	0
0010	ld	1	1	0	0	0100	0	0	0	0
0011	st	0	0	1	0	0100	0	0	0	0
0100	addi	0	1	0	1	0100	0	0	0	1
0101	multi	0	1	0	1	0111	0	0	0	1
0110	dec	0	1	0	0	0110	0	0	0	0
0111	jr	0	0	0	0	0100	0	0	1	0
1000	not	0	1	0	0	0000	0	0	0	0
1001	and	0	1	0	0	0001	0	0	0	0
1010	or	0	1	0	0	0010	0	0	0	0
1011	xor	0	1	0	0	0011	0	0	0	0
1100	add	0	1	0	0	0100	0	0	0	0
1101	sub	0	1	0	0	0101	0	0	0	0
1110	slr	0	1	0	0	1000	0	0	0	0
1111	srr	0	1	0	0	1001	0	0	0	0