IXYS

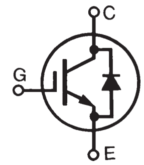
Advance Technical Information

GenX3™ 1200V IGBT w/ Diode

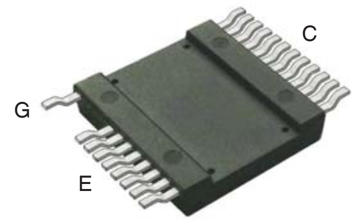
MMIX1G120N120A3V1

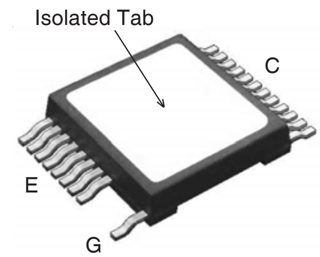
V_{CES} = 1200V
I_{C110} = 105A
$V_{CE(sat)}$ ≤ 2.2V

(Electrically Isolated Tab)



Ultra-Low-Vsat PT IGBT for
3kHz Switching





G = Gate E = Emitter
C = Collector

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	1200	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	1200	V
V_{GES}	Continuous	±20	V
V_{GEM}	Transient	±30	V
I_{C25}	T_C = 25°C	220	A
I_{C110}	T_C = 110°C	105	A
I_{CM}	T_C = 25°C, 1ms	700	A
SSOA (RBSOA)	V_{GE} = 15V, T_{VJ} = 125°C, R_G = 1Ω Clamped Inductive Load	I_{CM} = 240 @ 0.8 • V_{CES}	A
P_C	T_C = 25°C	400	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6 mm (0.062 in.) from Case for 10	260	°C
V_{ISOL}	50/60Hz, 1 minute	2500	V~
F_C	Mounting Force	50..200/11..45	N/lb.
Weight		8	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 250μA, V_{GE} = 0V	1200			V
$V_{GE(th)}$	I_C = 1mA, V_{CE} = V_{GE}	3.0		5.0	V
I_{CES}	V_{CE} = V_{CES}, V_{GE} = 0V			50	μA
	Note 2, T_J = 125°C			5	mA
I_{GES}	V_{CE} = 0V, V_{GE} = ± 20V			±100	nA
$V_{CE(sat)}$	I_C = 100A, V_{GE} = 15V, Note 1		1.85	2.20	V
	T_J = 125°C		1.95		V

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 2500V~ Electrical Isolation
- Optimized for Low Conduction losses
- Square RBSOA
- Anti-Parallel Ultra Fast Diode
- High Current Handling Capability

Advantages

- High Power Density
- Low Gate Drive Requirement

Applications

- Power Inverters
- UPS
- Motor Drives
- SMPS
- PFC Circuits
- Battery Chargers
- Welding Machines
- Lamp Ballasts
- Inrush Current Protection Circuits

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Min.	Typ.	Max.	
g_{fs}	I_C = 60A, V_{CE} = 10V, Note 1	45	73		S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		9900		pF
C_{oes}			655		pF
C_{res}			240		pF
Q_g	I_C = 120A, V_{GE} = 15V, V_{CE} = 0.5 • V_{CES}		420		nC
Q_{ge}			70		nC
Q_{gc}			180		nC
$t_{d(on)}$	**Inductive load, T_J = 25°C** I_C = 100A, V_{GE} = 15V V_{CE} = 960V, R_G = 1Ω Note 3		40		ns
t_{ri}			67		ns
E_{on}			10		mJ
$t_{d(off)}$			490		ns
t_{fi}			325		ns
E_{off}			33		mJ
$t_{d(on)}$	**Inductive load, T_J = 125°C** I_C = 100A, V_{GE} = 15V V_{CE} = 960V, R_G = 1Ω Note 3		30		ns
t_{ri}			75		ns
E_{on}			15		mJ
$t_{d(off)}$			685		ns
t_{fi}			680		ns
E_{off}			58		mJ
R_{thJC}				0.31	°C/W
R_{thCS}			0.05		°C/W
R_{thJA}			30		°C/W

Reverse Diode (FRED)

Symbol	Test Conditions (TJ = 25°C Unless Otherwise Specified)	Min.	Typ.	Max.	
V_F	I_F = 100A, V_{GE} = 0V, Note 1			1.8	V
I_{RM}	I_F = 50A, V_{GE} = 0V, $-di_F/dt$ = 200A/μs, V_R = 300V		20		A
t_{rr}			700		ns
R_{thJC}				0.50	°C/W

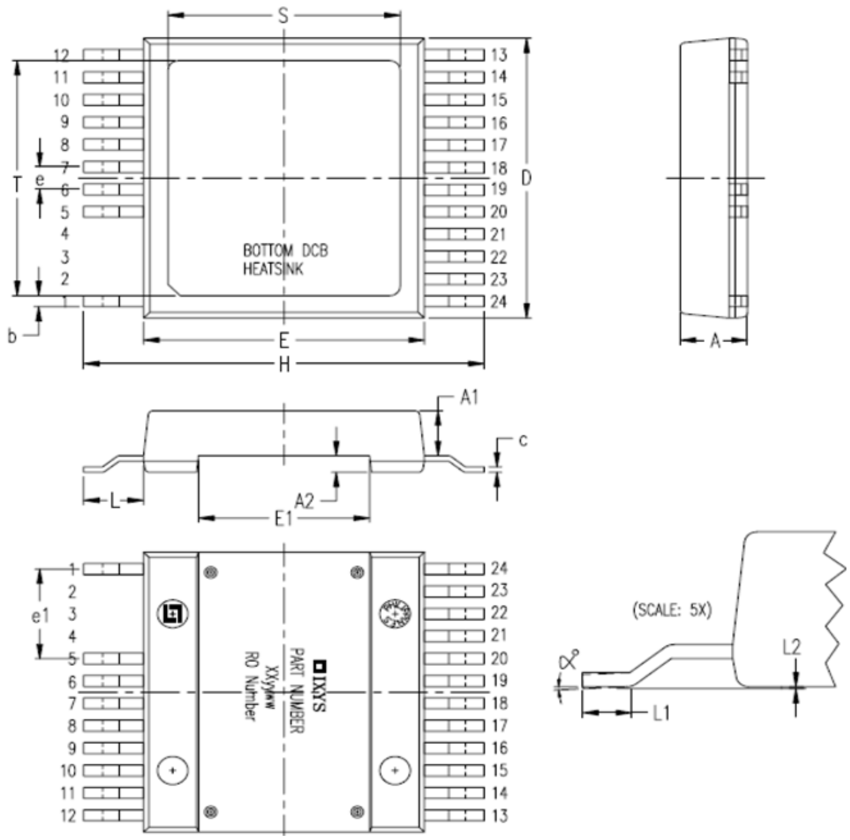
Notes:

1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.
2. Part must be heatsunk for high-temp Ices measurement.
3. Switching times & energy losses may increase for higher V_{CE}(Clamp), T_J or R_G.

ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

Package Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.209	.224	5.30	5.70
A1	.154	.161	3.90	4.10
A2	.055	.063	1.40	1.60
b	.035	.045	0.90	1.15
c	.018	.026	0.45	0.65
D	.976	.994	24.80	25.25
E	.898	.915	22.80	23.25
E1	.543	.559	13.80	14.20
e	.079 BSC		2.00 BSC	
e1	.315 BSC		8.00 BSC	
H	1.272	1.311	32.30	33.30
L	.181	.209	4.60	5.30
L1	.051	.067	1.30	1.70
L2	.000	.006	0.00	0.15
S	.736	.760	18.70	19.30
T	.815	.839	20.70	21.30
α	0	4°	0	4°

PIN: 1 = Gate
5-12 = Emitter
13-24 = Collector

Fig. 1. Output Characteristics @ T_J = 25ºC

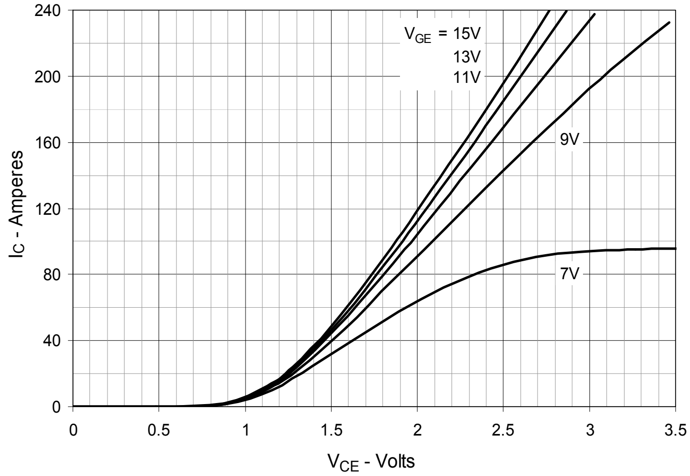


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

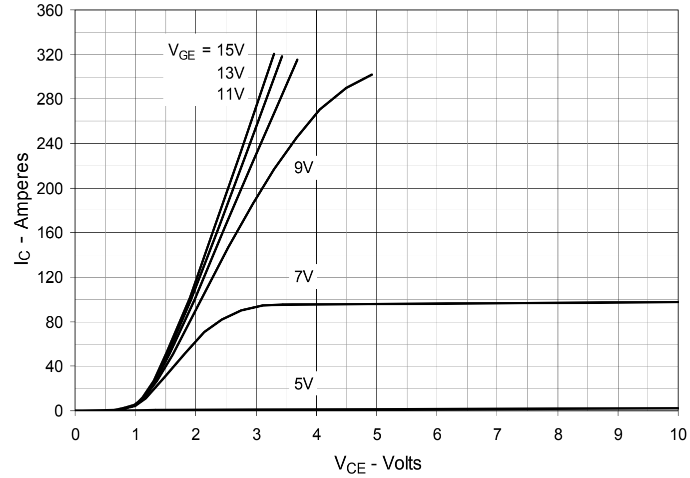


Fig. 3. Output Characteristics @ T_J = 125ºC

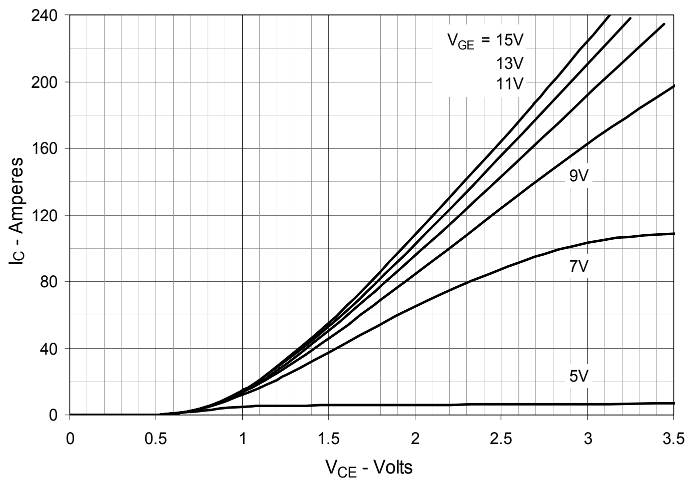


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

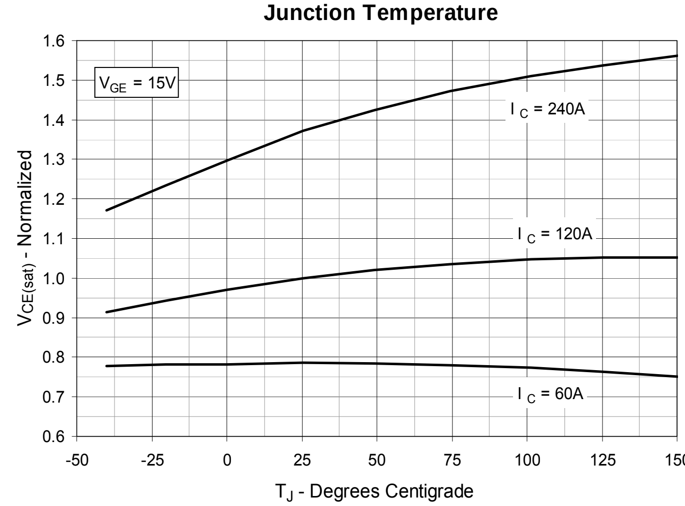


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

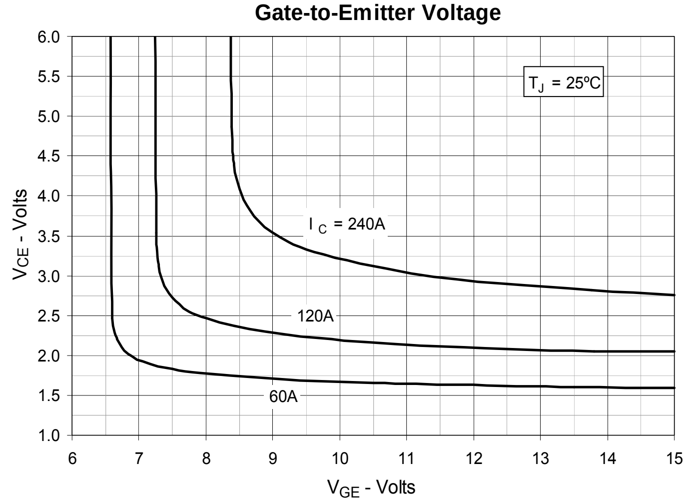
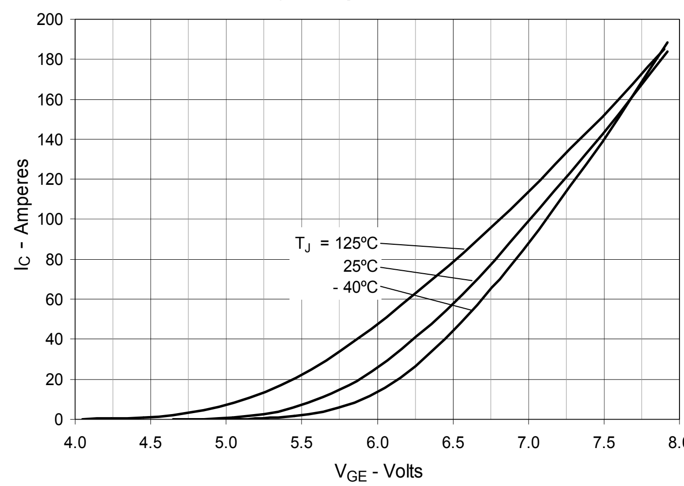


Fig. 6. Input Admittance



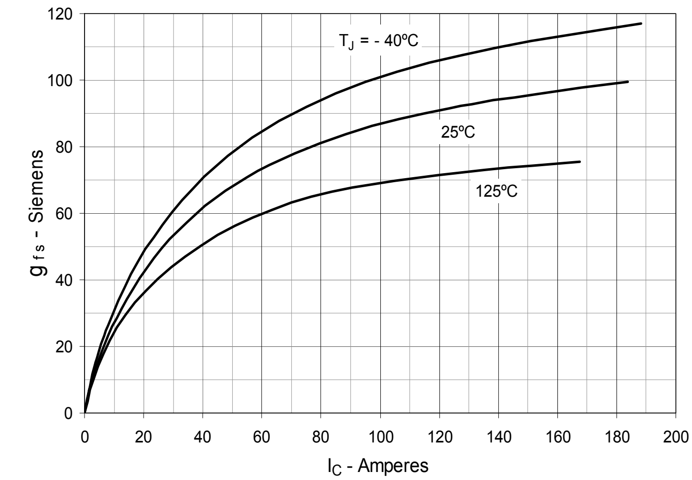


Fig. 7. Transconductance

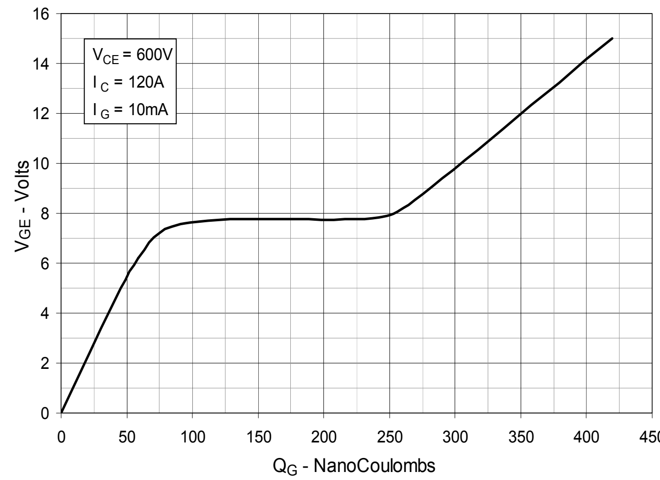


Fig. 8. Gate Charge

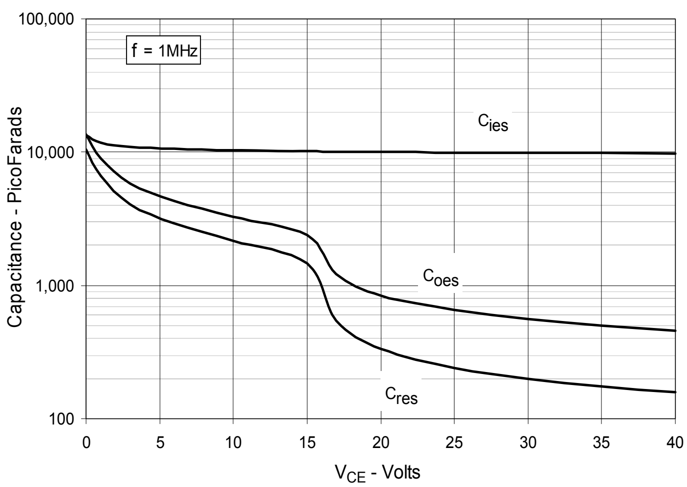


Fig. 9. Capacitance

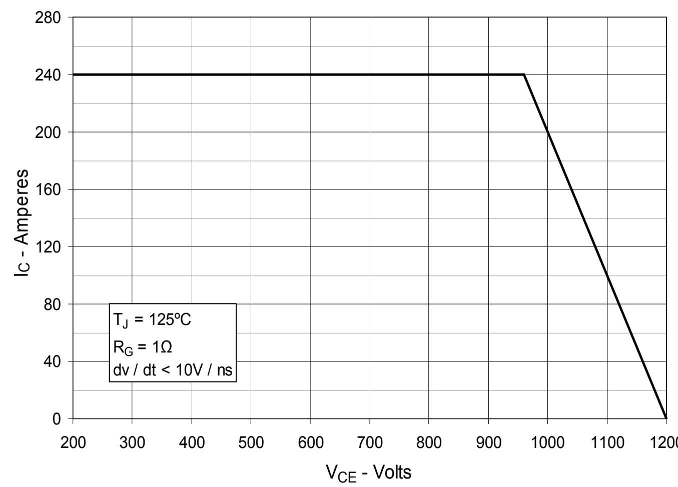


Fig. 10. Reverse-Bias Safe Operating Area

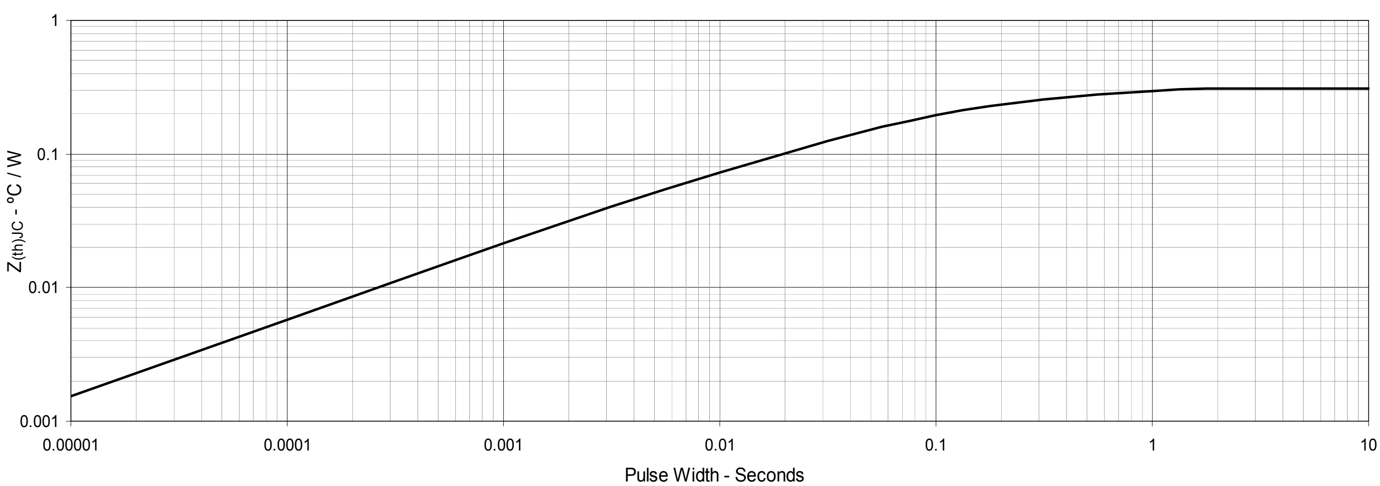


Fig. 11. Maximum Transient Thermal Impedance

Fig. 12. Inductive Switching Energy Loss vs. Gate Resistance

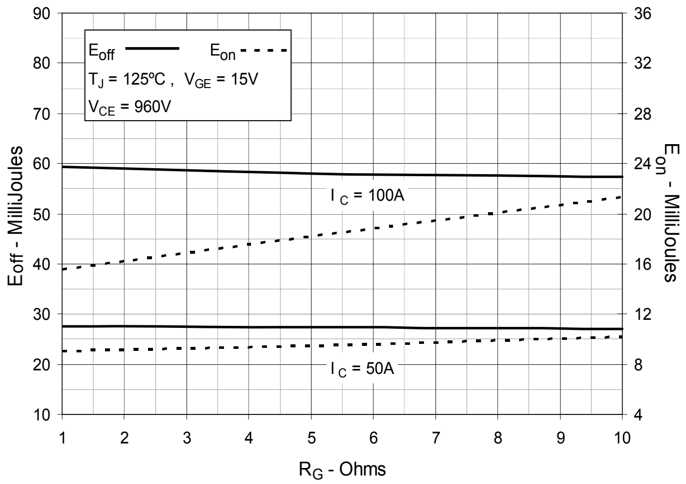


Fig. 13. Inductive Switching Energy Loss vs. Collector Current

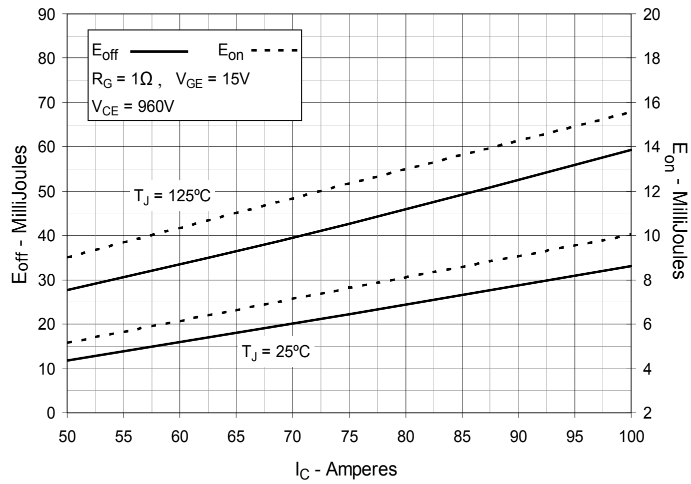


Fig. 14. Inductive Switching Energy Loss vs. Junction Temperature

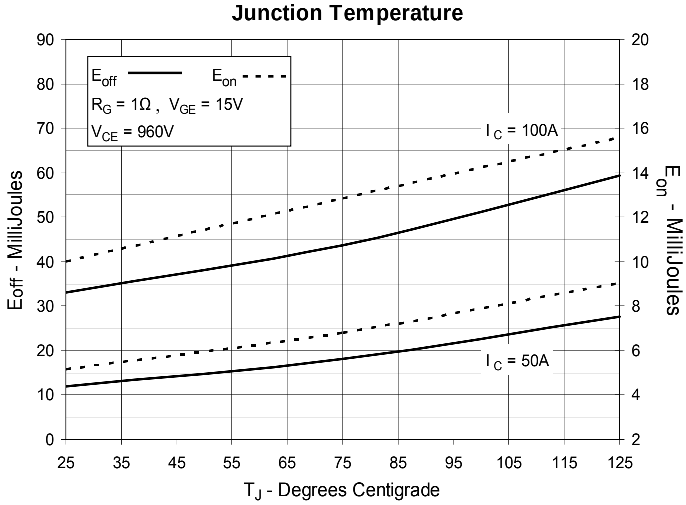


Fig. 15. Inductive Turn-off Switching Times vs. Gate Resistance

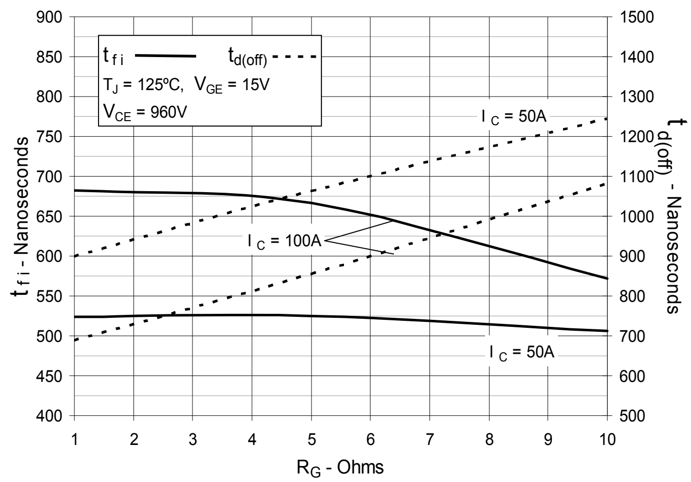


Fig. 16. Inductive Turn-off Switching Times vs. Collector Current

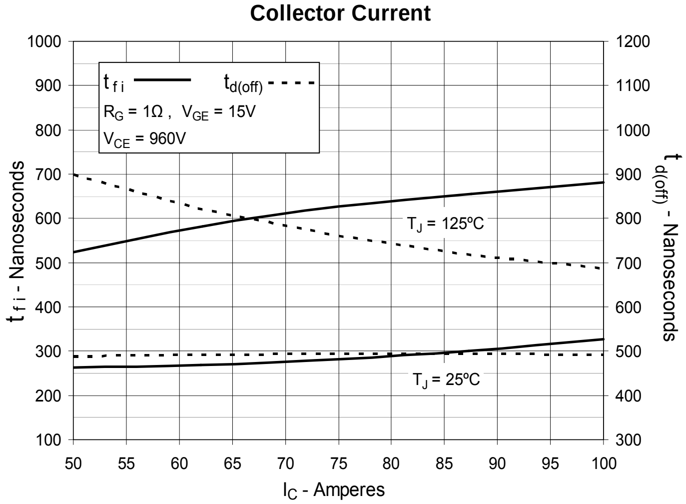


Fig. 17. Inductive Turn-off Switching Times vs. Junction Temperature

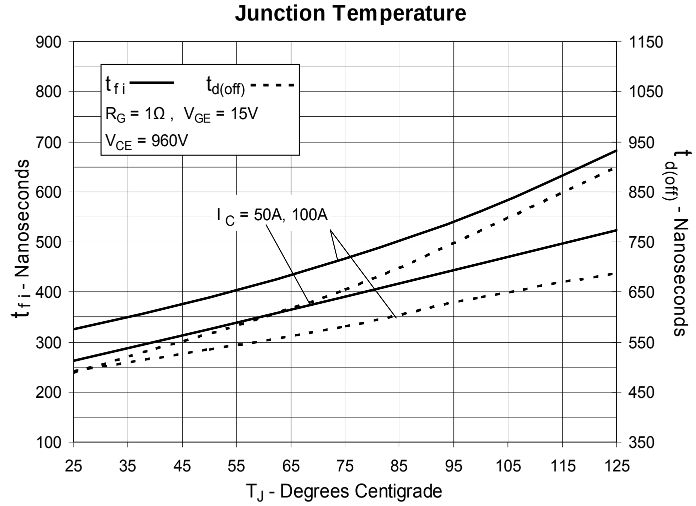


Fig. 18. Inductive Turn-on Switching Times vs. Gate Resistance

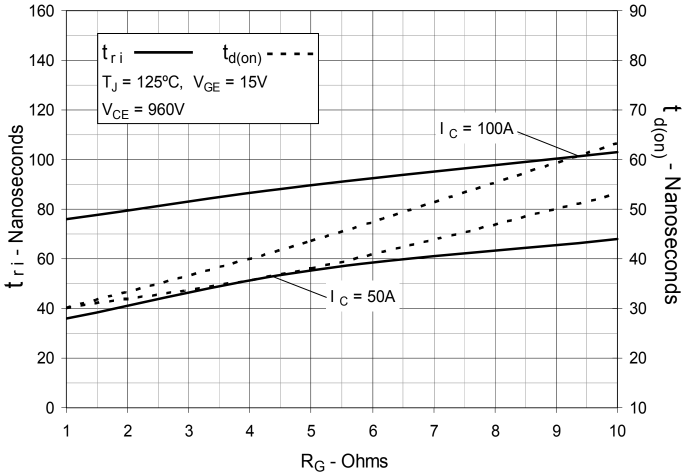


Fig. 19. Inductive Turn-on Switching Times vs. Collector Current

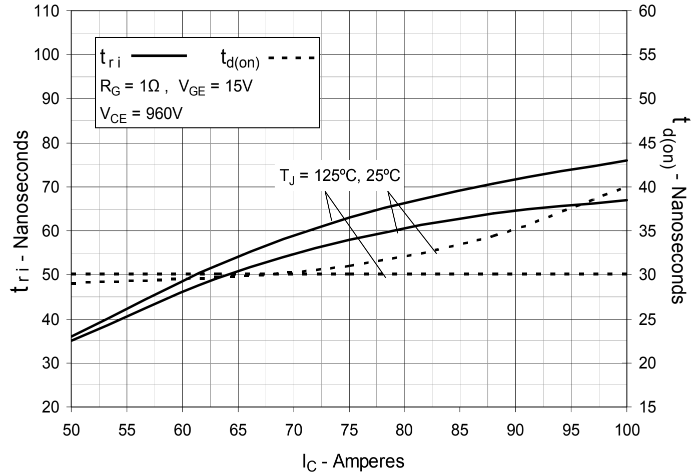


Fig. 20. Inductive Turn-on Switching Times vs. Junction Temperature